DESIGN AND ANALYSIS OF FIRST AND SECOND ORDER K-DELTA-1-SIGMA MODULATORS IN MULTIPLE FABRICATION PROCESSES

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ABSTRACT

Analog to digital converters (ADC) are an important category of electronic circuits that are required in order to convert real-world analog signals into the digital domain. One of the main trade-offs in ADC design is between data conversion speed and resolution. Delta Sigma ADCs are commonly used for high precision data conversion of low bandwidth signals such as those found in audio, industrial and biomedical applications. A major disadvantage of traditional Delta Sigma ADC architectures is that they have limited signal bandwidth and are not suited for high speed applications such as communication systems. The continuous time K-Delta-1-Sigma (KD1S) modulator designed and implemented in this thesis offers a solution to this problem by using time interleaving with and multiple feedback paths to increase the effective sampling rate.

Four different 1st and 2nd order continuous time KD1S modulators were extensively designed and simulated. These KD1S modulators were implemented in two different processes, a 0.5 µm CMOS process and a 0.35 µm SiGe BiCMOS process. All designs utilize 8 feedback paths (delta) and therefore have the required 8 phase shifted clocks. The main parameters that were simulated are signal-to-noise ratio (SNR), effective number of bits (ENOB), bandwidth and power consumption. These simulations were performed using a combination of LTSpice, and MATLAB. Overall, the 2nd order KD1S modulators have better performance than the 1st order designs across both processes.

The 2nd order KD1S modulator implemented in the 0.35 µm process has the best performance and was physically laid out using the Cadence Virtuoso suite. This design had an SNR of 76.73 dB with a 500 KHz input signal, which corresponds to an ENOB of 12.45 bits. This

resolution was achieved with a bandwidth of 1.92 MHz and an effective sampling rate of 983 MHz with a power consumption of 35.7 mW.

ACKNOWLEDGEMENTS

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CHAPTER 1: INTRODUCTION

Signals found in nature including sound, light and pressure are analog signals. In order to collect and process these naturally occurring signals by microprocessors in the digital domain, the data must be converted into its digital representation. This conversion is usually done using analog-to-digital converters (ADC). The role of data converters is crucial as digital electronics are dominating circuits, and their demand is constantly increasing in today's world [1]. This growing demand in turn requires data converters to improve in terms of performance, which is why data converters come in different topologies with each topology being better at a certain aspect for a specified application. Analog-to-digital converters can be the determining factor of a circuit's operation as it can limit the performance of a circuit; for example, in terms of speed or accuracy. Therefore, ADC design is important and needs to engulf different conditions to comply with the overall circuit application.

1.1 ADC Specifications

Analog-to-digital converters take an input signal that contains an infinite number of values. These values need to be quantized to a digital word with a limited number of N bits [1]. The number of bits in a digital word relates to the number of 2^N quantization levels, and these levels can determine the resolution of the converter. Resolution of a converter is the smallest difference the converter can resolve before switching into another level [1].

A block diagram of an ADC is presented in Figure 1.1, the figure shows the analog input signal and its respective representation as a digital word. The bits in the digital word are organized left to right from the Most Significant Bit (MSB) to Least Significant Bit (LSB). The output word can be related to the input signal as in Equation 1.1 [1].

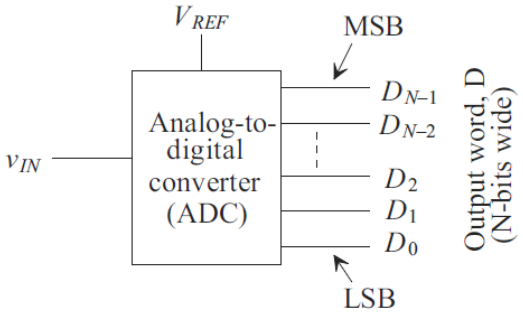

Figure 1.1 – Analog to Digital Converter block diagram [1]

$$v_{IN} = \frac{V_{REF}}{2^N}(D_0 + 2 \cdot D_1 + 4 \cdot D_2 + 8 \cdot D_3 + \ldots + 2^{N-2} \cdot D_{N-2} + 2^{N-1} \cdot D_{N-1})$$

$$v_{IN} = \sum_{n=0}^{N-1} D_n \cdot 2^n \cdot \frac{V_{REF}}{2^N} \tag{1.1}$$

1.2 ADC Architectures

Analog-to-digital converters come in different architectures to suite different type of applications. The architectures can be grouped into two categories, Nyquist-rate and oversampling. The main difference between the two categories lies in the process used to execute the conversion. Some Nyquist-rate ADC topologies include flash ADC, pipeline ADC, and successive approximation (SAR) ADC [3], [4]. On the other hand, most common oversampling ADC is the delta-sigma ADCs [3]. The commonly used ADC topologies will be briefly explained in this chapter with indication of their benefits and disadvantages.

1.2.1 FLASH ADC

Flash converters use $2^N - 1$ comparators based on the number of quantization levels needed, and 2^N resistors to form a resistor ladder as seen in Figure 1.2. The analog input voltage is compared to a reference value and results in a thermometer output code. The output produces more 1's when the input value is higher than the reference [1]. The main advantage of flash converters is speed as the input results in a digital word output at each clock cycle, therefore the conversion happens instantly after one comparator delay [1]. The disadvantage is area size as the area doubles for each one-bit increase in resolution. Due to the comparators, the converter possesses high input capacitance, and consumes large amount of power from the number of high-speed comparators. Due to area size flash converters area usually limited to 8-bit resolution [1].

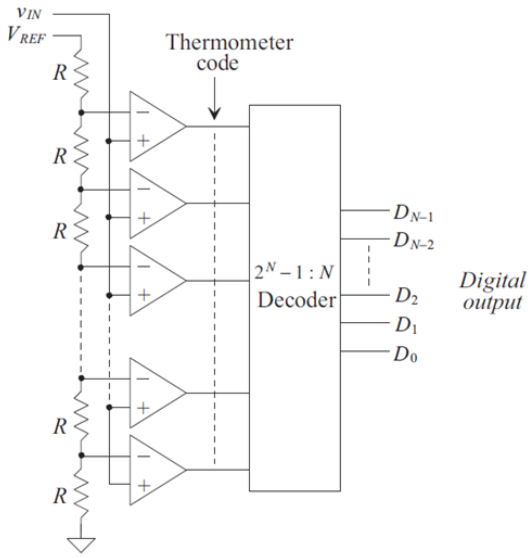

Figure 1.2 – Flash ADC block diagram [1]

1.2.2 PIPELINE ADC

Pipeline ADC converts the input in *N*-steps proportional to the number of bits. Each bit is converted in one stage such that every clock cycle, a new stage would be free to operate on a new

sample. [1]. The conversion process is carried in a certain manner depending on a comparison that occurs between the sampled value and a reference value [1]. Due to the nature of its process, the pipeline ADC is considered to operate by under-sampling and using multiple stages [5]. Therefore, the advantages of pipeline ADCs include speed since each stage takes care of one bit, and high resolution as this architecture can reach 10-13 bits of resolution [1]. The drawback from pipeline ADC topology is latency as *N*-stages are required to form an output. Moreover, error propagation can be a concern as each stage depends on the accuracy of the prior stage. Figure 1.3 shows a block diagram of a pipeline ADC (the figure changes depending on the number of bits).

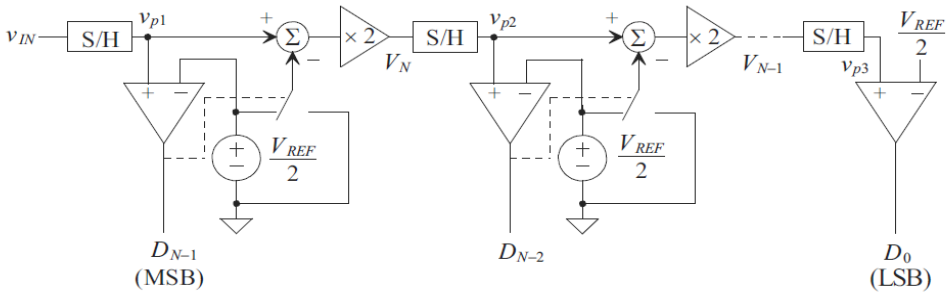

Figure 1.3 – Pipeline ADC block diagram [1]

1.2.3 INTEGRATING ADC

Integrating ADCs convert an analog signal to a digital word by performing integration on the input and comparing the integration time using a digital counter [1]. Two types of integrating ADCs are the single, and dual slope. The more slopes present in the integrating ADC, the more precise the ADC will be with the cost of longer conversion time. Single slope ADCs operate by integrating a reference voltage and comparing the result to a sampled input signal while a counter counts the number of clock pulses needed for the two compared values to be equal. The number of clock pulses corresponds to the actual input value; on the other hand, the counter output is the digital word representation of the analog input. ADC block diagram is seen in Figure 1.4.

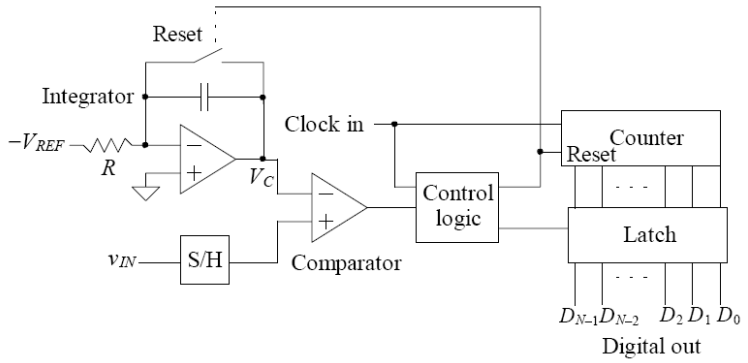

Figure 1.4 – Single-slope ADC block diagram [1]

Dual slope integrating ADCs perform two integrations on both the input and the reference voltage value. The first integration is a ramp-up charging period that depends on the input with a fixed time, and the second integration is a ramp-down discharging period that depends on the reference voltage value with a variable time. Counter calculates the number of clock pulses needed for the integrator to discharge to zero. The number of clock pulses corresponds to the input value and the counter output is the actual digital output [1]. The advantages of the integrating ADCs are high resolution of 12-16 bits, and low production cost [6]. The disadvantage of this ADC architecture would be the slow conversion rate. Block diagram of the ADC is shown in Figure 1.5.

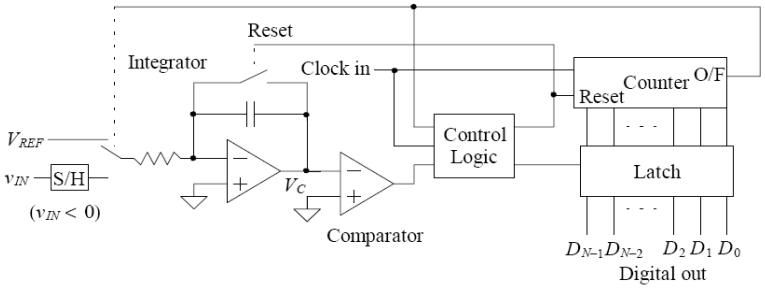

Figure 1.5 - Dual-slope ADC block diagram [1]

1.2.4 SUCCESSIVE APPROXIMATION (SAR) ADC

Successive Approximation ADC (SAR) achieves the conversion by doing a binary search through all the possible quantization levels before reaching the final digital word [4]. The analog input is

sampled and compared to a DAC output, and the comparison result controls the binary search. The output of the comparator is directly latched in the SAR register as seen in Figure 1.6, which is how the binary search directed. Using the previously mentioned iterative process the signal generated from the SAR register approximates the analog input value [4]. One of the advantages of using a SAR ADC are low power consumption as the architecture uses only one comparator. Also, the SAR takes a small layout area, and can reach a resolution of 16-bits. The disadvantage of using SAR ADC would speed as one clock cycle is needed for every bit conversion [6].

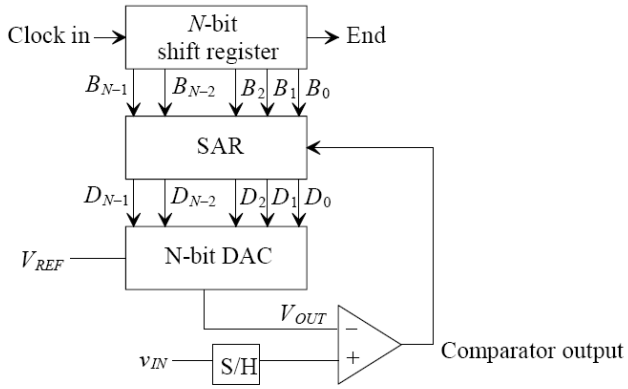

Figure 1.6 - SAR ADC block diagram [1]

1.2.5 DELTA-SIGMA ADC

In the delta-sigma ADC, quantization of the input signal happens using a modulator, and a digital filter. The modulator (Figure 1.7) uses a method called delta-sigma modulation where the output is a pulse density modulated signal with an average representing the input signal over a specific period [1]. The modulator consists of an integrator, a comparator (ADC), and a DAC in the feedback as shown in Figure 1.7. Moreover, the digital filter takes the modulator's bit stream output, and encodes the output into multi-level digital data. The delta-sigma modulator (DSM) is called oversampling because the modulator samples the input signal at a rate much higher than the highest frequency within the input bandwidth [1].

The advantages of delta-sigma ADCs are high resolution ranging from 12-24 bits, the ability to convert low level signals, and low production cost. Further, oversampling and averaging in the ADC allows for simple analog circuitry, which results in low power consumption. The disadvantage of the delta-sigma ADC is having low conversion bandwidth.

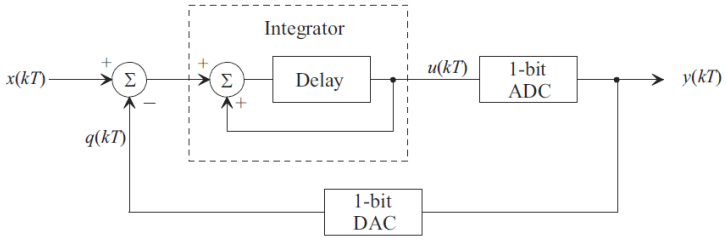

Figure 1.7 – Block diagram of a delta-sigma modulator [1]

The following table summarizes the overall advantages and disadvantages for some of the mentioned ADCs as these topologies are the most common. The resolution ranges of each architecture are also included in Table 1.1.

ADC TYPE	Advantages	Disadvantages	Resolution
Pipeline ADC	High speed High Bandwidth	Low resolution Data latency High Power Expensive	Up to 16 bits
SAR ADC	No cycle latency High accuracy Low power ease of use	Sample rate limited	Up to 16 bits
Delta-Sigma ADC	High resolution High stability Low cost Low power	Low speed Cycle latency	12-24 bits

Table 1.1 - ADC architecture advantages [1], [5]

1.3 ADC APPLICATIONS

The nature of a circuit where an analog to digital conversion is needed determines the characteristics required for the ADC. Knowing the advantages and disadvantages of the different ADC topologies, the appropriate architecture can be selected. For instance, ADCs can be picked based on their resolution and bandwidth capabilities. Other specifications that can guide the selection process are included in Table 1.1. Figure 1.8 presents different ADC applications in their resolution and bandwidth ranges, while Figure 1.9 shows the ADC architecture in their appropriate regions. Looking at these two figures, choosing an ADC can be made less challenging. A tradeoff is always present in ADCs, which is why the application for the converter is important since a favorable aspect of the ADC can be far more essential so that the drawbacks are acceptable.

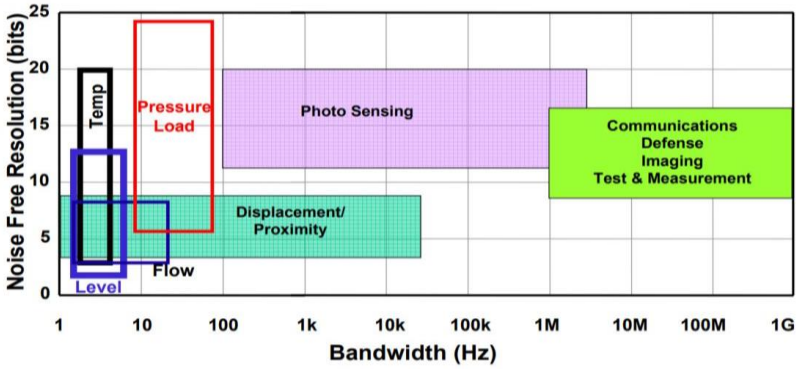

Figure 1.8 – Common applications vs. Bandwidth [5]

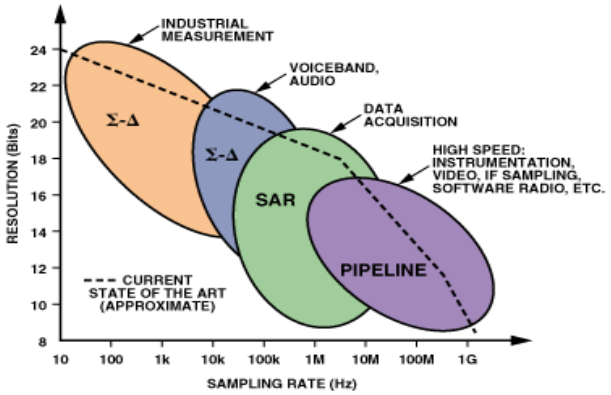

Figure 1.9 – ADC architecture Bandwidth vs. Resolution [7]

1.4 THESIS LAYOUT

This thesis will present the design and analysis of a first and second order K-Delta-1-Sigma (KD1S) modulator in two integrated circuit (IC) processes. This chapter provided a general overview of the different types of ADC architectures and mentioned their advantages and disadvantages. Chapter 2 details information regarding first and second order delta-sigma modulation and explains the classification of a DSM. Chapter 3 demonstrates the inherent difference between time interleaving and KD1S. Chapter 4 analyzes the requirements and design process of the DSM components with simulation results. Chapter 5 develops fundamental equations for the proposed 1^{st} and 2^{nd} order continuous time KD1S modulators. Chapter 6 shows simulation results of the proposed KD1S designs in a 500 nm and a 350 nm process. Lastly, chapter 7 investigates possible applications for the KD1S design and provides future research ideas.

CHAPTER 2: DELTA SIGMA MODULATION

2.1 SAMPLING

To process a continuous-time signal, sampling must be implemented as working with discretized signals is more convenient. Impulse sampling a signal is the procedure of multiplying an analog input signal with a unit impulse function as seen in Figure 2.1. The unit impulse function acts as a periodic impulse train consisting of pulses separated by a certain period that depends on the sampling frequency. When the unit impulse is multiplied with the input signal, the outputs of the process are discretized samples that are a set of impulses scaled to the amplitude of the input signal at their respective time [2].

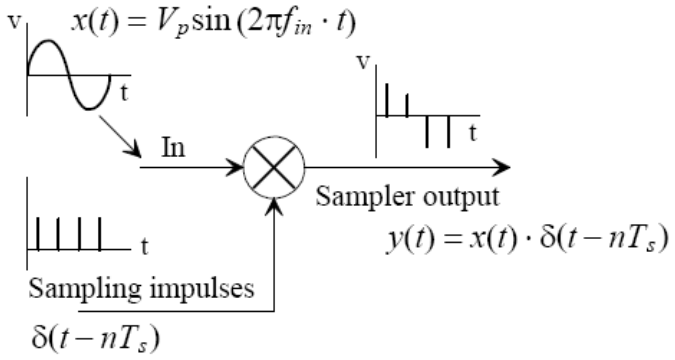

Figure 2.1 – Signal Sampling Process [2]

A signal can be oversampled, under-sampled, or sampled at the Nyquist rate. Nyquist rate sampling is satisfying the Nyquist-Shannon sampling theorem. This sampling theorem defines a sampling frequency that allows the converter to capture enough samples for a true representation of the analog input signal [1], [4]. The sampling rate required for this criterion is the following:

$$f_{sampling} = 2 \cdot f_{max} \tag{2.1}$$

where f_{max} is the highest frequency found in the input signal bandwidth while $f_{sampling}$ is the required sampling frequency [1]. This means that the converter can capture all the information necessary about the analog signal of finite bandwidth to digitize it when the sampling frequency is at least twice the highest frequency within the input bandwidth.

When the sampling frequency is below the Nyquist rate, the input signal would be considered under-sampled and signal aliasing appears. Aliasing occurs when data overlap and become indistinguishable. Aliasing is an issue as the output signal becomes distorted and could be representing a false input signal. This can prevent the recovery of the original signal [2].

Figure 2.2 presents an example of aliasing from under-sampling since the input signal frequency is higher than the sampling frequency. When connecting the sampled points, the output signal is at a different frequency than the input signal. This is because the number of samples captured is insufficient for true representation of the input signal.

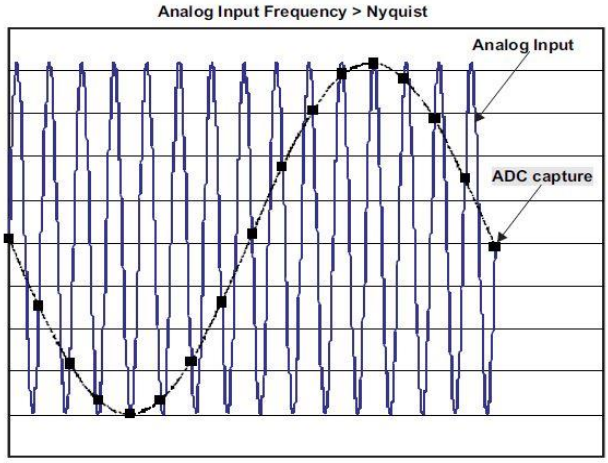

Figure 2.2 – Signal aliasing due to under-sampling [8]

In addition, oversampling is when the sampling frequency is multiple times higher than the Nyquist rate. A ratio can be used to represent the amount of oversampling called the oversampling ratio (OSR). The OSR relates the sampling frequency to the maximum input bandwidth and can

be written as in Equation 2.2 where f_s represents the sampling frequency and B is the input signal bandwidth.

$$OSR = \frac{f_s}{2 \cdot B} \tag{2.2}$$

An oversampling example, shown in Figure 2.3, demonstrates more discretized points are captured when sampling and therefore can represent the input signal correctly. Comparing Figures 2.2 and 2.3, the apparent difference is seen in the amount of points captured in each sampling category.

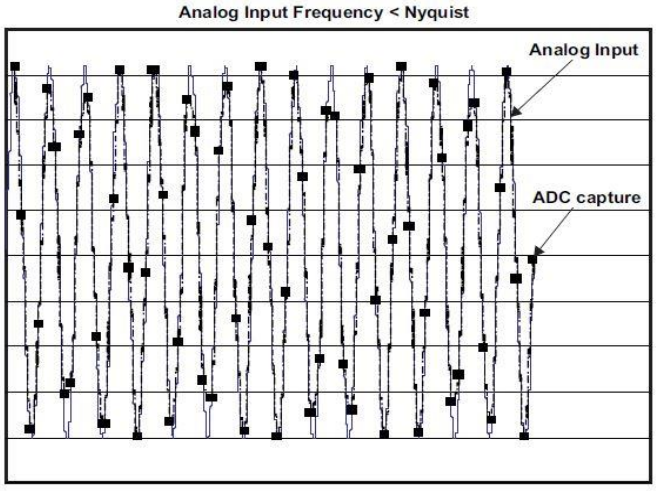

Figure 2.3 – Oversampling signal example [8]

Frequency domain representation of aliasing and oversampling is shown in Figure 2.4. After sampling, a bandlimited version of the input signal is populated at multiples of the sampling frequency as seen in Figure 2.4a. Aliasing occurs when the sampling frequency is less than the input frequency, and the sampled input versions overlap as in Figure 2.4b. However, when oversampling is employed, more spacing forms between sampled input signals as in Figure 2.4c.

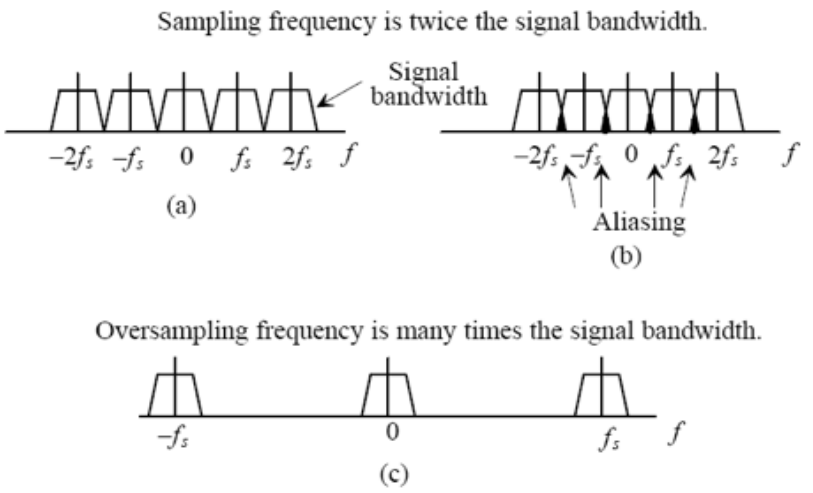

Figure 2.4 – Signal sampling and aliasing in frequency domain [1]

2.2 QUANTIZATION NOISE

Quantization noise is the effective noise added to a digitized signal, and it is always present with every analog to digital conversion [2]. Quantization noise can never be prevented, rather certain techniques can be used to reduce its effects in the input signal spectrum. One of the reasons quantization noise is always present is due to the mapping of an infinite amount of points (the continuous amplitude) into a limited amount of points (the discrete amplitude represented by a digital word). The block diagram in Figure 2.5 shows how quantization noise can be modeled in an ADC and since the noise is accompanied by every conversion it is directly added with the analog signal.

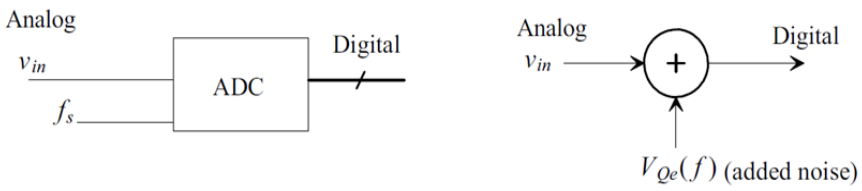

Figure 2.5 – Modeling ADC quantization noise [2]

Quantization noise can be found by taking the difference between an ADC input and a DAC output as in Figure 2.6 [2]. The ADC input is the original signal without quantization noise introduced yet while the DAC output is the reconstruction of the input signal, thus containing quantization noise. Taking this difference, the output would represent the quantization noise.

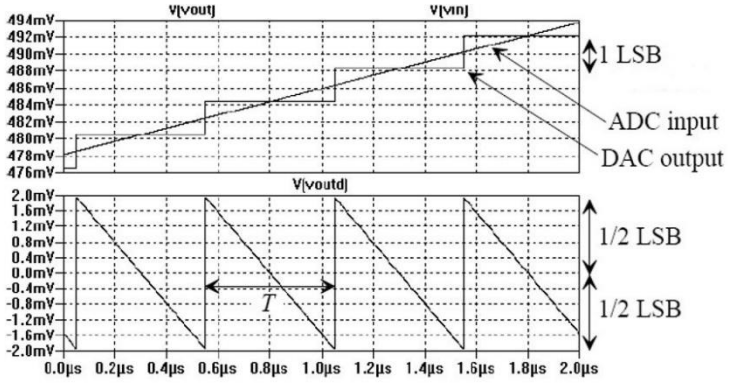

Figure 2.6 – Quantization noise difference between DAC and ADC [2]

Figure 2.6 can be used to characterize the quantization noise in its root mean square (RMS) value. This can be done for a specific period *T*, while noting that the noise varies between $\pm\frac{1}{2}LSB$ [2]. The RMS noise value can be calculated as in Equation 2.3.

$$V_{Qe,RMS} = \sqrt{\frac{1}{T}\int_0^T (0.5LSB - \frac{1LSB}{T}\cdot t)^2 dt} = \frac{1LSB}{\sqrt{12}} = \frac{V_{LSB}}{\sqrt{12}}, \qquad \left(\frac{V}{\sqrt{Hz}}\right) \tag{2.3}$$

The quantization noise can also be considered as a random variable within the same range of $\pm\frac{1}{2}LSB$. The probability of a quantization noise at a certain LSB is equal to the noise probability at any LSB within the range specified previously, this likelihood can be represented using a probability density function (PDF). As the intensity of different quantization errors is equal, the PDF is constant within $\pm\frac{1}{2}LSB$ as in Figure 2.7. The power of the quantization noise is the variance of the noise PDF, and the RMS noise voltage is the square root of the noise power. This process based on Figure 2.7, simplifies to the RMS noise in Equation 2.3 once again [2].

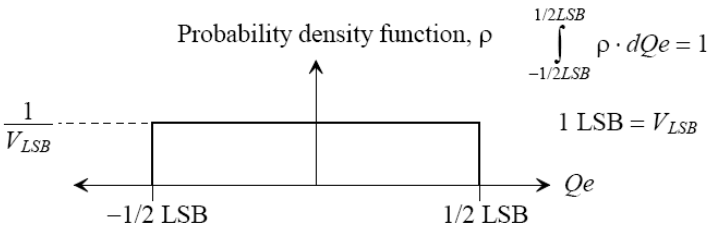

Figure 2.7 – PSD of the quantization noise in an ADC

Further, the voltage spectral density can be derived to know the value of the quantization noise at different frequencies. Voltage spectral density squared is the power spectral density which displays the power distribution function for different frequencies. Knowing that the area for the power spectral density of the quantization noise is equal to the output RMS value of the quantization noise squared, Equation 2.4 is derived.

$$V_{onoise,RMS}^2 = \int_0^\infty V_{onoise}^2(f) \cdot df, \qquad \left(\frac{V^2}{Hz}\right) \quad (2.4)$$

The RMS output noise is from Equation 2.3, and the output noise squared in terms of frequency is the unknown in Equation 2.4. Using this information and setting the limits to the desired spectrum (up to the Nyquist frequency), Equation 2.5 can be concluded. This equation is multiplied by 2 for considering a double-sided spectrum.

$$\frac{V_{LSB}^2}{12} = 2\int_0^{\frac{f_s}{2}} V_{Qe}^2(f) \cdot df, \qquad \left(\frac{V^2}{Hz}\right) \quad (2.5)$$

Noting from [2], if Bennett's criteria holds, the quantization noise voltage and power spectrum would be flat. Therefore, integrating Equation 2.5 from DC up to the Nyquist frequency, considered worst case due to all the quantization noise being located in the spectrum of interest, the integral is simply the area of a rectangle. As a result, Equation 2.5 can be simplified into Equation 2.6.

$$\frac{V_{LSB}^2}{12} = 2 \cdot V_{Qe}^2(f) \cdot [\frac{f_s}{2} - 0], \qquad \left(\frac{V^2}{Hz}\right)$$

$$\frac{V_{LSB}^2}{12} = V_{Qe}^2(f) \cdot f_s, \qquad \left(\frac{V^2}{Hz}\right)$$

$$V_{Qe}^2(f) = \frac{V_{LSB}^2}{12f_s}, \qquad \left(\frac{V^2}{Hz}\right)$$

$$V_{Qe}(f) = \frac{V_{LSB}}{\sqrt{12f_s}}, \qquad \left(\frac{V}{\sqrt{Hz}}\right) \qquad (2.6)$$

The quantization noise derived in Equation 2.6 can be seen in Figure 2.8. The noise is distributed evenly across the desired spectrum (meeting Bennett's criteria), with an amplitude that depends on the sampling frequency, f_s [2].

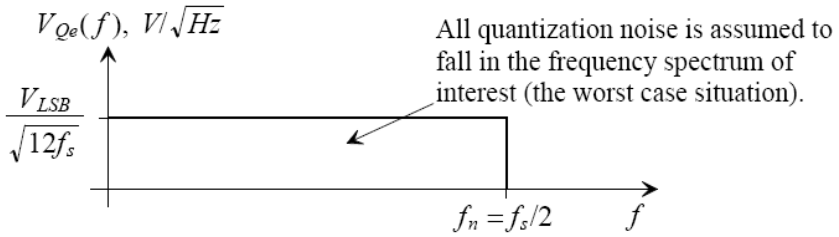

Figure 2.8 - Spectral density of quantization noise [2]

The area of the quantization noise is constant which signifies that increasing the sampling frequency would not decrease the noise even if the amplitude is reduced. Increasing the sampling frequency would simply spread the noise over a wider bandwidth up to a new Nyquist frequency. This confirms the discussion earlier that quantization noise can never be prevented, rather its effects can be reduced. A technique to reduce the quantization noise would be to use a filter to limit the noise introduced to the desired signal [2].

Lastly, the quantization noise spectral density shows how oversampling can be effective in decreasing the noise of the desired spectrum (spectrum up to the Nyquist frequency). However,

oversampling alone cannot achieve higher resolution in delta sigma modulators. High resolution is feasible with the combination of oversampling and noise shaping.

2.3 NOISE SHAPING

Noise shaping is the idea of shaping only the noise spectrum in the modulator without affecting the desired signal spectrum. Noise spectral shaping is done in a way to relocate the noise mostly to higher frequencies away from the input signal frequency.

Noise shaping combined with oversampling allows a delta sigma ADC to avoid the need for a high OSR to increase the resolution since the desired signal spectrum is limited and the noise spectrum is shaped to fall out of the region of interest [10]. In delta-sigma ADCs, the integrator acts as a high pass filter on the quantization noise that leads to noise shaping of the spectrum as shown in Figure 2.9.

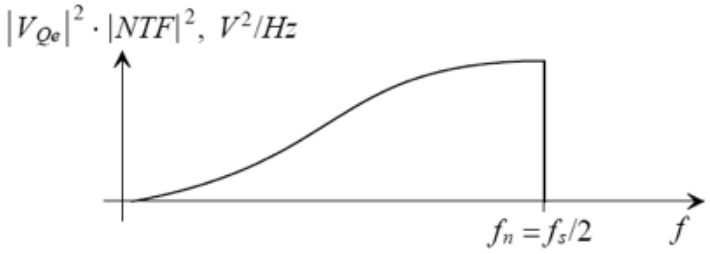

Figure 2.9 - Shaped quantization noise [2]

The integrator blocks noise at lower frequencies but allows noise at higher frequencies. In this way, the noise appears pushed out of the desired spectrum and shaped in an increasing manner. After quantization noise experiences noise shaping, it is called modulation noise [2].

For further improvement in resolution, filtering only the region of the desired signal as in Figure 2.10 is the way delta sigma modulators can reach higher resolution. Modulation noise is mainly centered at higher frequencies after shaping, thus allowing less noise to appear around the

input signal frequency. Along with filtering the baseband, a small quantity of the noise is present at the desired bandwidth in the end.

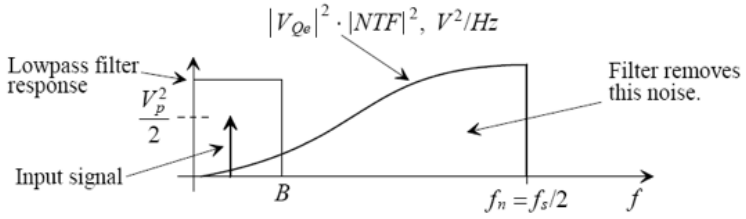

Figure 2.10 - Filtering modulation noise [2]

2.4 DELTA SIGMA MODULATION

As mentioned in Chapter 1, oversampling ADCs are different than Nyquist-rate ADCs in the conversion process executed, Figure 2.11 presents the components used in each ADC. Figure 2.11a shows typical blocks of a Nyquist-rate ADC, and Figure 2.11b shows conversion process for an oversampling ADC. The oversampling ADC mainly consists of a delta sigma modulator and a digital filter.

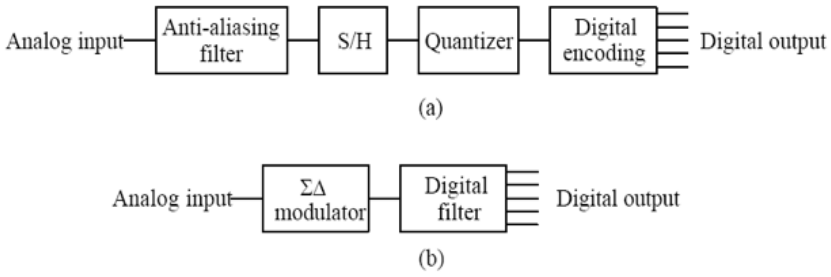

Figure 2.11 - Nyquist vs. Oversampling ADCs [1]

The delta sigma modulator eliminates the need for an anti-aliasing filter and a sample-and-hold circuit since oversampling is employed. A quantizer is not needed since the delta sigma modulator includes a comparator that performs the quantizing, and encoding is accomplished using a digital filter.

Further looking into how the delta sigma modulation is completed, a basic first order delta sigma modulator block diagram is presented in Figure 2.12.

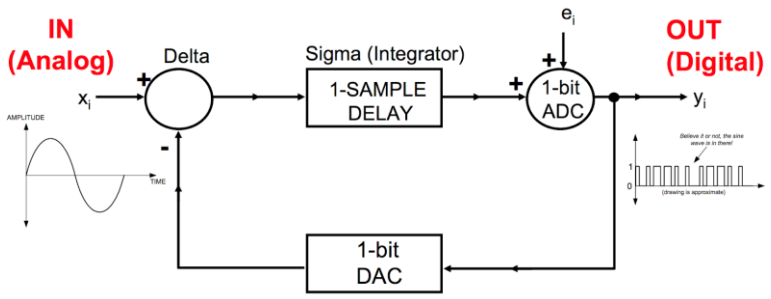

Figure 2.12 - First order DSM block diagram [7]

Four components make up the delta sigma modulator, the summation block, integrator, ADC, and the digital-to-analog converter (DAC). The DAC found in the feedback path inverts the ADC output and feeds it back to the summation block. The feedback signal is subtracted from the input signal through the summation block creating an error signal, then this error signal propagates to the integrator. The integrator accumulates the error and outputs a signal to the clocked comparator's input. Then the comparator acts on the integrator's output by comparing the value to a reference voltage. Output of the comparator moves to the modulator's output as well as feeds back through the DAC to form an error signal again. Because of this process, the feedback effectively forces the average DC value of the output to equal the input signal.

The output digital word of the delta sigma modulator is in the form of a pulse modulated signal which can be controlled in the manner of how often the signal is high or low to effectively be averaged and represent the analog input signal. The more the input signal increases reaching $+V_{ref}$, stream of 1's is outputted more often, whereas, more 0's are generated at the output when the input signal decreases towards $-V_{ref}$ [10].

The output averaged to represent the input signal means that if the converter averages 16 samples at a time, averaging these 16 samples should equal the input signal. For example, for a DC input shown in Equation 2.7 below, the correct output would be four times high and 14 times low in a random sequence.

$$V_{in} = 1.25\ V \qquad V_{ref+} = 5\ V \qquad V_{ref-} = 0\ V \tag{2.7}$$

For example, random 16 samples are given as 1011 0000 0100 0000, using Equation 2.8 to take the average of the16 sample, the output of the equation as detailed below equals the input voltage.

$$V_{in} = V_{ref+} - \left(V_{ref-}\right) \cdot \frac{\text{number of 1's}}{\text{samples}}$$

$$(5 - 0) \cdot {}^{4}/_{16} = 1.25\ V \tag{2.8}$$

2.4.1 FIRST ORDER DELTA SIGMA MODULATOR

By using a feedback, the modulator can now be further characterized into the feedback modulator group [2]. A block diagram of feedback modulators is shown in Figure 2.13

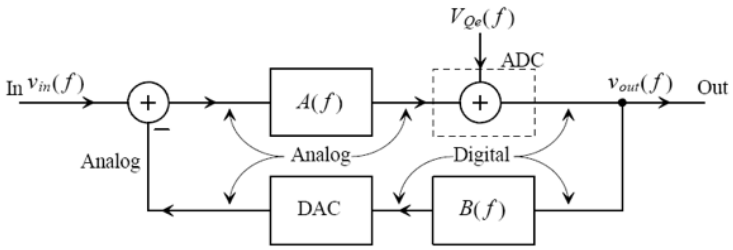

Figure 2.13 - Feedback modulator block diagram [2]

Using oversampling and feedback relaxes the accuracy requirements on the analog parts of the circuit granting the focus of precision on the digital components, which is less challenging to achieve with today's technology [3]. For example, the ADC and DAC used in the modulator can be 1-bit components rather than multi-bit. This benefit helps with reduced complexity, as well as it provides better linearity as the DAC is considered linear with only two outputs.

The combination of the feedback modulator and the digital filter allows for a 1-bit ADC and a 1-bit DAC with low resolution and reduced accuracy to function as a high-resolution analog to digital converter [2]. The following equation can be formed from the block diagram in Figure 2.13:

$$v_{out}(f) = [v_{in}(f) - v_{out}(f) \cdot B(f)]A(f) + V_{Qe}(f)$$

$$v_{out}(f) = A(f) \cdot v_{in}(f) - A(f) \cdot B(f) \cdot v_{out}(f) + V_{Qe}(f)$$

$$v_{out}(f)[1 + A(f) \cdot B(f)] = A(f) \cdot v_{in}(f) + V_{Qe}(f)$$

$$v_{out}(f) = \overbrace{\frac{A(f)}{1 + A(f) \cdot B(f)}}^{STF(f)} \cdot v_{in}(f) + \overbrace{\frac{1}{1 + A(f) \cdot B(f)}}^{NTF(f)} \cdot V_{Qe}(f) \tag{2.9}$$

A transfer function that shows the relationship between the input and output is called a signal transfer function (STF), while a transfer function showing the output relationship to the noise in the system is the noise transfer function (NTF). Looking at Equation 2.9, the STF is multiplied with the input signal, and the quantization noise is multiplied with the NTF.

The signal transfer function (STF) is desired to be equal to 1 so that all the input signal can be transferred to the output, and the noise transfer function (NTF) is preferably equal to 0 so that there is no quantization noise present at the output. Keeping the requirements in mind, the gain $A(f)$ of the forward path should be large while the gain of the feedback $B(f)$ should equal to 1. The considered gain values allow the signal to propagate through the modulator without any alteration while the noise spectrum is shaped [2].

Looking at Figures 2.13, a frequency domain model equation for the modulator can be developed by having $A(f) = \frac{1}{s}$ that is the transfer function of an integrator in s-domain. The ADC would be the summation block that adds quantization noise, and $B(f) = 1$ so that there is negative feedback. This yields to Equation 2.10 as detailed below:

$$v_{out}(f) = [v_{in}(f) - v_{out}(f)]\frac{1}{s} + V_{Qe}(f)$$

$$v_{out}(f) = \frac{v_{in}(f)}{s} - \frac{v_{out}(f)}{s} + V_{Qe}(f)$$

$$v_{out}(f)\left[1 + \frac{1}{s}\right] = \frac{v_{in}(f)}{s} + V_{Qe}(f)$$

$$v_{out}(f) = \overbrace{\frac{1}{1+s}}^{STF(f)} \cdot v_{in}(f) + \overbrace{\frac{s}{1+s}}^{NTF(f)} \cdot V_{Qe}(f) \tag{2.10}$$

This derivation shows a low pass filter transfer function, ($\frac{1}{s+1}$) for STF, and a high pass filter transfer function, ($\frac{s}{s+1}$) for NTF. As mentioned earlier the low pass filter is being multiplied with the input signal as a mean of filtering only the bandwidth of interest, while at the same time the high pass filter is being multiplied with the quantization noise to mostly have the noise pushed to higher frequencies [1].

2.4.2 SECOND ORDER DELTA SIGMA MODULATOR

A second order delta sigma modulator (DSM) consists of two integrators, 1-bit ADC, 1-bit DAC, two feedback paths, and the summation block. A block diagram of such modulator is shown below, this delta-sigma modulator is presented as a discrete time model.

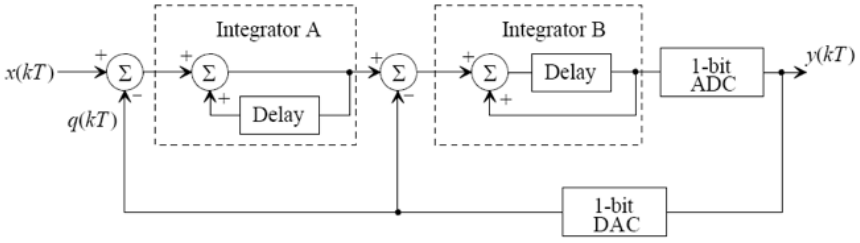

Figure 2.14 - Second order DSM [1]

First order DSM contains disadvantages such as dead zones. Dead zone is when the output does not move or decide for some ranges of the input, so the output would be considered dead and

unable to decide. This problem could be a result of nonlinearities, though the ADC and DAC are linear, the comparator is a nonlinear element which could lead to such problem along with the noise found at the output [2]. These problems can be reduced using a second order DSM that can improve the linearity and resolution of the modulator. Linearity is improved due to the better randomization of the output code as there are two feedback paths rather than one. The randomization of the output can prevent problems like dead zones. Moreover, second order DSM shapes the noise spectrum even more leading to a reduction in the modulation noise present around the input signal, thus increasing the resolution further [2].

Second order DSM arises a concern for instability. The use of multiple paths in higher order modulators can prompt delay accumulation, introduce new poles to the system (in discrete system), or large signals can reduce the comparator's gain by overloading the loop. All these factors can cause the DSM to be more vulnerable to instability, thus more stringent requirements and precautions would be placed on higher order modulators as stability can be more sensitive [2], [10]. A second order continuous delta-sigma modulator would be as Figure 2.15

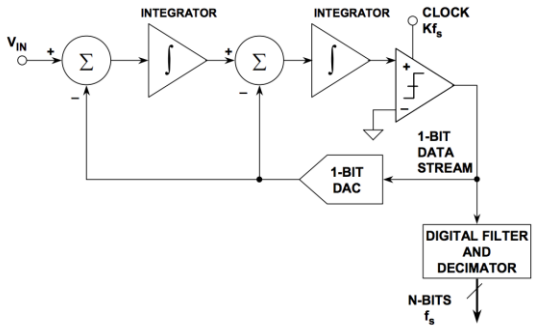

Figure 2.15 - Continuous time model of second order DSM [10]

Frequency domain model equations can be derived in a similar manner as in Equation 2.10 to present how the NTF and STF are changed with the second order modulator. $A(f)$ would be an

integrator again so $A(f) = \frac{1}{s}$, while $B(f)$ is still equal to 1. These equations are derived for the continuous time model, if discrete time is to be used then z-domain model would be derived.

$$[[\frac{1}{s}(v_{in}(f) - v_{out}(f))] - v_{out}(f)]\frac{1}{s} + V_{Qe}(f) = v_{out}(f)$$

$$\frac{v_{in}(f)}{s} - \frac{v_{out}(f)}{s} - v_{out}(f)) + s \cdot V_{Qe}(f) = s \cdot v_{out}(f)$$

$$\frac{v_{in}(f)}{s} + s \cdot V_{Qe}(f) = v_{out}(s + 1 + \frac{1}{s})$$

$$v_{out}(f) = \overbrace{\frac{1}{s^2 + s + 1}}^{STF(f)} \cdot v_{in}(f) + \overbrace{\frac{s^2}{s^2 + s + 1}}^{NTF(f)} \cdot V_{Qe}(f) \tag{2.11}$$

This derivation shows that the input spectrum is filtered with a second order low pass filter, on the other hand, the noise spectrum is being shaped with a second order high pass filter. These results show that the second order delta-sigma modulator shapes the noise spectrum even further with 40 dB/decade rather than 20 dB/decade as in the first order situation. And the input spectrum is filtered with a low pass filter that has a slope of 40 dB/decade resulting in more ideal filtering.

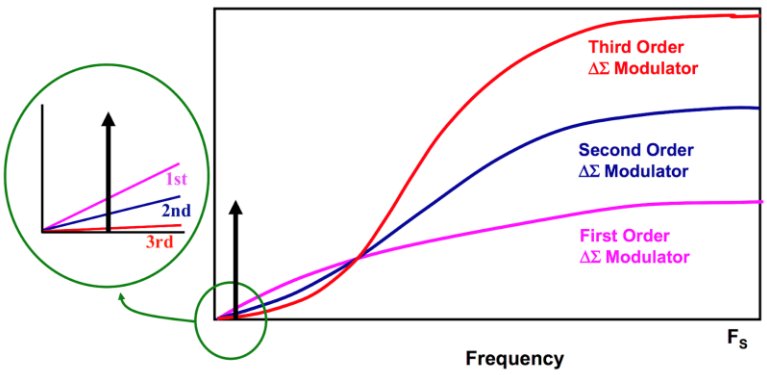

Figure 2.16 - modulation noise with different order DSM [5]

Modulation noise based on the DSM order is shown in Figure 2.16. The noise is larger at higher frequencies for higher order modulators, but looking at the band of interest, the modulation

noise decreases with the increasing modulator order. The modulation noise is seen flatter around the input signal with the 3rd order modulator while higher with a first order modulator [2], [5]. This is important because the noise is shaped more in the desired spectrum and can be later suppressed further using a filter to increase the modulator's resolution.

2.5 DIGITAL FILTERING

Oversampling ADC consists of a delta-sigma modulator followed by a digital decimating filter as shown in Figure 2.17 [5]

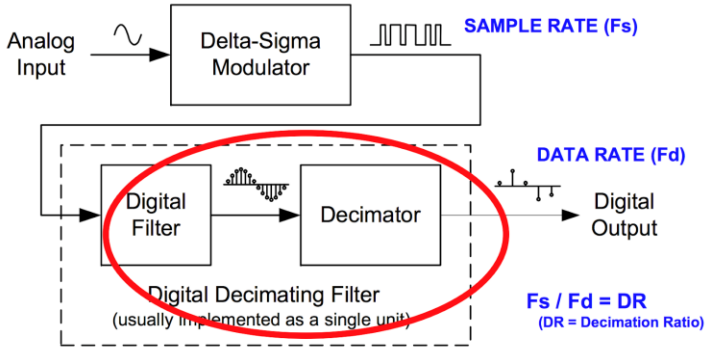

Figure 2.17 - Digital filtering block diagram [5]

The delta sigma modulator oversamples the data and uses noise shaping to increase the output resolution. However, the bit stream output of the delta sigma modulator still needs modifications as it still contains noise around the signal, and it is in the form of a 1-bit signal. These problems can be resolved in the digital domain using the digital decimating filter [5], [11].

A low pass digital filter that operates at the DSM's sampling frequency is placed at the output of the modulator as shown in Figure 2.10, the filter blocks the noise at higher frequencies and minimizes modulation noise in the desired spectrum [10]. An example of a lowpass digital filter would be a Finite Impulse Response (FIR) filter as in Figure 2.18, where the filter takes the

1-bit data from the DSM and outputs a word with multiple bits representing the analog input signal as seen at the output of the block diagram.

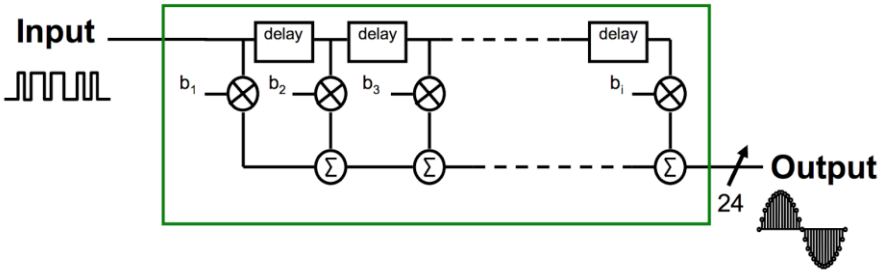

Figure 2.18 - Finite Impulse Response Filter [5]

Looking at the frequency domain in Figures 2.19 and 2.20, the FIR filter has a low pass sinc response, the filter response is not the ideal Brick wall filter but rather a response of the sampling sinc function. Figures 2.19 and 2.20 present the spectrum before and after the filtering process of the noise. Figure 2.19 displays the fundamental signal and modulation noise prior to filtering. The noise content is seen considerably high even after noise shaping.

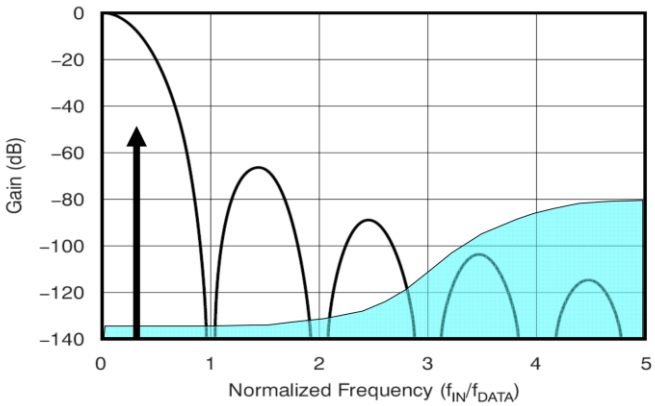

Figure 2.19 - Sinc filter with DSM output [5]

Figure 2.20 shows how the noise spectrum contains less noise due to filtering.

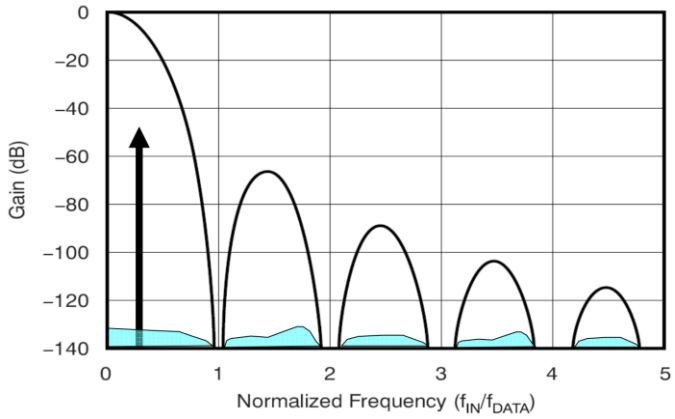

Figure 2.20 - Modulation noise after digital filtering [5]

After filtering, the data rate is fast, so a decimator is used to bring back the bandwidth from oversampling frequency up to the Nyquist frequency to slow down the data. The decimator does not cause any loss of information, its purpose is to down-sample the data and yield a final high-resolution output after filtering. A decimator block diagram is shown in Figure 2.21, the input is at a frequency f_s and the decimator reduces the sampling rate by K resulting in an output word at a rate of $\frac{f_S}{K}$.

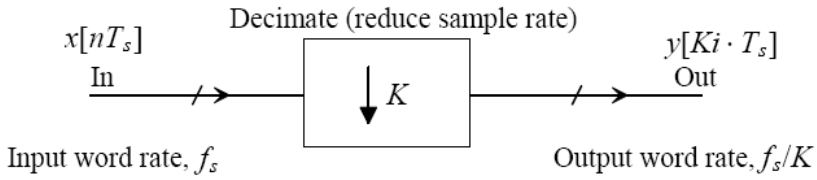

Figure 2.21 - Decimator block diagram [2]

The *K* in Figure 2.22 is called the decimation and it equals the sampling frequency divided by the data rate, so *K* is the reduction of the effective sampling frequency [2]. Figure 2.22b shows the signal with the digital low pass filter and a small *K* while Figure 2.22a shows the digital filter with larger *K*. Increasing *K* brings the digital low pass filter closer to the fundamental frequency

as the data rate decreases. The low pass filter now cuts noise even further out of the passband hence increasing the resolution.

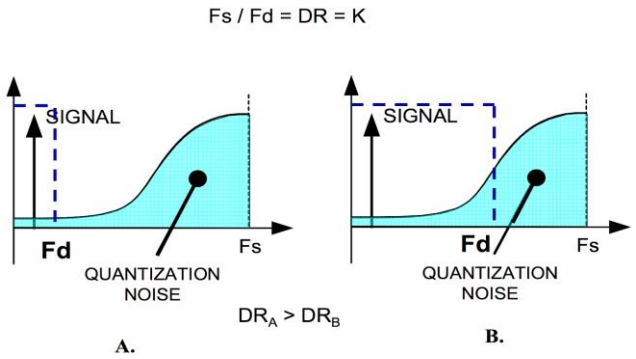

Figure 2.22 - Output of the decimator [5]

In this manner, the digital filter and decimator combined process the serial bit stream and generate the final output data [5], [10]. This thesis will mainly focus on the improvement of delta sigma modulations excluding the digital filtering part of the ADC. Further digital filtering techniques will not be discussed, and software approach will be used to execute this ADC step.

2.6 CLASSIFICATIONS OF DELTA SIGMA MODULATION

Delta sigma ADC can be divided into two more categories of active or passive, and discrete or continuous time. Most of the parts in the delta sigma modulator are active components but depending on the type of integrator used in the circuit the modulator can be classified as passive or active [3]. The two types of integrators are shown in Figure 2.23.

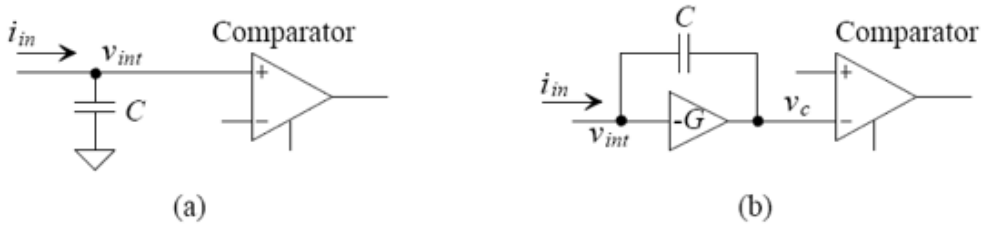

Figure 2.23 - Passive vs. Active integrators [2]

A passive integrator is one that uses just a capacitor to store the error signal as seen in Figure 2.23a. Passive delta sigma ADCs are preferred when low power consumption is sought with the cost of other limitations. Figure 2.24 shows a block diagram for a noise shaping modulator using passive integrator, based on the block diagram of Figure 2.12

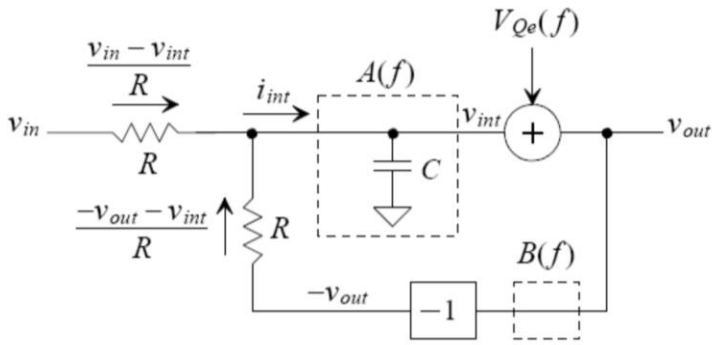

Figure 2.24 - Passive delta sigma modulator [2]

Solving for the output voltage using Kirchhoff's Current Law (KCL) the following equation is found with the complete derivation in [1]

$$v_{out}(f) = \overbrace{\frac{1}{1+j\omega RC}}^{NTF(f)} \cdot v_{in}(f) + \overbrace{\frac{j\omega RC}{1+j\omega RC}}^{STF(f)} \cdot V_{Qe} + \frac{-2 \cdot v_{int}}{1+j\omega RC} \tag{2.12}$$

Comparing preceding equation to Equation 2.9, an extra term is present that will add distortion to the output signal [2]. The extra noise is present at the output since the passive integrator used affects the circuit by causing nonlinearities. As shown in the equation, the error is directly dependent on the node voltage v_{int}, thus also depending on the input signal which can be unpredictable and uncontrollable [2]. Other than nonlinearities, the passive integrator leads to dead zone problems, which were discussed previously in this chapter [2]. These problems can cause a decrease in the modulator's resolution. Knowing that linearity is poor, passive delta sigma ADCs are not preferable for higher order noise shaping as linearity would be harder to control [3].

On the contrary, an active delta sigma ADC uses active integrator, that is an operational amplifier with capacitor in the feedback. An example of such integrator is shown in Figure 2.23b. Active integrators help keep node voltage v_{int}, the inverting input of the integrator, constant, and in turn improve the linearity of the ADC. Since v_{int} is constant, the extra noise term in equation 2.12 cancels and only quantization noise is left. Block diagram of an active noise shaping modulator is presented in Figure 2.25

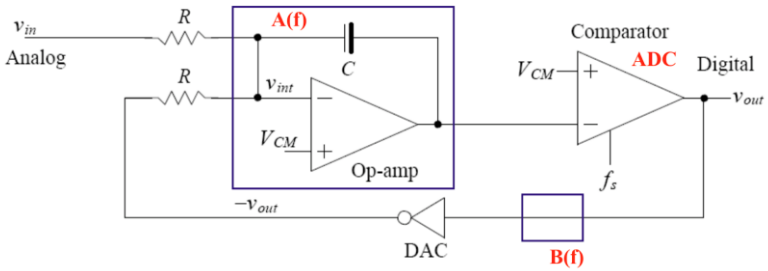

Figure 2.25 - Active DSM [2]

All the components are the same as in the passive modulator expect the integrator. An equation can be formed for the output of Figure 2.25. In the equation, all voltages are referred to V_{cm} to simplify the equation, and sign/inversions of the amplifier and comparator are considered. The final equation for $v_{out}(f)$ is derived below and v_{int} is still present, but this time the gain of the amplifier will help reduce the non-linearities, detailed derivations of v_{int} are shown in [2].

$$v_{out}(f) = \overbrace{\frac{1}{1 + j\omega R\frac{C}{G}}}^{STF(f)} \cdot v_{in}(f) + \overbrace{\frac{j\omega R\frac{C}{G}}{1 + j\omega R\frac{C}{G}}}^{NTF(f)} \cdot V_{Qe} + \frac{-2 \cdot v_{int}}{1 + j\omega R\frac{C}{G}}$$

$$v_{int} \approx \frac{i_{in}}{j\omega C \cdot G} \tag{2.13}$$

The effect of using an active amplifier with gain G is seen in Equation 2.13. As the gain $G \to \infty$, the voltage v_{int}becomes 0 and the extra term in Equation 2.12 is canceled [2]. This presents the reason for choosing an active over a passive integrator for DSM.

Furthermore, ADC can be considered continuous (CT) or discrete time (DT) circuit. Delta sigma ADCs were mainly continuous time but as switched capacitor (SC) capabilities improved with CMOS technology, discrete time ADCs became more common [4], [12]. The two ADCs are distinguished based on two factors, first is where the sampling is executed, second is the integrator circuits used. Figures 2.14 and 2.15 show a second order delta sigma modulator in both discrete and continuous time topologies respectively.

In discrete time ADCs, the sampling is done at the input of the ADC as discrete circuits expect a sampled input, and the integrator would be discrete. An example of a DT integrator is a discrete analog integrator (DAI) shown in Figure 2.26.

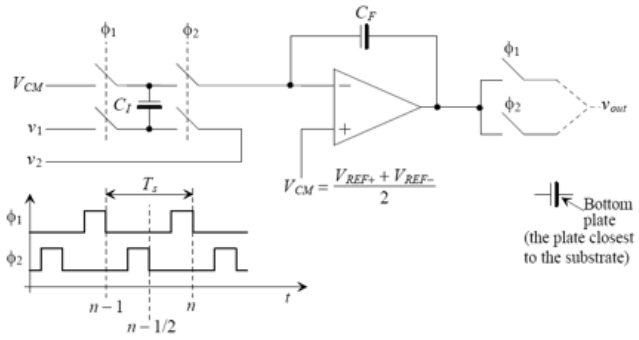

Figure 2.26 - Discrete Analog Integrator (DAI) [2]

The DAI contains SC controlled by non-overlapping clocks meaning the clock signals are never high or low at the same time as seen in the clock time diagram in Figure 2.26. Discrete time ADCs are popular due to their insensitivity to signal characteristics, precision, and accuracy. The drawbacks of DT ADCs would be the settling requirement of the SC as their capacitors have to fully charge/discharge within a certain period. The op-amp bandwidth is limited, leading to restrictions on the maximum SC clock frequency. Moreover, glitches from switching transients are present [2].

On the other hand, continuous time ADCs implement the input signal sampling at the quantizer that is the comparator rather than at the input as in the DT version. The integrator in CT circuit would be an active integrator as shown in Figure 2.27. The advantages of CT DSM include a double anti-aliasing filter effect since the input is sampled at the comparator. The double anti-aliasing filtering occurs because the input signal is filtered through the integrator prior to being sampled at the comparator, then once sampled and passed to the output, the modulator's output is filtered again through the digital filter.

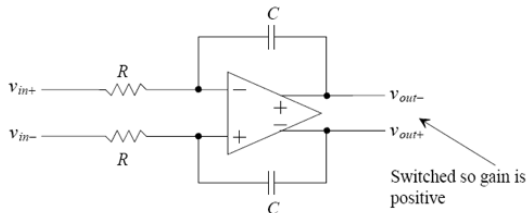

Figure 2.27 – Continuous time active integrator

Other advantages of the CT circuit include less input capacitance and kick back noise as SCs are not utilized. The frequency response of the filter is fixed meaning that the pole locations of the integrator do not change with frequency as in the DT ADCs [3]. Suited for simple mitigation to future CMOS processes. The disadvantages of continuous time ADCs would be large layout area due to the passive components, and process variation which could be less of a problem with new CMOS technology [12].

Provided that, the advantages of the CT ADC outweigh the drawbacks to achieve higher resolution, and fast conversion, which is why CT ADC topology is used in this thesis.

CHAPTER 3: TIME INTERLEAVING VS. KD1S

3.1 ADC SPECIFICATIONS

Analog-to-digital converter's dynamic performance is characterized by certain parameters. These parameters enable the comparison between ADCs in terms of performance, which is why it is important to define them. Parameters defined in this section will be specifically for frequency domain [14].

The first important parameter to be mentioned is signal-to-noise ratio (SNR). Quantization noise is present with every ADC conversion and cannot be eliminated, which is why SNR is used to measure the ratio of input signal to the noise in decibels. Higher SNR value means that the input signal strength is high in comparison to the noise or in other words, the noise is low in the measured signal bandwidth. The SNR equations differs depending on the ADC topology used [2]. The ideal SNR in decibels is written as:

$$SNR_{ideal} = 6.02N + 1.76 \quad (dB) \tag{3.1}$$

In addition, Effective Number of Bits (ENOB) can be resolved from ideal or measured SNR and it determines the number of bits of a converter. The ENOB equation including the measured SNR is as follows:

$$N_{eff} = \frac{SNR_{meas} - 1.76}{6.02} \tag{3.2}$$

Moreover, nonlinearities or mismatches in the circuit introduce other forms of noise. To measure this noise, signal-to-noise plus distortion ratio (SNDR) presents a better specification for the overall noise level in comparison to the input signal. SNDR or also known as signal-to-noise

and distortion (SINAD) is the combination of SNR along with the distortion tones found in the spectrum that can be determined using Equation 3.3 [2], [14].

$$SNDR = 20 \cdot log \frac{V_p/\sqrt{2}}{V_{Qe+D,RMS}} \tag{3.3}$$

And using this new measured SNDR, ENOB can be recalculated with the result to include the harmonic distortions.

$$N_{eff} = \frac{SNDR - 1.76}{6.02} \tag{3.4}$$

In many occasions, SNR and SINAD are used interchangeably, and to differentiate both is important. In the output spectrum usually the first five dominating tones are removed which is why SNR and SINAD can appear to have the same value if calculated within the low frequency bandwidth. The difference between SNR and SINAD appears when the input signal amplitude increases as shown in Figure 3.1, and both parameters have to be used carefully [2], [14].

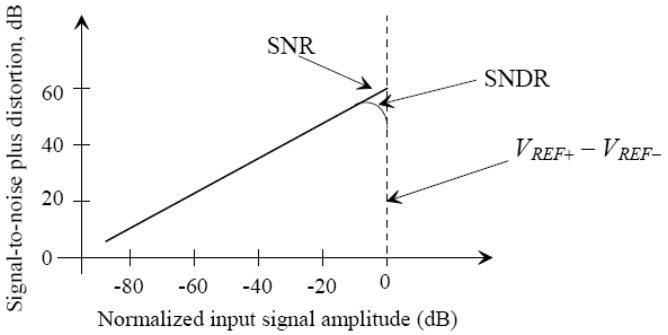

Figure 3.1 – SNDR and SNR with respect to input signal amplitude [2]

Likewise, dynamic range (DR) can be defined as the range of signal amplitudes a converter can resolve. Dynamic range can be calculated in different ways; one way is the ratio of largest output signal to the smallest output signal in the spectrum. Equation 3.5 below can be used to calculate the dynamic range for N bits. For example, if an ADC has a DR of 40 dB that means it

can resolve a signal amplitude from 1 to 100, and the converter must have at least 7 bits to resolve the signal range specified [14].

$$DR = 6.02N \tag{3.5}$$

3.2 TIME INTERLEAVING

Decimation was mentioned in Chapter 2 for its purpose to slow down digital output signal by dividing the sampling frequency with decimation factor *K*. Interpolation is the opposite of decimation as it increases the sampling rate of clocking by a factor of *K*. Both techniques are used in digital signal processing and manipulating the clocking frequency of the output data. The same idea can be applied in analog signal processing called *K*-path sampling [2]. This process is achievable by using more than one path (*K* paths in parallel) clocked at the same frequency on different clock phases. Input is common to all paths, and outputs are summed so that the effective output frequency is *K* times larger than the input frequency as shown in the following equation

$$f_{s,new} = K_{path} \cdot f_s \tag{3.6}$$

The *K*-path topology can be further controlled with the use of switches and a non-overlapping clock generator. Figure 3.2 shows the *K*-path topology and equivalent single path, called a time interleaved topology [2]. The non-overlapping clocks are never high or low at the same time and have clock edges $\frac{T_s}{K}$ spaced, where T_s is the sampling period. The input is common to all paths, but each path is non-zero/closed at a certain clock phase, ϕ_K. On the other hand, the output is connected/changing between the paths every $\frac{T_s}{K}$ [2]. For example, path 1 can be nonzero at $\{0, T_s, 2T_s, \ldots\}$ time intervals, while path 2 can be nonzero at $\{\frac{T_s}{K}, T_s + \frac{T_s}{K}, 2T_s + \frac{T_s}{K}, \ldots\}$ time intervals and so forth [2].

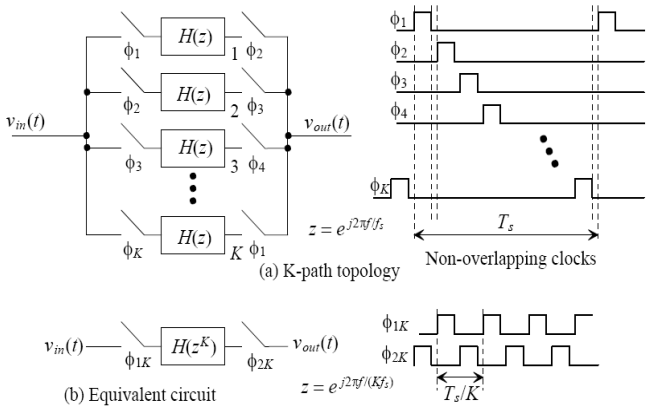

Figure 3.2 - Time Interleaving topology [2]

The equivalent circuit of Figure 3.2a is shown in Figure 3.2b, a non-overlapping clock with 50% duty cycle is feasible if the triggered edges are spaced by $\frac{T_s}{K}$. Moreover, as the effective frequency increases as in Equation 3.6, one delay in a single path is *K* delays in the effective path at faster sampling rate of K/T_s. Therefore, in z domain, if z is redefined at the new effective clock rate, then a delay of z^{-1} of the slow sampling frequency becomes z^{-K} of the new effective sampling frequency. Equation 3.7 can be used for analyzing *K*-path's system response where *K* stands for the number of paths interleaved [2].

$$z \rightarrow z^k \tag{3.7}$$

Time interleaving can be implemented with Nyquist rate analog-to-digital converters by having *K* slow ADCs put in parallel, to result in a fast time interleaved ADC [13]. The same analog input is applied to each path with an ADC, but the sampling clock is delayed by $\frac{T_s}{K}$ in each path, as a result, output changes at Kf_s and the overall effective ADC frequency is K times the input sampling speed [8]. This technique is appealing to use with Nyquist rate ADCs for its capability to increase the conversion rate. Sampling rate increase allows capturing a wider signal bandwidth which can ease frequency planning as well as reduce aliasing. The spectral density of the quantization noise as in Figure 2.8 now can be written in terms of the new frequency as follows:

$$V_{Qe}^2(f) = \frac{V_{LSB}^2}{12 \cdot K_{path} \cdot f_s} \tag{3.8}$$

Looking at Equation 3.8 the quantization noise spreads over wider frequency range as *K* increases having the same effect of increasing f_s.

Despite the benefits interleaving topology offers, there are design challenges that can be a disadvantage and even lead to a decrease in the SNDR. Some of the major problems that can take place are timing issues like clock jitter or clock skew, path matching, an increase in layout area, power draw, and complexity [2], [13]. The mentioned disadvantages can generate spurious tones in the output spectrum. Luckily, spectral components appear at known places in the spectrum and can be reduced using analog or digital calibration, but the calibration circuity increases the design process complexity. Figure 3.3 shows an example of the output spectrum with the unwanted tones mentioned above and how the number of tones increases with the number of ADCs interleaved [8], [13].

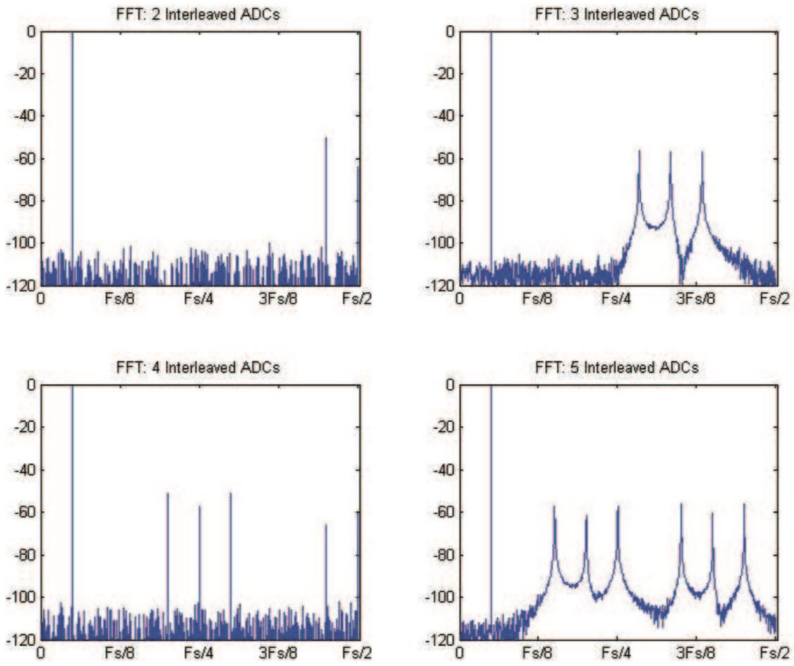

Figure 3.3 - Time Interleaving spectral tones [8]

3.3 K-DELTA-1-SIGMA (KD1S)

Time interleaving for Nyquist rate ADCs can be expanded to oversampling ADCs, specifically delta sigma modulators. The ADCs would be put in parallel just as in Figure 3.2 and non-overlapping clocks are used to control the input and output as shown in Figure 3.4.

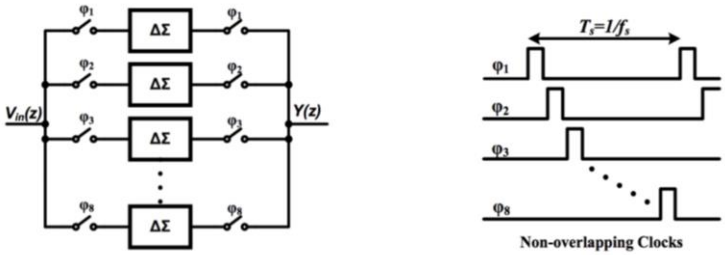

Figure 3.4 - Interleaving DSM [13]

Interleaving DSMs does not behave as a true delta-sigma modulator in terms of noise shaping because the noise is only spread out over a wider frequency range without being shaped to only higher frequencies. This is apparent in Figure 3.5 as the noise transfer function (NTF) spectrum contains tones repeating at odd frequencies of $\frac{f_S}{2}$ rather than being concentrated at higher frequencies. In addition, the feedback signal takes T_s, a whole clock period, to complete the loop where in true noise shaping the signal requires a loop delay less than $\frac{T_S}{K}$ [13].

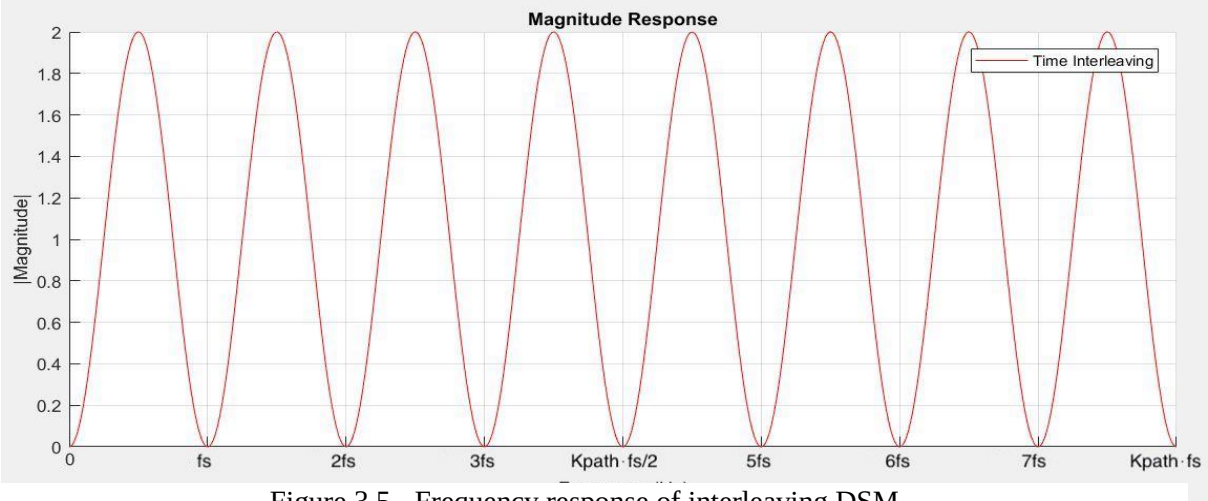

Figure 3.5 - Frequency response of interleaving DSM

Moreover, interleaving delta-sigma modulators contain the same drawbacks as in interleaving their counterparts Nyquist rate ADCs. Some of the drawbacks include the layout size and power consumption increase since *K* operational amplifiers and comparators are needed, and path mismatch can affect the overall system SNR.

These drawbacks along with the failure to operate as noise a shaping modulator prevents DSM from being interleaved as the Nyquist rate ADCs. Noise shaping is the tool that empowers and makes delta sigma modulation a compelling technique able to ease requirements on analog parts and offer higher resolution, thus without noise shaping DSM is not effective.

Since interleaving DSM in the method displayed earlier does not work, a new topology was developed in [2] which enables oversampling ADCs' operation with multiple paths. The topology realized uses *K*-paths that share an integrator, with *K* comparators to attain wide band noise shaping called K-Delta-1-Sigma (KD1S) [13]. KD1S enables high speed conversion while maintaining DSM benefits. An example of passive simple KD1S modulator topology is shown in Figure 3.6 where the integrator here is passive and common to all *K*-paths, having one integrator allows for quantization noise to be shaped to higher frequencies as well as the modulator can tolerate the lack of precision in analog circuitry. This topology provides the possibility for low power consumption since less components are used than the average time interleaved topologies [13].

Figure 3.6 shows the topology implementation with four paths, a single integrator, four comparators, and summed output forming 3 bits at four times the input sampling frequency [2].

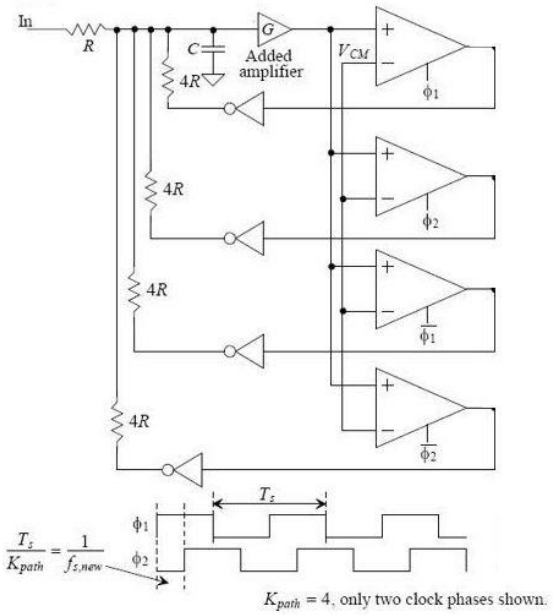

Figure 3.6 - 4-path passive KD1S [2]

Noise shaping is true in the KD1S topology as illustrated in Figure 3.7, the noise transfer function shows the modulation noise shaped to higher frequencies rather than having repetitive ripples forming. Figure 3.7 shows time interleaved DSM that is not valid in red, and a true noise shaping with KD1S in blue.

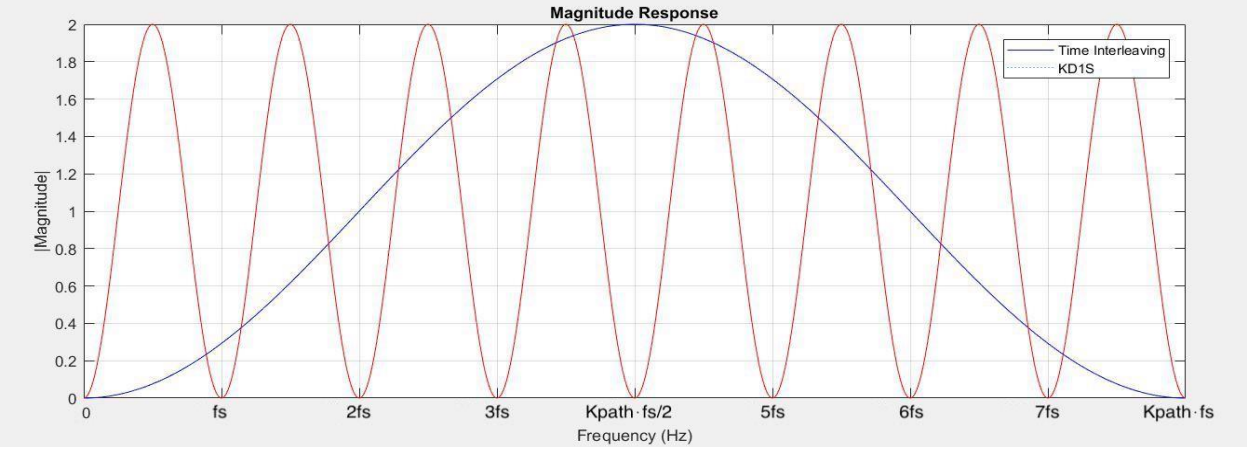

Figure 3.7 - Frequency response of KD1S modulator

Time interleaving is a handy technique to use with Nyquist rate ADCs when high sampling frequency is required. In Delta-Sigma modulation oversampling can be employed to achieve

higher sampling frequencies. Thus, the use of KD1S might be questioned as the same high conversion rate can be reached using one path in DSM ADC.

However, KD1S does not only provide higher sampling rate, it provides several other benefits that cannot be achieved with using only one path DSM [15]. Timing issues in the previous time interleaved topology are not a concern for KD1S as the deviation of time skew due to path mismatch are reduced by the oversampling ratio (OSR) in the digital filter along with the number of paths in the KD1S [15]. This also applies to clock jitter as the effects are reduced by OSR and *K*-paths. The reason KD1S is immune to timing issues is that the forward path is shared by the K-paths since the integrator is common. Any timing error that would be introduced to the signal is fed back and is filtered the same way as quantization noise. Also, layout area is smaller than the time interleaved Nyquist ADCs as the number integrators does not increase with the number of paths used and utilizing only one integrator along with oversampling grants lower power consumption. Moreover, KD1S topology offers an advantage in the ease of interfacing with software, which is helpful as the digital filtering will be done in a MATLAB software [2].

CHAPTER 4: DESIGN OF FIRST AND SECOND ORDER KD1S COMPONENTS

The KD1S topology proved to have several appealing advantages that prompts further research. This thesis will consider first and second order continuous time, active KD1S topology with $K_{path} = 8$. The continuous time, active KD1S modulator was selected for the benefits it offered, which are low power, high resolution, and high speed. Both first and second order KD1S modulators consist of common components, the components will be considered in this chapter for their general operation, design considerations, and simulations showing expected performance.

The simulations were done for the design in two manufacturing processes, Austria Micro Systems (AMS) S35 $0.35\mu m$, and OnSemiconductor C5 (C5) $0.5\mu m$. The following sections will show the simulation results for the AMS process, and the last section will present a table summarizing results in C5. The same design requirements were considered for both processes.

4.1 CLOCK GENERATION

The first component to be discussed is the clock generator shown in Figure 4.1. The sampling operation in the modulator is completed by utilizing different clock phases so that the *K* paths are never connected at the same instant to the feedforward path. The number of clock signals required in the KD1S design corresponds to the number of K_{path} used. The proposed design utilizes eight paths; thus, the clock generator is designed to produce eight non-overlapping clock signals.

The traditional ring oscillator usually consists of an odd number of inverter stages that generates an output fluctuating between the circuit supply voltage rails at a specific oscillation

frequency. The ring oscillator with odd number of stages is considered single ended and would not meet the design timing requirements of the KD1S. In the KD1S, clock edges need to be spread over all the clocking period, and in the case of the ring oscillator the clock edges are spread over half of the clock period. Also, with an odd number of stages, the clock signals would not have the equal timing between edges, which is why a single ended oscillator cannot be used. Alternately, a differential oscillator would need to be utilized for the design with eight paths to work accurately.

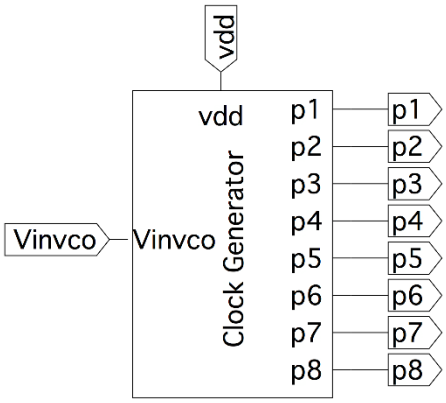

Figure 4.1 – Clock generator symbol

The differential ring oscillator is designed to be voltage-controlled. Voltage controlled oscillator means that the frequency of oscillation can be changed linearly with an input voltage, which is why Figure 4.1 has a DC input voltage of $V_{vin,VCO}$ rather than a clock input voltage.

The clock generator consists of two main components. The first component is a delay stage made of a non-overlapping clock generator that outputs two clock phases as shown in Figure 4.2. The delay stage consists of two paths, each path includes a NAND gate and an even number of inverters. The inputs to the delay stage are the NAND gate inputs. The NAND gate of a single path has two inputs, an external and an internal input. The external input is a clock signal, while the internal input is the swapped output of the opposite path. The clock inputs to the delay stage are opposite clock signals, and the outputs are two non-overlapping clock phases.

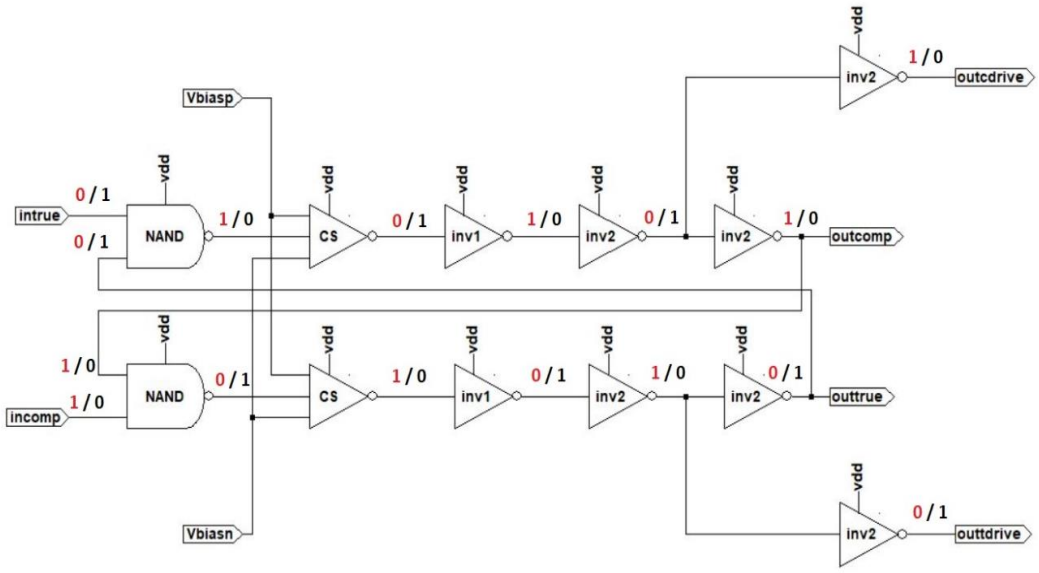

Figure 4.2 – Delay stage (non-overlapping clocks)

To generate the non-overlapping clocks, simply inverting a clock signal does not achieve the desired non-overlapping effect properly as the signals can still intersect for a certain time interval. Therefore, the delay stage in Figure 4.2 is employed [1].

The circuit operation in Figure 4.2 is explained through simple logic inputs of either 0 or 1 as annotated on the figure. The inputs in each path start with opposite signals that propagate through the NAND and NOT logic gates. Looking at the truth table for a NAND gate in Table 4.1, when one of the inputs are low/zero the output is automatically high/one regardless of the other input. While if one of the inputs are high, the other input value would be required to execute a proper output. Thus, the outputs of each delay path are fed back in a cross coupled manner to the second internal NAND input in the case a second input is needed for a decision. The path that has a 0 input reaches a decision first, then the decision is fed back to the second path to output a decision accordingly. As a result, the two outputs appear to have a gap called dead time between transitions from the delay in the paths that is set by the logic gates.

Input A	Input B	Output
0	**0**	1
0	**1**	1
1	**0**	1
1	**1**	0

Table 4.1 - NAND gate truth table

The clock generator is considered voltage-controlled oscillator (VCO) as the input voltage is linearly related to the output oscillation frequency. In Figure 4.2, the delay stage has a current starved (CS) inverter directly after the NAND gate used to make the oscillator voltage-controlled. The CS inverter, Figure 4.3, is named the following as the current through the inverter is limited, which slows the response time of the inverter. The current is limited by cascading a bias voltage controlled NMOS (Negative Metal-Oxide Semiconductor) and PMOS (Positive Metal-Oxide Conductor) devices, where the bias voltages are generated from a bias circuit shown in Figure 4.3.

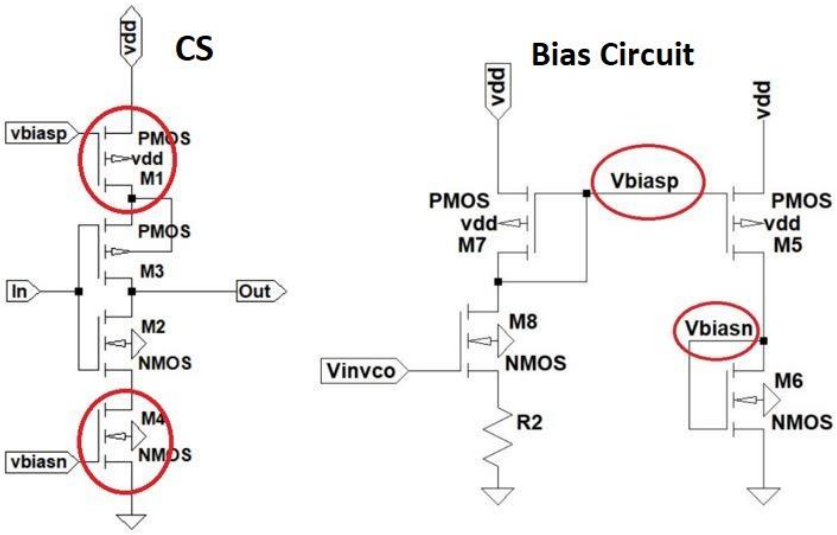

Figure 4.3 – Current starved inverter and bias circuit schematics

The circled nodes in the above bias circuit generate voltages V_{biasp} and V_{biasn} , these node voltages change respectively with the input $V_{vin,VCO}$. Since the current of the PMOS and NMOS devices, the circled devices in the CS inverter, is related to the bias voltages and the bias voltages change with $V_{vin,VCO}$, the current in the CS is controlled by the input of the bias circuit. To

understand how the delay is related to the current, the following explanation is provided. Any MOSFET (Metal-Oxide Semiconductor Field-Effect Transistor) device contains intrinsic capacitances, and with the added devices to the CS inverter acting as current sources, the inverter can be thought of as a linear current source charging/discharging a capacitor and bringing a constant voltage change as in Equation 4.1.

$$\frac{I}{C} = \frac{dv}{dt} \tag{4.1}$$

The charge current is inversely related to the propagation delays of the inverter and can increase or decrease their value. Thus, the delay of the inverter becomes adjustable, as a result the oscillation frequency can be controlled since the frequency is inversely proportional to the delay. The oscillation frequency can be varied with a minimum voltage, greater than the transistor's threshold voltage, of 0.3 V, and a maximum voltage of 3.3 V that equals VDD.

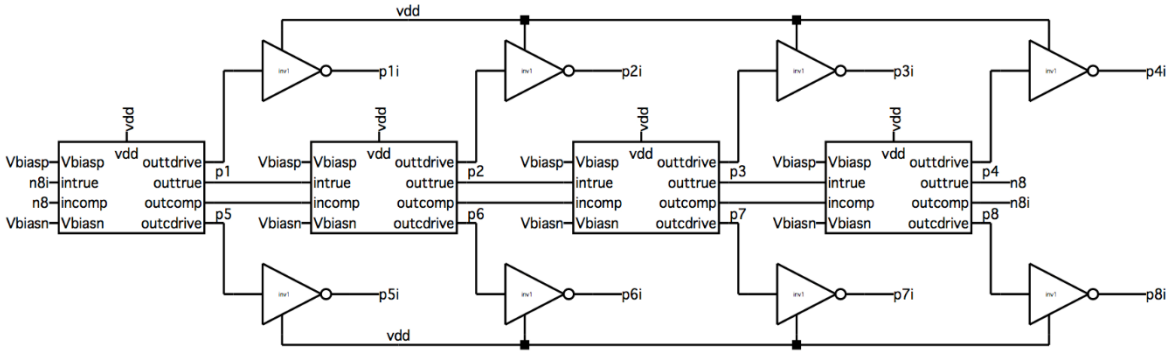

Figure 4.4 – Clock generator

Moreover, eight clock signals are needed and since one delay stage produces two clock signals, three more delay stages are used to generate the total 8 K_{path} clock signals. This leads to the second stage in clock generation, which is connecting four delay stages in a series manner. This is executed by attaching the true input/output and complement input/output signals together, as seen in Figure 4.4, then the ends are swapped and connected to the beginning inputs of the generator to create negative feedback. The negative feedback is needed for the oscillation to

happen, in the single ended ring oscillator this negative feedback is achieved with the use of odd number of stages. Each clock phase is inverted using a small inverter as seen in Figure 4.4 since this clock phase will be used in the feedback path control.

For running a simulation on the clock generator, an initial condition of zero has to be placed on one of the clock signals to get the oscillator to start, which is expected as the delay stage NAND gate requires one of the feedback inputs to operate properly as mentioned previously.

Figure 4.5 shows the output clock signals $\{p_1, p_2, p_3, \dots, p_8\}$ and $\{p_{1i}, p_{2i}, p_{3i}, \dots, p_{8i}\}$, the simulation was done with the maximum input voltage of 3.3 V to test the maximum frequency of the oscillator. The clock signals are seen to be successfully non-overlapping as the rising or falling edges do not occur at the same instance. The spacing between the signal transition edges are equal, this demonstrates that the clock generator is operating properly.

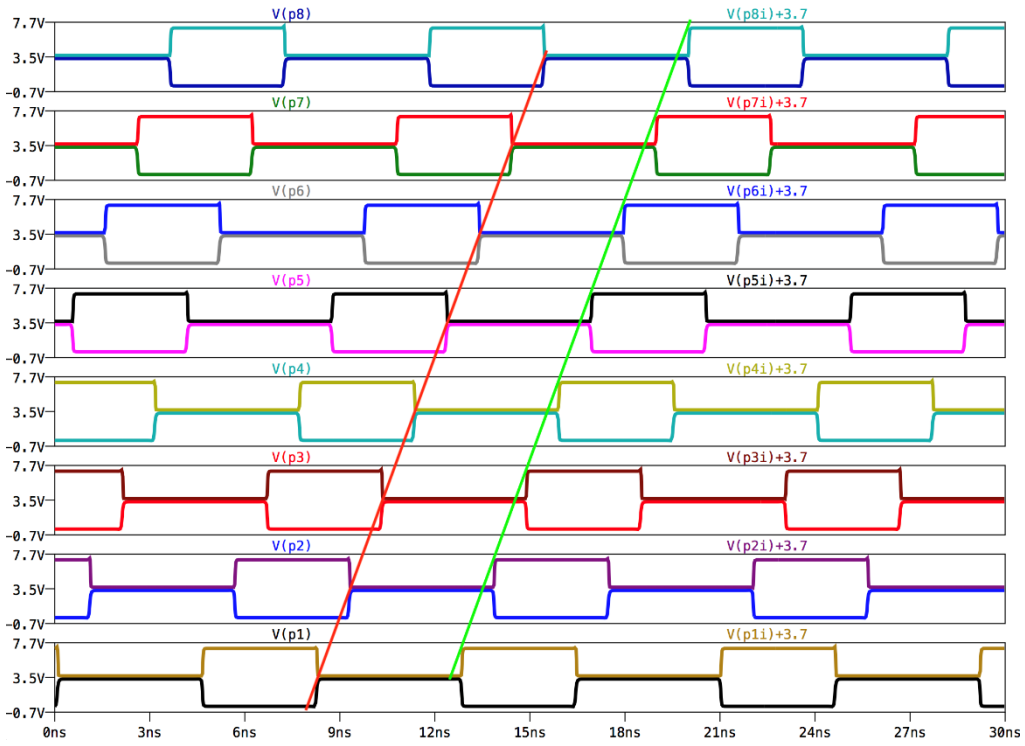

Figure 4.5 – Generated 8 non-overlapping clock phases

Figure 4.6 shows how there is a $486.34\ ps$ dead time between transitions. Lastly, Figure 4.7 shows how the frequency of the clock is varied as the input voltage $V_{vin,VCO}$ is varied from $3.3V$ to $0V$. The clock signals oscillate at $3.3\ V$, but once the input voltage drops to $0.3\ V$, the clock signals do not operate properly.

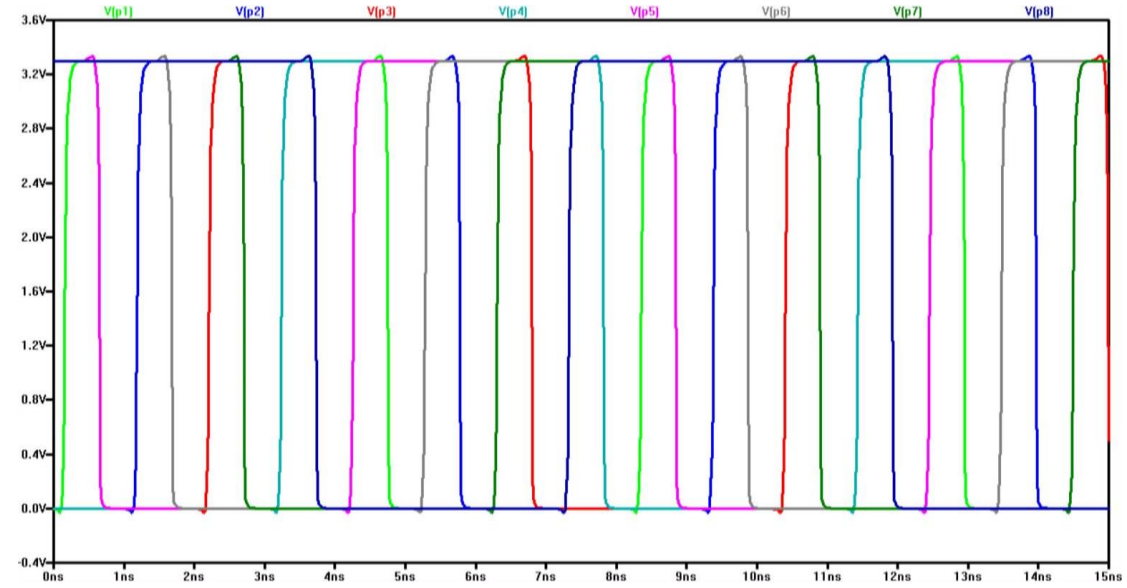

Figure 4.6 – Overlapping the 8 clock phases

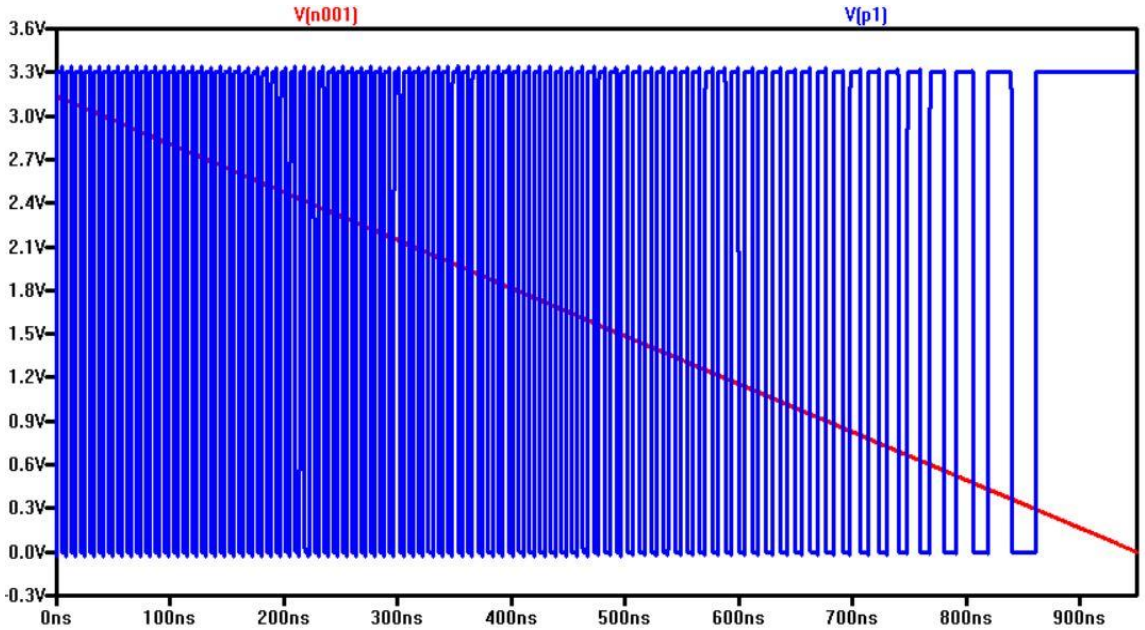

Figure 4.7 – Clock frequency vs. Input control voltage

Table 4.2 summarizes the range of the output frequency with respect to the input voltage. The frequency varies between $37MHz - 122MHz$, which is an $85MHz$ range.

$V_{vin,VCO}$ (V)	$f(Hz)$	$V_{vin,VCO}$ (V)	$f(Hz)$
0.5 V	37 MHz	**1.9 V**	111 MHz
0.9 V	68 MHz	**2.1 V**	118 MHz
1.2 V	86 MHz	**2.5 V**	119 MHz
1.5 V	99 MHz	**2.9 V**	120 MHz
1.7 V	107 MHz	**3.3 V**	122 MHz

Table 4.2 - Frequency with equivalent control voltage

Lastly, the eight generated clock signals satisfy the KD1S clock requirements as the edges are equally spaced and non-overlapping. The duty cycle of the clock signals is not perfectly 50%, but this is not essential in this continuous time KD1S as the design is edge triggered and independent of the duty cycle. Although if needed, the duty cycle could be altered by changing the number of inversions after the NAND gate.

4.2 INTEGRATOR

The integrator is composed of an operational amplifier (op-amp), resistor, and a capacitor. The integrator is one of the most important building blocks in the KD1S as it is the loop filter which enables noise shaping in delta sigma modulation. The op-amp is considered as the foundation of the integrator since it determines its performance. The capacitor is placed in the negative feedback of the op-amp, while the resistor is placed at inverting input of the integrator. Capacitor and resistor values determine the *RC* time constant of the integrator, and therefore should be picked carefully to avoid saturation and improper integration.

Figure 4.8 shows the op-amp design utilized for the integrator. The op-amp is a fully differential, self-biased amplifier. As the op-amp is self-biased, additional circuitry for DC biasing is not required. Thus, self-biasing can help with the design goal of reducing the power consumption as less devices are used. Moreover, the design is more stable as it is self-biased, it can be immune to temperature changes or process variations since nodes in the op-amp move together (nodes are physically tied together) as seen in Figure 4.8. This is important because stability of the amplifier controls the feedforward path. In addition, the outputs of this amplifier are produced from NMOS devices with a swing of $0\ V \sim 2.7\ V$, which is a benefit as it will interface better with the NMOS inputs of the comparator, which will be discussed in the next section.

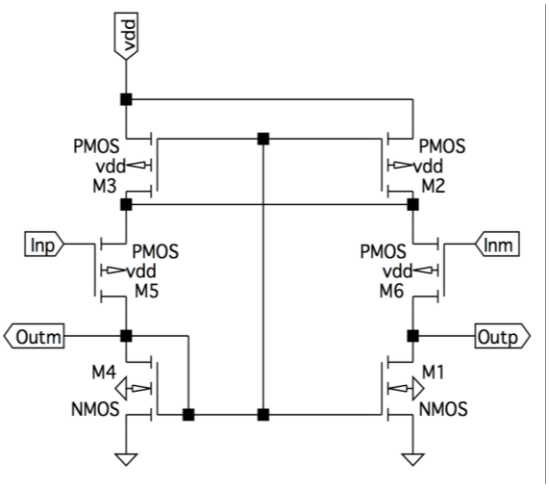

Figure 4.8 – Self bias operational amplifier

This op-amp topology is simple and fast. Minimum lengths are used in all NMOS and PMOS devices to reach high speed as the transition frequency of the devices increases when their lengths decrease. The chosen widths of the devices are large which leads to higher drain current, higher speed, and enables the amplifier to drive loads better. The amplifier needs to have good driving ability to avoid slew rate limitations. The trade-off of having high speed in the amplifier is low gain, but the gain of the amplifier is sufficient if larger than K_{path} or 8 in this design so the design gain is acceptable [1].

Figure 4.9 shows the output transfer curve and the derivative of the output which gives the DC gain of the circuit. The gain is approximately $20\,\frac{V}{V}$ and enough for the design requirements. The output transfer curve shows how there is no offset present at the output since the level switching happens in the middle at $1.65\,V$ (common mode voltage) with a DC input of $1.0\,V \sim 2.3\,V$. One of the amplifier input devices was made stronger to center the transfer curve so that no offset is present in the op-amp. The amplifier output saturates at $2.7\,V$ due to the output swing.

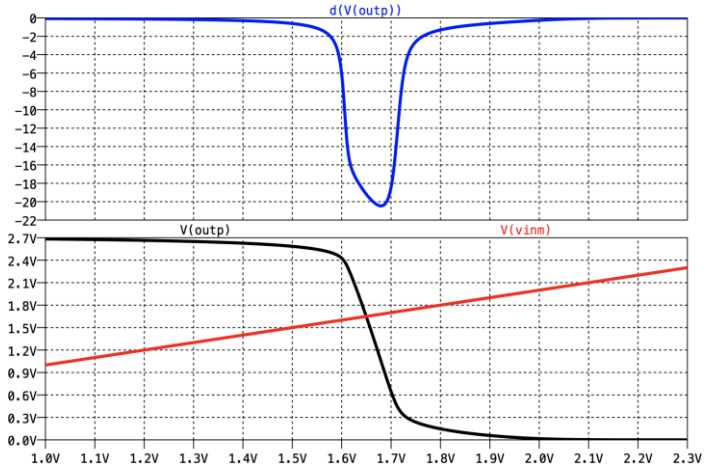

Figure 4.9 – DC sweep of op-amp output

The open loop frequency of the amplifier is shown in Figure 4.10. The op-amp has a unity gain frequency of $4\,GHz$ and the low frequency, open loop gain is $A_{OLDC} = 25.4\,dB$. The AC response was done with a load capacitance of $100\,fF$.

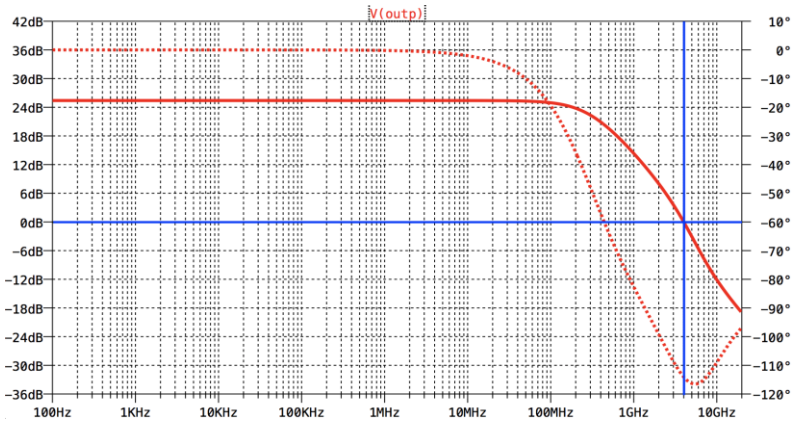

Figure 4.10 – Open loop response of self-biased amp

It is essential for the f_{un} of the op-amp to be high enough so that the integrator can properly perform the noise shaping without any SNR degradation. The unity frequency is required to at least be equal to $f_s/2$, but can be larger for better performance. According to [13], the f_{un} should be equal to $3f_s$ to achieve 99% settling time, and in this op-amp both conditions are satisfied.

The integrator consumes the most amount of power in the design, and one of the reasons being is the large unity-gain frequency of the op-amp [13]. A more specific calculation for the bandwidth required in relation to the desired N-bit resolution is in the following equation [13].

$$\frac{f_{3dB}}{f_s} > \frac{(N+1)\cdot ln(2)}{\pi} \tag{4.2}$$

Using Equation 4.2 with the results from Figure 4.10, Equation 4.3 shows that if the right-hand side of the equation is less than 3, the bandwidth of this design is sufficient.

$$\frac{300\ MHz}{100\ MHz} = 3 > \frac{(N+1)\cdot ln(2)}{\pi} \tag{4.3}$$

Also, the phase margin (PM) of the amplifier can be calculated from the AC response in Figure 4.10. The phase margin is $PM = 180° - |-114°| = 66°$, which means that the circuit is stable and fast since the PM value falls in the range of $45^\circ < PM < 90^\circ$. Having a PM of 45° provides faster rise and settling time, while a 90° PM provides unconditional stability as in an RC circuit [1]. Therefore, this PM of 66° ensures stability and fast operation of the device.

To ensure proper testing, the linear range for the op-amp's input was found to be approximately between $0.489V \sim 2.4V$ as shown in Figure 4.11. Therefore, any input in the measured range is appropriate for linear operation in the amplifier.

Moreover, the settling time must be fast so that the amplifier is capable of driving big loads. Fast operation is also required for the amplifier to keep pace with the circuit's speed, which is why the gain was sacrificed to achieve higher speed in the design.

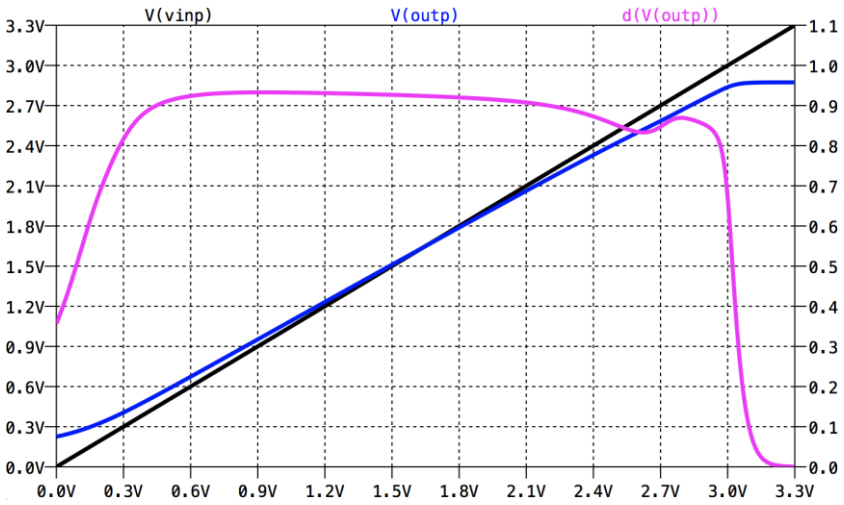

Figure 4.11 – Linearity test for the op-amp output range

The settling time can be calculated using the AC response in Figure 4.10 as the following:

$$f_{3dB} = \beta f_{un}, \tau = \frac{1}{2\pi f_{un} \cdot \beta}$$

$$\beta = 0.07625$$

$$\tau = \frac{1}{2\pi(4GHz) \cdot (0.07625)} = 521.82ps \tag{4.4}$$

The calculated settling time is estimated to be $521.82\ ps$ that is the time for the signal to fully settle and get to its final value after switching. Figure 4.12 shows the output of the circuit to a pulse input of $0.6V \sim 2.3V$, and a load capacitance of $100\ fF$. This figure can be used to measure the settling time.

The measured settling time is $490ps$, which is close to the calculated value in Equation 4.4. This circuit was loaded with a $100fF$ capacitor, while the comparator (the comparator is what will be connected at the integrator's output) is estimated to have $25fF$ input capacitance. A bigger load was used as it is favorable to design with margin expecting more input capacitance. The settling time measured reassures that the op-amp design is fast enough for the KD1S.

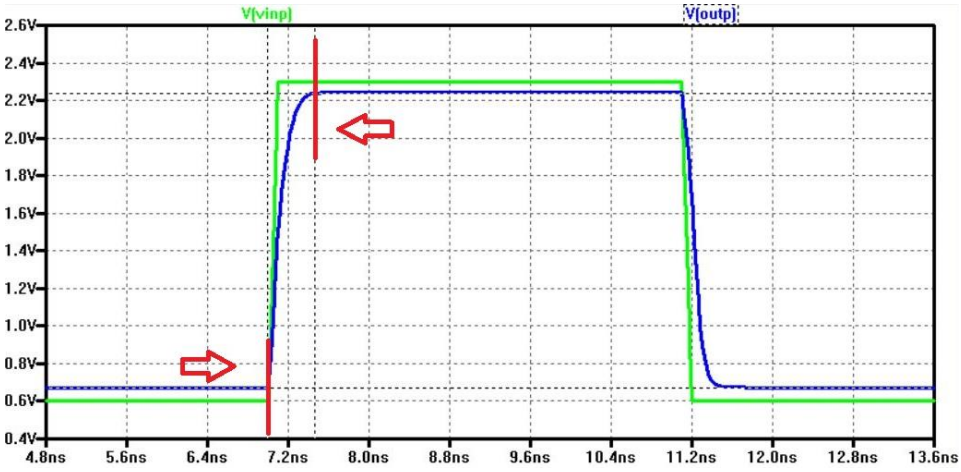

Figure 4.12 – Op-amp transient analysis

Equally important, the amplifier should not contain any slew rate limitations. Having a limited slew rate can lead to a gain error in the output. Although the output bandwidth would still be consistent with a gain error, the output could saturate and cause non-linearities that affect the SNR of the design.

Using the calculated settling time τ, Equation 4.5 can be used to check the op-amp for linear settling and minimal gain error [3]. The inverse of the settling time set the minimum value required for the slew rate. Substituting the known values into Equation 4.5, the SR value must be larger than or equal to the following $SR \geq 1/\tau = 1/521ps = 1.92 \times 10^9\ s$.

$$\tau \cdot SR \geq 1 \tag{4.5}$$

The same transient analysis in Figure 4.12 was used to measure the slew rate and check if the value satisfies Equation 4.5. To get the slew rate, the output is measured from 20% to 80% of its output swing. The result is a slope of $6.02965 \times 10^9\ s$ or $6.029\ \frac{mV}{ps}$, which is larger than the previous calculated value for linearity, thus equation is satisfied.

After verifying the performance of the op-amp, the integrator design is complete with adding the resistor on the input and the capacitor in the feedback of the amplifier (selecting a

resistor and a capacitor value will be investigated further in Chapter 5). The function of the integrator is to accumulate the error signal generated from the deviation between the input and output signals of the modulator. The integrator's output will keep increasing until the deviation is not present between the input and output signals of the modulator. For proper integration, the loop filter should not experience any slew rate limitations as mentioned previously. Appropriate RC values should be selected, and an input range for the integrator must be characterized to prevent signal saturation. Saturation can lead to wrong results and lower the SNR of the design. Lastly, offset in the integrator is not desirable as the offset value will be added directly to the output of the modulator. This can cause a shift in the output since the offset is not referred to an input and decreased by a gain.

The integrator is what enables the input signal to be band-limited/filtered before being sampled by the comparator, which is how there is built-in anti-aliasing filter leading to double the filtering in the continuous time design. This is the fundamental advantage of the CT topology to the DT topology. Due to the importance of the integrator, the design must be stable, fast, and implemented carefully. Other op-amp designs could have been used for the integrator in this circuit and reach better results, but the selected self-biased op-amp design is simple, fast, functional, and contains nominal circuity which is why it is used for this KD1S design

4.3 CLOCKED COMPARATOR

The clocked comparator design is the second most important component in the continuous time KD1S because it is the component which determines the output of the modulator. The comparator is considered the only non-linear component in the KD1S since it is the quantizer that introduces quantization noise to the converted signal. The comparator needs to have decisive signals within a

short amount of time, and the ability to resolve small signals. The design of the comparator is displayed in Figure 4.13, it is based on a sense amplifier topology with better sensitivity, wide input signal swing, better immunity to kickback noise, and a rising-edge triggered output [1]. The comparator consists of three stages, a pre-amplification, decision making or positive feedback, and an output buffer stage. The decision-making stage is marked with a red box in Figure 4.13, this stage is a sense amplifier (SA) designed as a cross-coupled inverter, which prompts fast operation.

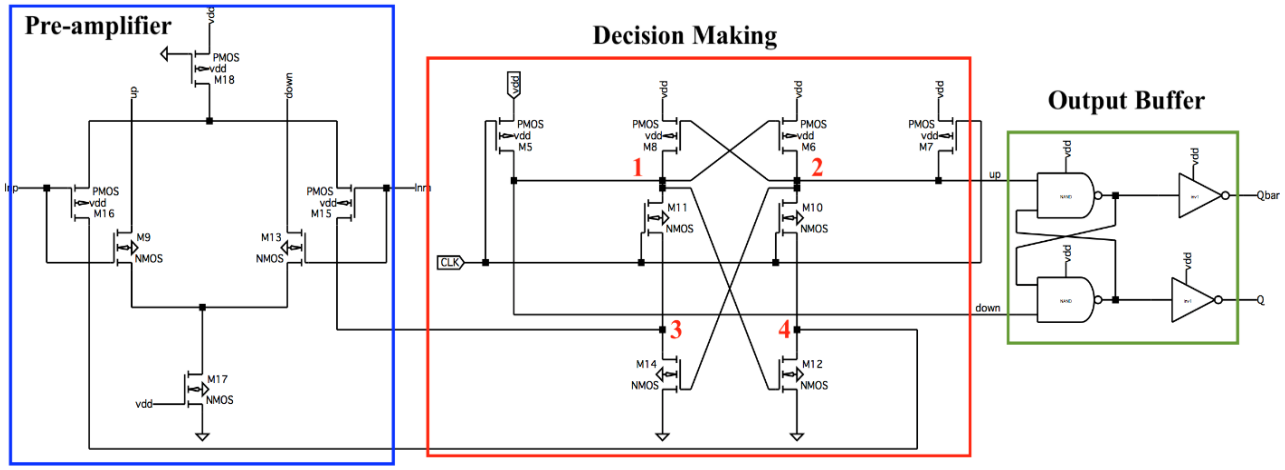

Figure 4.13 – Clocked comparator schematic

The operation of decision-making stage is explained for two cases, when the clock signal is low, and when the clock signal is high. In Figure 4.13, nodes 1 and 2 are the outputs of the SA, while nodes 3 and 4 are the inputs. The process of the circuit is first shown when the clock (*CLK*) signal is low, the flow is annotated in a color coordinated fashion in Figure 4.14. The low clock input causes M5/M7 PMOS devices to turn on while M10/M11 NMOS devices to turn off. This causes nodes 1 and 2 to be pulled to *VDD* as M5/M7 devices are on. Since the gates of M6/M8 PMOS devices are connected to nodes 1 and 2, the devices shut off with their gate potential at *VDD*. On the other hand, M12/M14 NMOS devices turn on because their gates are connected to nodes 1 and 2, which have been pulled to *VDD*. Lastly, devices M12/M14 turn on

leading nodes 3 and 4 to go to *GND*. The state when *CLK* is low is called memory erasing as all nodes are pulled to a known value independent of previous state.

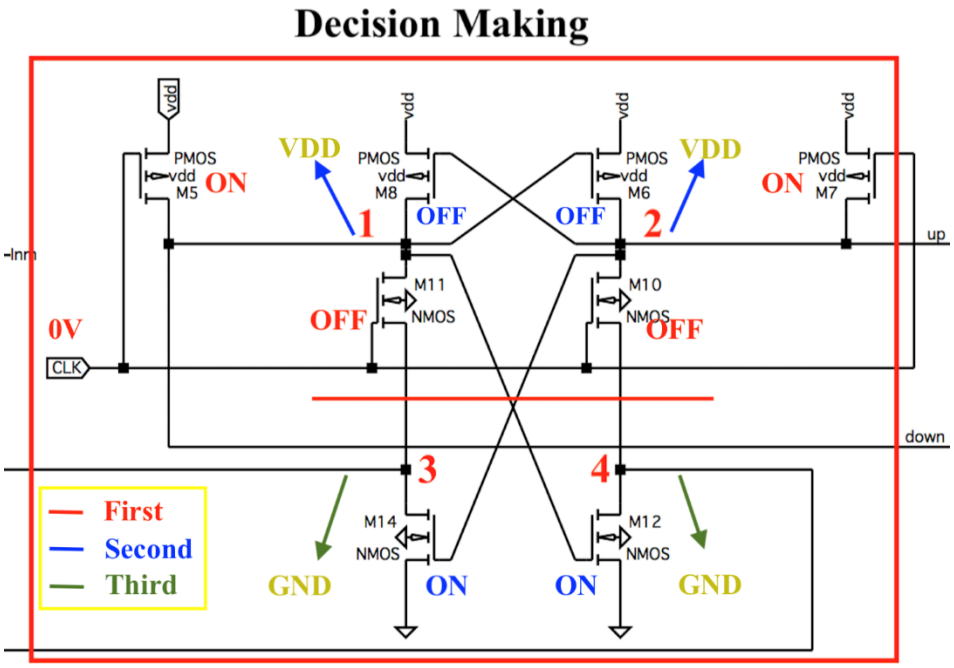

Figure 4.14 – Decision making operation with clock low

Next is the operation of the circuit when *CLK* is high, the operation is annotated in the same manner from previously in Figure 4.15. The high clock input voltage causes M5/M7 devices to turn off, while M10/M11 turn on, and previously turned on devices, M12/M14, stay on. The M10/M11 NMOS devices pull the potentials of nodes 1 and 2 down causing M6/M8 to turn on. At this point the outputs are both high, and when an input causes an imbalance in the circuit, where one side is stronger than the other, the latch snaps to a state and the output changes. For example, if M12 device is stronger than M14, the potential at node 4 decreases causing the potential of node 2 to pull down as well. Since the gate of the M8 PMOS device is connected to node 2, the device turns on and pulls node 1 to *VDD*. Node 1 causes M6 to turn off, which pulls node 2 to *GND*. Meanwhile, node 1 turns on device M12 even more and node 2, which is pulled further to ground, leads M14 device to shut off. This imbalance example caused node 1 to output *VDD*/high, and

node 2 to output *GND*/low. The following demonstrated how the latch snaps to a certain state and the outputs change. The opposite results would have happened in the same manner, if M14 was stronger than M12, node 2 output would be *VDD* while node 1 outputs *GND*.

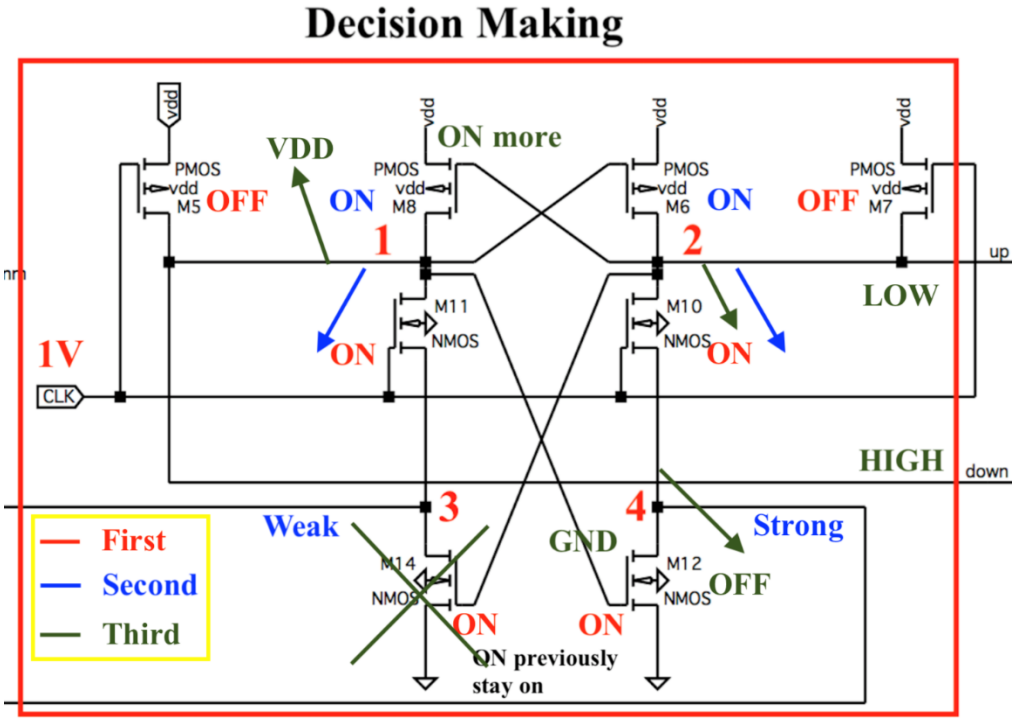

Figure 4.15 - -Decision making operation with clock high

The selected SA design possesses great immunity to kickback noise (injected noise through inputs when the states switch) as the inputs are in the pre-amplification stage away/detached from the positive feedback. This prevents the noise/glitches from the input signals to add up [1], [2]. Moreover, there is no DC path from *VDD* to ground in the SA design as clocked transistors, M10/M11, isolate the PMOS from the NMOS latches preventing current to be pulled between the nodes during switching states [1]. When the *CLK* signal is low the NMOS devices M10/M11 are off and separate the top and bottom of the circuit, which isolate the latches. Also, the design nodes are always at known values without memory of the previous state, which is achieved in the memory

erasing state mentioned earlier when *CLK* is low. This is important because having the nodes in the SA at an equilibrated value guarantees precise decisions independent of previous states [1].

The next stage to be discussed is the pre-amplification stage found in Figure 4.16. The sense amplifier circuit discussed earlier operates on current imbalance, whereas the pre-amplification circuit operates on input voltage differences. Pre-amplification (pre-amp) consists of two PMOS and NMOS differential amplifiers (diff-amp) that help provide better sensitivity, wider input swing, and isolates the input from the positive feedback [1]. The diff-amp circuits utilize long L devices, instead of the biased NMOS or PMOS current mirror, to set the bias current. The devices are fully on and can be considered as current sources.

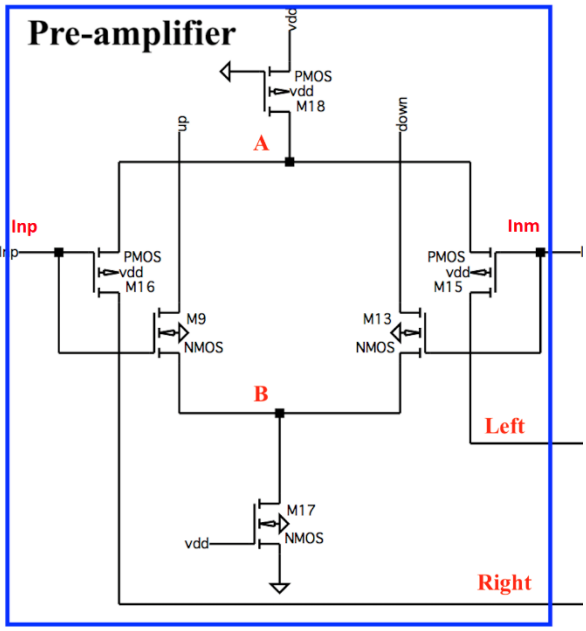

Figure 4.16 – Comparator's pre-amplifier stage

The input devices in both the NMOS and PMOS diff-amp increase the sensitivity of the circuit, they provide gain that helps amplify small input signals, which makes the comparator more sensitive to small voltage changes. Moreover, using both diff-amps is not necessary as the comparator is capable of normal operation with only one of the diff-amps, but two were used to provide wider input swing. The NMOS diff-amp would operate better with input common-mode

voltage that is too high, while the PMOS diff-amp would operate better with input common-mode voltage that is too low [1]. In addition, the input signals are isolated from the positive feedback, which prevents noise to add up in the circuit as mentioned previously. The pre-amp stage can be considered placed in the current path of the SA, which is how the current difference, current generated depending on the input signals, can create an imbalance in the SA so it can reach a decision. Looking at Figure 4.16, when the positive input, Inp, is higher than the negative input, Inm, node 1 goes to *VDD* while node 2 goes to *GND* in Figure 4.13. This happens because M12 NMOS sinks current faster than M14, in Figure 4.13, so the latch snaps in the mentioned way. When Inp < Inm, the output on node 1 goes to *GND* while the output on node 2 goes to *VDD*.

The last stage of the comparator is the output buffer seen in Figure 4.17, which is a Set-Reset latch (SR latch). The SR latch is added at the end of the comparator to create rising edge triggered output; meaning that the output only changes state on the rising edge of the clock signal. The inverters in the SR latch serve as buffers to square the output signal and decrease loading on the circuit. The operation of the latch is demonstrated in Figure 4.17 using simple logic of 0's and 1's. Starting with red first, the SR inputs are 0 and 1 as shown in the figure, these inputs are the result of the decision-making stage when *CLK* is high as shown in Figure 4.15. The upper NAND gate with a 0 input can decide without a second input value thus outputs a logic 1. The logic 1 from upper NAND is fed back to the lower NAND resulting in a logic 0 output. Both NAND outputs are inverted as they propagate to the final comparator output. Moving to blue in Figure 4.17, the inputs to the SR latch are now both logic 1, which is from the memory erasing state when *CLK* is low. Previous state outputs are still present in the latch, thus feed back to the NAND inputs respectively. Upper NAND outputs logic 1, while lower NAND outputs logic 0. Ending with the brown inputs of 1 and 0 for upper and lower NAND gates accordingly, these inputs are from the

positive feedback stage when *CLK* is high and the latch snapped to a different state. Lower NAND with 0 input decides a logic 1 output, and the output is feedback to the upper NAND input. The upper NAND with both inputs high. As portrayed, the outputs only changed state when the *CLK* is high, while maintain the previous state when *CLK* is low. As a result, the output is considered edge triggered that changes state only on the rising edge of the clock (when *CLK* signal changes from low to high).

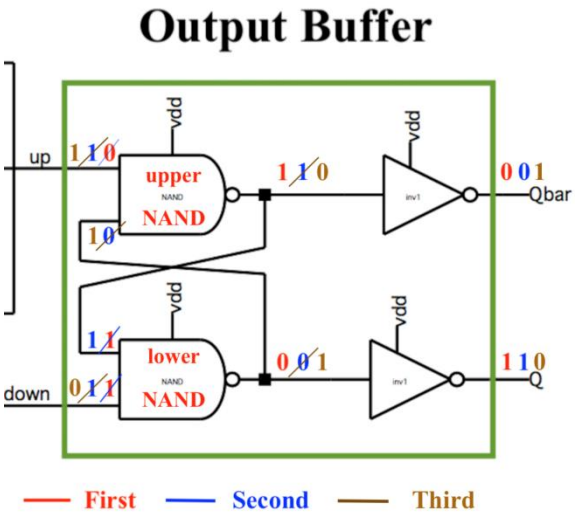

Figure 4.17 – Comparator's output buffer stage

Furthermore, the comparator needs to meet certain requirements to properly operate in the KD1S design. The most important aspect of the comparator is decisiveness; the comparator should be able to make a reliable decision during a certain time before the feedback path is disconnected. In addition, minimal delay should be anticipated in the forward path through the comparator to meet the KD1S timing requirements [1].

Any offset or noise in the comparator can change the input signal, thus these parameters need to be considered. The offset of comparator is not as critical as in the integrator design, because the offset as well as the comparator's input-referred noise, Figure 4.18a, can both be referred back

to the modulator's input as seen in Figure 4.18b. In general, internal noise in the circuit can be modeled at the input for further analysis (the noise is not actually at the input, but only modeled to represent the noise on the output) [1]. Since the noise and offset are referred to the input of the modulator, analysis show that the gain of the integrator reduces their effects. This is the reason noise of the comparator is not critical. The integrator's input-referred noise and offset is already at the integrators input and does not have a place to be referred back to.

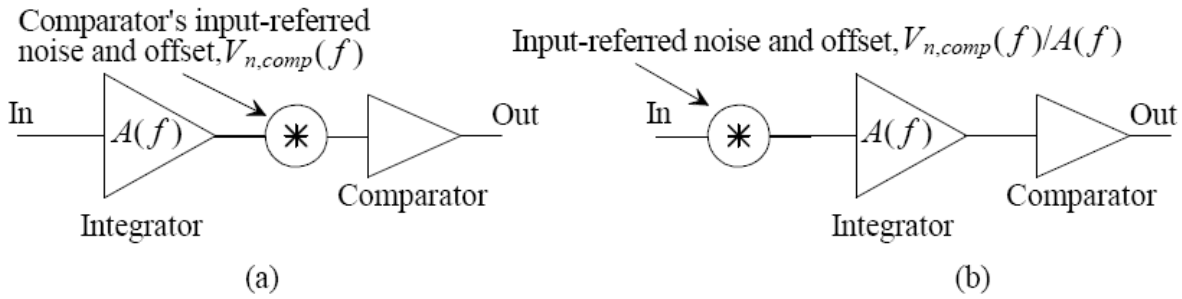

Figure 4.18 – Input referred noise of the comparator [2]

Simulations will be shown next to test the comparator's performance. The first simulation is a transient analysis of the comparator to measure the resolution, and the time required for the output to switch after triggering. Figure 4.19 shows a general operation of the comparator; the positive input is swept between $1.6361V \sim 1.6639V$ (a $27.8\,mV$ difference), while the negative input is held at the common-mode voltage of $1.65\,V$.

Both positive and negative outputs are shown in light and dark blue, clock in the red plot, and the input signal is shown in green in Figure 4.19. Both outputs of the comparator can accomplish a full output transition, which is the most essential feature needed in the quantizer. Having a high gain in the comparator is not required, a small gain is acceptable if the output is able to transition fully between rails as seen in Figure 4.19. Full output transition allows the modulator to function properly [1].

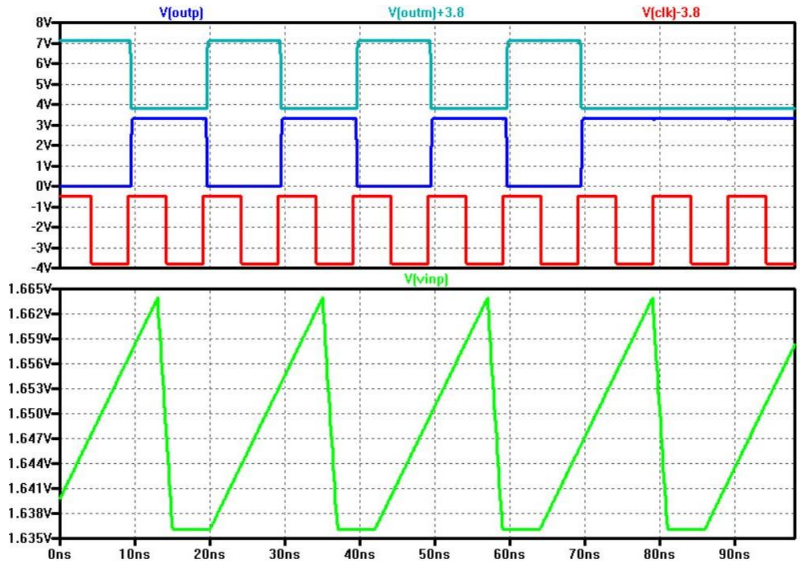

Figure 4.19 – Comparator ramp test for decisiveness

Like Figure 4.19, a transient simulation was performed in Figure 4.20 with a ramp going from $0V \sim 3.3V$ that is the full input swing, the clock was set at a high frequency, and both outputs were monitored until the first switching happened. The first switching happens when the minimum resolution of the circuit is reached (the smallest voltage the comparator can discriminate).

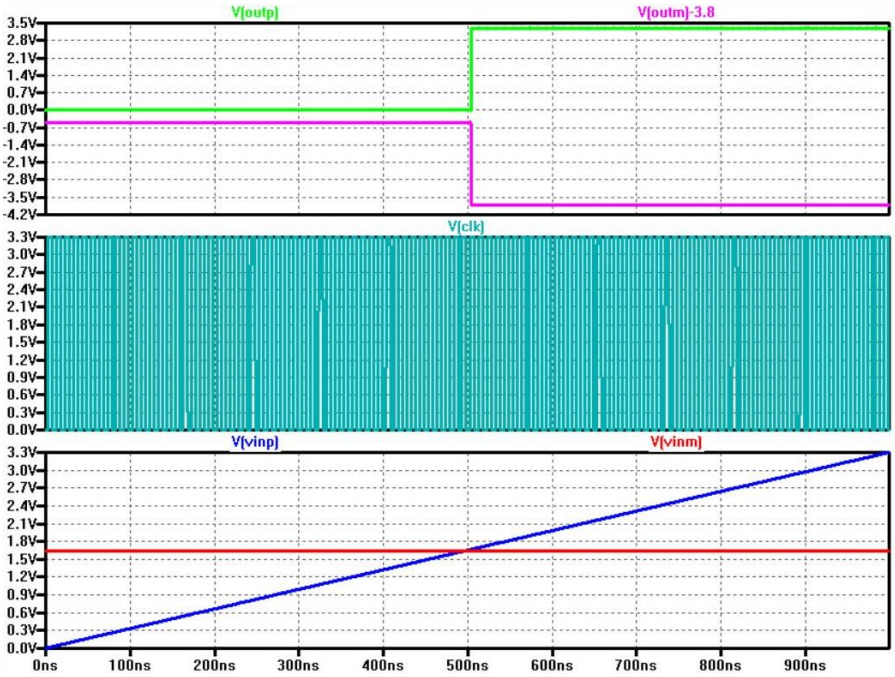

Figure 4.20 - Output switching test for comparator

Figure 4.21 utilizes the same simulation setup from Figure 4.19, the plots are zoomed it at around $500\ ns$ and the resolution is found to be $13.8\ mV$, which is half the sawtooth wave input in Figure 4.19. The total delay through the comparator is equal to $664.54\ ps$, which is good as the required settling time of the comparator is $\frac{T_S}{K_{path}} = \frac{\frac{1}{110MHz}}{8} = 1.1363ns$ (when the sampling frequency is 110 MHz). Measuring the time from the rising clock edge to both the positive and negative outputs, the switching times were measured to be $445.5\ ps$ and $350.46\ ps$ subsequently.

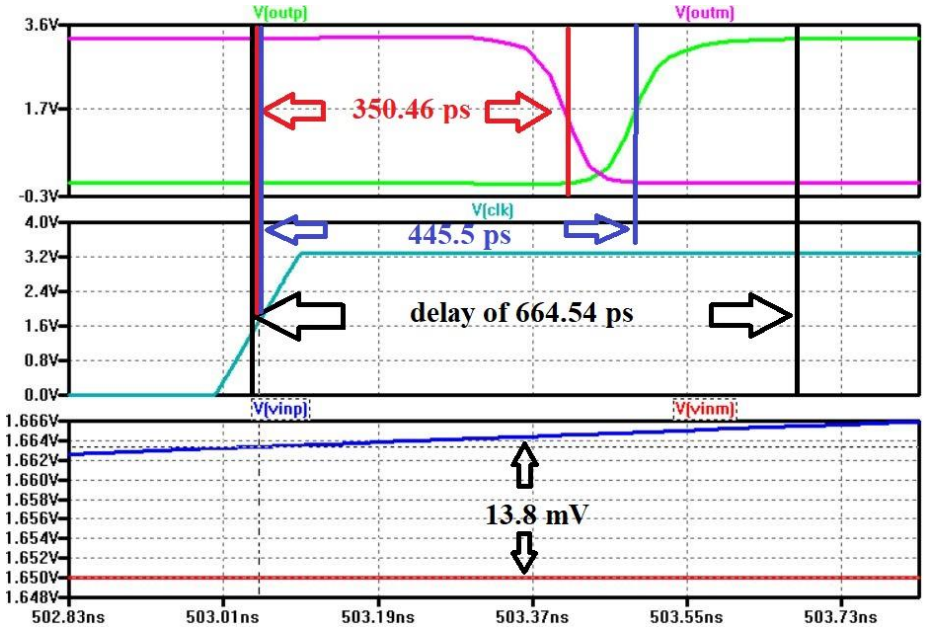

Figure 4.21 – Comparator delay and time measurements

The last measurement for the comparator is the rise and fall time when a full transition occurs. Using Figure 4.19 again, the rise time of the output is 95.4 ps while the fall time is $73.39\ ps$. All the results evaluated from the transient analysis indicate that the comparator is within bounds of the timing requirements, as well as the comparator's output can conduct a full transition within minimal time, adequate resolution, and fast slope.

Ultimately, the comparator expects an input signal that is not slew rate limited, since the output could oscillate, thus the integrator design was focused on fast transitions without slew rate problems. The comparator's most important concern is decision making even if the decision made is wrong as eventually the modulators output will be averaged, and such error would not affect the overall performance.

4.4 FEEDBACK PATH CONTROL AND TRANSMISSION GATES

The continuous time KD1S utilizes transmission gates (TGs), the clock generator, and the clocked comparator to control the *K* paths. The transmission gates, Figure 4.22, are used for two purposes, the first is to control the feedback paths using the clocks, and the second is to feedback less signal for preventing the integrator from saturating. The integrator in the forward path can receive excessive fed back signal, which can cause the integrator to saturate. The saturation can be prevented by either increasing the feedback capacitors or feeding less signal back. To decrease the fed back signal switches are clocked in series with a resistor in each path, in this manner the signal is connected to the forward path for a certain amount of time. During this time the signal passes a delay which limits its speed. The switches in the feedback are made using two parallel transmission gates that pass high and low signals thoroughly with a rail to rail output swing.

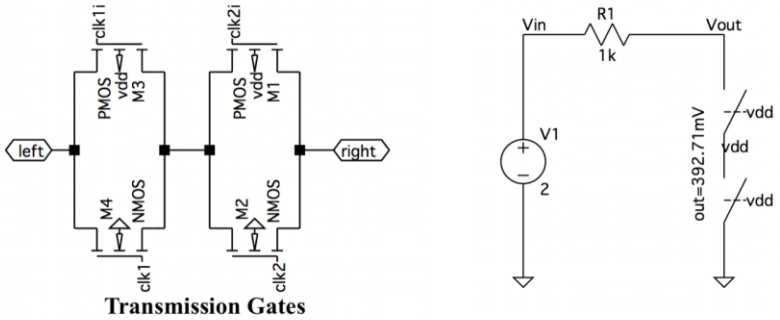

Figure 4.22 – TG schematic and resistance testing circuit

The transmission gates are shown in Figure 4.22; two internal inverters were used to generate opposite clocks for controlling the gates. The resistance of the switch was measured using the voltage divider shown in Figure 4.22 with a known resistance and input voltage, the overall resistance of the switch equals 244Ω. The transmission gate sizes were picked carefully to avoid the switches acting as capacitors, which would then require more driving from the clock generator to turn on the TG gates. The TGs need to have a rapid response with fast edges so that the current is passed to the resistor with minimal delay and result in a well-defined signal. Therefore, the delay of the TGs was measured with a large load capacitance of $100f$ to test limitations, the TGs were fully turned on by connecting the PMOS and NMOS gates to ground and *VDD* respectively. The overall delay through the loaded switch is equal to $46.48ps$. The speed of the TG was checked for adequacy by measuring the current through the feedback resistor during fast and slow clock signals to ensure enough charges are passing.

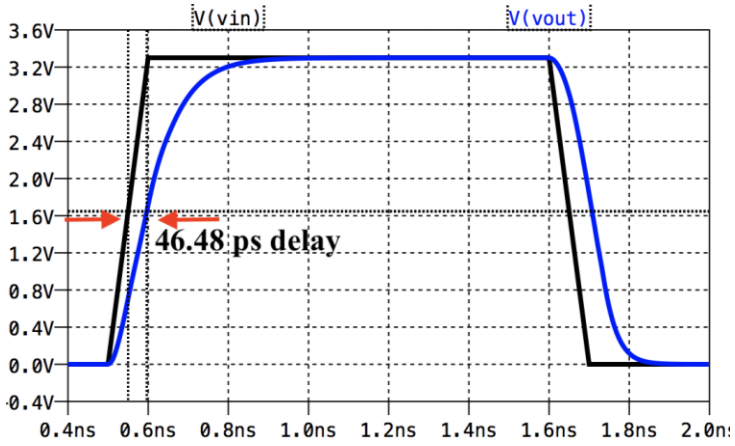

Figure 4.23 – TG transient analysis

To prevent resistance mismatch between feedback and feedforward paths, a dummy switch, that is always turned-on, was added to the feedforward path. The dummy switch has the same sizes as the TGs placed in the feedback loop. This compensates the feedforward path for the resistance in case the switches experience process variations.

Moreover, the feedback control process will be explained with the help of Figure 4.24 and Figure 4.25. Figure 4.24 is a sample path from the KD1S design with all the components connected appropriately, and Figure 4.25 presents the clock signal combinations for controlling the feedback switches and comparator. Note the dummy resistor is placed in the feedforward path after the input resistor in Figure 4.24. The feedback resistors are placed before the switch so that the V_{sum} junction only sees the resistor when the path is connected to the input of the integrator.

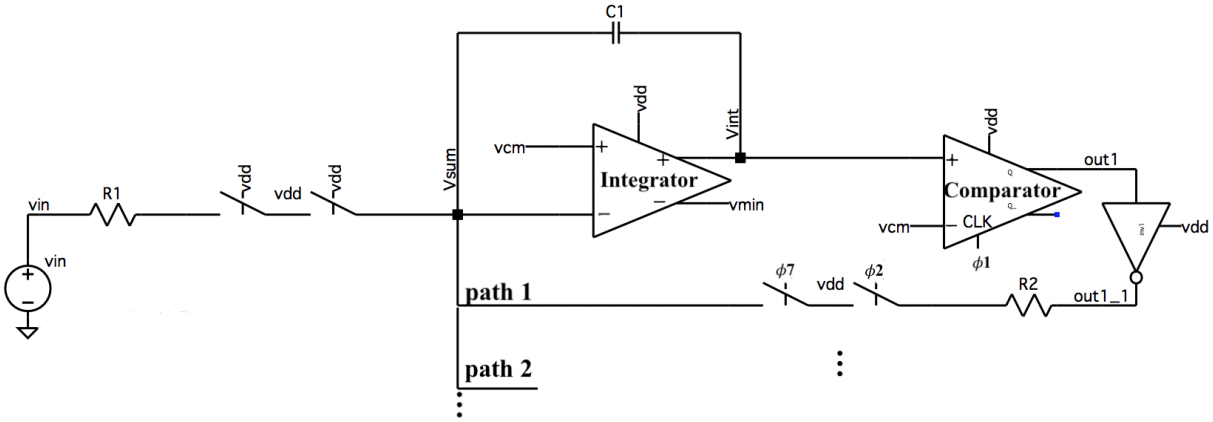

Figure 4.24 - One path example of the KD1S

Focusing on path 1, clock signals of Figure 4.25, $\{p1, p2, p3i\}$, $p2$ and $p3i$ are used to connect the feedback path to the feedforward path, and $p1$ triggers the comparator. The process is as follows, path 1 is clocked and connected to the feedforward path using clock phase $p3i$, after $1.5\ ns$ the comparator is clocked with $p1$ and has a time frame of $1.03\ ns$ to decide on an output. Then clock $p2$ goes high and allows a $1.05ns$ time window for the results to feedback through the resistors before the path is disconnected as clock $p3i$ goes low. In this manner, the paths are never connected to the feedforward loop at the same time, which prevents useless or wrong information to be associated and affect the decision of a different path.

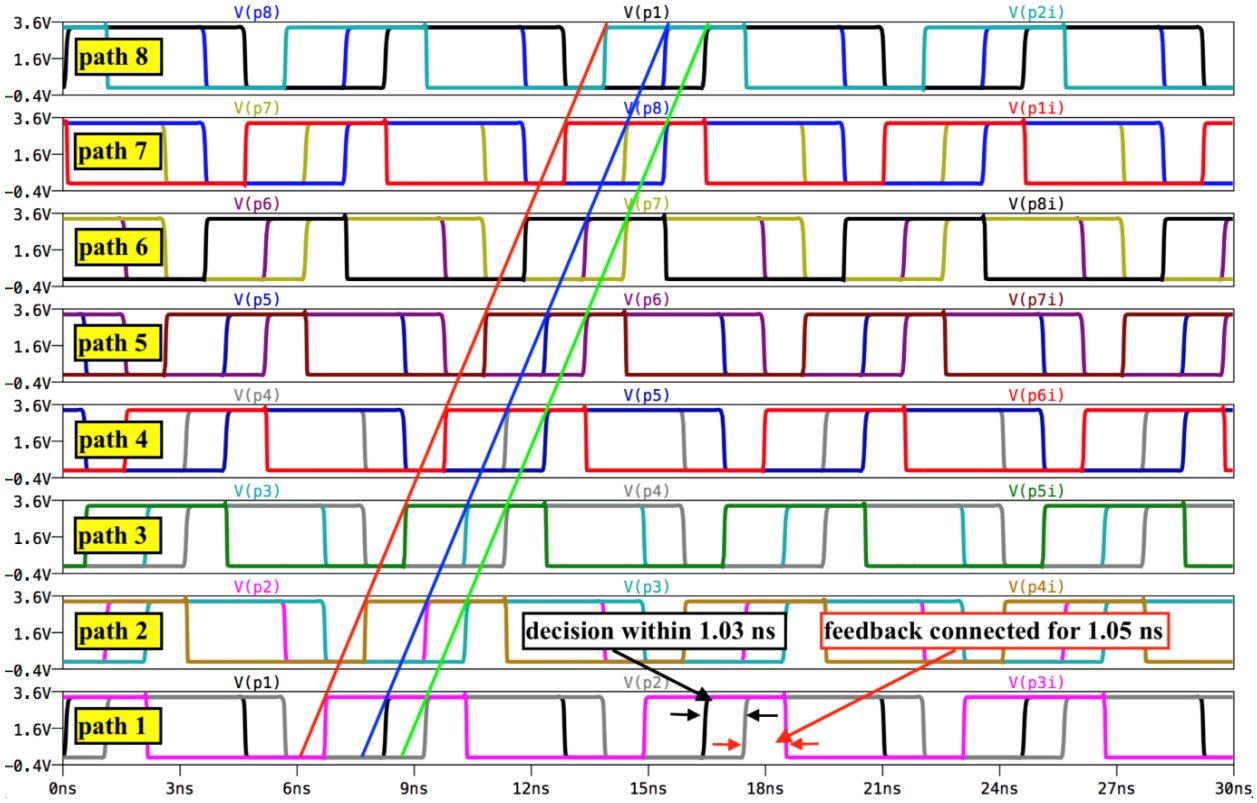

Figure 4.25 – Clock phases combination for logic control

Proper measurements were made to establish the timing of the control clocks; for example, the non-overlapping delay was designed slower to increase the spacing. The decision window for the comparator matched the required calculated value from previously, which ensures that the comparator will be able to make a reliable decision. In this form, eight signals are processed effectively, each of the path switches is closed for $\frac{T_s}{8}$ period and the parallel combination of 8 paths corresponds to a single path with eight times the frequency and one resistor, $\frac{R_{feedback}}{K_{path}}$. Eight paths were chosen in the design as it is a reasonable number to be applied for different applications. Using eight paths is effective as any mistake made in a certain path is shared between all the paths and a different path can compensate for the error, which will eventually be averaged.

Lastly, the inverters in the feedback were used to buffer the comparator output for sharper square signal and minimize the resistive loading on the output. The inverter also helps in maintaining the inversion in the loop, and is considered the DAC since it outputs an analog signal of either *VDD* or *GND*.

4.5 REGISTER

The output of the KD1S is random with high effective frequency, and in order to process the output bits digitally, the data has to be retimed properly. The output data will be decimated and filtered further using MATLAB software, therefore for easier interface an 8-bit register is used to store the bit stream and perform the decimation. The 8-bit shift register consists of 8 Data Flip Flop (DFF), where each store one bit as shown in Figure 4.26. The 8 DFF are synchronous to one clock phase that is the first phase of the clock generator, $p1$. The decimation in the register is equal to 8 as the register is only clocked after the 8 paths have made a decision. Decimation occurs because the input data to the register is coming fast and saved in the DFF every 1 ns, which is the time difference between the comparator clocks, and the register output is clocked every 8 ns to retime the output data.

Moreover, the DFF design has an output buffer stage to decrease loading and square signals rail to rail for precise output. The register output can be processed in MATLAB in a parallel or serial manner. In parallel mode, the bit order is not considered, and a filter is applied to the data by adding all the bits and averaging them together. In serial mode, the bits are descrambled and placed in order. For example, if the following are two output signals were given:

signal 1: 1111 0000

signal 2: 1010 1010 (4.6)

In parallel mode, the average of the signals is executed by adding all the bits together and dividing by the total number of bits as the following $\frac{1+1+1+1}{8} = \frac{1}{2}$, this makes signal 1 and signal 2 appear to be the same. In serial mode the signals are distinguishable as the bit order is held. This is the reason; the SNR of the serial mode is higher than Parallel mode SNR. Parallel mode SNR is poorer since bit information is lost in parallel mode due to the bits averaging, which creates noise in the spectrum.

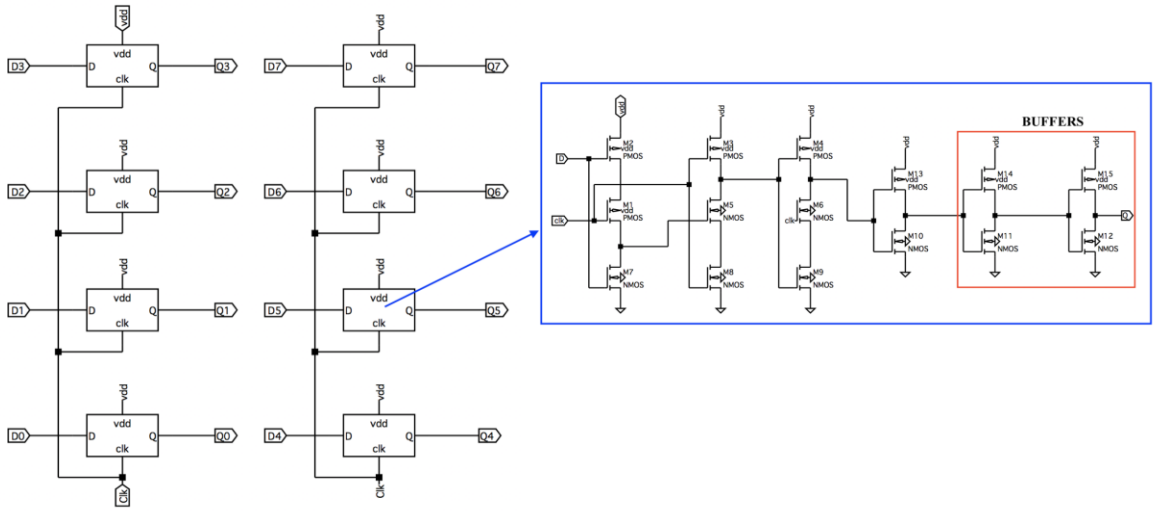

Figure 4.26 - 8-bit shift register schematic

4.6 SIMULATION RESULTS IN C5 PROCESS

This section summarizes the simulation results obtained using the C5 process, each component and its parameters are indicated in Table 4.3. The same design analysis and settings were used to obtain the results in the table. Meaning the same capacitor values, or source settings were used. The difference is mainly found in the power supply and common mode voltages. The C5 process follows the design requirements in the same manner as in AMS.

The C5 process results also ensure that the KD1S is possible with the parameter condition. Notice that the maximum clock frequency found in the clock generator of the C5 process is 20 MHz less than the frequency of the AMS process. The range of the oscillator is also not as tunable as in the AMS process. Overall, the AMS results were shown to be slightly better than in the C5 process, but this is expected as the processes are of different sizes.

SIMULATION RESULTS FROM C5 COMPONENTS **VDD = 5V, Vcm = 2.5 V**	
Clock Generator	
Clock Frequency	70 MHz ~ 106 MHz For a $V_{in,vco}$ of 0.5 V~ 5V
Dead time	581.83 ps
Integrator	
Output swing	0 V ~ 4 V
Gain	18 V/V
f_{un}	3.4 GHz
Linear range	1.2 V ~ 4.1 V
Settling time	706.01 ps
Slew rate slope	$13.368 \times 10^9\ s$
Clocked Comparator	
Resolution	37.85 mV
Switching time	500 ps
Rise time/ Fall time	116.51 ps/ 105.22 ps
Delay	693.68 ps
Transmission gates	
Delay	50 ps
Feedback Control	
Decision Time	1.18 ns

Table 4.3 - Summery of the C5 component parameters

CHAPTER 5: DESIGN OF 1ST AND 2ND ORDER KD1S

Previous chapters established the foundation for first and second order KD1S modulators, and each component was discussed and evaluated thoroughly. The KD1S design was simulated using two IC processes, Austria Micro Systems (AMS) S35 $0.35\mu m$ SiGe BiCMOS, and OnSemiconductor C5 (C5) $0.5\mu m$ CMOS. The main design is executed in the S35 process and the C5 process was done for comparison purposes. The schematics and simulations shown in this chapter will utilize the AMS technology process for demonstration purposes. The same design requirements and analysis were applied to circuit designs in both processes.

5.1 FIRST ORDER CT KD1S

The main components of the KD1S modulator were investigated in Chapter 4, the remaining design task is to choose the feedback parameters. Continuous first order KD1S feedback parameter synthesis begins with a one path CT active DSM, similar to components in Figure 4.23. The purpose of using just one path is to test different combinations of resistors (*R*) and capacitor (*C*) values which results in proper feedforward and feedback loop operation.

The output of the integrator should be limited within the linear range of the integrator as in Figure 4.11, with the output centered around the common-mode voltage. The time domain output equation for an active integrator using KCL is as follows (negative signs cancels as inverting input used):

$$V_{out} = \frac{1}{RC}\int V_{in}\, dt \tag{5.1}$$

Knowing that the output range is limited, and the integrator input is constantly changing after the feedback loop delay, different *RC* values will affect the output. Using small *RC* values in the loop can obstruct the integrator from normal behavior as the output will overflow. This happens because the integrator is constantly accumulating the error signal at a fast rate. This leads to saturation and the output losing centering on V_{cm}, especially at the peaks of the input sine wave for not being able to "keep-up". Using large *R* and *C* values requires more integration time and since the error signal keeps changing, the output amplitude is limited and revolves around the common-mode voltage. Properly selected *R* and *C* values result in the integrator output swinging around the common-mode voltage at a moderate level while staying within output boundaries.

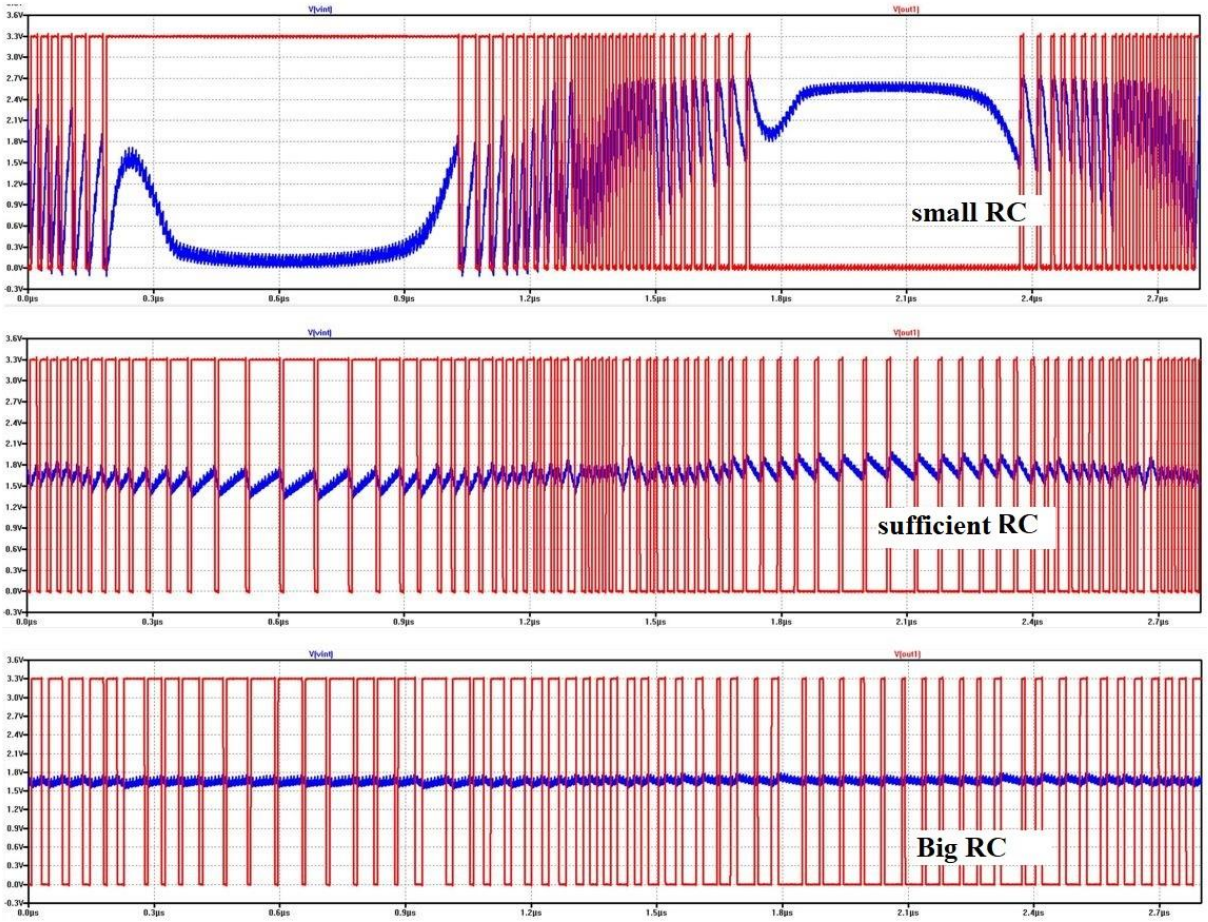

Figure 5.1 – Different RC combinations and output operation

The plot in Figure 5.1 shows the output signal and voltage at the integrator input of the one path DSM topology as in Figure 4.24 The circuit is used to demonstrate the output behavior of the integrator with different *RC* values. The topmost plot used $2k\Omega$ and $1pF$, the middle plot utilized $10k\Omega$ and $5pF$, and the bottom plot has $20k\Omega$ and $20pF$. As expected, the behavior of the integrator is affected by the selected *RC* combination. Proper integrator output behavior is seen with the *RC* of $10k\Omega$ and $5pF$, the output is increasing gradually following the input signal around V_{cm}.

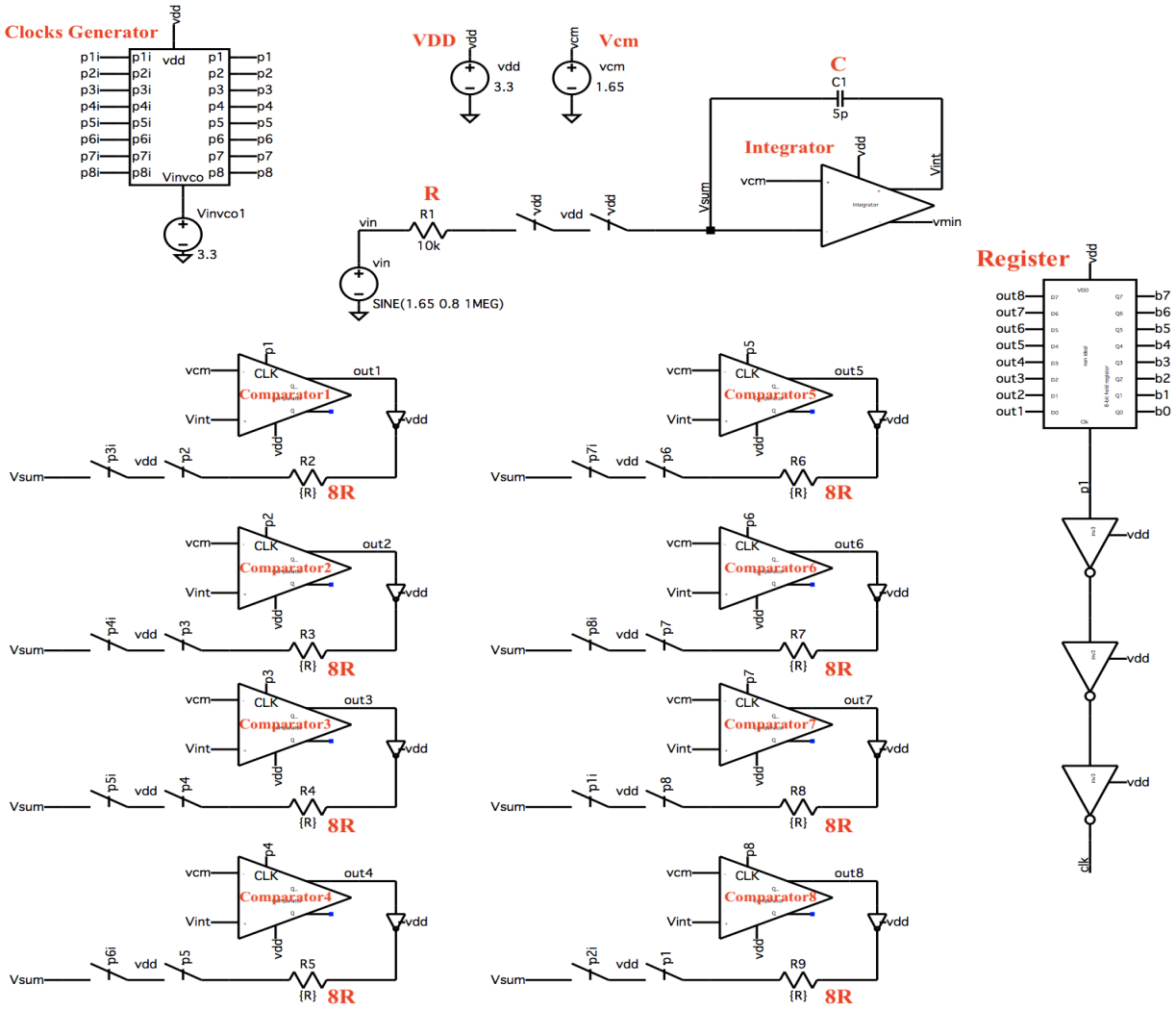

Figure 5.2 – First Order KD1S

The results of the first order DSM can be applied to the first order CT KD1S to pick the optimal RC combination. The feedforward path of the DSM and the KD1S will be identical, and the resistors in the feedback should equal $R_F = K_{path} \cdot R$ so that the loop gain stays at unity as mentioned in Section 4.4.The KD1S schematic is shown in Figure 5.2 with all components of previous chapter used, and the register stores the bits for software evaluation. The design parameters in Figure 5.2 are $VDD = 3.3\,V$, $V_{cm} = 1.65\,V$, $f_s = 122\,MHz$, $K_{paths} = 8$, and effective frequency of $f_{s,new} = 976\,MHz$. The KD1S design performance will be evaluated in the next chapter, while the remain of this section will characterize the first order KD1S by deriving important equations.

To define the input and output behavior of the system, transfer functions are needed. To derive the transfer function equations of the design a medium is necessary as KD1S design is continuous. The Laplace transform is needed for frequency domain analysis, which is relevant in the design of this modulator as the time domain does not show proper noise shaping behavior. The Laplace transform has an s-domain consisting of real and imaginary values and was used to for modeling the block diagrams of the DSMs in Equations 2.9- 2.11. Most of the continuous time DSM designs are based on discrete time models and are mapped later to continuous time using different transformations like impulse invariant transformation or bilinear z transform. This is because discrete time is easier to model in software and analyze in comparison to continuous time. Therefore, equations derived for the KD1S design will be based on the discrete time models, and later converted to frequency domain. Based on [1], as oversampling has fixed sampling frequencies at DC on the unit circuit, Taylor series can be used to bridge between the z and s domain as long as the input frequency is much less than the sampling frequency. An example in [1] was given for a discrete time switched capacitor circuit input of f = 0 Hz (DC) and z = 1 both have an output of

magnitude 1 as long as the condition holds. This practical way to transition when oversampling is given by the relationship:

$$z = e^{j2\pi f/f_s} \approx 1 + j2\pi\frac{f}{f_s} = 1 + \frac{s}{f_s} \quad \text{for } f \ll f_s \tag{5.2}$$

As oversampling is the foundation of KD1S the input frequency is always a magnitude less than the sampling frequency and the above derivation is valid.

Chapter 2 presented the block diagram model for feedback modulators in Figure 2.13 using s-domain, the same model in z-domain can be used to relate the output to the input as:

$$V_{out}(z) = \overbrace{\frac{A(z)}{1+A(z)}}^{STF(z)} \cdot v_{in}(z) + \overbrace{\frac{1}{1+A(z)}}^{NTF(z)} \cdot V_{Qe}(z) \tag{5.3}$$

Figure 5.3 presents the block diagram in the discrete model, the integrator used is a delaying digital integrator [2].

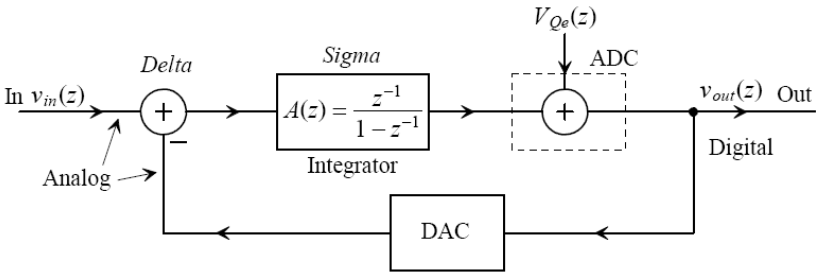

Figure 5.3 – Discrete time block diagram of first order DSM [2]

Using the A(z) formula in Equation 5.3, the output can be written as

$$v_{out}(z) = \left(v_{in}(z) - v_{out}(z)\right)\frac{z^{-1}}{1-z^{-1}} + V_{Qe}(z)$$

$$v_{out}(z) = \frac{z^{-1}}{1-z^{-1}} \cdot v_{in}(z) - \frac{z^{-1}}{1-z^{-1}} \cdot v_{out}(z) + V_{Qe}(z)$$

$$v_{out}(z) + \frac{z^{-1}}{1-z^{-1}} \cdot v_{out}(z) = \frac{z^{-1}}{1-z^{-1}} \cdot v_{in}(z) + V_{Qe}(z)$$

$$v_{out}(z)\left(\frac{1}{1-z^{-1}}\right) = \frac{z^{-1}}{1-z^{-1}} \cdot v_{in}(z) + V_{Qe}(z)$$

$$v_{out}(z) = z^{-1} \cdot v_{in}(z) + (1-z^{-1}) \cdot V_{Qe}(z) \tag{5.4}$$

Equation 5.4 shows that the input in a DSM experiences a delay, while the quantization noise is differentiated. Using the equation derived, a magnitude response for the system can be shown. The STF is the input signal delayed, while the NTF bode plot can be seen in Figure 5.4.

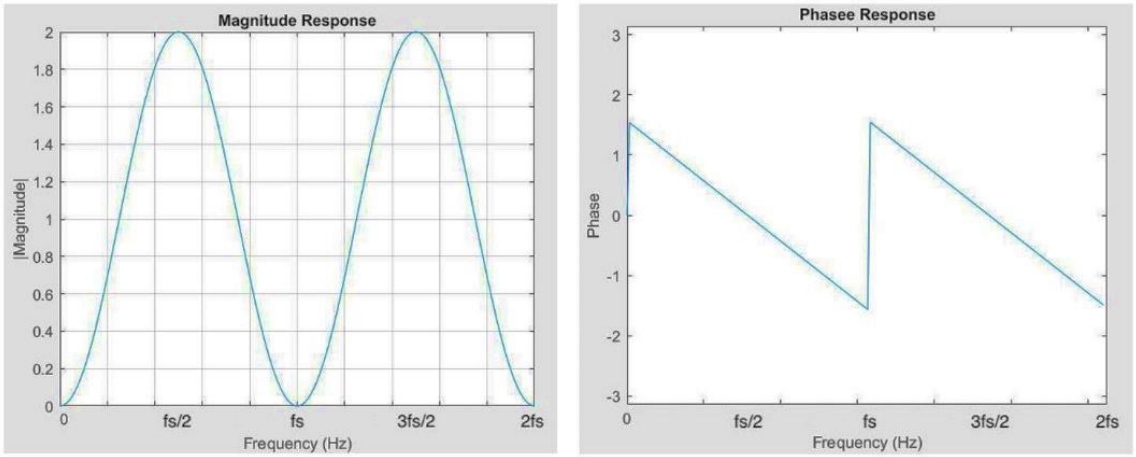

Figure 5.4 – The magnitude and phase response of Equation 5.4

The magnitude goes up to 2 and decreases to zero at $\{0, f_s, 2f_s, ..\}$ frequencies, while the phase response ranges between $\left\{-\frac{\pi}{2}, \frac{\pi}{2}\right\}$ and the switching occurs at the same frequencies that the magnitude equals zero. The digital differentiator will push the quantization noise to higher frequencies as the magnitude response behaves like a high pass filter leaving the baseband spectrum with reduced noise [2].

The z-domain plot of the NTF shows there is one pole at zero and one zero on the unity circle in Figure 5.5, thus the magnitude response is seen to go to zero at frequencies of $\{0, f_s, 2f_s, ..\}$. Stability in the z-domain requires poles to be inside the unit circle otherwise instability can occur, so the pole placement in the system is favorable.

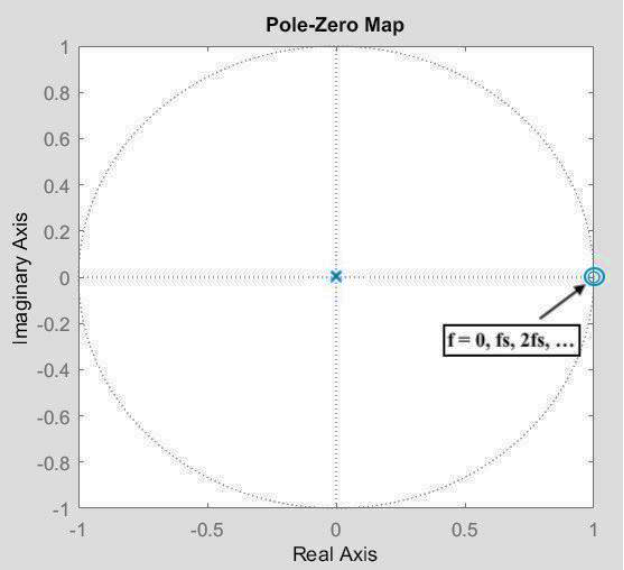

Figure 5.5 – Pole-Zero plot of Equation 5.4

The modulation noise can be derived using Equation 5.4 and 5.2, while the input quantization noise was derived in Equation 2.3 from Chapter 2.

$$NTF(z) \cdot V_{Qe}(z) = (1 - z^{-1}) \cdot V_{Qe}(z)$$

$$NTF(f) \cdot V_{Qe}(f) = \left(1 - e^{-j2\pi\frac{f}{f_s}}\right) \cdot \frac{V_{LSB}}{\sqrt{12 f_s}}$$

$$\text{where } V_{LSB} = \frac{V_{REF+} - V_{REF-}}{2^N} \tag{5.5}$$

In Equation 5.5, V_{LSB} is defined and N corresponds to the resolution of the modulator, which is 1 bit in the used DSM. Further, the RMS quantization noise can be derived using the power spectral density (PSD) of modulation noise. The modulation noise spectral density was shown in Figure 2.9, the plot shows noise power in $\frac{V^2}{Hz}$ for different frequencies. The plot equation is derived by taking the magnitude squared of Equation 5.5 as the following:

$$|NTF(f)|^2 \cdot |V_{Qe(f)}|^2 = \frac{V_{LSB}^2}{12 f_s} \cdot \left|\left(1 - e^{-j2\pi\frac{f}{f_s}}\right)\right|^2$$

$$|NTF(f)|^2 \cdot |V_{Qe(f)}|^2 = \frac{V_{LSB}^2}{12f_s} \cdot \left|(1 - (cos(2\pi\frac{f}{f_s}) - jsin(2\pi\frac{f}{f_s}))\right|^2$$

$$|NTF(f)|^2 \cdot |V_{Qe(f)}|^2 = \frac{V_{LSB}^2}{12f_s} \cdot \left|(1 - (cos2\pi\frac{f}{f_s}) + jsin(2\pi\frac{f}{f_s}))\right|^2$$

$$|NTF(f)|^2 \cdot |V_{Qe(f)}|^2 = \frac{V_{LSB}^2}{12f_s} \cdot \left|\sqrt{(1 + cos(2\pi\frac{f}{f_s}))^2 + (sin(2\pi\frac{f}{f_s}))^2}\right|^2$$

$$|NTF(f)|^2 \cdot |V_{Qe(f)}|^2 = \frac{V_{LSB}^2}{12f_s} \cdot \left|\sqrt{1 - 2 \cdot cos\left(2\pi\frac{f}{f_s}\right) + [1]}\right|^2$$

knowing that $\cos^2\left(2\pi\frac{\mathrm{f}}{\mathrm{f_s}}\right) + \sin^2\left(2\pi\frac{\mathrm{f}}{\mathrm{f_s}}\right) = 1$

$$|NTF(f)|^2 \cdot |V_{Qe(f)}|^2 = \frac{V_{LSB}^2}{12f_s} \cdot \left|\sqrt{2\left(1 - cos\left(2\pi\frac{f}{f_s}\right)\right)}\right|^2$$

knowing that $1 - cos(x) = 2sin^2(\frac{x}{2})$

$$|NTF(f)|^2 \cdot |V_{Qe(f)}|^2 = \frac{V_{LSB}^2}{12f_s} \cdot \left|\sqrt{4 \cdot sin^2\left(\pi\frac{f}{f_s}\right)}\right|^2$$

$$|NTF(f)|^2 \cdot |V_{Qe(f)}|^2 = \frac{V_{LSB}^2}{12f_s} \cdot 4 \cdot sin^2(\pi\frac{f}{f_s}) \tag{5.6}$$

The RMS quantization noise of the modulator can be derived using the noise power spectral density in Equation 5.6. Using $V_{Qe,RMS}$, the SNR of the single path, first order DSM is obtained. The calculation of the RMS noise will be executed using an ideal filter with bandwidth as in Equation 5.7 for quantization noise in the desired spectrum.

$$B = \frac{f_s}{2 \cdot OSR} \tag{5.7}$$

The equation is derived in the following manner:

$$V_{Qe,RMS}^2 = 2\int_0^B |NTF(f)|^2 \cdot |V_{Qe(f)}|^2 \cdot df = 2\int_0^B \frac{V_{LSB}^2}{12f_s} \cdot 4 \cdot sin^2(\pi \frac{f}{f_s}) \cdot df$$

$$V_{Qe,RMS}^2 = 8 \cdot \frac{V_{LSB}^2}{12f_s} \cdot \int_0^B sin^2(\pi \frac{f}{f_s}) \cdot df \qquad \frac{V^2}{Hz} \tag{5.8}$$

An approximation of $sin(x) \approx x$ can be made for the small signal section under the filter, thus

$$V_{Qe,RMS}^2 \approx 8 \cdot \frac{V_{LSB}^2}{12f_s} \cdot \int_0^{\frac{f_s}{2 \cdot OSR}} (\pi \frac{f}{f_s})^2 \cdot df \approx \frac{8\pi^2 \cdot V_{LSB}^2}{12 \cdot f_s^3} \int_0^{\frac{f_s}{2 \cdot OSR}} f^2 \cdot df \approx \frac{\pi^2 \cdot V_{LSB}^2}{12 \cdot 3 \cdot OSR^3} \tag{5.9}$$

Knowing that SNR is the signal over the noise ratio and using Equation 3.3 and 5.5, the following can be derived:

$$SNR_{ideal} = 20 \cdot log \frac{V_p/\sqrt{2}}{V_{Qe,RMS}} \textit{ also knowing that } \quad 2V_p = V_{REF+} - V_{REF-} \rightarrow V_{LSB} = \frac{2V_p}{2^N}$$

$$SNR_{ideal} = 20 \cdot log \frac{V_p/\sqrt{2}}{\frac{2\pi \cdot V_p}{2^N\sqrt{12} \cdot \sqrt{3} \cdot OSR^{3/2}}} = 20 \cdot log \frac{2^N\sqrt{12} \cdot \sqrt{3} \cdot OSR^{3/2}}{2\sqrt{2}\pi}$$

$$SNR_{ideal} = 20 \cdot \left[log \frac{2^N\sqrt{12}}{2\sqrt{2}} + log \frac{\sqrt{3}}{\pi} + log(OSR^{3/2}) \right]$$

$$SNR_{ideal} = 6.02N + 1.76 - 5.17 + 30 \cdot log(OSR) \quad dB \tag{5.10}$$

The derived ideal SNR is mainly dependent on the OSR value as the DSM is composed of 1 bit, $N = 1$, therefore the bit increase due to OSR is $N + N_{inc}$ as the following:

$$N_{inc} = \frac{30 \cdot log(OSR) - 5.17}{6.02} \quad bits \tag{5.11}$$

Or the effective number of bits can be found as below:

$$N_{eff} = [6.02N + 1.76 - 5.17 + 30 \cdot log_{10}(OSR)] \frac{log_{10}2}{log_{10}2}$$

$$N_{eff} = 6.02N + 1.76 - 5.17 + 9.03 \cdot log_2(OSR)$$

$$N_{eff} = N - 0.566 + 1.5 \cdot log_2(OSR) \quad bits \tag{5.12}$$

This shows that every doubling in the OSR can lead to a $N_{inc} = 1.5$ bit increase in the resolution. If a non-ideal filter is used for filtering the signal, the SNR value would be lower, for example, using a sinc filter would result in an SNR that is 2.16 dB lower [2].

Similarly, the first order KD1S design equations can be derived in the same manner as the first order DSM. The details of the derivation will not be documented fully as the steps are equivalent to the previous equations. As KD1S uses *K*-paths to increase the modulator SNR, the actual sampling frequency changes to an effective sampling frequency in terms of *K*. The equation relating the input to the output for KD1S is the same as in Equation 5.4, but the z from Equation 5.2 would include the effective sampling frequency that is $f_{s,new} = f_s \cdot K_{path}$. Figure 5.4 and 5.5 would now include the new effective sampling frequency and while maintaining the same shape and output.

Using K paths changes the PSD of $V^2{}_{Qe}(f)$ as the quantization noise is stretched over a wider bandwidth because $f_s \rightarrow K_{path} \cdot fs$. Figure 2.8 shows how the noise spectrum is affected by the sampling frequency, and with the new effective frequency, the noise is spread over wider range [2]. The new PSD equation for the noise is as shown below:

$$V_{Qe}^2(f) = \frac{V_{LSB}^2}{12 \cdot K_{path} \cdot f_s} \tag{5.13}$$

Using the new quantization noise equation, the modulation noise of the KD1S can be written as:

$$NTF(f) \cdot V_{Qe}(f) = \left(1 - e^{-j2\pi \frac{f}{K_{path} \cdot f_s}}\right) \cdot \frac{V_{LSB}}{\sqrt{12 \cdot K_{path} \cdot f_s}} \tag{5.14}$$

The same process from before is repeated, taking the magnitude of the modulation noise and limiting the spectrum with a Brick wall filter. The desired bandwidth is now equal to:

$$B = \frac{f_{s,new}}{2 \cdot OSR_{new}} \tag{5.15}$$

The OSR in the equation is for a *K* path wide output and it is at the new effective frequency such that $OSR_{new} = K_{path} \cdot OSR$, where *K* is averaging ratio implying to the number of output points averaged together. This is done to compare SNR in the same bandwidth.

The modulation noise can be simplified as the following:

$$|NTF(f)|^2 \cdot |V_{Qe(f)}|^2 = \frac{V_{LSB}^2}{12 \cdot K_{path} \cdot f_s} \cdot \left| \left(1 - e^{-j2\pi \frac{f}{K_{path} \cdot f_s}}\right) \right|^2$$

$$|NTF(f)|^2 \cdot |V_{Qe(f)}|^2 = \frac{V_{LSB}^2}{12 \cdot K_{path} \cdot f_s} \cdot \left| \sqrt{2\left(1 - cos\left(2\pi \frac{f}{K_{path} \cdot f_s}\right)\right)} \right|^2$$

$$|NTF(f)|^2 \cdot |V_{Qe(f)}|^2 = \frac{V_{LSB}^2}{12 \cdot K_{path} \cdot f_s} \cdot 4 \cdot sin^2(\pi \frac{f}{K_{path} \cdot f_s}) \tag{5.16}$$

Thus, the RMS quantization noise is equal to:

$$V_{Qe,RMS}^2 \approx 8 \cdot \frac{V_{LSB}^2}{12 \cdot K_{path} \cdot f_s} \cdot \int_0^{\frac{f_s \cdot K_{path}}{2 \cdot K_{path} \cdot OSR}} (\pi \frac{f}{K_{path} \cdot f_s})^2 \cdot df$$

$$V_{Qe,RMS}^2 \approx \frac{8\pi^2 \cdot V_{LSB}^2}{12 \cdot f_s^3 K_{path}^3} \int_0^{\frac{f_s}{2 \cdot OSR}} f^2 \cdot df \approx \frac{\pi^2 \cdot V_{LSB}^2}{12 \cdot 3 \cdot OSR^3 \cdot K_{path}^3}, \quad \frac{V^2}{Hz} \tag{5.17}$$

Again, SNR is equation is determined using the new RMS quantization noise as shown below:

$$SNR_{ideal} = 20 \cdot log \frac{V_p/\sqrt{2}}{\frac{2\pi \cdot V_p}{2^N \sqrt{12} \cdot \sqrt{3} \cdot K_{path}^{3/2} OSR^{3/2}}}$$

$$SNR_{ideal} = 20 \cdot log \frac{2^N \sqrt{12} \cdot \sqrt{3} \cdot K_{path}^{3/2} OSR^{3/2}}{2\sqrt{2}\pi}$$

$$SNR_{ideal} = 20 \cdot \left[log \frac{2^N \sqrt{12}}{2\sqrt{2}} + log \frac{\sqrt{3}}{\pi} + log \left(K_{path}^{3/2} OSR^{3/2} \right) \right]$$

$$SNR_{ideal} = 6.02N + 1.76 - 5.17 + 30 \cdot log(K_{path} \cdot OSR), \quad dB \tag{5.18}$$

Using SNR, ENOB as well as the N_{inc} can be estimated as in Equation 5.22:

$$N_{eff} = N - 0.566 + 1.5 \cdot log_2(K_{path} \cdot OSR) \quad bits$$

$$N_{inc} = \frac{30 \cdot log(K_{path} \cdot OSR) - 5.17}{6.02} \quad bits \tag{5.19}$$

The ENOB and *N* increase equations show that for every doubling in the *OSR*, the KD1S topology resolution increases by 1.5 bits. The increase is as in the DSM, but the main difference is that the modulator now has a higher effective frequency.

KD1S design characterizations demonstrates the advantages KD1S has on the normal delta-sigma modulator. The noise in the design is reduced and shaped due to oversampling and *K*-path utilization. The first order KD1S can be applied for cases where low power is desired but high resolution and speed are also needed, the design uses only one integrator and can achieve 8 bits of resolution with 8 paths.

5.2 SECOND ORDER CT KD1S

First order KD1S design is appropriate for high speed, high resolution, and moderate power use, on the other hand, second order KD1S can achieve higher resolution with a small increase in power as a tradeoff. As mentioned in Section 2.4.2, second order delta sigma provides better noise shaping than the first order DSM because of the two integrators used in the design. The two integrators offer a second order noise shaping that pushes the noise further to higher frequencies and leaves less noise present in the baseband spectrum.

Moreover, the second order modulator offers better randomization of the feedback signal which contributes to lowering the non-linearities present in the design such as dead zones. These benefits come at the expense of the second order DSM being more prone to instability. The

additional delay through the two integrators and comparators can increase the chances of instability in the system. Integrator saturation can also be a concern, therefore choosing correct *RC* values is a challenge. These are the reasons higher order delta-sigma modulators are usually limited to second or third order since stability is a critical issue as the order of the modulator increases. The second order KD1S design will be presented in the same manner as in Section 5.1. Second order delta-sigma modulator with mathematical characterization will be detailed, and then second order KD1S design characterizations will follow.

Selecting RC combinations for the KD1S needs to take into consideration thermal noise, increasing the capacitor value, leads to less thermal noise but can increase the settling time and consume more power [2]. The equation relating C value to noise is as follows:

$$V_{onoise,RMS} = \sqrt{{kT}/{C}}$$

$$\text{where } \; k = 13.8 \times 10^{-24} (J/\,^{\circ}K), \;\; T = \; temperature\ in\ Kelvins \tag{5.20}$$

The first order KD1S capacitor value was 5 pF which results in approximately $64\ \mu V$ RMS thermal noise at $300\ ^{\circ}K$. The noise was sufficiently low enough to not affect circuit operation as the output behavior was operating in the correct manner. In the second order KD1S, the stability concern leads to the capacitor value selection being more critical, as while excess noise is not desirable but an increase in settling time can increase the delay in the loop [2]. The second order KD1S with a single path is shown in Figure 5.6 below:

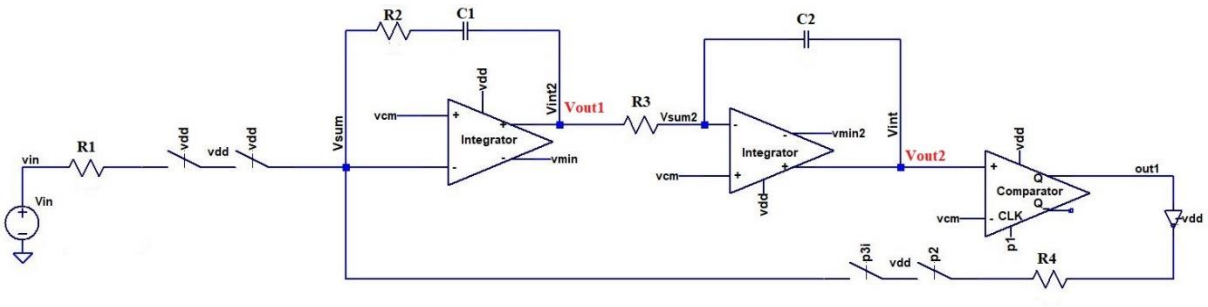

Figure 5.6 – Single path second order DSM

Shown in Figure 5.6 are two integrators with *R* and *C*, and one comparator for the single path. The additional resistor *R2* was added in the first integrator feedback so that a zero in s-domain is added to the system to help dampen possible oscillations that can happen due to stability. Using s-domain, the second order integration process in Figure 5.6 will be shown in two ways, with and without the added resistor to show the effects. The equations are as shown below:

$$\frac{v_{in}}{R_1} = C\frac{dv_{out1}}{dt} = sC_1v_{out1} \quad \rightarrow \quad v_{out1} = v_{in} \cdot \frac{1}{sC_1R_1}$$

$$v_{out2} = v_{out1} \cdot \frac{1}{sC_2R_3} = v_{in}\frac{1}{s^2R_1R_3C_1C_2}$$

$$\frac{v_{out2}}{v_{in}} = \frac{1}{s^2R_1R_3C_1C_2} \tag{5.21}$$

Equation 5.21 presents the system's transfer function, and the system contains no zeros and one pole at origin on the imaginary axis. In s-domain, the stability requirements are to have poles on the left half of the plane to maintain stability, left plane poles cause instability, and pole on the imaginary axis present marginal stability. The marginal stability is a concern as the second order system is already more prone to instability, thus the additional resistor was included to introduce a zero in the system. Having a zero in the system aids in dampening the system

response to help in preventing instability. The transfer function of the system including resistor *R2* is as the following:

$$\frac{v_{in}}{R_1} = \frac{v_{out1}}{{}^{1}/_{sC_1} + R_2} \quad \rightarrow \quad v_{out1}R_1 = v_{in} \cdot \left(\frac{1}{sC_1} + R_2\right) = v_{in} \cdot \left(\frac{1 + sC_1R_2}{sC_1}\right)$$

$$v_{out1} = v_{in} \cdot \left(\frac{1 + sC_1R_2}{sR_1C_1}\right)$$

$$\frac{v_{out1}}{R_3} = \frac{v_{out2}}{{}^{1}/_{sC_2}} \quad \rightarrow \quad v_{out2} = v_{in} \cdot \left(\frac{1 + sC_1R_2}{s^2R_1R_3C_1C_2}\right) \tag{5.22}$$

Equation 5.22 shows that the system pole is the same at 0, and an extra zero at $s = {}^{-1}/_{R_2C_1}$ on the left side of the plane. Continuous time delta sigma modulators maintain a constant pole position, which is an advantage over DT DSM whose poles change position.

The same process for selecting *RC* combinations was completed as in Figure 5.1, and the final RC combinations that gave a satisfactory output are summarized in this Table 5.1.

Resistor Value	**Capacitor Value / Noise**
Resistor Values for Figure 5.6	$R_1 = 15\ k\Omega$
	$R_2 = 1\ k\Omega$
	$R_3 = 3\ k\Omega$
Capacitor Values for Figure 5.6, and Nosie	$C_1 = 20\ pF, V_{onoise,RMS\approx 20\ \mu V}$
	$C_2 = 3\ pF, V_{onoise,RMS\approx 64\ \mu V}$

Table 5.1 – Second order RC values

To achieve the desired *RC* combination effect, the large *RC* values were mainly placed on the first integrator so that the thermal noise and non-linearities that could be a result of settling time restrictions can be filtered by the second integrator.

Further, the second order DSM equations will be derived based on the discrete model of Figure 2.14, the figure shows a delaying integrator and a non-delaying integrator used in the block diagram. The input and output can be related as follows:

$$v_{out}(z) = [(v_{in}(z) - v_{out}(z)) \cdot \frac{1}{1 - z^{-1}} - v_{out}(z)] \cdot \frac{z^{-1}}{1 - z^{-1}} + V_{Qe(z)}$$

$$v_{out}(z) = \frac{z^{-1}}{(1 - z^{-1})^2} \cdot v_{in}(z) - \frac{z^{-1}}{(1 - z^{-1})^2} \cdot v_{out}(z) - \frac{z^{-1}}{1 - z^{-1}} \cdot v_{out}(z) + V_{Qe(z)}$$

$$v_{out}(z) = \frac{z^{-1}}{(1 - z^{-1})^2} \cdot v_{vin}(z) - \frac{z^{-1} + z^{-1}(1 - z^{-1})}{(1 - z^{-1})^2} \cdot v_{out}(z) + V_{Qe(z)}$$

$$v_{out}(z) \cdot [\frac{1}{(1 - z^{-1})^2}] = \frac{z^{-1}}{(1 - z^{-1})^2} \cdot v_{vin}(z) + V_{Qe(z)}$$

$$v_{out}(z) = z^{-1} \cdot v_{in}(z) + (1 - z^{-1})^2 \cdot V_{Qe}(z) \quad (5.23)$$

The above equation proves how the noise in the second order KD1S experiences second order filtering so that the desired spectrum noise is further pushed out to higher frequencies. On the other hand, the input signal simply goes through a delay unchanged.

The magnitude and phase response were analyzed in the same manner for the second order as in Figure 5.4, and the results are shown below:

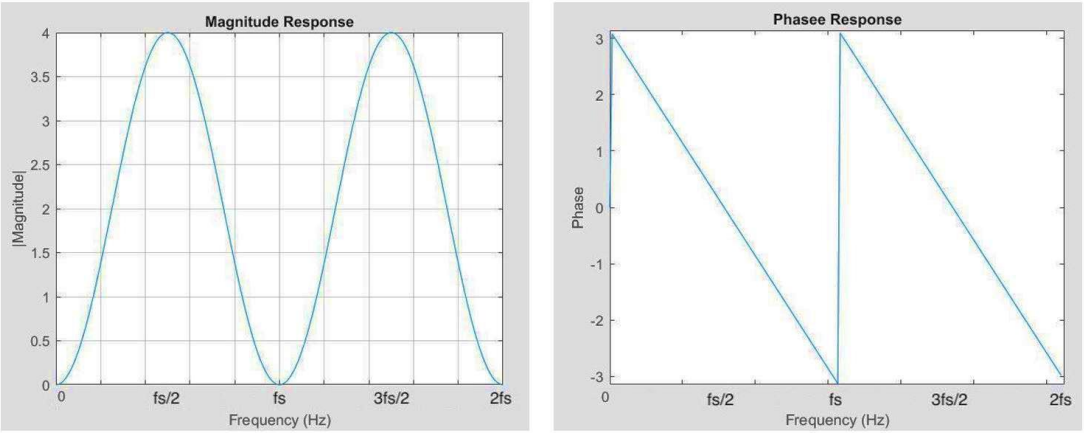

Figure 5.7 – Magnitude and phase response of second order DSM

As expected, the magnitude response goes to zero at the same frequencies as in the first order, the only difference is that the signal response goes to a higher magnitude value, twice the magnitude of the first order design, of 4. This increase is like Figure 2.16 where the second order magnitude response is higher at higher frequencies and lower at near the baseband.

The pole-zero plot is also evaluated in Figure 5.8, the plot shows two zeros at the unity circle and two poles at unity. The stability issue was addressed in the design as mentioned previously by adding an extra resistor in the feedback of the first integrator. The magnitude and phase plots in both first and second order repeat as KD1S modulators are a sampling system.

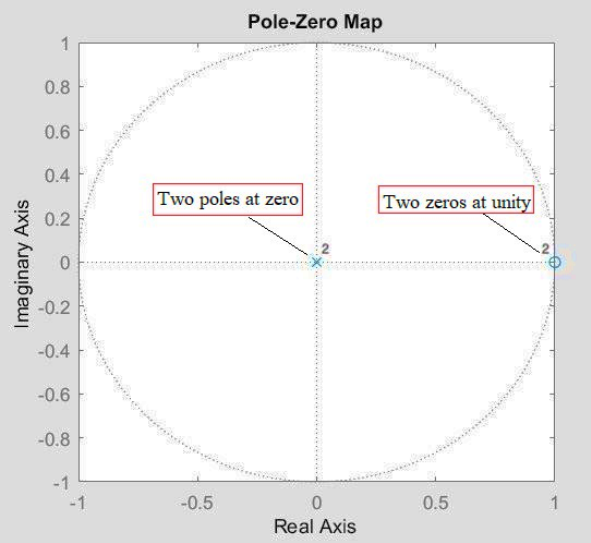

Figure 5.8 – Pole-Zero plot of Equation 5.23

Likewise, the SNR for second order DSM can be expressed using RMS quantization noise. To express the $V_{Qe,RMS}$, the quantization noise is shaped and filtered by multiplying with the NTF. The magnitude of the modulation noise is simplified in the manner shown below:

$$|NTF(f)|^2 \cdot |V_{Qe(f)}|^2 = \frac{V_{LSB}^2}{12 f_s} \cdot \left| \left(1 - e^{-j2\pi \frac{f}{f_s}}\right)^2 \right|^2$$

$$|NTF(f)|^2 \cdot |V_{Qe(f)}|^2 = \frac{V_{LSB}^2}{12f_s} \cdot \left| \left(1 - \left(cos2\pi\frac{f}{f_s}\right) + jsin\left(2\pi\frac{f}{f_s}\right)\right)^2 \right|^2$$

$$|NTF(f)|^2 \cdot |V_{Qe(f)}|^2 = \frac{V_{LSB}^2}{12f_s} \cdot \left| \sqrt{(1 + cos(2\pi\frac{f}{f_s}))^2 + (sin(2\pi\frac{f}{f_s}))^2}^2 \right|^2$$

$$|NTF(f)|^2 \cdot |V_{Qe(f)}|^2 = \frac{V_{LSB}^2}{12f_s} \cdot \left| 2\left(1 - cos\left(2\pi\frac{f}{f_s}\right)\right) \right|^2$$

$$|NTF(f)|^2 \cdot |V_{Qe(f)}|^2 = \frac{V_{LSB}^2}{12f_s} \cdot \left| 4 \cdot sin^2\left(\pi\frac{f}{f_s}\right) \right|^2$$

$$|NTF(f)|^2 \cdot |V_{Qe(f)}|^2 = \frac{V_{LSB}^2}{12f_s} \cdot 16 \cdot sin^4(\pi\frac{f}{f_s}) \tag{5.24}$$

Next, the modulation noise is filtered to the same bandwidth as in the first order modulator for fair comparison, the following equation can be concluded (multiplying by 2, the equation considers double sided spectrum):

$$V_{Qe,RMS}^2 = 2\int_0^B |NTF(f)|^2 \cdot |V_{Qe(f)}|^2 \cdot df = 2\int_0^B \frac{V_{LSB}^2}{12f_s} \cdot 16 \cdot sin^4(\pi\frac{f}{f_s}) \cdot df$$

$$V_{Qe,RMS}^2 = 32 \cdot \frac{V_{LSB}^2}{12f_s} \cdot \int_0^B sin^4(\pi\frac{f}{f_s}) \cdot df \tag{5.25}$$

Simplifying the equation even further as shown below:

$$V_{Qe,RMS}^2 \approx 32 \cdot \frac{V_{LSB}^2}{12f_s} \cdot \int_0^{\frac{f_s}{2 \cdot OSR}} (\pi\frac{f}{f_s})^4 \cdot df \approx \frac{32\pi^4 \cdot V_{LSB}^2}{12 \cdot f_s^5} \int_0^{\frac{f_s}{2 \cdot OSR}} (f)^4 \cdot df$$

$$V_{Qe,RMS}^2 \approx \frac{\pi^4 \cdot V_{LSB}^2}{12 \cdot 5 \cdot OSR^5}, \quad \frac{V^2}{Hz} \tag{5.26}$$

In the same fashion, SNR is specified for the second order DSM using the previously derived RMS quantization noise as a ratio with the peak input signal, the equation is documented below:

$$SNR_{ideal} = 20 \cdot log \frac{V_p/\sqrt{2}}{\frac{2\pi^2 \cdot V_p}{2^N\sqrt{12} \cdot \sqrt{5} \cdot OSR^{5/2}}} = 20 \cdot log \frac{2^N\sqrt{12} \cdot \sqrt{5} \cdot OSR^{5/2}}{2\sqrt{2}\pi^2}$$

$$SNR_{ideal} = 20 \cdot \left[log \frac{2^N\sqrt{12}}{2\sqrt{2}} + log \frac{\sqrt{5}}{\pi^2} + log(OSR^{5/2}) \right]$$

$$SNR_{ideal} = 6.02N + 1.76 - 12.9 + 50 \cdot log(OSR), \quad dB \tag{5.27}$$

Utilizing the second order design SNR, the ENOB and bits increase in resolution is stemmed from SNR as follows:

$$\text{rewriting} \quad SNR_{ideal} = 6.02(N + N_{inc}) + 1.76 \quad dB$$

$$N_{inc} = \frac{50 \cdot log(OSR) - 12.9}{6.02}, \quad bits \tag{5.28}$$

$$N_{eff} = N - 1.85 + 2.5 \cdot log_2(OSR), \quad bits \tag{5.29}$$

Second order DSM equations show the benefits that this design offers over the first order counterpart. In a simple single path second order DSM, doubling the OSR would increase the bit resolution by 2.5 bits, a 15 dB increase in SNR [2].

Correspondingly, second order KD1S design equations are rooted from the single path delta sigma modulator, the equations are executed in the same manner with the new effective frequency depending on the *K* paths used in the design. The second order CT KD1S circuit is extended from Figure 5.6 by adding 7 extra paths containing comparators. The design has the same *RC* value combinations, same clocking logic as the first order; only the feedforward path is different than the first order design. The negative feedback is maintained in the loop by using the positive comparator output followed by the DAC/inverter, and by using the inverting terminal of the two integrators in the feedforward path as seen in Figure 5.7.

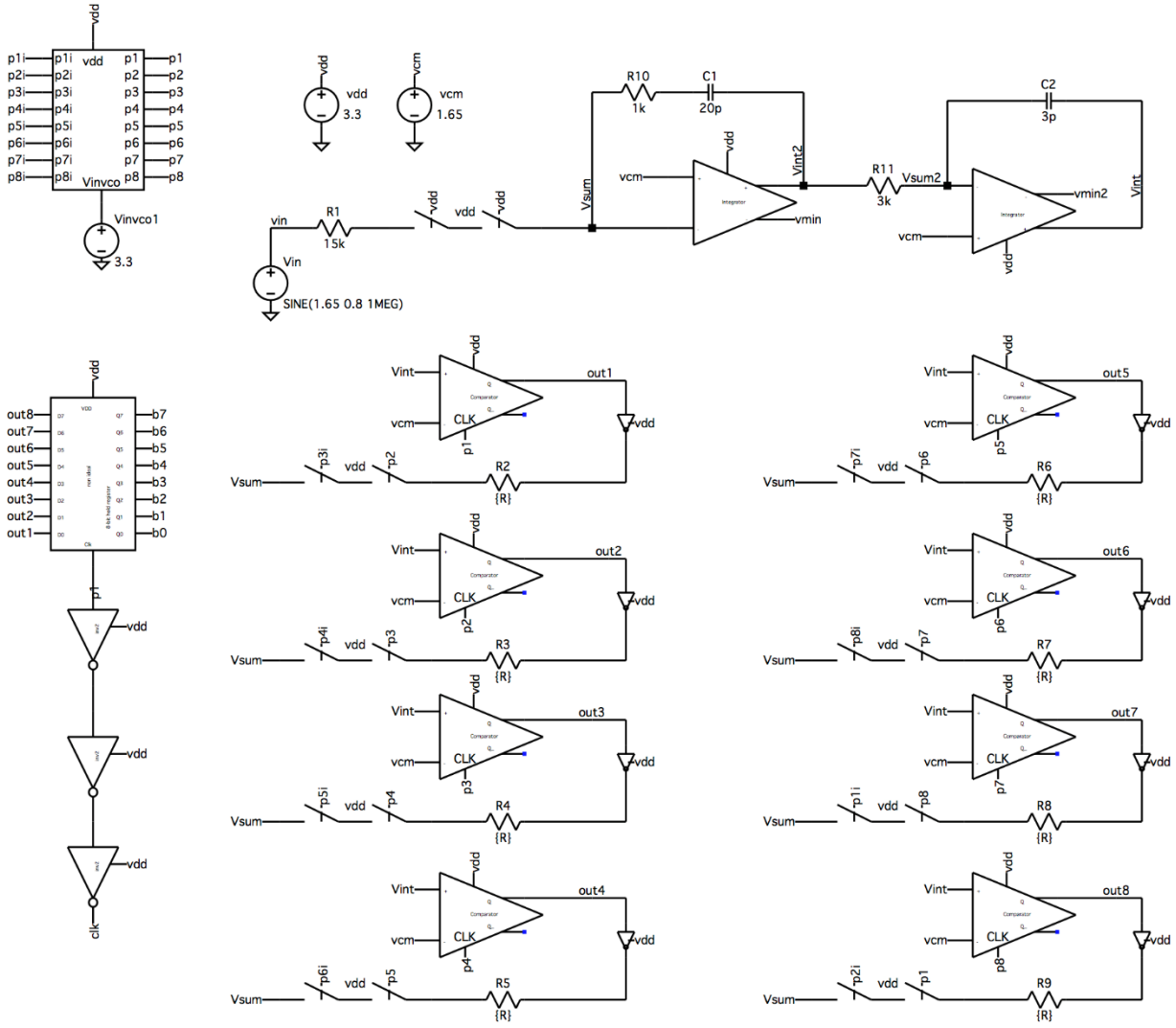

Figure 5.9 - Second order KD1S schematic

The equations characterizing the second order KD1S will be based on the second order DSM but with a new effective frequency $K_{path} \cdot f_s$. The quantization noise will equal Equation 5.13 as the *K* paths used hold the same effect on the quantization noise spectrum. The NTF product with the quantization noise to derive modulation noise is as the following:

$$NTF(f) \cdot V_{Qe}(f) = \left(1 - e^{-j2\pi \frac{f}{K_{path} \cdot f_s}}\right)^2 \cdot \frac{V_{LSB}}{\sqrt{12 \cdot K_{path} \cdot f_s}} \tag{5.30}$$

Equation 5.30 will be utilized to calculate the RMS quantization noise in the spectrum to calculate SNR. The modulation noise magnitude is executed first, and then filtering.

$$|NTF(f)|^2 \cdot |V_{Qe(f)}|^2 = \frac{V_{LSB}^2}{12 \cdot K_{path} \cdot f_s} \cdot \left| \left(1 - e^{-j2\pi \frac{f}{K_{path} \cdot f_s}}\right)^2 \right|^2$$

$$|NTF(f)|^2 \cdot |V_{Qe(f)}|^2 = \frac{V_{LSB}^2}{12 \cdot K_{path} \cdot f_s} \cdot \left| 2\left(1 - cos\left(2\pi \frac{f}{K_{path} \cdot f_s}\right)\right) \right|^2$$

$$|NTF(f)|^2 \cdot |V_{Qe(f)}|^2 = \frac{V_{LSB}^2}{12 \cdot K_{path} \cdot f_s} \cdot 16 \cdot sin^4(\pi \frac{f}{K_{path} \cdot f_s}) \tag{5.31}$$

Applying the same filter used on all the modulators to derive RMS quantization noise, the following result is reached:

$$V_{Qe,RMS}^2 \approx \frac{V_{LSB}^2}{12 \cdot K_{path} \cdot f_s} \cdot 2 \cdot \int_0^{\frac{f_s \cdot K_{path}}{2 \cdot K_{path} \cdot OSR}} 16 \cdot sin^4(\pi \frac{f}{K_{path} \cdot f_s}) \cdot df$$

$$V_{Qe,RMS}^2 \approx 32 \cdot \frac{V_{LSB}^2}{12 \cdot K_{path} \cdot f_s} \cdot \int_0^{\frac{f_s \cdot K_{path}}{2 \cdot K_{path} \cdot OSR}} (\pi \frac{f}{K_{path} \cdot f_s})^4 \cdot df$$

$$V_{Qe,RMS}^2 \approx \frac{32\pi^4 \cdot V_{LSB}^2}{12 \cdot f_s^5 K_{path}^5} \int_0^{\frac{f_s}{2 \cdot OSR}} f^4 \cdot df \approx \frac{\pi^4 \cdot V_{LSB}^2}{12 \cdot 5 \cdot OSR^5 \cdot K_{path}^5}, \qquad \frac{V^2}{Hz} \tag{5.32}$$

The SNR equation can be revised for the second order KD1S using Equation 5.32

$$SNR_{ideal} = 20 \cdot log \frac{V_p/\sqrt{2}}{\frac{2\pi^2 \cdot V_p}{2^N \sqrt{12} \cdot \sqrt{5} \cdot K_{path}^{5/2} OSR^{5/2}}}$$

$$SNR_{ideal} = 20 \cdot log \frac{2^N \sqrt{12} \cdot \sqrt{5} \cdot K_{path}^{5/2} OSR^{5/2}}{2\sqrt{2}\pi^2}$$

$$SNR_{ideal} = 20 \cdot \left[log \frac{2^N \sqrt{12}}{2\sqrt{2}} + log \frac{\sqrt{5}}{\pi^2} + log \left(K_{path}^{5/2} OSR^{5/2} \right) \right]$$

$$SNR_{ideal} = 6.02N + 1.76 - 12.9 + 50 \cdot log(K_{path} \cdot OSR), \quad dB \tag{5.33}$$

Bit increase, and resolution can be simplified from Equation 5.33

$$N_{eff} = N - 1.85 + 2.5 \cdot log_2(K_{path} \cdot OSR) \quad bits$$

$$N_{inc} = \frac{50 \cdot log(K_{path} \cdot OSR) - 12.9}{6.02}, \quad bits \tag{5.34}$$

The second order KD1S overpowers the first order design as the effective SNR increase is 15 (dB) at the new sampling frequency. The following equations will be used in the next chapter for comparing simulation's SNR value to the ideal case SNR value.

5.3 COMPARING SAMPLING IN MODULATORS

The benefits of KD1S topology are more apparent when compared to normal DSM and simple oversampling without noise shaping. The following plot shown in Figure 5.10 presents different OSR values with the corresponding resolution improvement. This plot was created using the N_{inc} equations for each delta sigma modulator type. As seen in Figure 5.10, simple oversampling does not achieve high resolution since the noise is not being pushed to higher frequencies. Having a second order DSM can achieve high resolution even without utilizing *K* paths as seen when *OSR*=10,000, the second order DSM achieves an increase of 31 bits while first order KD1S resolution increase was 23 bits. The second order KD1S resolution increase is higher at every OSR than any of the other modulators, which is why this topology was appealing for high resolution, and high-speed aspects.

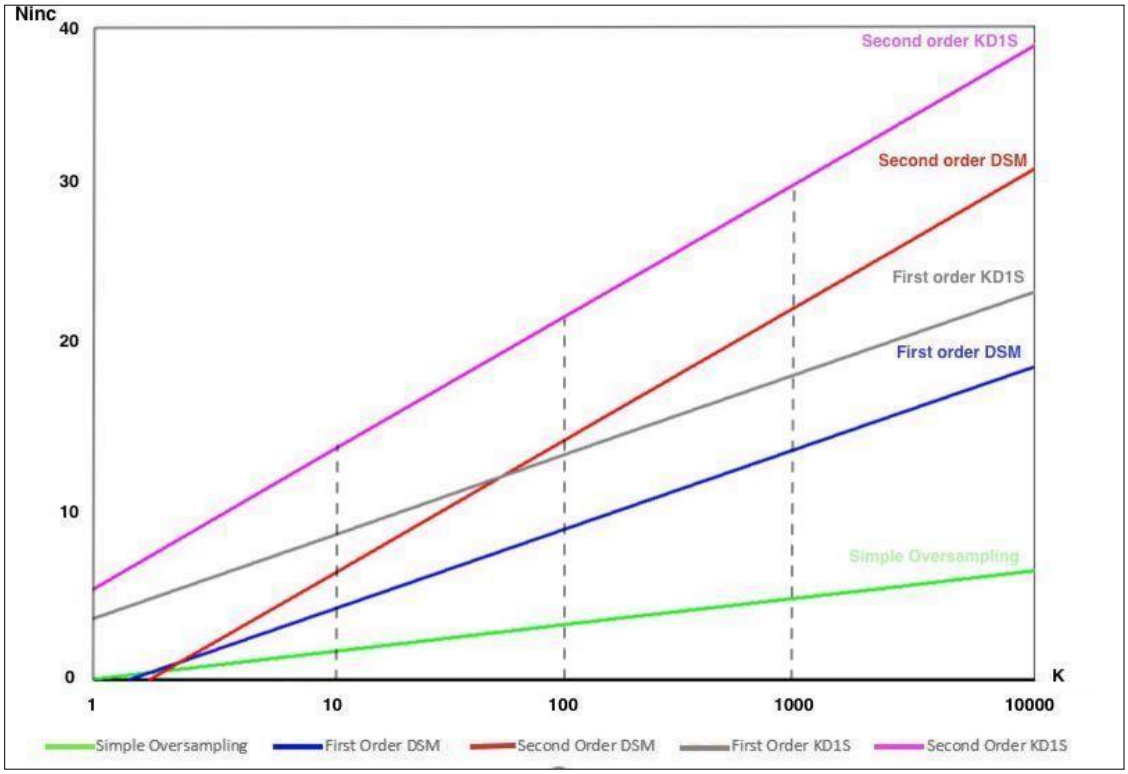

Figure 5.10 – Comparison between different modulators bit increase vs. OSR

CHAPTER 6: DESIGN SIMULATION AND COMPARISON

Previous chapters presented the theory and concept of KD1S design to prove the effectiveness of the modulator. This chapter will present simulations for the KD1S design to compare performance of the first and second order modulators in the two process design kits (PDK) AMS and C5. The performance in general will be referenced for effectiveness based on the requirements presented in Chapters 3 and 5.

6.1 AMS AND C5 KD1S SIMULATIONS

The current CMOS technology facilitates cheap, fast, and low power designs. As technology advances, process matching is improving, which makes circuits more reliable. The ADC design takes advantage of the advancement in today's technology yielding to cheap, low power, fast, and reliable high-resolution converters [16]. The two processes used for the KD1S design are AMS and C5, AMS technology contains 4 metal layers, operates at 3.3 V, and has a minimum length of $0.35\ \mu m$. On the other hand, the C5 process design kit (PDK) consists of 3 metal layers, operates at 5 V, and has a minimum length of $0.6\ \mu m$. Layout of the design was done in the AMS process only for the second order KD1S modulator, the layout sizes and execution process will be discussed in the following sections.

The KD1S design as mentioned in previous chapters was mainly focused on only delta sigma modulation, and the digital filtering was not considered as it will be completed using MATLAB software. A MATLAB script from [2] is used to collect the simulation data from

LTspice and execute the filtering. The data was initially stored in a shift register for easier interface as digital data is easier to manipulate using digital signal processing (DSP).

The MATLAB code expects a raw file generated from LTspice that contains information about the input (*vin*), clock signal used for the shift register (*clk*), and the stored output bits (*b0-b7*). In the script itself, voltage supply (*vdd*) is entered, number of paths is supplied, and lastly the desired OSR for limiting the bandwidth is specified as well. These parameters allow the script to perform Fourier Transform (FT) for windowing the data as this process can guarantee clean edges with an integer number of cycles. Clean edges are preferred as random starting and ending point in the sinusoidal input can create abrupt edges leading to a lower SNR. The first five tones are removed from the spectrum to enable SNR calculation without distortion. To reconstruct the data for plotting, a second order sinc filter is used to clean the signal output. If further filtering is desired for the output, a higher order sinc filter can be used but attenuation will occur in the output signal. In the first and second order CT KD1S, using only a second order sinc filter is enough based on the following equation to reconstruct the signal:

$$L \cdot log_2(K) \geq \frac{30 \log_{10} K - 5.17}{6.02} \tag{6.1}$$

$$L \cdot log_2(K) \geq \frac{50 \log_{10} K - 12.9}{6.02} \tag{6.2}$$

The left side of Equations 6.1 and 6.2, present the bit increase in output word due to the filter. The variable *K* represents the number of points averaged in the filter, and *L* is the filter order. The bit increase from the filter is compared with the bit increase equations from Chapter 5 for first and second order design. The first order KD1S bit increase is in Equation 6.1, while second order is in Equation 6.2. If $K \leq 256$, an L of 2 would satisfy both equations. The MATLAB script analyzes *K* of 64, 128, and 256, which means using a second order sinc filter is acceptable.

After decimation was performed by the 8-bit register, averaging the signal is accomplished through MATLAB by choosing different effective oversampling ratios. In general, averaging affects a signal in a similar manner to a low pass filter, and the input-output relationship is shown as a transfer function in Equation 6.3.

$$H(z) = \frac{1 - z^{-K_{avg}}}{1 - z^{-1}} \tag{6.3}$$

Since the design consists of 8-paths, and *K* averaging is completed in MATLAB, the effective *OSR* can be specified as in Equation 6.4. For instance, averaging by 8, results in an effective *OSR* of 64.

$$OSR_{effective} = K_{path} \cdot K_{average} = 8 \cdot K_{average} \tag{6.4}$$

Using *OSR* of different value can change the bandwidth of the KD1S in software without affecting the actual hardware design, and in this way higher SNR can be achieved.

Finally, after the script runs the windowing and filtering, the command window in MATLAB would display the obtained SNR, ENOB, sampling frequency, and bandwidth of the design for serial and parallel mode. Plots are also shown at the end in frequency and time domain for the corresponding filtering mode.

Furthermore, for proper evaluation of the circuit's performance coherent sampling was utilized in order to have the signal begin and end at the same point; coherent sampling is having the ratio of f_s/f_{in} equal to a whole integer. This method of sampling minimizes the effects of spectral leakage which can occur due to abrupt edges. Abrupt edges are not desired as the phenomena can introduce non linearities into the system and cause the appearance of new false frequencies into the spectrum [2]. Also, for accurate FFT results a certain number of samples must

be captured from the input signal. In this design, the simulation process depended on the following equation from [8]:

$$\frac{f_{in}}{f_s} = \frac{M}{N} \quad \xrightarrow{yields} \quad M = N \cdot \frac{f_{in}}{f_s} \tag{6.5}$$

where f_{in} represents the input signal frequency, f_s is the sampling frequency value, *M* corresponds to the number of cycles needed to obtain the desired value of samples, and *N* is the number of samples that will be captured. The preferred number of output cycles is an odd number for preventing repeated samples to appear in the spectrum. Having repeated samples does not lead to an error, but it increases the time required for simulations. The number of samples is usually in powers of 2, commonly used values consist of 1028, 4096, 8192 and so on. In this thesis, *N*=1028 samples were used for reasonable simulation time. Knowing all the parameters in Equation 6.5, only the number of cycles is calculated for different simulation settings based on the input and sampling frequencies.

The KD1S modulator design was analyzed using different test conditions for investigating its performance. The tests will be summarized using tables, and comparison between processes will be included for both first and second order designs. In Chapter 5, the first and second order KD1S modulator schematic in the AMS process were shown in Figures 5.2 and 5.9 respectively. The same figures will be used for the AMS process simulations in the chapter. As for the C5 process simulations, the two KD1S schematics with values are shown in Appendix 1 as Figures 1 and 2.

6.1.1 LINEARITY TEST

The first simulation is the ramp input test for checking the linearity of the system, as well as for characterizing the linear input and output range of the KD1S. The simulation was executed by

having a slow rising ramp as an input signal to the modulator, the ramp input ranges from 0 V to the *VDD* of the design evaluated. The delay through the modulator is considered and added to the input ramp as a delay on the source so that the output is not shifted. The output is expected to have no dead zones, and to increase linearly with the input.

The output of the circuit was filtered to compare with the ramp input using first and second order simple *RC* filter. The roll-off frequency of the *RC* filter was picked considering the input signal frequency. To create the filter, the bits of the register were added using a resistor string to form an R_{total} value, then a normal *RC* filter was sketched.

The first order ramp test in the AMS process is shown in Figure 6.1, the output shows no dead zones as it is switching constantly around the ramp input. An offset is shown at higher input amplitudes, which could be due to the modulator limiting the signal due to overflow. The *RC* filter could also introduce a small phase shift which is why the output has a different slope than the input. The first order KD1S ramp test shows that the output's linear range is approximately within 0.5V to 2.8V. The output from the KD1S was also smoothed with a second order RC filter to show the signal with less ripples and compare better with the input. A start up transient can be seen at the beginning of the input due to the capacitor in the filter.

Figure 6.2 shows a zoomed in part of the ramp, the output does not contain non-linearities in the specified ranges mentioned earlier. The green output is the first order *RC* filter output, and the blue line is the second order *RC* filter output.

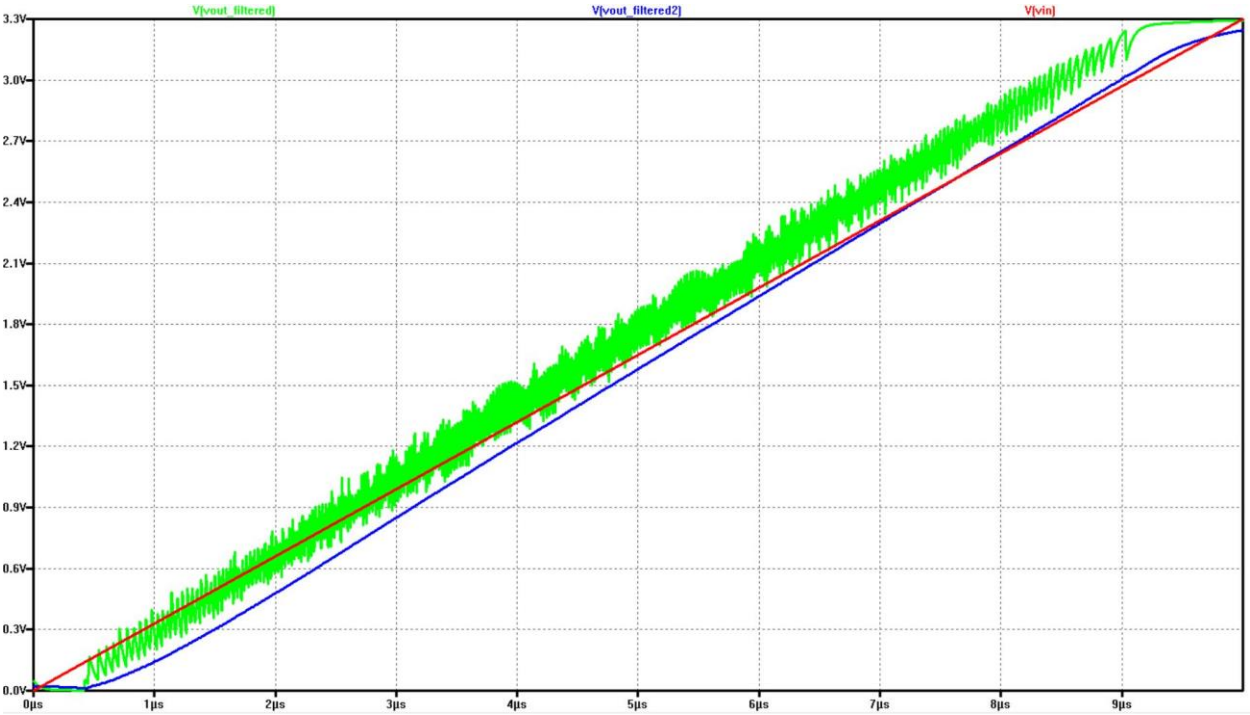

Figure 6.1 - Ramp test of first order KD1S in AMS

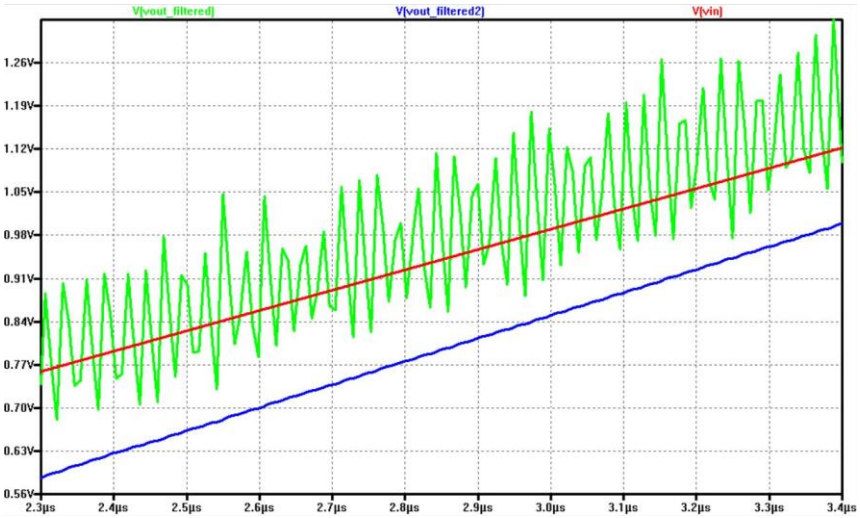

Figure 6.2 - zoom in Figure 6.1

Similarly, the ramp test with the same settings but different *VDD* was done in the C5 process displayed below in Figure 6.3.

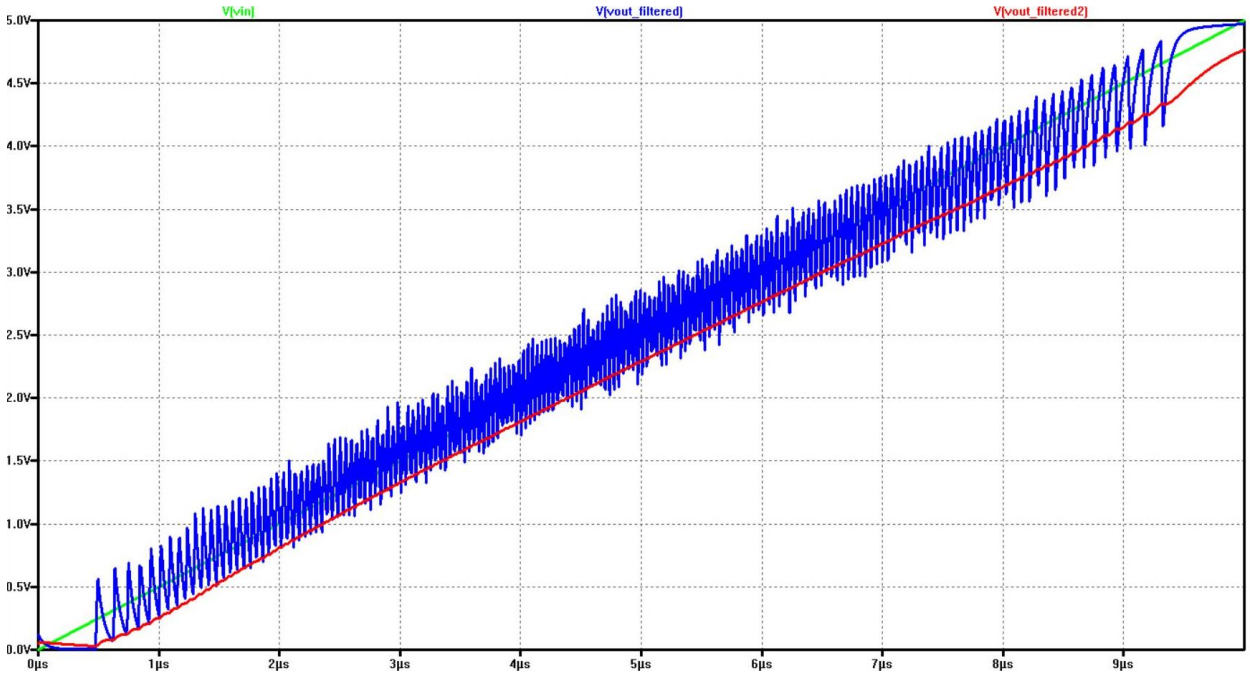

Figure 6.3 - Ramp test for first order KD1S in C5

The C5 process shows no dead zones, which reassures that there are not any non-linearities in the design. The output in Figure 6.3 shows better centering around the input signal as there is no offset at the output, with a linear range from 1.0 V to 4.0 V. Also, the second order *RC* filter in C5 version shows that the output is increasing with the input ramp but not as linearly like AMS process.

The AMS and C5 first order KD1S have the same topology but differ by process and by selected loop RC values. The capacitor values are identical in the C5 and AMS versions of the first order KD1S modulators, however the resistor values differ. Moreover, the sampling frequency in AMS with a *VDD* of 3.3 V is 122 MHz, while at a 5V *VDD* in the C5 process it is 100 MHz. This explains why the output in Figure 6.1 appears to switch faster with smaller ripples than the output seen in Figure 6.3. Moreover, the second order KD1S design ramp test is shown again in the same manner for both processes. All performed simulations had the same input settings as the 1st order

KD1S for a fair comparison, and the same filter at the output. The second order KD1S in the AMS process is shown in Figure 6.4.

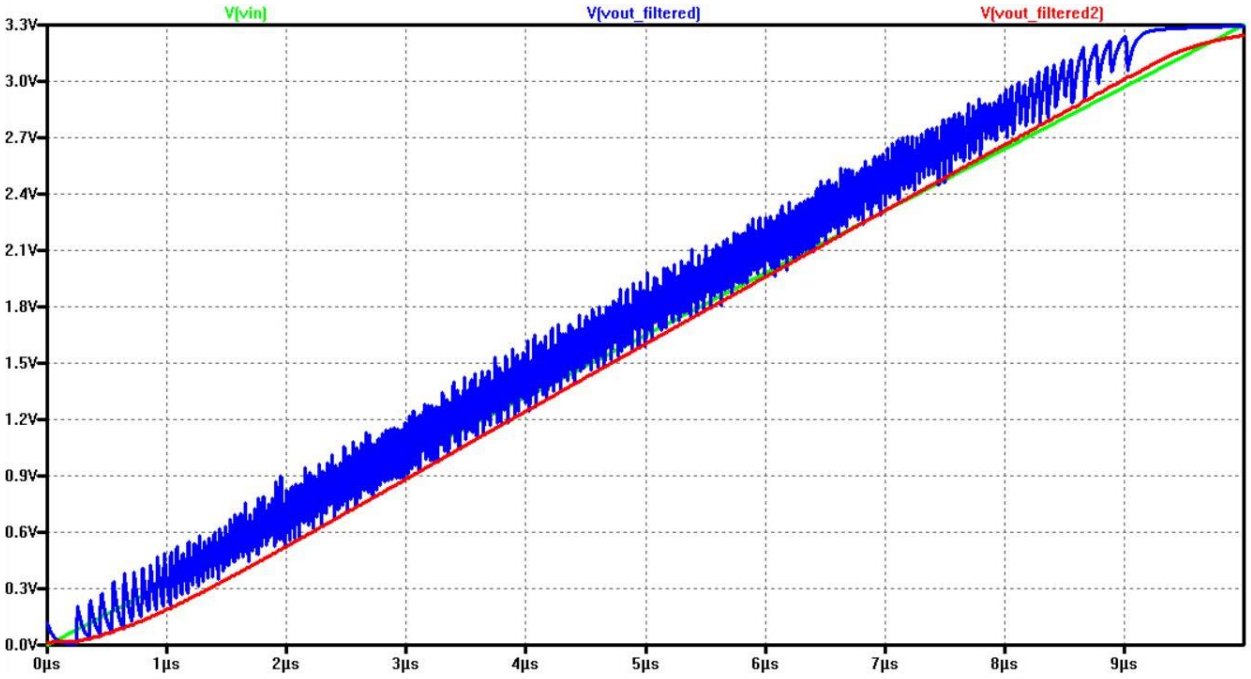

Figure 6.4 - Ramp test for second order KD1S in AMS process

The output of the test shows that the second order design is linear since there are no dead zones present. Dead zones would appear as a horizontal line in the output because the modulator is unable to switch to another level as mentioned in Chapter 2. The output is linearly increasing with the ramp input and mostly linear within the range of 0.6 V to 2.7 V. The second order design shows a more consistent output swing between switching than in the first order AMS design of Figure 6.1.

Similarly, the ramp test implemented for the second order KD1S in the C5 process is shown next:

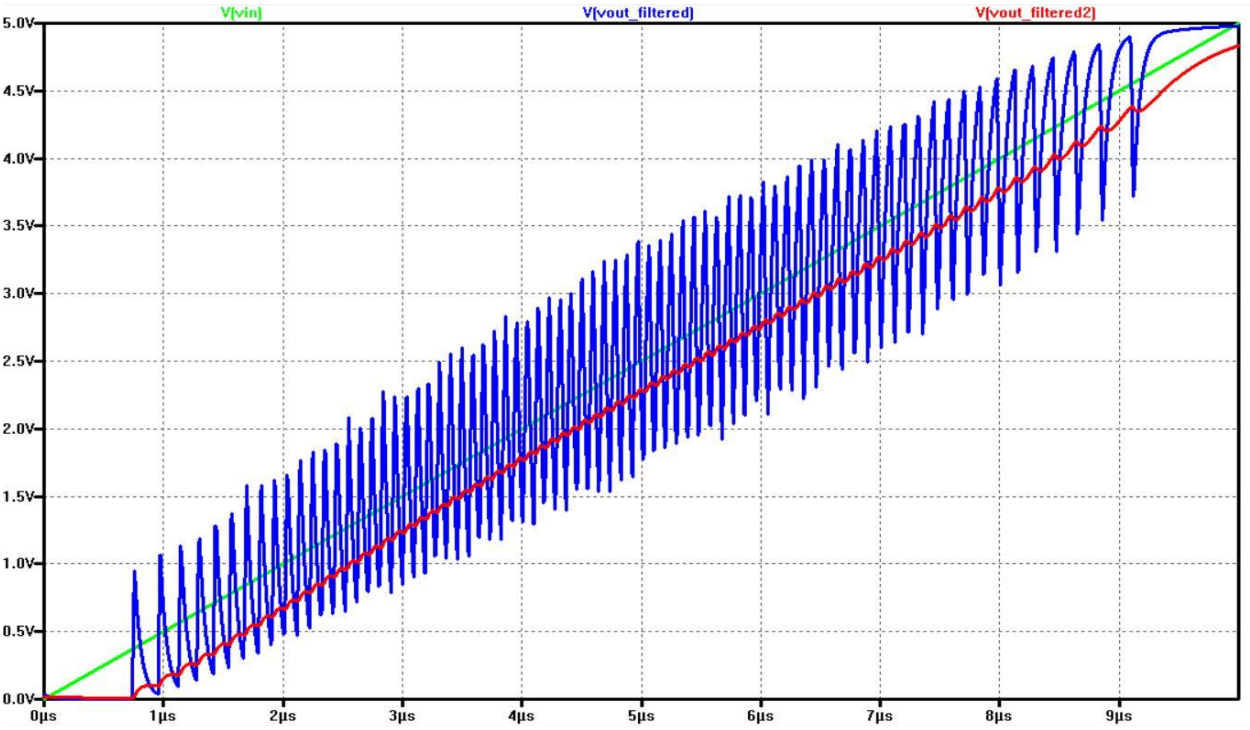

Figure 6.5 - Ramp test for second order KD1S in C5

The filtered output exhibits linearity as the system is always switching and linearly increasing around the input ramp. The linear range of the second order KD1S ranges from 1.1 V to 3.9 V. In this figure, it is more apparent how the ripple of the output in the C5 is larger than the AMS process because the sampling frequency in C5 is lower.

Lastly, a table summarizing the approximate linear ranges of the designs in each process are documented and presented below:

KD1S Design	**AMS PDK**	**C5 PDK**
1st Order KD1S	0.5 V ~ 2.8V	1.0 V ~ 4.0 V
2nd Order KD1S	0.6V ~ 2.7 V	1.1 V ~ 3.9 V

Table 6.1 - Linear ranges of designs in AMS and C5

6.1.2 DIFFERENT INPUT AMPLITUDES

The second type of test that was performed on the KD1S designs is checking the output performance for different input amplitudes. The input amplitudes investigated were selected from the linear ranges specified in Table 6.1 for preventing output saturation. One extreme case will be presented in the table to show the effect of saturation on the design performance. The input sinusoidal signal contains an offset of $V_{cm} = 1.65V$ for AMS and $V_{cm} = 2.5V$ for C5. An amplitude is specified so that the peak to peak voltage is within the linear range. Simulations for each process have the same settings. AMS has a *VDD* of 3.3 V, input frequency of 1 MHz, and a sampling frequency of 123 MHz at 3.3 V input control voltage. The C5 process has a 5 V *VDD*, 1 MHz input frequency, and sampling of 100 MHz at 5 V input control voltage. The bandwidth of the output will depend on the following equation:

$$B = \frac{f_{s,new}}{2 \cdot OSR_{effective}} \tag{6.6}$$

Different amplitude results will be shown for first order KD1S design in the two processes. Next, the second order designs in the two processes will be summarized. The amplitudes used in the simulations will be indicated on the left side of the tables.

Starting with the first order KD1S in the AMS process, three different amplitude results will be shown and later compared to the C5 process. Note that the ranges of both processes are different as the supply voltages differ.

1st AMS	Parameter	*S 64*	*P 64*	*S 128*	*P 128*	*S 256*	*P 256*
V_{pp} 0.7 V	$f_{s,new}$	983 MHz	123 MHz	983 MHz	123 MHz	983 MHz	123 MHz
	SNR	46.89	45.13	57.05	54.11	63.45	60.40
	N_{eff}	7.49	7.20	9.18	8.69	10.24	9.74
	BW	7.68MHz	7.68MHz	3.84MHz	3.84MHz	1.92MHz	1.92MHz
V_{pp} 1.0 V	$f_{s,new}$	983 MHz	123 MHz	983 MHz	123 MHz	983 MHz	123 MHz
	SNR	49.33	47.31	61.73	58.90	69.90	67.61
	N_{eff}	7.90	7.56	9.96	9.49	11.31	10.94
	BW	7.68MHz	7.68MHz	3.84MHz	3.84MHz	1.92MHz	1.92MHz
V_{pp} 1.5 V	$f_{s,new}$	983 MHz	123 MHz	983 MHz	123 MHz	983 MHz	123 MHz
	SNR	32.37	31.17	42.51	41.92	48.45	47.28
	N_{eff}	5.08	4.89	6.77	6.67	7.76	7.56
	BW	7.68MHz	7.68MHz	3.84MHz	3.84MHz	1.92MHz	1.92MHz

Table 6.2 - First order KD1S in **AMS** process with different amplitudes

1st C5	Parameter	*S 64*	*P 64*	*S 128*	*P 128*	*S 256*	*P 256*
V_{pp} 1.5 V	$f_{s,new}$	853 MHz	106 MHz	853 MHz	106 MHz	853 MHz	106 MHz
	SNR	40.16	35.81	50.43	49.20	55.42	53.90
	N_{eff}	6.38	5.65	8.08	7.88	8.91	8.66
	BW	6.66MHz	6.66MHz	3.33MHz	3.33MHz	1.67MHz	1.67MHz
V_{pp} 1.8 V	$f_{s,new}$	853 MHz	106 MHz	853 MHz	106 MHz	853 MHz	106 MHz
	SNR	41.31	37.69	50.79	46.65	55.72	54.06
	N_{eff}	6.57	5.97	8.14	7.45	8.96	8.68
	BW	6.66MHz	6.66MHz	3.33MHz	3.33MHz	1.67MHz	1.67MHz
V_{pp} 2 V	$f_{s,new}$	853 MHz	106 MHz	853 MHz	106 MHz	853 MHz	106 MHz
	SNR	32.37	31.17	42.51	41.92	48.45	47.28
	N_{eff}	5.08	4.89	6.77	6.67	7.76	7.56
	BW	6.66MHz	6.66MHz	3.33MHz	3.33MHz	1.67MHz	1.67MHz

Table 6.3 - First Order KD1S in **C5** process with different amplitudes

For concise tables, abbreviations were used for serial and parallel as *S* and *P*, peak to peak voltage as *Vpp*, and bandwidth as *BW*. Comparing Tables 6.2 and 6.3, the highest resolution for the first order modulators in both processes occurs at amplitudes in the middle of the linear input range. As it can be seen all the serial values are higher than the parallel outputs due to the loss of information as mentioned in the earlier chapter. As the amplitude gets close to the *VDD* of the design, the SNR and ENOB degrade drastically since saturation occurs, this is the worst case that was mentioned.

The AMS process achieved higher resolution than the C5 process for most of the OSR values. Moreover, increasing the effective OSR to 256, led to the highest resolution result out of the other effective OSR values. Next, the same tables are shown for the second order design in AMS and C5.

2nd AMS	**Parameter**	***S 64***	***P 64***	***S 128***	***P 128***	***S 256***	***P 256***
V_{pp} **0.7 V**	$f_{s,new}$	983 MHz	123 MHz	983 MHz	123 MHz	983 MHz	123 MHz
	SNR	54.60	49.15	71.40	60.48	73.36	68.80
	N_{eff}	8.77	7.87	11.56	9.75	11.89	11.13
	BW	7.68MHz	7.68MHz	3.84MHz	3.84MHz	1.92MHz	1.92MHz
V_{pp} **1.0 V**	$f_{s,new}$	983 MHz	123 MHz	983 MHz	123 MHz	983 MHz	123 MHz
	SNR	49.61	47.95	64.91	61.05	75.20	72.60
	N_{eff}	7.95	7.67	10.49	9.85	12.20	11.76
	BW	7.68MHz	7.68MHz	3.84MHz	3.84MHz	1.92MHz	1.92MHz
V_{pp} **1.4 V**	$f_{s,new}$	983 MHz	123 MHz	983 MHz	123 MHz	983 MHz	123 MHz
	SNR	36.75	36.60	49.77	49.54	61.77	61.34
	N_{eff}	5.81	5.78	7.97	7.93	9.97	9.89
	BW	7.68MHz	7.68MHz	3.84MHz	3.84MHz	1.92MHz	1.92MHz

Table 6.4 - Second order KD1S in **AMS** process with different amplitudes

2nd C5	Parameter	*S 64*	*P 64*	*S 128*	*P 128*	*S 256*	*P 256*
V_{pp} 1.5 V	$f_{s,new}$	853 MHz	106 MHz	853 MHz	106 MHz	853 MHz	106 MHz
	SNR	46.57	43.04	59.72	58.79	67.12	65.50
	N_{eff}	7.44	6.85	9.62	9.47	10.85	10.59
	BW	6.66MHz	6.66MHz	3.33MHz	3.33MHz	1.67MHz	1.67MHz
V_{pp} 1.8 V	$f_{s,new}$	853 MHz	106 MHz	853 MHz	106 MHz	853 MHz	106 MHz
	SNR	45.65	42.64	60.01	56.62	65.90	64.78
	N_{eff}	7.29	6.79	9.67	9.11	10.65	10.47
	BW	6.66MHz	6.66MHz	3.33MHz	3.33MHz	1.67MHz	1.67MHz
V_{pp} 2 V	$f_{s,new}$	853 MHz	106 MHz	853 MHz	106 MHz	853 MHz	106 MHz
	SNR	42.37	38.23	51.35	48.87	55.35	54.74
	N_{eff}	6.74	6.06	8.23	7.82	8.90	8.80
	BW	6.66MHz	6.66MHz	3.33MHz	3.33MHz	1.67MHz	1.67MHz

Table 6.5 - Second order KD1S in **C5** process with different amplitudes

The second order KD1S in the AMS process was able to achieve a 12-bit resolution using an OSR of 256. Since the KD1S is a second order topology, the system is more prone to instability if the input amplitude is large. The input amplitude of 1.5 V caused the system to oscillate in the AMS process, shown in Table 6.4, and become unstable, which is why another amplitude was provided in the table. The degradation in SNR is apparent in the tables as the input signal reaches the rail voltage.

The simulated SNR results can be compared to the ideal SNR equations from Chapter 5. Taking into consideration that the ideal SNR will be higher than the simulated SNR, because an ideal filter was used to derive these equations while an averaging filter was applied to the data in MATLAB to achieve the results shown in the tables. Using Equations 5.19 and 5.34, the following table is formed for the ideal effective number of bits for different OSR values.

Effective OSR	First Order KD1S	Second Order KD1S
64	9.43	14.15
128	10.93	16.65
256	12.40	19.15

Table 6.6 - Ideal resolution for different OSR

As seen in Table 6.6, the ideal values are higher than the simulation results.

The MATLAB script also generates time and frequency domain plots of the signals in serial and parallel mode. Plots for the first order KD1S in the AMS process are shown below:

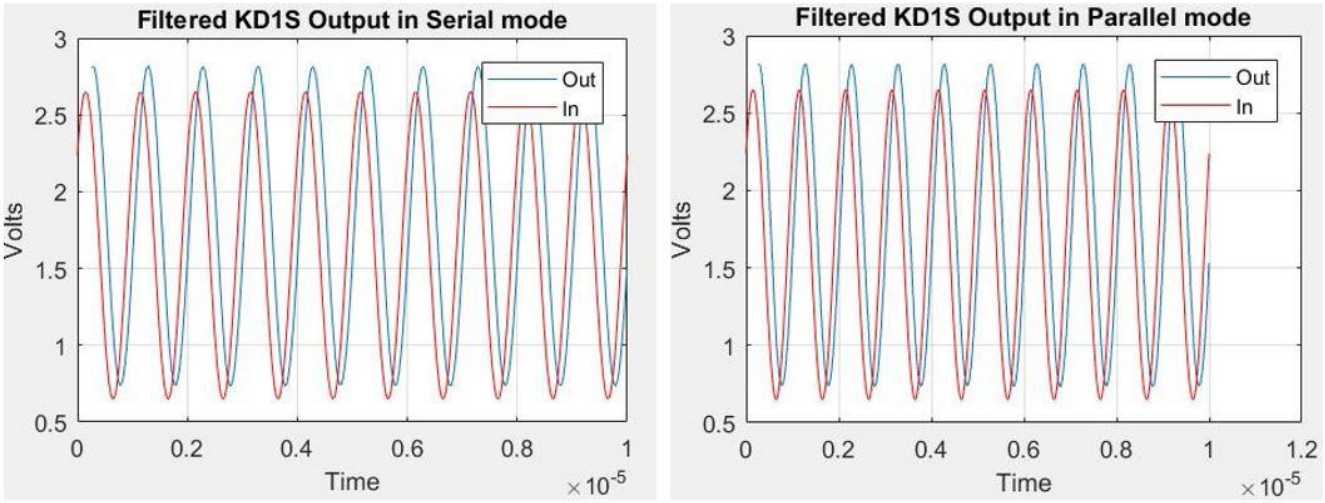

Figure 6.6 - Time domain of first order KD1S at 1.0 V amplitude

The following is the output for an amplitude of 1.0 V. The time domain shows both serial and parallel filtered signals. The signals are seen to be shifted up, but this can be fixed digitally. Looking at the time domain plots does not offer much insight into the KD1S operation. Therefore, frequency domain output of the same circuit is shown next in serial and parallel modes.

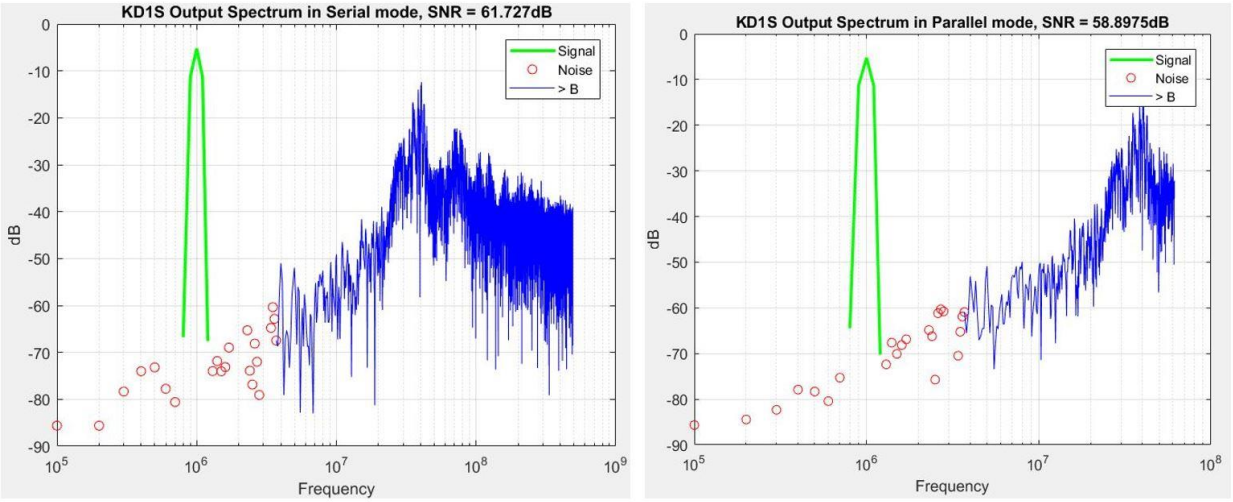

Figure 6.7 - Frequency domain of first order KD1S using 1.0 V amplitude

Figure 6.7 shows the spectrum of the output; the red dots represent the noise while green is the input signal shown with 5 data points due to the windowing that was applied to clean up the edges of the signal. The modulation noise is seen at higher frequencies outside the desired spectrum, and a small amount of noise is left in the baseband.

6.1.3 DIFFERENT SAMPLING FREQUENCIES

Moreover, the sampling frequency can be changed in the designs by changing the input voltage of the clock generator. The clock generator implemented in the AMS process can be varied in frequency within 37 MHz ~ 122 MHz, on the other hand, the C5 process frequency ranges within 70 MHz ~ 106 MHz. In some cases, using a slower sampling frequency can actually increase the resolution because the clock pulses are more ideal in shape. This results in a more ideal feedback signal through the DAC and decreases the nonlinearities in the signal. This phenomenon is only due to the use of a non-ideal clock and can be mitigated with better clock generator design. The maximum sampling frequencies from the designs were already used in the previous sections,

therefore, other frequencies in the clock generator range were chosen. The amplitude with the best results from Section 6.1.2 were used in their corresponding KD1S design.

The first order KD1S in the AMS process was simulated first, the results are shown in Table 6.7:

1st AMS	**Parameter**	**S 64**	**P 64**	**S 128**	**P 128**	**S 256**	**P 256**
f_{in} **450kHz** f_s **37 MHz**	$f_{s,new}$	301 MHz	38 MHz	301 MHz	38 MHz	301 MHz	38 MHz
	SNR	54.15	45.57	61.99	59.28	69.88	67.93
	N_{eff}	8.70	7.27	10.00	9.55	11.31	10.99
	BW	2.35MHz	2.35MHz	1.18MHz	1.18MHz	0.59MHz	0.59MHz
f_{in} **900kHz** f_s **68 MHz**	$f_{s,new}$	562 MHz	70 MHz	562 MHz	70 MHz	562 MHz	70 MHz
	SNR	52.17	49.69	62.82	59.36	71.40	67.63
	N_{eff}	8.37	7.96	10.14	9.57	11.56	10.94
	BW	4.39MHz	4.39MHz	2.20MHz	2.20MHz	1.10MHz	1.10MHz
f_{in} **950kHz** f_s **86 MHz**	$f_{s,new}$	859 MHz	107 MHz	859 MHz	107 MHz	859 MHz	107 MHz
	SNR	48.93	46.85	61.87	58.20	66.40	66.23
	N_{eff}	7.83	7.49	9.98	9.37	10.73	10.71
	BW	6.71MHz	6.71MHz	3.35MHz	3.35MHz	1.68MHz	1.68MHz

Table 6.7 - First order KD1S in **AMS** process with different f_s

1st C5	**Parameter**	**S 64**	**P 64**	**S 128**	**P 128**	**S 256**	**P 256**
f_{in} **690kHz** f_s **69 MHz**	$f_{s,new}$	553 MHz	69 MHz	553 MHz	69 MHz	553 MHz	69 MHz
	SNR	39.16	36.16	46.80	45.27	49.65	49.00
	N_{eff}	6.21	5.71	7.48	7.22	7.95	7.84
	BW	4.32MHz	4.32MHz	2.16MHz	2.16MHz	1.08MHz	1.08MHz
f_{in} **800kHz** f_s **80 MHz**	$f_{s,new}$	662 MHz	83 MHz	662 MHz	83 MHz	662 MHz	83 MHz
	SNR	39.60	38.78	47.98	47.29	49.82	49.76
	N_{eff}	6.28	6.15	7.67	7.56	7.98	7.97
	BW	5.17MHz	5.17MHz	2.59MHz	2.59MHz	1.29MHz	1.29MHz

f_{in} **980kHz** f_s **98 MHz**	$f_{s,new}$	779 MHz	97 MHz	779 MHz	97 MHz	779 MHz	97 MHz
	SNR	42.66	37.22	50.63	49.05	60.28	57.25
	N_{eff}	6.79	5.89	8.11	7.85	9.72	9.22
	BW	6.08MHz	6.08MHz	3.04MHz	3.04MHz	1.52MHz	1.52MHz

Table 6.8 - First Order KD1S in **C5** process with different f_s

The clock generator in the AMS process contains a broader range than the C5 process, and the frequency changes more linearly with the input voltage as well. This could be due to the use of a different bias circuit for the CS bias voltages, the C5 has a cascaded bias circuit while the AMS contains a single stage bias circuit. The AMS was tested at a frequency of 107 MHz, which is the maximum frequency of the KD1S in the C5 process, for comparison. The KD1S in the AMS process achieves higher resolution than the C5 process when sampling at the same frequency. Second order KD1S with different frequencies were simulated next:

1st AMS	**Parameter**	**S 64**	**P 64**	**S 128**	**P 128**	**S 256**	**P 256**
f_{in} **450kHz** f_s **37 MHz**	$f_{s,new}$	301 MHz	38 MHz	301 MHz	38 MHz	301 MHz	38 MHz
	SNR	50.18	50.65	66.60	64.93	76.66	71.94
	N_{eff}	8.04	8.12	10.77	10.49	12.44	11.65
	BW	2.35MHz	2.35MHz	1.18MHz	1.18MHz	0.59MHz	0.59MHz
f_{in} **900kHz** f_s **68 MHz**	$f_{s,new}$	562 MHz	70 MHz	562 MHz	70 MHz	562 MHz	70 MHz
	SNR	51.13	50.34	69.33	62.56	77.99	72.79
	N_{eff}	8.20	8.07	11.22	10.10	12.66	11.80
	BW	4.39MHz	4.39MHz	2.20MHz	2.20MHz	1.10MHz	1.10MHz
f_{in} **950kHz** f_s **86 MHz**	$f_{s,new}$	859 MHz	107 MHz	859 MHz	107 MHz	859 MHz	107 MHz
	SNR	50.26	49.22	63.74	63.40	74.53	69.72
	N_{eff}	8.05	7.88	10.29	10.24	12.09	11.29
	BW	6.71MHz	6.71MHz	3.35MHz	3.35MHz	1.68MHz	1.68MHz

Table 6.9 - Second order KD1S in **AMS** process with different f_s

1st C5	Parameter	S 64	P 64	S 128	P 128	S 256	P 256
f_{in} 690kHz f_s 69 MHz	$f_{s,new}$	553 MHz	69 MHz	553 MHz	69 MHz	553 MHz	69 MHz
	SNR	47.76	73.14	58.73	57.35	65.36	64.83
	N_{eff}	7.64	6.87	9.46	9.23	10.56	10.47
	BW	4.32MHz	4.32MHz	2.16MHz	2.16MHz	1.08MHz	1.08MHz
f_{in} 800kHz f_s 80 MHz	$f_{s,new}$	662 MHz	83 MHz	662 MHz	83 MHz	662 MHz	83 MHz
	SNR	48.93	43.83	56.77	53.82	59.99	57.16
	N_{eff}	7.83	6.98	9.13	8.64	9.67	9.20
	BW	5.17MHz	5.17MHz	2.59MHz	2.59MHz	1.29MHz	1.29MHz
f_{in} 980kHz f_s 98 MHz	$f_{s,new}$	779 MHz	97 MHz	779 MHz	97 MHz	779 MHz	97 MHz
	SNR	47.42	43.64	57.84	55.69	61.56	61.36
	N_{eff}	7.58	6.95	9.31	8.95	9.93	9.90
	BW	6.08MHz	6.08MHz	3.04MHz	3.04MHz	1.52MHz	1.52MHz

Table 6.10 - Second Order KD1S in **C5** process with different f_s

The input frequency in Tables 6.7 to 6.10 was changed accordingly each time to be within the new design bandwidth at the corresponding sampling frequency. The new input frequencies were indicated on the left side of the tables. Equation 6.6 shows that decreasing the sampling frequency directly decreases the bandwidth of the system, which is why the input frequency is altered to be within the system's input bandwidth. The AMS process in first and second order designs are seen to perform better with sampling frequencies that occur in the middle of the clock generator frequency range, while C5 operates better with the highest sampling frequency.

6.1.4 DIFFERENT INPUT FREQUENCIES

In addition, different input frequencies were tested to characterize the KD1S efficiency. The output filter bandwidth was kept constant for the same sampling frequency. This had the effect of artificially improving the resolution of higher input signal frequencies by eliminating more of the

harmonics. For The sampling frequencies used in this simulation are the maximum f_s of both processes, 106 MHz and 122 MHz.

Tables 6.11 and 6.12 include the results for the 1st order KD1S in the AMS and C5 process at different input frequencies:

1st AMS	Parameter	S 64	P 64	S 128	P 128	S 256	P 256
f_{in} 100kHz	$f_{s,new}$	983 MHz	123 MHz	983 MHz	123 MHz	983 MHz	123 MHz
	SNR	50.60	47.06	58.62	55.62	64.17	63.15
	N_{eff}	8.11	7.52	9.44	8.94	10.36	10.19
	BW	7.68MHz	7.68MHz	3.84MHz	3.84MHz	1.92MHz	1.92MHz
f_{in} 300kHz	$f_{s,new}$	983 MHz	123 MHz	983 MHz	123 MHz	983 MHz	123 MHz
	SNR	49.53	47.11	57.29	55.53	63.18	61.73
	N_{eff}	7.93	7.53	9.22	8.93	10.20	9.96
	BW	7.68MHz	7.68MHz	3.84MHz	3.84MHz	1.92MHz	1.92MHz
f_{in} 500kHz	$f_{s,new}$	983 MHz	123 MHz	983 MHz	123 MHz	983 MHz	123 MHz
	SNR	49.27	46.89	57.72	54.75	68.21	66.60
	N_{eff}	7.89	7.49	9.29	8.80	11.03	10.77
	BW	7.68MHz	7.68MHz	3.84MHz	3.84MHz	1.92MHz	1.92MHz

Table 6.11 - First order KD1S in **AMS** process with different input frequency

1st C5	Parameter	S 64	P 64	S 128	P 128	S 256	P 256
f_{in} 100kHz	$f_{s,new}$	853 MHz	106 MHz	853 MHz	106 MHz	853 MHz	106 MHz
	SNR	40.64	36.93	43.76	43.25	46.89	46.57
	N_{eff}	6.46	5.84	6.97	6.89	7.49	7.44
	BW	6.66MHz	6.66MHz	3.33MHz	3.33MHz	1.67MHz	1.67MHz
f_{in} 300kHz	$f_{s,new}$	853 MHz	106 MHz	853 MHz	106 MHz	853 MHz	106 MHz
	SNR	39.90	37.48	44.97	43.05	49.29	48.51
	N_{eff}	6.33	5.93	7.18	6.86	7.89	7.76
	BW	6.66MHz	6.66MHz	3.33MHz	3.33MHz	1.67MHz	1.67MHz

f_{in} **500kHz**	$f_{s,new}$	853 MHz	106 MHz	853 MHz	106 MHz	853 MHz	106 MHz
	SNR	40.60	37.47	45.43	42.72	49.66	48.30
	N_{eff}	6.45	5.93	7.25	6.80	7.95	7.73
	BW	6.66MHz	6.66MHz	3.33MHz	3.33MHz	1.67MHz	1.67MHz

Table 6.12 - First Order KD1S in **C5** process with different input frequency

As shown in Tables 6.11 and 6.12, the higher input frequencies resulted in the highest resolution, which is unexpected and can be explained as follows. The output filter bandwidth was kept constant for the same sampling frequency. This had the effect of artificially improving the resolution of higher input signal frequencies by eliminations more of the harmonics.

For example, some of the results with a 100 KHz input frequency have a lower resolution than the results with a 1 MHz input frequency. This is counterintuitive as noise shaping should lead to higher resolutions for lower input frequencies. The reason for this discrepancy is that the MATLAB filter removes the first 5 harmonics to compute the SNR. However, there are often significant spurs out to the 10^{th} harmonic and beyond. This will show up for a lower input signal frequency but not for a higher one due to the filter bandwidth. The decision was made to keep the filter bandwidth the same because most applications are not optimized for a single input frequency. The second order designs in AMS and C5 are detailed below, the same behavior is seen with having higher resolution for higher input frequencies.

1st AMS	Parameter	S 64	P 64	S 128	P 128	S 256	P 256
f_{in} 100kHz	$f_{s,new}$	983 MHz	123 MHz	983 MHz	123 MHz	983 MHz	123 MHz
	SNR	50.30	47.78	64.38	58.87	74.34	68.41
	N_{eff}	8.06	7.64	10.40	9.48	12.05	11.07
	BW	7.68MHz	7.68MHz	3.84MHz	3.84MHz	1.92MHz	1.92MHz
f_{in} 300kHz	$f_{s,new}$	983 MHz	123 MHz	983 MHz	123 MHz	983 MHz	123 MHz
	SNR	48.71	46.70	62.85	59.38	71.36	67.36
	N_{eff}	7.80	7.46	10.15	9.57	11.56	10.89
	BW	7.68MHz	7.68MHz	3.84MHz	3.84MHz	1.92MHz	1.92MHz
f_{in} 500kHz	$f_{s,new}$	983 MHz	123 MHz	983 MHz	123 MHz	983 MHz	123 MHz
	SNR	49.45	48.55	62.66	58.67	76.73	72.05
	N_{eff}	7.92	7.77	10.11	9.45	12.45	11.67
	BW	7.68MHz	7.68MHz	3.84MHz	3.84MHz	1.92MHz	1.92MHz

Table 6.13 - Second order KD1S in **AMS** process with different input frequency

1st AMS	Parameter	S 64	P 64	S 128	P 128	S 256	P 256
f_{in} 100kHz	$f_{s,new}$	853 MHz	106 MHz	853 MHz	106 MHz	853 MHz	106 MHz
	SNR	46.48	43.09	52.33	50.78	55.10	54.91
	N_{eff}	7.42	6.86	8.40	8.14	8.86	8.83
	BW	6.66MHz	6.66MHz	3.33MHz	3.33MHz	1.67MHz	1.67MHz
f_{in} 300kHz	$f_{s,new}$	853 MHz	106 MHz	853 MHz	106 MHz	853 MHz	106 MHz
	SNR	45.76	42.77	52.21	50.81	55.34	54.80
	N_{eff}	7.31	6.81	8.38	8.14	8.90	8.81
	BW	6.66MHz	6.66MHz	3.33MHz	3.33MHz	1.67MHz	1.67MHz
f_{in} 500kHz	$f_{s,new}$	853 MHz	106 MHz	853 MHz	106 MHz	853 MHz	106 MHz
	SNR	46.76	43.69	52.16	50.40	60.92	59.87
	N_{eff}	7.47	6.96	8.37	8.08	9.82	9.65
	BW	6.66MHz	6.66MHz	3.33MHz	3.33MHz	1.67MHz	1.67MHz

Table 6.14 - Second order KD1S in **C5** process with different input frequency

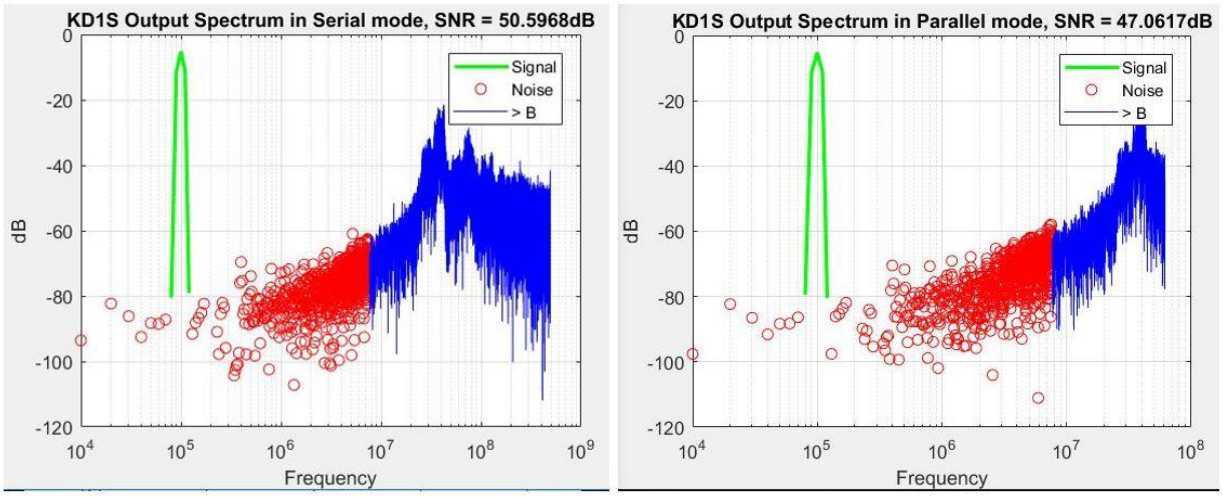

Figure 6.8 - Spectrum of First order KD1S with 100 kHz input frequency (in AMS)

The simulations in this section required many samples as the input frequency was reduced. Due to the number of captured samples, the frequency spectrum produced by MATLAB shows a good representation of noise shaping. Spectrums of Table 6.11 at 100 kHz are shown in Figure 6.8, modulation noise is seen to be low at lower frequencies and concentrated heavily at higher frequencies.

6.2 KD1S POWER ANALYSIS

Low power considerations were maintained when designing the KD1S modulator, like using minimum sizes for logic gates. The most power consuming components in the design are the operational amplifier used as an integrator and the comparators. Two tables were constructed to break down the power consumption in the designs for the two processes.

. The op-amp is the component in the designs that consumes the most amount of power. Thus, the second order KD1S is seen to reach higher power consumptions than the first order design. Table 6.15 displays the power utilization of the op-amp and comparator.

Component	AMS (in RMS)	C5 (in RMS)
Op-amp	$1.8644\ mA \cdot 3.3V = \mathbf{6.153\ mW}$	$7.378\ mA \cdot 5V = \mathbf{36.89\ mW}$
Comparator	$605.82\ \mu A \cdot 3.3V = \mathbf{1.999\ mW}$	$1.373\ mA \cdot 5V = \mathbf{6.865\ mW}$

Table 6.15 - Power consumption of op-amp and comparator in AMS and C5

Knowing that the first order design contains one integrator and eight comparators the power is shown in Table 6.16 along with the passive components. Second order design uses two integrators and eight comparators leading to higher use of power.

Design	AMS (in RMS)	C5 (in RMS)
1st Order KD1S	$9.7822\ mA \cdot 3.3V = \mathbf{32.28\ mW}$	$31.628\ mA \cdot 5V = \mathbf{158.14\ mW}$
2nd Order KD1S	$10.8208\ mA \cdot 3.3V = \mathbf{35.708\ mW}$	$39.204\ mA \cdot 5V = \mathbf{196.02\ mW}$

Table 6.16 - Power expenditure of the first and second order KD1S designs

6.3 LAYOUT

Second order KD1S modulator layout was executed in the AMS process using Cadence. The design utilizes a total of 22 pins, the pin layout is summarized in Table 6.17. Pins were connected to either a digital or an analog pad, the digital pads contain ESD protection as well as buffers to prevent loading, while analog pads only contain ESD protection. Three pins were connected to the reference voltages; ground and *VDD*. Eight input clock pins were added for backup in case the internal clock generator fails. Having external clock pins enables the connection to high speed clock generator like DG535 pulse generator that can create non-overlapping clocks. The clock pads were digital so that they are isolated from external effects. Moreover, the clock generator has its own power supply voltage so that the device can be off in case the use of the external clocks was desired.

Pin Number	Pin Name
Pin<23>	$V_{vco,VDD}$
Pin<24>	VDD
Pin<25>	V_{cm}
Pin<26>	V_{in}
Pin<27>	$V_{in,vco}$
Pin<28>	p_1
Pin<29>	p_2
Pin<30>	p_3
Pin<31>	p_4
Pin<32>	p_5
Pin<33>	p_6
Pin<34>	p_7
Pin<35>	p_8
Pin<36>	b_0
Pin<37>	b_1
Pin<38>	b_2
Pin<39>	b_3
Pin<40>	b_4
Pin<1>	b_5
Pin<2>	b_6
Pin<3>	b_7
Pin<20>	GND

Table 6.17 - Pin layout table

Clock generator layout is seen in Figure 6.9, the left side of the layout contains the bias circuit for the CS inverter, and the eight stages share a single *VDD* and ground, therefore, in the layout the designs were connected in an up-side down manner to save space.

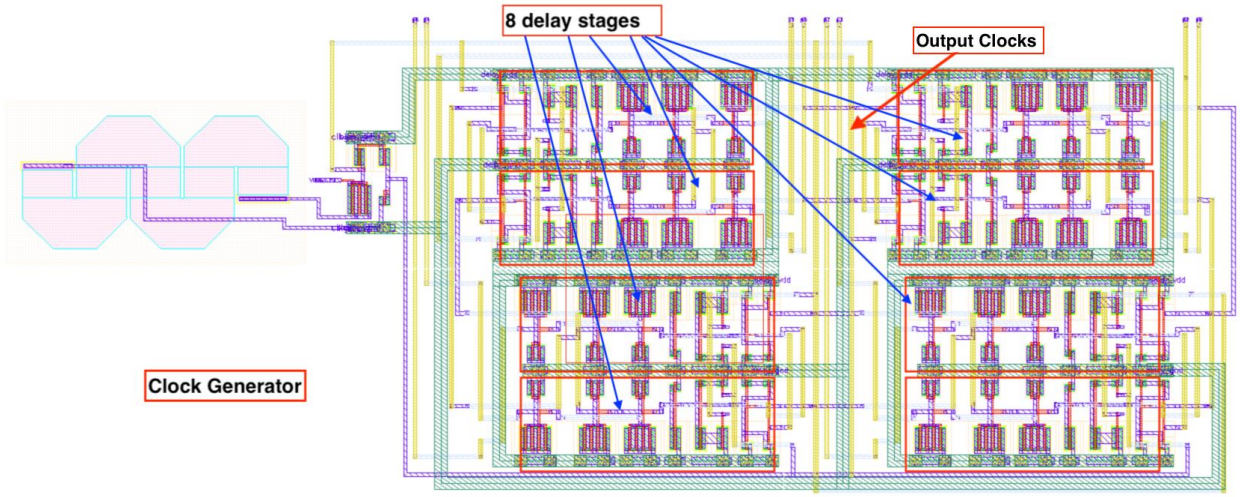

Figure 6.9 - Clock generator layout

The self-biased amplifier is shown next, the input devices are large PMOS devices and take most of the layout are as seen in Figure 6.10. Layout has differential inputs and outputs.

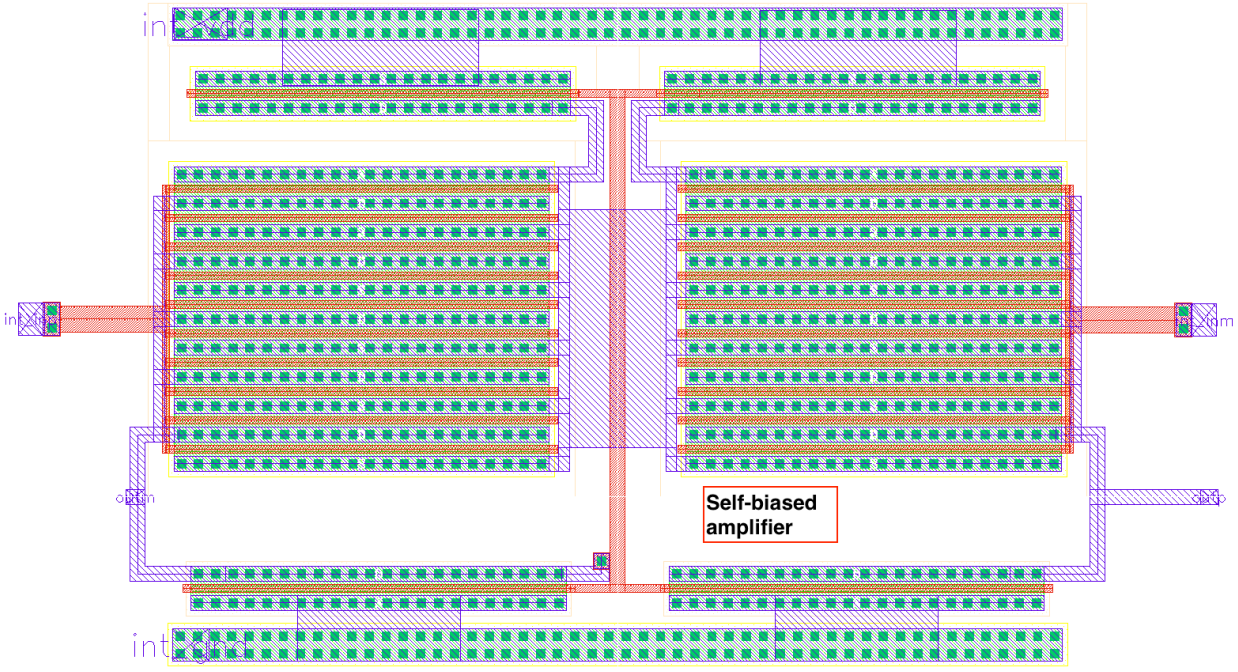

Figure 6.10 - Self biased amplifier layout

Next is the comparator layout in Figure 6.11, the same three stages are shown as in Figure 4.13.

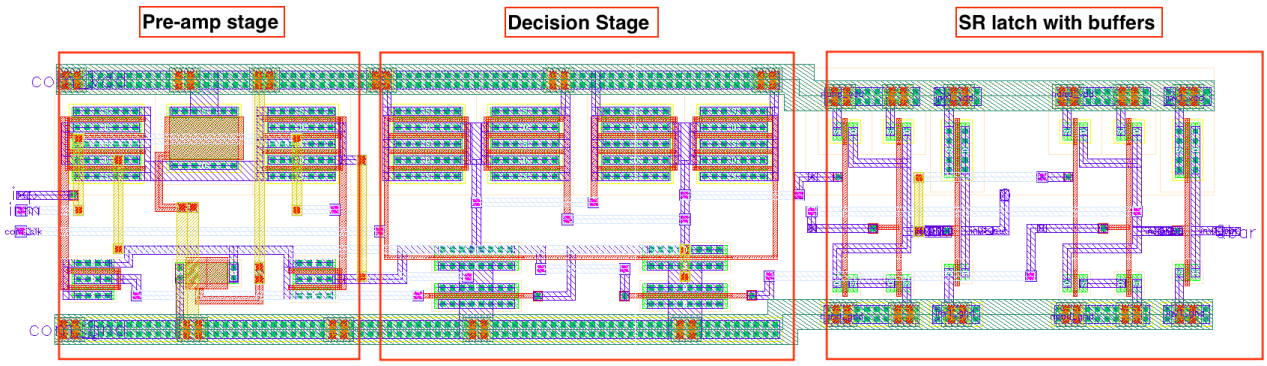

Figure 6.11 - Clocked comparator layout

The layout of the eight feedback paths is displayed in Figure 6.12, the resistors consume most of the area. Therefore, to reserve space the comparators, inverters, and TGs were placed in between resistors as annotated on the figure. The ground and power supply connections were once again connected up-side down.

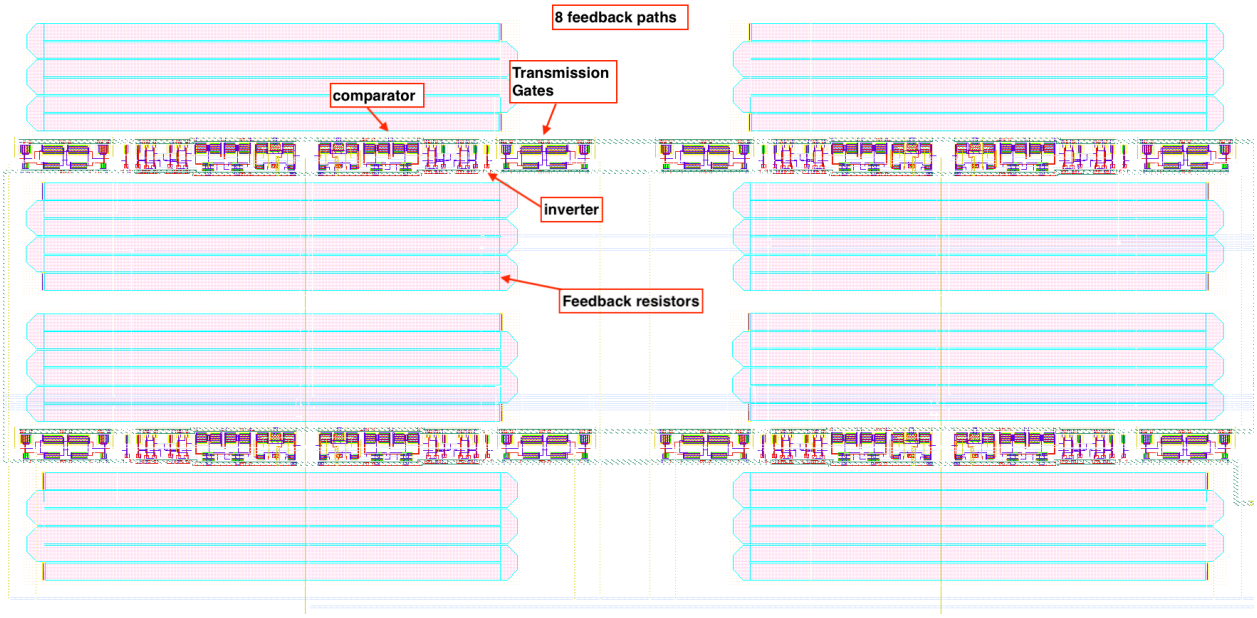

Figure 6.12 - Feedback path layout zoomed in

The register layout used a clock tree configuration to reduce any possible clock latency and have the bits delayed. The clock signals in this manner have the same path from any end by

branching the outputs as seen in Figure 6.13. The eight DFF are seen on the sides of the register with the buffers preceding the clock signals.

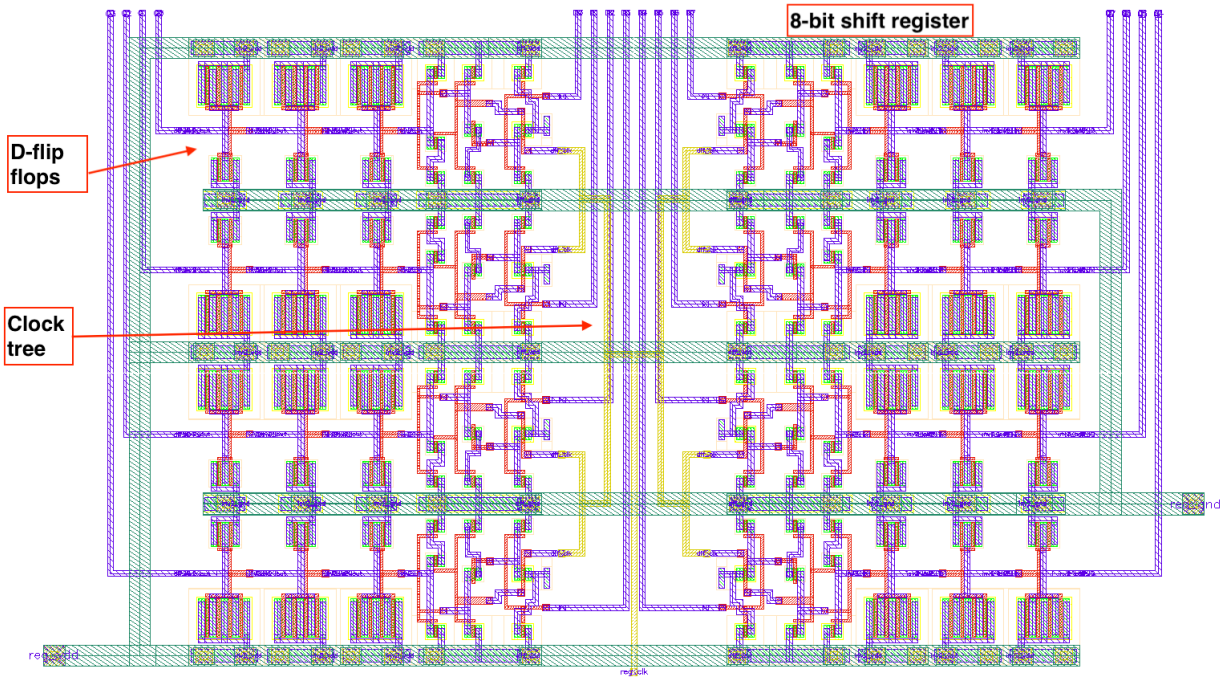

Figure 6.13 - 8-bit shift register layout

Figure 6.14 presents a zoomed in picture of the feedforward path.

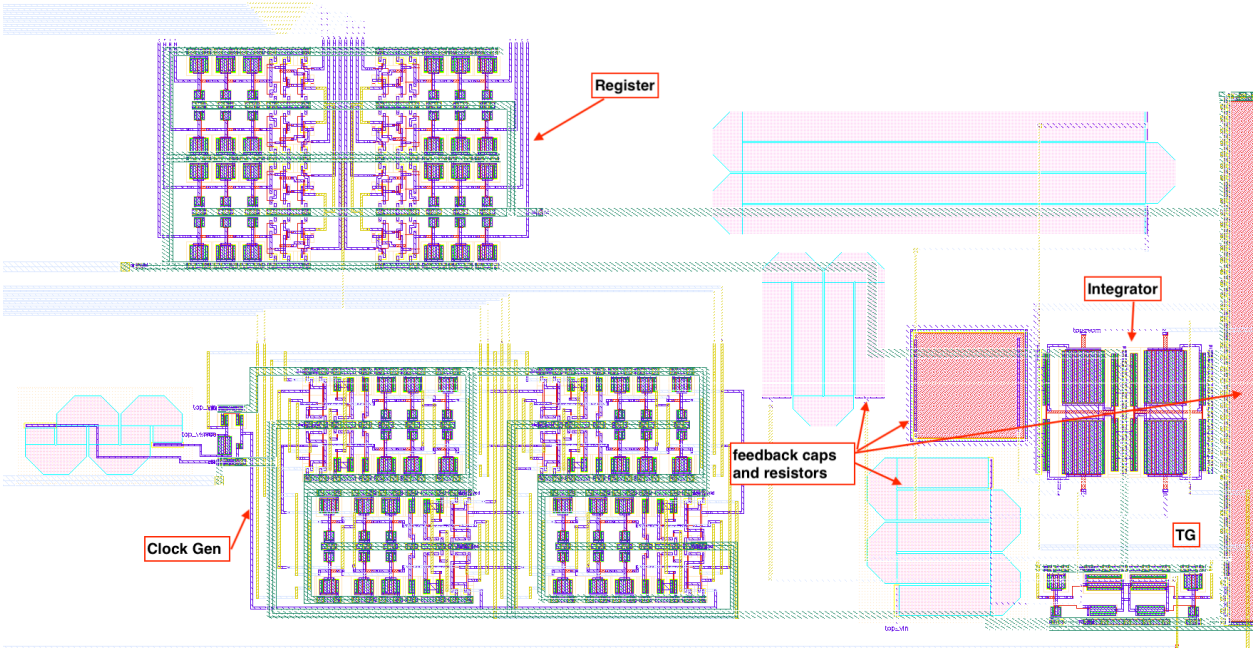

Figure 6.14 - Feedforward path zoomed in

Finally, the whole top level is shown in Figure 6.15, which includes all the layouts from previous figures combined. The top level occupies a $346\ \mu m\ \times\ 1369\ \mu m$ area.

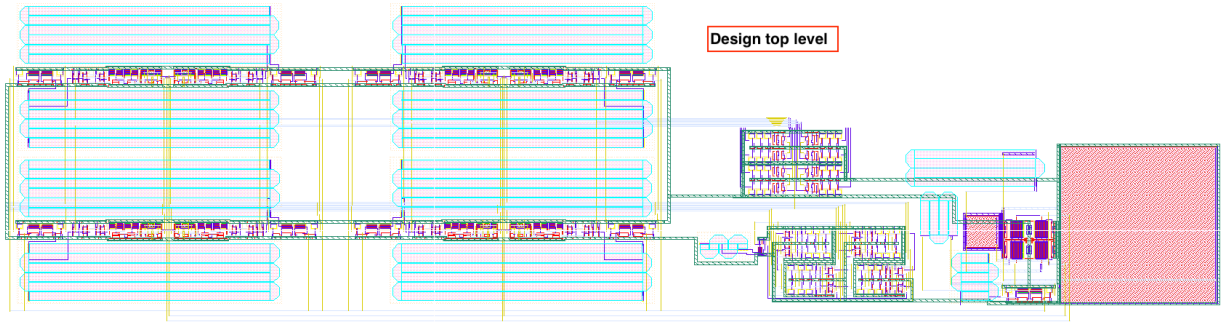

Figure 6.15 - Top level second order KD1S layout

The top-level layout was placed in a pad frame that contains 40 pads in total. The pads used for the KD1S pins were detailed earlier in Table 6.17. The top level has a total area of $1892\ \mu m\ \times\ 1892\ \mu m$. A different circuit was laid out to fill the space which is not related to this thesis.

The AMS process contains 4 metal layers, each metal layer was used in a certain direction for ease of connection in the top layer. Metal 1 was used everywhere and connected in any direction or angle. Metal 2 was only used horizontally, and mainly for the short connections. Metal 3 was only used vertically, and mainly for the clock signals as it is wide with low resistance. Lastly, Metal 4 was only used for the reference voltages, power supply and for ground. Metal 4 is the widest metal and on top of the cross section, which allows for power to experience less capacitance as it is far away from all the other metals.

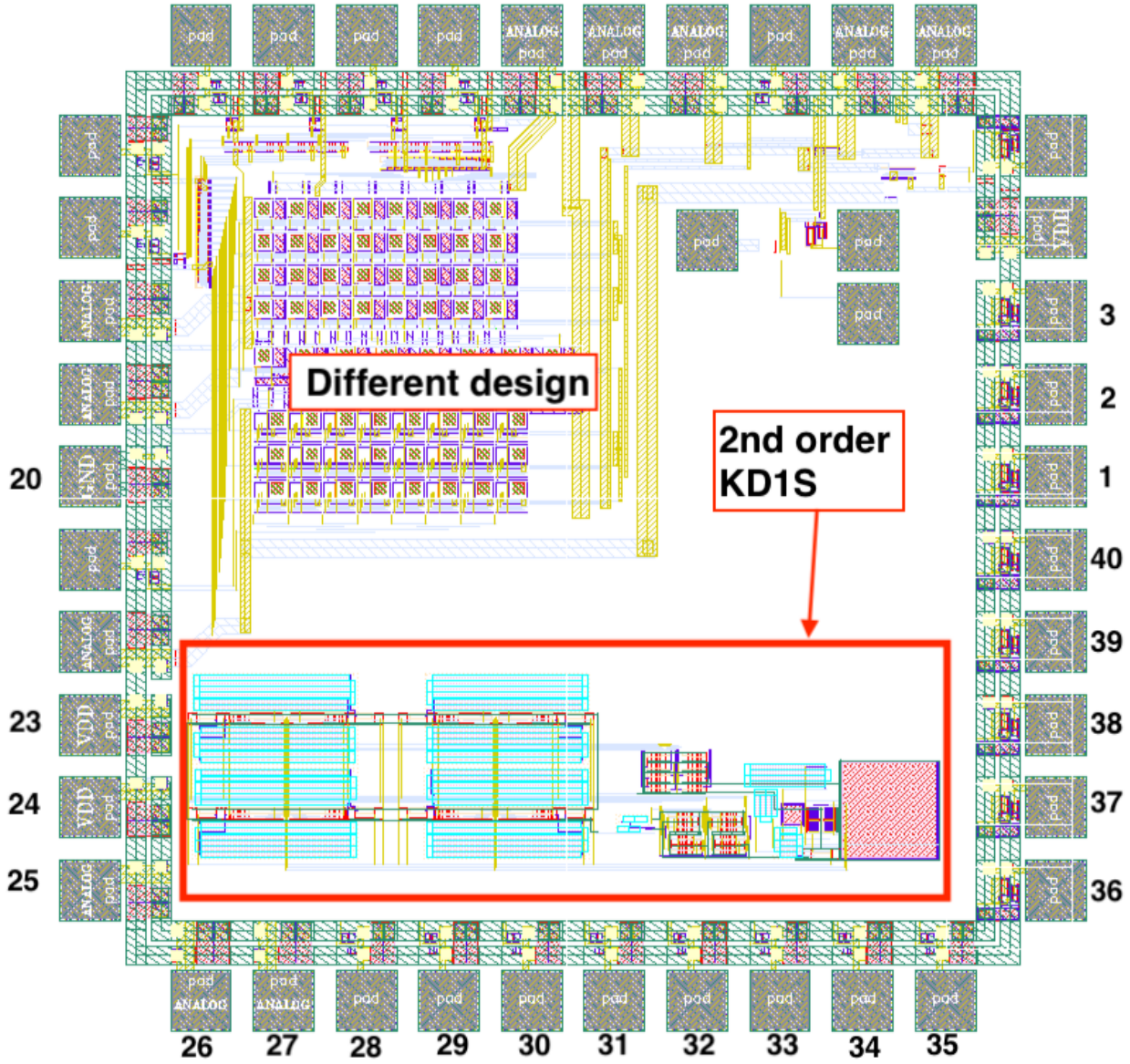

Figure 6.16 - Chip layout

6.4 CONCLUSION

After running different types of simulations, the AMS process can be concluded to perform better than the C5 process, which is due to the IC process feature size being smaller and faster as mentioned in the beginning of the chapter. Since the AMS process is smaller than the C5 and

utilizes lower supply voltage value, the AMS process in first and second order topologies consume power considerably less than the C5 designs. The K-Delta-1-Sigma design can achieve a resolution of 12 bits while maintaining high effective sampling frequency. Increasing the OSR can be executed in software and further filtering can be attained. Overall, the KD1S design achieved the purpose of high resolution, high speed, while maintaining low power for its given performance.

CHAPTER 7: APPLICATIONS AND FUTURE RESEARCH

The KD1S ADC can be used in many applications requiring both high speed and high resolution. One of the applications that would an ideal fit for the KD1S ADC is for communication systems. Wireless communication requires bandwidths that are within the KD1S design near the 1 GHz range. Some of the communication's applications can be in cellular, ultra-wide band communication in RFIC design, imaging, and testing and measurements.

Further improvements can be applied to the KD1S design to reduce power consumption further. To decrease the power consumption, alternative designs for the comparator and integrator could be used. For example, the comparator is a device that compares two inputs and decides on the output accordingly. The same behavior can be found in a clocked flip flop, only when the clock is high the flip flop would decide on an output. Changing the comparator to be a digital component can decrease the power drastically as smaller sizes can be used for logic gates.

Another area for further research is having a second order KD1S topology that combines passive and active integrators. Passive integrators encompass lower power utilization but cannot achieve high resolution alone. Combining a hybrid KD1S of active and passive could decrease the power consumption while maintaining the high resolution. The passive integrator would be placed first in the feedforward loop so that its effects can be filtered with the succeeding active integrator.

APPENDIX 1

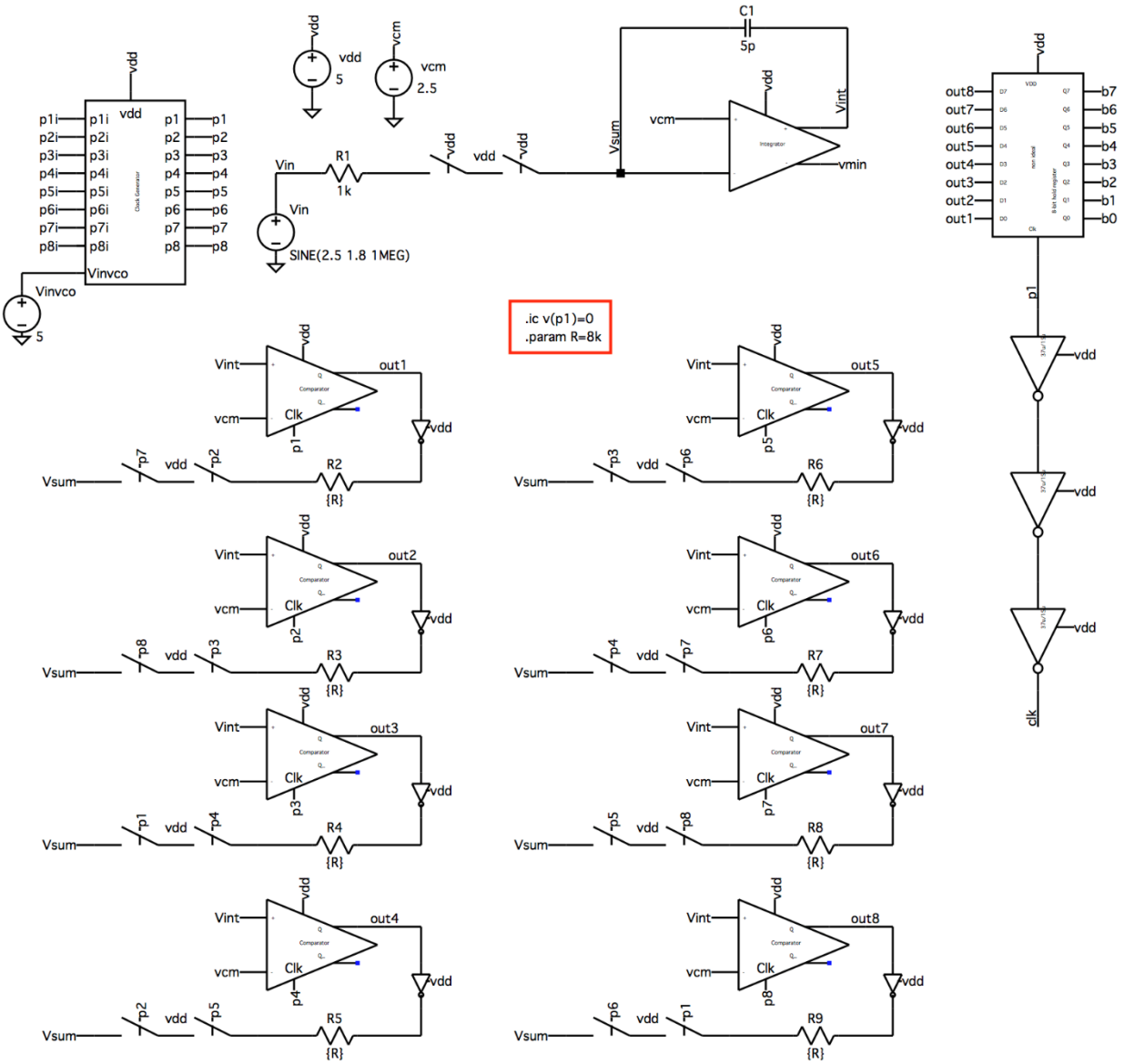

Figure A1 - First order KD1S modulator in C5 process

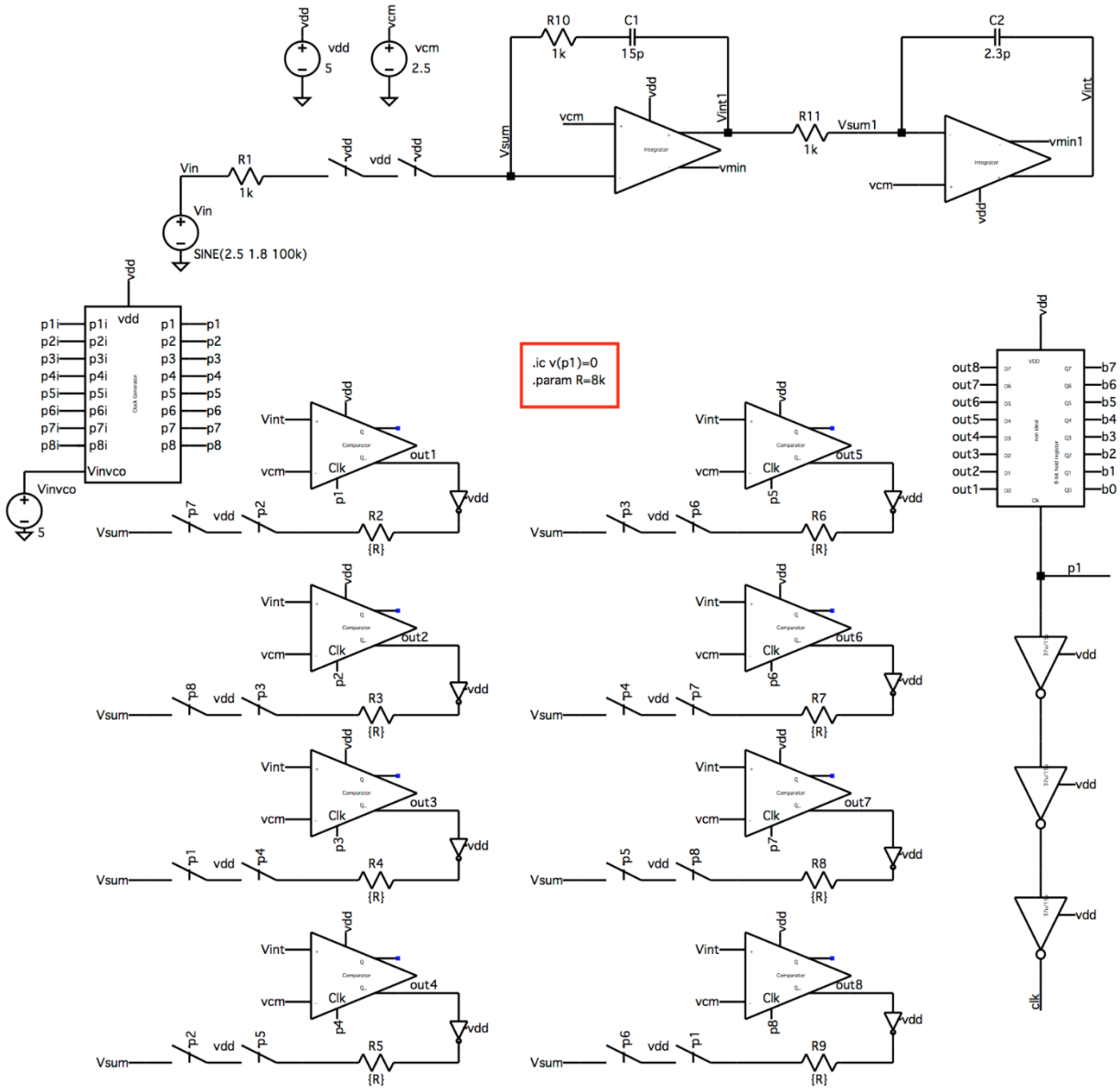

Figure A2 - Second order KD1S modulator in C5 process

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