DELTA SIGMA MODULATOR USED IN CMOS IMAGERS

by

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The project presented by Indira Priyadarshini Vemula entitled DELTA SIGMA

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I dedicate this work to my parents and brother. I would also like to thank all my friends and well-wishers for their encouragement and best wishes.

ABSTRACT

Image sensors consist of a pixel array where each pixel consists of a photosensitive diodes and an amplifier. These photodiodes take a portion of an image and convert it into electrons. Pixels produce an electrical signal representing the image. Analog-to-digital converters are used to convert the measured analog output signal into an easily readable digital form. The desired information regarding the signal is easily acquired from this digital signal.

Project Goals

- To test the performance of the delta sigma modulator used in CMOS imagers. The chip is fabricated in the MOSIS using 0.5um process.

- To design a delta sigma modulator to reduce the effects of mismatch.

Project Organization

Chapter one: A description of CMOS imagers and pixel implementation. In addition, the various types of ADCs used in the imaging system are discussed.

Chapter two: A description of different blocks used in a DSM: NMOS source follower, feedback circuit and comparator. In addition, the operation of the entire DSM circuit is discussed.

Chapter three: A description of the DSM circuit design used to eliminate mismatch and a description of the D-flipflop counter.

Chapter four: The results obtained from testing the DSM chip and also the simulation

results obtained from the circuit designed to eliminate mismatch.

Chapter five: The conclusion and future work of the design

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LIST OF ABBREVATIONS

BSU...Boise State University

DSM...Delta Sigma Modulation

MOS.. Metal Oxide Semiconductor

PMOS... P-channel Metal Oxide Semiconductor

NMOS ....N-channel Metal Oxide Semiconductor

SPICE.. Simulation Program with Integrated Circuit Emphasis

APS ....Active Pixel Sensor

ADC ....Analog to Digital Converter

SCR .... Switched Capacitor Resistor

TG.. Transmission Gate

R... Resistance

f... Frequency

C... Capacitance

CHAPTER 1: INTRODUCTION

CMOS Image Sensors

Imaging systems convert an image into a signal that is indicative of the image. There is a tremendous demand for integration of image sensors with circuits. These include circuits for driving the image sensor and for performing on-chip signal processing. This level of electronic integration results in good imaging performance with low noise. This led to the development of CMOS image sensors as CMOS is readily accessible and implementation of on-chip signal processing circuit is easy. This is the reason why CMOS image sensors are considered to be more popular when compared to charge coupled devices [1]. Image sensors consist of a pixel array where each pixel consists of a photosensitive diode and an amplifier. These photodiodes take a portion of an image and convert it into electrons. Pixels produce an electrical signal representing the image. Analog-to-digital converters are used to convert the measured analog output signal into an easily readable digital form. Advantages of the CMOS imager when compared to charge coupled devices are low cost, less power consumption and operation at low voltages and compatibility between the electronic devices integrated on-chip [2].

CMOS image sensors are classified into two types depending on the pixel implementation.

Passive Pixel Image Sensor

This topology of sensor consists of only one transistor, which acts as a switch and a photodiode as shown below in figure 1.1. When the switch is closed the voltage across

the photodiode charges the column bus capacitance. Passive pixel image sensors appear to be simple, but noise and scaling problems are some of the issues associated with them [3].
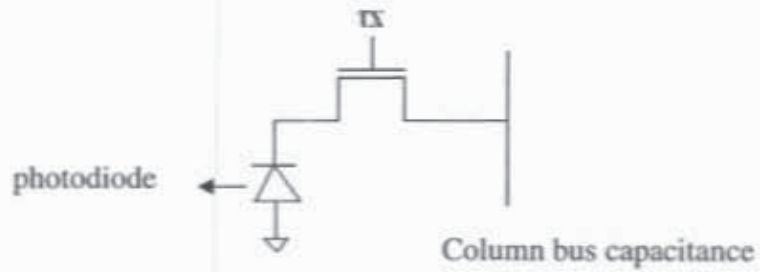
Figure 1.1 Passive pixel image sensor

Active Pixel Image Sensor

In comparison to passive pixel image sensors, the active pixel uses more than one transistor. Here the photodiode coverts the light intensity applied to it into a charge. This charge is then converted to a voltage and passed to the column bus capacitance [4].
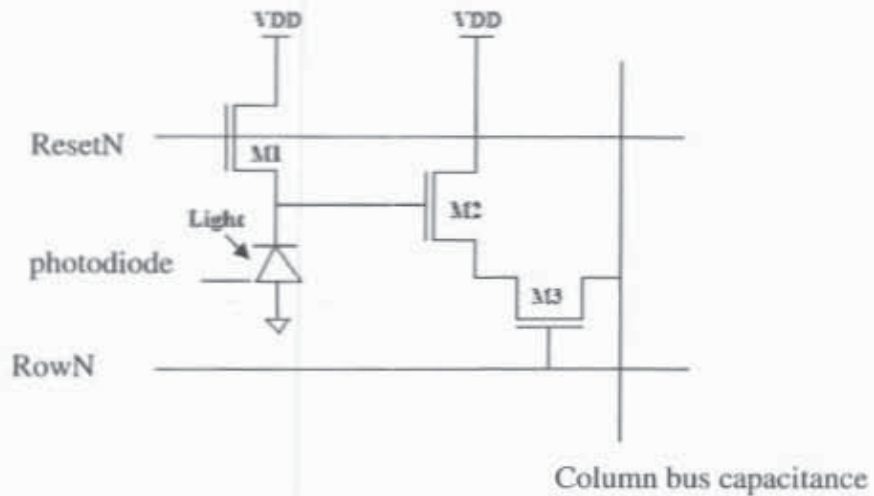
Figure 1.2 Active pixel image sensor

CMOS Image Sensor Architecture
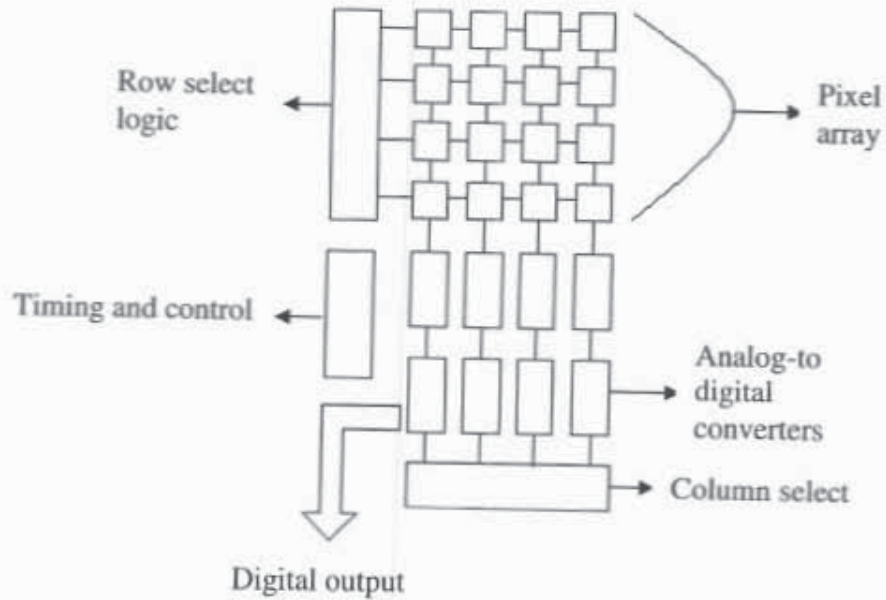
Figure 1.2 CMOS image sensor architecture

Typically CMOS image sensors consist of an array of pixels as shown in figure 1.2. In this architecture only one row is selected at a time using row select logic. The selected row of pixels is then connected to the APSs, which perform several functions such as charge integration, sample and hold, etc. Each column of the pixel has an analog-to-digital converter, which converts the analog output from the APS to digital output. This column select line is used to read the digital value representation out of ADC or the analog output from APS [3].

Analog-to-Digital Converter

Analog-to-digital converters play a very important role in imaging systems. These converters are used to convert the measured analog output signal into an easily readable digital form. The desired information regarding the signal is easily acquired from this digital signal. One of the drawbacks associated with these ADCs is that they limit the speed of the entire circuit. Therefore, selection of an ADC with high speed and good resolution is very important for the performance of the overall system. Various types of ADCs used in imaging systems are flash ADC, integrating ADC, sigma-delta ADC, and successive approximation ADC [5].

Flash ADCs are extremely fast when compared to all the ADC architectures mentioned above. But the main disadvantage associated with this architecture is complex analog design due to the use of 2^N-1 comparators connected in parallel. This parallel architecture leads to a mismatch between the comparators, an increase in power consumption, and an exponential increase in area with increase in number of bits. As a result this type of ADC is not typically used beyond 10 bits of resolution [5].

The successive-approximation ADC, also known as bit-weighing conversion, consists of S/H circuit, comparator, successive approximation register and DAC. The analog output of DAC is compared to the applied analog input signal to get the desired result [6]. The performance of this architecture lies between flash ADC and dual-slope ADC, which is discussed later in this section. This ADC is slower in speed but has high resolution when compared to the flash ADC. When compared to integrating ADC they are higher in speed and lower in resolution [7].

The basic principle of operation for the integrating ADC is that the digital output is obtained by integrating the input signal over a certain time period. Some types of integrating ADCs are single-slope ADC, dual-slope ADC and multi-slope ADC. Though the most widely used among these architectures is the dual-slope ADC [7].

The delta sigma modulator is the most commonly used ADC architecture in CMOS imager sensors because of its high resolution, use of low precision analog components, low cost and compatibility with component. A first order delta sigma modulator is shown in the following figure 1.4.
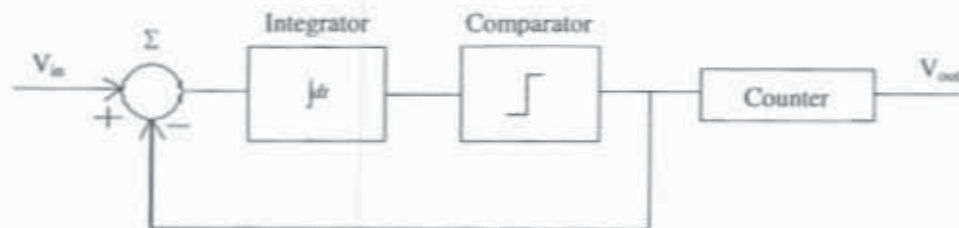
Figure 1.4 First order Delta Sigma Modulator

The first order delta sigma modulator consists of a summer, integrator, quantizer (comparator) and a counter. The counter performs digital filtering. The input signal V_{in} is fed into the integrator via a summing junction. The output of the integrator is fed into the comparator, which is a 1-bit quantizer. Then the output of the quantizer is fed to the digital filter and also to the summation junction where the difference between input and output signals is taken [8][9].

Two important techniques used by the DSM are oversampling and noise shaping. Oversampling reduces the quantization noise by sampling the input signal at a frequency greater than the nyquist frequency. Noise shaping distributes the quantization noise over a greater bandwidth so that it is low in the band of interest. The following graph in figure 1.5 shows the noise shaping of an oversampled first order DSM.
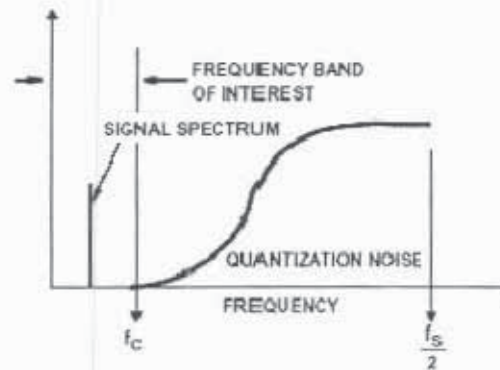
Figure 1.5 Noise shaping of oversampled 1st order DSM[9]

The purpose of the digital filter in DSM is to attenuate the signal and the quantization noise, which are present outside the bandwidth of interest in order to provide sharp cutoff at the bandwidth of interest. The following are the graphs that demonstrate the shape of quantization noise in the out-of-range bandwidth before filtering and after filtering [9].
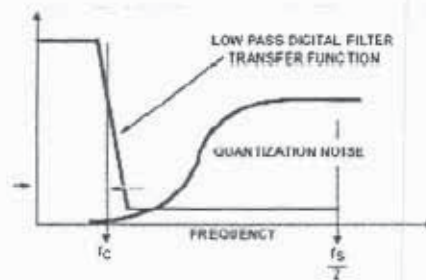
Figure 1.6 Before filtering [9]
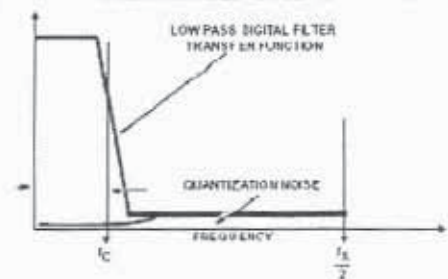
Figure 1.7 After filtering [9]

CHAPTER 2: SENSE AMPLIFIER DESIGN

Block Diagram

The block diagram of the delta sigma modulator is shown in figure 2.1. The reference voltage from the pixel is sampled onto the hold capacitor in the reference path using the S/H circuit and then the desired voltage is sampled in the signal path.
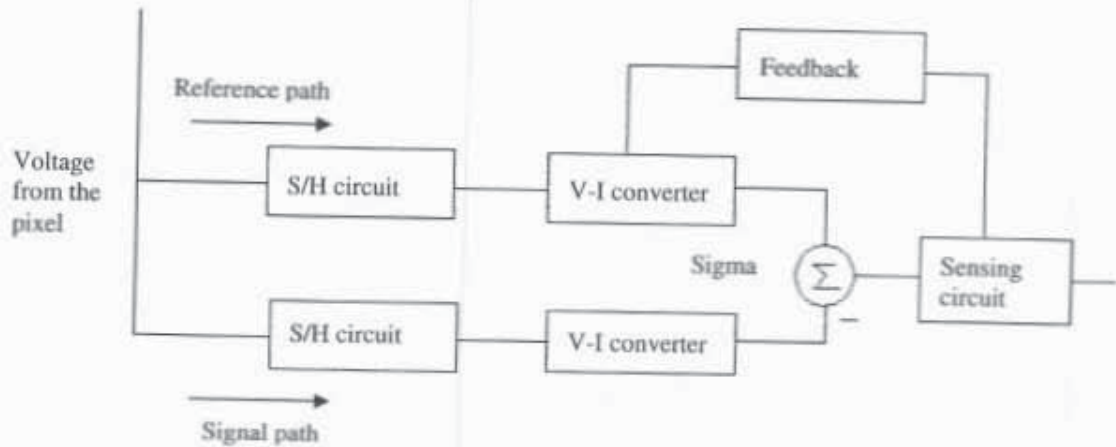
Figure 2.1. Block diagram of Delta Sigma Modulator

Reference voltage and signal voltage are converted into currents using voltage-current converters. The NMOS source follower acts as a voltage to current converter. The difference between these currents is fed into the sigma capacitor. The difference in the currents is taken in order to subtract out the variations in threshold voltage of the NMOS source follower from pixel to pixel.

The voltage from the sigma capacitor and the reference path voltage are compared using a sensing circuit. A clocked comparator with SR latch is used as the sensing circuit. Feedback path is enabled or disabled depending on the output of the sensing circuit.

A switched capacitor circuit is used to implement a feedback circuit. The feedback circuit is enabled when the current in the reference path is different from the current in the signal path. And then the feedback circuit tries to equalize currents in both the paths. The desired signal is obtained by comparing the currents in the reference path and the signal path and by averaging the number of times the feedback path is enabled.

Sample and Hold

One of the basic S/H circuits is shown in the figure 2.2. When the clk signal goes high M1 is on and the input signal, V_{in} charges the hold capacitor (C_h). When the clk signal goes low M1 is off, however, the capacitor remains charged with the same voltage level as the input signal. The reason the capacitor is called a hold capacitor is because it holds the charge even after the switch is closed. The disadvantage of using a single NMOS or PMOS as a switch is the presence of charge injection and clock feedthrough, which results in non-linearity and reduction in resolution.
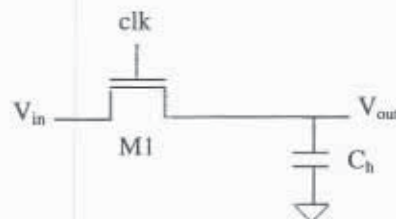
Figure 2.2. Basic S/H circuit

Charge Injection:

When the clk signal goes high M1 is on and a channel consisting of mobile

charges is formed under the gate oxide and the capacitor is charged with the input

voltage. When M1 is off, the charge under the gate oxide is injected onto either side of

the MOSFET. This results in some of the charge being injected towards the input signal

and some towards the hold capacitor. Because of this injected charge, the voltage

sampled onto the hold capacitor changes [4].
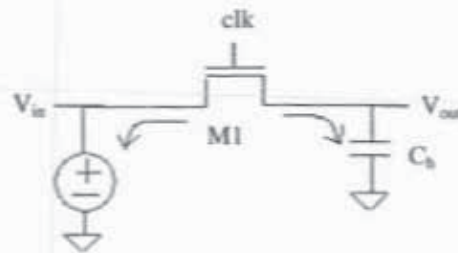
Figure 2.3 Circuit showing charge injection

Charge Feedthrough:

As figure 2.4 illustrates when M1 is on, the clk signal is fed through the C_{gs} and

C_{gd}, which has no effect on the output voltage. The capacitor, C_h, is charged with the

input voltage.
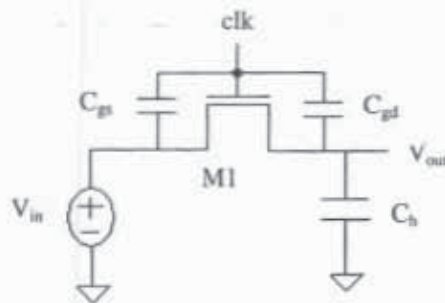
Figure 2.4. Circuit showing clock feedthrough

When M1 is off, a voltage divider is formed between the C_{gs}/C_{gd} and C_h. Clk signal is fed through this voltage divider resulting in a change in voltage across the capacitor [4].

Charge injection and clock feedthrough can be avoided by using the transmission gate (TG) rather a single NMOS or PMOS switch. The advantages of using TG as a switch are (i) full logic level swing; it can pass logic high and logic low without a threshold voltage drop, (ii) lower resistance because the NMOS and PMOS are connected in parallel, and (iii) the charge released from both NMOS and PMOS devices are equal and opposite tending to cancel each other. TG has a larger layout area when compared to single NMOS and PMOS devices, and requires two clk signals. Figure 2.5 shows a simple sample and a hold circuit implemented using TG.
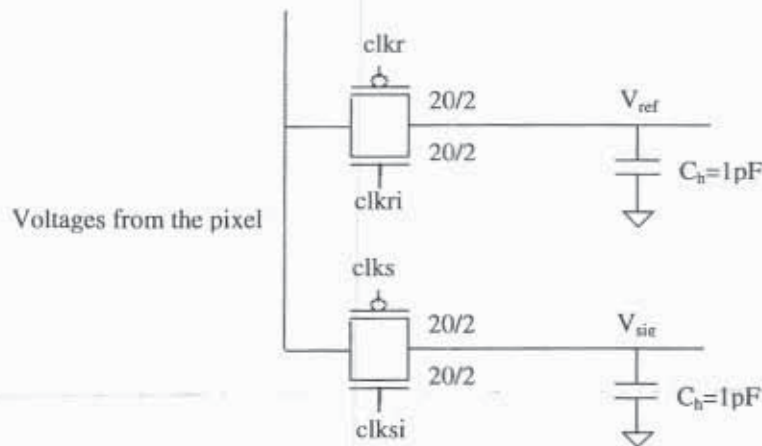
Figure 2.5. Sample and hold circuit with TG

The simulation below shows that TG1 is turned on first, resulting in sampling the reference voltage, and then TG2 is turned on sampling the signal voltage on the hold capacitor.
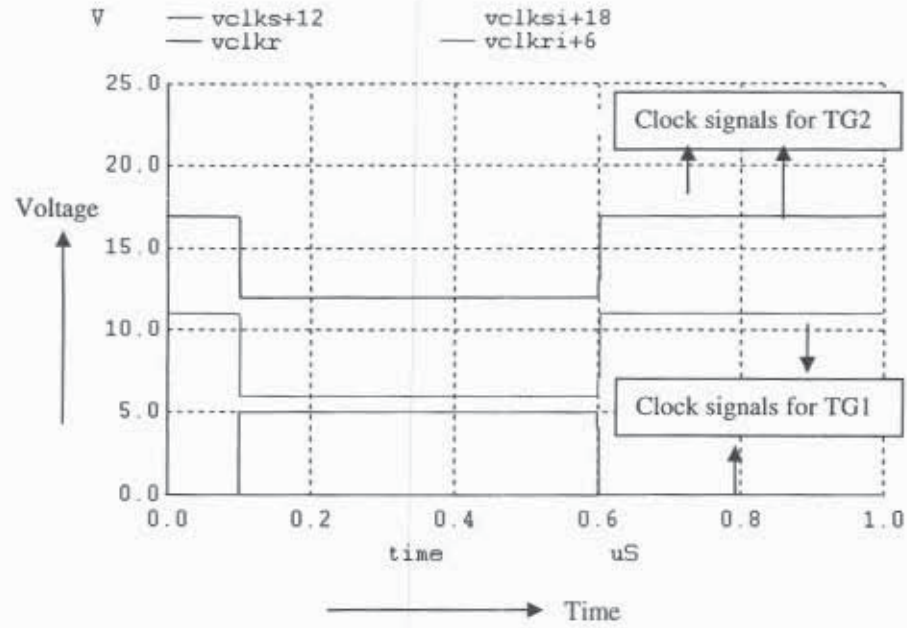
Figure 2.6. Showing clock signal used to turn on TGs

From the simulation below, V_{ref} is 2.5V is sampled first, and V_{sig} is 2.2V is sampled after a delay of 0.1u. The simulation shows that the voltage on the hold capacitor remains at 2.5V or 2.2V even after the TGs are turned off.
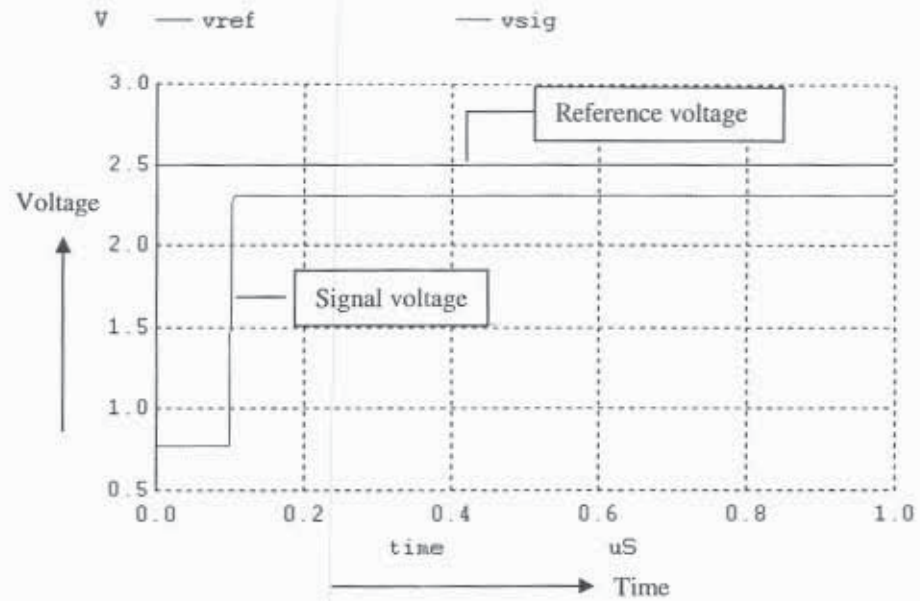
Figure 2.7. Showing reference voltage and signal voltage

Voltage to Current Converter

NMOS source followers perform voltage to current conversion. The reference voltage V_{ref} is sampled first and converted into reference current I_{ref}, and then the signal voltage V_{sig} is sampled and converted into signal current I_{sig} as shown in figure 2.8.
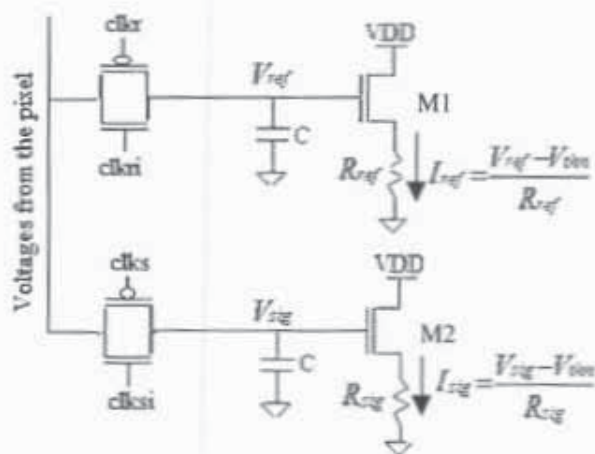
Figure 2.8. Voltage to current conversion

Some of the disadvantages of using the above topology are (i) the value of the resistor can vary with temperature, process characteristics, etc., and (ii) large layout area. In order to overcome these disadvantages a switched capacitor resistor is used instead of a resistor. Figure 2.9 shows a voltage to current converter implemented using SCR. A PMOS device with source, drain and body connected to VDD is used as a switched capacitor.
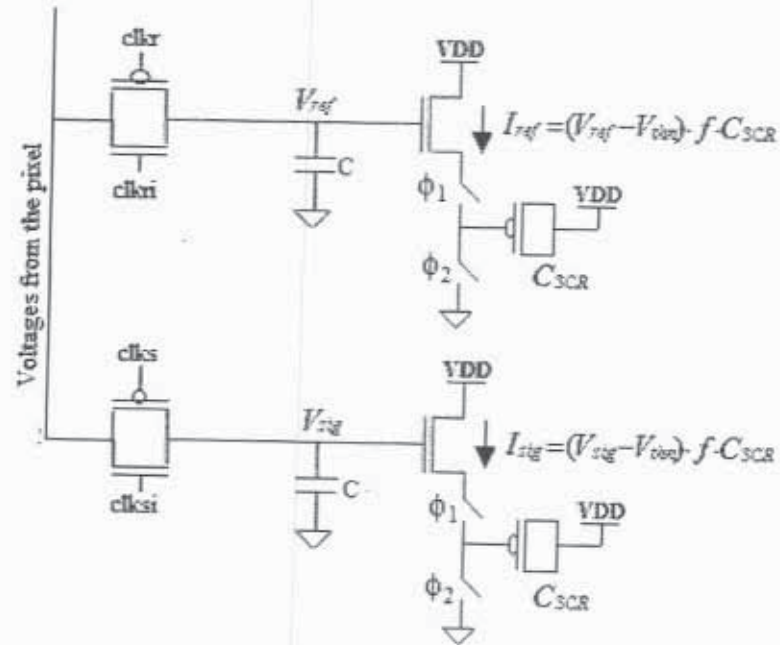
Figure 2.9. Voltage to current conversion using SCR

Feedback Circuit

The feedback circuit is implemented using switched capacitor resistor as shown below.
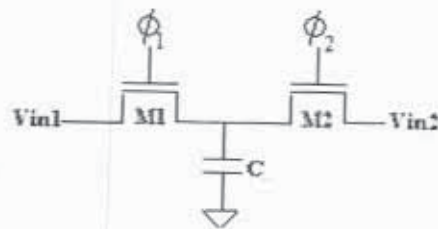
Figure 2.10. SCR implemented using NMOS device

ϕ_1 and ϕ_2 are non-overlapping clock signals, they are never high at the same time for NMOS and never low at the same time for PMOS. If $V_{in1} > V_{in2}$ and ϕ_1 is high then M1 is on and the capacitor is charged to voltage V_{in1} [4].

Therefore the charge stored on the C is given as,

$$Q_1 = C \cdot V_{in1} \qquad \qquad \text{...(2.1)}$$

When ϕ_2 is high M2 is on and the capacitor is discharged to voltage V_{in2}.

Therefore the charge stored on the C is given as,

$$Q_2 = C \cdot V_{in2} \qquad \qquad \text{...(2.2)}$$

Difference between the charges Q_1 and Q_2 is transferred between V_{in1} and V_{in2} during every clock interval.

$$Q_1 - Q_2 = C \cdot (V_{in1} - V_{in2}) \qquad \qquad \text{...(2.3)}$$

Average current transferred is given by,

$$I_{avg} = \frac{C \cdot (V_{in1} - V_{in2})}{T} \qquad \qquad \text{...(2.4)}$$

$$I_{avg} = \frac{(V_{in1} - V_{in2})}{R} \qquad \qquad \text{...(2.5)}$$

Equating (2.4) and (2.5),

$$\frac{C \cdot (V_{in1} - V_{in2})}{T} = \frac{(V_{in1} - V_{in2})}{R} \qquad \qquad \text{...(2.6)}$$

$$R = \frac{T}{C} \text{ where } T = \frac{1}{f} \qquad \qquad \text{...(2.7)}$$

Therefore,

$$R = \frac{1}{f \cdot C} \qquad \qquad \text{...(2.8)}$$

The resistor value depends on the clock frequency and on the capacitance so SCR can be used for realizing large resistors like more than $M\Omega$ by simply adjusting the clock frequency. The advantage of using a switched capacitor circuit is that it occupies a

smaller layout area when compared to the resistor. The disadvantage of using a switched

capacitor circuit is that the circuit is complicated because of the usage of two clock

signals [4].
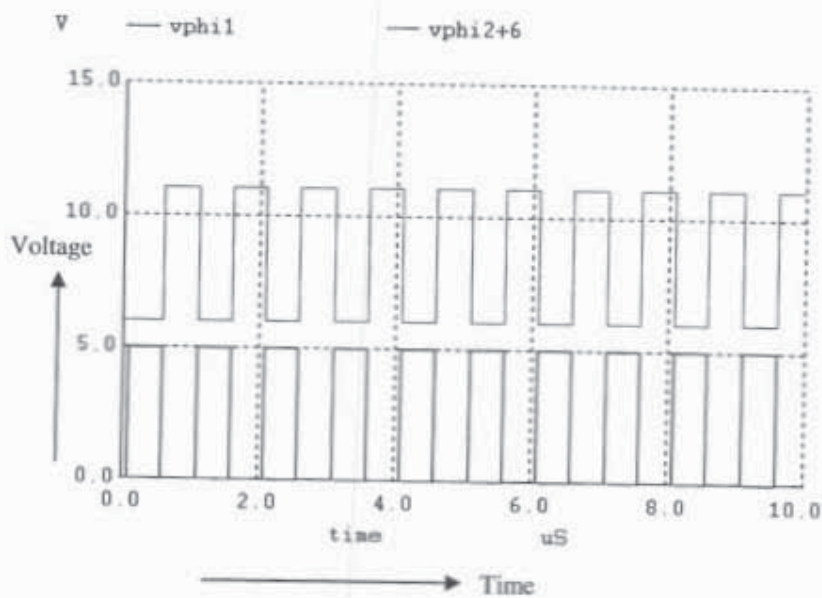
Figure 2.11. Showing non-overlapping clocks
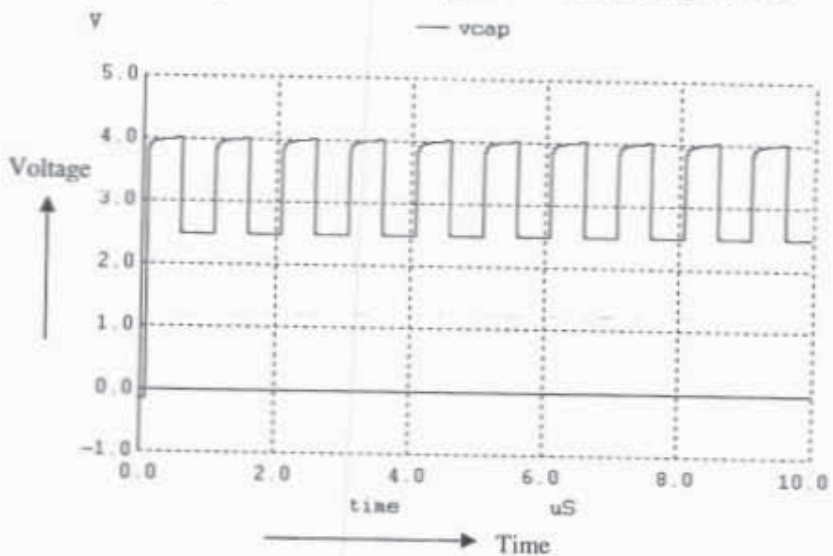
Figure 2.12. Showing the voltage across the capacitor using NMOS switch

Figure 2.12 show that the capacitor is not completely charged to 5V and this is because of the presence of body effect in NMOS. For PMOS devices the body effect can be eliminated because they can be fabricated in their own wells and have separate bodies. Figure 2.13 shows SCR implemented using PMOS switches. Capacitor charges all the way to 5V.
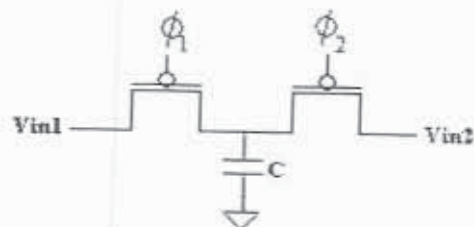
Figure 2.13 SCR implemented using PMOS device
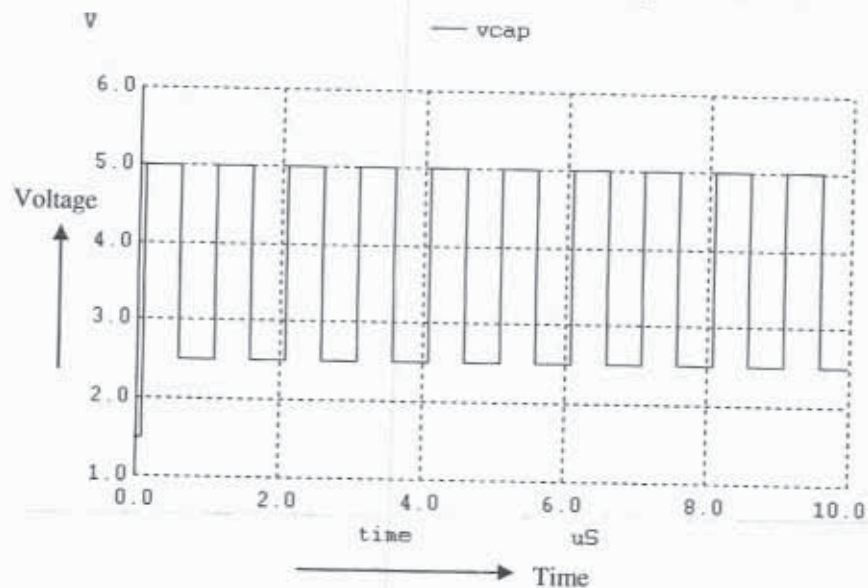
Figure 2.14. Showing voltage across the capacitor using PMOS switch

Input Circuit of DSM
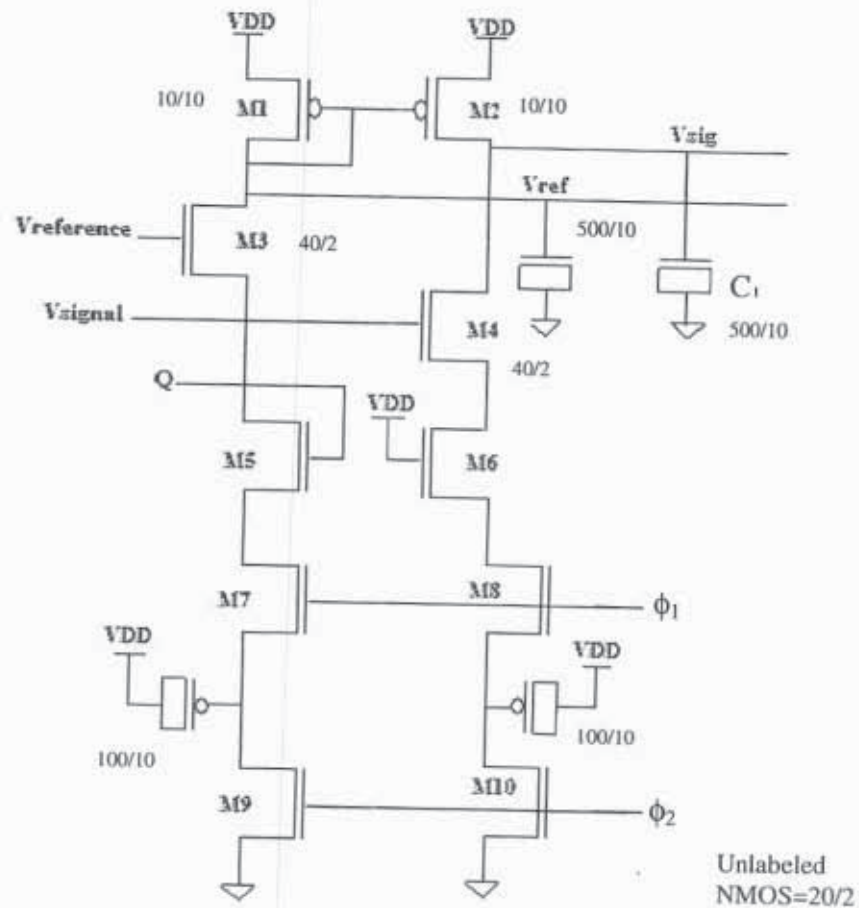
Figure 2.15 DSM input circuit

NMOS common drain amplifier is used to perform the voltage to current conversion. M3 and M4 are made wider so that their V_{gs} is close to V_{thn}. When the $V_{reference}$ is greater than V_{signal}, the current flowing through M3 increases because the gate-source voltage increases, but the current flowing in M4 decreases because gate-source voltage is less. Because of the PMOS current mirror the current flowing in M1 (reference path) is mirrored onto the other side (M2). So the difference between the currents flowing in the reference path and the signal path charges the capacitor C_1.
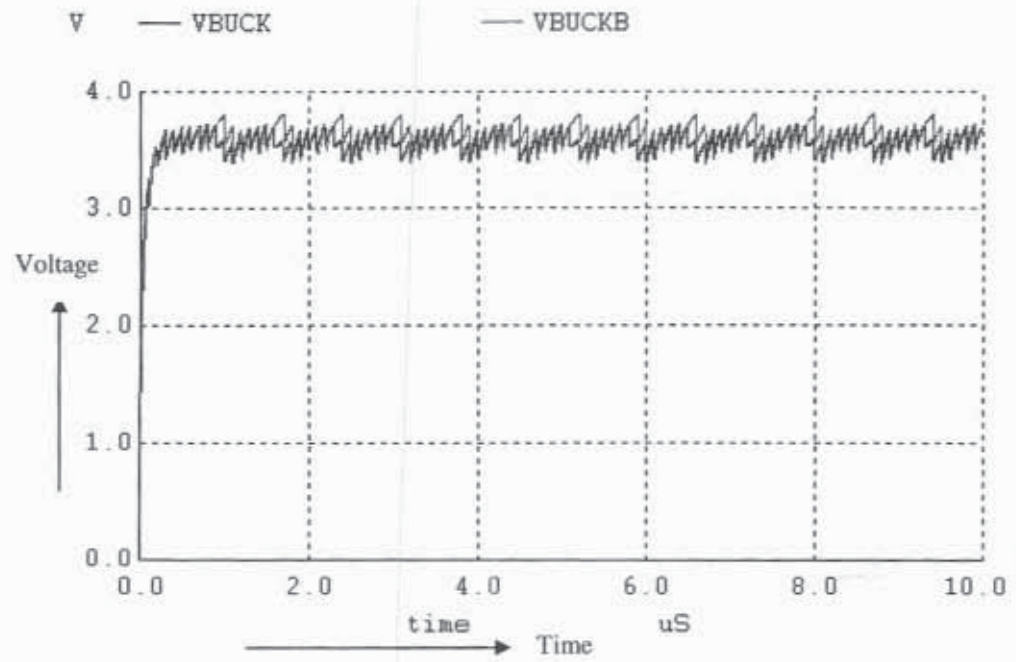
Figure 2.16 Simulation showing inputs to the comparator

Figure 2.16 shows that voltages V_{ref} and V_{sig} ideally follow each other because of the feedback circuit.

Comparator

A clocked comparator with SR latch is used as the sensing circuit as shown below.
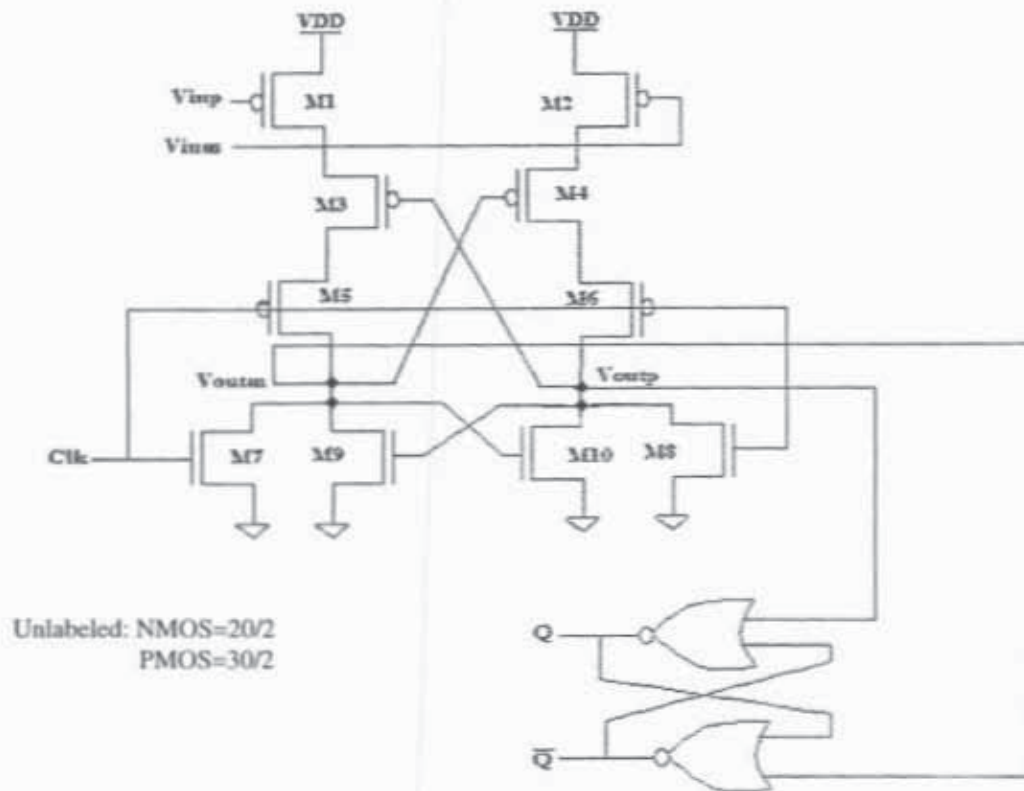
Figure 2.17 Comparator with SR latch

When clk is high, M5 and M6 are turned off whereas M7 and M8 are on causing both the outputs V_{outp} and V_{outm} to go low and the outputs of the SR latch to remain unchanged. When clk is high there is no path from VDD to ground. Inputs V_{inm} and V_{inp} are compared when clk goes low. If $V_{inp} > V_{inm}$ when clk is low the current flowing M1 is less when compared to the current flowing in M2 because V_{sg} of M1 is less than V_{sg} of M2. M5 and M6 are on when clk is low whereas M7 and M8 are off causing V_{outp} to go

to high and Q to go low. This increases the gate voltage of M9 causing it to turn on and

pulls V_{outm} low and $\overline{Q}$ high. The operation of the figure 2.17 is shown below. V_{inp} is at

2.5V and V_{inm} is at 2V. When clk (phi2) is high both the outputs are low but when clk

(phi2) is low and $V_{inp}>V_{inm}$, V_{outp} is high and V_{outm} is low.
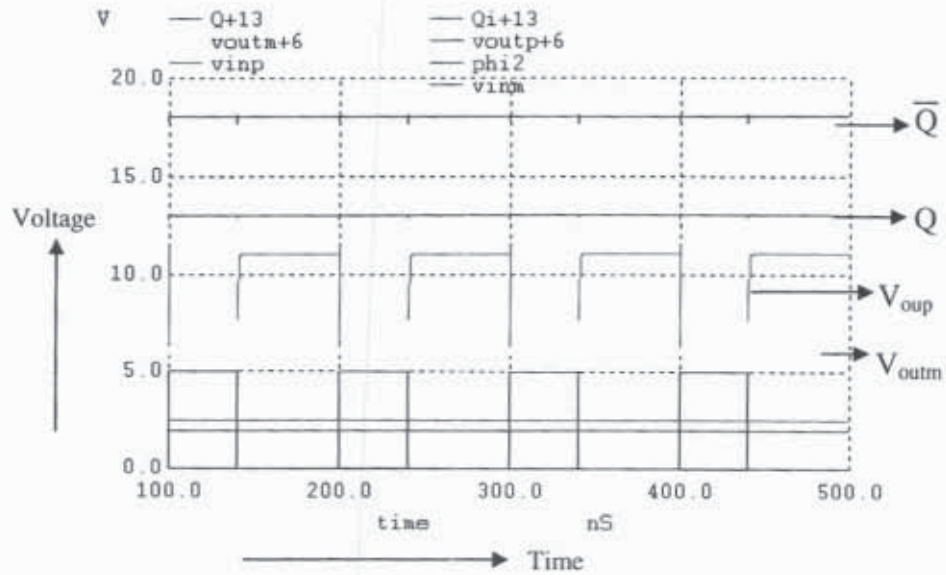
Figure 2.18 Showing the operation of the comparator
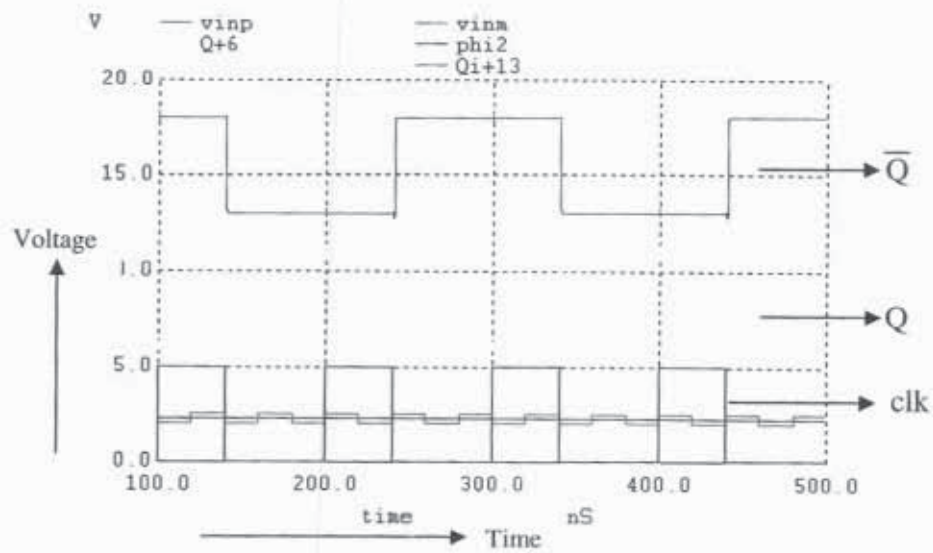
Figure 2.19. Showing the operation of figure 2.16 with Vinp swept from 2V to 2.5V

Delta Sigma Modulator
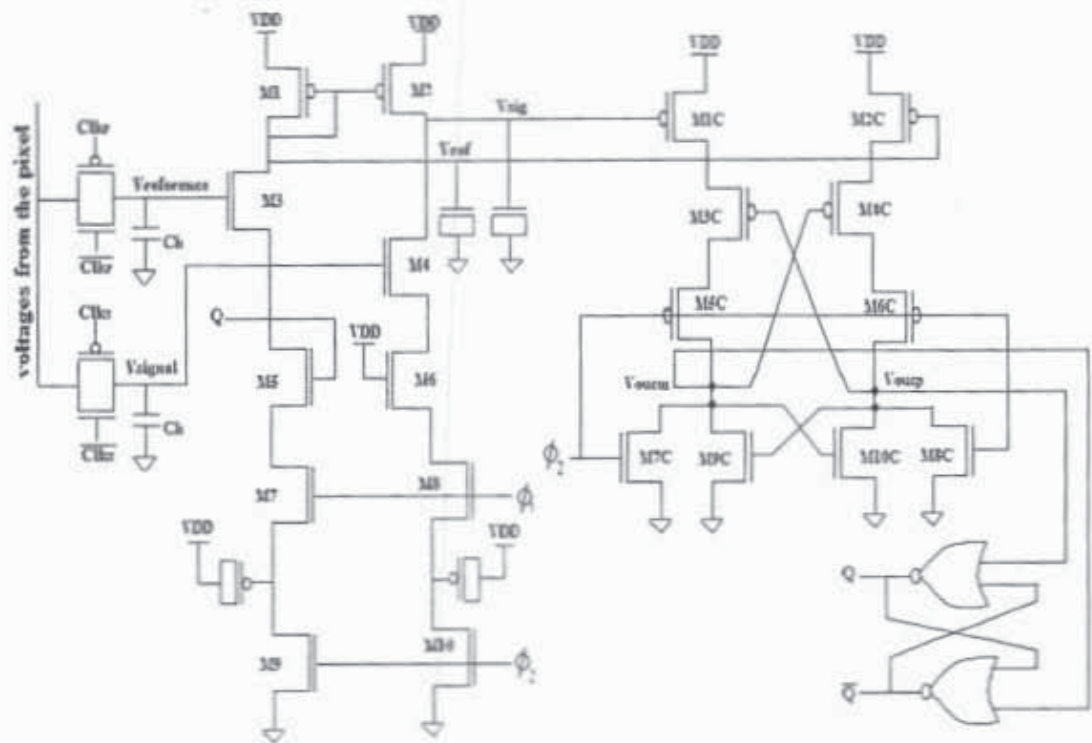
Figure 2.20 Delta Sigma Modulator

Voltages from the pixels are sampled onto the hold capacitors. First the reference

voltage is sampled followed by signal voltage. Voltages are converted into currents using

NMOS source follower. If $V_{reference} > V_{signal}$ then the current flowing in reference path

(M3) is more than the current flowing signal path (M4). The current flowing is M1 is

mirrored onto M2 and the difference between reference current and signal current is used

to charge the capacitor on node V_{sig}. Capacitor on node V_{ref} is at lower voltage when

compared to V_{sig}. When ϕ_2 is low V_{outp} will go high and V_{outm} will go low causing Q to

go low and $\overline{Q}$ to high. When Q is low the feedback path is disabled decreasing the current

is reference path and increasing the voltage on node V_{ref} until the currents in both paths are equal.

$\overline{Q}$ is given to the up-counter, which counts the number times the feedback path is enabled. The desired signal from the column voltage can be determined by comparing the reference current to signal current and by averaging the number of times the feedback path is enabled to equalize the currents in both the paths.

CHAPTER 3: DSM DESIGN FOR OFFSETS

No Offset

Figure 3.2 is the simulation of the DSM circuit shown in figure 3.1 without offset. V_{ref}=2.5V and V_{sig}=2.3V.
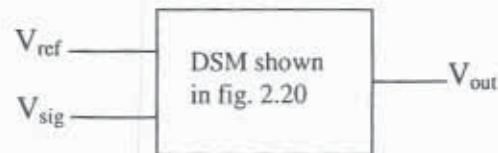
Figure 3.1 Block diagram of DSM without offset

Start sensing at 2us
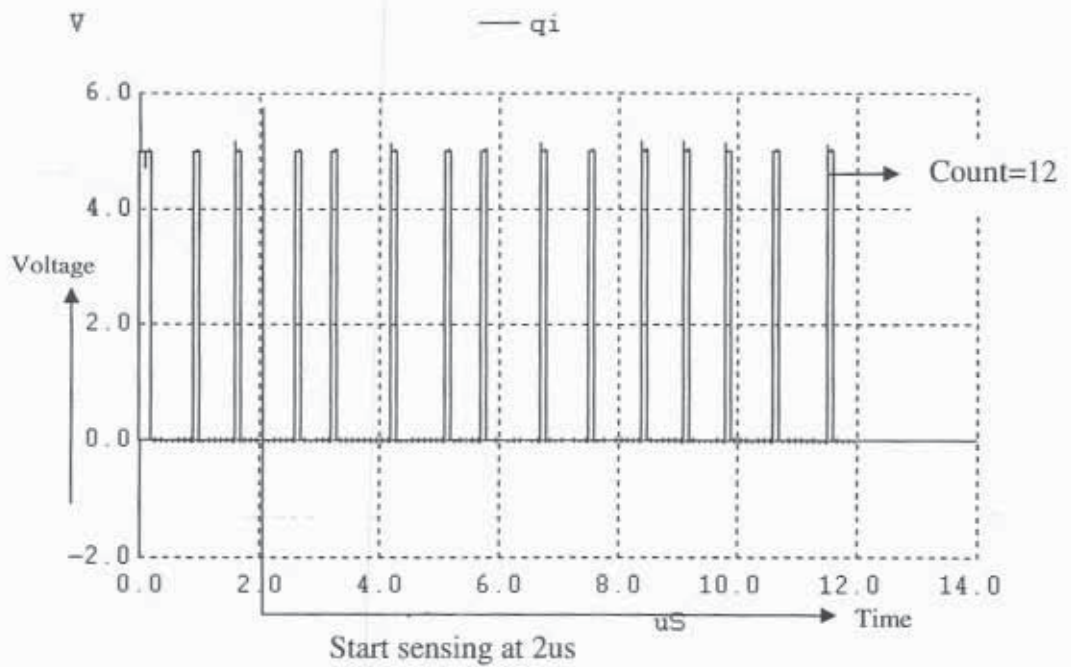
Figure 3.2 Simulation showing the count of DSM without offset

Inverters
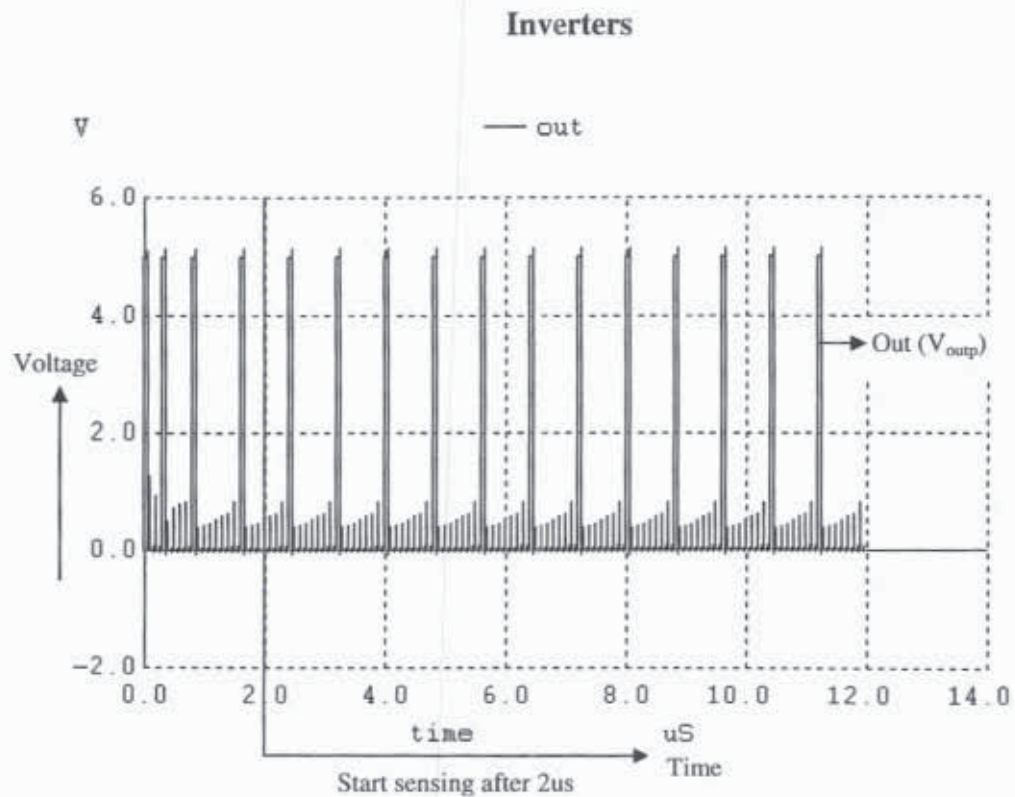
Figure 3.3 Output of DSM circuit shown in figure 2.20

Figure 3.3 shows the output of the DSM circuit shown in figure 2.20 V_{outp} (out), which is given to the input of the counter. When V_{outp} is fed to the counter there is a possibility that the counter will count the glitches shown in the above simulation, which gives an incorrect count. In order to avoid this error inverters are used at the output of the DSM as shown in figure 3.4.
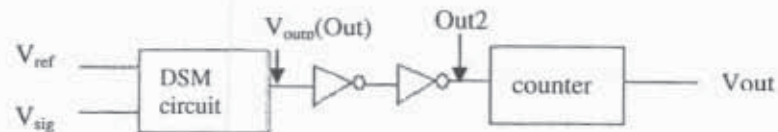
Figure 3.4 DSM circuit with inverters and a counter
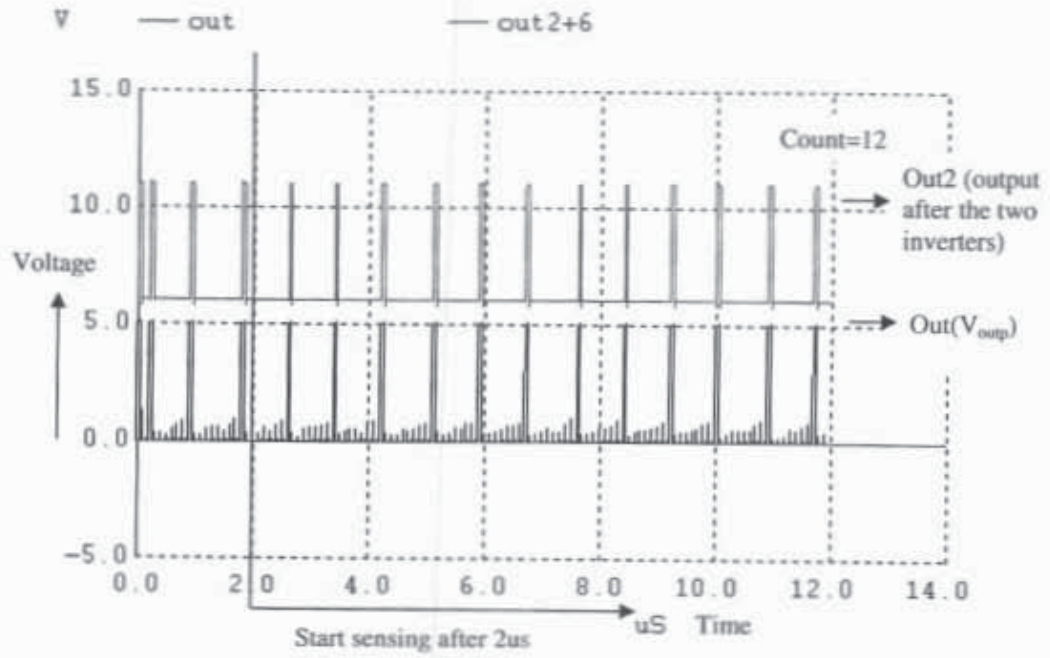
Figure 3.5 Simulation showing the output before and after inverters

Counter

In this project an edge-triggered D-FF is used as a counter. The output of the D-FF changes at the rising edge of the clock.
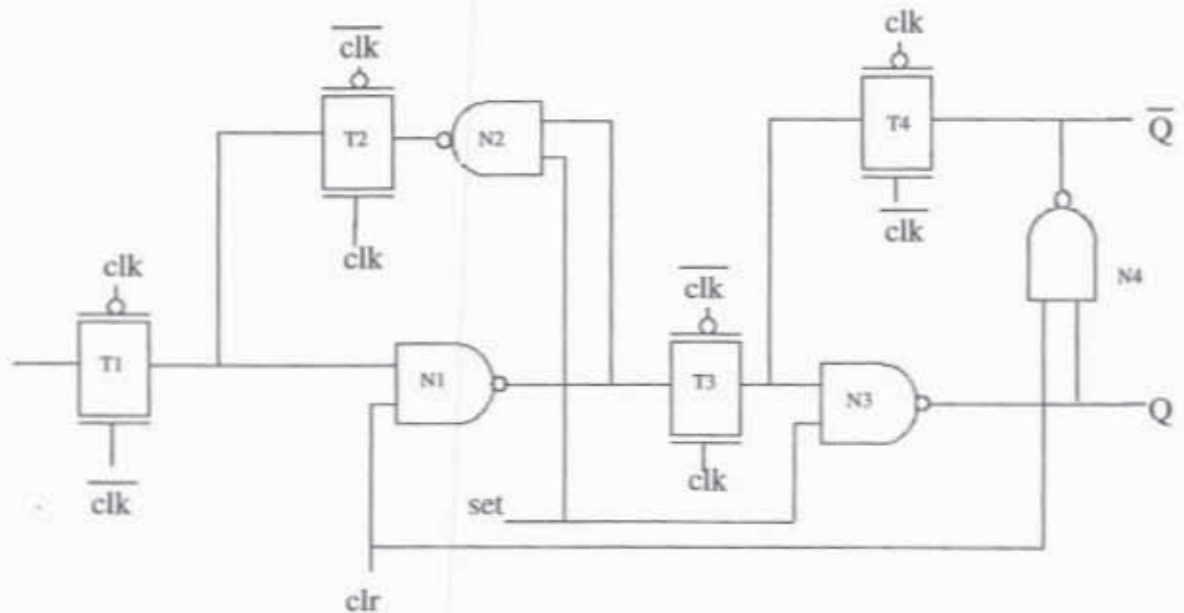
Figure 3.6 D-FilpFlop

When clk is low T1 and T4 are on. T2 and T3 are off. The D input is passed to the node 1. When clr is low the output of N1 is always high. Now when clk goes high T1 and T4 are off while T2 and T3 are on. If set is high Q=0 and $\overline{Q}$=1. When clr and set both go high and input D is high then Q=1 and $\overline{Q}$=0 and if input D is low then Q=0 and $\overline{Q}$=1. When clr is high and set is low then Q=1 and $\overline{Q}$=0 for both high or low on input D. When clr and set both go low then both Q and $\overline{Q}$ are high. Figure 3.7 shows the simulation, which demonstrates the working of D-FF.
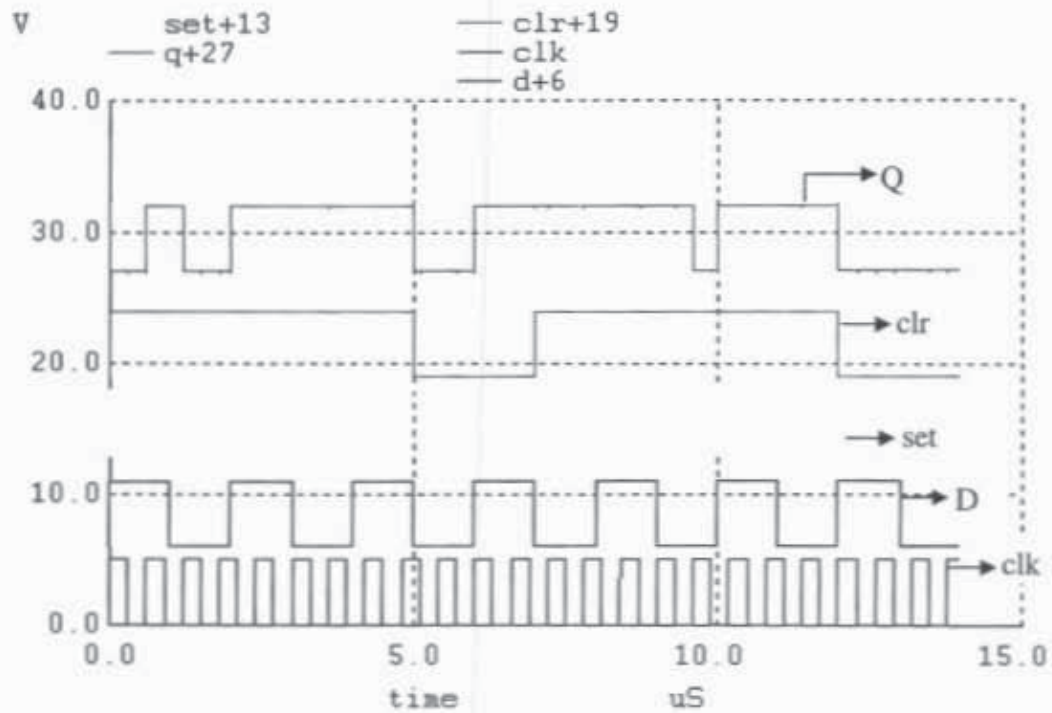
Figure 3.7 Simulation showing the working of D-FF

Figure 3.8 shows how the counters are connected to form an architecture called ripple-up counter. This project uses 10-bit counter where 10 counters are connected to each other as shown in the below architecture. Output $\overline{Q}$ from the previous counter is fed into the input D of the same counter and also to the clk of the next counter. The count generated by each counter is given by the output Q. The output b_0 of the first counter represents $(2^0.x_0)$ where x_0 is either high or low. Similar b_1 is $(2^1.x_1)$ and finally b_9 is $(2^2.x_9)$.
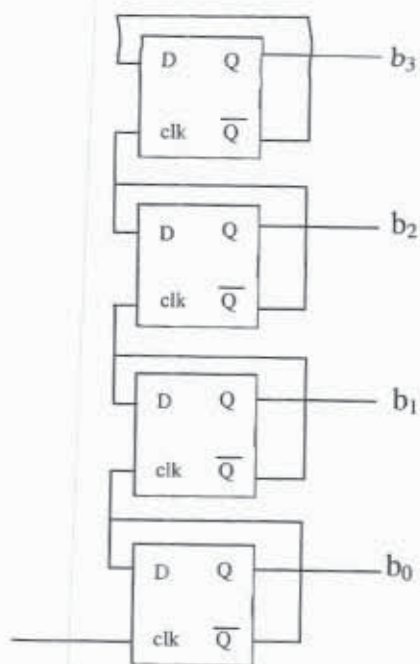
Figure 3.8 Ripple up counter

$$Count=(2^0 \cdot 0)+(2^1 \cdot 0)+(2^2 \cdot 1)+(2^3 \cdot 1)=12$$
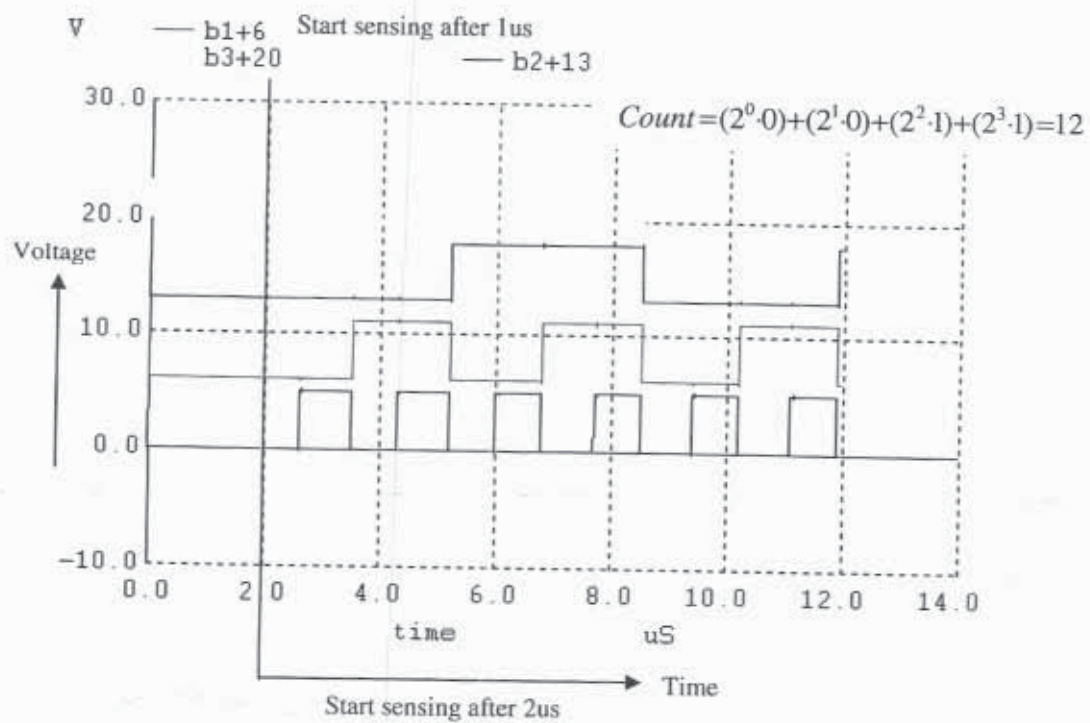
Figure 3.9 Simulation showing the output of the counter

With Offset

In the DSM sensing circuit there are two separate paths one for reference voltage and the other for signal voltage. There is a possibility that there can be a mismatch between these paths like threshold voltage mismatch, mismatch in the resistance, etc. Because of this mismatch the image will have vertical streaks, which will reduce the quality of the image. Figure 3.10 shows the block diagram of DSM circuit with an offset voltage. This offset voltage is just a model of the difference between the reference path and the signal path. This voltage can be either positive or negative [4].
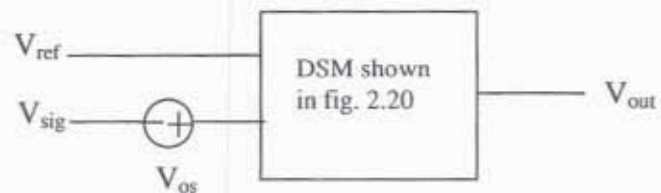
Figure 3.10 Block diagram of DSM with offset
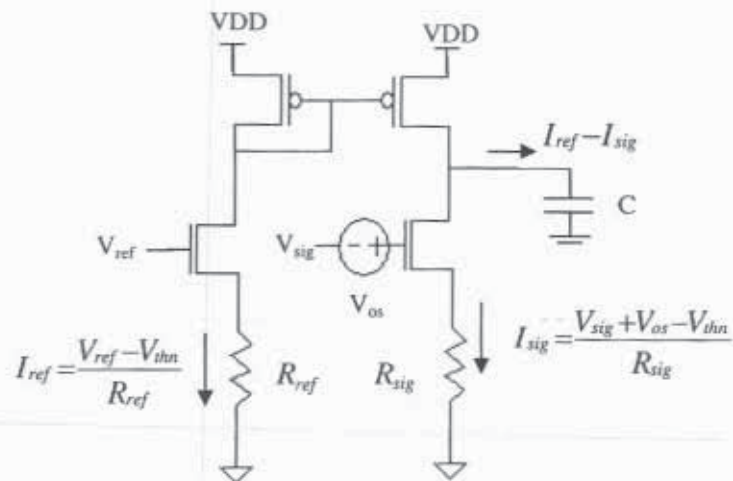
Figure 3.11 Voltage to current conversion

Figure 3.11 shows the voltage to current conversion in the DSM circuit with an offset voltage connected in series with the gate of the NMOS in signal path.

Current flowing in the reference path is,

$$I_{ref} = \frac{V_{ref} - V_{thn}}{R_{ref}} \qquad \text{...(3.1)}$$

Let $V_{ref.shift} = V_{ref} - V_{thn}$ where V_{ref}=reference voltage and V_{thn}=threshold voltage

Current flowing in the signal path,

$$I_{sig} = \frac{V_{sig} + V_{os} - V_{thn}}{R_{sig}} \qquad \text{...(3.2)}$$

Let $V_{sig.shift} = V_{sig} - V_{thn}$ where V_{sig}=signal voltage

Over a period of time the charge on the capacitor C remains on average a constant. Therefore,

$$I_{ref} = I_{sig} \qquad \text{...(3.3)}$$

$$\frac{V_{ref.shift}}{R_{ref}} = \frac{V_{sig.shift} + V_{os}}{R_{sig}} \qquad \text{...(3.4)}$$

Where $R_{ref} = \dfrac{1}{f \cdot C \dfrac{(N-M)}{N}}$ and $R_{sig} = \dfrac{1}{f \cdot C}$

$$\frac{V_{ref.shift}}{\dfrac{1}{f \cdot C \dfrac{(N-M)}{N}}} = \frac{V_{sig.shift} + V_{os}}{\dfrac{1}{f \cdot C}} \qquad \text{...(3.5)}$$

$$V_{sig.shift} = V_{ref.shift} \frac{(N-M)}{N} - V_{os} \qquad \text{...(3.6)}$$

Figure 3.13 shows the output of the DSM after the inverters.
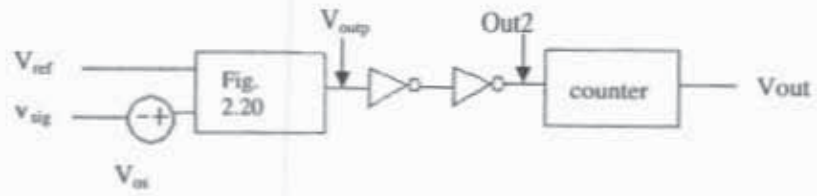
Figure 3.12 DSM circuit with inverters and counter
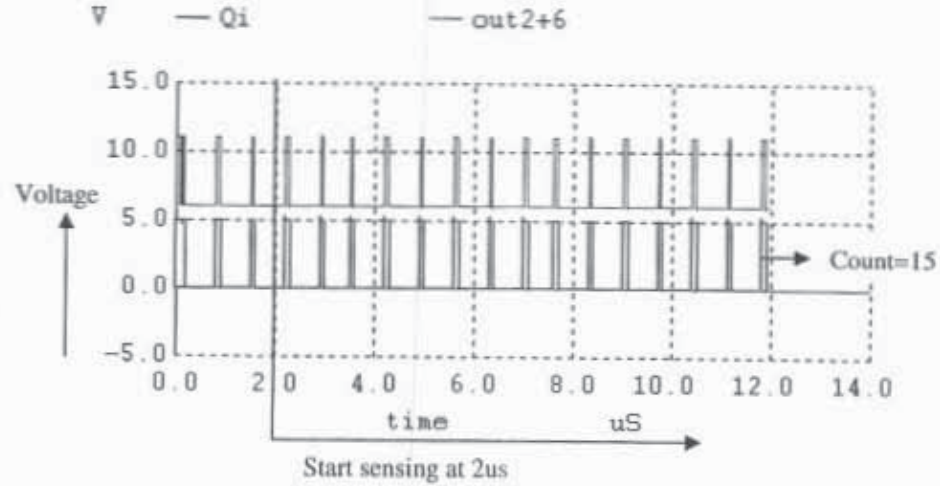
Figure 3.13 Simulation showing the output of DSM with V_{os}= -50mV
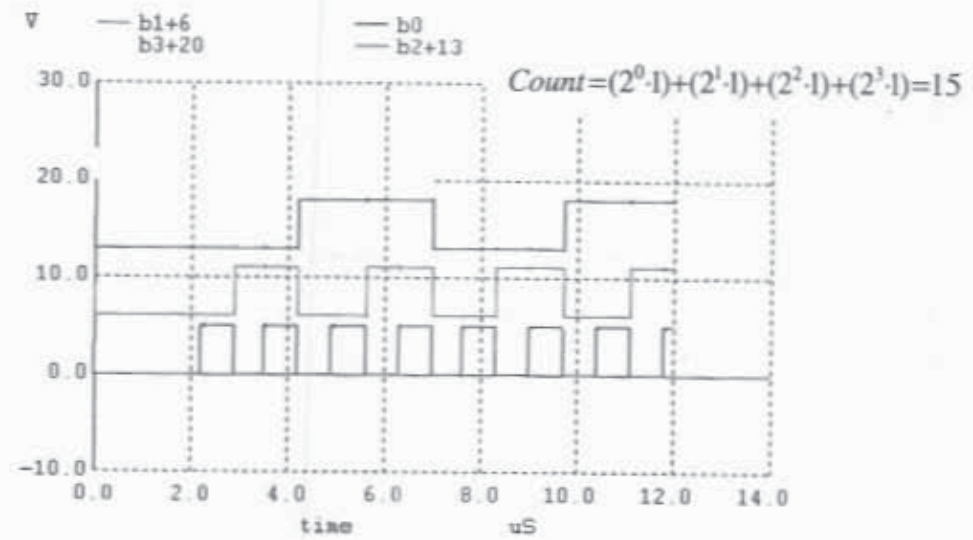
Figure 3.14 Showing the output of the counter in figure 3.12

Eliminating Offset

In order to reduce the effects of mismatch the inputs of the DSM are switched halfway through the sense time i.e during first half of the sense time when S is high the offset in on the signal voltage path and during the other half of sense time when S is low the offset is on the reference voltage path as shown in figure 3.15. Doing this will average out the mismatch ideally to zero [4]. The topology shown in figure 3.15 will work only if the difference between V_r and V_i is greater than V_{os}.
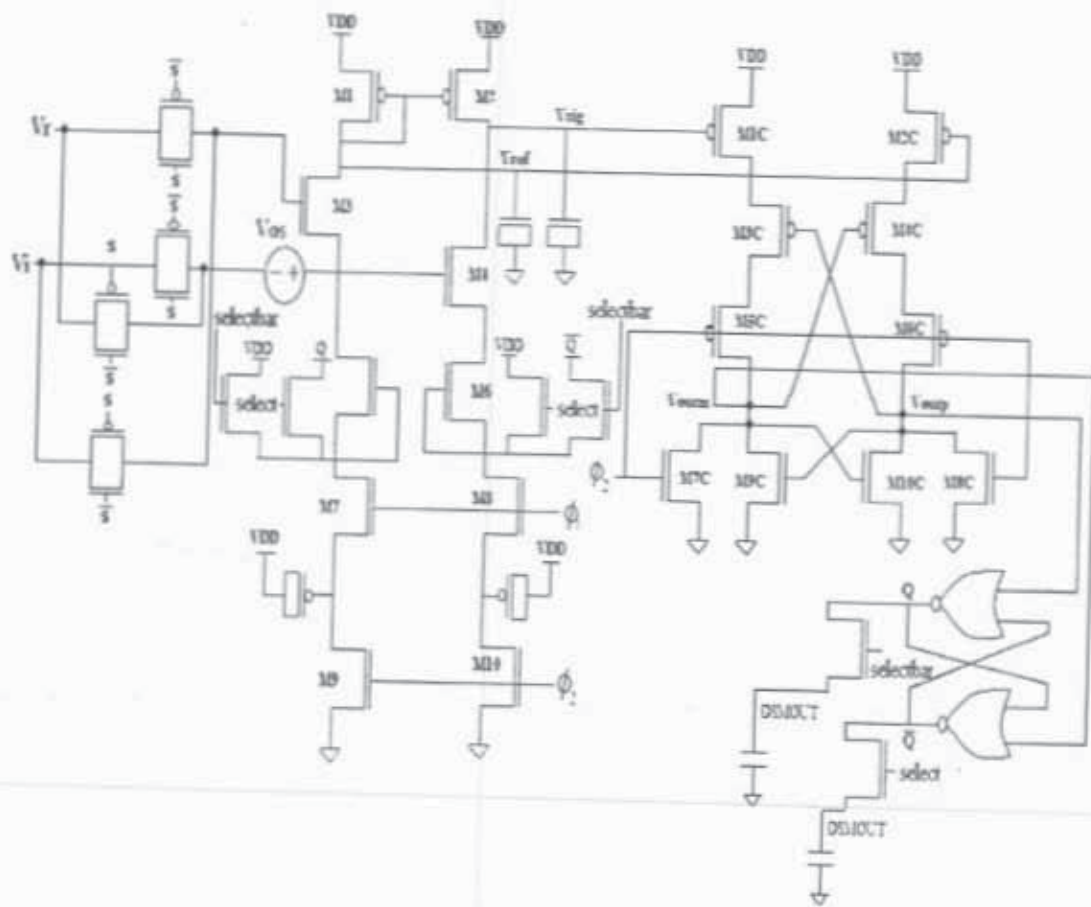
Figure 3.15 Switching the inputs halfway through the sense time

When the input voltages are switched the feedback circuit must also be switched.
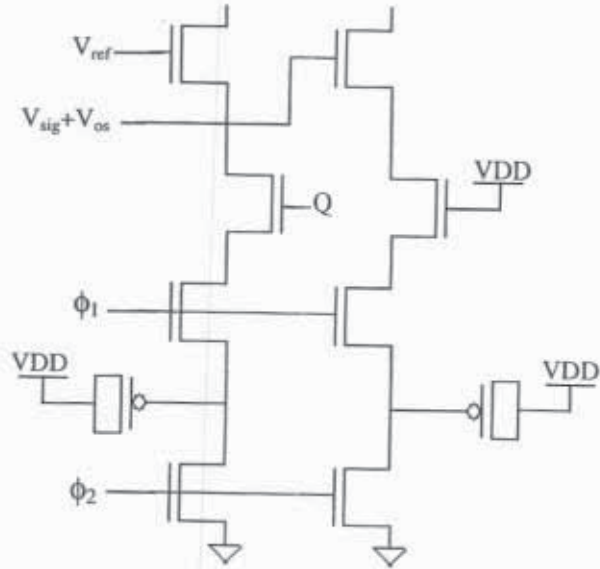
Figure 3.16 Feedback Circuit when S is high
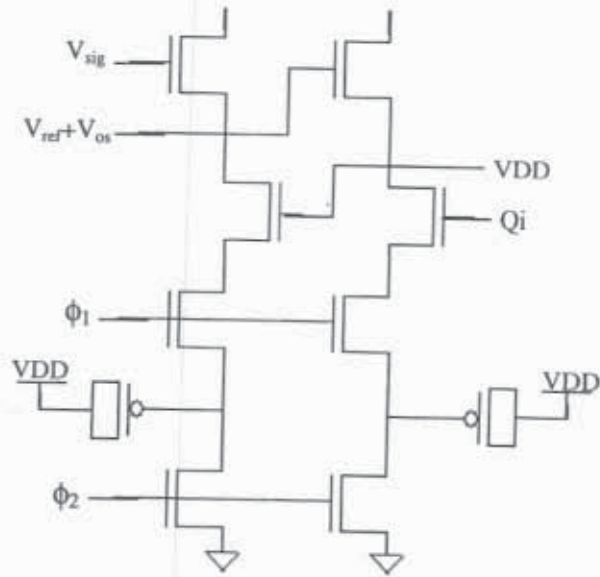
Figure 3.17 Feedback Circuit when S is low

Figures 3.16 and 3.17 show that the feedback circuit is always applied to the reference path even though the feedback circuit is switched.

During the first half of the sense operation the schematic of DSM is as shown below.
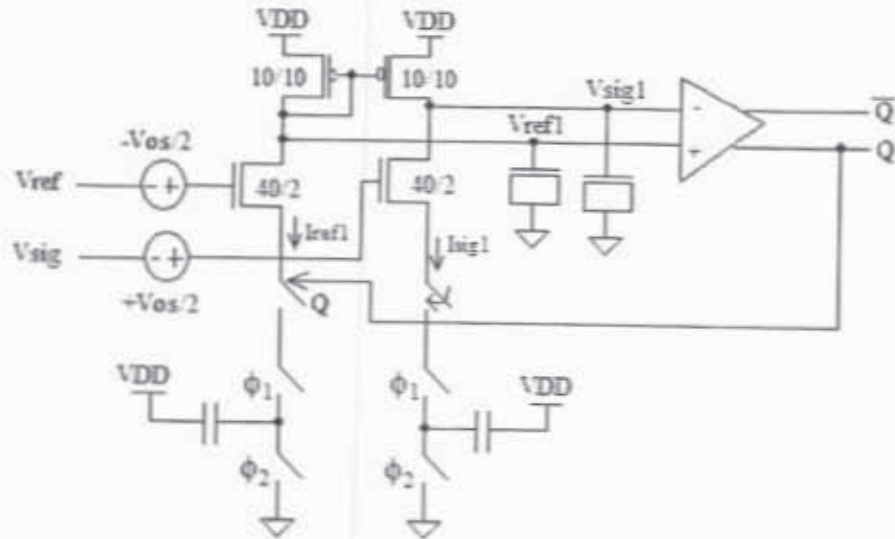
Figure 3.18 Voltage to current conversion during first half of the sense time

Current flowing in the reference path is,

$$I_{ref1} = \frac{V_{ref} - \frac{V_{os}}{2} - V_{thn}}{R_{ref}} \qquad \ldots(3.7)$$

Let $V_{ref.shift} = V_{ref} - V_{thn}$

$$I_{ref1} = \frac{2V_{ref.shift} - V_{os}}{2R_{ref}} \qquad \ldots(3.8)$$

Current flowing in the signal path is,

$$I_{sig1} = \frac{V_{sig} + \frac{V_{os}}{2} - V_{thn}}{R_{sig}} \qquad \ldots(3.9)$$

Let $V_{sig,shift} = V_{sig} - V_{thn}$

$$I_{sig1} = \frac{2V_{sig,shift} + V_{os}}{2R_{sig}}$$ ...(3.10)

Where $R_{ref} = \dfrac{1}{f \cdot C \cdot \dfrac{(N-M)}{N}}$ and $R_{sig} = \dfrac{1}{f \cdot C}$

During the second half of the sense operation the inputs are switched and the feedback circuit is also switched as discussed earlier in this chapter.
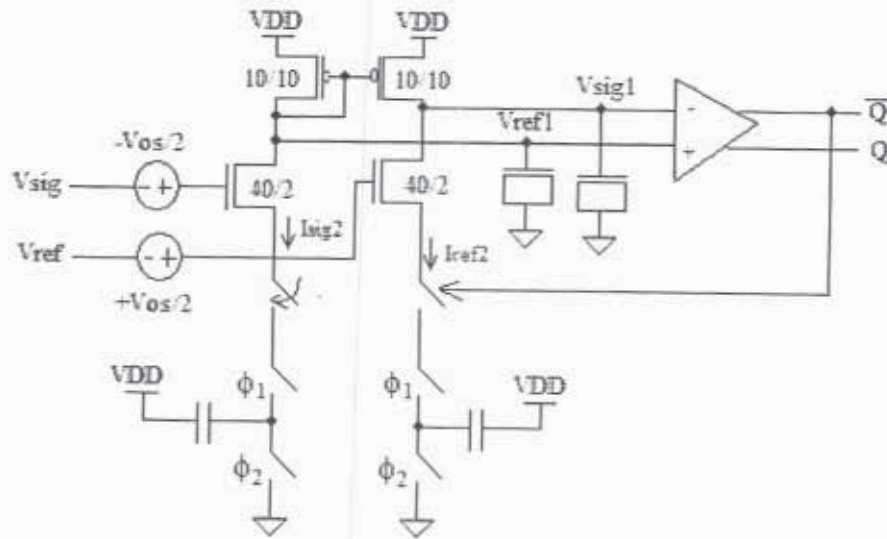
Figure 3.19 Voltage to current conversion during second half of the sense time

Current flowing in the reference path is,

$$I_{ref2} = \frac{V_{ref} + \dfrac{V_{os}}{2} - V_{thn}}{R_{ref}}$$ ...(3.11)

Let $V_{ref,shift} = V_{ref} - V_{thn}$

$$I_{ref2} = \frac{2V_{ref,shift} + V_{os}}{2R_{ref}}$$ ...(3.12)

Current flowing in the signal path is,

$$I_{sig2} = \frac{V_{sig} - \frac{V_{os}}{2} - V_{thn}}{R_{sig}} \qquad ...(3.13)$$

Let $V_{sig.shift} = V_{sig} - V_{thn}$

$$I_{sig2} = \frac{2V_{sig.shift} - V_{os}}{2R_{sig}} \qquad ...(3.14)$$

Where $R_{ref} = \dfrac{1}{f \cdot C \dfrac{(N-M)}{N}}$ and $R_{sig} = \dfrac{1}{f \cdot C}$

Because of the comparator and the feedback circuit the charge on the capacitor is constant. Therefore,

$$I_{ref1} + I_{ref2} = I_{sig1} + I_{sig2} \qquad ...(3.15)$$

Substituting the values for I_{ref1}, I_{ref2}, I_{sig1} and I_{sig2}

$$\frac{2V_{ref.shift} - V_{os}}{2R_{ref}} + \frac{2V_{ref.shift} + V_{os}}{2R_{ref}} = \frac{2V_{sig.shift} + V_{os}}{2R_{sig}} + \frac{2V_{sig.shift} - V_{os}}{2R_{sig}} \qquad ...(3.16)$$

$$\frac{V_{ref.shift}}{R_{ref}} + \frac{V_{ref.shift}}{R_{ref}} = \frac{V_{sig.shift}}{R_{sig}} + \frac{V_{sig.shift}}{R_{sig}} \qquad ...(3.17)$$

Substituting the values for R_{ref} and R_{sig}

$$\frac{V_{ref.shift}}{\dfrac{1}{f \cdot C \dfrac{(N-M)}{N}}} = \frac{V_{sig.shift}}{\dfrac{1}{f \cdot C}} \qquad ...(3.18)$$

$$V_{sig.shift} = V_{ref.shift} \cdot \frac{(N-M)}{N} \qquad ...(3.19)$$

N= number of times the DSM circuit is clocked

M=number of times the output goes high

Figure 3.20 shows the block diagram of the complete DSM circuit designed to eliminate the effects of path mismatch. Inverters are connected at the output of the DSM in order to eliminate the glitches as discussed in the earlier part of this chapter.
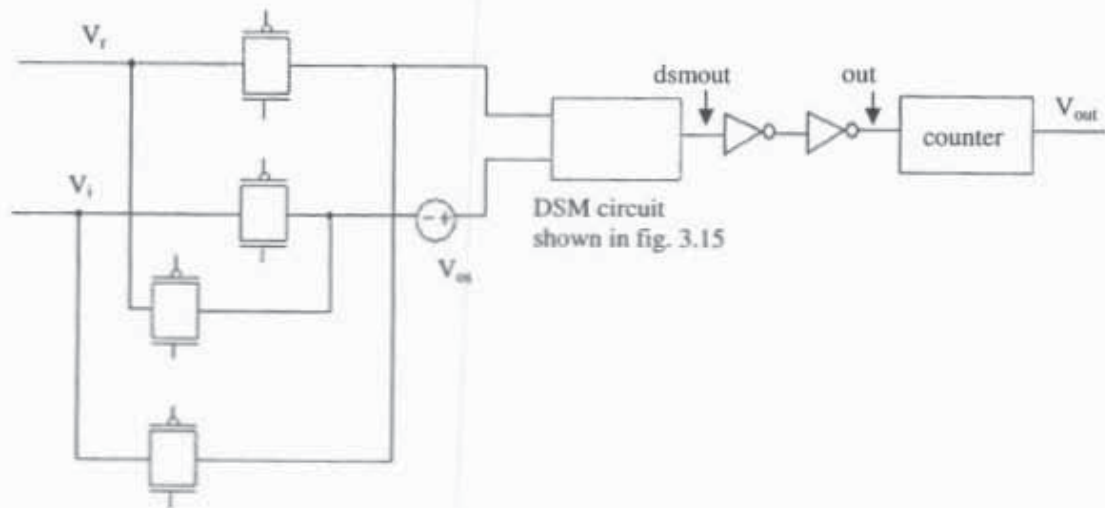
Figure 3.20 Block diagram representation of DSM circuit designed to eliminate offset

Figure 3.21 shows the simulation of figure 3.20 with an offset voltage of -50mV. Whenever starting the sense operation or switching the inputs in between the sense operation there will be a starting transient. That is the reason the counter is disabled during the start of sense operation and again in between the sense operation when the inputs are switched as shown in figure 3.21.
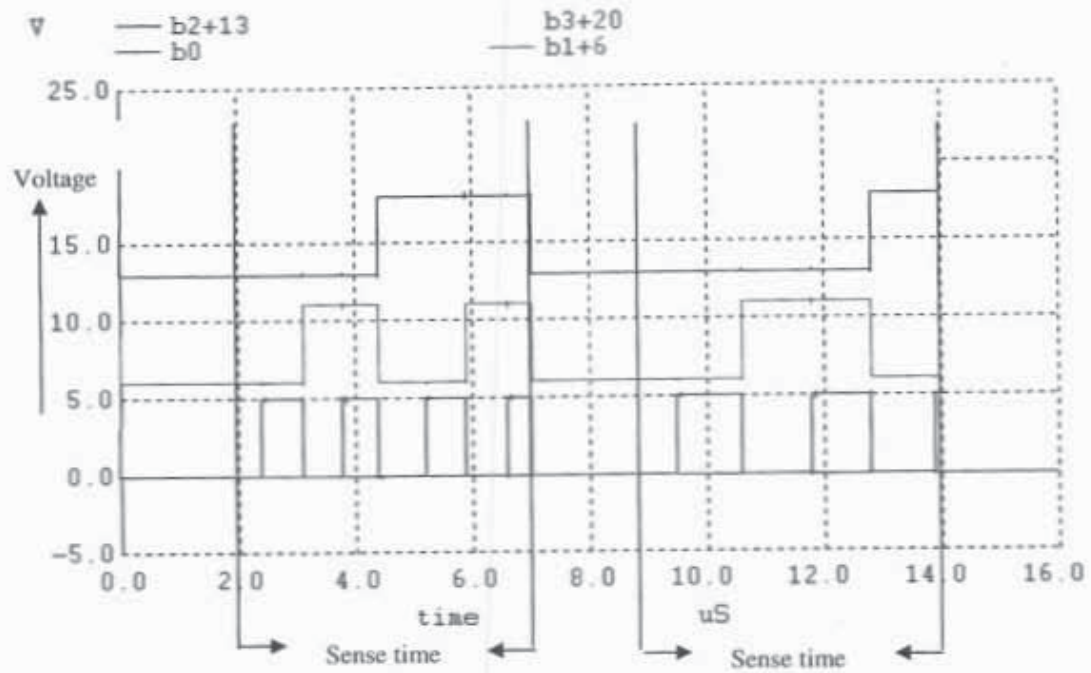
Figure 3.21 Simulation of figure 3.20

Count during the first half of the simulation i.e. when the offset in on the signal voltage path (2us to 7us),

$$C_1 = b_0 + b_1 + b_2 + b_3 = (2^0 \cdot x_0) + (2^1 \cdot x_1) + (2^2 \cdot x_2) \qquad \ldots(3.20)$$

$$C_1 = (2^0 \cdot 1) + (2^1 \cdot 1) + (2^2 \cdot 1) + (2^3 \cdot 1) = 1 + 2 + 4 \qquad \ldots(3.21)$$

$$C_1 = 7 \qquad \ldots(3.22)$$

Count during the second half of the simulation i.e. when the offset in on the reference voltage path (9us to 14us),

$$C_2 = b_0 + b_1 + b_2 + b_3 \qquad \ldots(3.23)$$

$$C_2 = (2^0 \cdot 1) + (2^1 \cdot 0) + (2^2 \cdot 1) = 1 + 0 + 4 \qquad \ldots(3.24)$$

$$C_2 = 5 \qquad \qquad \ldots(3.25)$$

Adding equations (3.22) and (3.25) will give the total count,

$$Count = C_1 + C_2 = 7 + 5 \qquad \qquad \ldots(3.26)$$

$$Count = 12 \qquad \qquad \ldots(3.27)$$

Count given by equation (3.27) is same as the count generated by the simulation in figure 3.2, which is the count generated by the DSM circuit without offset.

CHAPTER 4: RESULTS

Test Setup
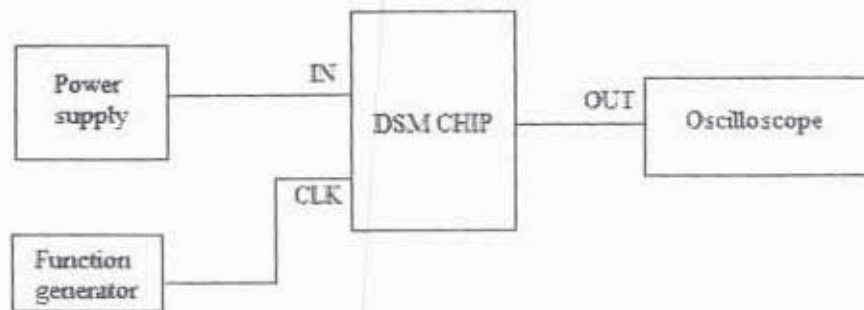
Figure 4.1 Schematic diagram showing test setup

The power supply voltage (VDD=5V) is applied to the DSM chip from the triple

outlet DC power supply. Clock of frequency 10MHz with amplitude of 5V is applied to

the chip from the waveform function generator. Reference voltage, which is constant, is

applied to the chip from the power supply. The signal voltage (V_{sig}) is varied using the

power supply generator. The digital output of the DSM chip is displayed on the

oscilloscope. The amplitude of signal pulse is $5V_{p-p}$ and the width of signal pulse is

100ns.

Results Obtained from Testing DSM Chip

Reference voltage (V_{ref}=2.5V), which is constant, is applied to the chip from the power supply. The signal voltage (V_{sig}) is varied from 2.5V to 0.7V using the power supply generator where 0.7V is the threshold voltage.

$V_{ref} = 2.5V, V_{thn} = 0.7V$

$N=100$, Where N = number of times DSM is clocked

Hand calculations:

$V_{ref.shift} = V_{ref} - V_{thn} = 2.5V - 0.7V = 1.8V$

For $V_{sig} = 2.4V$ $V_{sig.shift} = V_{sig} - V_{thn} = 2.4V - 0.7V = 1.7V$

Simulation results:

$V_{sig} = 2.4V$

$$V_{sig.shift} = \frac{N-M}{N} \times V_{ref.shift}$$

M=6 as shown in figure 4.2, where M=number of times Qi goes high

$$V_{sig.shift} = \frac{94}{100} \times 1.8 = 1.69V$$

Testing Results:

$V_{sig} = 2.4V$

$$V_{sig.shift} = \frac{N-M}{N} \times V_{ref.shift}$$

M=5, where M=number of times Qi goes high

$$V_{sig.shift} = \frac{95}{100} \times 1.8 = 1.71V$$
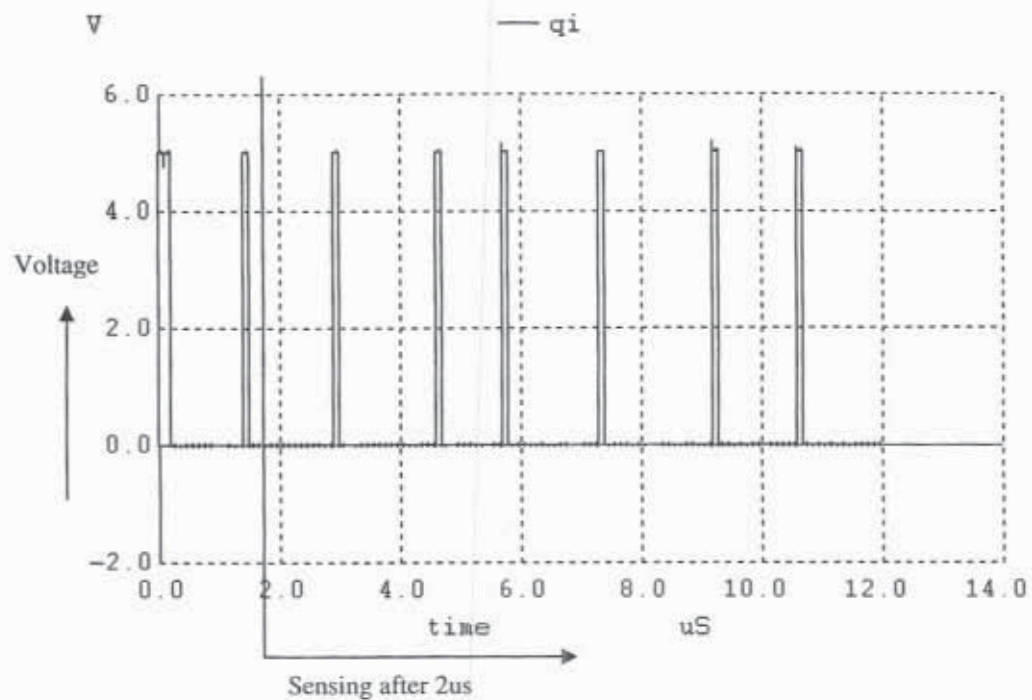
Figure 4.2 Showing the output of the DSM circuit shown in figure 2.20

Table 4.1 Tested and Calculated signals for constant reference voltage (V_{ref}=2.5V) and different signal voltages

Signal voltage (V_{sig})	V_{ref} - V_{sig}	Hand Calculations $V_{sig,shift}$	Count, M (from SIMS)	SIM results $V_{sig,shift}$	Count, M (from testing)	Testing results $V_{sig,shift}$
2.5	0	1.8	1	1.78	0	1.8
2.45	0.05	1.75	4	1.72	1	1.782
2.4	0.1	1.7	6	1.69	5	1.71
2.35	0.15	1.65	10	1.62	7	1.674
2.3	0.2	1.6	12	1.58	11	1.602
2.25	0.25	1.55	15	1.53	13	1.56
2.2	0.3	1.5	18	1.47	17	1.49
2.15	0.35	1.45	21	1.42	20	1.44
2.1	0.4	1.4	23	1.38	23	1.38
2.05	0.45	1.35	26	1.33	25	1.35
2	0.5	1.3	29	1.28	29	1.28
1.95	0.55	1.25	32	1.22	33	1.2
1.9	0.6	1.2	34	1.18	35	1.17

1.85	0.65	1.15	38	1.11	38	1.11
1.8	0.7	1.1	40	1.08	41	1.06
1.75	0.75	1.05	43	1.02	47	0.954
1.7	0.8	1	46	0.97	50	0.9
1.65	0.85	0.95	49	0.91	50	0.9
1.6	0.9	0.9	51	0.88	50	0.9
1.55	0.95	0.85	54	0.82	57	0.77
1.5	1	0.8	57	0.77	61	0.702
1.45	1.05	0.75	60	0.72	63	0.66
1.4	1.1	0.7	63	0.66	67	0.594
1.35	1.15	0.65	65	0.63	69	0.558
1.3	1.2	0.6	67	0.59	80	0.26
1.25	1.25	0.55	70	0.54	81	0.34
1.2	1.3	0.5	73	0.48	85	0.27
1.15	1.35	0.45	75	0.45	89	0.198
1.1	1.4	0.4	78	0.39	90	0.18
1.05	1.45	0.35	81	0.34	91	0.162
1	1.5	0.3	83	0.3	93	0.119
0.95	1.55	0.25	86	0.25	94	0.108
0.9	1.6	0.2	88	0.21	96	0.072
0.85	1.65	0.15	90	0.18	97	0.054
0.8	1.7	0.1	92	0.14	98	0.026
0.75	1.75	0.05	94	0.1	98	0.026
0.7	1.8	0	97	0.054	98	0.026

Figure 4.3 shows the comparison between the count generated from the simulations and the count generated from testing the chip. Count is the number of times Q_i goes high.
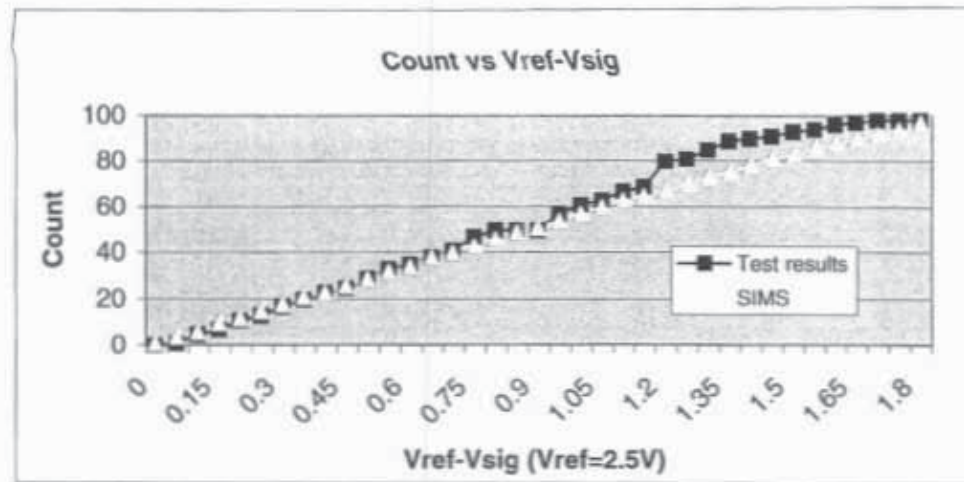
Figure 4.3 Count generated from testing the DSM chip (V_{ref}=2.5V)

Figure 4.4 shows the comparison between the shifted signal voltage ($V_{sig,shift}$) generated from the simulations and the shifted signal voltage ($V_{sig,shift}$) generated from testing the chip.
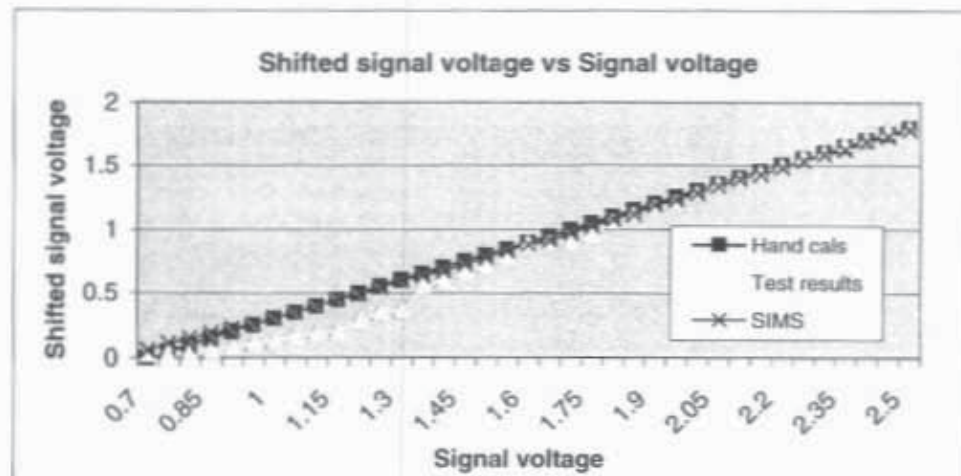
Figure 4.4 Comparison between hand calculations and testing results

Figure 4.5 shows the comparison between the count generated from the simulations and the count generated from testing the chip for V_{ref}=2.6V. Count is the number of times Qi goes high.
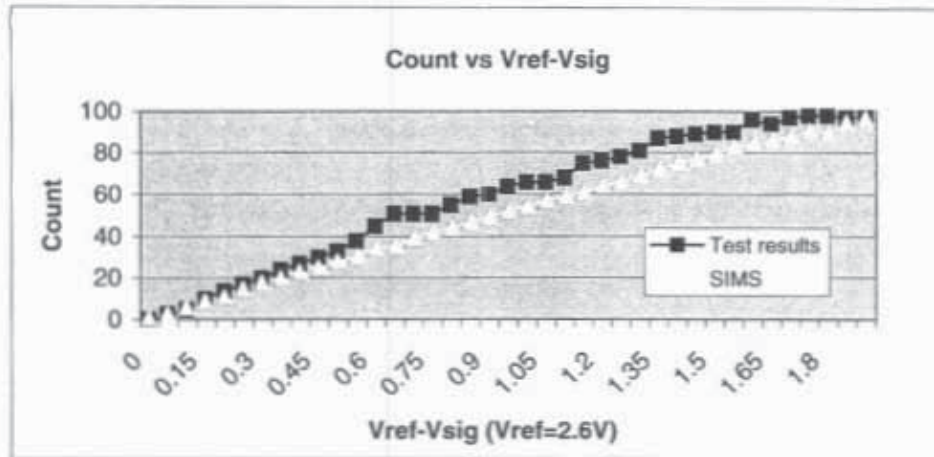
Figure 4.5 Count generated from testing the DSM chip

Figure 4.6 shows the comparison between the shifted signal voltage ($V_{sig.shift}$) generated from the simulations and the shifted signal voltage ($V_{sig.shift}$) generated from testing the chip for V_{ref}=2.6V.
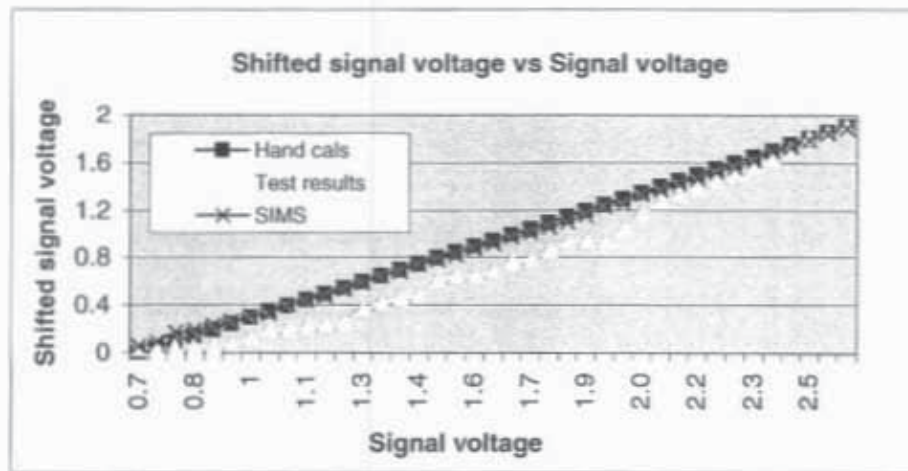
Figure 4.6 Comparison between hand calculations and testing results

The non-linearity observed in figure 4.3 and 4.5 is due to the following reasons,

1) As signal voltage (V_{sig}) approaches the threshold voltage

2) Body effect of the NMOS source follower

3) Limited to 100 count

Simulation Results of DSM Designed to Eliminate Mismatch

Negative offset voltage

Power supply voltage, VDD=5V. Clock of frequency 10MHz with amplitude of

5V is applied to the DSM circuit. Threshold voltage, V_{thn}=0.7V

Reference voltage, V_{ref} =2.5V

Signal voltage varying from V_{sig} =2.4–0.7V

Hand calculations:

$$V_{ref,shift}=V_{ref}-V_{thn}=2.5V-0.7V=1.8V$$

For V_{sig}=2.4V, $V_{sig,shift}=V_{sig}-V_{thn}=2.4V-0.7V=1.7V$

Simulation Results:

Without offset

$$V_{sig,shift}=\frac{N-M}{N}V_{ref,shift}$$

$N=1000$, where N = number of times DSM is clocked

M=61, where M=number of time the output Qi goes high

$$V_{sig,shift}=\frac{939}{1000}1.8=1.69V$$

Eliminate offset

Offset voltage, V_{os}=-50mV

$$V_{sig,shift}=\frac{N-M}{N}V_{ref,shift}, \quad N=1000 \text{ and } M=60$$

$$V_{sig,shift}=\frac{940}{1000}1.8=1.69V$$

Table 4.2 Simulated and Calculated signals for constant reference voltage
(V_ref=2.5V) and different signal voltages

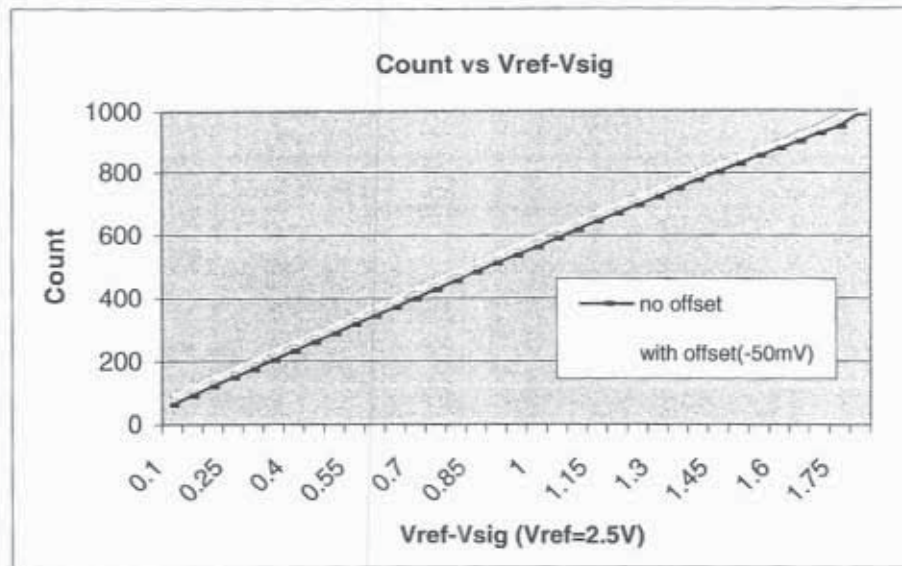| Signal Voltage V_{sig}	$V_{ref} - V_{sig}$	Count (M) no offset	Count (M) with offset (-50mV)	Count (M) eliminate offset (-50mV)	$V_{sig,shift}$ Hand cals	$V_{sig,shift}$ no offset	$V_{sig,shift}$ eliminate offset (-50mV)
2.4	0.1	61	92	60	1.7	1.69	1.69
2.35	0.15	90	118	89	1.65	1.63	1.63
2.3	0.2	118	147	118	1.6	1.58	1.58
2.25	0.25	147	175	147	1.55	1.53	1.53
2.2	0.2	175	204	176	1.5	1.48	1.48
2.15	0.25	203	232	205	1.45	1.43	1.43
2.1	0.4	231	260	232	1.4	1.38	1.38
2.05	0.45	259	288	262	1.35	1.33	1.32
2	0.5	287	316	290	1.3	1.28	1.27
1.95	0.55	316	344	318	1.25	1.23	1.22
1.9	0.6	343	373	347	1.2	1.18	1.17
1.85	0.65	371	400	376	1.15	1.13	1.12
1.8	0.7	400	429	404	1.1	1.08	1.07
1.75	0.75	428	456	433	1.05	1.02	1.02
1.7	0.8	455	484	461	1	0.98	0.97
1.65	0.85	484	511	489	0.95	0.92	0.91
1.6	0.9	511	539	517	0.9	0.88	0.86
1.55	0.95	537	566	544	0.85	0.83	0.82
1.5	1	563	593	572	0.8	0.78	0.77
1.45	1.05	591	620	599	0.75	0.73	0.72
1.4	1.1	617	647	627	0.7	0.68	0.67
1.35	1.15	644	672	654	0.65	0.64	0.62
1.3	1.2	670	700	680	0.6	0.59	0.57
1.25	1.25	698	726	709	0.55	0.54	0.52
1.2	1.3	724	752	732	0.5	0.49	0.48
1.15	1.35	751	777	759	0.45	0.44	0.43
1.1	1.4	777	805	783	0.4	0.4	0.39
1.05	1.45	804	828	811	0.35	0.35	0.34
1	1.5	829	854	840	0.3	0.3	0.28
0.95	1.55	855	879	860	0.25	0.26	0.25
0.9	1.6	880	899	890	0.2	0.21	0.19
0.85	1.65	902	928	914	0.15	0.17	0.15
0.8	1.7	928	950	922	0.1	0.12	0.14
0.75	1.75	949	982	945	0.05	0.09	0.09
0.7	1.8	990	998	996	0	0.025	0.025

Figure 4.7 Count generated by figure 2.20 and by figure 3.7 with
$$V_{os}=-50mV$$

Figure 4.8 Count generated by figure 2.20 and by figure 3.15 with
$$V_{os}=-50mV$$

Below figure shows the count generated by the DSM without offset and DSM

circuit with offset (V_{os}= -50mV) for V_{sig} from 2.2V to 1.95V. The plot shows that the

number of times the output Qi goes high is different without offset and with the presence of offset. This results in reduction in quality of the image.

Figure 4.9 Showing the count in figure 4.7

Figure 4.10 Showing the count in figure 4.8

Figure 4.10 shows the count generated by the DSM without offset and the DSM sensing circuit designed to eliminate offset ($V_{os}= -50mV$) for V_{sig} from 2.2V to 1.95V. The plot shows that the number of times the output goes high is approximately the same without offset and even with the presence of offset.

Figure 4.11 shows the comparison between the shifted signal voltage ($V_{sig,shift}$) generated from the hand calculations and the shifted signal voltage ($V_{sig,shift}$) generated from simulations for V_{ref}=2.5V and V_{os}=-50mV.

Figure 4.11 Comparison between hand calculations and simulated results

Positive offset voltage

Power supply voltage, VDD=5V. Clock of frequency 10MHz with amplitude of 5V is applied to the DSM circuit. Threshold voltage, V_{thn}=0.7V

Reference voltage, V_{ref} =2.5V

Signal voltage varying from V_{sig} =2.4V–0.7V

Offset voltage, V_{os}=50mV
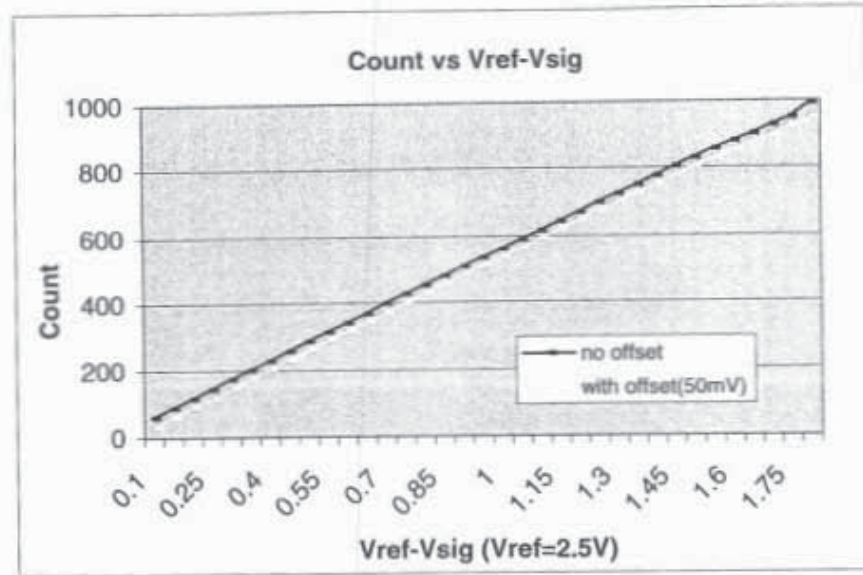
Figure 4.12 Count generated by figure 2.20 and by figure 3.7 with
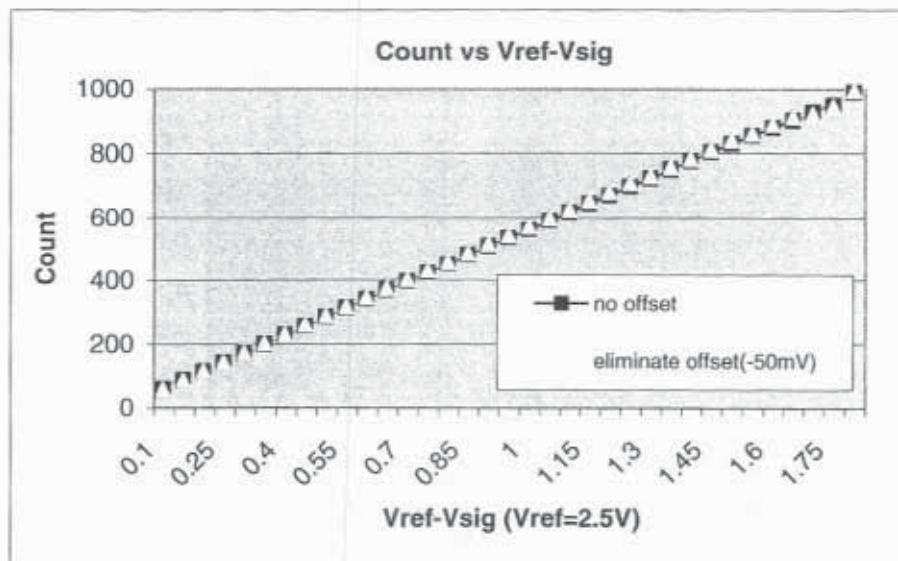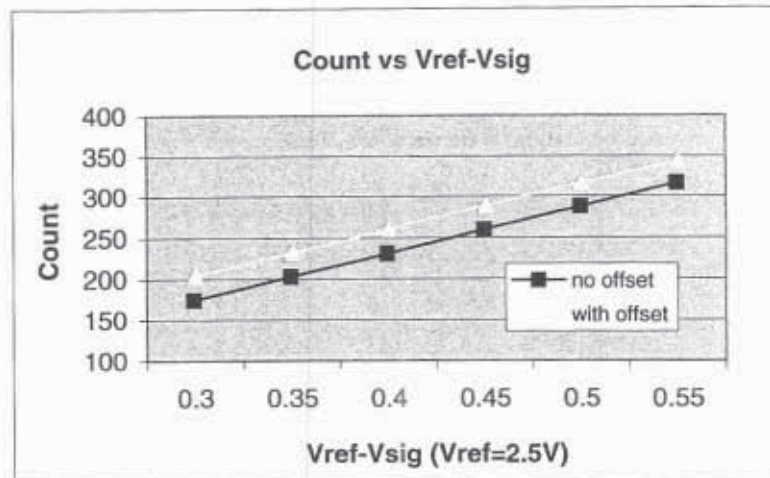V_{os}= 50mV
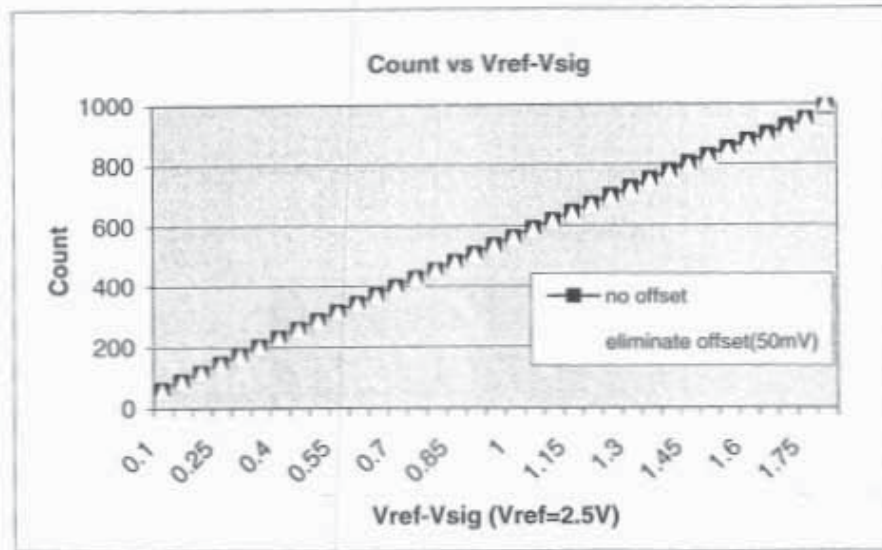
Figure 4.13 Count generated by figure 2.20 and by figure 3.15 with
V_{os} =50mV

Below figure shows the count generated by the DSM without offset and DSM with offset (offset voltage is 50mV) for V_{sig} from 2.2V to 1.95V. The plot shows that the number of times the output Qi goes high is different without offset and with the presence of offset. This results in reduction in quality of the image.
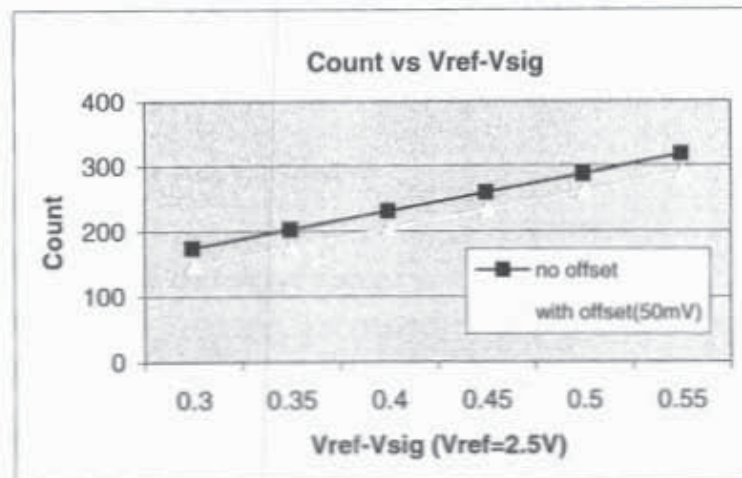
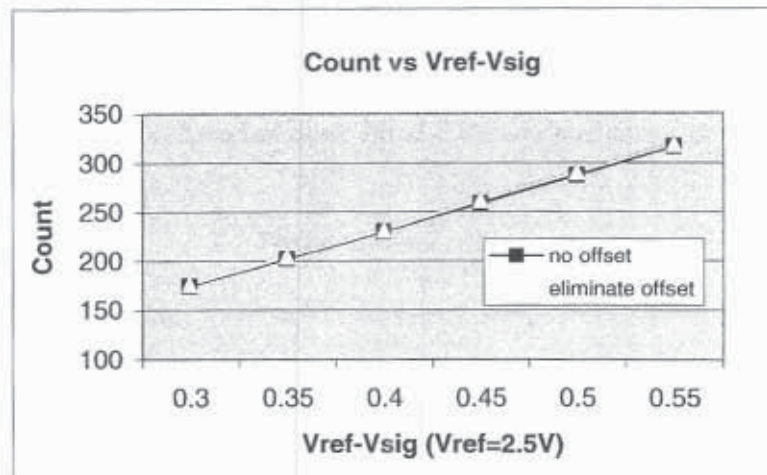**Figure 4.14 Showing the count in figure 4.12**
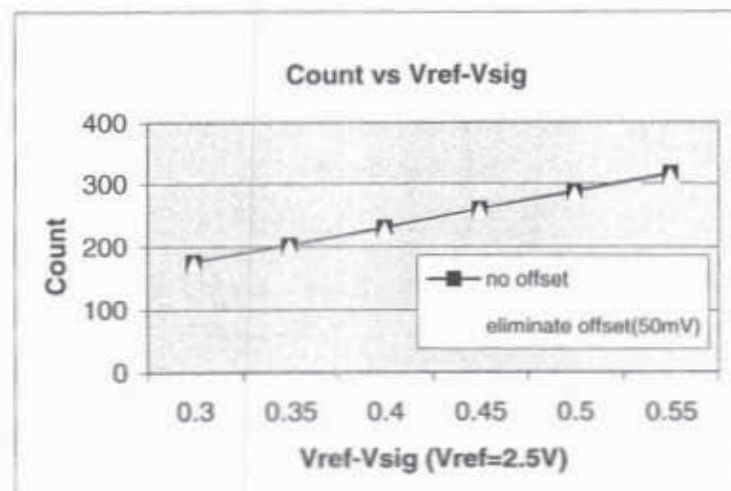
Figure 4.15 Showing the count in figure 4.13

Figure 4.15 shows the count generated by the DSM without offset and the DSM designed to eliminate offset (offset voltage is 50mV) for V_{sig} from 2.2V to 1.95V. The plot shows that the number of times the output goes high is approximately the same without offset and even with the presence of offset.

Figure 4.16 shows the comparison between the shifted signal voltage ($V_{sig,shift}$) generated from the hand calculations and the shifted signal voltage ($V_{sig,shift}$) generated from simulations for V_{ref}=2.5V and V_{os}=50mV.
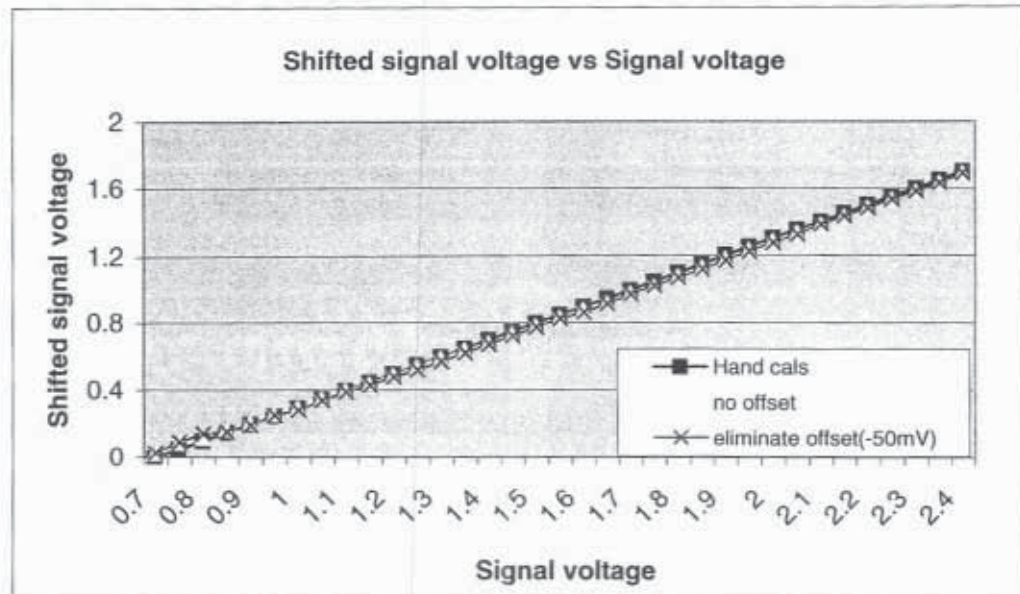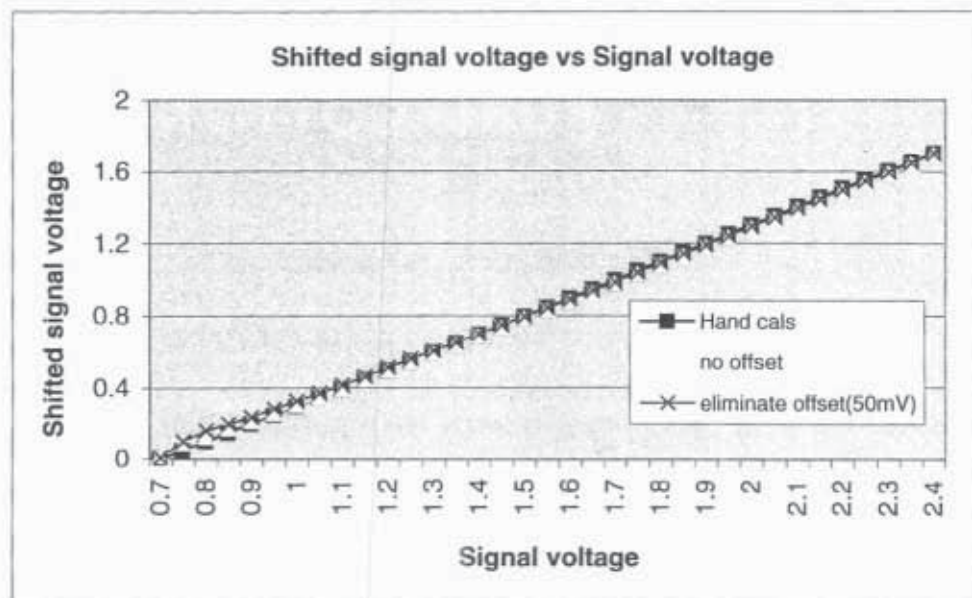

Figure 4.16 Comparison between hand calculations and simulated results

Resolution of the DSM

The resolution can be calculated by using the equation shown below:

$$V_{res} = \frac{V_{ref,shift}}{N} = \frac{(2.5-0.7)}{1000} = 1.8mV$$

Table 4.2 shows that when the input changes from 2.4V to 2.3V the difference in the count is 57, from 2.3V to 2.2V the count difference is 57, from 2.2V to 2.1V the difference is 56, from 2.1V to 2V the difference is 56, from 2V to 1.95V the code is 57. Consider an average change of 56 counts per 100mV change in the input voltage in order to get a better estimation for the resolution. So,

$$V_{res} = \frac{100mV}{57} = 1.75mV$$

$$V_{ref,shift} = V_{res} \cdot N = 1.75mV \cdot 1000$$

So, $V_{ref,shift} = 1.75V$ and $V_{thn} = V_{ref} - V_{ref,shift} = 0.75V$

Calculations of the shifted reference and signal voltages using $V_{thn} = 0.72V$ instead of $V_{thn} = 0.7V$ are shown below:

$V_{ref} = 2.5V$, $V_{ref,shift} = 2.5 - 0.75 = 1.75V$

1) For $V_{sig} = 2.4V$

   $V_{sig,shift} = 2.4 - 0.75 = 1.65V$ (Hand cals)

   $V_{sig,shift} = \frac{1000-61}{1000} \cdot 1.75 = 1.64V$ (SIMS)

2) For $V_{sig} = 2.3V$

   $V_{sig,shift} = 2.3 - 0.75 = 1.55V$ (Hand cals)

$$V_{sig,shift} = \frac{1000-118}{1000} \cdot 1.75 = 1.54V \text{ (SIMS)}$$

Table 4.3 Simulated and Calculated signals for constant reference voltage (V_{ref}=2.5V) and different signal voltages

Signal Voltage V_{sig}	$V_{ref}-V_{sig}$	Count	$V_{sig,shift}$ Hand cals V_{thn}=0.7V	$V_{sig,shift}$ SIMS V_{thn}=0.7V	$V_{sig,shift}$ Hand cals V_{thn}=0.75V	$V_{sig,shift}$ SIMS V_{thn}=0.75V
2.4	0.1	61	1.7	1.69	1.65	1.64
2.35	0.15	90	1.65	1.63	1.6	1.69
2.3	0.2	118	1.6	1.58	1.55	1.54
2.25	0.25	147	1.55	1.53	1.5	1.49
2.2	0.2	175	1.5	1.48	1.45	1.44
2.15	0.25	203	1.45	1.43	1.4	1.39
2.1	0.4	231	1.4	1.38	1.35	1.34
2.05	0.45	259	1.35	1.33	1.3	1.29
2	0.5	287	1.3	1.28	1.25	1.24
1.95	0.55	316	1.25	1.23	1.2	1.19
1.9	0.6	343	1.2	1.18	1.15	1.14
1.85	0.65	371	1.15	1.13	1.1	1.1
1.8	0.7	400	1.1	1.08	1.05	1.05
1.75	0.75	428	1.05	1.02	1	1
1.7	0.8	455	1	0.98	0.95	0.95
1.65	0.85	484	0.95	0.92	0.9	0.9
1.6	0.9	511	0.9	0.88	0.85	0.85
1.55	0.95	537	0.85	0.83	0.8	0.81
1.5	1	563	0.8	0.78	0.75	0.76
1.45	1.05	591	0.75	0.73	0.7	0.71
1.4	1.1	617	0.7	0.68	0.65	0.67
1.35	1.15	644	0.65	0.64	0.6	0.62
1.3	1.2	670	0.6	0.59	0.55	0.57
1.25	1.25	698	0.55	0.54	0.5	0.52
1.2	1.3	724	0.5	0.49	0.45	0.48
1.15	1.35	751	0.45	0.44	0.4	0.43
1.1	1.4	777	0.4	0.4	0.35	0.39
1.05	1.45	804	0.35	0.35	0.3	0.34
1	1.5	829	0.3	0.3	0.25	0.29
0.95	1.55	855	0.25	0.26	0.2	0.25
0.9	1.6	880	0.2	0.21	0.15	0.21
0.85	1.65	902	0.15	0.17	0.1	0.17

0.8	1.7	928	0.1	0.12	0.05	0.12
0.75	1.75	949	0.05	0.09	0	0.08
0.7	1.8	990	0	0.025	-0.005	0.01

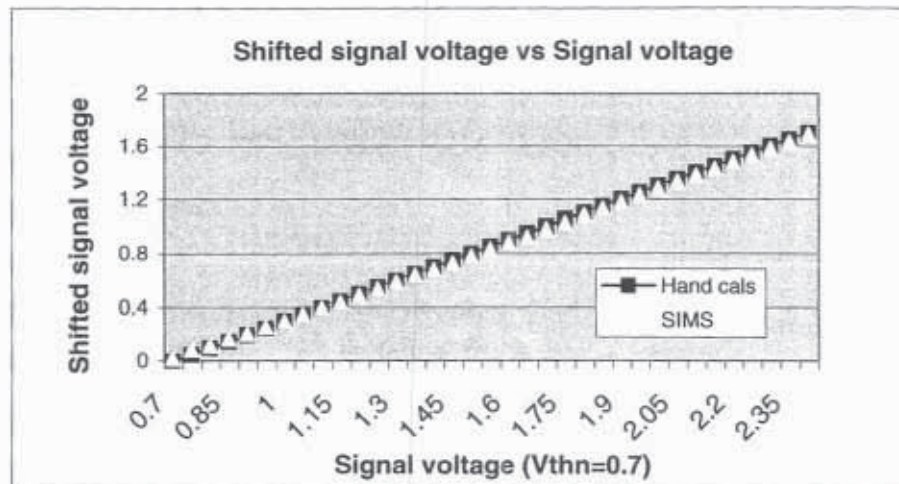**Figure 4.17 Comparison of voltages between hand calculations and simulated results for V_{thn}=0.7V**
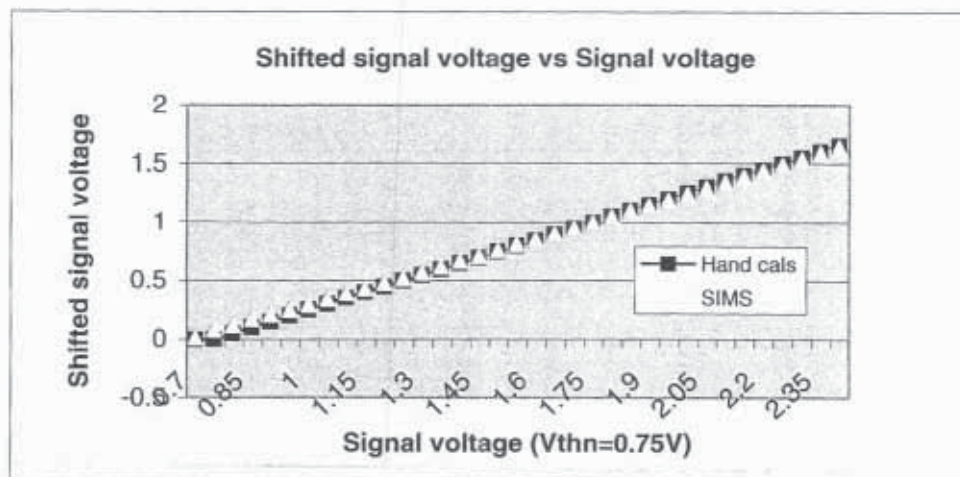

Figure 4.18 Comparison of voltages between hand calculations and simulated results for V_{thn}=0.75V

It can be seen from the above two plot that the shifted signal voltage calculated using V_{thn}=0.75V are closer to hand calculations when compared to the shifted signal voltage calculated using V_{thn}=0.7V.

Chip Image

Figure 4.19 shows the layout of the DSM sensing circuit shown in figure 2.20.

This chip in fabricated in 0.5um process in the MOSIS. Apart from the entire DSM

sensing circuit test structures of buffer, comparator, DSM input circuit and nand gate
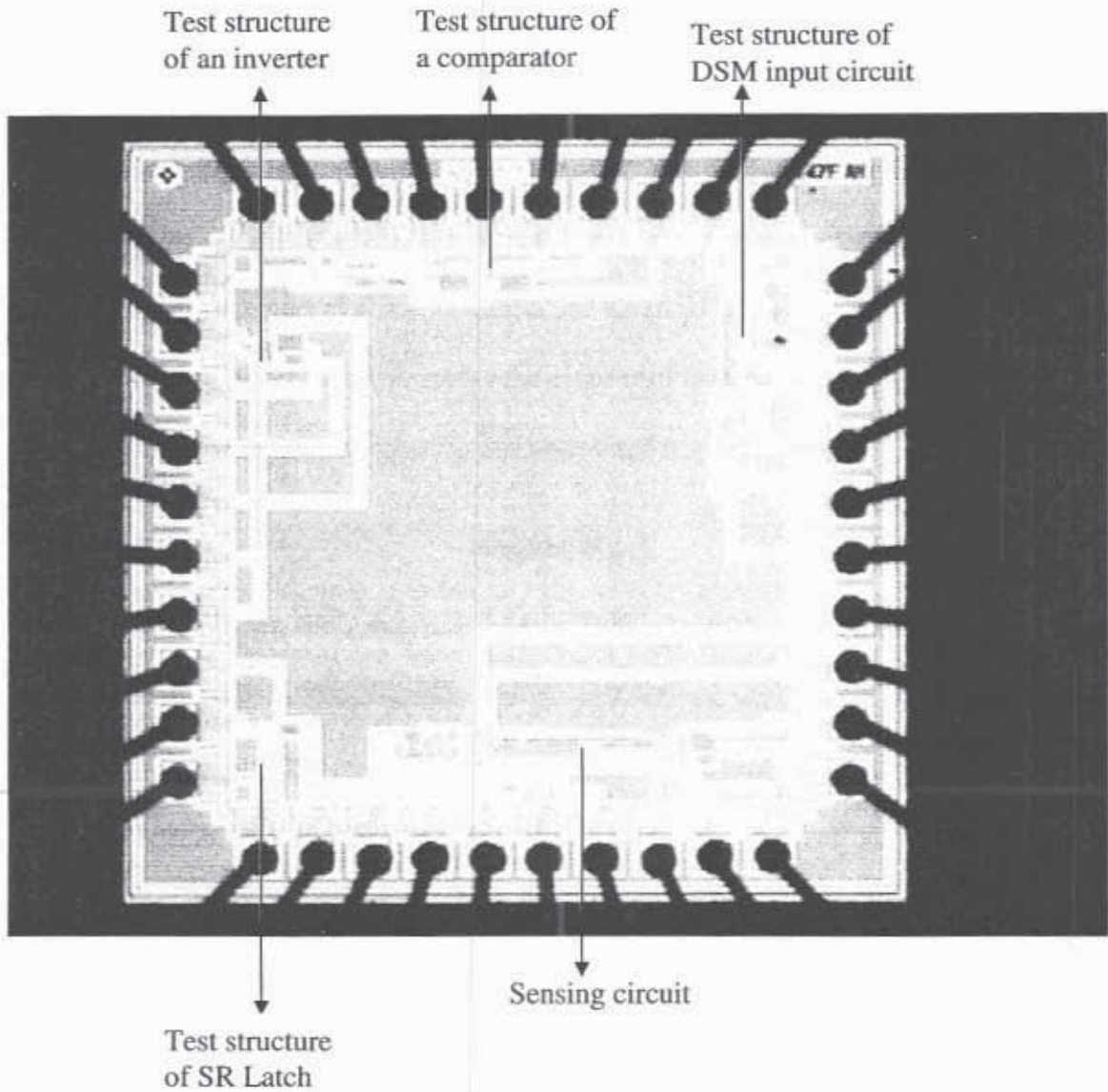
have also been laid out.

Test structure
of an inverter

Test structure of
a comparator

Test structure of
DSM input circuit

Sensing circuit

Test structure
of SR Latch

Figure 4.19 Layout of DSM sensing Circuit

CHAPTER 5: CONCLUSION

A sigma delta modulator that eliminates the mismatch in the signal paths of the sensing circuit has been designed. The inputs of the DSM are switched halfway through the sense time so that the offset is on reference path for half the sense time and for remaining half of the sense time the offset is on the signal path. Switching the inputs results in eliminating the offsets by averaging the mismatch ideally to zero. The output of the DSM is a digital output, which is used to determine the analog output coming from the pixel. This digital output is given to the D-FF, which acts as a counter. The counter is disabled during the start of sense operation and again in between the sense operation when the inputs are switched. It counts the number of times the output of ADC has gone high. The desired signal voltages can be determined from this count.

Future Work

In delta sigma ADC there can be a column mismatch, which means that in one column the threshold voltages can be 490mV and 500mV which other column may have threshold voltages of 510 and 520. This mismatch will reduce the quality of the image. A sigma delta ADC, which eliminates the effects of column mismatch can be designed.

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