CURRENT-MODE PHOTON-COUNTING CIRCUIT WITH SIGE BICMOS INPUT STAGE

by

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Abstract

Continued advances in photodetector technology have helped improve the imaging capabilities of LiDAR systems or other time-of-flight imaging efforts. As a major part of the receiver within a LiDAR system, the photodetector can offer features such as faster rise times, narrower pulse widths, or larger gains to help achieve greater timing resolution or sensitivity to faint light levels. These benefits, however, are contingent on the ability of the accompanying readout circuit to reliably process the fast, electrical signals generated by the photodetector. While common front-end circuits involve the use of feedback amplifiers, their stability can become a major concern at higher frequencies. In pursuit of an alternative topology, this thesis investigates the design of a current-mode photon-counting circuit for LiDAR applications.

In this effort, four test circuits were explored which were based on the concept of a current comparator. The proposed circuit would compare the photodetector current signal with that of an adjustable reference current and generate a 1.8-V digital signal whenever one current magnitude exceeded the other. The design, simulation, and layout of the circuits were done using a 180-nm SiGe BiCMOS process, and the photodetector of interest was a microchannel plate photomultiplier tube (MCP-PMT). To interface with the photodetector, the designs feature a BiCMOS regulated cascode (RGC) input stage which provides a low input impedance of about 2-ohms up to 500-MHz or, when used with a 47-ohm in-series matching resistor, about 50-ohms up to 2-GHz. The circuits can detect typical signals from the detector which include pulses that are 300-ps FWHM wide with a minimum height of 8-uA at count rates up to 1-GHz. The corresponding output pulses from the designs had a delay which ranged from 0.9 to 1.2-ns. Each circuit had a static power consumption no more than 5.5-mW/ch with an anticipated dynamic power consumption substantially less than the target of 20-mW/ch.

Initial test results on the fabricated chip confirmed the basic function of the test circuits using lower frequency signals with amplitudes near 300-μA. Further testing will, however, be necessary to fully characterize the designs and to see how viable the proposed designs are for the intended application.

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