A Highly-Sensitive Global-Shutter CMOS Image Sensor with on-Chip Memory for hundreds of kilo-frames per second scientific experiments

By

Konstantinos Moutafis

Bachelor of Science in Electrical and Computer Engineering

National Technical University of Athens, 2007

Master of Science in Energy and Environmental Technology, Economics

City University of London, 2009

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of the requirements for the

Doctor of Philosophy in Electrical Engineering

Department of Electrical and Computer Engineering

Howard R. Hughes College of Engineering

The Graduate College

University of Nevada, Las Vegas

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ABSTRACT

In this work, a highly-sensitive global-shutter CMOS image sensor with on-chip memory that can capture up to 16 frames at speeds higher than 200kfps is presented. The sensor fabricated and tested is a 100 x 100 pixel sensor, and was designed to be expandable to a 1000 x 1000 pixel sensor using the same building blocks and similar architecture.

The heart of the sensor is the pixel. The pixel consists of 11 transistors (11T) and 2 MOSFET capacitors. A 6T front-end is followed by a Correlated Double Sampling (CDS) circuitry that includes 2 capacitors and a reset switch. The 4T back-end circuitry consists of a source follower, in-pixel current source and 2 switches. The pixel design is unique because of the following. In a relatively small area, 15.1um x 15.1um, it performs CDS that limits the noise stored in the pixel memories to less than 0.33mV rms and allows the stored value to be read in a single readout. Moreover, it has in-pixel current source, which can be turned OFF when not in use, to remove the dependency of its output voltage to its location in the sensor. Furthermore, the in-pixel capacitors are MOSFET capacitors and do not utilize any space in the upper metal layers, therefore, they can be used exclusively for routing. And at the same time it has a fill factor greater than 40%, which important for high sensitivity.

Each pixel is connected to a dedicated memory, which is outside the pixel array and consists of 16 MOSFET capacitors and their access switches (1T1C design). Fifty pixels share a line for their connection to their dedicated memory blocks, and, therefore, the transfer of all the stored pixel values to the on-chip memories happens within 50 clock cycles. This allows capturing consecutive frames at speeds higher than 200 kfps. The total rms noise stored in the memories is 0.4 mV.

For the readout, 2 pipeline 100 MHz 12-bits ADCs were selected. Before the reading of each stored frame, the floating common lines inside the memory blocks are reset to remove any dependency on previous readings. Each memory block has its own output buffer which consists of a source follower, a current source and 2 switches. Fifty memory blocks share a line for their connection to the ADC. The total rms noise that is read from the ADC is 0.33mV.

The readout time is 8ms, and it is fast enough to ensure that the memories are not having a significant voltage drop due to leakages. The calculated leakage during this time is negligible but the testing results indicate that it can become significant when the memories are exposed to light. Therefore, the memory blocks have to be covered from light for high irradiance conditions.

The ADCs selected for the readout circuitry were tested for input referred noise and were proved to have a significant amount (0.7mV rms). This increases the total input referred noise to $38e^-$, compared to the expected $15e^-$. The resulting SNR of the presented sensor is 43.9 dB and the Dynamic Range (DR) is 57.5dB.

The image sensor was proved to operate at 200kfps and for exposure times as low as 1us. Its sensitivity is close to the expected value, and specifically $22.3uV/e^-$. The linearity of the sensor is within $\pm$1.9% and the nonuniformity error for 50% saturation is 4.1%. The latter can be reduced with software calibration.

The fast, low noise and highly sensitive image sensor presented in this work was proved to be able to operate as expected and therefore it can be expanded to a Mpixel sensor, due to its unique characteristics. The ADCs noise will be removed and a light blocking layer will be applied above the memories. The resulting sensor will have the same SNR but the DR will be greater than 63dB.

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For my wife Claire and my daughter Fey

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CHAPTER 1: INTRODUCTION

Engineers around the world use video cameras to analyze high-speed phenomena in numerous fields such as aerodynamics, computer imaging, high energy physics, hydrodynamics, material science research, mechanics, nanotechnology and military/defense research [1, 2, 3]. The human eye has an exposure time of about 100ms [4], which makes it insufficient to capture shorter lasting phenomena or unblurred images of small fast-moving objects. Therefore, high-speed cameras are needed in order to capture one or more instances of them and then visualize them at a slower rate.

The most common types of image sensors are CCD (Charged Coupled Device) and CMOS (Complementary Metal Oxide Semiconductor). To capture an image, these sensors can either use a Global-Shutter, capturing an entire frame all at once, or Rolling-Shutter, where the sensor is exposed in a progressive motion. Most CCD sensors employ Global-Shutter, while there are many CMOS sensors having rolling shutter [5, 6]. The basic schematics of CCD and CMOS sensor architectures can be seen in Figure 1.

In CCD, the signal from each pixel is serially transferred to a single Analog-to-Digital Converter. The number of the pixels and the rate at which the individual pixels can be transferred and then digitized sets the frame rate limit., which is the rate that a camera can capture consecutive pictures (video). A CMOS sensor can use one converter per column, which reduces the number of pixels digitized per converter and consequently increases the frame rate. However, the entire array must still be converted one row at a time. To achieve higher frame rates, each individual row is able to begin next frame's exposure once completing previous frame's readout. These exposure delays between lines can create Rolling Shutter artifacts, such as wobble, skew

(Figure 2), spatial or temporal aliasing, and make the use of a Global-Shutter scheme necessary for high speed imaging.

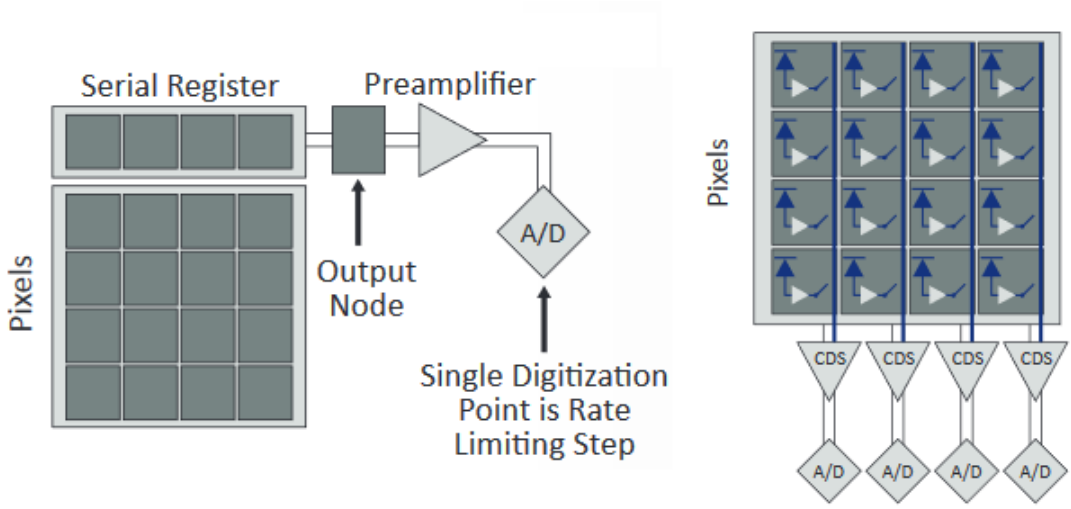

Figure 1: Basic architectures of CCD (left) and CMOS (right) [7]

Figure 2: Rolling Shutter skew artifact [5]

A CMOS image sensor can also be used in Global Shutter mode. Each pixel transfers simultaneously its charge to a memory, usually within the pixel, where it waits to be digitized. This eliminates the overlapping capability of the sensor and reduces the frame rate in half [7]. Sony, Blackmagic Design, Aja, RunCam and On Semiconductors are just some of the CMOS Global Shutter cameras available in the market and some can achieve frame rates up to 120 frames per second [8, 9, 10, 11, 12].

One way to increase the frame rate of the sensor is to store a small number of frames on-chip before reading them out. This mode is known as Burst mode, while the traditional reading out each frame before capturing the next one mode is called Continuous. In both cases the frame rate is limited by RC delays and slew rate. But when operating at Continuous mode the values to be read have to pass through the readout circuitry, and this will reduce the frame rate dramatically. In addition, more pixel lines in a sensor working in continuous mode would lead to a smaller frame rate, because more pixels would have to be read through the read out circuitry.

The number of pixels of an image sensor is important because they affect the detail the camera can resolve, which is usually called resolution. For example, a 1Mpixel camera focusing on a 1m x 1m scene can ideally resolve a up to 1mm detail. However, higher resolution usually comes with a cost of lower frame rate as discussed earlier. Converting the received light information and storing it locally in each pixel for some frames could increase the frame rate dramatically but will also affect the light to electrons conversion efficiency and this will eventually reduce the Signal to Noise Ratio (SNR) and the Dynamic Range (DR) of the sensor.

Some approaches on how the frame rate can be increased, and how this affects the resolution and the noise of an image sensor are discussed in the following chapter.

CHAPTER 2: LITERATURE REVIEW

To increase the output date rate of an image sensor, several papers have suggested parallel output circuits architectures [13] or column-parallel ADCs [14, 15, 16, 17]. However, the improvements at the frame rates are limited by the RC delays of the pixels output wires, slew rate and converter reading times. The readout speed of these approaches is limited to 10 Gpixels/s [18]. At this speed, the maximum achievable frame rate for a 1Mpixel sensor is 10kfps, for a 2Mpixel sensor is 5kfps and so on.

Conventional burst image sensors use the CCD technology, and have the on-chip memory next to each pixel [19, 20, 21]. These sensors can achieve very high frame rates without reducing the number of pixels (100 stored frames for 81kpixels at 1Mfps in [20]), at the cost of a small fill factor. A 709kpixels CMOS image sensor having 180 CCD memory cells in pixel is presented in [22] and is reported to achieve 5Mfps in burst mode and 1,180fps in continuous mode, again at the cost of a small fill factor (11%). The main drawback of this approach is the small fill factor, because the photosensitive active area in the pixel is getting relatively smaller, which results in less electrons produced from the photons hitting the silicon. This could be a problem for high speed photography or video because the light available in small exposure times is limited and it is important to use it efficiently.

Microlenses can be used to “boost” the fill factor to about 70%, at the cost of making the sensor more dependent on the lens aperture and the angle of incident photons [23]. Backside Illumination (BSI) is another technology that can be used to increase the fill factor to near 100% [24], and it can be used in both CCD and CMOS image sensors. This technology can be really useful for high-speed burst image sensors with in pixel memory, but the costs and complexity

associated with it are high. Moreover, problems due to signal leakages from pixels to memories and mechanical problems due to wafer thinning have to be addressed.

Two high-speed (up to 20Mfps in Burst mode) global-shutter 100kpixels CMOS image sensors, having 128 on-chip memories per pixel, spatially separated from the active area of the image sensor, in a 0.18μm CMOS with pinned photodiode process, have been fabricated and tested in [18] and [25] by the same team of authors. The pixel design (Figure 3) enables in-pixel Correlated Double Sampling (CDS) in a single readout which is very useful for high speed imaging. Moreover, multiple pixel output wires per column (4 pixels share a line) are used in these works, resulting in 32 output wires per column (Figure 4). Finally, pixel source followers use in-pixel current sources to drive the signals to the memories, instead of in-column current sources. The use of in-column current sources would give different voltage drops on the pixel output wires depending on the distance between the pixel and the current source and this would lead to image shading. On the other hand, when using in-pixel current sources the reference current does not flow in the pixel output wires and therefore the output signal is not related to the different parasitic resistances of those wires.

The main drawback of [18] and [25] is that the two capacitors used for the in-pixel noise reduction circuit create a capacitive voltage divider that reduces the voltage swing at the output of the pixel, which effectively reduces the conversion gain of the pinned photodiode and consequently increases the input referred noise. To reduce this effect, the coupling capacitor must be much larger than the sampling and hold capacitor, which has to be large itself to keep the reset thermal noise small. Moreover, both capacitors have to be linear, so that the output can be linear too. Another problem is that the 32 lines per column, together with the relatively big in-pixel capacitors and the triple well process used for the source followers, plus the rest of the

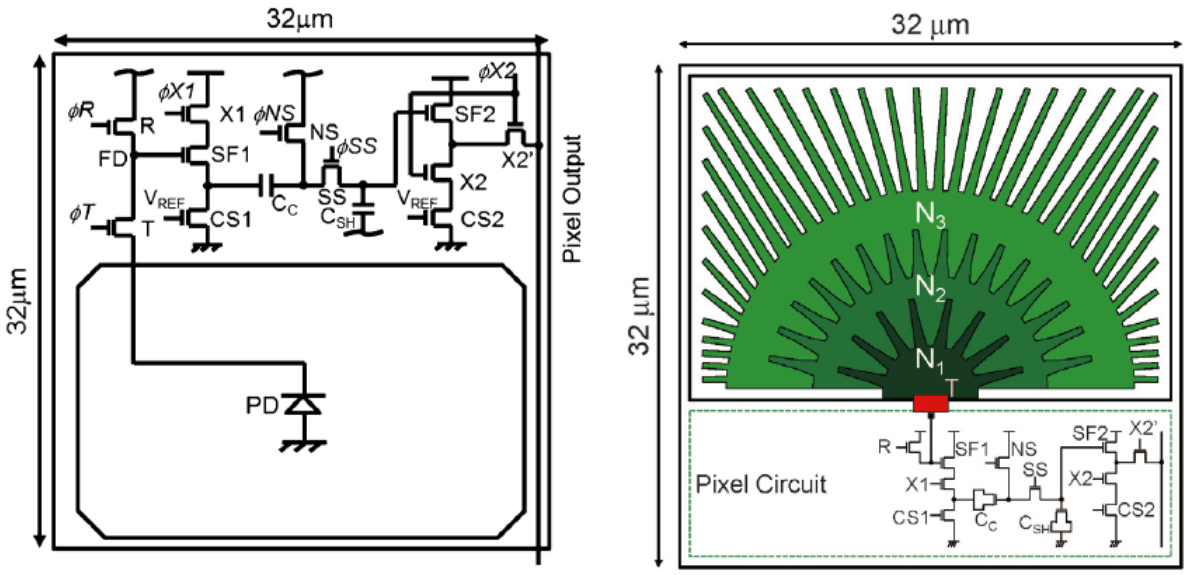

Figure 3: Pixel designs in [18] and [25]

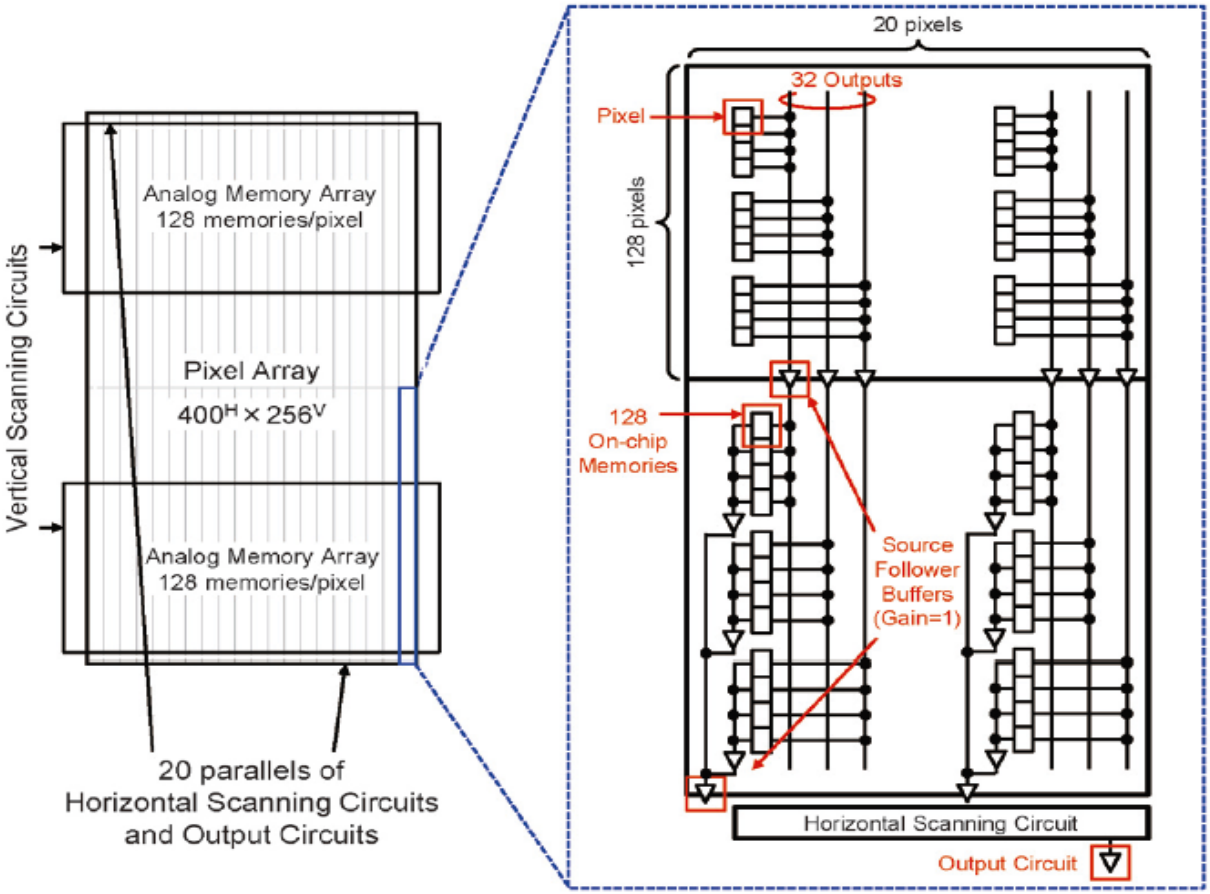

Figure 4: Block diagram of sensors developed in [18] and [25]

in-pixel circuitry, limit the fill factor of the pixel to 37% in [18] and 55% in [25], even if the pixel used is relatively big (32um in both papers). The increase in the latter is mainly because two metal layers were used for the connections between the pixels and the on-chip memories compared to only one in [18].

The problems described above limits the applicability of [18] and [25] for high-speed Mpixel sensors, because more pixels would mean extra lines per column, resulting in much smaller fill factors. However, a large fill factor and consequently high light sensitivity is crucial for high-speed applications, because in order to capture high speed phenomena, short exposure time is needed, and the light collected in that time is usually small. Moreover, because of the large pixel used, the distances between the pixels and the memories would be unnecessarily large for Mpixel sensors, increasing the delays and consequently reducing the frame rate.

In [26], another architecture for in-pixel CDS in a single readout is proposed and tested to pixels as small as 4.8um (Figure 5). Similar to [18] and [25], the sampling and hold capacitor can be much larger than the floating diffusion capacitance, keeping the reset thermal noise small. The difference is that the coupling capacitor is now after the sampling and hold capacitor and there is no voltage divider effect. The coupling capacitor does not have to be much larger than the sample and hold capacitor, and as long as it is much larger than the parasitic capacitances, the requirement to be linear is relaxed. This could be very useful for high speed imaging, where a large fill factor is usually necessary, because the size of the capacitor does not have to be very big. However, in [26], only the pixel architecture is presented and tested. Therefore, the pixels functionality is not tested as part of a complete image sensor, with specific number of pixels at specific speeds and exposure times. Moreover, the sizes of the capacitors and the other devices used in pixel to give the presented results are not given, neither the resulting fill factors. Finally,

there are no in-pixel current sources for the source followers. The source follower after the floating diffusion (M3) is using a pulse signal to turn it ON or OFF, which could create delay problems and noise in large image sensor architectures. The pixel output source follower depends on an in-column source follower which would result in voltage drops that depend on the distance between the pixel and the source follower.

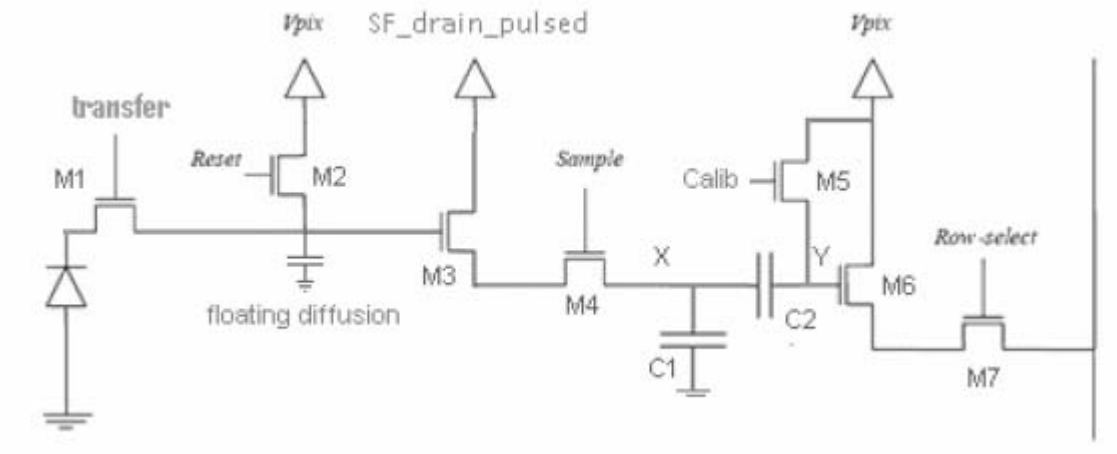

Figure 5: Pixel design in [26]

CHAPTER 3: MOTIVATION

High-speed imaging is necessary to capture high speed phenomena. Global-shutter image sensors are able to capture those phenomena without any rolling shutter artifacts and with acceptable blur if the integration (exposure) time is set so that the motion blur is below a specified limit. The conversion efficiency from photons to electrons can be crucial for high speed applications because of the limited photons available per pixel and is process dependent but also depends on the fill factor of the pixel. Conventional burst mode sensors use the CCD technology and on-chip memory at the cost of small fill factors, which may make them unsuitable for low light high speed applications.

In Figure 6, we see that CCD image sensors can achieve frame rates up to billions of frames per second when they operate in burst mode. The ultra-high speed cameras come in three categories; rotating mirror (RM CCD), beam-split optical paths (ICCD) and on-chip memory [27].

The ultra-high speed cameras using on-chip memory have either a small fill factor, or a little higher fill factor but they are not scalable to Mpixel size sensors. Kirana camera has a fill factor of 11% [28], while the other 2 sensors (small red dots) are based on the pixel and sensor architecture described in CHAPTER 2 ([18], [25]) , which result in a small fill factor, compared to the pixel size. The large pixel they use, makes them a bad fit for Mpixel expansion.

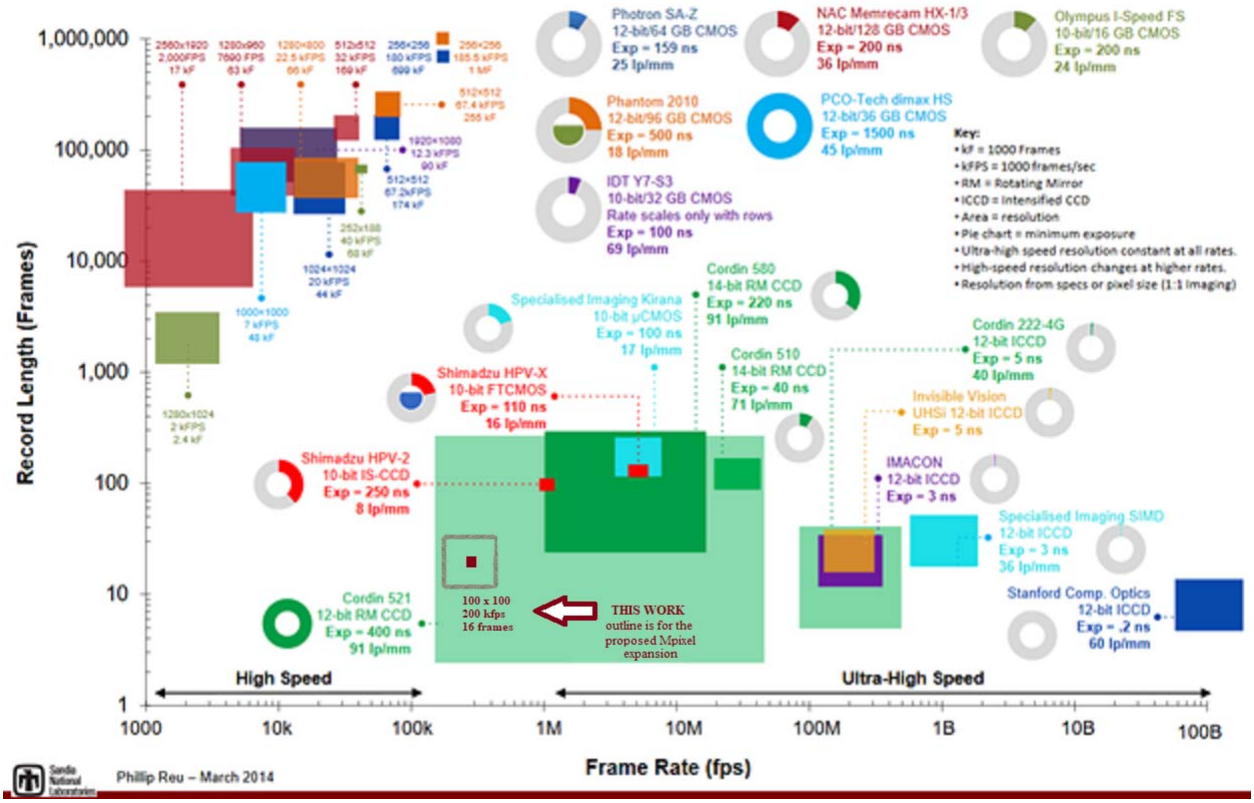

Figure 6: The state of high-speed imaging [27], and the sensor presented in this work

The cameras using rotating mirrors are using a rotating mirror to spread the light from the captured scene to a series of sensors mounted on a drum at extremely high rates, while the cameras that use beam-split optical paths, they first split the image into multiple paths and then use image intensifiers to increase the light available in each path. One problem with these cameras is that each of the multiple sensors they use, will have different characteristics and will be seeing a slightly different field of view. This creates the need of a stationary film to be used as reference for each different sensor [29, 30]. Moreover, image intensifiers create significant blurring, and the rotating mirror tends to create vibrations. The calibration of these sensors are very challenging [30].

CMOS image sensors shown in Figure 6 achieve speeds up to 200kfps for 65kPixels sensors, while their speed is limited to 20kfps for a Mpixel sensor. The record length is now thousands to million frames compared to less than 100 of frames recorded by the CCD cameras. Shimadzu's FTCMOS shown in graph can capture 128 frames at up to 5 Mfps speed at the cost of reduced number of pixels (100 kPixels) and consequently small resolution, and the same specs apply for its newer, more light sensitive, FTCMOS2 version of it [31]. The scalability of this sensor (number of pixels) is hard if not impossible because of the 1-to-1 connection between pixels and memories, and because the camera is based on the work presented in [18] and [25] and is expected to have all the discussed problems.

From the above, it is clear that there is no available product to achieve more than hundred thousand frames per second capture speed using the CMOS technology and its discussed advantages, while allowing a sensor with a large number of pixels and consequently high resolution or large Field of View (FOV). This sensor could be used to provide high resolution information to an incident around a single event, which could be used for fragment size and 3D shape determination of fast moving objects.

In this work a Low-Noise Highly-Sensitive Global-Shutter image sensor with on-Chip Memory is designed in standard CMOS with pinned photodiode process and tested for high-speed applications. This sensor can be expanded to a Mpixel sensor operating at hundreds of kiloframes per second in burst-mode.

CHAPTER 4: IMAGE SENSOR DESIGN

4.1 CONVENTIONAL 4T PIXEL

The image sensor is using a Pinned Photodiode (PPD) light-sensitive element. The pinned photodiode structure uses a shallow p+ layer on top of an n-well layer of a traditional pn junction photodiode. The n-well is "sandwiched" between the p+ layer on top and the p epi layer underneath. The top p+ layer and the underlying p epi are connected using a surrounding p-well and both p+ and p epi are grounded. A transfer gate (TG) and floating n+ in p-well diffusion (FD) are added to the basic pinned photodiode (PPD) structure to implement charge transfer from the PPD to a FD storage node. A cross-section of a 4T Pixel using X-Fab's PPD device is shown in Figure 7.

The main advantages of the PPD as compared to a standard pn junction are reduced dark current, lower noise, and increased quantum efficiency. Another advantage of the PPD is the inherent gain associated with the charge transfer from the PPD to the Floating Diffusion (FD) which is important for low light or high-speed applications. Conversion gain is inversely proportional to the parasitic capacitance of the FD node and is calculated according to equation (1) [32].

$$CG = \frac{q}{C_{FD}} \tag{1}$$

Where q is the elementary charge (1.602×10^{-19} coulombs) and C_{FD} is the capacitance at the input of the charge detection node (input of the source follower).

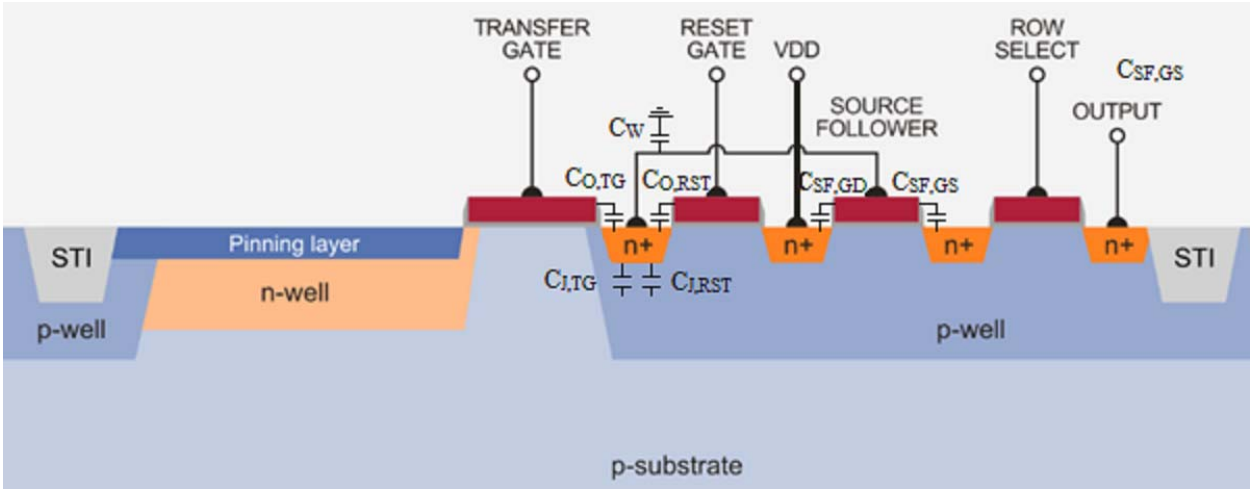

Figure 7: X-Fab 4T PPD pixel cross-section [33], including the different parasitic elements that are used for the Floating Diffusion (FD) capacitance calculations

4.1.1 FLOATING DIFFUSION CAPACITANCE

The FD capacitance can be calculated using the following equation:

$$C_{FD} = C_{O,TG} + C_{J,TG} + C_{O,RST} + C_{J,RST} + C_W + C_{SF,GD} + (1 - A_{SF}) \times C_{SF,GS} \quad (2)$$

The capacitances used to calculate the FD capacitance are described below.

$C_{O,TG}$ is the Transfer Gate overlap capacitance and is equal to (C_O x W_{TG}) , where W_{TG} is the dimension of the Transfer Gate's edge that overlaps the source of the TG, and C_O is the NMOS gate to source/drain overlap.

$C_{J,TG}$ is the transfer gate diffusion capacitance and is equal to ($C_{JA,TG}$ + $C_{JSW,TG}$) , where $C_{JA,TG}$ is the bottom area capacitance of the Transfer Gate's source implant (C_{JA} x L x W), $C_{JSW,TG}$ is the sidewalls capacitance of the same implant (C_{JA} x (2L_{TG} x W_{TG})).

$C_{O,RST}$ is the RST Gate overlap capacitance and is equal to (C_O x W_{RST}).

$C_{J,RST}$ is the RST Gate diffusion capacitance and is equal to ($C_{JA,RST}$ + $C_{JSW,RST}$ + $C_{JGE,RST}$), where $C_{JGE,RST}$ is the gate edge diffusion capacitance (C_{JGE} x W_{RST}).

C_W is the parasitic capacitance related to the metal wires.

$C_{SF,GD}$ is the gate to drain capacitance of the Source Follower (SF). Since the SF operates in saturation when electrons are read from the Pinned Photodiode, the gate to drain capacitance is equal to (C_O x W_{SF}) [34].

$C_{SF,GS}$ is the gate to drain capacitance of the SF, and is equal to (2/3 x C_{OX} x W_{SF} x L_{SF}), when operating in saturation [34].

As can be seen in equation (2), the input capacitance of the SF is equal to ($C_{SF,GD}$ + (1 – A_{SF}) x $C_{SF,GS}$, where A_{SF} is the gain of the SF. To get this formula we can use the following equations as described in [34]:

$$Q_{IN} = \Delta v_{IN} \times C_{GD} + (\Delta v_{IN} - A_{SF} \times \Delta v_{IN}) \times C_{GS} \quad (3)$$

$$C_{IN} = \frac{Q_{IN}}{\Delta v_{IN}} = C_{GD} + C_{GS} \times (1 - A_{SF}) \quad (4)$$

From the above, it is clear that in order increase the Conversion Gain we have to reduce the FD capacitance. And since, the capacitances related to the RST switch and the SF NMOS cannot be reduced, assuming that we are using minimum size devices, the easiest way to increase our gain is through careful design of the Transfer Gate.

There are 3 predominant designs for the transfer gate (TG) of the pinned photodiode: the bottom, the u-shaped and the central (see Figure 8). The central TG design is the best as far as lagging and conversion gain is concerned but it may reduce the fill factor and have more parasitics than u-shaped TG. For small pixel sizes (less than 10um x 10um active area), lagging is not an issue. Transfer times of 60 ns and less have been demonstrated in [35] for large 50um pixels with virtually no image lag.

In our case, where the number of photons is small, the conversion gain is one of the most important factors, when it comes to deciding the pixel design, because it provides noise free gain. However, we also want to keep the fill factor as high as possible and at the same time keep the parasitics low. Hence, the u-shaped TG will be the choice for this work.

X-FAB, the foundry that will be used for the image sensor presented in this work, has a special device, called ne3tx, to be used as a transfer gate when laying out the PPD. Unfortunately, they have not released a model for this specific device in their PDK yet, so extracting the layout to get a value for the FD node capacitance is not an option. However, the method described in the previous pages can be used to calculate the FD capacitance, and has be proved to be accurate according to previous XFAB customers . To calculate the diffusion capacitances of the TG, only the bottom and sidewalls capacitances are added up, and the gate edge capacitance is omitted. This is because, according to the foundry, the junction is to p-substrate, so it is expected to be small. Moreover, previous customers of the foundry that used the same process and the same transfer gate, have verified that the estimation method described above is giving a capacitance which is very close to the capacitance they measured after testing.

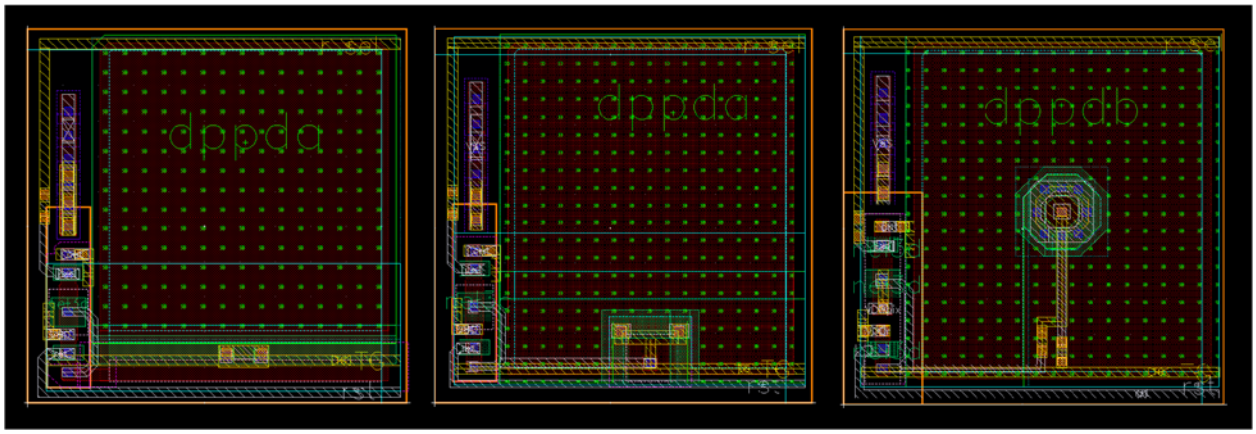

Figure 8: Bottom, u-shaped and central transfer gate pixel designs (left to right)

The diffusion capacitances are nonlinear and depend on the bias of the junction node. The capacitance at different bias voltages can be calculated using the following formula [34]

$$C_J = \frac{C_{j0}}{\left[1 - \frac{V_D}{V_{bi}}\right]^m} \tag{5}$$

where C_{j0} is the zero-bias capacitance of the junction, which is the capacitance when the voltage across the junction, V_D, is zero. V_{bi} is the area or sidewall junction potential, and m is the area or sidewall grading coefficient.

In the FD capacitance calculations, the capacitances that depend on the bias are $C_{J,TG}$ and $C_{J,RST}$.

Table 1 summarizes the FD capacitance and the corresponding conversion gain for three different transfer gate designs. It also gives the capacitance and the resulting gain at 2.3V, which is closer to where our FD will be operating. The fill factor for a pixel 15.1um x 15.1um with 10um x 10um active area, which are the sizes for the pixel that will be used for this work, is also calculated for the three different gates, assuming that the active area is only limited by the choice of transfer gate and the resulting wiring.

	TG		
	Bottom	**U-shaped**	**Central**
Zero bias C_{FD} [fF]	13.560	5.034	5.344
Conversion gain [uV/e^-]	11.799	31.785	29.942
C_{FD} @2.3V [fF]	10.868	4.525	4.998
Conversion gain @2.3V [uV/e^-]	14.722	35.362	32.010
Fill Factor [%]	39.9	41.6	41.1

Table 1: FD capacitance for various transfer gate designs, and the expected fill factor for a 15.1um x 15.1um pixel with 10um x10um active area

As can be seen in the table above, the U-shaped Transfer Gate has the largest conversion gain together with the largest fill factor. And since image lag is not expected to be a problem for a small pixel size, it is selected for the pixel in this work.

4.1.2 NOISE IN CONVENTIONAL 4T PIXEL OPERATION

Figure 9 shows the schematic of a conventional low noise CMOS image sensor read out chain. The timing diagram of this read out chain and the noise mechanisms affecting it are shown in Figure 10. During the integration (exposure), the PPD accumulates electrons generated by the incident photons. During the readout, the pixel is connected to the column through a Row Selection switch and the Reset switch is turning ON in order to set the potential of the Floating Diffusion node (Sense node (SD) in this figure) higher than the pinning voltage of the PPD. The higher the difference in potential between the V_{RST} and the pinning voltage of the PPD, the faster the transfer of the electrons in the transfer stage later on. The voltage level at the Floating Diffusion node, after the reset, is sampled at the end of the read out chain and then the Transfer Gate, which controls the barrier between the PPD and the FD node, goes ON to start the charge

transfer of the accumulated electrons from the PPD to the FD. After this transfer is completed, the voltage level at the FD node is sampled again at the end of the chain. The reset and transfer samples are then differentiated and this is called Correlated Double Sampling (CDS).

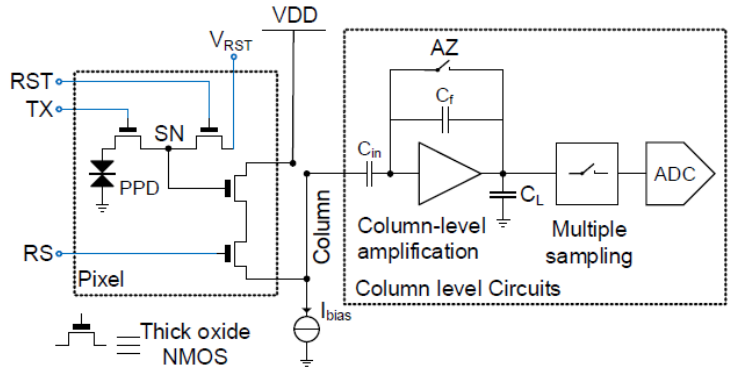

Figure 9: Schematic of conventional low noise CMOS image sensor readout chain [36]

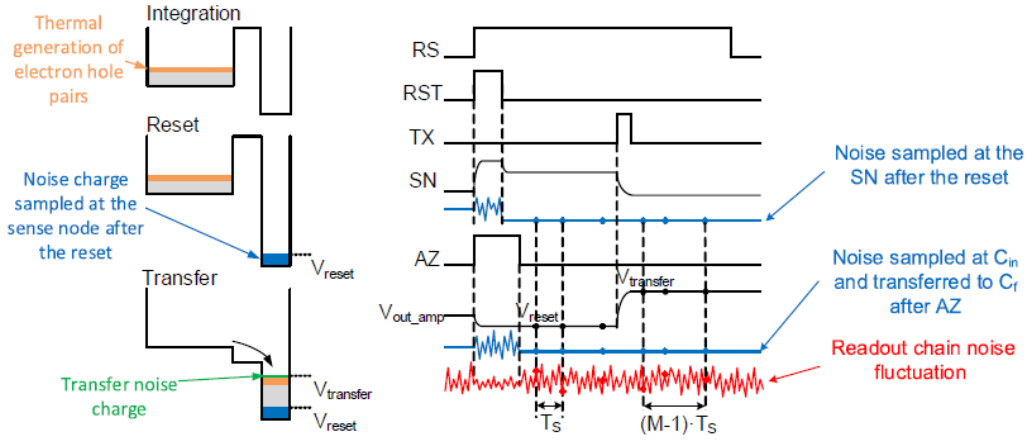

Figure 10: Timing diagram of the read out chain of a conventional low noise CMOS image sensor and the noise mechanisms affecting it [36]

With CDS, the kT/C noise at the FD node because of the reset, is canceled. And this is important, because this noise is high due to the small capacitance at the FD node. Moreover, in state-of-the-art CMOS image sensor the dark current in PPD has been reduced to a few e^- / s, so it can be neglected for exposures below hundreds of ms [36].

4.2 IMAGE SENSOR ARCHITECTURE

A conventional 4T pixel CMOS image sensor with conventional readout architecture does not allow high frame rates for high pixel count (Mpixel) sensors. Moreover, to capture high speed phenomena without any rolling shutter artifacts a Global Shutter sensor is needed. To understand better the need for the Global Shutter scheme, the following example is given.

Assume that a 1000x1000 (1Mpixel) image sensor is read by 1000 parallel 2.5 Msamples/second ADCs and a Rolling Shutter scheme is used. Then the row readout time would be 400ns (= 1 / 2.5M) and the exposure of the last row would start 400us after the exposure of the first row. This would make the sensor useless for capturing high speed phenomena that need only a few us exposure times. For example, a 3,000 m/s moving object would have moved 1.2m between the exposure of the first and last row. The above ignores completely the need of CDS, which could double the time difference between the exposure of the first and last row.

If for the same sensor architecture described in the previous example, a Global shutter scheme is used, the maximum achievable frame rate would be limited by the speed of the ADC, and the RC delays of the pixels output wires. Assuming that the readout speed in each column is again 2.5 Msamples/second, the frame rate is limited to 2.5M / 1000 = 2.5kfps. Even for a sensor readout speed of 10 Gpixel/s, using the most advanced readout techniques, the maximum achievable frame rate is 10G/1M = 10kfps for a Mpixel image sensor.

From the above, it is clear that a global shutter scheme is needed, but a high frame rate cannot be achieved using conventional readout schemes. In order to increase the frame rate to hundreds of thousand frames per second, on-chip memory has to be used. In this work each pixel

has a dedicated on-chip memory block that has 16 analog memories, which are used to save 15 consecutive frames at a very high frame rate and a frame for calibration purposes.

These memories will be on-chip but outside the pixel area. That way the fill factor of the pixel is not reduced. Moreover, fifty pixels share one metal line, resulting in 2 lines per column for a 100x100 image sensor. The control signals are global, meaning that all pixels integrate the light and store the related information simultaneously, but since 50 of them share a line, they transfer their locally stored light information to the analog memories at 50 different time slots. The reason we choose to connect multiple pixels on a single line is space (fill factor). The limiting factor of how many pixels connect to one line is time (frame rate).

When reading from memory, first the common lines in each memory block are reset, to avoid dependency on previous readings due to charge sharing. Similar with the pixel array, 50 memory blocks share a line, and from there the stored values are read by the ADC.

It should be noted that the shared line used to read from the pixels is different from the shared line used to read from the memories. In this design, the blocks that share a line from the pixel also share a read-out line. That way, the chip can operate easily in both continuous and burst mode as needed.

In Figure 11, the architecture of the image sensor developed in this work is shown. Each ADC sees a pair of 50 pixel/memories set, that work in parallel when writing from pixels to on-chip memories, and in series when reading from memories. That way, the architecture can be expandable to a Mpixel size sensor, where the time between frames will be the settling time needed to write from the 50 pixel sets to their dedicated memories. A 1000 x 1000 pixel

architecture would consequently use 40 ADCs (both up and down) and each column would have 10 lines connecting pixels to memories. More about that will be discussed in CHAPTER 8.

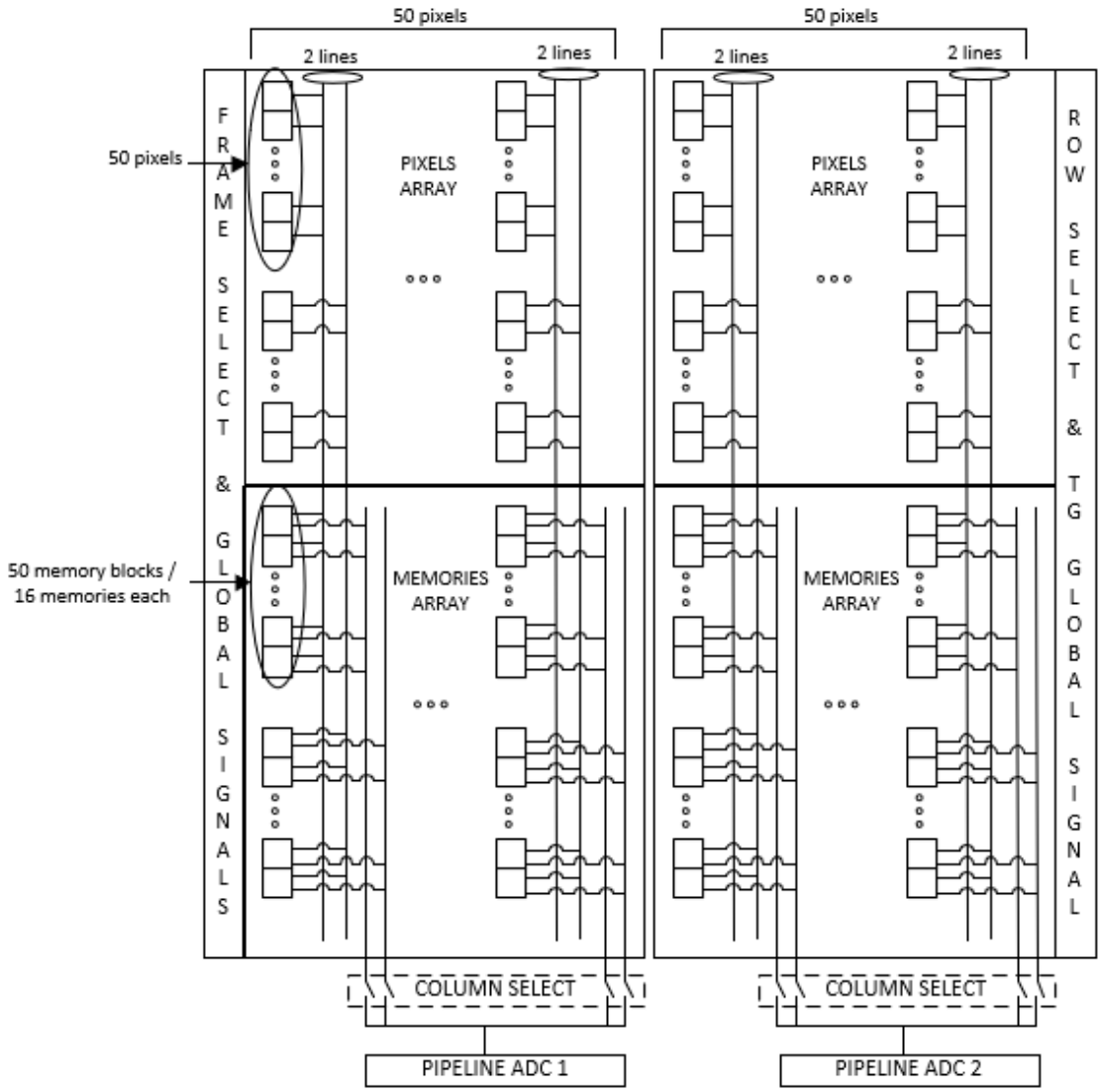

Figure 11: Image sensor architecture in this work

4.3 ON-CHIP CAPACITORS

Capacitors are used in-pixel to allow Global Shutter Behavior and Correlated Doubling Sampling. Moreover, capacitors are used for the dedicated to each pixel memory blocks that are used to save up to 16 frames at very fast frame rate. All this capacitors are chosen to be linear, for a large operation swing and at the same time be area efficient. Since the top metal layers have to be used for the routing of signals, the power supplies and the connection between pixels, memories and ADCs, Metal Insulator Metal (MIM) capacitors are not be the capacitors of choice for pixels and memory blocks. However, they are used for the ADCs, where the physical design is not that tight, because of their higher linearity.

Table 2 summarizes the different options for MIM and MOSFET capacitors that are available in the 180nm process that is used for this work. The capacitance is calculated for a 2um x 2um device size. Figure 12 illustrates the capacitance of the capacitance of the different available capacitors. In green are the capacitors used in-pixel and for the memory blocks.

Capacitor Type	Capacitance (fF)	Leakage Current (fA)
Single MIM	5.36	0.2
Single MIM (high)	11.05	20
Double MIM	10.72	0.2
Double MIM (high)	22.10	20
Triple MIM	16.08	0.2
Triple MIM (high)	33.14	20
Accumulative MOS (1.8V)	33.20	0.516
NMOS (1.8)	33.84	-
Accumulative MOS (3.3V)	**20.00**	**0.386**
Low threshold MOS (3.3V)	**21.16**	**-**

Table 2: Capacitance and leakage current for a 2um x 2um capacitor in the used 180nm process and the drain leakage currents for 2um width devices

(in bold are the capacitors used for the pixels and the memory blocks)

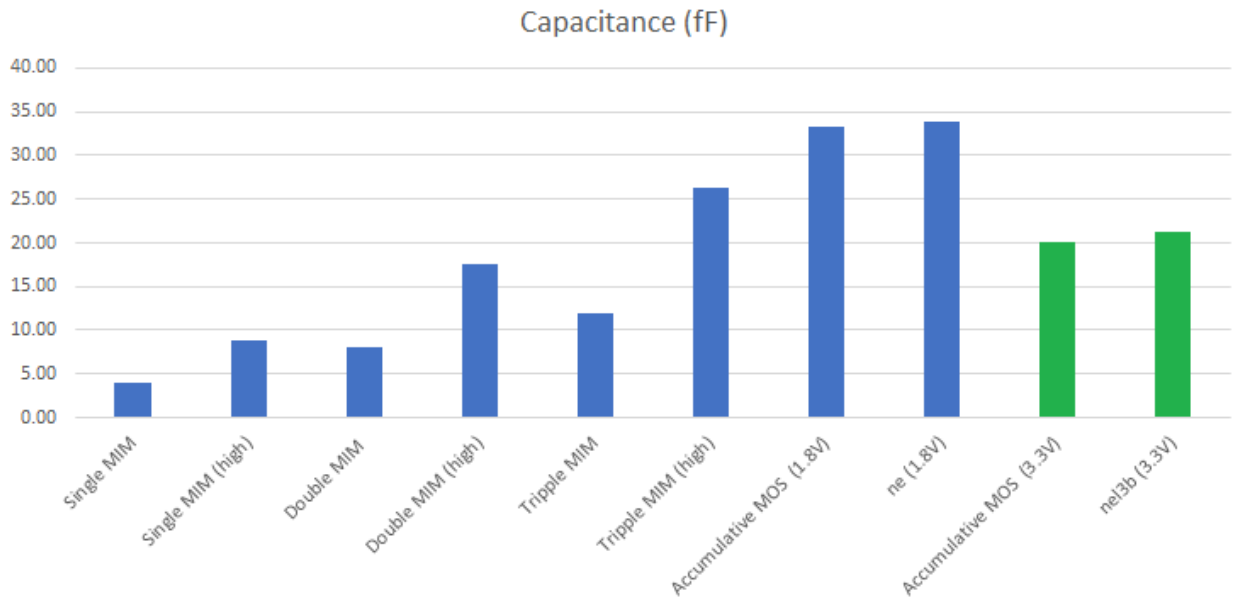

Figure 12: Capacitance of different 2um x 2um capacitors in the used process (in green are the capacitors used for the pixels and the memory blocks)

The capacitors chosen for this work are 3.3 MOSFET devices, and as can be seen from the table and graph above, the have less capacitance only from high capacitance triple MIM and the 1.8 MOSFET devices. The high capacitance triple MIM capacitor has a relatively high leakage current (about 3mV voltage drop for a 60fF capacitor in 10ms), but the main reason it is not selected is because it fully occupies 3 metal layers that can be used for routing. The leakage levels for the MOSFET capacitors are negligible (below the noise level for 10ms readout time). The reason that the 1.8 V devices are not selected for this work is that they cannot hold values higher than 1.8 V. In pixel capacitors have to hold values higher than 1.8 V. Memory block capacitors, although they are designed to hold values less than 1.8V they may see values higher than that, because of fast transients, user errors, or ESD events. Hence, the safest and more area efficient choice for capacitors are the 3.3 V accumulative MOSFET and low threshold MOSFET capacitors.

The variation of the gate capacitance of the devices used in the pixel and in the memory blocks with respect to the gate-source (VGS) voltage can be seen in Figure 13. As can be seen, in-pixel capacitances will be around 67fF, analog memories will be around 60fF, and they will all be linear for the range of operation.

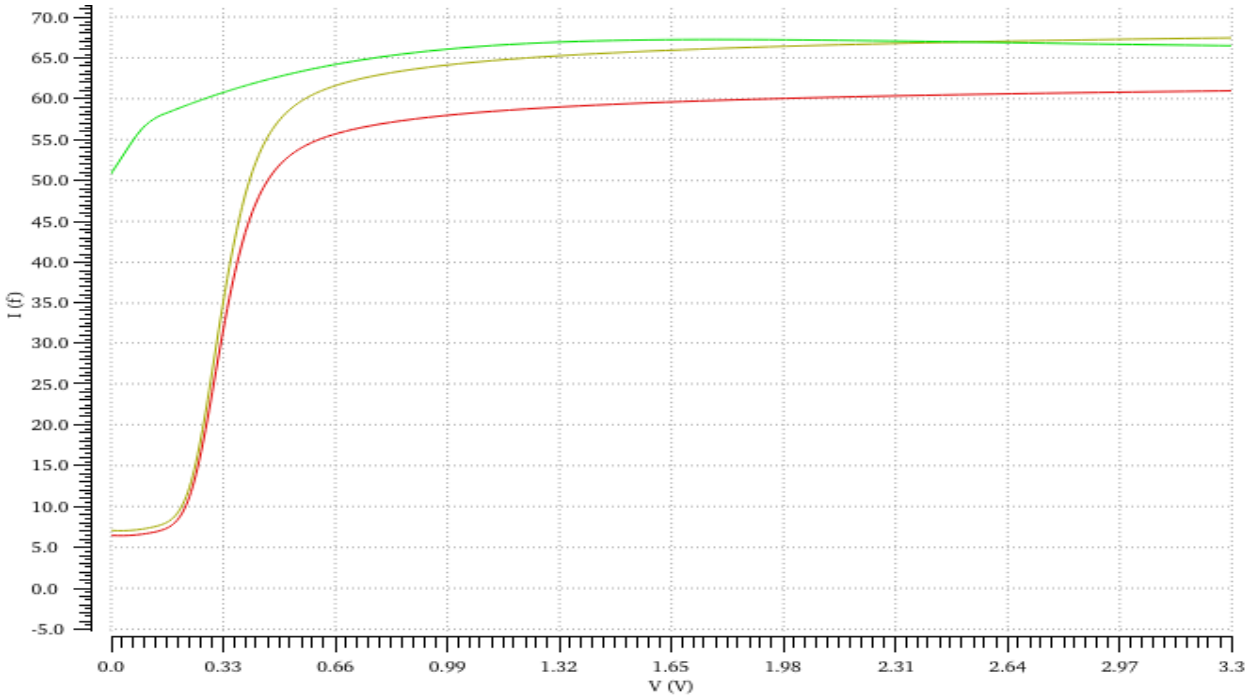

Figure 13: Variation of the gate capacitance with gate-source (VGS) voltage.
(in-pixel: SH capacitor {yellow}, CC capacitor {green} | memory blocks: analog memory {red})

The reason that we used the accumulative MOSFET for the in-pixel coupling capacitor, is because we want it to operate in the linear, or close to linear range from lower values. As can be seen in the figure above, for 200mV VGS the CC capacitor is already at more than 90% of its linear capacitance value. This capacitor, since it has an NWEL, it is surrounded by a guard ring to avoid latch-ups. The NMOS capacitors do not have this need for guard ring, and are the capacitors of choice for the in-pixel Sample and Hold capacitor and the analog memories.

4.4 PIXEL DESIGN

A 5-T (5 transistors) PPD pixel (Figure 14) separates the exposure from the transfer period and allows Global Shutter behavior. However, it cannot eliminate the reset noise because of the lack of the CDS operation. Therefore, a 5-T pixel is not a good choice for a low noise, Highly Sensitive image sensor.

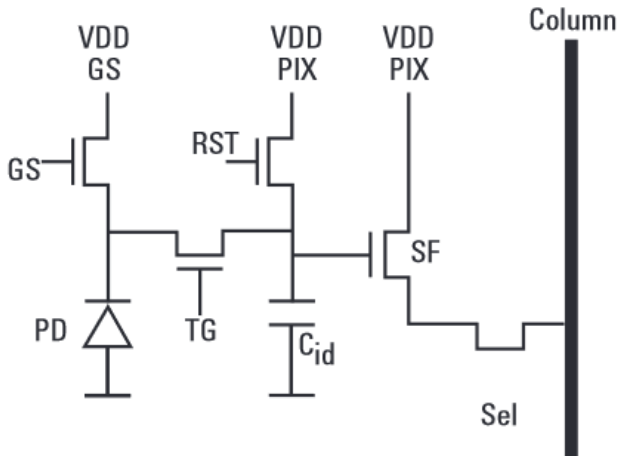

Figure 14: Xensium-FT CMOS imagers 5-T pixel [37]

To reduce the noise in a global shutter scheme, CDS is necessary and it has to be in-pixel for a global shutter operation. In-pixel CDS has been presented in [18], [25] and [26] and discussed in CHAPTER 2. In this work, a pixel that allows Global Shutter operation and in-pixel CDS is used. The schematic of this pixel can be seen in Figure 15. The presented pixel incorporates two stages: the Reset and the Exposure stage. The timing diagram of the pixel operation can be seen in Figure 16. The advantages of this pixel compared to pixels presented in previous work will be discussed at the end of this chapter, after its operation and noise reduction ability have been explained, and its physical design has been justified.

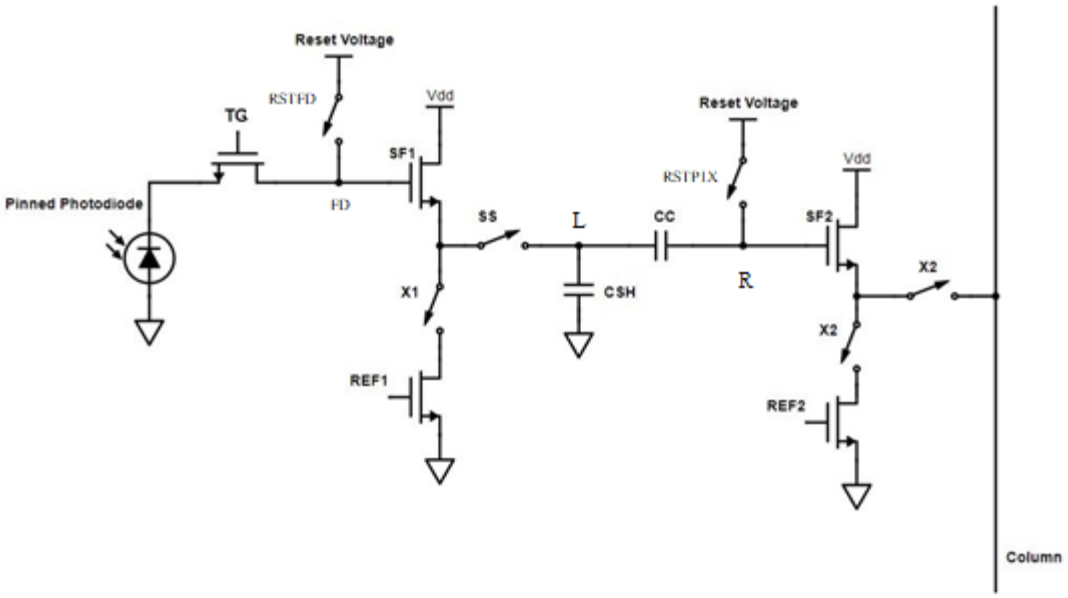

Figure 15: Schematic of the Pixel used in this work

Figure 16: Timing diagram of the pixel operation

During the Reset Stage, the photodiode is reset by turning the transfer gate (TG) ON, while the reset FD switch (RSTFD) switch is also ON. That way, the photodiode will not be holding any electrons at the beginning of the electrons integration stage that will follow, just after TG turns OFF.

During the Exposure (integration) Stage, TG is OFF and the PPD is collecting the electrons generated by the incident photons. The SS and X1 switches are turned OFF until just before the end of the this stage, so that the previous value stored from the previous exposure is not lost before sampling the reset value and the signal value of the current exposure.

Just before the end of the Exposure Stage, we sample first the reset value and then the signal generated by the incident photons during the exposure period. To sample the reset value, the RSTFD switch goes OFF and the SS, X1 and RSTPIX switches go ON. The reset value of the FD including it kTC noise is sampled on the sampling capacitor CSH, while the right side of the coupling capacitor CC is held at a fixed DC voltage. Since SF1 (source follower 1) is operating in saturation during the transfer of the reset signal, the noise at the node at the right of CC (R) will be given by the following equation [26]

$$V_{n,RMS,_R} = \sqrt{\frac{kT}{CC + Cp}} \tag{6}$$

where C_p is the parasitic capacitance at node R.

After the reset signal is sampled, RSTPIX goes LOW and TG goes ON. The FD node goes down because the removal of the potential barrier between PPD and TG (TG LOW) now allows the collected electrons to transfer from PPD to FD and reduce its potential. The output of the source follower follows this movement and the same movement is also seen by the R node at the right of the coupling capacitor. The noise at node R will be given by the following equation

$$V_{n,RMS,_R} = \sqrt{\frac{kT}{CSH + \frac{CC \times Cp}{CC + Cp}}} \times \frac{CC}{CC + Cp} \tag{7}$$

In the presented design CSH and CC are 67fF, while the parasitic capacitance at node R is about 5fF. Hence, the total kTC RMS noise at the node before the second source follower (node R) is about 0.33mV (330uV) at room temperature. In that we have to add the flicker noise from the first and second source followers, which have input referred flicker noise 10uV*um/√Hz and 804.5Hz corner frequency. Their RMS flicker noise is calculated to be 55uV and 16uV respectively. Assuming the source followers have gain close to 1 and since $\frac{CSH}{CSH+Cp} =$ 0.93, the total noise at node R is $\sqrt{330^2 + (55 * 0.93)^2 + 16^2} = 334uV$, which is very close to the calculated thermal noise. For a Conversion Gain of 35uV/e^-, the noise from the pixel operation is equal to the charge of about 10e^-.

From the above, it is clear that the output of the pixel will not include the kTC noise of the FD reset value, which would be high because the parasitic capacitance of the FD node is on purpose small, and the threshold variations of the first source follower. In-pixel CDS can be performed in a single read out. However, the drawback of a single read out is that the threshold voltage variations of the second source follower will not be cancelled out. That is why the reset value at the input of the second source follower will also be stored in one of the on-chip memories for calibration purposes.

Pixel source followers have in-pixel current sources with switches to turn them off when not in use. The use of in-pixel current sources for the source followers that drive the signals to the memories instead of in-column current sources, ensure that the output will not be affected by the distance between the pixel and the current source. The source follower design has been done carefully, so that the image sensor has good linearity and can operate at high frame-to-frame speeds, both for the design presented in this work and the proposed Mpixel expansion.

The switches are necessary for the operation of the 10 kpixels sensor but will be even more important for the Mpixel expansion. All source followers 1 (output of the FD) are on at the same time during the writing to the on-chip memories operation of the sensor, and more specifically they turn ON, just before the sampling of the reset and the signal from the PPD in pixel. The current through each current source is 5.77uA and the total current drawn from them operating together is 57.70mA (10 kpixels). The current from 1 million pixels storing their values together would be 5.77A. This value maybe high and could be reduced by using techniques that will be discussed in CHAPTER 8.

After the signal values are stored, all pixels in a row start transferring their stored values to their dedicated memory blocks, and this happens simultaneously row by row. All the pixels from one every fifty rows (2 rows for the 10kpixel or 20 rows for the Mpixel expansion) transfer their values at the same time. The current through each of the current sources for the pixels output source followers is 99.18uA, and the total current drawn from them operating together is 19.84mA for the 10kpixels sensor and 1.98A for the Mpixel expansion. More about the Mpixels expansion in CHAPTER 8.

The linearity of the in-pixel source followers is affected by this switching operation minimally, as can be seen in Figure 17 and Figure 18. The gain of the in-pixel source followers could be closer to one if a triple well process was used, but the benefits of the increased linearity would be of no use since the fill factor of the pixel would be drastically decreased, because of the use of deep NWELL devices to eliminate the body effect.

The total gain of the pixel is expected to be

$$A_{pixel}\left[\frac{V}{V}\right] = A_{SF1} \times A_{SF2} \times \frac{CC}{CC + C_p} = 0.915 \times 0.93 \times 0.93 = 0.79 \qquad (8)$$

or in terms of electrons

$$A_{pixel}\left[\frac{uV}{e^-}\right] = A_{pixel}\left[\frac{V}{V}\right] \times CG = 0.79 \times 35\frac{uV}{e^-} = 27.65\frac{uV}{e^-} \quad (9)$$

where CG is the calculated Conversion Gain for the designed pixel.

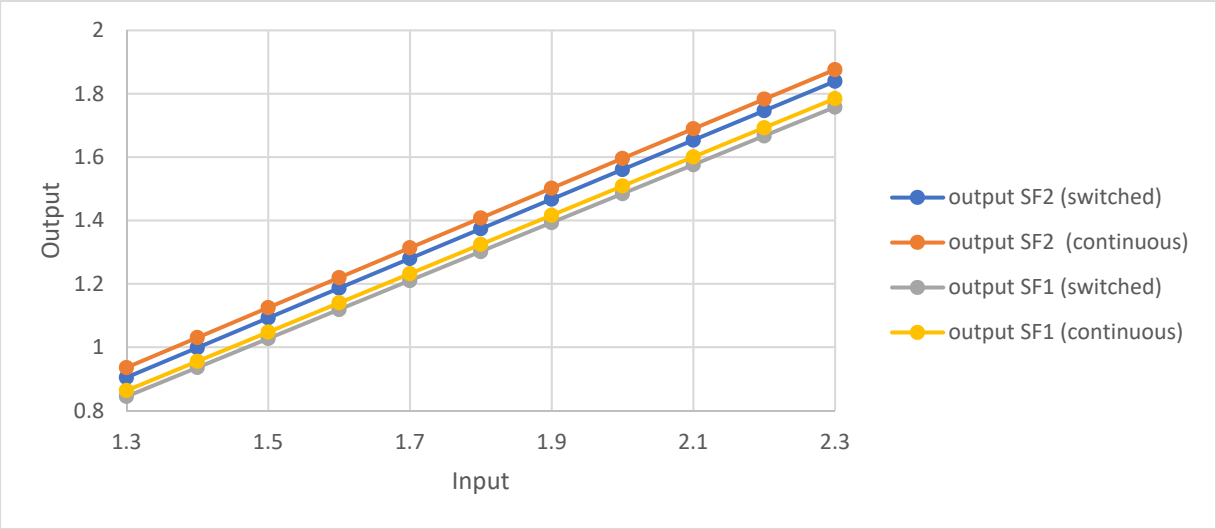

Figure 17: Output vs Input of the in-pixels source followers with or without switches

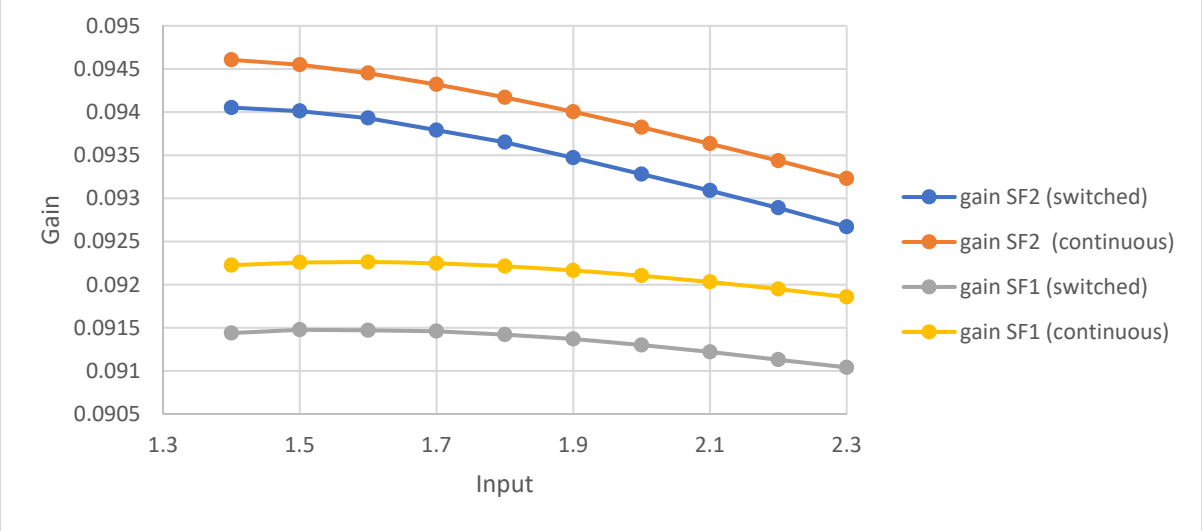

Figure 18: Gain vs Input of the in-pixels source followers with or without switches

The transient response of the source followers used in pixel can be seen in the following figures. The switches, the parasitic resistances, the parasitic capacitances of lines and devices and the capacitances of the devices have been used as their load.

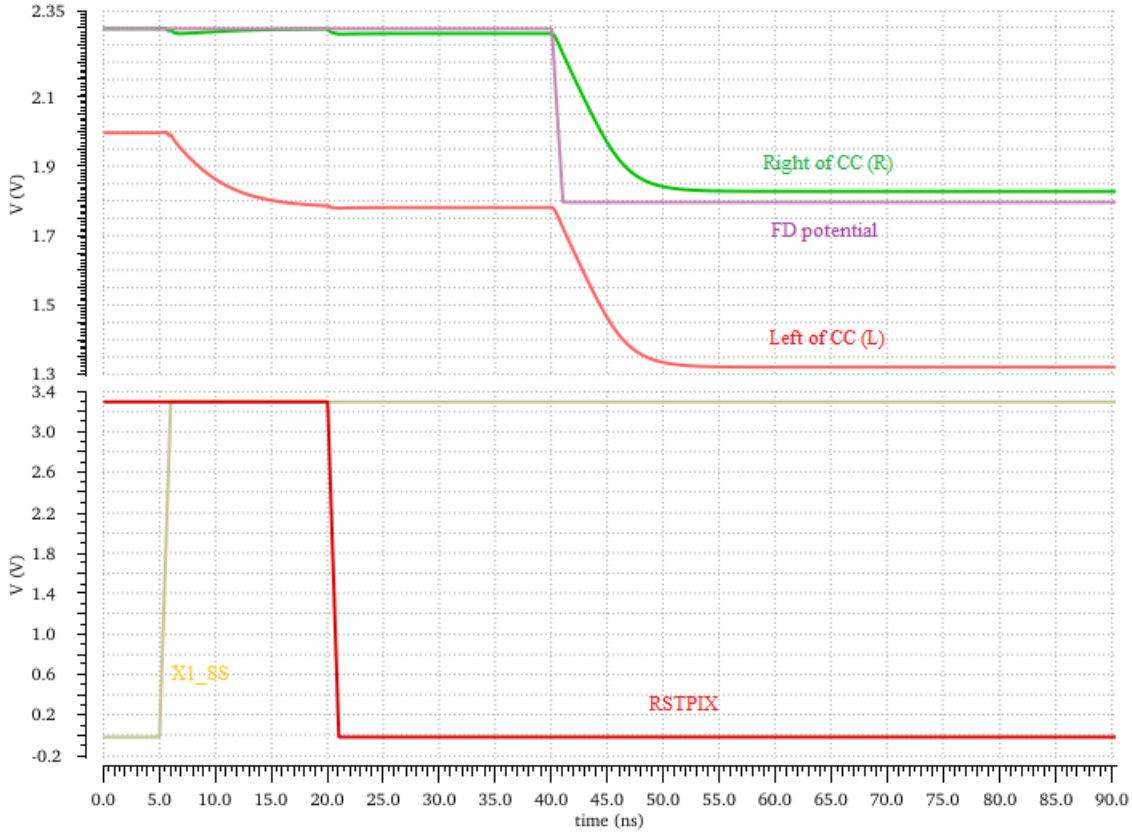

Figure 19: Transient response of SF1

From Figure 19, for 12 bits accuracy (difference from the settling value less than $1.8/2^{12}$), the settling time from the input of SF1 to the input of SF2 is less than 16ns for the transfer of the reset and the signal values. In this work, SS and X1 turn of together and remain ON at least 220ns. RSTPIX goes HIGH together with SS and X1 and remain ON for 100ns, and during this time the CC cap is holding the reset value from both sides. After that, TG turns ON for 100ns to transfer the signal.

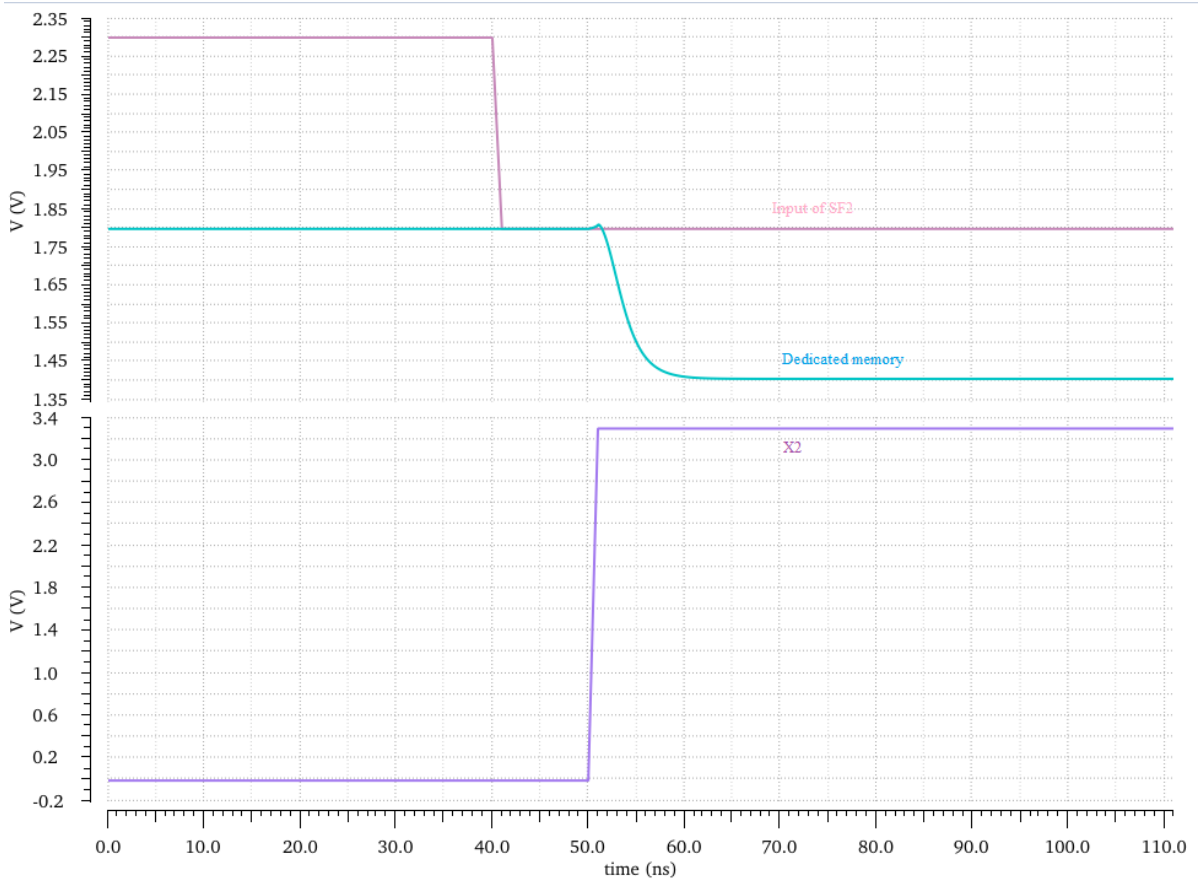

Figure 20: Transient response of SF2 using distances from the presented image sensor

From Figure 20, the settling time from the input of SF2 to the dedicated pixel memory is less than 14ns. In this work the clock for these transfers has a period of 70ns. The total time needed to transfer all 50 rows of pixels to the memories is 70ns x 50 = 3.5us. These transfers can start immediately after SS and X1 switches are turned off, and have to finish because they turn ON again. If we allow some extra time (20ns) before and after the transfers, the minimum period of a frame is 3.5us + 0.22us + 0.02us = 3.74us. Hence, with the current setup of signals, the maximum achievable frame rate of the presented sensor is 267 kframes per second, for an exposure smaller than 3.5us.

This frame rate can be even higher for the 10 kpixel sensor if we make the clock for the transfers between pixels and memory blocks faster, 50ns period, which will still be slow enough for 12 bit settling. The resulting frame rate for a 50ns transfer clock would be 360 kframes per second, for an exposure smaller than 2.5us.

However, a 70ns transfer clock would allow enough settling time even for the propose Mpixel expansion of the sensor, and this is why it is used in this work. As can be seen in Figure 21, the settling time from the input of SF2 to the dedicated pixel memory is less than 45ns for the Mpixel sensor. For this simulation the projected capacitances and resistances for the architecture presented in CHAPTER 8 have been used. Therefore, the sensor presented in this work is expected to be able to operate at frame rates higher than 200 kfps, even for the million pixels design.

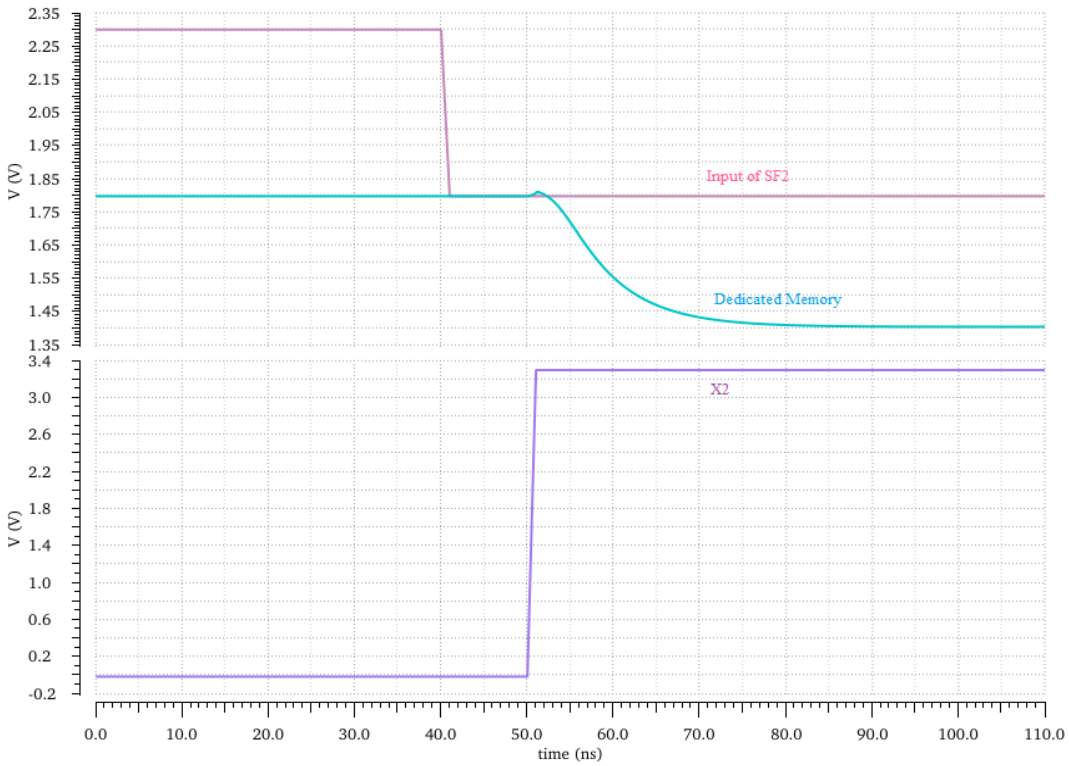

Figure 21: Transient response of SF2 using Mpixel sensor distances

The simulated settling times in Figure 20 and Figure 21 are calculated for the worst case, which is the delay from the last row of the pixels to the last row of the memories. And this is because the height of 50 pixels (15.1um x 50 = 0.755mm) is bigger than the height of 50 memories (26um x 50 = 1.3mm). For example, the distance between the first row of pixels to the first row of memories for the bottom half of pixel/memory sets of the Mpixel would be 0.755mm x 10 = 7.55mm, while the distance between the last rows would be 1.3mm x 10 = 13mm.

In the settling time simulations, the capacitances of the 50 devices at the beginning and the 50 devices at the end of the lines are included. The ON resistances of the switches used in the simulated paths, the analog memory at the end of the path and the parasitic resistances and capacitances of the paths are also included in the simulations.

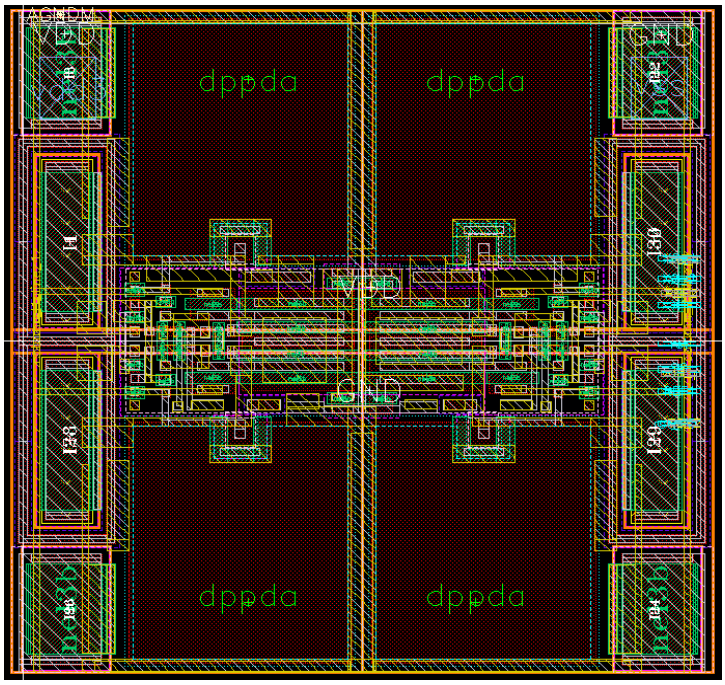

Figure 22: Pixel array's repeating element layout in Cadence

The layout of a set of 4 pixels is used as the repeating element of the designed pixel array and can be seen in Figure 22. The pixel size is 15.1um x 15.1um, the active PPD area is 10um x 10um, and the resulting fill factor is 41.6%. The size of the pixel was chosen to be small, so that more pixels can fit per given area, while the RC delays remain small, but big enough so that the resulting fill factor remains above 40%. All the routing is above the non-active pixel areas and consequently the fill factor is not affected.

A u-shaped transfer gate has been chosen to minimize the floating diffusion capacitance, and consequently increase the conversion gain, keeping the fill factor high at the same time. A pinned photodiode with the lowest available pinning voltage has been selected to allow fast charge transfer, which is crucial for high speed applications, at the cost of a smaller full well capacity, which is not important for low light (short exposure) applications, because of the limited number of the collected photons due to the small integration time.

Six metal layers have been used for routing, so that there is more space between the metal lines and the subsequent coupling capacitances are small enough for high speed operation. Moreover, the active area is minimally shaded, since metal lines can be stacked above the non-active pixel areas. The ability to stack metal lines, because of the multiple metal layers used, will keep the coupling capacitances small enough, so that the sensor can be expanded to a Mpixel sensor operating at hundreds of thousands frames per second, and at the same time will keep the active pixel area minimally shaded.

This pixel design in this work is unique because of the following:

- It is relatively small (15.1um x 15.1um), while achieving the following:
    - Low noise, by performing in pixel CDS using big enough capacitors to limit the RMS noise at the input of its output source follower at about $10e^-$
    - Its output voltage does not depend on the distance between its output source follower and a column current source, since all pixels have dedicated, in-pixel, current sources
    - The active area of the pixel is 10um x 10um, to allow the accumulation of enough electrons in low-light and short exposure conditions and a fill factor greater than 40%
- It uses low threshold voltage, high area efficient capacitors that allow large voltage swing at their not voltage dependent (linear) area of operation. These capacitors are MOSFET capacitors and do not take up space from the upper metal layers (MIM, Metal Insulator Metal capacitors). These layers are used exclusively for the connections between pixels and on-chip memory blocks, for control signals and power supplies
- NMOS source followers are built in a twin well process to keep size to minimum. A triple well process would drastically reduce the fill factor of the 15um pixel used
- In-pixel current sources are driven ON only when needed, so that they can be strong enough to allow fast transfer times even for Mpixels sensor parasitic capacitances and resistances and at the same time they are not creating excessive voltage drops
- The process dedicated capacitors (MOSVC) that are used as coupling capacitors and have an NWELL, are surrounded by a guard ring to avoid latch-ups. All other in-pixel devices do not have an NWELL. This guarantees reliable operation and space efficiency

4.5 MEMORY BLOCKS

The sensor will have the ability to take 16 consecutive pictures. In order to do that, 16 storage capacitors per pixel are needed on chip. For the reasons explained in section 4.3 about on-chip capacitors, the capacitor of choice in this work for the memory blocks is an NMOS MOSFET 3.3V device operating in strong inversion (Figure 23 and Figure 13). Its capacitance at the operation region will be 60fF.

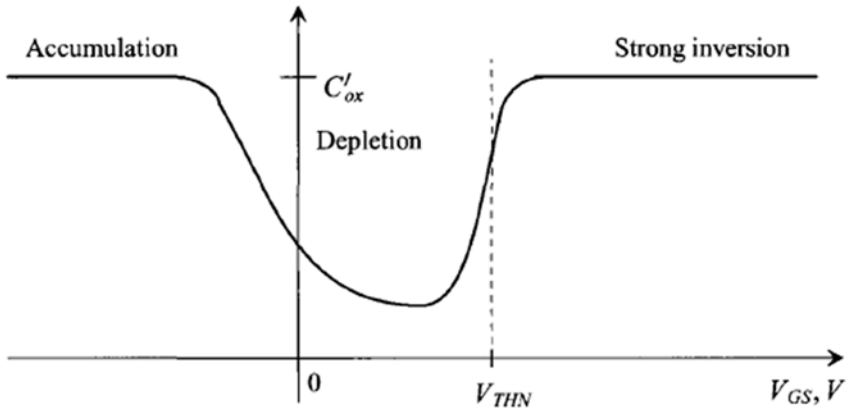

Figure 23: The variation of the gate capacitance with gate-source (VGS) voltage [34]

Each memory block consists of 16 1T1C (1 Transistor – 1 Capacitor) elements, each of which has an NMOS switch and an NMOS capacitor, the required input and output access switches, a reset switch, and a source follower driven by a current source designed inside the block. Similarly to the pixel, a switch turns OFF the source current source when not in use. The schematic of the memory block can be seen in Figure 24 and the layout in Figure 25.

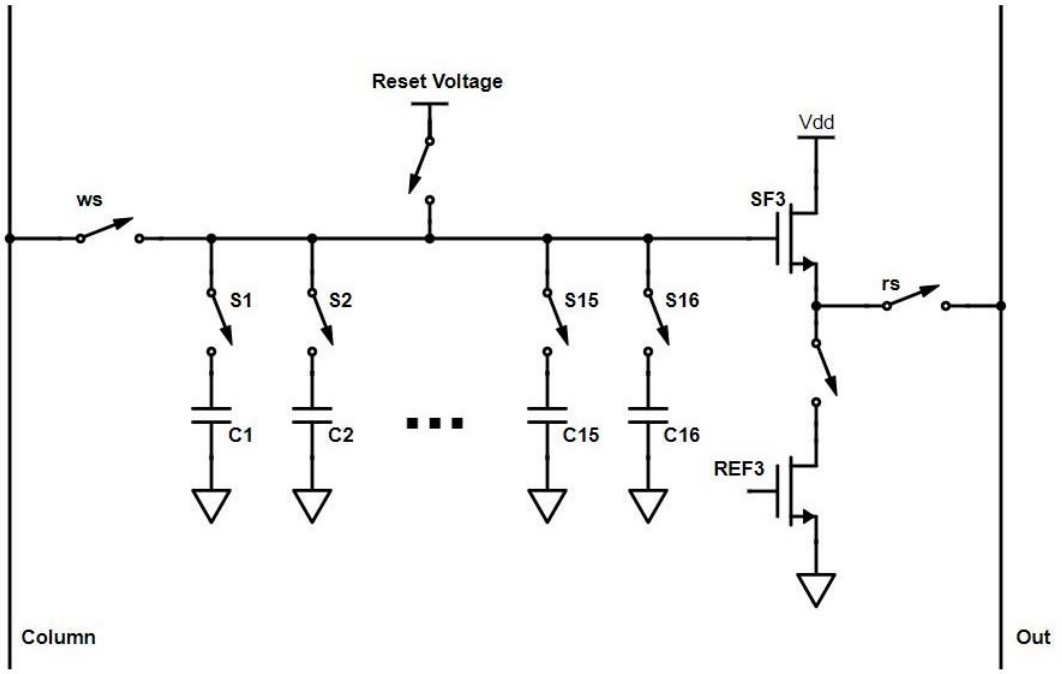

Figure 24: Memory Block schematic

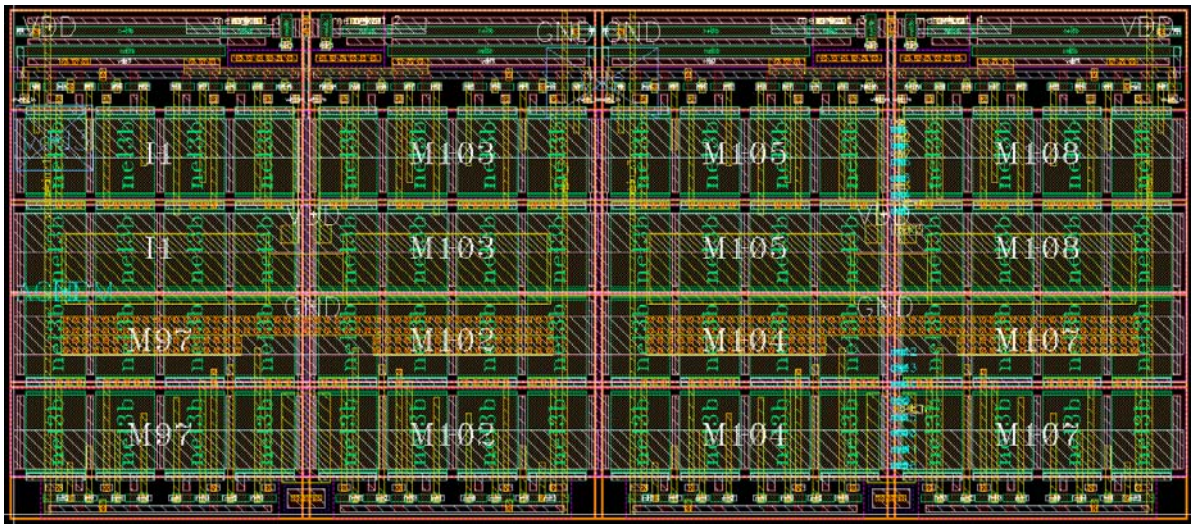

Figure 25: Memories array's repeating element layout in Cadence (4 Memory Blocks)

Every memory block is dedicated to a specific pixel and 50 blocks share a line for their connection to the pixels they read from, resulting into 2 lines per column connecting pixels to memories. Pixel operation signals are global, meaning that all pixels integrate the light and store the related information simultaneously in-pixel. But, since 50 of them share a line (to keep pixel fill factor high), they transfer their locally stored light information to the analog memories at 50 different time slots. In 50 cycles all pixel values are transferred from in-pixel memories to their dedicated memory blocks memories. First frame pixel values are saved in the first memory of each memory block, second frame values are saved in the second and finally last frame is saved to the sixteenth memory of each block.

Each memory block is also connected to a shared line through a source follower that is designed to drive the transfer of the values from the read memory to the input of the ADC. Similar with the connection between pixels and memory blocks, the same fifty memory blocks that share a line with the pixels, share a line with the ADC. This allows the sensor to operate easily in both burst mode, which is the main mode of the camera, and continuous mode, which is a nice feature.

When reading from memory, the lines that holds the 16 1T1C (1 Transistor – 1 Capacitor) elements in each memory block are reset globally before accessing the next memory, in order to cancel any dependency on previous readings. This is important because the parasitic capacitance of the common line in each block is expected to be about 13fF, which is relatively high, compared to the size of the analog memories themselves. The stored values that are read from each memory and transferred to the ADC are changing their values when their access switch turns ON for frame reading, because of the charge sharing of the accessed analog memory

and the parasitic capacitance of the connecting line. The value at the input of the source follower will be:

$$V_{G,SF3} = \frac{C_{mem} \times V_{stored} + C_{par} \times V_{reset}}{C_{mem} + C_{par}} \quad (10)$$

where C_{mem} is the analog memories capacitance (60fF), C_{par} is the parasitic capacitance of the line connecting the memories in each memory block (20fF), V_{stored} is the value at the read memory and V_{reset} is the potential of the line after reset and before reading from the memory.

The resulting gain because of the charge sharing with the parasitic capacitance when reading from memory is given by the following formula:

$$A_{mem,read} = \frac{C_{mem}}{C_{mem} + C_{par}} = \frac{60}{60 + 13} = 0.82 \quad (11)$$

The gain of the source followers used inside the memory blocks can be seen in the following figure.

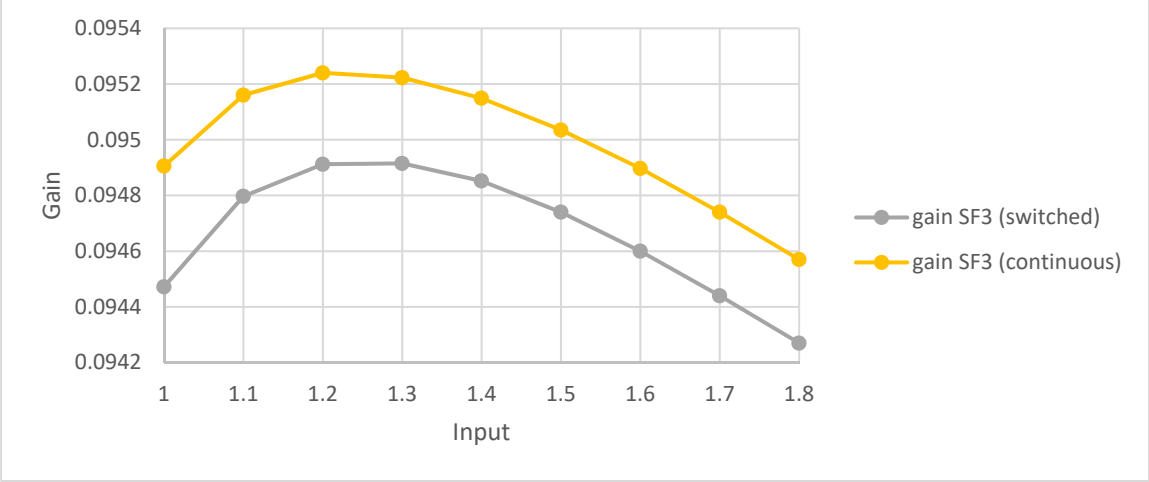

Figure 26: Gain vs Input of the memory block source follower with or without switches

Therefore, the total gain added to the camera because of the memory block is calculated to be:

$$A_{memory} = A_{mem,read} \times A_{SF3} = 0.82 \times 0.95 = 0.78 \quad (12)$$

The complete system gain (before ADC) is now:

$$A_{system}\left[\frac{V}{V}\right] = A_{pixel} \times A_{memory} = 0.79 \times 0.78 = 0.62 \quad (13)$$

Or

$$A_{system}\left[\frac{uV}{e^-}\right] = A_{pixel}\left[\frac{uV}{e^-}\right] \times A_{memory} = 27.65 \times 0.78 = 21.57\frac{uV}{e^-}$$

The transient response of the source follower used in the memory blocks can be seen in Figure 27 (pink is the input of the SF, green is the input of the ADC and grey is the switching signal) . The presented response is for the worst case scenario, or more specifically for the memory block with the greater distance from the ADC. The switches, the parasitic resistances, the parasitic capacitances of lines and devices and the capacitances of the devices have been used as load. For 12 bits accuracy, the settling time to transfer a memory value from the memory block to the input of the ADC is less than 95ns. Hence, the ADC can operate at 10MHz and the readout from all the 16 frames of all the memory blocks of the presented images sensor can be done in 10,000/2 x 16 x 100n = 8ms.

The transient response of the memory blocks source follower in the case of the proposed 1 Mpixel expansion can be seen in Figure 28. The settling time in this case is about 130ns. Therefore, the ADCs could operate at 8MHz and the readout time will be 50ms (= 125ns x 1Mpixels / 40 ADCs x 16 frames).

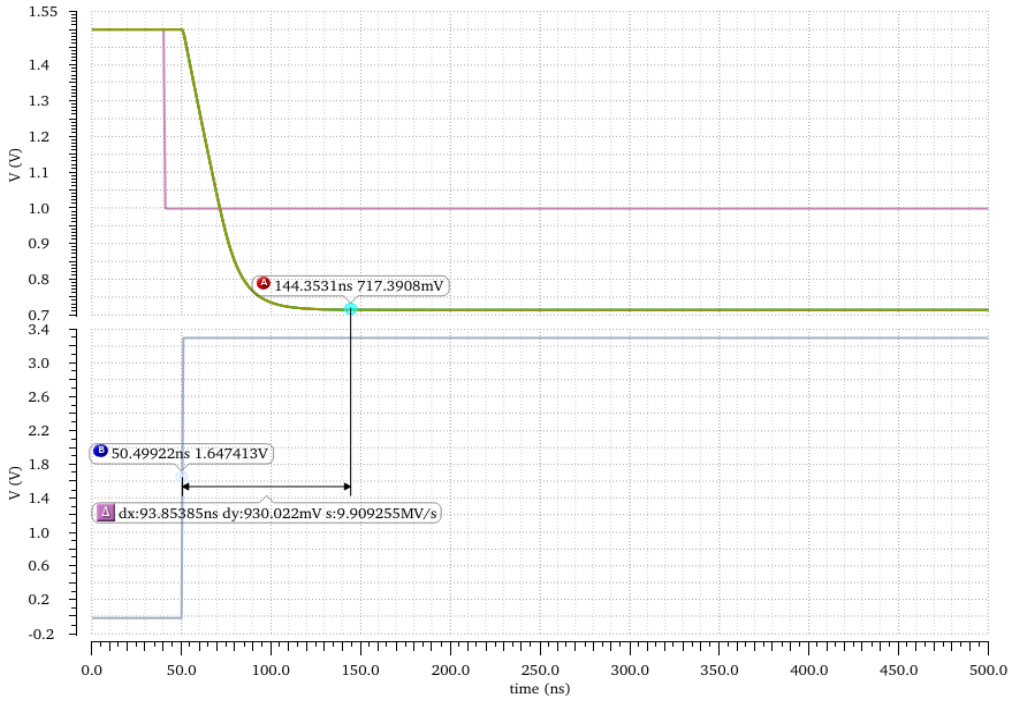

Figure 27: Transient response of SF3 using distances from the presented image sensor

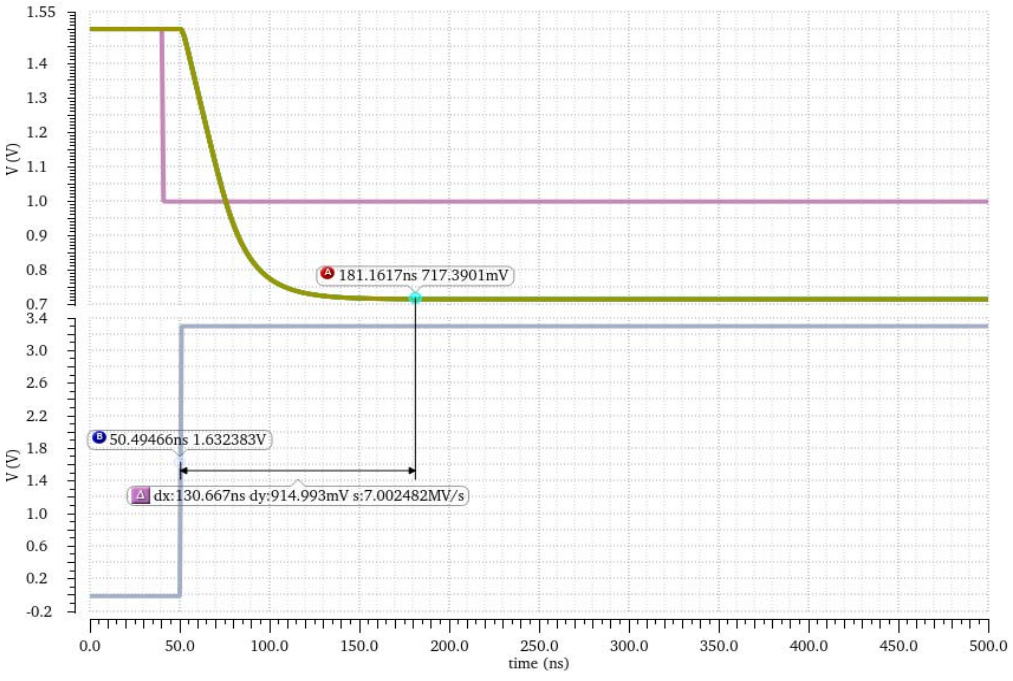

Figure 28: Transient response of SF3 using distances from the proposed Mpixel expansion

Note that the source followers in the memory blocks are directly connected to the input of the ADC. This is not a problem for the 10kpixel design, but it would make the design of a Mpixel expansion of this sensor much easier if a low capacitance buffer was used just before the ADC. That way, the small source followers inside the memory blocks would not have to drive the large input capacitance of the ADC but the smaller capacitance of the added buffer.

All the devices in the memory block are 3.3V NMOS devices. For the access devices in the blocks, this means that 1.8V values can easily be passed, which would be impossible if 1.8V NMOS devices were used instead, and it is something necessary since they are within the operational swing. Moreover, the leakages when the access devices are OFF are much smaller for the 3.3V devices compared to the 1.8V devices.

The access devices used in the 1T1C memories will have a negative VGS when OFF, and their VDS will be less than 1V. Since their off-state leakage is reported to be less than 10fA for VGS = -0.5V and VDS = 3.3V for a 10um wide device, our access devices (0.42um width) are expected to have an off-state leakage much less than 0.42fA. In this current we could also include the PN junction current between the n+ NMOS implant and the PWELL, which is calculated to be around 0.21fA at 27ºC. Note that it would be important to keep the operating temperature low, because for high temperatures the leakages could increase to 92fA @125ºC.

Since our readout time is 8ms the maximum voltage drop due to leakages for this time will be (leakages are in the opposite direction)

$$dV_{due\ to\ leakages} = \frac{I_{leakage} \times t_{max}}{C_{storage}} = \frac{(0.42 - 0.21)f \times 8m}{60f} = 28uV \qquad (14)$$

which is well below the noise and consequently will not affect the operation of the sensor.

The kTC noise at the analog memories is calculated to be 0.26mV rms. Hence, the total rms noise sampled at the analog memory is

$$V_{n,RMS,M} = \sqrt{(V_{n,RMS,R}A_{SF2})^2 + (V_{n,RMS,kTCm})^2} \quad (15)$$

$$= \sqrt{(0.33 \times 0.93)^2 + 0.26^2} = 0.4mV$$

The kTC noise introduced in the system when resetting the common line inside the memory block is $V_{n,RMS,par}$ = 0.564mV, but the total noise that is read from the memories because of the charge sharing between the memory capacitance (C_{mem}) and the parasitic capacitance of the common line (C_{par}) is given by the following equation

$$V_{n,RMS,SF3i} = \frac{\sqrt{(V_{n,RMS,M} \times C_{mem})^2 + \left(V_{n,RMS,par} \times C_{par}\right)^2}}{C_{mem} + C_{par}} \quad (16)$$

$$= \frac{\sqrt{24^2 + 7.3^2}}{73} = 0.344mV$$

The noise that is seen by the ADC is finally

$$V_{n,RMS,TOTAL} = V_{n,RMS,SF3i} \times A_{SF3} \quad (17)$$

$$= 0.344 \times 0.95 = \mathbf{0.33mV}$$

The **input referred noise** is then given by the following formula

$$V_{n,RMS,input\ referred} = \frac{V_{n,RMS,TOTAL}}{A_{system}} \quad (18)$$

= 0.53 mV

= 15.30 e^-

4.6 DIGITAL BLOCKS

The digital blocks that are used in the presented image sensor are shift registers, buffers and inverters. Shift registers are used to select the required row, column, or frame that we want to write to or read from. The main block of the shift registers consists of a positive edge D Flip-Flop with Reset and Set and a low active D-Latch with Reset as seen in Figure 29. Using N of these blocks in series the required functionality of an N-bit shift register is achieved. A 16-bit shift register created using these blocks can be seen in Figure 30.

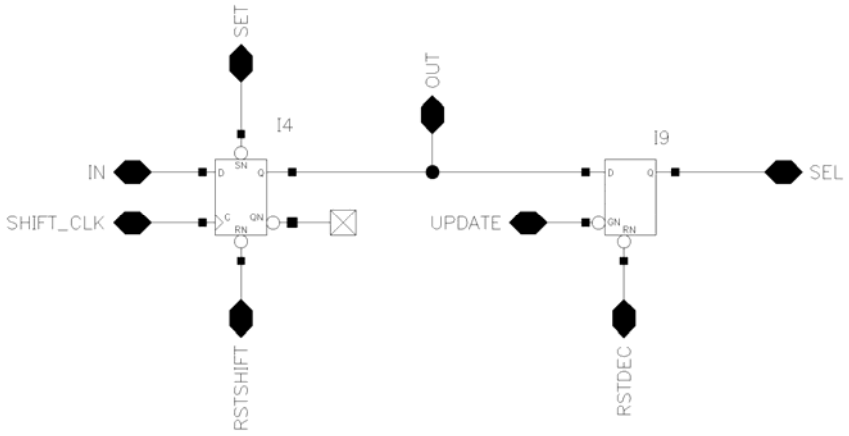

Figure 29: Schematic of the building block of the shift registers in Cadence

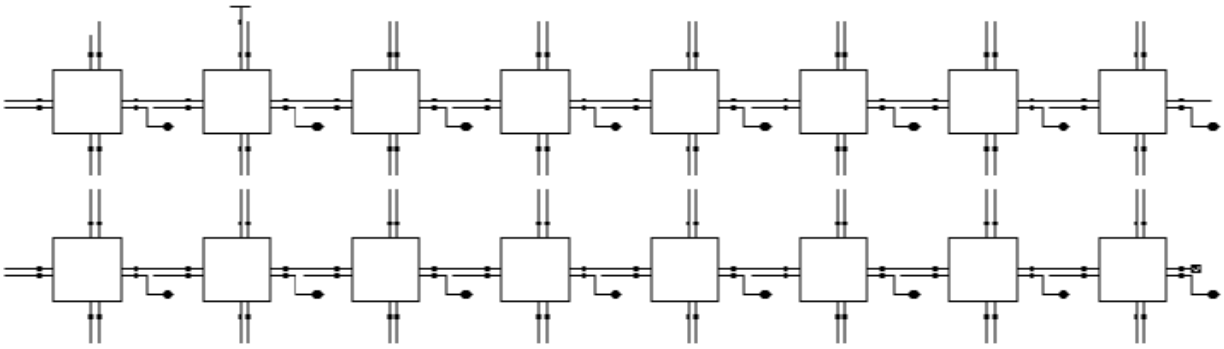

Figure 30: Schematic of a 16-bit shift register in Cadence

The following shift registers are used in this design:

- Row Select Shift Registers

  4 50-bit shift registers, 2 for the pixel array (writing) and 4 for the memory (2 for writing and 2 for reading). 2 lines, one per set of 50 rows, are written or read at a time.

- Frame Select Shift Register

  1 16-bit shift register for selecting a memory (frame) in the memory blocks

- Column Select Shift Registers

  2 100-bit shift registers. 2 columns, one per ADC, are read at a time

The shift registers are controlled by the following signals:

- RSTSHIFT: reset the shift register (asynchronous – active Low)
- SET: “starts” the shift register (asynchronous – active low)
- SHIFT_IN: the shift register “starts” at the next rising edge (synchronous)
- UPDATE: the output updates when Low (asynchronous – active low)
- RSTDEC: when Low it turns the current output Low (asynchronous – active low)

One or more shift-registers can share the clock (CLK) and the control signals. Note that UPDATE and RSTDEC signals do not affect the “shifting” process, just the outputs of the register. Using the RSTDEC signal it is ensured that the following line does not turn ON before the previous one is fully OFF. This is important when writing values from the pixels to the memories, because each memory has to store the value of only one pixel and this value should

not be affected by the previous or following writing operations. When reading from the memories this is not important because the values are now sampled by the ADCs. Using the UPDATE signal the writing or reading of some lines and columns can be skipped. This feature is important for bigger sensors, e.g. the proposed Mpixel expansion of the sensor, since the writing and reading times can be decreased by skipping lines and columns (trade resolution for speed). For example, if only one out of two lines and one out of two columns are read, the reading time can be increased by 4.

The global digital signals and the outputs of the shift registers are buffered according to the resistance and the capacitance of their load. For example, the buffers that drive the output switches of the pixels and the output switches of the memory blocks are 4 times bigger than the buffers driving the input switches of the memory blocks. This is because the width of the first switches is 2um, while the width of the latter switches is 0.42um, therefore the capacitance of the driven load is smaller, since the resistance is the same in both cases (resistance of metal wires) and the capacitance is mainly the capacitance of the gates driven.

The row select shift registers are designed having the same pitch as the pixels, so there is one buffer per output. The frame select shift register has only 16 outputs and these are buffered at the beginning of every of the 100 rows of memories.

Finally, because the column select shift registers drive PMOS switches, inverters have been used to drive them ON when the output of the shift register goes high. PMOS 1.8 V switches have been used in this case, instead of NMOS 1.8 V switches, because the latter cannot pass the high values (as high as 1.5 V) that need to be read from the memory blocks. NMOS 3.3V switches could also be used but the use of 3.3 V switches could create unpredictable problems in a 1.8 V power domain.

4.7 ANALOG TO DIGITAL CONVERTER (ADC)

The image sensor uses two 12-bits 100MHz pipeline ADCs, which are IP block of Alphacore Inc. They have been chosen to have enough resolution and speed so that they are not limiting the performance of the image sensor.

The ADC consists of the following sub-blocks: self-bias, non-overlap clock generator, clock buffers, four pipelined sub-stages with 2.5 bits per stage, and at last a 4-bit flash ADC. The 0.5-bit in the pipeline sub-stages is for redundancy calibration, to overcome an offset in sub-ADCs up to Vref/8. The 4-bit flash ADC at the last stage is used to save power and also simplify the design. The outputs of the ADC are 16 and give samples at both at the rising and the falling edge of the clock. These outputs are added up in a certain way for calibration purposes and then one out of two samples are discarded. That way a 12-bit calibrated value is attached to every memory read.

The ADCs in the current work are using a 10 MHz clock, and sample the values read from the memories both at the rising and the falling edges of the clock. Each ADC is connected to 100 lines (2 lines per memory column) and reads the values stored in the memories one-by-one. The quantization rms noise of the 12-bit ADC is $1.8V / (2^{12} \times \sqrt{12}) = 0.13mV$, which is lower than the 0.26mV noise seen at the input of the ADCs, because of the noise in the pixels and memories, and is not expected to limit the performance of the sensor.

Moreover, the linearity of the sensor has been simulated and it is expected to have a linear performance when its negative input is tied at Vref = 0.9V and it positive input is swinging between 1.8V and ground. The operational swing of the voltage at the input of the ADC is

expected to be between 1.5V and 0.6V, hence the ADC is a great fit for reading the stored values in the memory blocks.

The layout of the 12-bit pipeline ADC in Cadence can be seen in Figure 31.

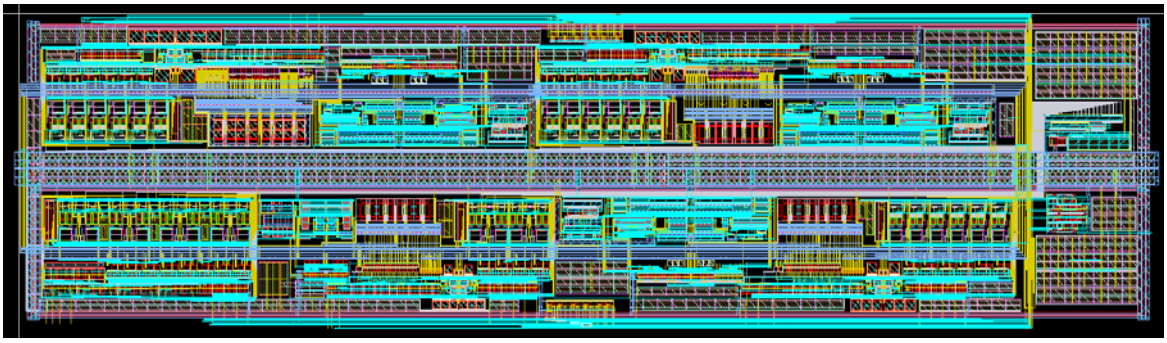

Figure 31: Layout of the 12-bit pipeline ADC in Cadence

For the power tracing, the power and ground lines have been designed very wide and multiple metal layers are used to minimize the voltage drops. Moreover, multiple supply pairs have been used and the free space has been filled with decoupling capacitors, so that the effect of the bondwires inductance is minimized. Finally, the signals and reference traces have designed as similar as possible for both ADCs, to keep their performance uniform. Small shifts can always be fixed later using software calibration.

4.8 INPUT / OUTPUT (I/O) PADS

The I/O pads will be standard cells with ESD protection, provided by the foundry. The following things have been considered for the proper selection of the number of power pads to be used in this work.

- DC characteristics: bond wires and on-chip power rails generate a resistive voltage drop. DC voltage drops will be reduced by:
    - Distributing supply pairs evenly around high current input/output cells
    - Having many supply pairs bonded out
    - Using 6-layer metal
- Electromigration: a long-term reliability hazard that occurs if a high current density flows in metal interconnections and displaces metal atoms. A metal track that suffers electromigration will eventually break and the device will fail. The limit for the I/O cells used in this work is 35mA.
- AC characteristics: voltage transients are generated when the output drivers and internal core logic cells switch states
    - More supply pairs reduce the effect the bond wires
    - Separate analog and digital supplies for the core
- PCB and final device test considerations
    - Poor PCB layout can dramatically increase parasitic inductances
    - Test environment is generally worse than the application environment, so more supply pins are needed

To avoid the damage of the image sensor by ESD stress, ESD protection devices are used on all the pads. The basic ESD protection scheme is two-fold: to safely discharge the ESD current via a low-impedance shunting path and to clamp the voltage on an I/O pin to a sufficient low level [38]. The protection devices and interconnects can withstand the discharge current without damage, and the current path for the ESD discharge is designed to have the lowest impedance for an ESD shock compared to all possible parasitic discharge paths.

The image sensor in this work uses a common ESD ground rail that runs through all the pads of the chip. The ESD power rail is cut into two areas. The upper part runs through all of the pads around the pixels and the memory and the lower part is for the ADC pads. This is because the ADC is using 1.8V logic compare to the 3.3V logic used for the rest of the sensor.

The following power supply signals and references have been used in this work:

Pixel and Memory

- VDD3: Analog power supply for the pixel and memory arrays
- VDD_P: Analog power supply for the pixel reset (FD and in-pixel memory)
- VDD_M: Analog power supply for the memories reset
- VSS: Common analog ground for the supplies above, and substrate connections in the pixel and memory arrays area
- DVDD3: Digital power supply for the row decoders and buffers, and I/O cells core rail
- DGND: Digital ground for the row decoders and buffers, and substrate connections for the areas outside pixel and memory
- AGNDM: Isolated ground for noise isolation and latch up protection. It also the ground used for substrate in the ADCs area
- REF 1 to 3: References for the in-pixel (1 and 2) and memory source followers

ADCs

- AVDD / AGND: Analog power supply and ground
- AVDDL: Digital power supply for the ADCs and the column decoders and buffers
- AGNDL: Digital power ground for the ADCs and the column decoders and buffers
- VREFP, VREFN and VCM: Positive and negative references, and common mode voltage

ESD protection and I/O buffers

- VDDOR: Power supply for the I/O cells input/output buffers and ESD protection structures for the pixels and memory area
- VDDOR_ADC: Power supply for the I/O cells input/output buffers and ESD protection structures for the ADCs area
- GNDOR: Common ESD ground and ground for the above, and substrate connections for the I/O cells
- VDD_ADC: Power supply for the I/O cells core rail for the ADC area

A summary of the I/O signals and supplies used in this work can be seen in Table 3. The digital I/O signals are

Number of signals	Signal Type	Description
9	Power supply	Analog and digital supplies
6	Power ground	Ground for the supplies and/or substrate
6	Voltage reference	Used for current sources and ADCs
4	Analog I/O	Direct access to 2 pixel-to-memory columns and the inputs of the 2 ADCs
27	Control signal	Shift registers, global signals for pixel or memories, ADCs enable, access switches
4	Clock	Shift registers and ADCs
34	Digital output	Outputs of the ADCs plus 2 used for input buffers parametric testing
90	**TOTAL**	

Table 3: Summary of I/O signals and supplies in the image sensor chip

4.9 THE IMAGE SENSOR

The image sensor presented in this work is built in a 0.18um CMOS with pinned photodiode process with 6 metal layers. It has 10,000 15.1um x 15.1um pixels, with a 41.6% fill factor, in a 100 x 100 configuration, and it is able to capture a total of 16 frames at speeds up to 267 kframes per second, for an exposure smaller than 3.5us. This is achieved by storing the frame values on-chip, using an array of 10,000 memory blocks (15.1um x 26um each), one per pixel, containing 16 NMOS capacitors used as memories. The stored values are read after all 16 frames have been transferred to the memory blocks by two 12-bit pipeline ADCs, which have been selected to be fast and low noise, so that they do not limit the performance of the image sensor.

The full chip layout can be seen in Figure 32. Its dimensions, including the pad ring, are 3010um x 6554um. The total number of the I/O pads used in this design are 278, of which 31 are digital inputs, 34 are digital outputs, 4 are analog inputs/outputs and 209 are power supplies. An increased number of power supply pairs has been used to ensure that the voltage drops are low and uniform between pixels and memories. Moreover, multiple metal layer power supply rings have been created around the core of the sensor for all the different supplies, analog and digital, as well as the reference voltages. Bellow these rings, MOSFET capacitors have filled all the available space to provide the required decoupling capacitance needed to reduce transient switching spikes. High current input/output cells have been distributed equally around the core to ensure that the decoupling capacitors can handle the local transient spikes. Finally, Metal Insulator Metal (MIM) capacitors have been used in the ADCs area together with the MOSFET capacitors to increase the decoupling capacitance available even further.

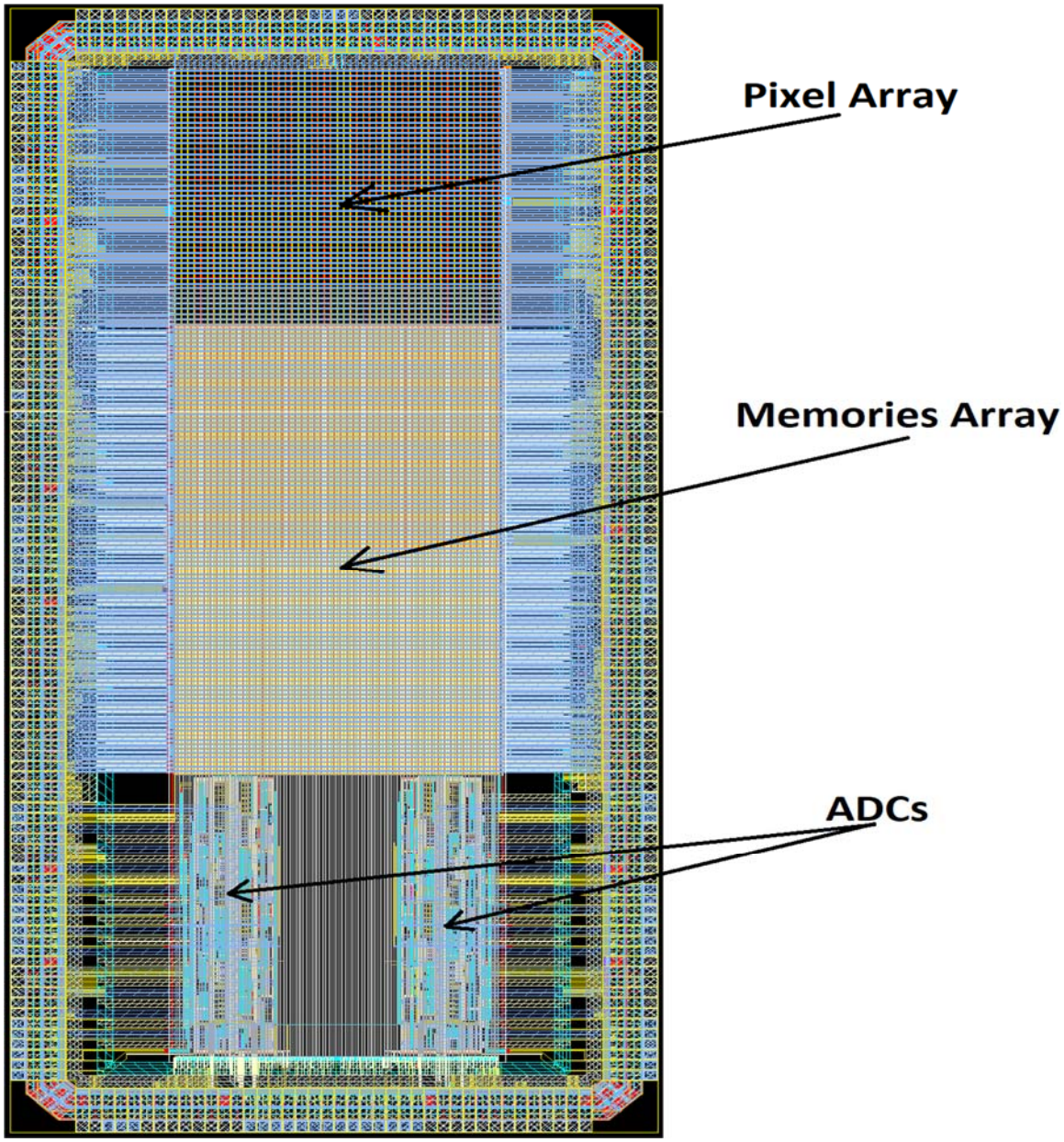

Figure 32: Full test chip layout in Cadence

The readout time of the image sensor is 8ms, which is fast enough to ensure that the leakages at the designed on-chip memories will be below the noise level for the whole readout time.

A picture of the image sensor ass seen in the microscope can be seen in the following figure.

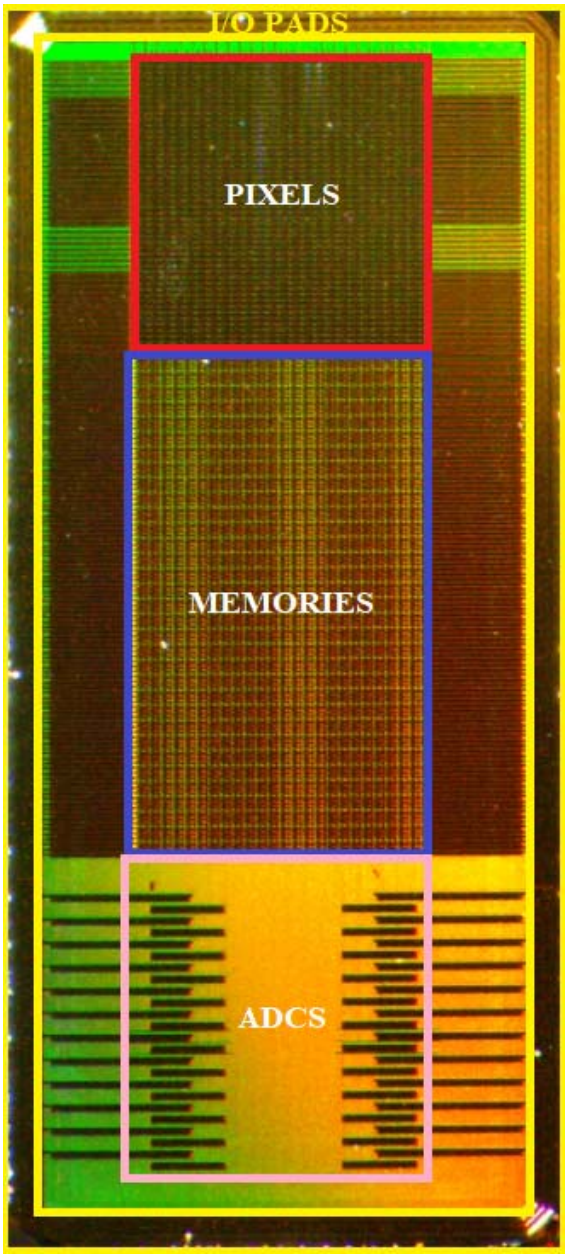

Figure 33: The image sensor as seen in the microscope

The expected performance of the presented image sensor is summarized in the following section.

4.10 EXPECTED PERFORMANCE

The specifications of the presented image sensor and its expected performance are summarized in the following table.

Process technology	0.18um CMOS with pinned photodiode
Die size	3010um x 6554um
Pixel size	15.1um x 15.1um
Active PPD area	$9.6um^{H}$ x 10.6 um^{V}
Fill factor	41.6 %
Quantum Efficiency @ 550nm	88 %
# of pixels	10,000 (100x100)
# of frames in burst mode	16
# of pixel sharing an output line	50
# of parallel outputs	2
# of PADS	278
Minimum integration (exposure) time	1 us
Shortest delay between frames	3.74 us
Maximum frame rate	267 kfps

Conversion gain	35 uV/e^-
Full well capacity	200,000e^-
Absolute sensitivity (rms)	0.57mV / 16.39 e^-
Input (FD) saturation	800mV / 22,857 e^-
DR	62.89 dB
SNR	43.59 dB
Readout Time	8 ms
Memory Leakage @ 27º C	Bellow noise level
Image Lag @ 267 kfps	Below measurement limit
Spectral sensitive range	425nm – 700nm

Table 4: Summary of the image sensor performance

The Dynamic Range (DR) is defined as the input saturation divided by the absolute sensitivity. The Signal-to-Noise Ratio (SNR) is defined as the square root of electrons available to the active area in saturation [39]. The maximum theoretical DR and SNR can be calculated using the full well capacity electrons instead of the electrons available in saturation, and for the current sensor they are 83.41dB and 53.01dB respectively.

The maximum SNR is limited by the shot noise, which is associated with the random arrival of photons at any image sensor and it is the natural fundamental limit on noise performance [40]. The time between the arrival of photons is governed by Poisson statistics and consequently the uncertainty in the number of photons collected during a given exposure time is given by [40]:

$$\sigma_{shot} = \sqrt{S} \tag{19}$$

where σ_{shot} is the shot noise and S is the signal, both expressed in electrons.

For the absolute sensitivity, the quantization noise of the ADC is added to the input referred noise calculated using equation (18). The reason why only the quantization noise of the ADC is added is because the other ADC noises in simulations are much smaller than the quantization noise. To find the input referred noise of the ADC using simulations, a DC value was used as input and the outputs of the ADC were collected and plotted as a histogram. Since the noise is approximately Gaussian, the standard deviation of the histogram is the input referred noise [41]. A detailed description of how to calculate the standard deviation and consequently the input referred noise of the ADC is given in [42].

CHAPTER 5: CAMERA DEVELOPMENT

5.1 CAMERA ASSEMBLY

The image sensor chip is directly wire-bonded onto a Printed Circuit Board (PCB) as seen in Figure 34. Because of the high number of chip pads, 4 PCB pad tiers have been used per side. The wirebonds are covered with transparent glob top epoxy, but the sensor is not covered by glass. The sensor is protected by the lens mount that was designed and 3d printed exclusively for this sensor. A special design was necessary because its bottom opening had to be large enough to fit both the sensor and the wirebonds. Moreover, the c-mount opening of the lens mount was designed to be above the active area of the sensor, which in this case is different than the center of the sensor. At the bottom of the mount an Anti-Reflection (AR) coated high efficiency window, with a 425nm - 700nm wavelength range, is glued on it to protect the sensor from physical damage and dust.

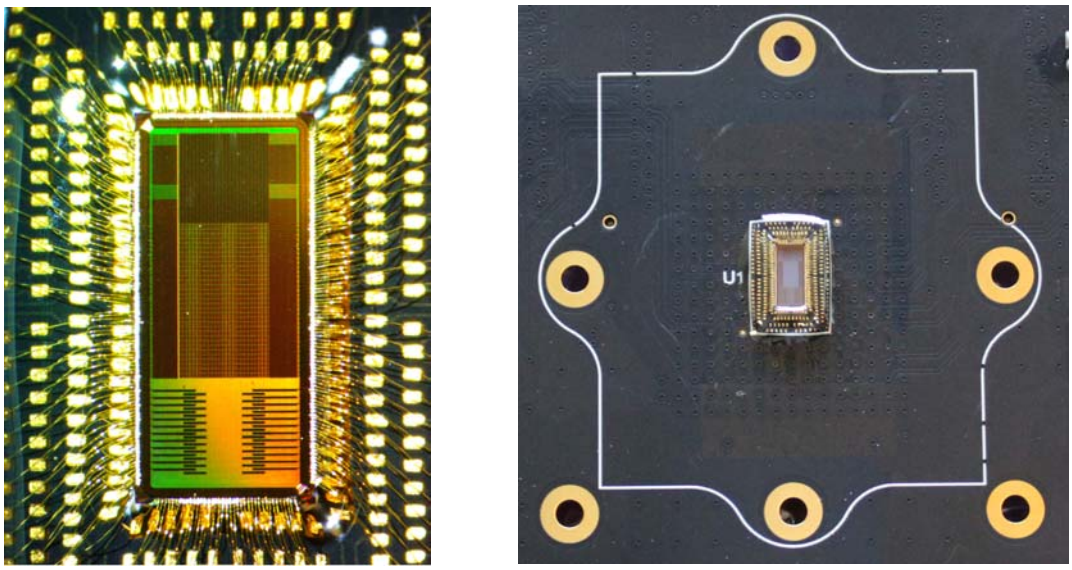

Figure 34: The image sensor on the PCB

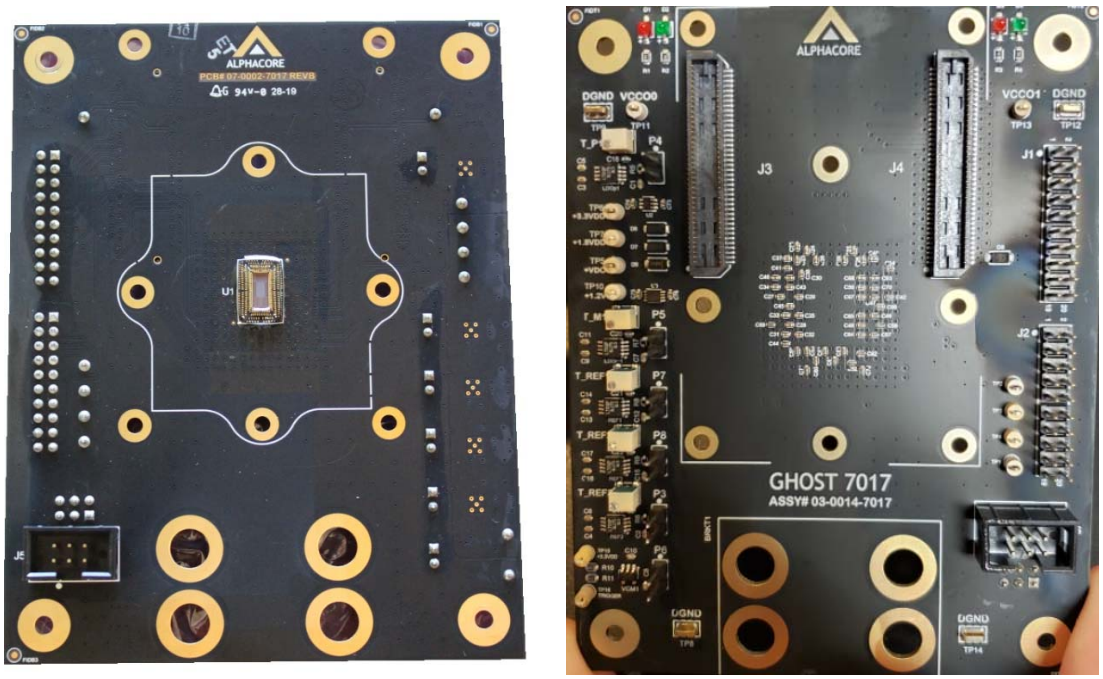

Figure 35: The camera PCB

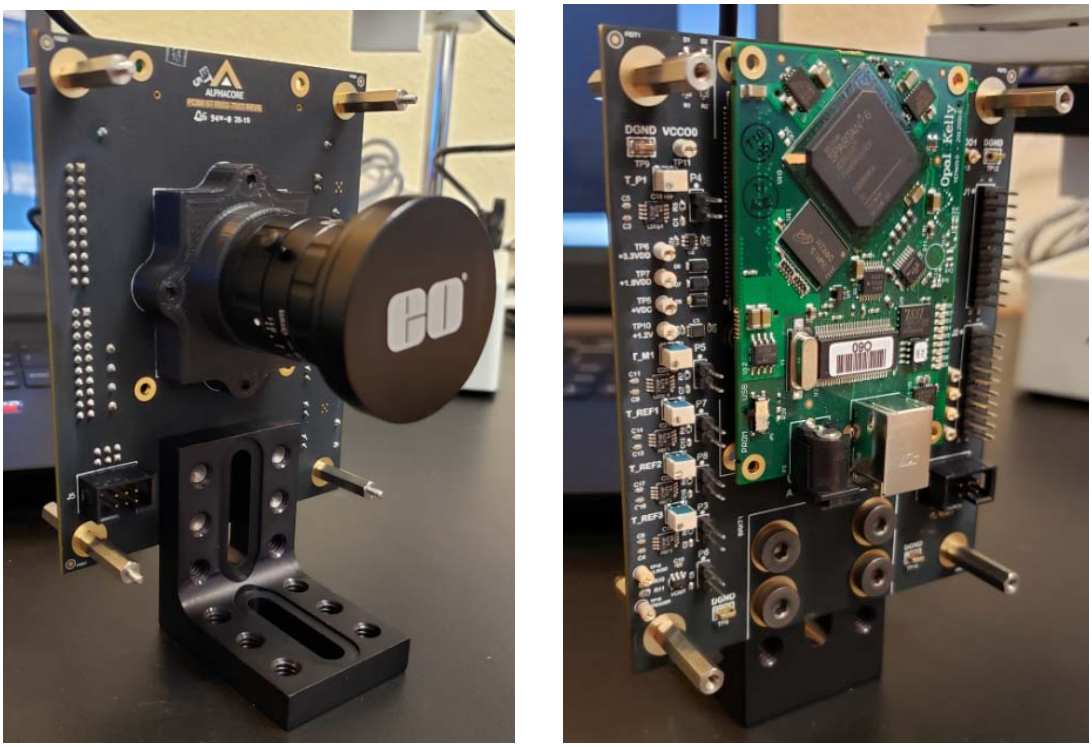

Figure 36: The camera PCB with the lens mount, the FPGA and the lens attached

The PCB designed to host the image sensor can be seen in Figure 35. It includes all the necessary low-dropout (LDO) regulators, protections, decoupling capacitors, test points and headers, and it is designed to accept a separate FPGA module board that will plug directly into the headers on the underside of the board. The FPGA module is based on Xilinx Spartan 6 with on board DDR2 SDRAM and Flash memory, PLL and power management LDO's. This module will provide the digital signals and clocks to the camera board, and will read the camera outputs. It will also provide power to the camera board. Through this module the camera assembly is connected to a PC using a USB cable.

Finally, the camera board is generating a clock signal that can be used as input to the LED board that will be used for testing the exposure and speed performance of the sensor and will be presented in CHAPTER 6. It is also generating a trigger signal than can be optionally used to start the operation of the LED board. The transfer of these signals between the two boards, together with the common ground, an external trigger signal and a signal used to count full LED cycles, is happening using a 6 wire flat cable.

5.2 FPGA CODE AND SOFTWARE DEVELOPMENT

The heart of the camera developed in this work is the image sensor presented in CHAPTER 4. The signals needed by this sensor in order to operate are provided by a XEM6010 module, which is a USB 2.0 integration module based on Xilinx Spartan-6 FPGA (Field Programmable Gate Array). Moreover, this module is programmed to read the outputs from the ADCs and transfer them safely to a PC.

The FPGA code is written in Verilog and it is simulated to verify the behavior of the signals needed by the sensor. Then the code is synthesized, placed and routed, and specific FPGA pins are assigned to all output and input signals. Functional and timing gate level simulations are performed to ensure that the actual hardware design performs within the required specifications. Finally, a programming file is generated. This file is used to configure the FPGA when running the camera software.

To enable the control of the FPGA (i.e. start the exposure, reset the FPGA) and allow the transfer of the read images from the FPGA to the PC, FrontPanel SDK is used, and it provides three essential components as seen in Figure 37. For the software application, an API and a robust driver to communicate with the FPGA module over USB or PCI Express is provided. For the FPGA module, it provides a device firmware to manage FPGA configuration and communication, and small FPGA IP blocks that are integrated with the HDL code to make communication simple.

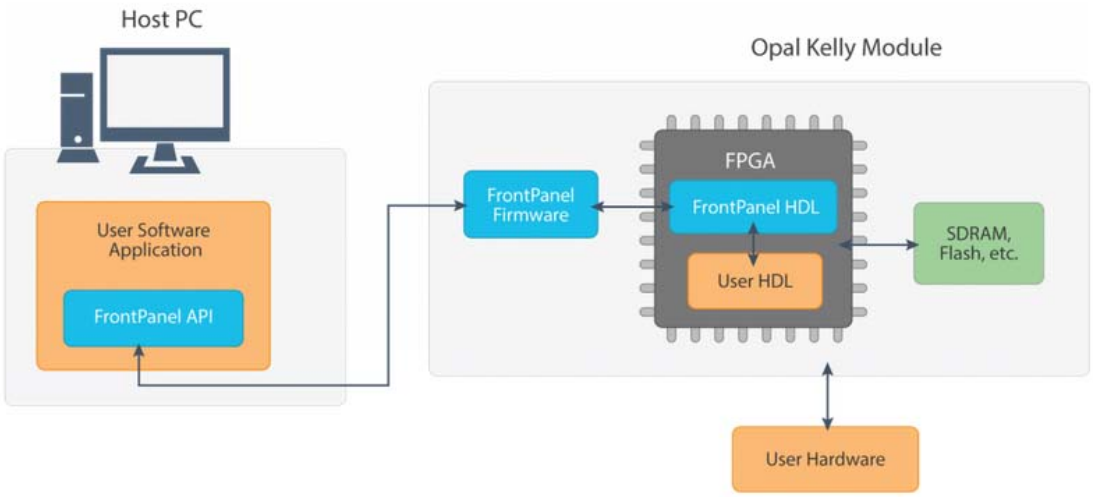

Figure 37: Front panel components used to accelerate the camera design [43]

The camera software is written in C++ and it has the following functionalities:

- Sets the exposure time and frame rate for the sensor
- Triggers the capture of a series of 16 images
- Shows the 16 frames captured
- Calibrates the first 15 frames based on the 16th reference frame
- Allows continuous operation
- Calculates the frame rate and shows the missed frames for the continuous operation
- Saves the resulting images
- Resets the FPGA

The Graphical User Interface (GUI) for the camera software can be seen in the following figure.

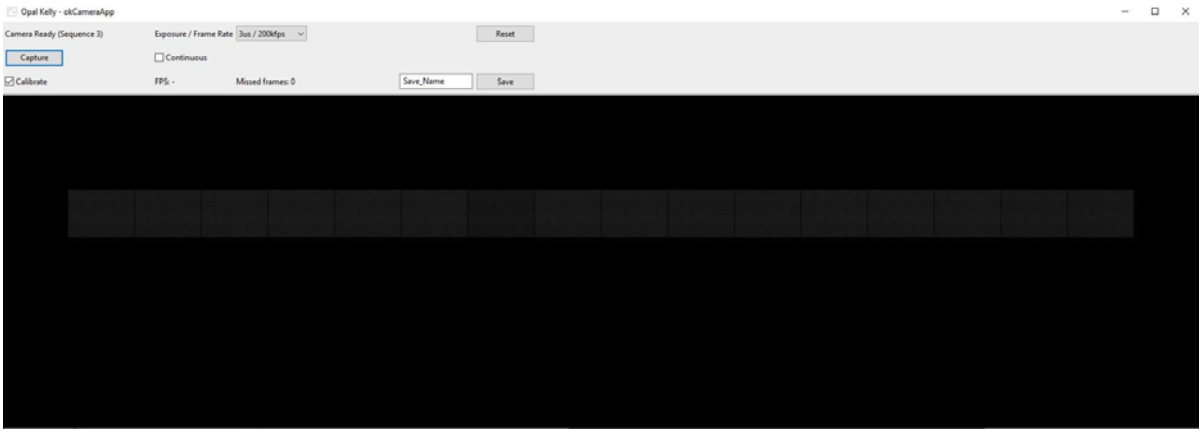

Figure 38: Camera GUI

The images shown in the GUI are 8 bit images. When the user saves the image, the software saves the 8 bit image in bmp format, as well as the 12 bit image information in csv format.

CHAPTER 6: TESTING

6.1 PERFORMANCE PARAMETERS

There are many parameters that can be used to evaluate the performance of an image sensor. We can classify these parameters into three main categories:

1. Image Sensor Layout:

   pixel count, pixel pitch, image format,

2. Pixel Physics:

   Quantum Efficiency, Fill Factor, Full Well Capacity, Conversion Gain, dark current, image lag

3. Image Sensor Readout:

   Signal-to-Noise-Ration (SNR), Dynamic Range (DR), linearity, power consumption, bit depth, frame rate, spatial nonuniformity

The parameters in the first category are straightforward and depend on the number and size of pixels as well as the number of rows versus the number of columns. These parameters can be used when creating a complete imaging system including the lenses. The minimum feature size of an object under inspection (resolution), the Field of View (FOV) of the camera and the minimum sensor spatial resolution (in line pairs per mm) for a given contrast, are just some of the image quality metrics that depend both on image sensor layout parameters and the selected lens.

The parameters in the second category depend on the device physics and the pixel layout.

Quantum Efficiency (QE) is process dependent and is the percentage of electrons generated by the photons hitting the active area of the pixel and depends on the wavelength of the incident photons. For the process used in this work the QE is 64% at 450nm, 88% at 550nm and 74% at 600nm.

The **Fill Factor (FF)** will affect the total number of electrons generated, since the active area of the pixel is a fraction of the pixel size. Fill factor is defined as the percentage of the unshaded active pixel area out of the total pixel area.

The **Full Well Capacity (FWC)** depend on the active area size. A rough estimate for the process used is $2{,}000e^-/um^2$, which results in a FWC for the presented sensor of $200{,}000e^-$.

The **Conversion Gain (CG)** depends on the FD capacitance and is calculated as described in CHAPTER 4. It is defined as the uV change of the FD potential for every electron transferred from the PPD.

The **dark current** is the small leakage current that flows in the PPD even if no light is available as a result of many different physical phenomena that occur in the PPD [44]. Dark current is negligible in the presented sensor because of the small exposure times.

Image Lag is the result of incomplete charge transfer from the PPD to the floating diffusion. This is not expected to be a problem in the presented work because of the large differential between the reset diode voltage (2.3 V) and the pinned diode voltage (<0.96 V), and because of the large reset time for the PPD (RSTFD and TG are ON for at least 100ns before every new frame). Transfer times of 60 ns and less have been demonstrated in [35] for large 50um pixels with virtually no image lag.

The parameters in the third category depend on the complete image sensor design.

The **Signal-to-noise Ratio (SNR)** is equal to the square root of electrons available to the active area in saturation. The **Dynamic Range (DR)** is equal to the input saturation divided by the input referred noise [39].

The **linearity** of the sensor can be expressed as the percentage difference between the mean gray values minus the dark values for different irradiation levels and the least-squares linear regression line that has the minimum deviation from the measured values.

The **power consumption** is the power consumed by the whole camera assembly.

The **bit depth** is the number of bits of available information per pixel. This can be as high as the number of bits of the ADCs, but most of the times it is less than that to reduce the noise seen in the image and to reduce transfer times.

The **frame rate** is the reciprocal of the time difference between the start of exposure between two consecutive frames. The maximum achievable frame rate is equal to the reciprocal of the exposure time.

The **spatial nonuniformity**, is a metric used to describe how much the outputs of the image sensor vary from pixel to pixel, when the sensor is exposed to a uniform light source or not exposed to light at all. Sometimes these nonuniformities are called “Fix Pattern Noise” (FPN), but this term will not be used in this work since it can be misleading, because inhomogeneities are spatially constant with no temporal variation and thus are correctable [45].

6.2 TESTING METHODS

The following testing methods will be used to characterize the sensor. The setup presented in section 6.2.1 and the methods presented in sections 6.2.2 and 6.2.3 are based on the EMVA 1288 standard for the characterization of image sensors and cameras as seen in [39]. In sections 6.2.4 and 6.2.5, the setup and methods for testing the sensor exposure and frame speed are presented.

6.2.1 SETUP FOR SENSITIVITY, LINEARITY, NOISE AND NONUNIFORMITY

For the measurement of sensitivity, linearity, noise and nonuniformity, a setup with a light source and the required lenses that irradiates the image sensor without a mounted lens homogenously is used.

The setup can be seen in Figure 39 and includes the following components:

- High power, 3.2 W, white LED
- High power LED driver
- Optical lenses
- Optical bandpass filters
- Photodiode power sensor
- Power and energy meter interface for the power sensor
- Optomechanical components

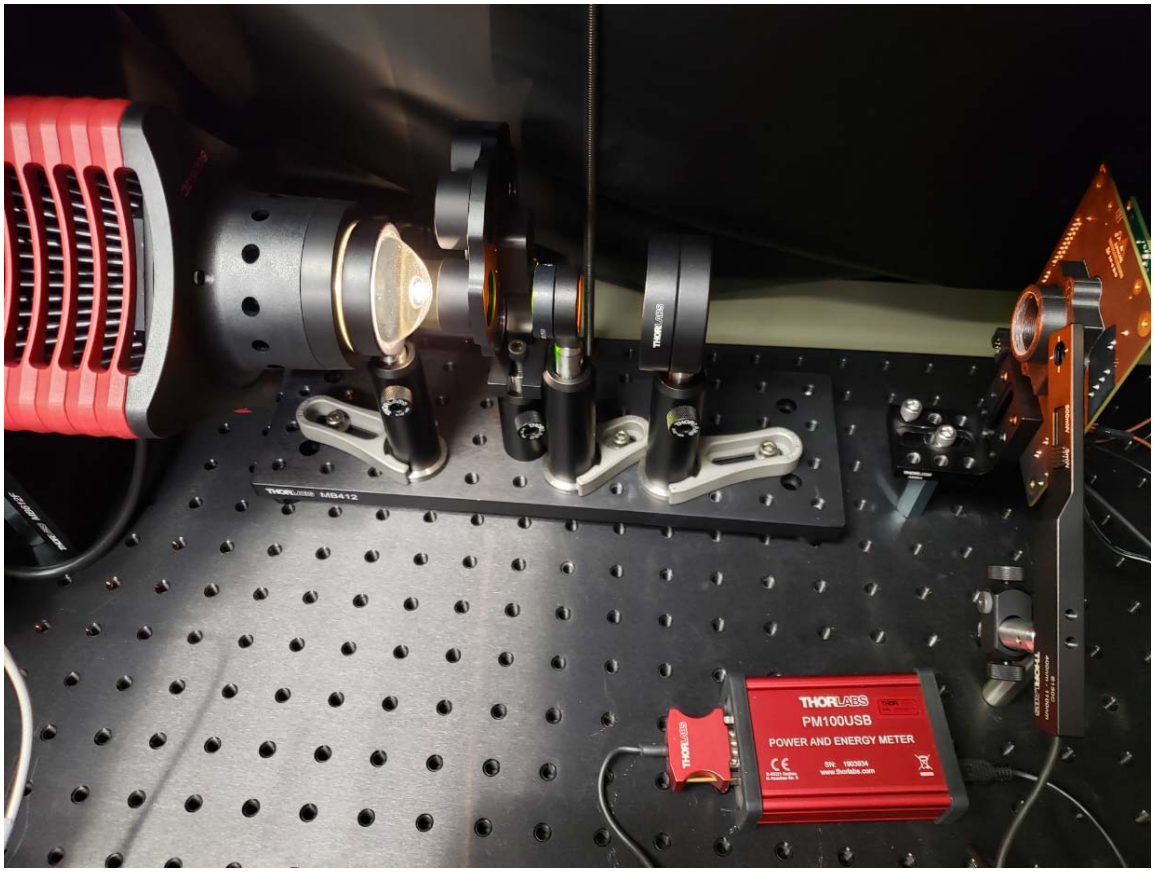

Figure 39: Optical setup for testing sensitivity, linearity, noise and nonuniformity

Three bandpass filters were used for the testing of the sensor, with a central wavelength (CWL) of 450nm, 550nm and 600nm, and a Full Width Half Maximum (FWHM) of 10nm$\pm$2nm. The bandpass filters are needed for 2 reasons. First, because the photodiode power sensor has a different response for light at different wavelength, and consequently the power meter interface used to measure the current created by the sensor needs to know the wavelength of the light to translate the current it reads to power. Second, the image sensor also has different response to different wavelength (QE specification). So, in order to fully characterize it, light needs to have a limited width of wavelengths.

However, because the bandpass filter keep only a portion of the light, the light is not enough for testing the sensor at 3us exposure. That is why the sensor is tested for 300us exposure when using the bandpass filters. But, since we want to characterize the sensor performance at 3us also, we will use the unfiltered full light to create enough light and we will make an estimate of the light power seen at the surface of the sensor under test. Besides, important performance parameters like the Dynamic range and the Signal-to-Noise Ratio will be measured accurately since they do not depend on the measured number of photons at the sensor surface.

6.2.2 METHODS FOR SENSITIVITY, LINEARITY AND NOISE

Exposure time is kept constant for the image sensor throughout each test performed in this section, and what is changing is the irradiance by changing the LED source current. Fifty equally spaced irradiation values that create image values between the minimum (dark) and the maximum digital gray values are used. At each irradiation level two images are captured. For dark conditions, hundred images are captured, instead of two, for better calculation of the temporal variance, and because they will also be used to characterize the spatial nonuniformity of the sensor for no light. For all other lighting conditions, it is sufficient to capture only two images since the noise is stationary and homogenous [39].

The measurements are performed at room temperature and the image information used is both the whole 12-bit information from the ADCs and the 8-bit images saved by the software. The offset of the image sensor under test is set so that it is as small as possible but also large enough to ensure the values from the camera with no light are above 0 for 99.5% of the pixels.

A physical model of the camera and the mathematical model of a single pixel can be seen in Figure 40. All noise sources, except for the photon (shot) noise which is equal for all cameras, depend on the specific construction of the image sensor and the camera electronics.

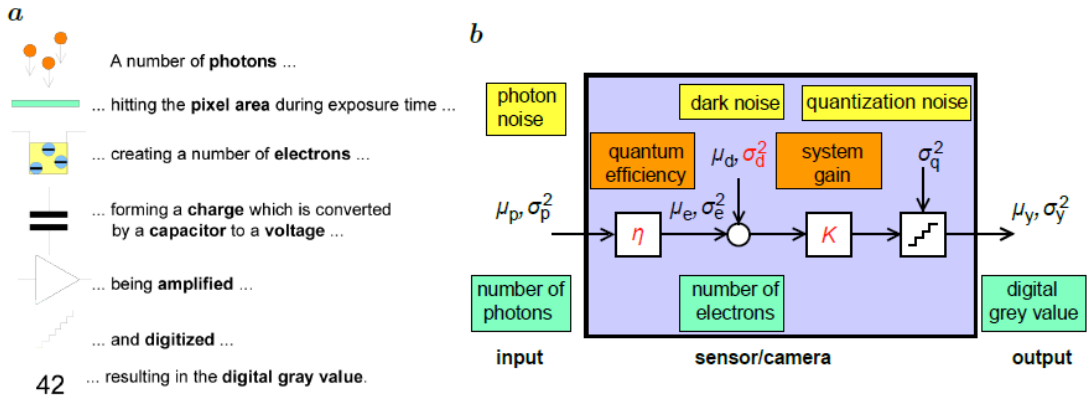

Figure 40: (a) Physical model of the camera and (b) Mathematical model of a single pixel [39]

The mean number of photons that hit a pixel area A during the exposure time t_{exp} can be computed from the measured irradiance E on the sensor surface in W/m^2 by

$$\mu_p = \frac{AEt_{exp}}{hv} = \frac{AEt_{exp}}{\frac{hc}{\lambda}} \tag{20}$$

or by using the values for the speed light c = 2.99792458 x 10^8 m/s and Planck's constant h = 6.6260755 x 10^{-34} Js, the mean number of photons that hit a pixel area A are

$$\mu_p[photons] = 50.34 \times A\,[\mu m^2] \times t_{exp}\,[ms] \times \lambda\,[\mu m] \times E\left[\frac{\mu W}{cm^2}\right] \tag{21}$$

where λ is the wavelength of the light.

A fraction of the photons that hit the surface of the sensor is converted into electrons. This quantity is the product of the Quantum Efficiency (QE) and the Fill Factor (FF) of the sensor. Therefore the quantum efficiency of the sensor is given by

$$QE\ [\%]\ =\ \frac{\mu_e}{FF\ \times\ \mu_p}\ \times 100 \tag{22}$$

The electrons are converted into a voltage, amplified and finally converted into a digital signal y by an Analog-to-Digital Converter (ADC). This process is assumed to be linear and can be described by the following equation

$$\mu_y = K(\mu_e +\ \mu_d) =\ \mu_{y,dark} + K\mu_e \tag{23}$$

where $\mu_{y,dark}$ is the output of the sensor for no light in Data Numbers (DN), and K is the overall system gain.

The number of electrons fluctuate statistically, and according to the laws of quantum mechanics the probability is Poisson distributed. Therefore, the variance of the electrons generated (σ_e^2) is equal to the mean of the electrons (μ_e) as seen in the following equation (shot noise)

$$\sigma_e^2\ =\ \mu_e \tag{24}$$

Due to the linear signal model, as described by equation (23), all noise sources add up. The noise sources related to the sensor read out circuitry can be described by a signal independent normal distributed noise source with variance σ_d^2. The variance of the noise added by the ADC is $\sigma_q^2 = \frac{1}{12}DN^2$. And since all noises add up linearly, the total temporal variance of the signal y, σ_y^2, is given by

$$\sigma_y^2 = K^2(\sigma_d^2 + \sigma_e^2)\ +\ \sigma_q^2 \tag{25}$$

Using equations (23) and (24) the noise can be related to the measured mean digital signal by the following equation

$$\sigma_y^2 = K^2\sigma_d^2 + \sigma_q^2 + K\left(\mu_y - \mu_{y,dark}\right) \tag{25}$$

In equation (25), the first and second terms can be treated as an offset, and then from the linear relationship between the variance of the noise, σ_y^2, and the mean output value of the system, $\mu_y - \mu_{y,dark}$, the overall system gain, K, can be determined from the slope, and the dark noise variance, σ_d^2, from the offset.

The method described above is known as the photon transfer method [39]. To find the **system gain (K)** graphically, the light induced variance, $\sigma_y^2 - \sigma_{y,dark}^2$, is plotted against the light induced mean, $\mu_y - \mu_{y,dark}$. A least squares linear regression line is created by using the measurements between 0 and 70% of the saturation level. The saturation point is the first point in the photon transfer curve to be greater than the following 2 points when scanning from the right to the left.

The slope of the linear regression line is calculated using a matrix approach. The matrix formulation can be written as

$$\boldsymbol{Y} = \boldsymbol{X}\boldsymbol{\beta} + \varepsilon \tag{26}$$

$$\boldsymbol{Y} = \begin{pmatrix} Y_1 \\ Y_2 \\ \vdots \\ Y_n \end{pmatrix}, \qquad \boldsymbol{X} = \begin{pmatrix} 1 & x_1 \\ 1 & x_2 \\ \vdots & \vdots \\ 1 & x_n \end{pmatrix}, \qquad \boldsymbol{\beta} = \begin{pmatrix} \beta_0 \\ \beta_1 \end{pmatrix}, \qquad \varepsilon = \begin{pmatrix} \varepsilon_1 \\ \varepsilon_2 \\ \vdots \\ \varepsilon_n \end{pmatrix}$$

where **Y** is a (n x 1) vector of the response variables, X is a (n x 2) matrix called the design matrix, and β is a (2 x 1) vector of unknown parameters [46].

For the linear regression line to be used for the photon transfer curve plot, no intercept will be used, and **X** and **β** are written in matrix notation as follows

$$\boldsymbol{X} = \begin{pmatrix} x_1 \\ x_2 \\ \vdots \\ x_n \end{pmatrix}, \qquad \boldsymbol{\beta} = (\beta_1) \tag{27}$$

The normal equations obtained in the least squares method are given by

$$\boldsymbol{X^T Y} = \boldsymbol{X^T X \hat{\beta}} \tag{28}$$

and the unique solution to the normal equations is given by

$$\boldsymbol{\hat{\beta}} = (\boldsymbol{X^T X})^{-1} \boldsymbol{X^T Y} \tag{29}$$

An example Photon Transfer curve is given in the EMVA 1288 standard and can be seen in Figure 41.

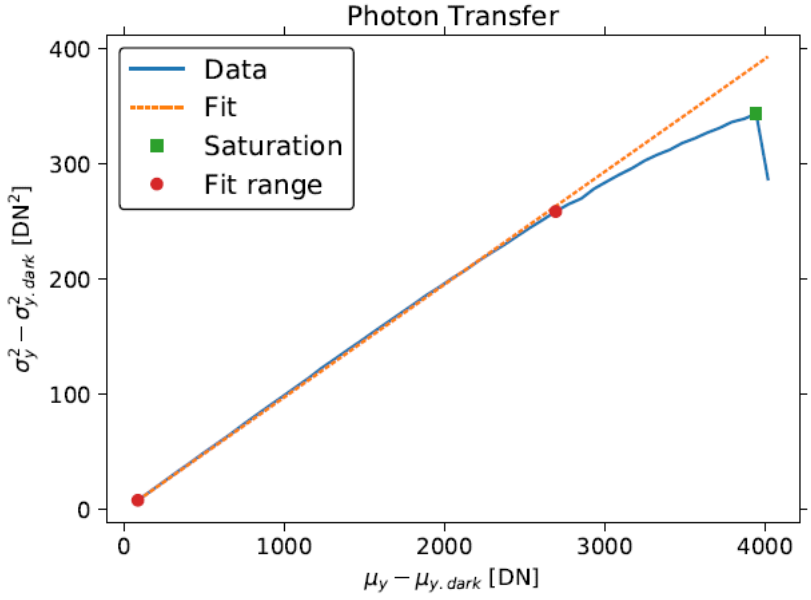

Figure 41: Example Photon Transfer curve as seen in EMVA 1288 standard [39]

The **temporal dark noise**, excluding the quantization effects, is calculated using the following equation

$$\sigma_d[e^-] = \sqrt{(\sigma_{y,dark}^2 - \sigma_q^2)}/K \tag{26}$$

or including the effects of quantization by

$$\sigma_d[DN] = \sqrt{\sigma_{y,dark}^2} \tag{27}$$

If $\sigma_{y,dark}^2 \leq 0.24$, then the temporal noise is dominated by the quantization noise and cannot be estimated reliably. In that case, the upper limits of the dark temporal noise are 0.4/K electrons or 0.49 DN.

The temporal variance of the signal, σ_y^2, that is used in Photon Transfer curve plot can be calculated for each of the irradiation level as the mean of the squared difference of the two images captured at this level as described by the following equation

$$\sigma_y^2 = \frac{1}{2NM}\sum_{m=0}^{M-1}\sum_{n=0}^{N-1}(y^A[m][n] - y^B[m][n])^2 \tag{28}$$

where M is the number of rows and N is the number of columns.

The variance of the signal for no light, $\sigma_{y,dark}^2$, is calculated as follows

$$\sigma_{y,dark}^2 = \frac{1}{LNM}\sum_{l=0}^{L-1}\sum_{m=0}^{M-1}\sum_{n=0}^{N-1}({y_{dark}}^l[m][n] - \mu_{y,dark}[m][n])^2 \tag{29}$$

where L is the number of images capture with no light (100 images for this work), and $\mu_{y,dark}(m,n)$ the average dark pixel value.

To calculate the Quantum Efficiency (QE) of the sensor we first create another plot, Sensitivity plot, with the mean number of photons hitting each pixel on the x-axis and the difference between the mean output at each irradiation level and the mean output at dark. An example Sensitivity curve is given in the EMVA 1288 standard and can be seen in Figure 42.

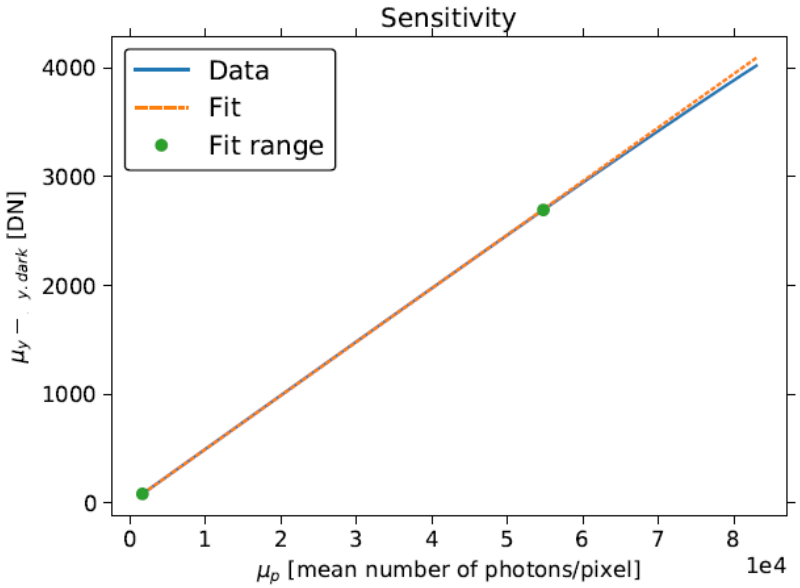

Figure 42: Example Sensitivity curve as seen in EMVA 1288 standard [39]

Similar to the Photon Transfer curve, a linear least regression line, using again the no-intercept model, is created by using the data points in the range between the minimum value and 70% saturation ($i.e. 0.7(\mu_{y,sat} - \mu_{y,dark})$). The slope of this line is the responsivity, R, of the sensor and relates the mean outputs to the mean incident photons as follows

$$\mu_y - \mu_{y,dark} = R\mu_p \tag{30}$$

Quantum Efficiency can now be calculated using the following equation

$$QE = \frac{R}{K \times FF} \tag{31}$$

where FF is the Fill Factor of the pixel.

Quantities in photons can now be translated to electrons and vice versa by using equation (22), in which we can substitute the product QE x FF by the calculated R/K parameter, which in this work it will be named **Effective Quantum Efficiency (EQE)** and will be given by the following equation

$$EQE = \frac{R}{K} \tag{32}$$

The **Absolute Sensitivity** threshold of the sensor is given by the following equation

$$\mu_{p,min}[photons] = \frac{1}{EQE}\left(\frac{\sigma_{y,dark}}{K} + \frac{1}{2}\right) \tag{33}$$

and the **Saturation Capacity** of the sensor, $\mu_{p,sat}$, is the number of photons that correspond to the number of photons at the saturation point that was found during the Photon Transfer curve method described before ($\mu_{p,sat}$).

The **Maximum SNR** is calculated using the following equation

$$SNR_{max} = \sqrt{\mu_{p,sat} \times \mathrm{EQE}} \tag{34}$$

or $20\log_{10}(SNR_{max})$ in dB and $\log_2(SNR_{max})$ in bits.

The **measured SNR** is calculated using the measured mean and the variance of the output values according to the following equation

$$SNR = \frac{\mu_y - \mu_{y,dark}}{\sigma_y} \tag{35}$$

The **theoretical SNR** is given by the following equation

$$SNR[\mu_p] = \frac{EQE \times \mu_p}{\sqrt{{\sigma_d}^2 + \sigma_q^2/K^2 + EQE \times \mu_p}} \tag{36}$$

The **ideal SNR** is given by the following equation

$$SNR[\mu_p] = \sqrt{\mu_p} \tag{37}$$

These values, together with SNR values that include the spatial nonuniformities (DSNU and PRNU) and will be described in section 6.2.4, are plotted in a single plot as seen in the following figure.

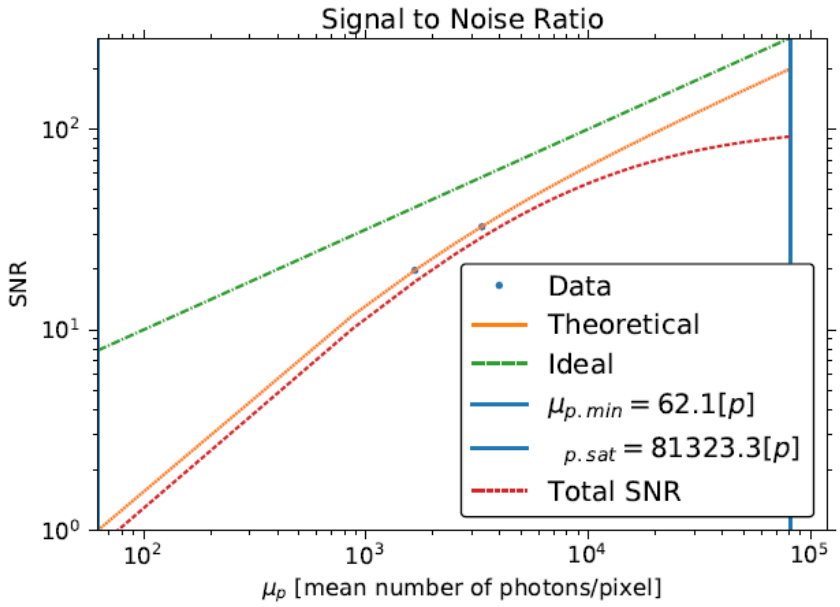

Figure 43: Example SNR graph as seen in EMVA 1288 standard [39]

The **Dynamic Range (DR)** of the sensor can be calculated as the ratio of the signal saturation to the absolute sensitivity threshold as shown in the following equation

$$DR = \frac{\mu_{p,sat}}{\mu_{p,min}} \tag{38}$$

To characterize the **Linearity** performance of the sensor, a plot of the mean output values for each irradiation level minus the mean dark values of the sensor is made, similar to what can be seen in Figure 44. To calculate the maximum and minimum percentage linearity errors, a percentage least squares linear regression line is created. This is different than the absolute regression method presented before, and this is because the quantity that needs to be minimized here is the percentage error instead of the absolute error.

The least squares percentage regression method is described in [46], and the normal equations are given by

$$\boldsymbol{X^T D^2 X \hat{\beta}} = \boldsymbol{(DX)^T DY} \tag{39}$$

and the unique solution to the normal equations is given by

$$\boldsymbol{\hat{\beta}} = \boldsymbol{(X^T D^2 X)^{-1} X^T D^2 Y} \tag{40}$$

The difference between the least regression line and the actual data gives the percentage error, as seen in Figure 44 (b).

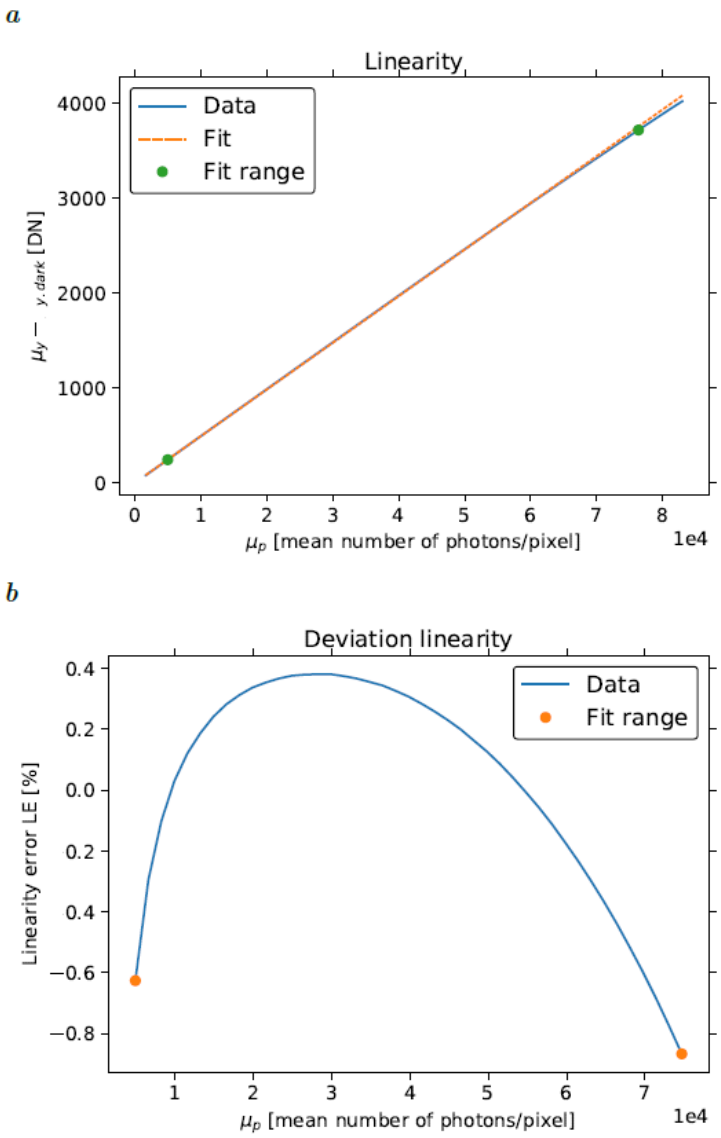

Figure 44: Example linearity plots as seen in EMVA 1288 standard [39]

(a) linearity plot from data and the linear regression line (b) percentage deviation from linear regression

6.2.3 METHODS FOR SPATIAL NONUNIFORMITY

The spatial nonuniformity measurements are performed using the same setup that was used for sensitivity, linearity and noise, as described in section 6.2.1.

To calculate nonuniformities, the temporal noise must be suppressed, so that it becomes much smaller than the spatial noise. This can be achieved by averaging a large number of images. In this work, 100 dark images and 100 images captured at 50% saturation will be averaged. All spatial variances will be denoted with the symbol s^2 to distinguish them easily from the temporal variances that are denoted with the symbol σ^2.

The means of the means of the hundred M x N dark and 50% saturation images, $\langle y_{dark} \rangle$ and $\langle y_{dark} \rangle$ respectively, are given by

$$\mu_{y,dark} = \frac{1}{MN} \sum_{m=0}^{M-1} \sum_{n=0}^{N-1} \langle y_{dark} \rangle [m][n] \ , \qquad \mu_{y,50} = \frac{1}{MN} \sum_{m=0}^{M-1} \sum_{n=0}^{N-1} \langle y_{50} \rangle [m][n] \tag{41}$$

and the spatial variances are given by

$$s^2_{y,dark} = \frac{1}{MN-1} \sum_{m=0}^{M-1} \sum_{n=0}^{N-1} \left(\langle y_{dark} \rangle [m][n] - \mu_{y,dark} \right)^2 \tag{42}$$

$$s^2_{y,50} = \frac{1}{MN-1} \sum_{m=0}^{M-1} \sum_{n=0}^{N-1} (\langle y_{50} \rangle [m][n] - \mu_{y,50})^2 \tag{43}$$

The **DSNU** (dark signal nonuniformity) and **PRNU** (photo response nonuniformity) values as defined by the EMVA 1288 standard are based on spatial standard deviations and are given by the following equations

$$DSNU_{1288} = \frac{s_{y,dark}}{K}\,[e^-], \qquad PRNU_{1288} = \frac{\sqrt{s_{y,50}^2 - s_{y,dark}^2}}{\mu_{y,50} - \mu_{y,dark}}\,[\%] \tag{44}$$

The DSNU is defined as the dark spatial standard deviation and is expressed in electrons (e^-) by dividing with the overall system gain K. The PRNU is defined as the 50% saturation spatial standard deviation relative to the mean value and is expressed in %.

The spatial nonuniformities are illustrated by plots of horizontal and vertical profiles of the DSNU and PRNU as seen in the following figure.

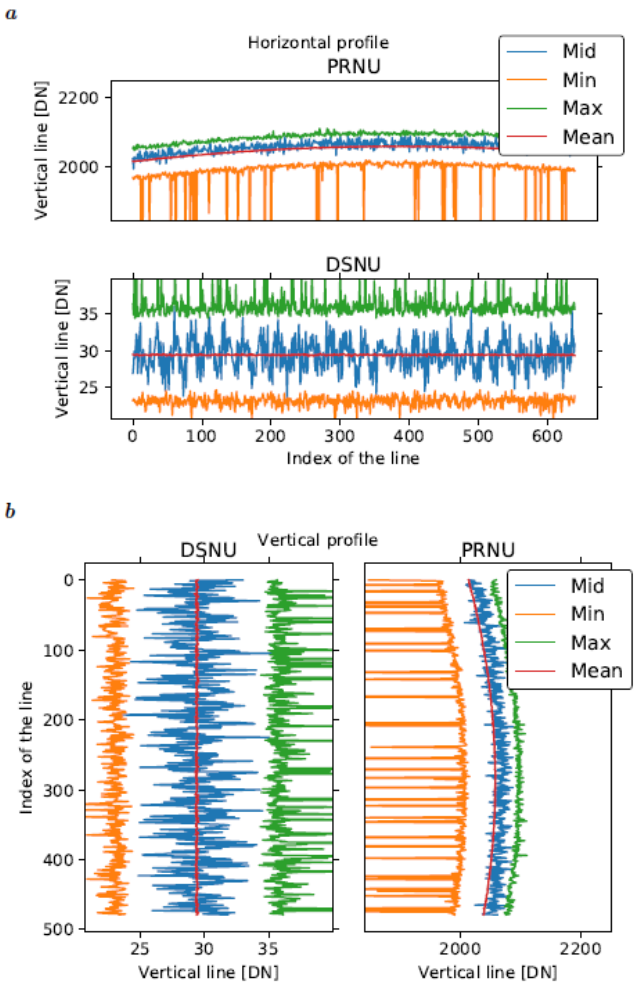

Figure 45: Example horizontal profiles (a) and vertical profiles (b) of spatial nonuniformities as seen in EMVA 1288 standard [39]

Each plot contains the following four plots:

- Mean: Average of rows (columns)
- Max: Maximum of all rows (columns)
- Min: Minimum of all rows (columns)
- Middle: Middle row (column)

Defect pixels can be detected using logarithmic histograms for PRNU and DSNU. Before evaluation of PRNU ,a high pass filter is applied to the original mean image by subtracting a 5x5 box-filtered image as seen below

$$y' = y - {}^{5}\mathrm{R} \times y, \quad \text{with} \quad {}^{5}\mathrm{R} = \begin{bmatrix} 1 & 1 & 1 & 1 & 1 \\ 1 & 1 & 1 & 1 & 1 \\ 1 & 1 & 1 & 1 & 1 \\ 1 & 1 & 1 & 1 & 1 \\ 1 & 1 & 1 & 1 & 1 \end{bmatrix} / 25 \tag{45}$$

This method suppresses low frequency spatial variations of the light source without reducing the variance of the white noise significantly. For the proposed 5x5 box filter, the reduction is standard deviation is only 4% (39). No high pass filtering is performed with the DSNU mean image.

Example logarithmic histograms for DSNU and PRNU can be seen in Figure 46. The blue line represents the modeled normal probability density distribution of the pixels, corresponding to the calculated spatial variances (the variance of DSNU has been divided by 0.96 to account for the high pass filtering).

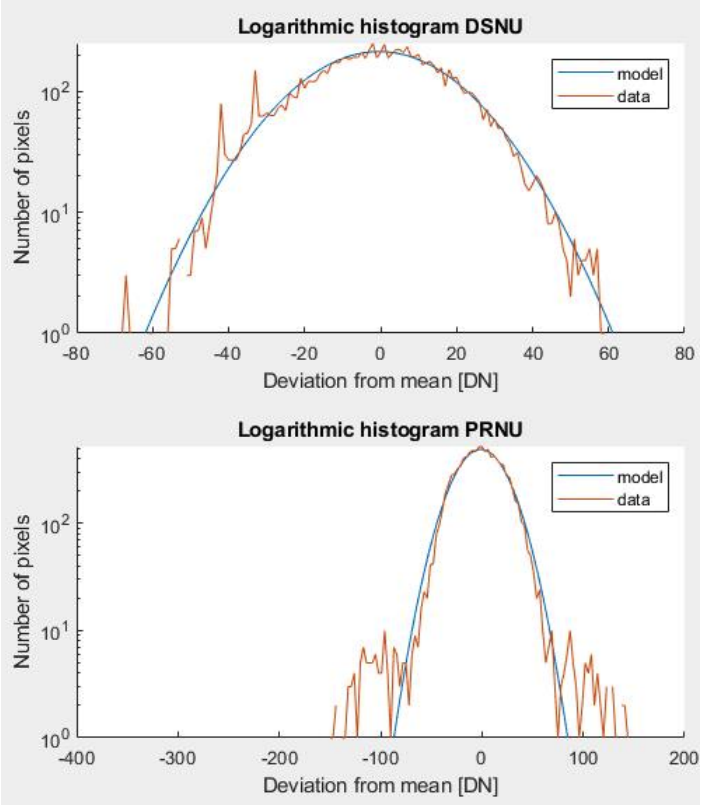

Figure 46: Example logarithmic histograms for DSNU (a) and PRNU (b).

Different thresholds can be used for spotting defect pixels. For example, pixels with a deviation from the mean greater than 4 times the standard deviation (4σ) could be defined as defect. The exact position of these defect pixels in an image can be recorded and a map of defect pixels can be created. This map can be used to replace the values of these pixels by the values of the 8 pixels surrounding them or using some other defect pixel correction technique.

6.2.4 SETUP FOR TESTING EXPOSURE AND FRAME RATE

The presented image sensor is designed to operate at frame rates higher than 200 kfps and with exposures as low as 1us. To verify these specifications of the sensor, an LED Chaser board has been designed and fabricated.

The LED circuit consists of six 4017 decade counters in a cascade configuration. Their outputs are connected to 49 high intensity LEDs. The clock is provided by an external pin, and the LEDs are turning ON and OFF, one at a time (in sequence 1 to 49 as seen in Figure 48), for every clock cycle. After LED 49 turns off, LED 1 turns ON and this “chasing” keeps going on. The schematic and layout of the board fabricated, as designed in Altium, are shown in Figure 47 and Figure 48 respectively.

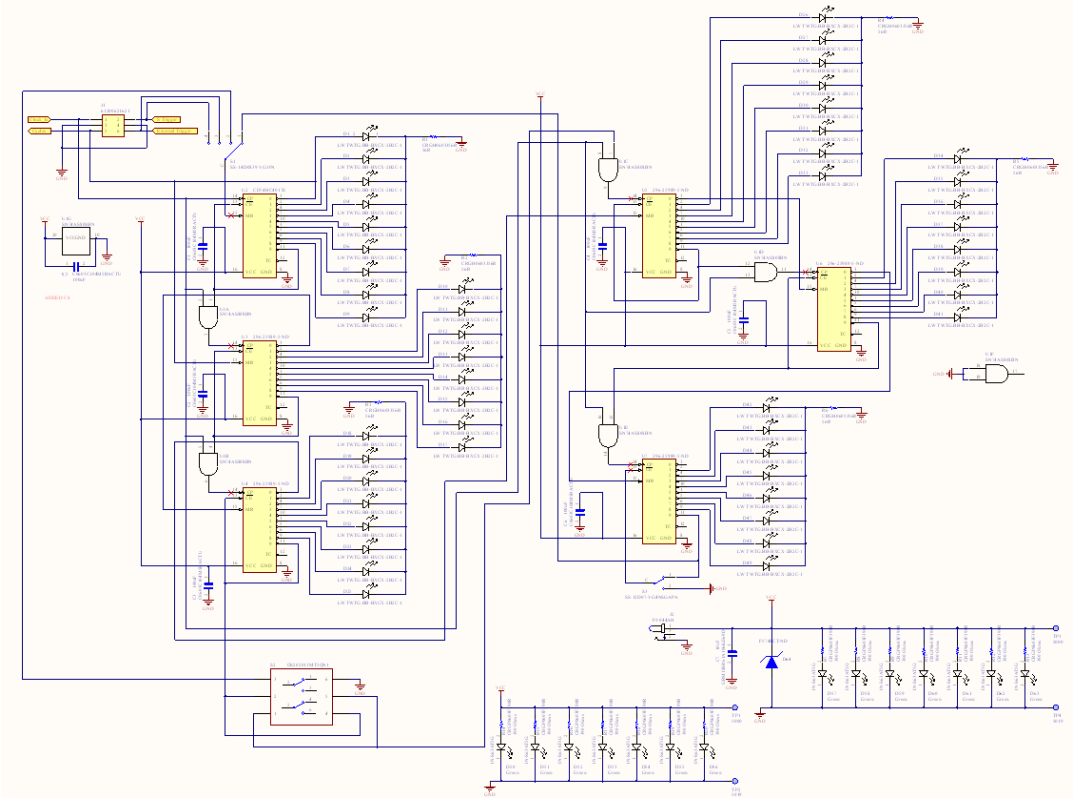

Figure 47: Schematic of the LED Chaser in Altium

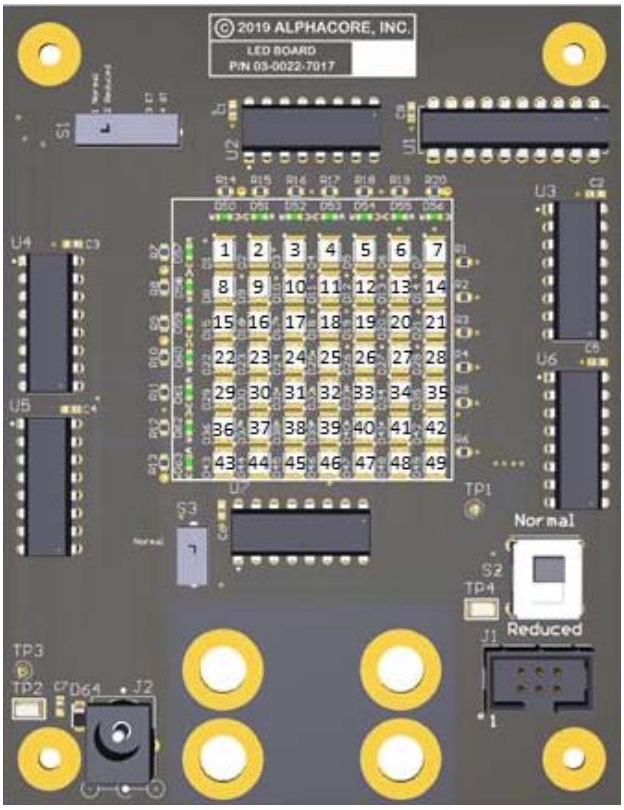

Figure 48: Layout of the LED Chaser board in Altium

Except for the continuous chasing functionality, the board has some more features that are useful for the image sensor testing that will be described in section 6.2.5. It can be triggered externally for the start of its operation. It can operate in reduced mode, where only 25 of the 49 LEDs are rotating. And, finally, it has an output pin that goes high once per chasing cycle, which can be used for measuring times greater than the time provided by one LED chasing cycle.

The testing setup (Figure 49) for the speed and exposure measurements, includes the LED Chaser board and the camera under test with a C-mount lens mounted on it. The lens f-number and focus and the distance between the 2 boards are adjusted so that the captured images are focused and include all the LEDs.

Figure 49: Test setup for measuring exposure and frame speed

The bottom picture in Figure 49 shows also the box that has been designed to protect the users from the high intensity LEDs while testing. The power cables (one per board) and the six wire flat cable that is used to connect the camera board with the LED board (clock, triggers, cycles counting and ground) are not shown in these pictures.

The clock for the LED board will be provided by the camera board using a flex cable. Moreover, the external trigger pin of the camera will be transferred through the same cable. That way the camera and the LED board can be triggered at the same time. A software trigger form the camera is also provided. Finally, the cycles counting pin of the LED board is connected to the camera, so that the camera can track the number of the LED cycles.

6.2.5 METHODS FOR TESTING SENSOR EXPOSURE AND FRAME RATE

The sensor exposure and frame rate can be measured using the setup presented in section 6.2.4. The two boards should be facing each other, and be at the closest possible distance that allows the selected lens to focus properly and the captured images to include all the LEDs.

To measure the **Exposure** of the image sensor we set the clock period of the LED board, T_{LED} to be smaller the Exposure, E. The number of the LEDs that are ON (Bright) in the captured image, B, can be used to measure the exposure, which will be within the range given by the following equation

$$(B-1) \times T_{LED} \leq E < B \times T_{LED} \tag{46}$$

For example, if 3 LEDs are on and T_{LED} is 1us (1 MHz), the exposure will be between 2 us and 3 us. For a smaller clock period of 200ns (5 MHz), if 15 LEDs are ON, the exposure will be between 2.8 us and 3 us.

To test the **Frame Rate** of the image sensor, f_{sensor}, the LED board should operate in its reduced mode, in which only 25 out of the total 49 LEDs are rotating, and the LED clock frequency, f_{LED}, has to be set higher than the frequency of the sensor according to the following equation

$$f_{LED} = 25 \times f_{sensor} \tag{47}$$

If the Frame Rate is accurate, the exact same LEDs should be bright in all frames. However, this would also be the case if the frame rate was f_{sensor} / 2. That is why one more test must be performed. The frequency of the LED board is set equal to the expected frame rate. If the expected frame rate is correct then there should be only one LED advancement from frame to

frame. If the frame rate is half of the expected value, then there would be a two LED advancement between consecutive frames.

The **response** of the image sensor can also be measured using the LED board. The LED Chaser should operate in its triggered mode, and both the LED and the camera board should be triggered externally. The trigger could either be software (capture button) or hardware (trigger switch). The frequency of the LED board should be chosen to be as small as possible to increase measurements accuracy, but the ratio of the Exposure time over the LED clock period should always be kept bellow 50, to ensure that the image captures the ON time of the LEDs in one cycle only, otherwise all LEDs would be bright and the response time would not be possible to be measured.

Finally, the **synchronization** of more than one cameras can be tested by using the LED board. Again, the LED frequency should be chosen according to the exposure of the cameras to be tested. The cameras have to be focused on the same LED board, and the exact same LEDs will be bright if the cameras are synchronized. Alternatively, two set of cameras – LED boards can be used and the mismatch in the captured images will be the synchronization error.

6.2.6 OTHER TESTS

Two more tests will be performed to measure the on-chip memory leakages and the inter-frame nonuniformity of the image sensor. The setup presented in 6.2.1 will be used.

To measure the **leakages** of the sensor, the reading procedure will be delayed by 10ms and 20ms and the mean values of the frames will be compared. To suppress the temporal noise 10 images will be captured for each delay, and the sensor will operate at 50% saturation level

throughout this test. Ten images will be enough here because mean values of whole images will be used instead of individual pixel values. The resulting memory leakage rate will be given in DN/ms using the following equation

$$Q_{leakage}\left[\frac{DN}{ms}\right] = \frac{\mu_{y,\tau_d} - \mu_{y,0}}{\tau_d} \tag{48}$$

where μ_{y,τ_d} is the mean output of the sensor in Data Numbers when the readout is delayed by τ_d.

The leakage rate can also be given in units of uV/ms by multiplying the amount of leakage calculated in (48) by V_{LSB}, which is 439uV for a 12-bit 1.8V ADC. To refer this leakage back to where it occurs, the on-chip memory, we have to divide $Q_{leakage}$ with the gain added to the camera because of the memory blocks, as given in equation (12). The resulting leakage in the memories will be

$$Q_{leakage}\left[\frac{uV}{ms}\right] = \frac{Q_{leakage}\left[\frac{DN}{ms}\right]}{A_{memory}} \times V_{LSB}\left[\frac{uV}{DN}\right] \tag{49}$$

To measure the **nonuniformity** of the image sensor for all the captured frames, a similar method to what was used to measure intra-frame (within the same frame) nonuniformity of the sensor will be used.

The means of the means of the hundred M x N dark and 50% saturation images for all F captured frames, $\langle y_{dark}\rangle$ and $\langle y_{dark}\rangle$ respectively, are given by

$$\mu_{y,dark,F} = \frac{1}{FMN}\sum_{f=0}^{F-1}\sum_{m=0}^{M-1}\sum_{n=0}^{N-1}\langle y_{dark}\rangle[f][m][n], \quad \mu_{y,50,F} = \frac{1}{FMN}\sum_{f=0}^{F-1}\sum_{m=0}^{M-1}\sum_{n=0}^{N-1}\langle y_{50}\rangle[f][m][n] \tag{50}$$

and the spatial variances for all the captured frames are given by

$$s_{y,dark,F}^2 = \frac{1}{FMN-1}\sum_{f=0}^{F-1}\sum_{m=0}^{M-1}\sum_{n=0}^{N-1}\left(\langle y_{dark}\rangle[f][m][n] - \mu_{y,dark,F}\right)^2 \tag{51}$$

$$s_{y,50,F}^2 = \frac{1}{FMN-1}\sum_{f=0}^{F-1}\sum_{m=0}^{M-1}\sum_{n=0}^{N-1}\left(\langle y_{50}\rangle[f][m][n] - \mu_{y,50,F}\right)^2 \tag{52}$$

The **DSNU** (dark signal nonuniformity) and **PRNU** (photo response nonuniformity) for all the captured frames are based on spatial standard deviations and are given by the following equations

$$DSNU_{Full} = s_{y,dark,F}\,[DN], \qquad PRNU_{Full} = \frac{\sqrt{s_{y,50,F}^2 - s_{y,dark,F}^2}}{\mu_{y,50} - \mu_{y,dark}}\,[\%] \tag{53}$$

The spatial nonuniformities for all the frames can be illustrated by plots of horizontal and vertical profiles of the DSNU and PRNU similar to the ones shown in Figure 45. For the horizontal profiles, nonuniformities will be plotted for the frames being side by side. For the vertical profiles, nonuniformities will be plotted for the frames being the one the one below the other.

Finally, the dark and 50% saturation means, and the DSNU and PRNU for each of the captured frames will be plotted. The signal variations in different frames and their nonuniformity performance can now be seen.

6.3 TESTING SOFTWARE

All images needed for the testing methods described in section 6.2 are captured using the software described in section 5.2. All the parameters are calculated, and all the plots are created using software that was developed in MATLAB, following the equations and procedures described in section 6.2.

The developed MATLAB code developed is able to read from either of the 8-bit bmp images or the 12-bit images information saved in csv format. Moreover, code was developed that converts the 12-bit images information to 16-bit png images, which can be used for further characterization in software that uses images as input.

A basic tutorial of a software developed in Python by European Machine Vision Association (EMVA), uses images as input, and generate complete EMVA reports can be seen in [47]. All the calculations and plots in this work that are related to the EMVA 1288 standard are generated exclusively using the developed MATLAB code, but were also cross-checked using the python code provided by EMVA.

A full description of the performance of the image sensor presented in this work, and all the generated plots can now be seen in CHAPTER 7.

CHAPTER 7: IMAGE SENSOR PERFORMANCE

The methods described in section 6.2 were used to characterize the performance of the image sensor. The results for sensitivity, linearity, noise and nonuniformity are given in section 7.1. In section 7.2, the sensor is tested for nonuniformity for all the captured frames. In section 7.3, the leakage measurements for the analog memory are given. In section 7.4, the accuracy of the exposure and frame rate of the image sensor is verified. And finally, in section 7.5, the performance of the sensor, based on the testing results is summarized and compared to the expected performance.

7.1 SENSITIVITY, LINEARITY, NOISE AND NONUNIFORMITY

The plots generated using the methods described in section 6.2.2, and EMVA 1288 standard [39], can be seen in figures 50 to 54. The first four figures show the photon transfer, the sensitivity, the linearity and the Signal-to-Noise Ratio curves of the image sensor under different testing conditions that will be used for this section and are listed here:

- Case 1: 450nm light, 300us exposure, 3.3kfps
- Case 2: 550nm light, 300us exposure, 3.3kfps
- Case 3: 600nm light, 300us exposure, 3.3kfps
- Case 4: 425nm - 700nm light, 3us exposure, 200kfps

The reason that the tests for cases 1 to 3 is at lower frame rate, is because the filtered light of the used light source is not enough to generate enough photons to perform the required testing from dark to saturation. In case four, light is enough but the incident photons measurement is approximate since used power meter can only measure light at a specific wavelength.

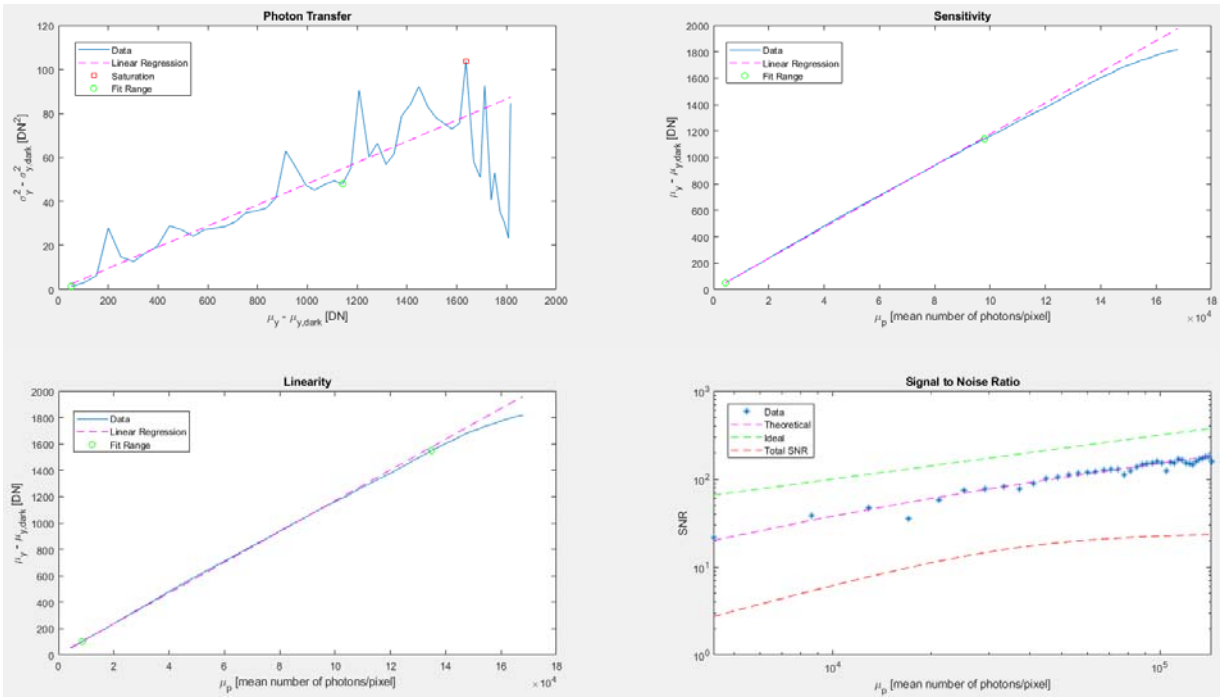

Figure 50: Photon transfer, Sensitivity, Linearity and SNR curves [Case 1]

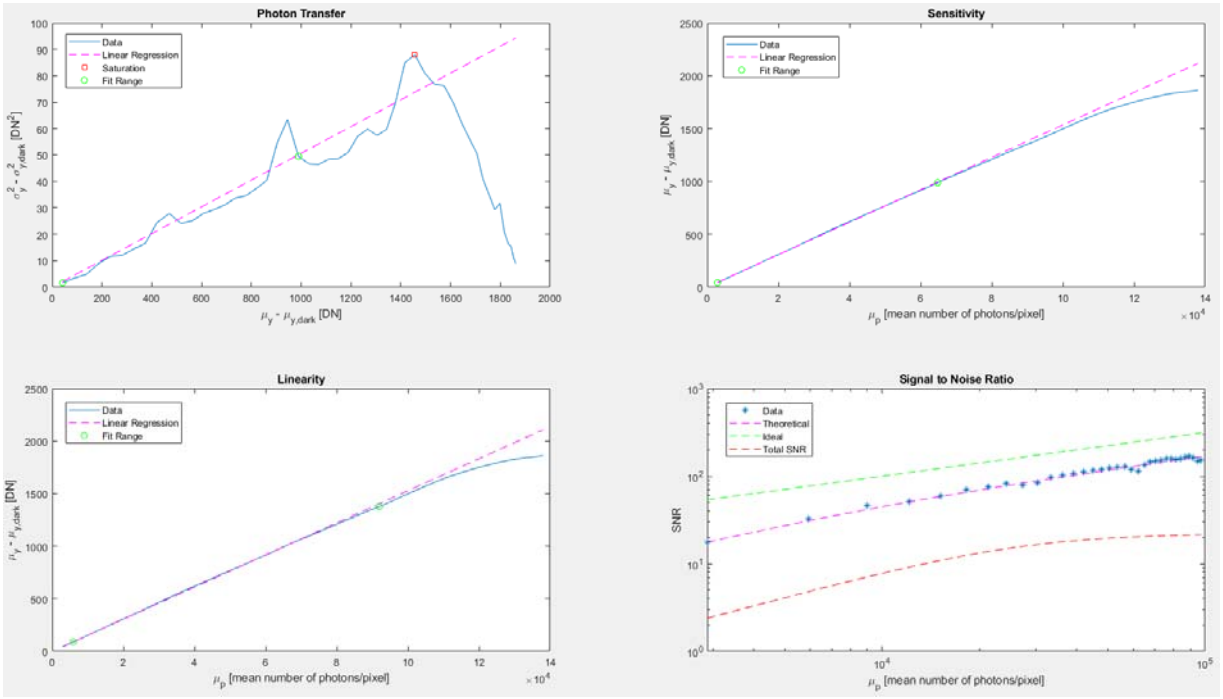

Figure 51: Photon transfer, Sensitivity, Linearity and SNR curves [Case 2]

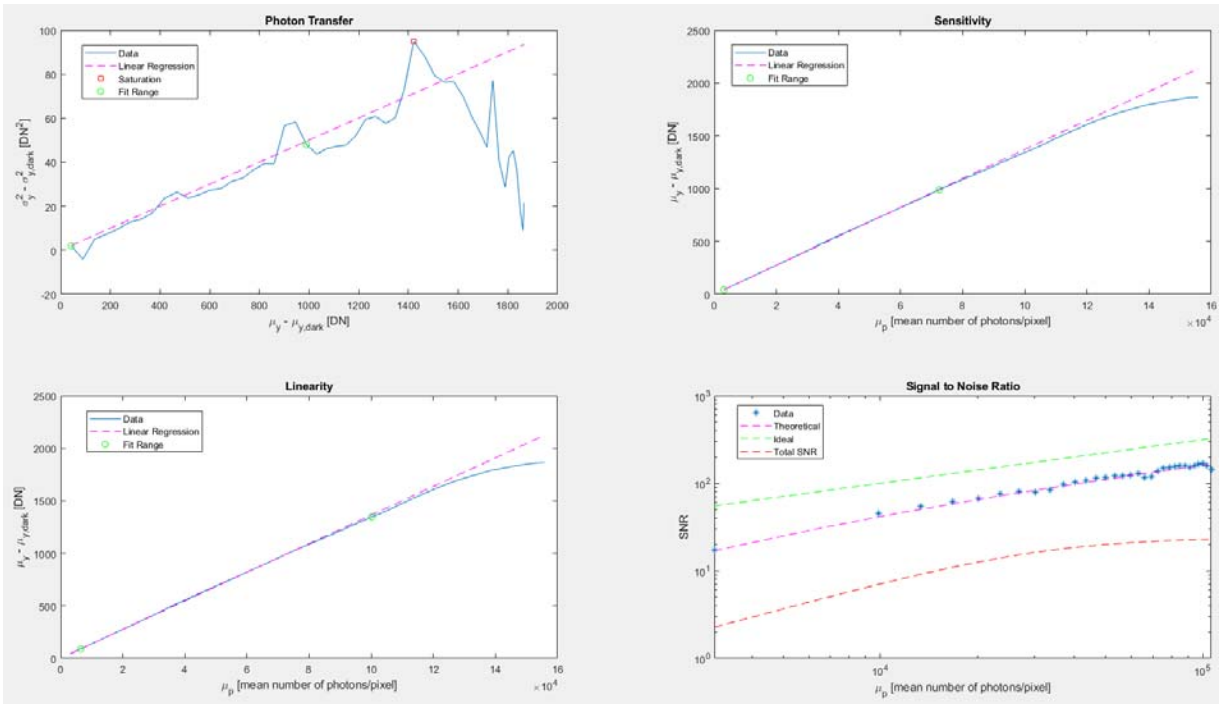

Figure 52: Photon transfer, Sensitivity, Linearity and SNR curves [Case 3]

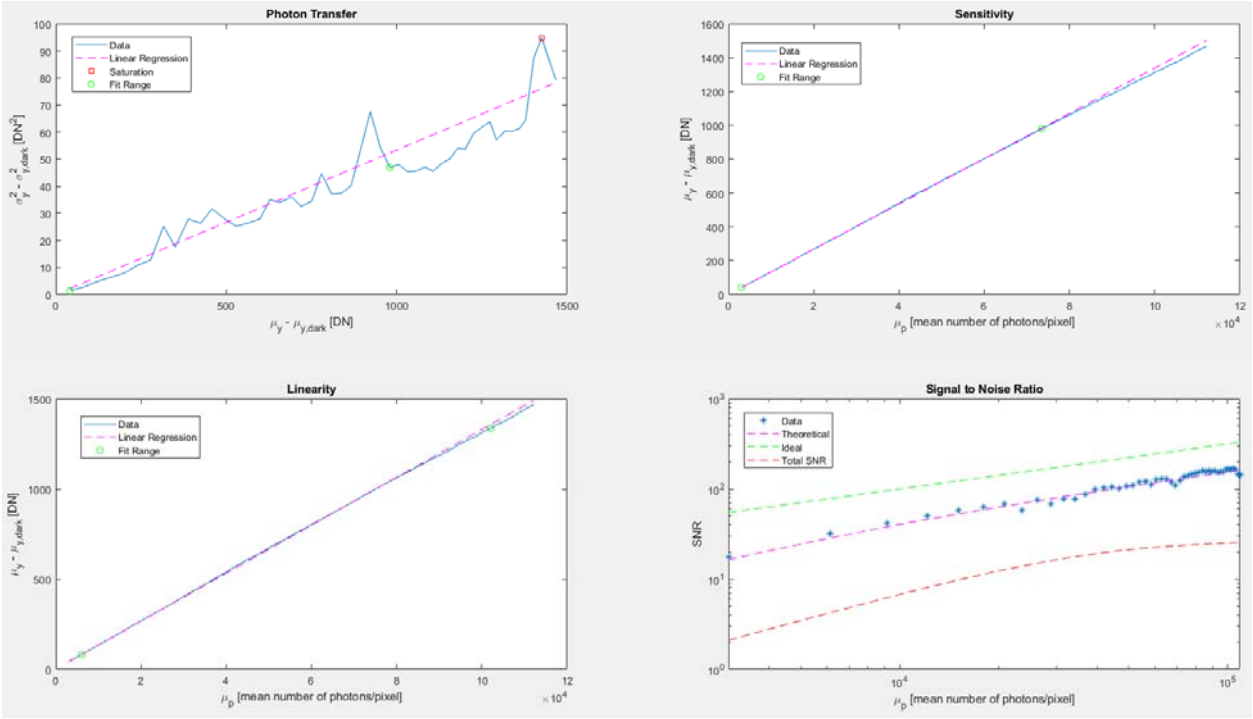

Figure 53: Photon transfer, Sensitivity, Linearity and SNR curves [Case 4]

It should be noted, that since the amounts of photons in case 4 is approximate, because of the lack of a direct measuring method, the curves seen in Figure 53 are accurate for extracting all the required performance characteristics except for the quantum efficiency. This should not be a problem, since the quantum efficiency of the sensor is characterized for different wavelengths in cases 1 to 3.

The following figure shows the percentage deviation of the linearity curves from the linear regression lines seen in the four previous figures for cases 1 to 4.

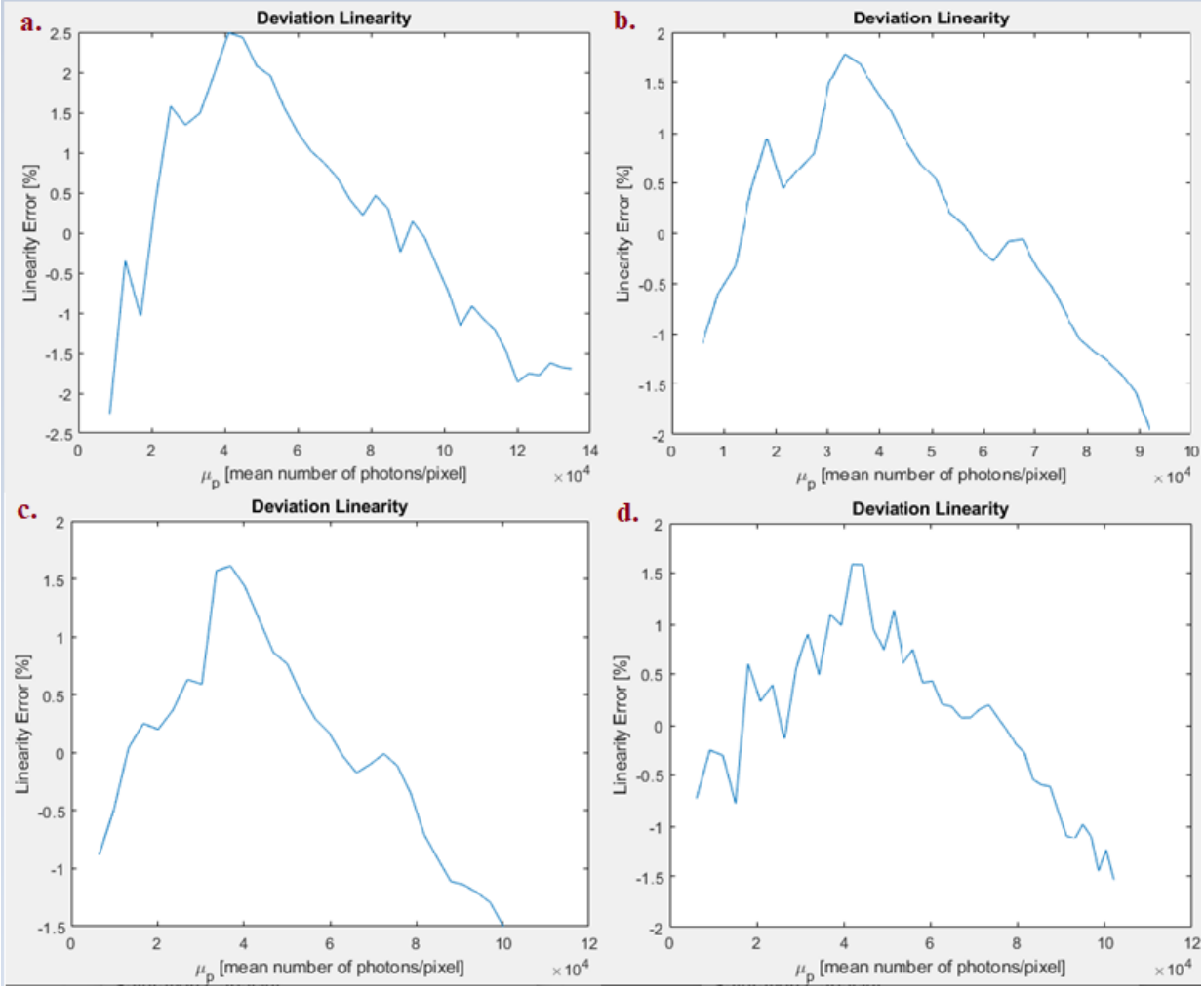

Figure 54: Percentage deviation from linear regression for cases 1 to 4 (a to d respectively)

The spatial nonuniformities of the sensor are illustrated by plots of horizontal and vertical profiles of DSNU and PRNU in figures 55 to 58. Each sub-figure contains four profiles (mean, max, min and middle row or column) as described in section 6.2.3. The PRNU profiles were created using images at about 50% saturation. The DSNU profiles are the same for figures 55 to 57, since the same 100 images where used for dark signal nonuniformities for 300us exposure at 3.3kfps operation. In Figure 58, the DSNU profile is different, because a different set of 100 dark images captured at 3us and 200kfps were used.

In case 4, only the bottom half of the image sensor is used for all the measurements and plots in this section. This is because, as it will be explained in section 7.3, the leakages of the memories are very high when the sensor is exposed to a very strong light. Since the light that is used for testing the image sensor with 3us exposure needs to be very strong, to characterize the performance of the sensor at its full range, the only way to make the sensor functional for the required testing is to cover the memories. And because the foundry did not have a special layer for this reason, and not any other high accuracy method was used to block the light above the memories, this was done in an approximate manner, covering the light above the memories at the lens mount level.

Since the method used to block the light was approximate, not all the memories were covered uniformly, and the top memories were partially exposed, degrading their performance and consequently the performance of the sensor. Therefore, only the bottom part of the sensor was used for all the tests in this section, because the memories corresponding to the bottom part of the pixel array were fully covered, hence, their performance was not hurt by the excessive light.

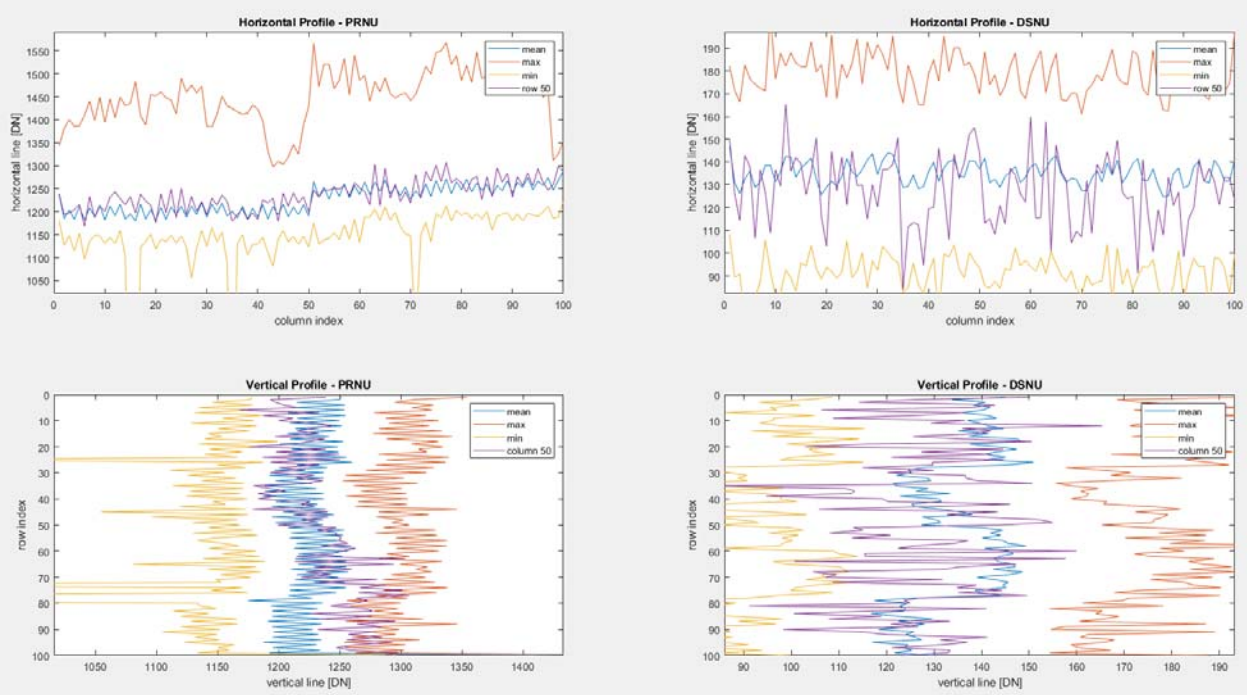

Figure 55: Horizontal and Vertical profile of PRNU (left) and DSNU (right) [Case 1]

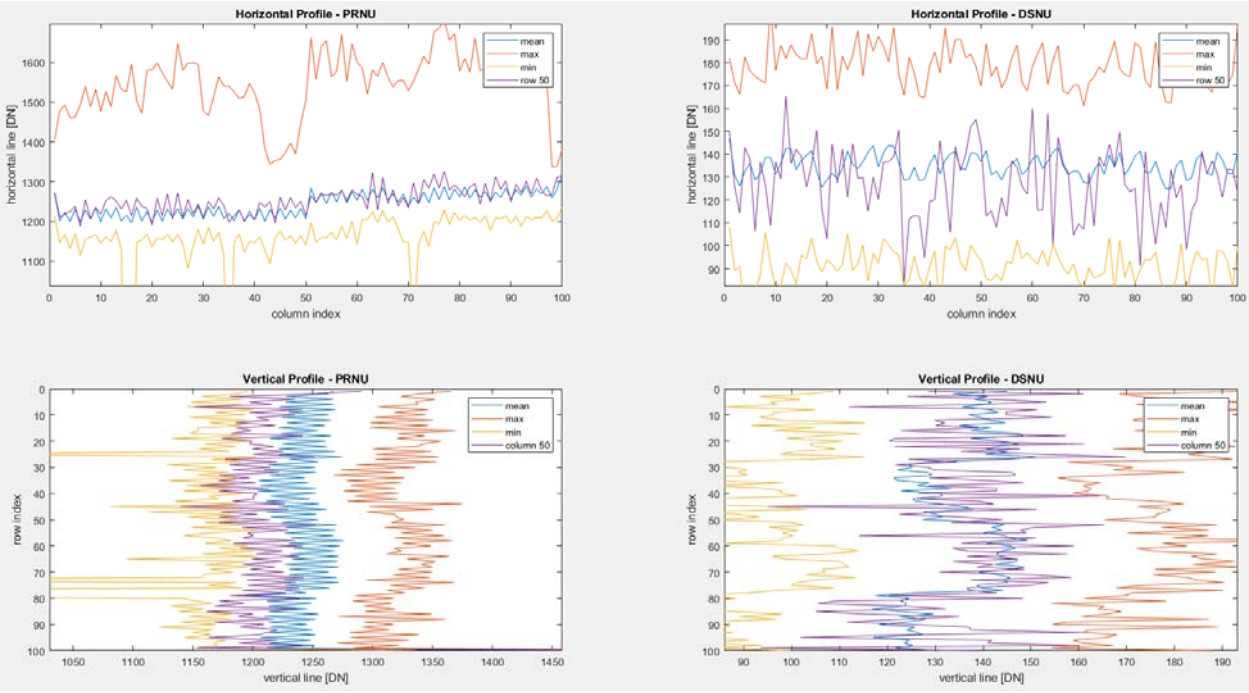

Figure 56: Horizontal and Vertical profile of PRNU (left) and DSNU (right) [Case 2]

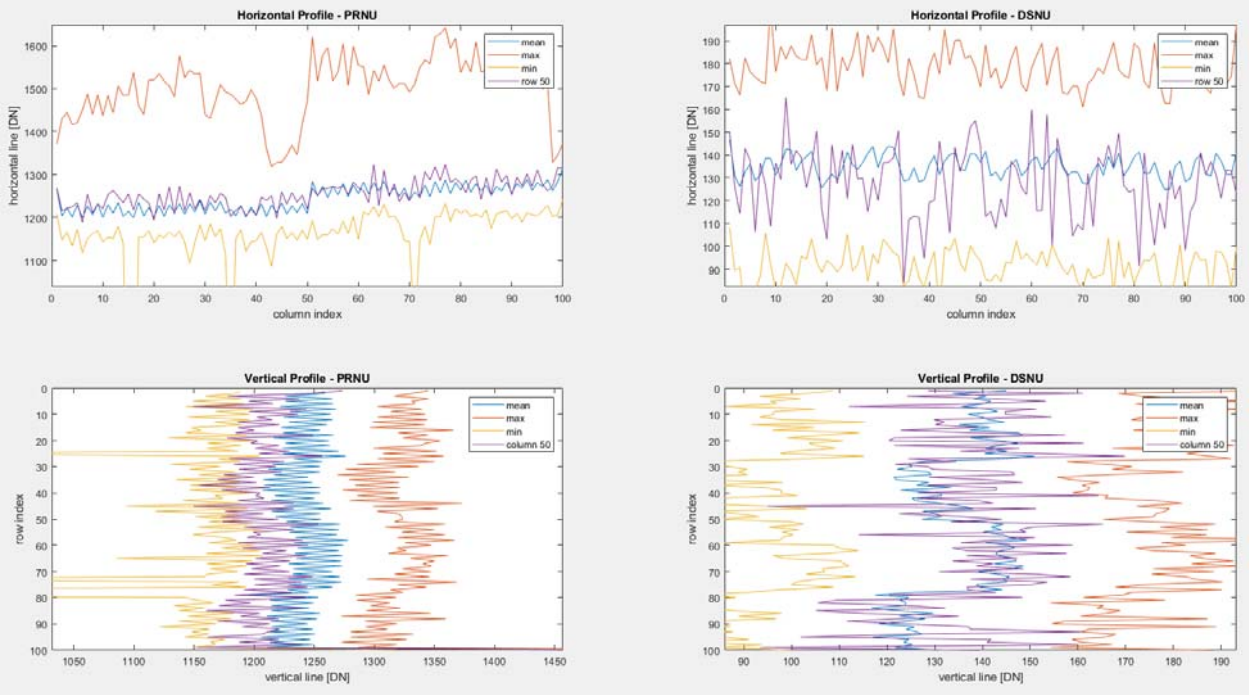

Figure 57: Horizontal and Vertical profile of PRNU (left) and DSNU (right) [Case 3]

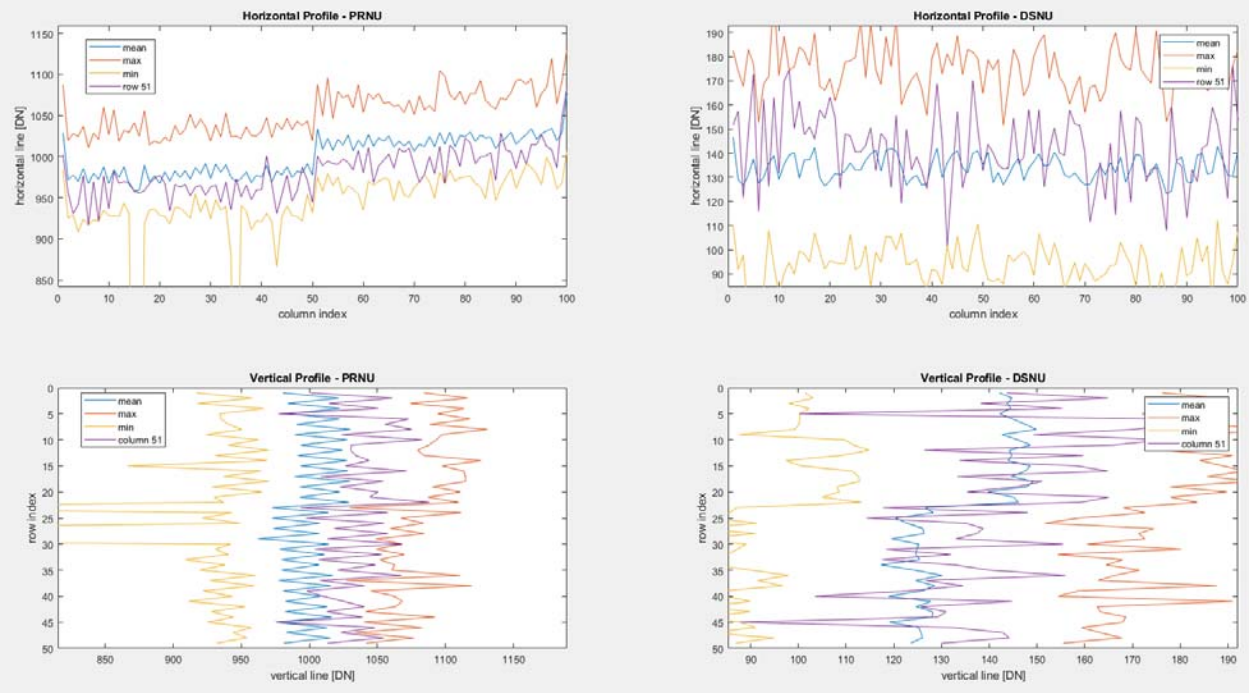

Figure 58: Horizontal and Vertical profile of PRNU (left) and DSNU (right) [Case 4]

Logarithmic histograms for DSNU and PRNU for all the four testing cases can be seen in figures 59 to 62. Before the evaluation of the PRNU average image, it was high-pass filtered as described in section 6.2.3.

The blue line, in all plots, is the normal probability density distribution corresponding to the dark or 50% saturation measured spatial variance. The pixels outside this line can be characterized defected (defect pixel definition depends on the application), but in our case these pixels are very limited for the first three cases and almost do not exist in case 4.

Most of the pixels that deviate more than expected from the mean are at the edges of the sensor, which are not usually used for image creation. Moreover, in this work the calibration of the images for spatial nonuniformities is very limited and out of scope.

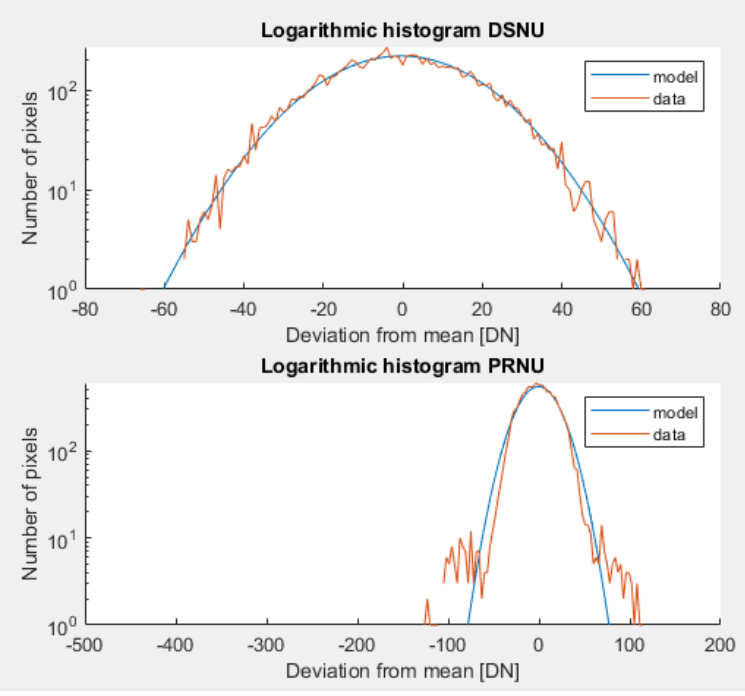

Figure 59: Logarithmic histograms for DSNU (up) and PRNU (down) [Case 1]

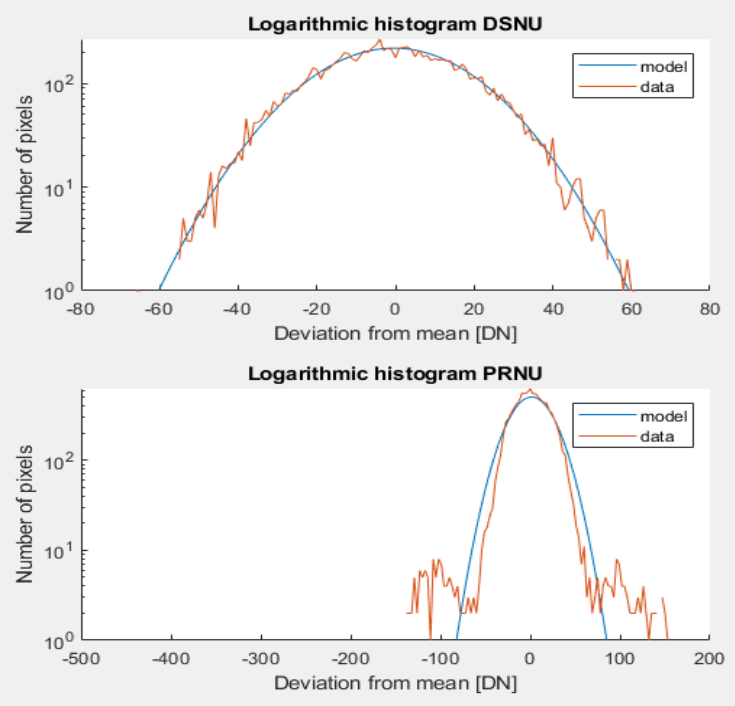

Figure 60: Logarithmic histograms for DSNU (up) and PRNU (down) [Case 2]

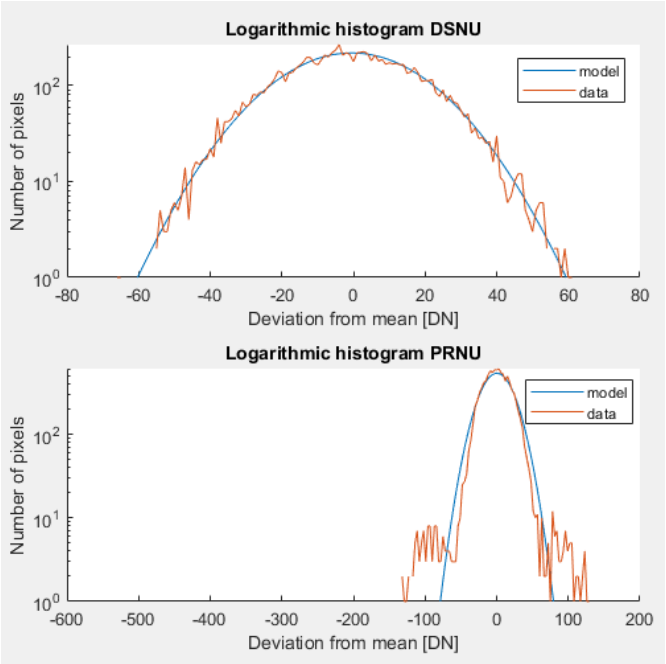

Figure 61: Logarithmic histograms for DSNU (up) and PRNU (down) [Case 3]

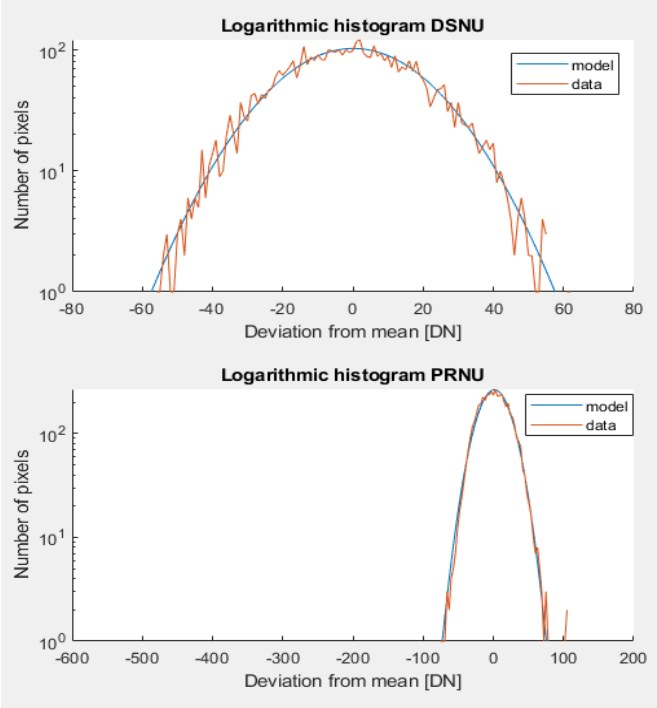

Figure 62: Logarithmic histograms for DSNU (up) and PRNU (down) [Case 4]

The results that can be extracted from the figures above and from the calculations described in sections 6.2.2 and 6.2.3, as given by the software created for testing, described in section 6.3, can be seen in Figure 63 for cases 1 to 3, and Figure 64 for case 4.

It should be noted that for case 4 (Figure 64), the quantum efficiency calculation and all the quantities that are in photons are approximate, since no accurate method for the measurement of incident photons at the sensor was available for white light. Moreover, these tests are ideally performed with monochromatic light with a FWHM of less than 50nm or white light and an appropriate bandpass filter [39]. However, all the other results, like system gain, SNR, DR, nonuniformities and linear errors are expected to be accurate. The quantum efficiency of the sensor can be extracted from cases 1 to 3.

Quantum Efficiency:	24.5 %	30.3 %	27.4 %
System Gain:	0.048 DN/e^-	0.051 DN/e^-	0.050 DN/e^-
Temporal Dark Noise			
without quantization noise:	41.524 e^-	39.446 e^-	39.871 e^-
with quantization noise:	2.019 DN	2.019 DN	2.019 DN
Signal-to-Noise Ratio (max)			
----------	187	172	171
----------	45.46 dB	44.69 dB	44.63 dB
----------	7.6 bits	7.4 bits	7.4 bits
Signal-to-Noise Ratio:	43.95 dB	43.62 dB	43.10 dB
----------	7.3 bits	7.2 bits	7.2 bits
Absolute Sensitivity Threshold			
----------	173.5 p	133.1 p	149.0 p
----------	0.8 p /μm^2	0.6 p /μm^2	0.7 p /μm^2
----------	42.5 e^-	40.4 e^-	40.8 e^-
----------	0.2 e^- /μm^2	0.2 e^- /μm^2	0.2 e^- /μm^2
Saturation Capacity			
----------	143518 p	97231 p	106195 p
----------	629.4 p /μm^2	426.4 p /μm^2	465.7 p /μm^2
----------	35123 e^-	29474 e^-	29070 e^-
----------	154.0 e^- /μm^2	129.3 e^- /μm^2	127.5 e^- /μm^2
Dynamic Range:	58.35 dB	57.27 dB	57.06 dB
----------	9.7 bits	9.5 bits	9.5 bits
Spatial Nonuniformities			
$DSNU_{1288}$ ----------	379.0 e^-	360.0 e^-	363.9 e^-
----------	18.2 DN	18.2 DN	18.2 DN
$PRNU_{1288}$ ----------	4.1 %	4.4 %	4.1 %
Linearity Error			
MAX ----------	2.5 %	1.8 %	1.6 %
MIN ----------	-2.3 %	-2.0 %	-1.5 %

Figure 63: Sensor performance at 450nm, 550nm and 600nm (left to right) [Cases 1 to 3]

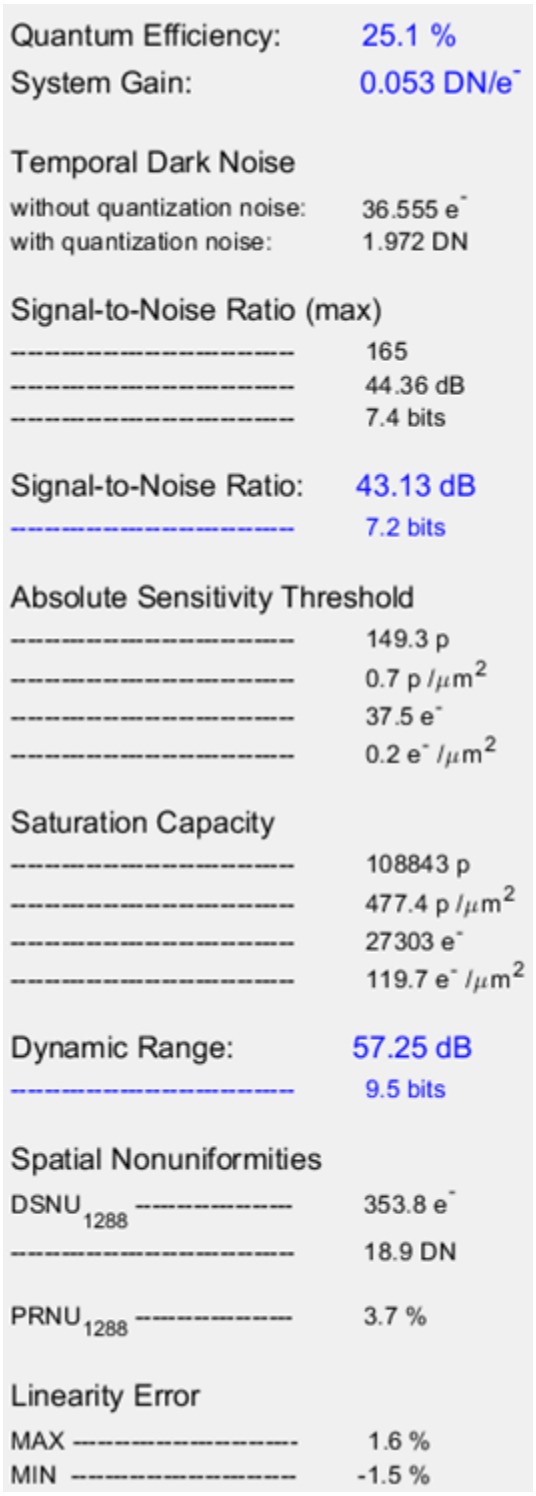

Figure 64: Sensor performance at 200kfps [Case 4]

The calculated Quantum Efficiency in Figure 63 and Figure 64 is the effective QE (EQE). It is the product of the QE of the sensor due to the physics of the process used, the fill factor and the transmission losses through the protective glass at the bottom of the lens mount. The typical transmission percentage through the optical window used on the lens mount for mechanical and dust protection of the sensor can be seen in the following figure.

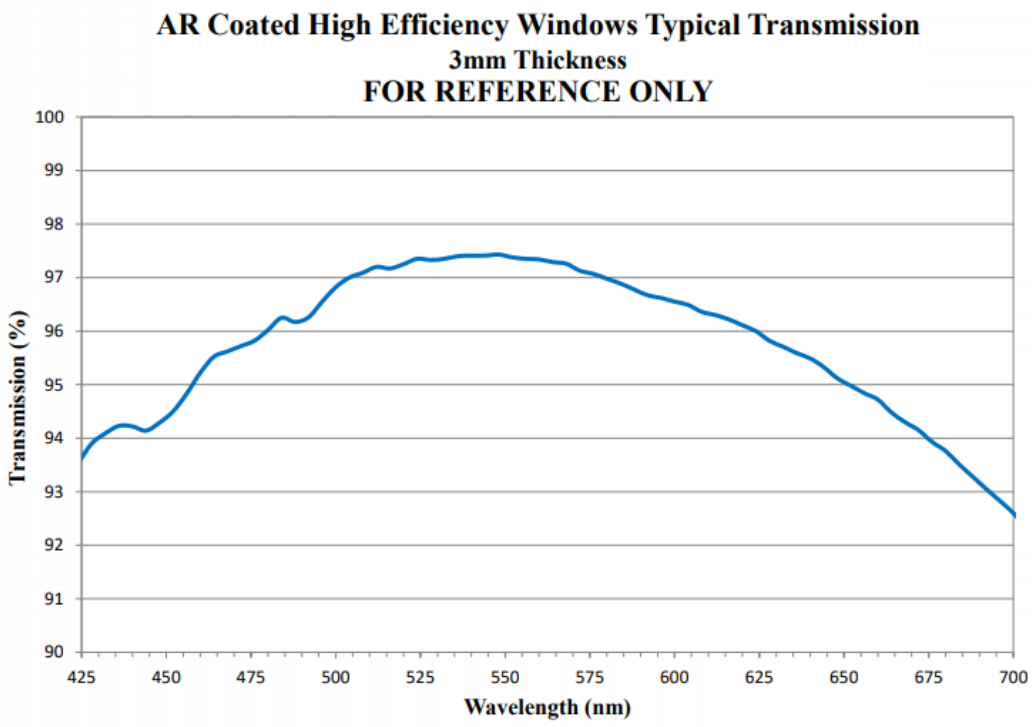

Figure 65: Typical transmission percentage of the optical window used for sensor protection

More about how the results above compare to the expected results will be discussed in section 7.5.

7.2 ALL FRAMES NONUNIFORMITIES

The nonuniformities for the fourteen first captured frames, for all the four cases described in section 7.1, were calculated using the equations given in section 6.2.6. The calculated DSNU and PRNU are given in Table 5. As can be seen, the spatial nonuniformities for all the captured frames of the sensor are very close to the values calculated in the previous section for a single frame.

Case #	1	2	3	4
DSNU (DN)	20.8			21.4
PRNU (%)	4.1	4.5	4.1	3.6

Table 5: DSNU and PRNU for all captured frames

The average outputs, the dark signal and photo response nonuniformities per frame can be seen in the following figures. Moreover, the horizontal and vertical profiles of PRNU and DSNU for all the captured frames can also be seen.

In all of these figures it can be clearly seen that frame 7 has lower output averages than the other frames. This can be easily detected by naked eye, especially for dark images like the one shown in Figure 38. The reason this happens is layout dependent, it has been detected (increased parasitic capacitance) and will be fixed in a future tapeout by more careful layout design. However, it can also be easily fixed using software.

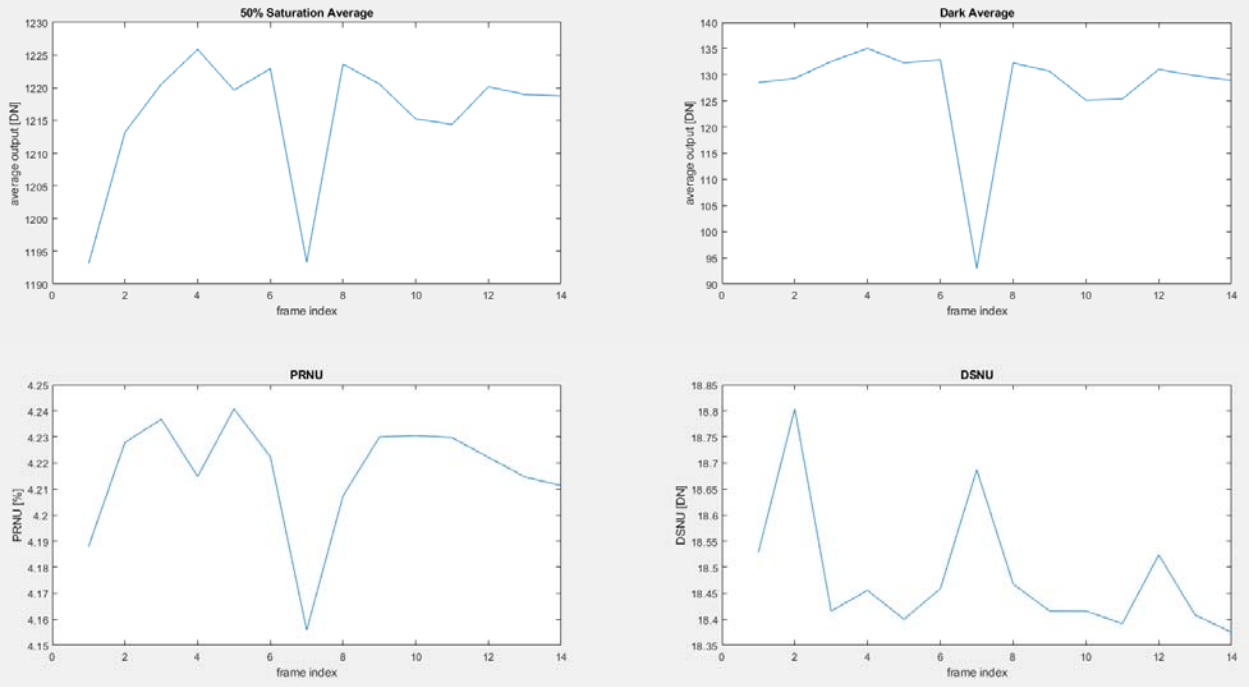

Figure 66: Averages and nonuniformities for all frames [Case 1]

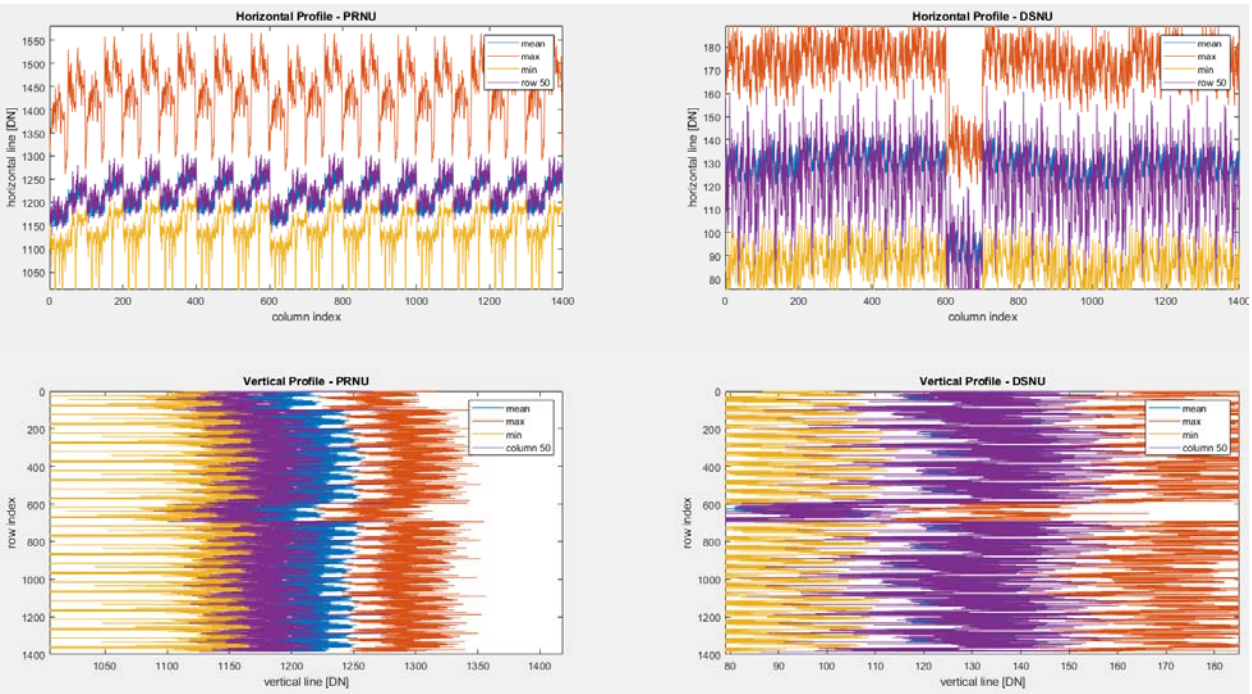

Figure 67: Horizontal and Vertical profile of nonuniformities for all frames [Case 1]

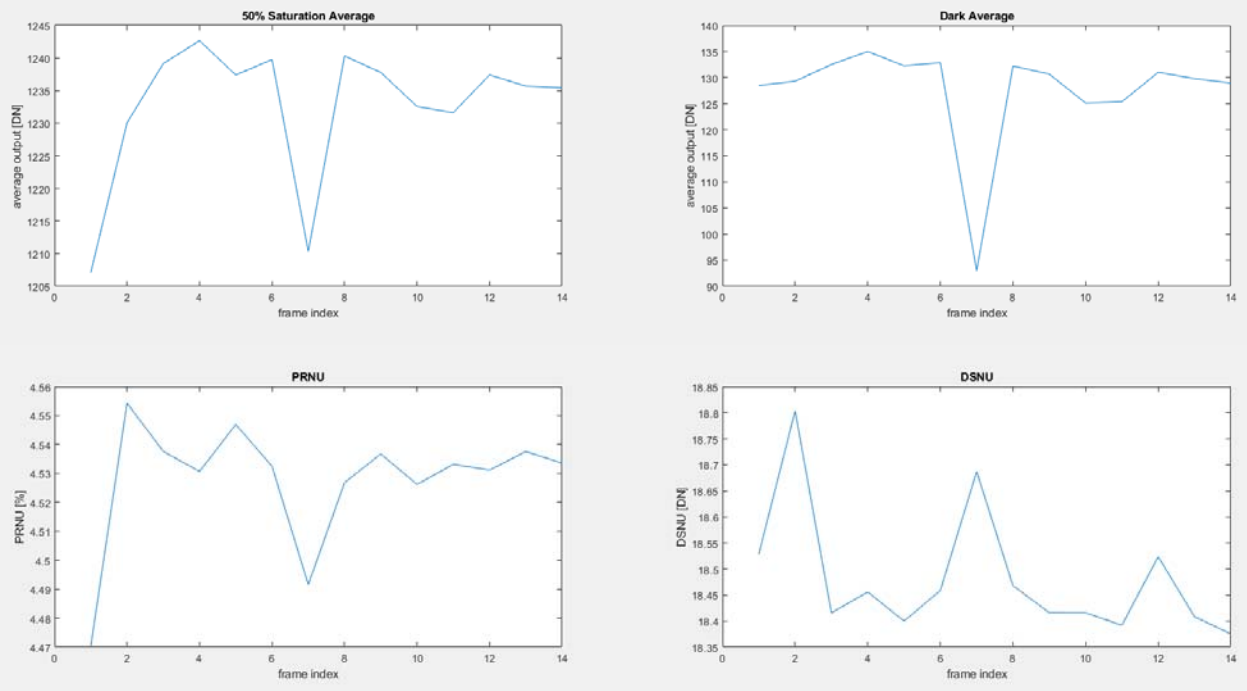

Figure 68: Averages and nonuniformities for all frames [Case 2]

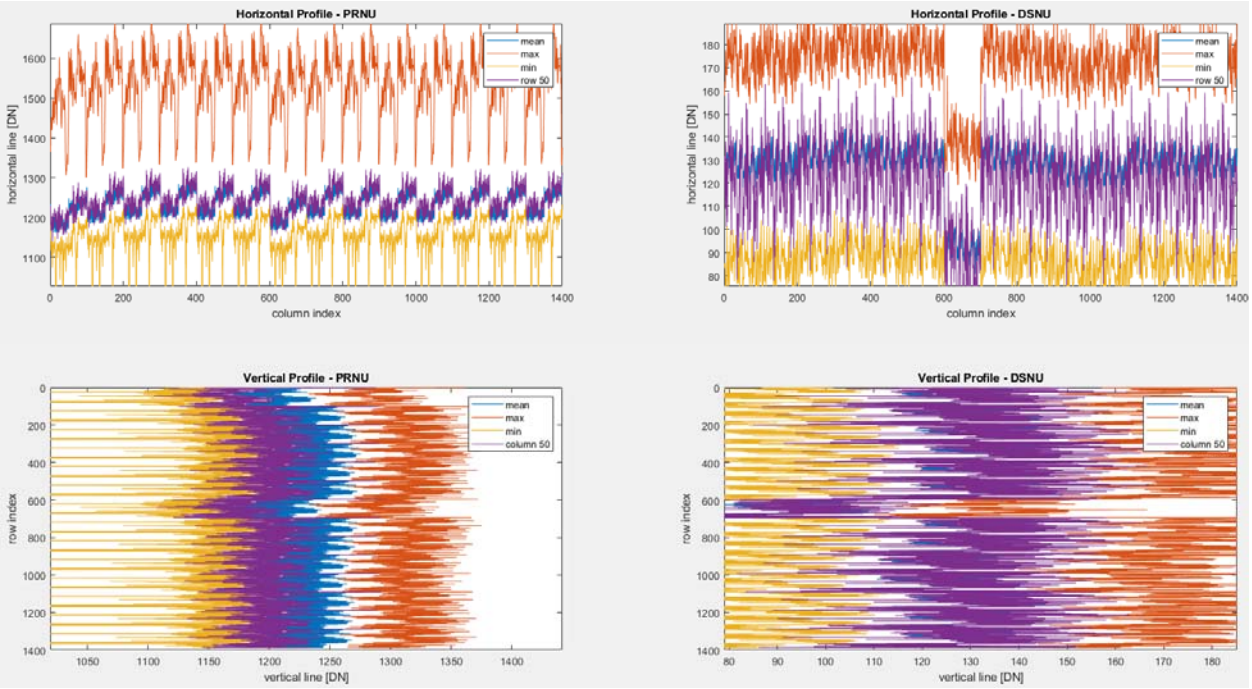

Figure 69: Horizontal and Vertical profile of nonuniformities for all frames [Case 2]

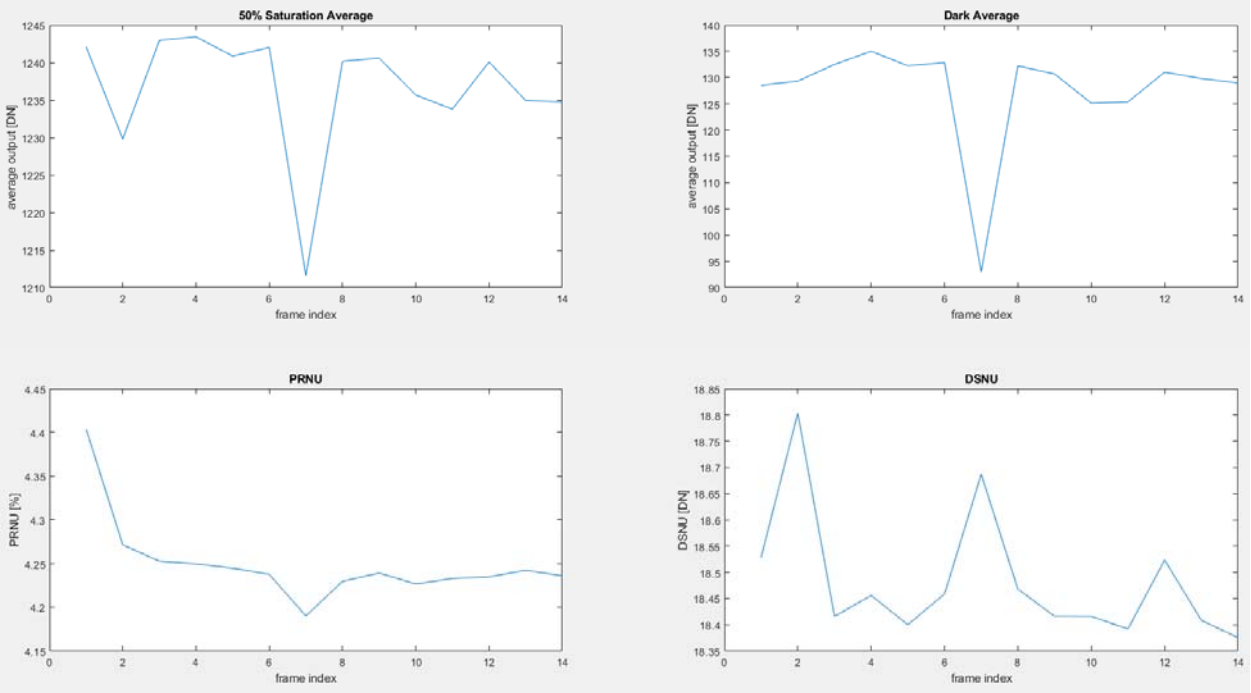

Figure 70: Averages and nonuniformities for all frames [Case 3]

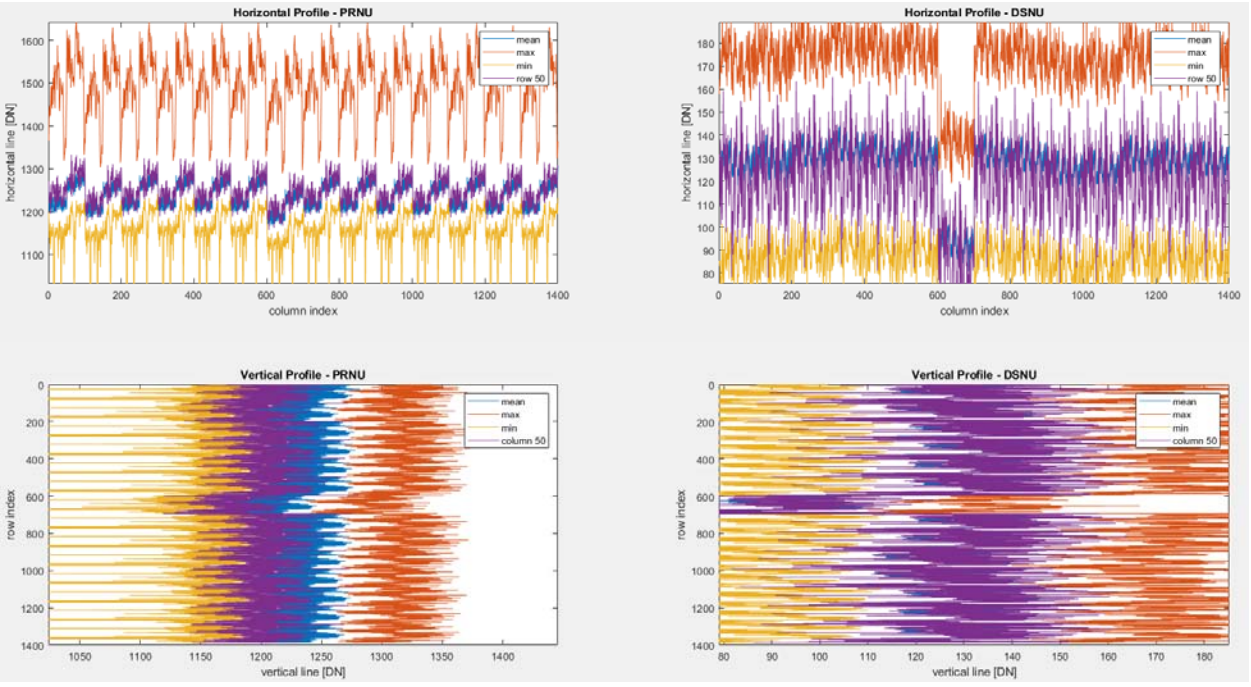

Figure 71: Horizontal and Vertical profile of nonuniformities for all frames [Case 3]

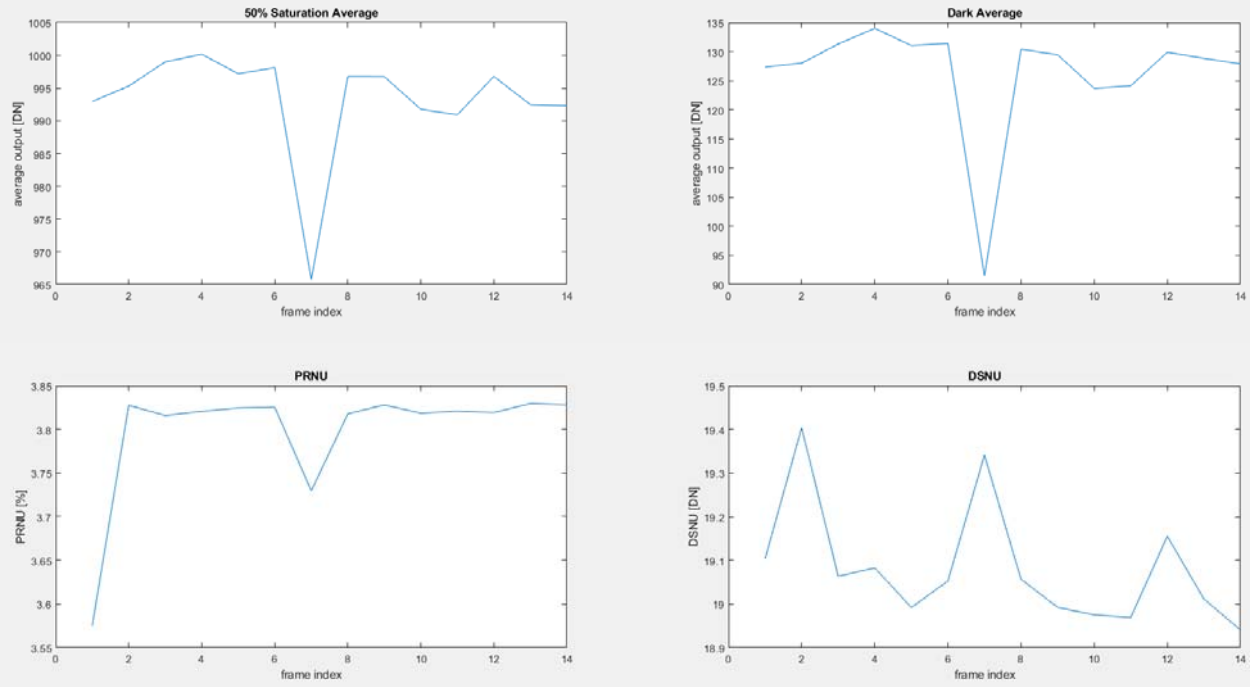

Figure 72: Averages and nonuniformities for all frames [Case 4]

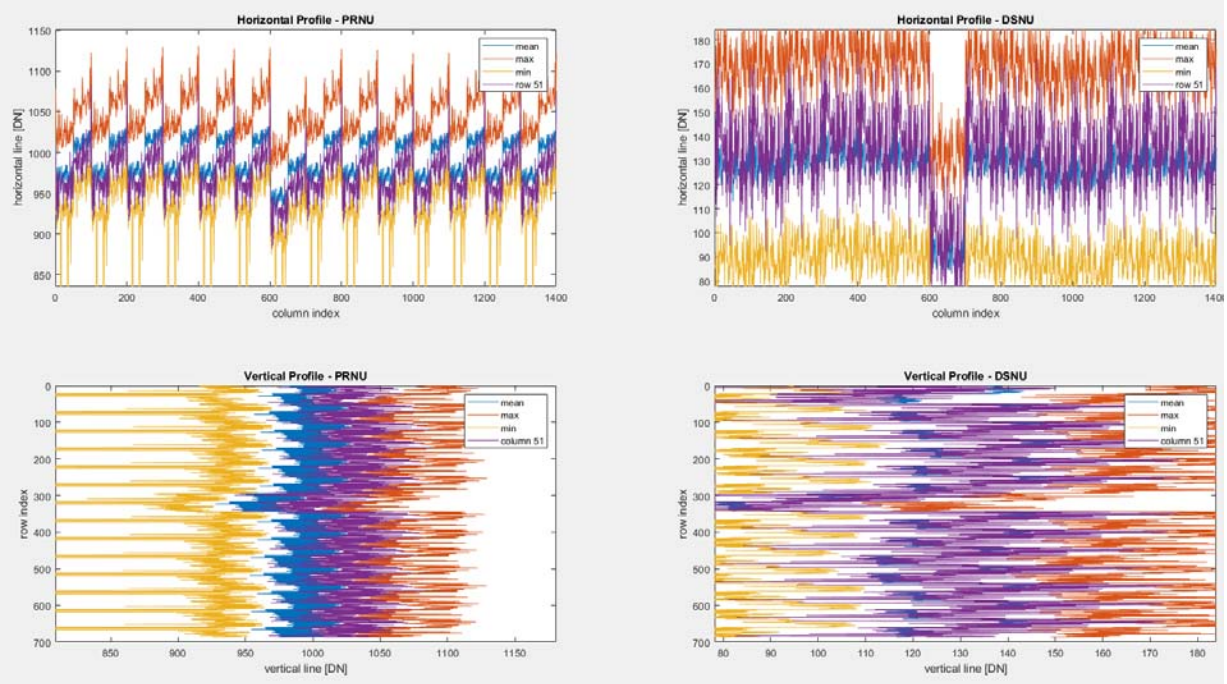

Figure 73: Horizontal and Vertical profile of nonuniformities for all frames [Case 4]

7.3 MEMORY LEAKAGES

In section 4.5 the expected leakages for the memories were calculated to be negligible. However, these calculations did not take into account the light that hits the memories and increase their leakages.

In this section, the leakages were calculated using the method described in section 6.2.6 for the following cases

- Case A: 300us exposure, 550nm light, 192DN mean image output, irradiance 1.95uW/cm^2
- Case B: 3us exposure, white light (425nm-700nm), 577DN mean image output, irradiance 1,930 uW/cm^2
- Case C: 3us exposure, white light (425nm-700nm), 1360DN mean image output, irradiance 5,350 uW/cm^2
- Case D: 3us exposure, white light (425nm-700nm), 1280DN mean image output, irradiance 5,000uW/cm^2, **Covered memories**

The testing results, leakage rate versus irradiance, can be seen in Figure 74. In Table 6, the results are summarized and some camera specific calculations are made. The readout time for the designed camera is 8ms and each frame readout is the 1/16th of this time. The readout time for the Mpixel sensor expansion is expected to be about 50ms, so the results in the last 2 rows would be 625% higher.

The last two cases (last two columns in Table 6) are at about 50% saturation with a 3us exposure time. In the first of these two cases (case C), the leakage within the frame is about 4 DN and it is expected to be more than 8 DN in saturation. On the other hand, the leakage when the memories are covered are less than 1 DN, and is expected to remain below 1 DN even for saturation. Intra-frame leakage will remain below 2.5 DN for the Mpixel expansion.

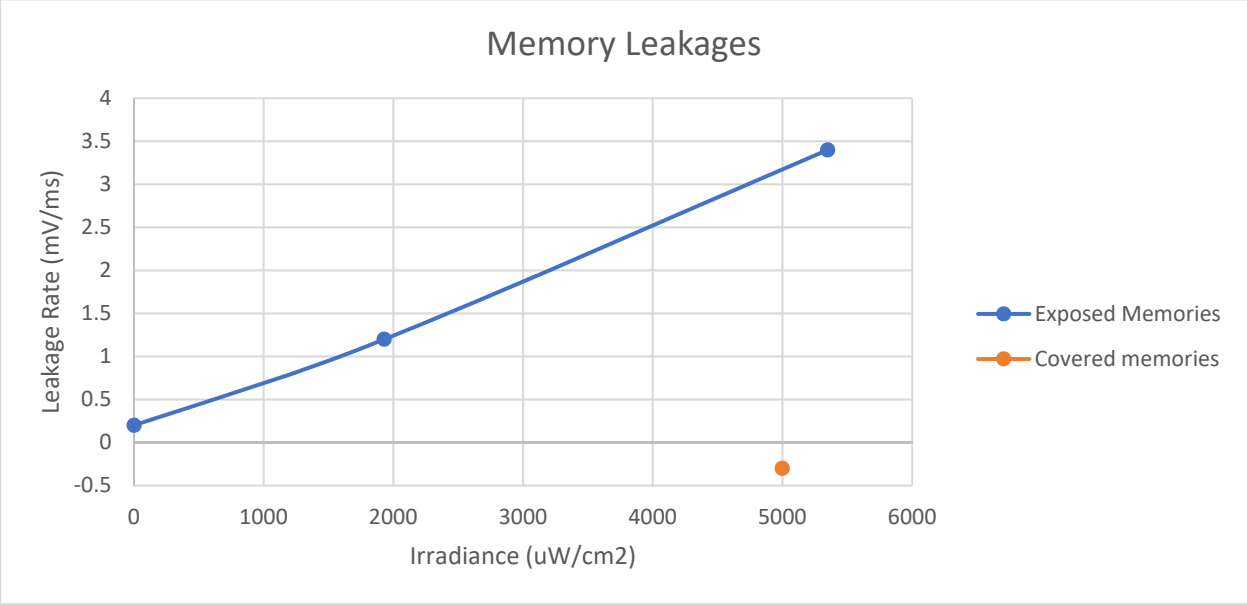

Figure 74: Memory Leakage Rate vs Irradiance

Case #	A	B	C	D
Exposed to Light	YES	YES	YES	NO
Exposure (us)	300	3	3	3
Irradiance (uW/cm^2)	1.95	1930	5350	5000
Leakage Rate (mV/ms)	0.2	1.2	3.4	-0.3
Readout Leakage (mV)	1.6	9.6	27.2	-2.4
Intra-frame Leakage (mV)	0.1	0.6	1.7	-0.15

Table 6: Memory Leakages

It should be noted that in the first 3 cases, where memories are exposed to light, the leakage rates are positive, but in the last case, where memories are covered, the leakage rate is negative. This indicates that the main leakage path for exposed memories is from the memory node to ground, L2 path in Figure 75, since the DN increases (stored value goes down). On the other hand, the main leakage path for exposed memories is from the reset node to the memory, L1 path in Figure 75, since the DN decreases (stored value goes up).

PN junction leakages also reduce the reset node voltage, but since this node is reset before each frame readout, these leakages contribute only to the leakages within the same frame readout.

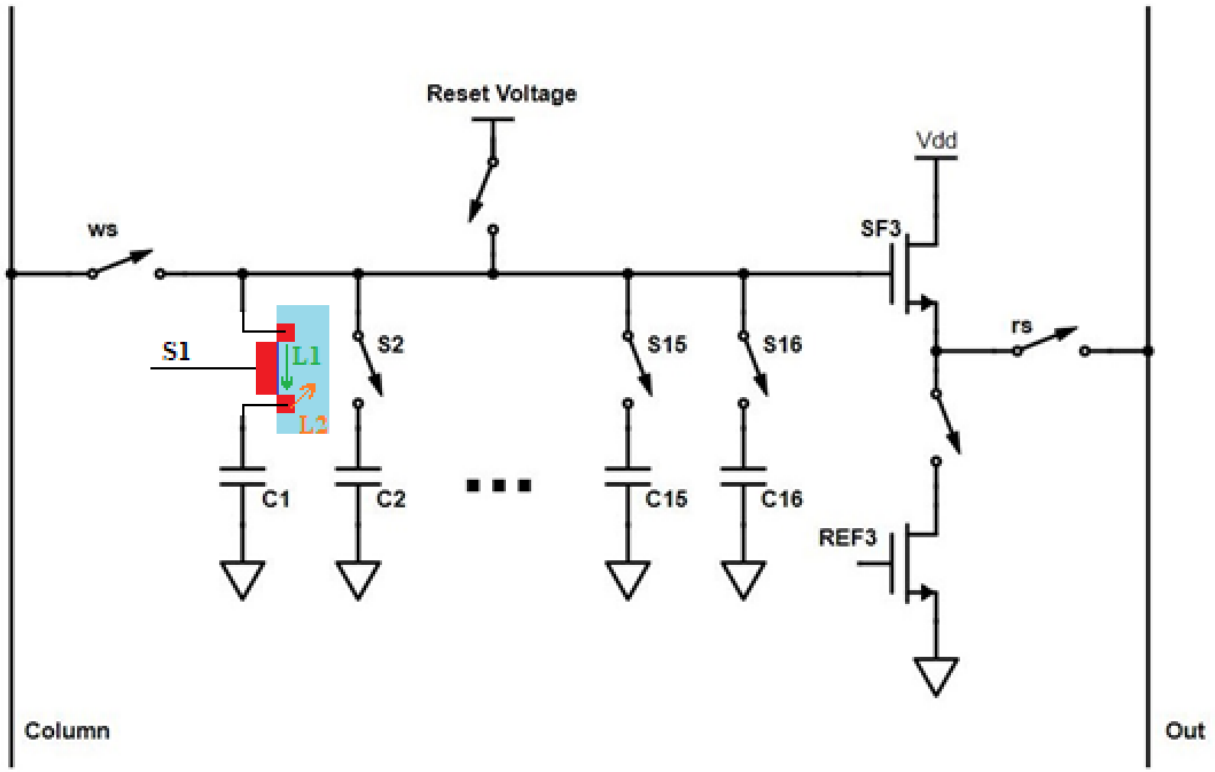

Figure 75: Main leakage mechanisms in memories

7.4 EXPOSURE AND FRAME RATE

The setup and methods described in sections 6.2.4 and 6.2.5 where used to verify the exposure and the frame rate of the image sensor.

To verify the 3us exposure of the sensor when operating at 200kfps, the LED clock was set at 1MHz, 5MHz and 10MHz, and the images captured can be seen in figures 76 to 78. As the LED clock goes lower, the LEDs turn ON for a smaller amount of time, i.e. 100ns for 10MHz clock, and the amount of light captured by the sensor from each LED is limited. LED operating at 100MHz can still be seen by the sensor, but it is easier to be identified as ON or OFF with image processing, as can be seen in Figure 79.

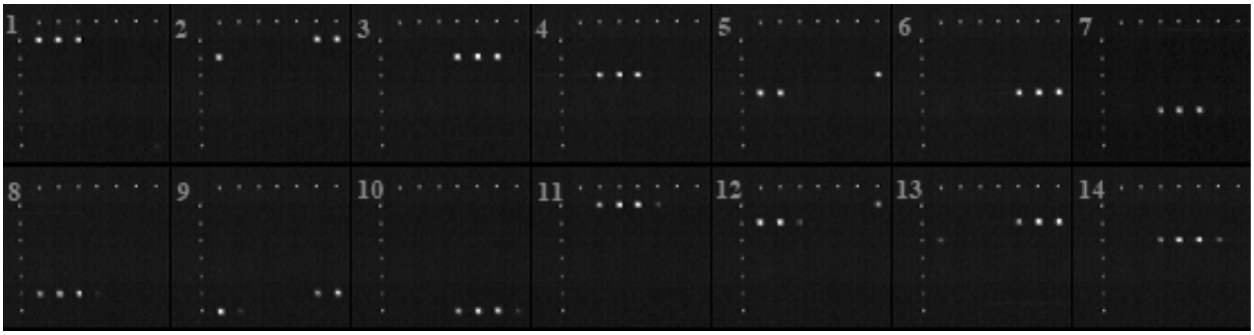

Figure 76: LED exposure test 1 - 3us exposure at 200kfps, LED frequency 1MHz

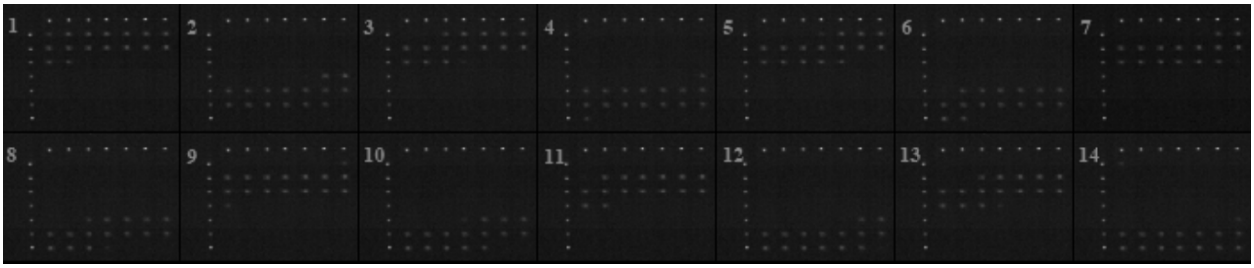

Figure 77: LED exposure test 2 - 3us exposure at 200kfps, LED frequency 5MHz

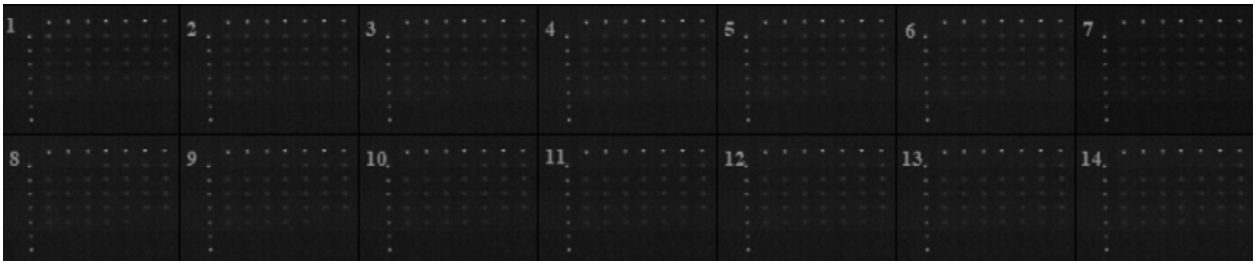

Figure 78: LED exposure test 3 - 3us exposure at 200kfps, LED frequency 10MHz

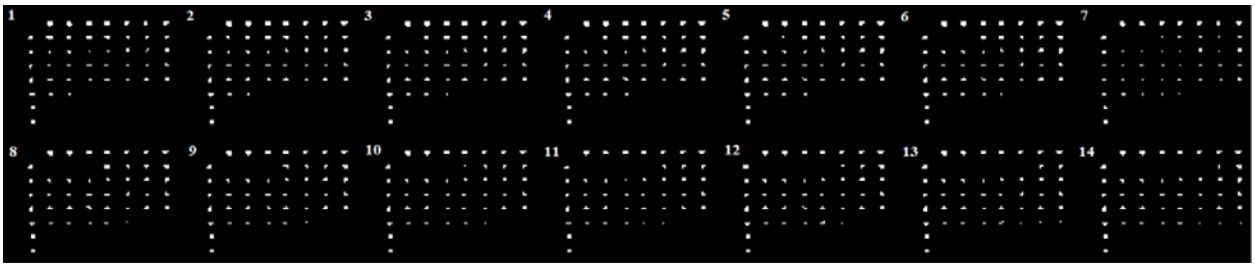

Figure 79: Image in Figure 78 enhanced in MATLAB for clarity

Using figures 78 and 79, for higher accuracy, the calculated Exposure is between 2.9us and 3us. This is because the maximum number of LEDs that are ON in any frame are 30, and by using equation 46 in section 6.2.5 the resulting exposure is between 2.9us and 3us.

In Figure 80, the exposure of the image sensor is set to 1us, and it can be seen that up to 11 LEDs are ON in the captured frames. Hence, the image sensor can operate at 1us exposure and it can be set accurately.

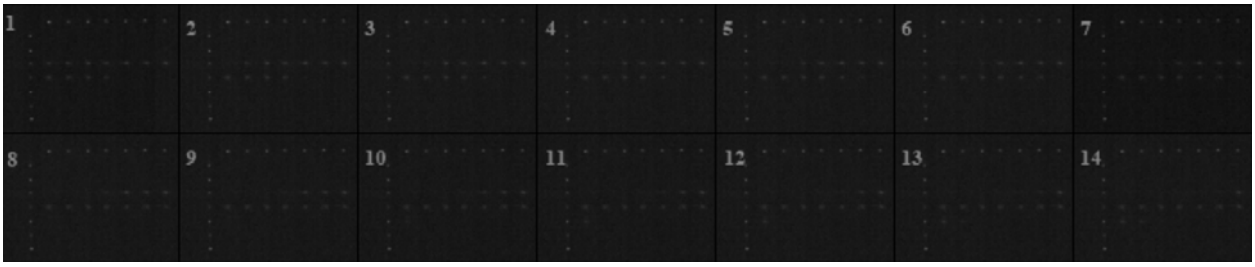

Figure 80: LED exposure test 4 - 1us exposure at 200kfps, LED frequency 10MHz

To verify that the sensor operates at 200kHz, or more precisely at 198.4kfps because the frame period is exactly 5.04us, the LED clock has to be set 25 times faster than that, i.e. $clock_{LED}$ = 25x198.4kHz = 4.96MHz, and the LED board should operate in reduced mode, i.e. only 25 out of the 49 LEDs are rotating.

The image of the LEDs operating at 4.96MHz can be seen in Figure 81. In this image it is clear that the exact same LEDs are ON in all captured frames.

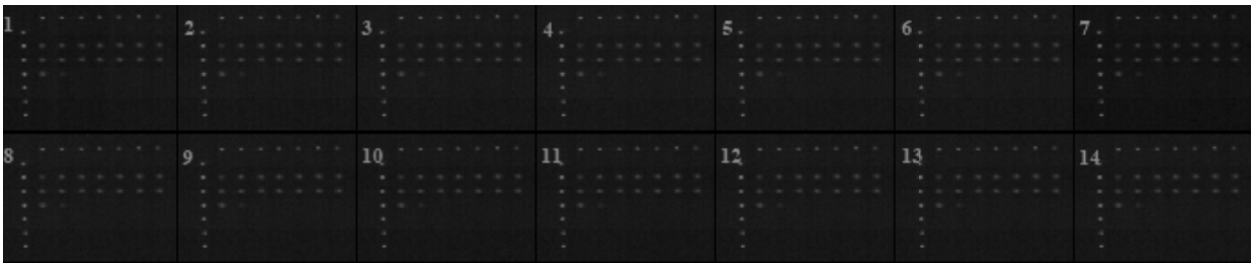

Figure 81: 25 LEDs rotating at 4.96MHz

To verify that the sensor is not operating in half the expected frame rate, i.e. 198.4/2 = 99.2 kfps, a final test has to be performed. The LED clock is set equal to the expected image sensor frame rate. The captured image when the LED clock matches the frame rate of the sensor can be seen in Figure 82. In this image, it can be clearly seen that there is a rotation of exactly one LED from frame to frame. Hence, the expected frame rate of the image sensor is verified.

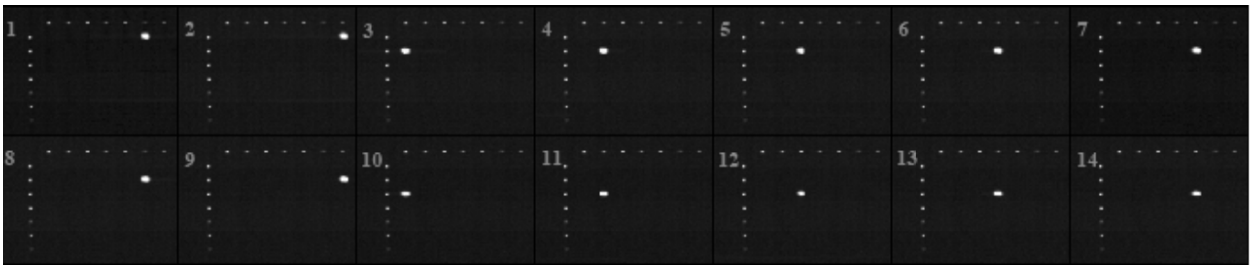

Figure 82: 25 LEDs rotating at speed equal to the frame rate (198.4kHz)

To test the response of the image sensor the operation of the LED board is set to Software Triggered, and the LED clock is set to 10MHz. The first 2 frames captured by the camera after the trigger can be seen in Figure 83.

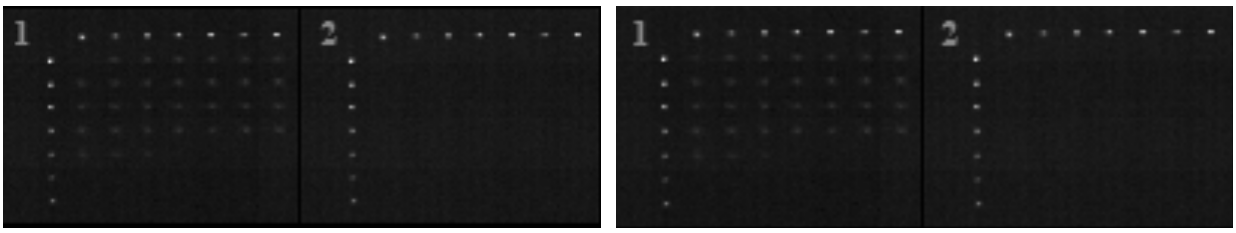

Figure 83: The response of the LED board in Software Trigger mode ($clock_{LED}$ = 10MHz)

In Figure 83 two images can be seen, side by side, because the trigger test was repeated 2 times. This is because it was noticed that the first LED sometimes it is slightly ON in the captured image. Therefore, the sensor response to software trigger is expected to be less than the clock period, which is 100ns for this test.

Summarizing, the image sensor has been verified that it can operate at 200kfps and that its exposure can be set accurately. Moreover, the response of the sensor to software trigger was measured to be below 100ns. The presented sensor can also be triggered externally, and this is a useful feature, because it can be synchronized accurately with the trigger of fast speed events that need to be captured by a highly sensitive, global shutter, high speed camera, which is exactly what was designed and tested in this work. Finally, more than one of the designed cameras can be triggered at the same time to increase the field of view, or the resolution of the captured images.

7.5 PERFORMANCE SUMMARY

The image sensor has been tested to operate at frame rates up to 200kfps and with exposure times as low as 1us. It has also been verified that the frame rate and exposure times can be set accurately. Moreover, the performance of the sensor has been evaluated at both 3.3kfps and 200kfps and seems to be independent of the frame rate.

The sensitivity and noise performance of the presented image sensor is summarized in Table 7. The quantum efficiency and the quantities in photons are emitted from the table since they depend on the wavelength of the incident light. The performance of the sensor at 3.3kfps/300us exposure has been averaged from the three tested cases.

SENSITIVITY AND NOISE PERFORMANCE			
Test Case	3.3kfps/300us	200kfps/3us	Theoretical
SYSTEM GAIN (uV/e^-)	21.97	23.29	21.57
INPUT REFERRED NOISE (e^-) (excluding quantization)	40.28	36.56	15.30
ABSOLUTE SENSITIVITY (e-)	41.23	37.5	16.39
SATURATION CAPACITY (e^-)	31,222	27,303	22,857
SNR (dB) [max]	44.94	44.36	43.59
SNR (dB)	43.95	43.62	-
DR (dB)	57.57	57.25	62.89

Table 7: Performance of the Image Sensor

It can be seen in table 7, that the expected **input referred noise** and the **absolute sensitivity threshold** (which includes quantization noise of the ADC) are not close to the measured results. Hence, it is assumed that the input referred noise of the ADC is not 0, as the simulations were indicating.

To measure the input referred noise of the ADCs, the memories are tied to the memory reset voltage, a single row and a single column switches turn ON, and the ADCs are now reading a DC voltage (reset voltage – V_{GS} of the memory blocks source follower). The histogram of the output codes of the ADCs should be normal, since the noise is approximately Gaussian, and the standard deviation of the histogram will correspond to the effective input rms noise of the ADC in terms of LSBs rms [41].

The histograms of the ADCs for a DC input voltage can be seen in Figure 84. The histograms have been plotted in MATLAB with normalization set to 'pdf' to produce an estimation of the probability density function. The probability density function for a normal distribution with mean μ, standard deviation σ, and variance σ^2 is given by the following equation [48]

$$f(x, \mu, \sigma) = \frac{1}{\sigma\sqrt{2\pi}} e^{-\frac{(x-\mu)^2}{2\sigma^2}} \tag{54}$$

This function is overlaid over the ADCs histograms, and it is verified that the outputs of the ADCs are close to normal.

The standard deviations for ADC 1 and ADC2 were calculated 1.53 LSB rms and 1.67 LSB rms respectively. Therefore, the rms noise is 0.67 mV rms for ADC1 and 0.73 mV rms for ADC2.

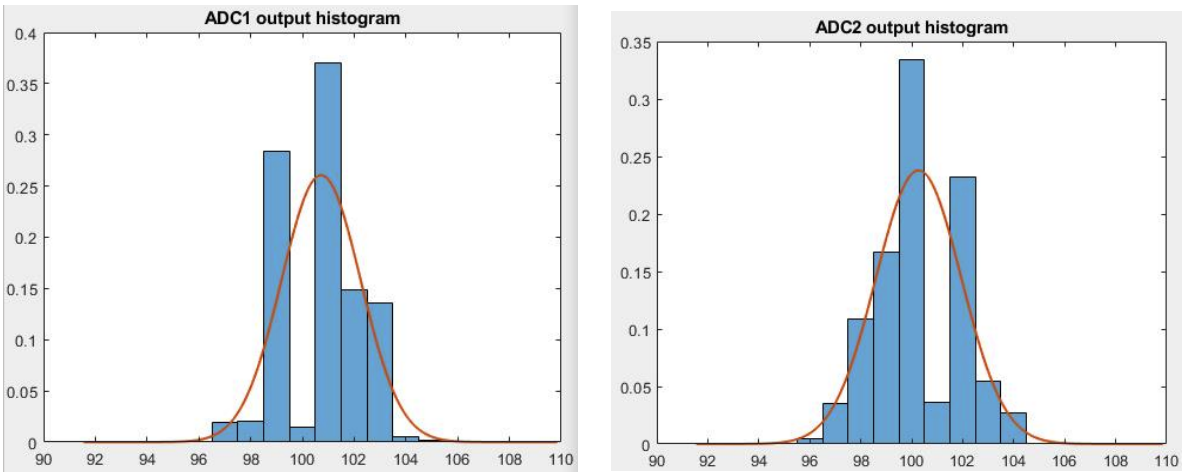

Figure 84: Histogram of ADCs for a DC input

Adding this input referred RMS noise of the ADC, averaged to $V_{n,RMS,ADC}$ = 0.7 mV rms), to the noise of the rest of the sensor at the input of the ADC (equation 17), the total rms noise at the input of the ADC is given by the following equation

$$V_{n,ADC\ INPUT} = \sqrt{(V_{n,RMS,TOTAL})^2 + {V_{n,RMS,ADC}}^2} = \sqrt{0.33^2 + 0.7^2} = 0.774\ mV\ rms \qquad (55)$$

Therefore, the input referred noise of the sensor in electrons is (see equation 13 for A_{system})

$$V_{n,RMS\ INPUT\ REFERRED}[e^-] = \frac{V_{n,ADC\ INPUT}[uV]}{A_{system}\left[\frac{uV}{e^-}\right]} = \frac{774}{21.57} = 35.88\ e^- \qquad (56)$$

And the sensitivity threshold is

$$Sensitivity\ Threshold\ [e^-] = \frac{\sqrt{{V_{n,ADC\ INPUT}}^2 + \frac{V_{LSB}^2}{12}}}{A_{system}\left[\frac{uV}{e^-}\right]} = 36.36\ e^- \qquad (57)$$

The performance of the image sensor, including the input referred ADC noise can be seen in Table 8. The theoretical performance is now very close to the measured performance.

SENSITIVITY AND NOISE PERFORMANCE			
Test Case	3.3kfps/300us	200kfps/3us	Theoretical
SYSTEM GAIN (uV/e^-)	21.97	23.29	21.57
INPUT REFERRED NOISE (e^-) (excluding quantization)	40.28	36.56	**35.88**
ABSOLUTE SENSITIVITY (e-)	41.23	37.5	**36.36**
SATURATION CAPACITY (e^-)	31,222	27,303	22,857
SNR (dB) [max]	44.94	44.36	43.59
SNR (dB)	43.95	43.62	-
DR (dB)	57.57	57.25	**55.97**

Table 8: Performance of the Image Sensor including ADC noise in the theoretical column (in **bold** the values that were adjusted)

The spatial nonuniformity and linearity performance of the image sensor is summarized in Table 9. The sensor has similar performance for all test cases, and, therefore, the average performance for all test cases is given. Dark signal and photon response nonuniformities can be reduced with software calibration but this is not part of this work.

SPATIAL NONUNIFORMITY AND LINEARITY PERFORMANCE	
$DSNU_{1288}$ (e^-)	364
$DSNU_{1288}$ (DN)	18.4
$DSNU_{ALL\ FRAMES}$ (DN)	21.0
$PRNU_{1288}$ (%)	4.1
$PRNU_{ALL\ FRAMES}$ (%)	4.1
LINEARITY ERROR [MAX / MIN] (%)	1.9 / -1.8

Table 9: Spatial Nonuniformity and Linearity Performance of the image sensor

The leakage performance of the image sensor, and more specifically the leakages from the on-chip memories are given in . The leakage rate is heavily dependent on the irradiance, but can be minimized if the memories are covered with a material that blocks the light. In this work the light was covered using a blocking surface on the lens mount but it would be much more efficiently and accurately covered if a light blocking layer was applied directly on-chip.

LEAKAGE PERFORMANCE				
EXPOSED TO LIGHT	YES	YES	YES	NO
IRRADIANCE (uW/cm^2)	1.95	1930	5350	5000
LEAKAGE RATE (mV/ms)	0.2	1.2	3.4	-0.3

Table 10: Leakage Performance of the image sensor

The complete specifications of the image sensor as part of the camera assembly presented in this work are summarized in Table 11. Some results have been averaged from the measurements for the different test setups.

COMPLETE CAMERA SPECIFICATIONS	
PROCESS TECHNOLOGY	0.18um CMOS with pinned photodiode
DIE SIZE (um)	3010 x 6554
PIXEL PITCH (um)	15.1
FILL FACTOR (%)	41.6
PIXELS	10,000
ON-CHIP MEMORIES	16
EQE (%) 450nm / 550nm / 600nm	24.5 / 30.3 / 27.4
MAXIMUM FRAME RATE (kfps) (at full resolution)	267
MINIMUM EXPOSURE (us)	1
SYSTEM GAIN (uV/e^-)	22.3
ABSOLUTE SENSITIVITY (e-)	38
SATURATION CAPACITY (e^-)	30,000
SNR (dB)	43.9
DR (dB)	58.0
READOUT TIME (ms)	8
SPECTRAL SENSITIVITY RANGE (nm)	425 - 700

Table 11: Camera Specifications

CHAPTER 8: MPIXEL SENSOR EXPANSION

The image sensor designed in this work was optimized to be expandable to a Mpixel sensor. The reasons that make the presented sensor unique and allow its expansion can be summarized as follow:

- Small pixel design while achieving the following
    - Low noise. In-pixel CDS reduces noise to 0.33mV rms at the input of the in-pixel output source follower (SF2), or 10.3 e^- input referred
    - In-pixel current sources make the output voltage independent of the physical location of the pixel
    - Fill factor greater than 40%
- The low threshold voltage and high area efficient MOSFET capacitors used for in-pixel CDS and on-chip memories allow large linear voltage swing and do not use any upper metal layers that are therefore free to be used for routing
- Source followers used in pixels and memory blocks are built in a twin well process to keep their size minimum
- In-pixel current sources are switched off when not in use
- The design (combination of SFs, current sources and switches) allows fast transfers between pixels and memories (less than 50ns for Mpixel sensor 12-bit settling) and between memories and ADCs (less than 130ns). At the same time, the maximum current drawn by the current sources during these transfers is 5.77A for the global shutter operation (1M current sources) of the PPD source followers, 1.98A for the operation of the output

pixel source followers (20,000 current sources per transfer cycle) and 1.6A for the operation of the memory source followers (20,000 per cycle).

- 50 pixels share a line, therefore only 10 lines are needed per column to transfer values between pixels and memories. Since 6 metal layers are used for routing over the non-active pixel area, the fill factor will not be hurt from shading
- The choice of 12-bits ADCs with a maximum operating frequency of 100MHz, ensures that the quantization noise will not hurt the performance of the sensor

The architecture of the proposed Mpixel expansion can be seen in Figure 85 and the resulting layout in Figure 86. The image sensor remains square for maximum optical efficiency and the frame rate remains above 200kfps. To achieve the high frame rate, pixel have again a dedicated on-chip memory block and all pixels transfer their stored values to the memories in 50 clock cycles. Since, the calculated 12-bit settling time is expected to be below 50ns, including all the parasitic resistances and capacitances, the 70ns clock that was used in the 10kpixel design can also be used here.

The readout time is expected to increase from 8ms to 50ms, since each of the 40 ADCs will have to read 500 x 50 memory blocks (was 100 x 50 memory blocks in the 10 kpixel design), which equals to 400,000 reads (16 reads from each memory block). Hence, if the readout clock is set at 8MHz, the total readout time needed is 400,000 x 1/8M = 50ms.

The expected voltage drop due to leakage at the last memory during this time, assuming that the memories are covered and the leakage rate remains 0.3mV/ms, is calculated to be 15mV,

and, therefore, the intraframe voltage drop due to leakage will be 0.94mV. This may be too high for the operation of the sensor and therefore means to reduce it will be investigated.

The following methods to reduce the voltage drop due to leakage, at least at the levels of the presented kpixel sensor when the memories are partially covered, will be investigated

- Reduce the readout time by
    - Reducing the capacitance seen by the memory block source followers. This could be achieved by using one, or a combination of the following methods
        - Using a low input capacitance driver for the ADC
        - Use a different switching scheme for the column select switches at the ADC. The parasitic capacitance of the 500 switches could be reduced to 104 if a group select switch is used for every set of 100 switches
    - Reducing the line resistance
        - Using larger switches
        - Using wider lines. Post-layout simulations should be used to find the optimal solution between line resistance and parasitic capacitance
    - Using more ADCs. Doubling the number of the ADCs will reduce the readout time by half
- Replace the access switches of the memories with other devices with less leakages. XFAB has NMOS devices with less leakages than the ones used in this work, which were not used for this work because they were relative new and also because the presented sensor was part of a Multi-Project-Wafer (MPW), so only specific devices were available. The leakages of the devices from other foundries will also be researched

- Completely block the light from memories directly on-chip. XFAB does not have a light blocking layer available, but other foundries do. If the switch to another foundry is not an option, others methods to block the light will be investigated
- Increase the capacitance of the on-chip memories. This could be achieved by using 1.8V devices instead of 3.3V devices. The capacitance of those devices is 60% higher for the same area and therefore they could reduce leakages a lot.

To reduce the number of the Mpixel sensor pins, serializers will be used to reduce the output pins from the ADCs to 32. These serializers should be able to operate at a speed 20 times higher than ADC clock. In Figure 86, two 320-to-16 serializers have been used, one at the top and one at the bottom of the sensor. Moreover, to further reduce the number of pins, the control signals will be limited by using more on-chip logic.

Multiple multi-layer metal layer power supply rings will be created around the core of the sensor for all the different supplies, analog and digital, as well as the reference voltages. Bellow these rings, MOSFET capacitors will fill the available space to provide the required decoupling capacitance needed to reduce transient switching spikes. High current input/output cells will be distributed equally around the core to ensure that the decoupling capacitors can handle the local transient spikes. Metal Insulator Metal (MIM) capacitors will be used in the ADCs area together with the MOSFET capacitors to increase the decoupling capacitance available even further. Finally, all sensor I/O pads will have ESD protection and a common ESD ground ring will run through all the pads of the chip. The power supply ring will be separate for the 1.8V ADC areas. ESD rails will be bonded out through multiple pads for all the sides of the sensor.

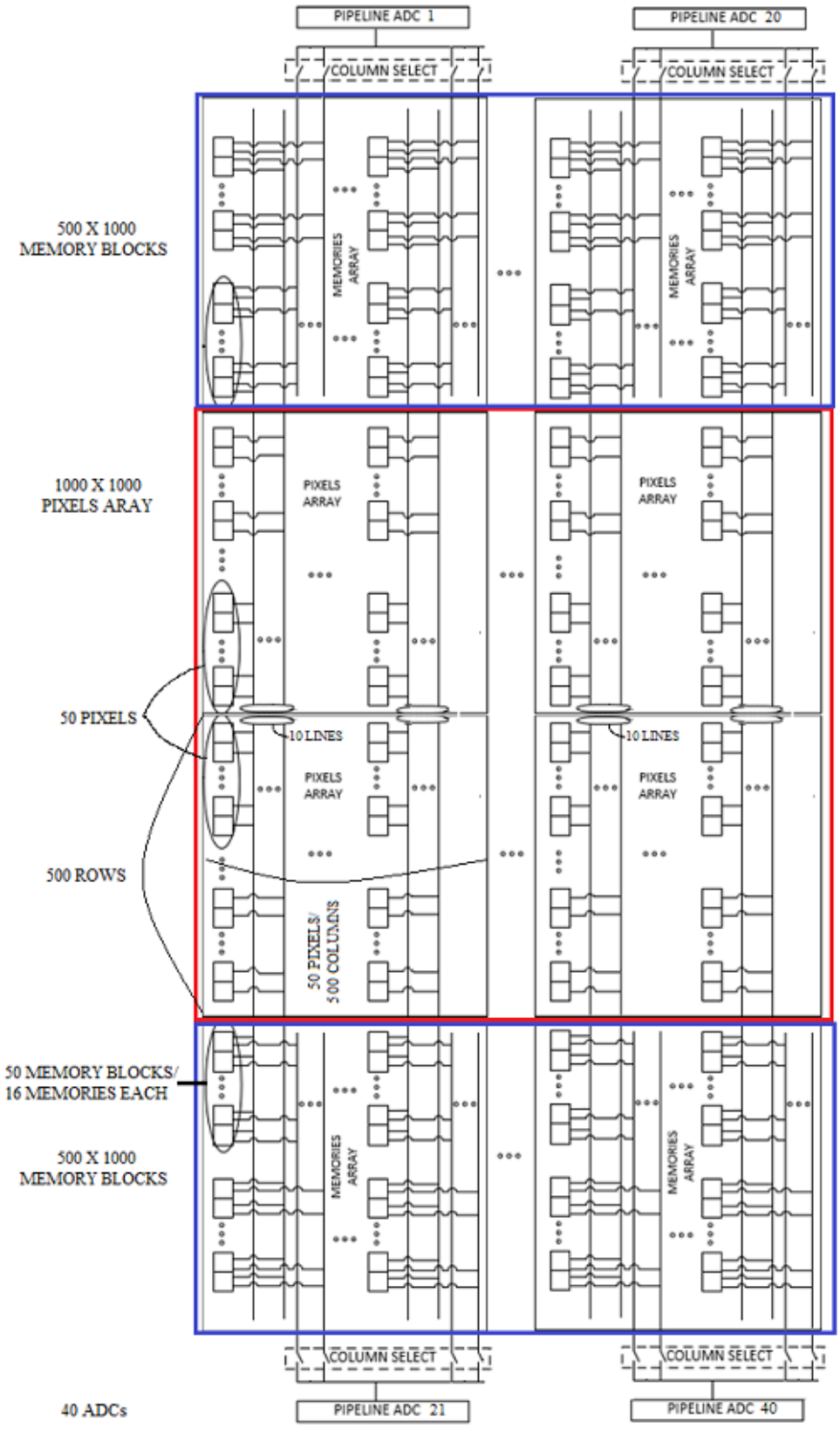

Figure 85: Proposed Mpixel Expansion Image sensor architecture

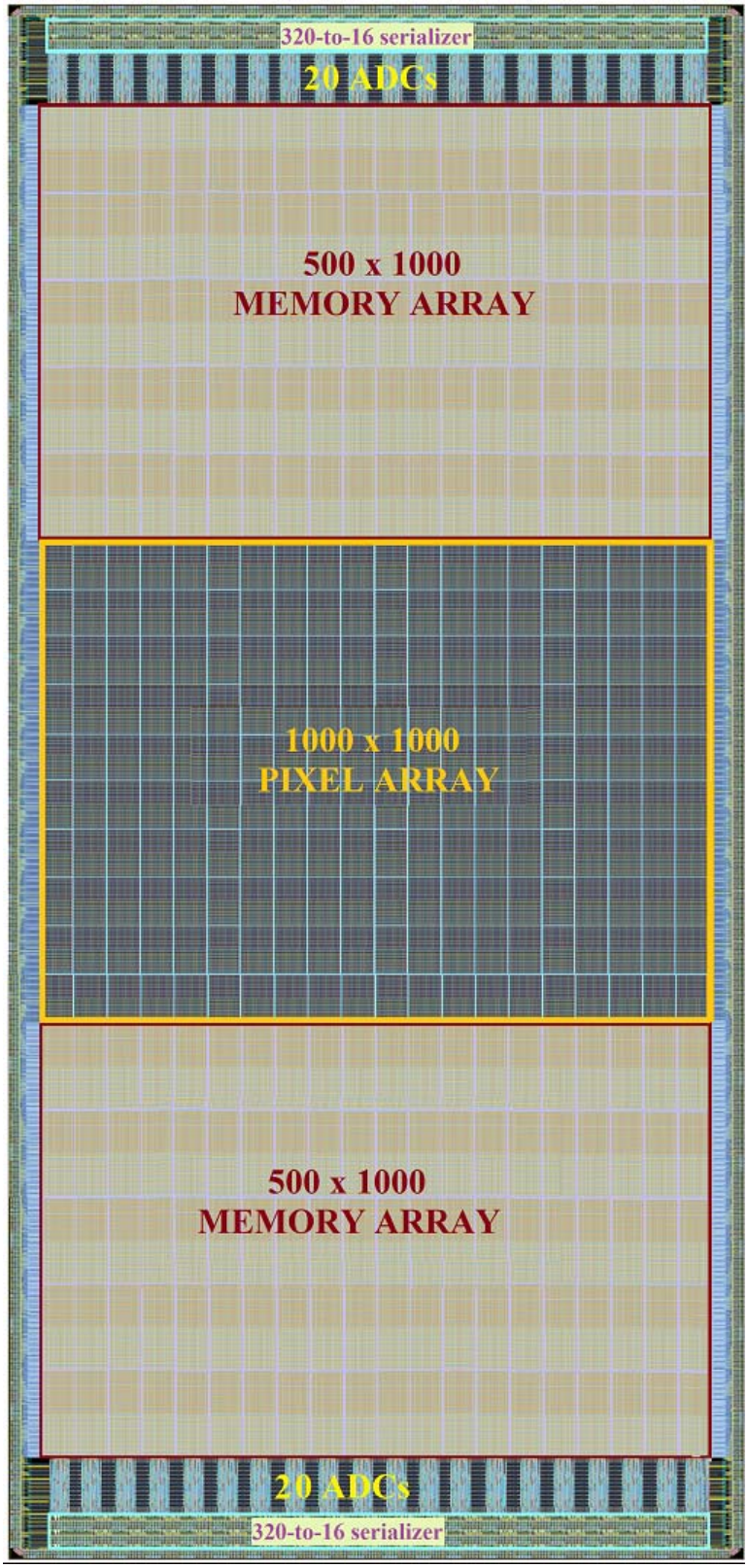

Figure 86: Proposed Mpixel Expansion draft layout

The complete specifications of the Mpixel sensor expansion are expected to be better than the 10kpixel sensor presented in this work, mainly because the input referred noise of the ADC will be minimized. The expected specifications are summarized in the following table.

MPIXEL CAMERA SPECIFICATIONS	
PROCESS TECHNOLOGY	0.18um CMOS with pinned photodiode
DIE SIZE (mm)	16 x 46
PIXEL PITCH (um)	15.1
FILL FACTOR (%)	41.6
PIXELS	1,000,000
ON-CHIP MEMORIES	16
EQE (%) 450nm / 550nm / 600nm	24.5 / 30.3 / 27.4
MAXIMUM FRAME RATE (kfps) (at full resolution)	267
MINIMUM EXPOSURE (us)	1
SYSTEM GAIN (uV/e^-)	22.3
ABSOLUTE SENSITIVITY (e-)	16
SATURATION CAPACITY (e^-)	30,000
SNR (dB)	43.9
DR (dB)	65.46
READOUT TIME (ms)	< 20ms
SPECTRAL SENSITIVITY RANGE (nm)	425 - 700

Table 12: Expected Mpixel Sensor Specifications

CHAPTER 9: CONCLUSION

In this work, a highly-sensitive, global-shutter image sensor with on-chip memory, built in a 0.18um CMOS process with pinned photodiode is presented. The unique characteristics of the pixel design and the selected architecture ensure that it can operate at frame rates greater than 200kfps even if it is expanded to a Mpixel sensor.

The main contributions of this work are the following:

- A unique **pixel design** with in-pixel CDS that limits the noise stored to the in-pixel memories to less than 0.33mV rms and allows the stored value to be read in a single readout. The capacitors used are MOSFET capacitors and therefore do not utilize any space in the upper metal layers that can be used exclusively for routing. Moreover, the in-pixel current sources for the source followers remove the dependency of the pixel output to its location in the sensor. These current sources can be switched OFF when not in use, and therefore the maximum current drawn by the sensor at any time is limited. The source followers are NMOS devices built in a twin well process for space efficiency, but at the same time they are designed to transfer the pixel values to memories fast, with 12-bit settling times less than 50ns even for a Mpixel sensor. The fill factor of the designed pixel is greater than 40%, which is important for high sensitivity. But also, the size of the pixel has been kept small, 15.1um x 15.1um, which is important for the expandability of the sensor.
- A compact **memory block** design, 26um x 15.1um, that includes 16 low threshold voltage NMOS devices operating in strong inversion. Each memory has its own low leakage access device (1T1C design), and the common line has a reset switch so that the dependency on

previous readings is removed. Each memory block has its own source follower and current source that can be turned off when not in use. The source follower is designed in a twin well process for space efficiency, and sized to be able to transfer the stored memory values fast to the ADC. The total rms noise at the input of the ADC after the memory block operation is 0.33mV.

- An **architecture** that allows frame rates higher than 200kfps even for a Mpixel sensor expansion, without reducing the sensitivity of the sensor. Memory blocks are placed outside of the pixel array so that the sensitivity of the sensor is not reduced. Fifty pixels share a line that connects them with their dedicated memory, and 6 metal layers are used to ensure that the sensor will not suffer from shading due to routing.
- Complete sensor **characterization** for sensitivity, noise, linearity and nonuniformities performance. Moreover, a unique setup and methods for verifying the frame rate and exposure of the image sensor were presented. Using the same setup, the trigger response of the sensor can be tested. A method for testing the leakages of the sensor was also presented. The setups and methods for the testing of the sensor are well documented and can be replicated.
- A proposed **Mpixel expansion** architecture. The architecture is based on the presented and tested image sensor. Methods to reduce the voltage drop due to leakage were discussed.

The proposed design in this work has achieved its goal of designing and testing a highly-sensitive, global-shutter CMOS image sensor with on-chip memory that can operate at frame rates greater than 200kfps for exposure times as low as 1us. This work can be the basis of a future work that will design and test a Mpixel image sensor operating at the same high frame

rates as the presented sensor, but it will also learn from the lessons learned in this work and achieve even better performance. The reduction of the voltage drops due to memory leakages using the methods presented in this work and the selection of an ADC with negligible input referred noise are the main tasks to be completed before moving forward.

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CURRICULUM VITAE

KONSTANTINOS MOUTAFIS

Contact Information

Email: moutaf@gmail.com

Education

University of Las Vegas, Nevada, USA

PhD, Electrical and Computer Engineering, December 2019

City University of London, UK

MS, Energy and Environmental Technology, January 2009

National Technical University of Athens, Greece

BS/MS, Electrical and Computer Engineering, May 2007