A 1-BIT ANALOG TO DIGITAL CONVERTER USING DELTA SIGMA MODULATION FOR SENSING IN CMOS IMAGERS

by

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The project presented by Bhavana Kollimarla entitled A 1-BIT ANALOG TO DIGITAL CONVERTER USING DELTA SIGMA MODULATION FOR SENSING IN CMOS IMAGERS is hereby approved:

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ABSTRACT

Image sensors consist of an array of photo detector elements each of which transforms a small portion of the image into electrons. The pixel produces an electrical signal (from the charges generated) that is indicative of the image. This analog signal is then converted into a digital signal by the analog to digital converter [18]. Variations in process, temperature and noise affect the performance of the sensing circuit causing a fixed pattern noise on the image. The main goal of this project is to design a low power low noise 1-bit analog-to-digital converter (ADC) using delta sigma modulation (DSM), which is robust with process variations and power supply noise.

Project Goal

- To design an ADC circuit that determines the intensity of light applied to the CMOS image sensor using an averaging technique.
- To design a circuit using simple signal processing that is robust with temperature, noise and other process variations.

Project Organization

This project is divided into 5 chapters.

Chapter One describes the basic principle of CMOS image sensors, pixel circuits and the image sensor array. Chapter Two gives an introduction to the DSM technique, some other sensing techniques using DSM and the need for this sensing technique. Chapter Three describes the individual building blocks of the design; the NMOS source followers,

current mirror, feedback circuit and comparator design and also covers the complete design of the circuit. Chapter Four describes the simulations results obtained for the design. It also discusses the layout of the circuit. Chapter Five contains the conclusions of the design.

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LIST OF ABBREVIATIONS

BSU ..... Boise State University.

MOS ..... Metal Oxide Semiconductor.

PMOS ..... P-channel Metal Oxide Semiconductor.

NMOS ..... N-channel Metal Oxide Semiconductor.

CMOS ..... Complementary Metal Oxide Semiconductor.

SPICE ..... Simulation Program with Integrated Circuit Emphasis.

TG ..... Transmission Gate.

PG ..... Pass Gate.

APS ..... Active Pixel Sensor.

ADC ..... Analog to Digital Converter.

DSM ..... Delta Sigma Modulation.

SCR ..... Switched Capacitor Resistance.

R ..... Resistance.

C ..... Capacitance.

t ..... Time.

λ ..... Channel length modulation.

ro ..... Output Resistance.

LIST OF SYMBOLS

VDD ..... Supply Voltage

Id,sat ..... Saturated drain current.

Vds ..... Drain to Source Voltage.

Vthn ..... Threshold Voltge.

Vsd ..... Source to Drain Voltage.

Vsg ..... Gate to Source Voltage.

Vcol ..... Column Voltage.

Iref ..... Reference Current.

Isig ..... Signal Current.

q ..... Charge.

Rsc ..... Switched Capacitor Resistance.

Phi1 ..... Clock.

A ..... Amperes.

T ..... Temperature.

V ..... Volts.

m ..... Milli.

p ..... Pico.

μ ..... Micro.

n ..... Nano.

f ..... Femto.

CHAPTER 1: BACKGROUND

CMOS Image Sensors

The science of converting an image to a signal that is indicative of the image is imaging. Imaging systems have applications in the commercial, consumer, defense, medical, industrial, and scientific fields including mobile video communications and other hand held devices. Size minimization, power consumption, and integrating multiple functions within the camera module are some of the huge challenges in such applications. Image sensors consist of an array of photo detector elements each of which transforms a small portion of the image into electrons. The pixel produces an electrical signal (from the charges generated) that is indicative of the image. This analog signal is then converted into a digital signal by the analog to digital converter. The major reason for the growing interest in CMOS imagers is that they allow a higher level of integration. They can also be operated at lower power supply voltages and consume less power when compared to charge coupled devices (CCD). The CCD devices have their own advantages in terms of performance and image quality [1] [3] [19].

CMOS Camera System

A typical CMOS camera system [3] is shown in figure 1.1. Light from the image to be recorded is captured on to image sensing elements using optics (a lens is used to focus the image). The light from the optical system is converted into an electrical signal by the image sensor (by the pixel). The electrical signal is then processed by the signal-processing module (like an ADC) into a format that is required by the display unit [3].

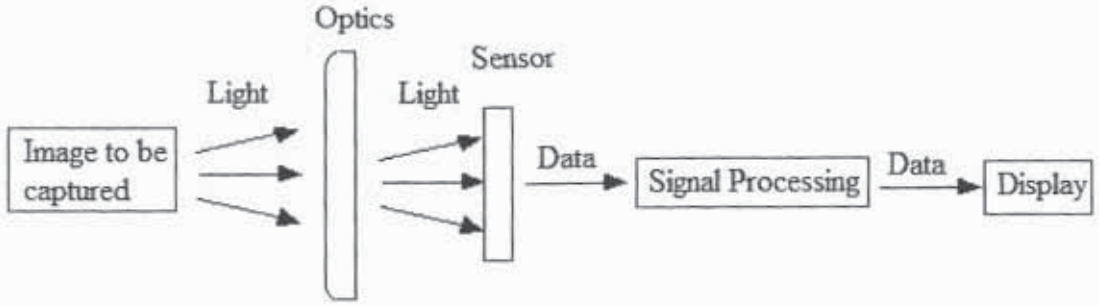

Figure 1.1. Typical CMOS camera system

The image sensor and the analog to digital converter are discussed here.

A CMOS active-pixel image sensor contains a photo-detector element (a photodiode or a photo gate) and an active transistor (an amplifier) for readout of the pixel signal. A pixel converts the signal from the photodiode into a form that can be read out by the addressing circuit. When light is incident on a photodiode it is converted into charge and a photocurrent is produced. The various readout methods for the CMOS active pixel sensors (APS) are the a) current mode readout (where the photocurrent is read out directly - difficult approach due to the small photocurrents), b) charge integration and voltage readout (the photocurrent is converted in to a voltage by accumulating it on to a capacitor-most common approach), c) charge integration and sensing readout (the photocurrent is integrated on a capacitor and the charge is read out directly-difficult approach), and the d) resistive current to voltage conversion method (the photocurrent is converted in to a voltage by a large resistive load – resistor matching between the pixels can become difficult) [3]. In this project a delta sigma A/D converter for use with a voltage mode pixel has been designed, fabricated and tested.

CMOS Pixel Circuits

CMOS pixels can be divided into two groups a) passive pixel b) active pixel (photodiode type & photo gate type). The passive pixel or 1-transistor (1T) contains no amplification.

It is the simplest of all and has a single transistor and a photodiode but has noise and sensitivity problems. The active pixel has better noise performance compared to the passive pixel. The active pixel sensors (APS) can be implemented as 3T pixel, 3T pixel with a transfer gate, 4T pixel and logarithmic pixel circuits [2].

The general architecture of an APS (charge integration and voltage readout method) is shown in figure 1.2. P is the photodiode that converts light into charges. A is a buffer amplifier (usually implemented using an NMOS source follower) that isolates the photodiode from the bit line. It converts the charge (electrons generated by the photodiode) in to a voltage that is readout on to the imager's column line. C comprises of the photodiode capacitance, parasitic capacitances of gate of the amplifier and source capacitance of a reset switch present in this topology. The charge to voltage conversion takes place at this node capacitance.

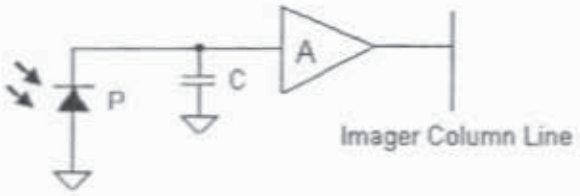

Figure 1.2. Architecture of an APS

3T Pixel

A NMOS 3T active pixel [4] is shown in figure 1.3. When RST goes high M1 turns on. The voltage across the diode is set to VDD and the photodiode is reverse biased. When the row select RS goes high the voltage (VDD-Vgs of MS) is readout on to the column line by the source follower MS. This is the dark or the reference voltage of the pixel since the accumulated charges on the photodiode are drained out. After a suitable integration time (photon accumulation time) controlled by the RST transistor M1 photo generated charges accumulate on to the photodiode and discharge it from the dark or the reference voltage at a rate approximately proportional to the incident light. This voltage is the desired signal that corresponds to the intensity of light applied to the photodiode. The RS and RST signals should be driven to voltages greater than VDD to fully turn on the NMOS devices.

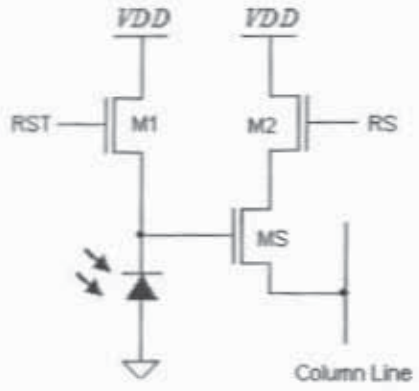

Figure 1.3. Schematic of a 3T APS

When the RS signal goes high this voltage is sampled on to the column line. The performance of the source follower is critical to obtain a good gain and bandwidth of the pixel's output. Increasing the width of the source follower (SF) increases the gain but decreases the bandwidth of the pixel. Increasing the width of the RS switch reduces its

'on' resistance and helps in increasing the gain and frequency bandwidth of the pixel's output. Increasing the width of the SF decreases the gate to source voltage and holds it more close to the threshold voltage thus giving a better conversion. Threshold voltage variation of the source follower causes non-linearity in the pixel. Fixed pattern noise (a noise pattern observed on the captured images), arises due to variations in threshold voltage of source follower, dark current and 1/f noise. This is a common problem with 3T APS. The correlated double sampling (CDS) technique is employed to remove fixed pattern noise in the pixels. In CDS technique the pixel's reset value is subtracted from the signal value to remove the offset, non-uniformities and the threshold voltage of the source follower in the pixel [1][3] [4] [5] [6].

4T Pixel

A 4T pixel is shown in figure 1.4. By turning on the M1 (reset transistor) and MG (transfer gate) the photodiode is reset and the reference voltage is readout to the column when RS goes high. The transfer gate is then shut off and the integrated charge is stored on the photodiode. After the charge is stored the transfer gate is turned on and the desired signal that corresponds to the intensity of light is readout on to the column line. The photo-generated electrons are converted into a voltage by the source follower. The number of volts per electron is the conversion gain. The conversion gain is increased and noise is reduced here since the capacitance at the sense node (gate of MS) is reduced. The reduction in the capacitance is because of the isolation of the photodiode capacitance by the transfer gate [1][3] [4] [5] [6].

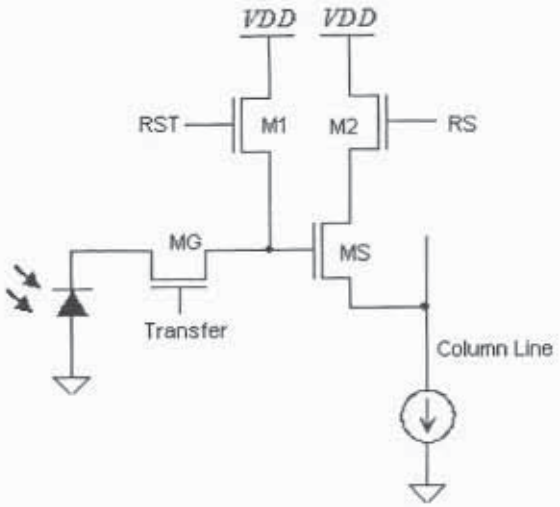

Figure 1.4. Schematic of a 4T APS

Pinned Photodiode

Figure 1.5 shows the schematic of the APS with a pinned photodiode implementation. The photodiode is implemented using a pinned diode in order to reduce the dark current (a temperature dependant current that is still present when the photodiode is reverse biased), noise and to have a high quantum efficiency thus achieving a high performance pixel. It consists of a pinned diode (p^+-n-p) where the photons are collected away from the surface thus reducing noise due to dark current. The charge generated by the photons is transferred on to the floating diffusion for readout. The capacitance on the floating diffusion node (gate of MS) is critical since having too high a capacitance reduces the conversion gain and too low of a capacitance could saturate the signal when the full charge is transferred [6][7].

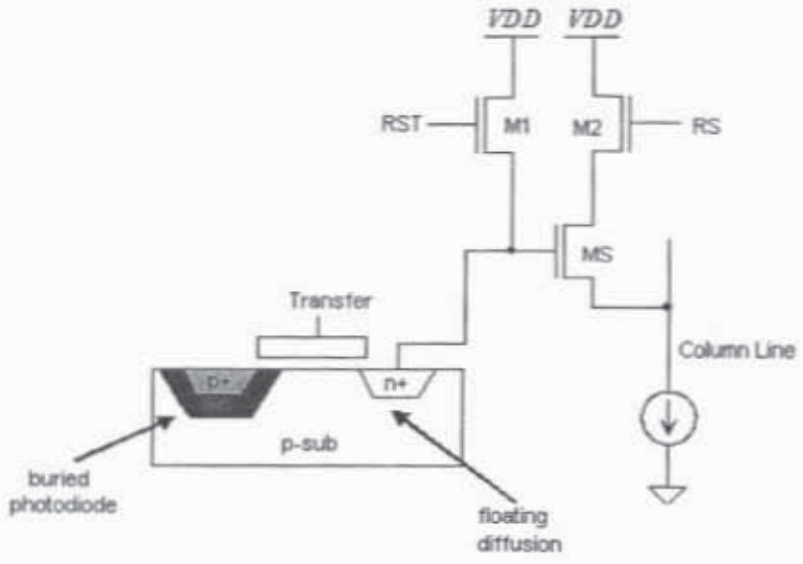

Figure 1.5. APS with a pinned photodiode

ADC Implementation

CMOS imagers allow the integration of analog to digital converters on a single die. The various approaches for implementing ADC's with active pixel sensors are: [3]

1. Column level analog to digital converter: The APS array consists of an array of ADC's at the bottom. One or more columns of the pixel array share a single ADC in this approach. Generally all the ADC's will be operating in parallel thus allowing a low or a medium speed ADC to be used. Mismatch of the converters on the columns and fitting the ADC in the pixel pitch are the common problems with this method [3].
2. Chip-level analog to digital converter: Here a single ADC is used for the entire APS array. This method minimizes layout area but requires a high speed pipelined ADC if the APS array size is big [3].
3. Pixel-level analog to digital converter: Each pixel is designed with its own converter. This method has various advantages over the column level and chip level ADC's. It consumes low power, works with low voltage, has the ability to observe the pixels outputs continuously and has a high SNR. Also a very low speed ADC can be used with these architectures [3].

Column Parallel Architecture for A/D Conversion

Column Parallel Architecture for A/D Conversion [11] for CMOS image sensors is shown in figure 1.6. At the intersection of every row and a column line we have a pixel block shown in figure 1.4. This is a semi parallel architecture where all the pixels connected to one entire column shares a single ADC. A single row is activated at a time and the columns are readout in parallel.

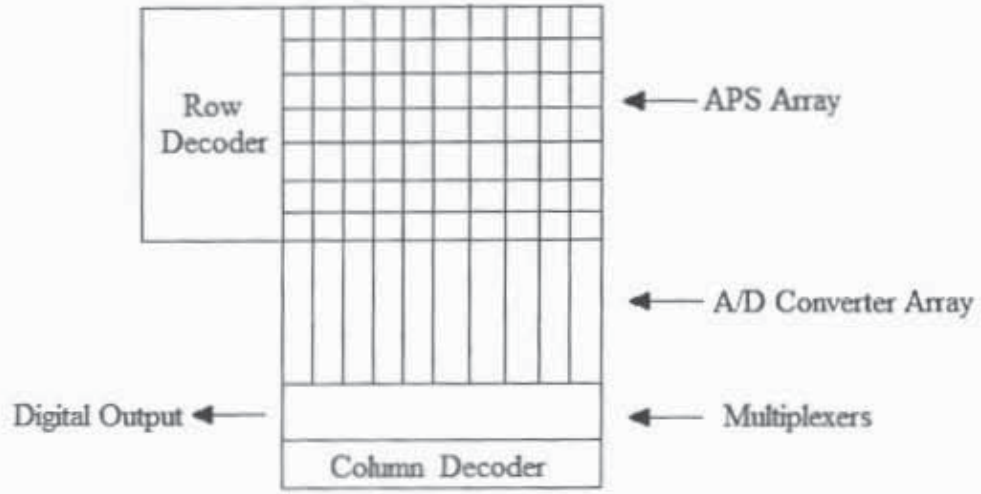

Figure 1.6. Column Parallel Architecture for A/D Conversion in a CMOS imager

CHAPTER 2: INTRODUCTION

Δ-Σ Modulators

There are several approaches for designing analog to digital converters (ADC) like sigma-delta, successive approximation, and single slope/dual slope techniques. ADC architectures like successive approximation converters and dual-slope converters provide high resolution at the cost of using high precision sample and hold circuits, high-speed and high accuracy integrators. Laser trimming of components is required for these Nyquist rate converters for accuracy without which these architectures cannot be implemented in the current IC technology [10]. Over sampling sigma delta ADC's use simple data conversion circuitry in place of precise and complex analog components and achieve high resolution. Sigma delta ADC's are preferred over the traditional architectures because of their averaging nature, which makes it more robust to CMOS process variations, and they require less component accuracy [11].

The block diagram of a typical first order one-bit delta-sigma [Δ-Σ] modulator [12] is shown in figure 2.1. It consists of an integrator and a quantizer. The integrator takes the difference between the input and the output signals. The quantizer is implemented with a 1-bit comparator, which converts an analog signal to a high, or a low signal value. The input signal is first sampled, quantized and then digitized [2].

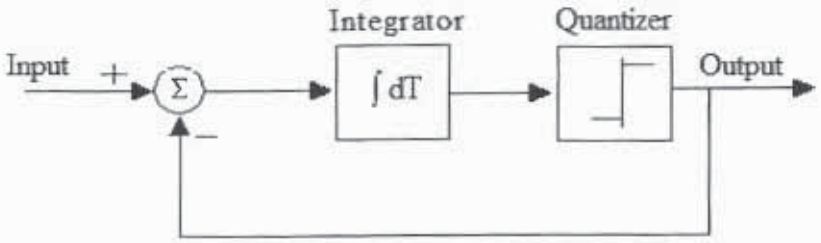

Figure 2.1. First Order Δ-Σ modulator

Δ-Σ Modulators are based on over sampling and noise shaping techniques. Over sampling reduces the quantization noise power by spreading it over a bandwidth larger than the signal bandwidth. Noise shaping attenuates noise in the signal band by pushing it out of the bandwidth of the input signal. A low pass filter like a counter shown in figure 2.2 can be used to attenuate the out of band quantization noise. A high resolution A/D conversion can thus be achieved. But there is a penalty in speed as it takes more time to sample the input [10]. However achieving higher over sampling ratios is easier than producing precise analog components for reducing component mismatch [11]. Further aliasing is not a problem in delta sigma ADC's [2].

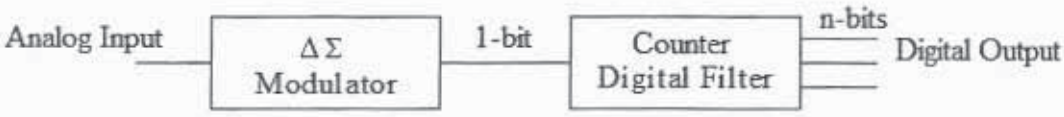

Figure 2.2. Block Diagram of over sampled A/D converters

Various architectures for designing ADC's using sigma delta have been proposed [11] [12] [13] [14]. A Δ-Σ ADC with a semi-parallel architecture for an image sensor [11] has been developed where the modulator is implemented with a switched capacitor integrator. But the non-idealities of the circuit components like finite op-amp gain;

limited op-amp bandwidth affected the ADC's performance. A topology developed by Fowler -[12] is based on synchronous first order Δ-Σ modulator at pixel level that requires biasing circuitry and number of analog components where precision and matching of transistors could become an issue. The main shortcomings with the circuit is the fixed pattern noise on the images which is caused by variations in process parameters of the MOSFET's from pixel to pixel. A MCBS (multichannel bit-serial) ADC, which is Nyquist rate pixel level analog to digital converter, has been developed by Yang et al. [13]. A Nyquist rate converter has the advantage of reduced output date rate when compared to over sampled converters. But the comparator gain-bandwidth played an important role in determining the ADC's performance in this design. A free running oscillator used as a Δ-Σ modulator has been developed [14] for a low power CMOS imager. The oscillator is designed with diff-amp and number of common source amplifiers that have threshold voltage variations. This topology needs external control signals to generate the bias voltages. A voltage to frequency conversion for each pixel has been implemented where each column has an ADC and one row is operated at a time. This method is advantageous since the analog signals need not be transmitted [12]. The ADC design discussed here has a unique voltage to current conversion technique for each pixel in order to not disturb the voltages of the pixel and to keep the pixel isolated from the sensing circuitry. Also taking the difference in the reference and signal currents makes the circuit robust with various process and threshold voltage variations. The circuit is symmetrical hence any ground noise or VDD noise common to the reference and signal paths affects the outputs in a similar fashion and the error will be averaged out with time. The ratio of the capacitors cancels out and thus any process variations are also cancelled

out. The capacitors on the input of the comparator average out the noise. The comparator gain is not important here, as the error will be averaged out with time. The sense can be run indefinitely in this sensing technique and increasing the sense time increases the resolution. Errors due to thermal noise will be averaged out by sensing for a longer time thus increasing the signal to noise ratio.

A low power, low noise, 1-bit analog-to-digital converter (ADC) using delta sigma modulation (DSM) techniques to be used with a voltage mode CMOS imaging pixel array has been designed. NMOS source followers are used for linear voltage to current conversion. A switched capacitor resistor topology is used instead of a resistor to minimize layout area and to overcome design challenges. The comparator circuit used to compare the reference and the intensity signals has a good sensitivity of around 8mV. The power consumed for each column is around 600uW.The design has good linearity characteristics, low power consumption, low noise, no buffers and a simple implementation. The circuit is implemented in a 0.5um AMI C5 process technology. The proposed DSM sensing circuit is applied to CMOS imaging sensors to measure light intensity applied to a pixel.

ADC's accept an analog input voltages or currents and converts these inputs into a digital value. The reference and the signal to be measured are the inputs to the ADC and the output of the ADC can be given to a counter which counts the number of high's of the DSM circuit and gives a digital word representing the input. A sigma delta ADC has a high resolution and it takes a number of input samples to converge on a result. Averaging for a longer time gives an output that is closer to the input and also reduces the error.

This sensing design is robust with variations in process shifts, threshold voltages, temperature, capacitances, comparator offsets and has a good sensing accuracy. The resolution increases with increasing sense times and sampling for a longer period.

This circuit gives a good conversion for voltage ranges from 3.2V (Black) to 0.7V (bright). The performance of the Δ-Σ ADC shown in figure 2.3. The reference voltage is held at 3.2 V and the signal voltage corresponding to the desired intensity voltage from the pixel is varied from 0.7V to 3.35V. We see that the hand calculations match the simulation results giving a good sense for these voltage ranges.

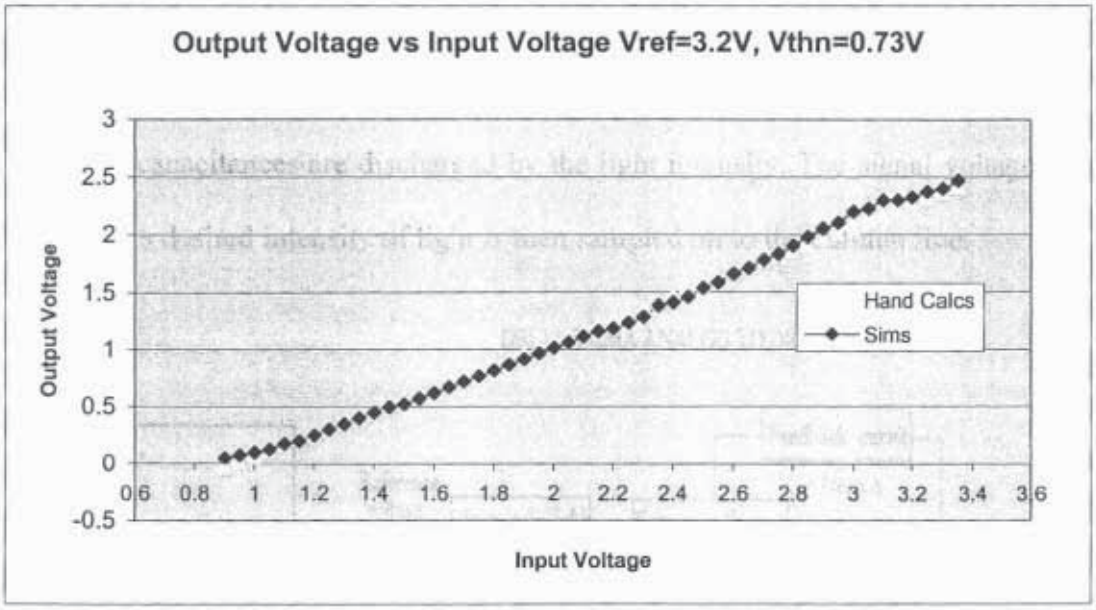

Figure 2.3. Simulation results of the Δ-Σ ADC

In NMOS source followers the linearity is affected because the body effect cannot be eliminated. A comparator is used to determine which of the two voltages the reference or the desired intensity signal paths is greater. The output of the DSM can be given to a counter, which can be thought of as a digital filter.

CHAPTER 3: SENSE AMPLIFIER DESIGN

SYSTEM BLOCK DIAGRAM

The block diagram of the DSM sensing circuit is shown in figure 3.1. A CMOS imager consists of a pixel array in which each individual pixel consists of a photo detector element to convert a certain intensity of light in to voltage. The photodiode is first reset to a voltage (VDD) this is the reference voltage that is readout on to the imager column. The photo diode is then isolated for a certain amount of exposure time during which the junction capacitances are discharged by the light intensity. The signal voltage corresponding to this desired intensity of light is then sampled on to the column line.

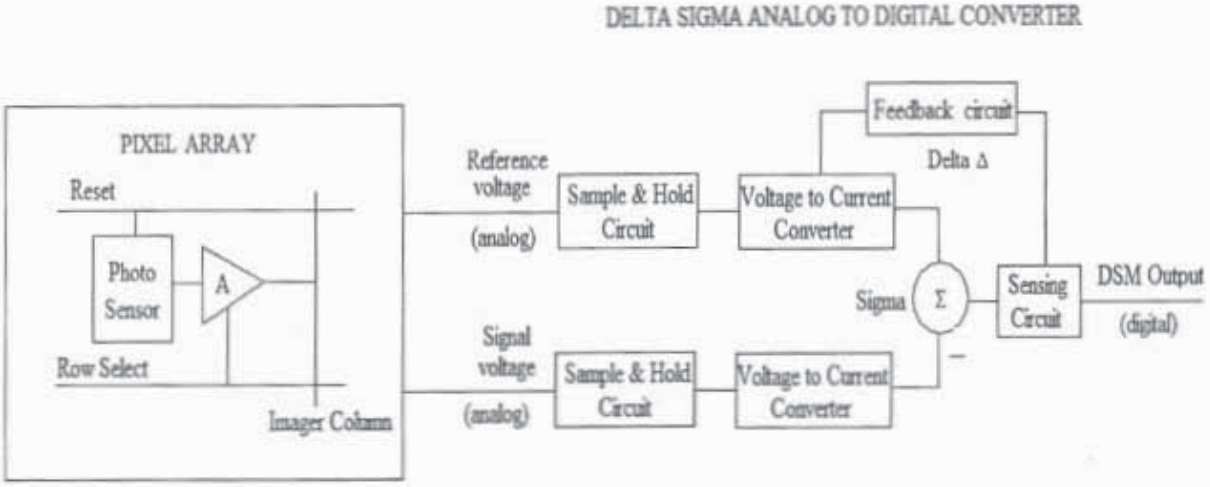

Figure 3.1. Sensing Circuit Block Diagram

A common row line is connected to all the access transistors in a row in order to read and reset all the pixels in the same row simultaneously. After an exposure time the

stored charges on the photodiodes in the same row are read out simultaneously on to the bit line. Each bit line is then connected to an ADC to sense the bit line voltage [8]. Here we are designing a novel sensing circuit to determine the desired signal voltage on the column line of the imager corresponding to the intensity of light. The DSM output is a 1-bit digital representation of the desired signal voltage indicative of the intensity of light. Figure 3.1 shows the block diagram of the delta sigma analog to digital converter that senses the column voltage from the pixel. This column voltage indicates the amount of light incident on the photodiode when an image is captured by the camera.

The reference and the signal voltages from the column line are first sampled with the sample and hold circuit shown in the block diagram. These voltages are then given to the voltage to current converter block.

An NMOS common drain amplifier performs the voltage to current conversion. The reference and the signal voltages are converted into currents to isolate the sensing circuit from the pixel voltages. The reference and signal currents are then applied to the sigma block.

The difference in the reference and the desired signal currents is summed in the sigma capacitor. The difference in currents is to be taken in order to subtract out the variations in threshold voltage of the source follower from pixel to pixel [2]. The voltage from the summing capacitor is then applied to the sensing circuit block.

The sensing circuit is a clocked comparator with the SR latch that compares the voltages from sigma capacitor and the reference signal path. The comparator is implemented with PMOS input transistors and the transistors with higher gate voltage sources lower current. The output of the latch is used to enable the feedback circuit.

The feedback circuit is implemented with a switched capacitor circuit, which removes a precise amount of charge. The feedback circuit tries to adjust the current in the reference and desired signal paths until they are equal. The desired signal corresponding to the intensity of the signal from the pixel can be determined by comparing the desired signal current to the reference signal current and by averaging the number of times the switch in the feedback path has been enabled to equalize the currents.

Voltage to Current Conversion

The reference and desired voltages from the column line in the pixel are converted in to currents by the NMOS source follower (SF). Figure 3.2 shows the input circuit [2] used for the design, which performs the voltage to current conversion. M1 is an NMOS source follower, which performs the voltage to current conversion.

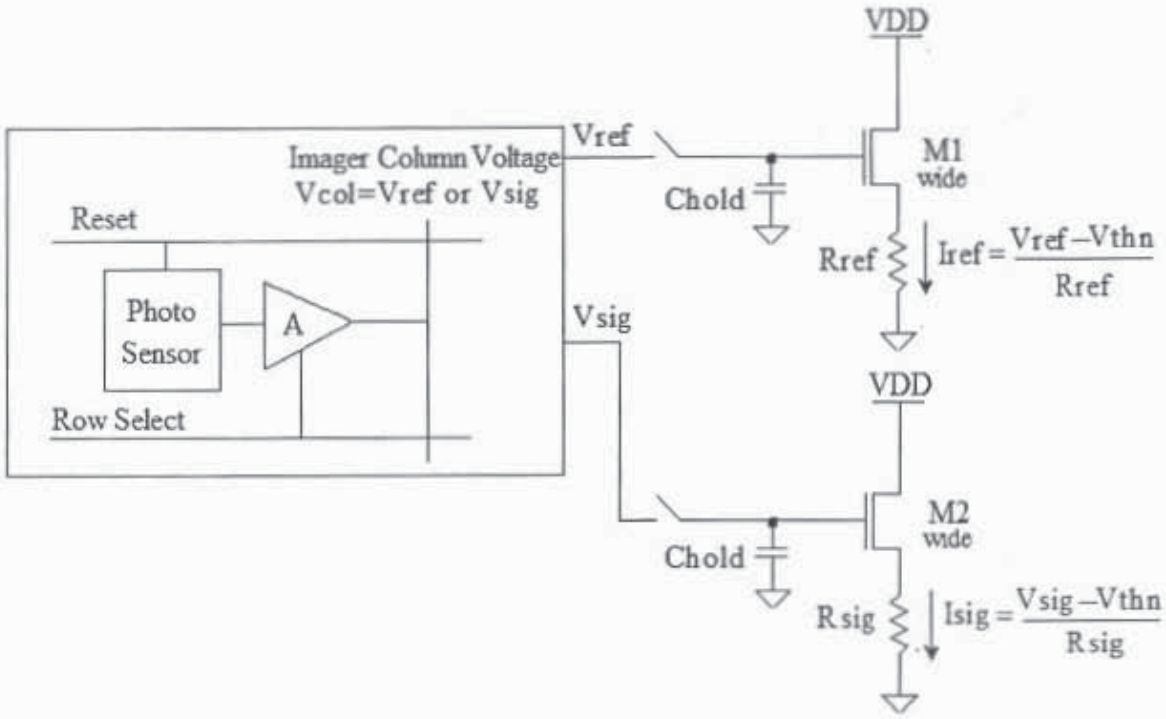

Figure 3.2. Voltage to Current Conversion

In this design resistor is replaced with a switched capacitor resistor [SC Resistor], which has been discussed in the following sections.

Figure 3.3 shows the input circuit [2] with the resistor implemented using a switched capacitor resistor; a PMOS device with gate drain and body shorted to VDD is used for the capacitor.

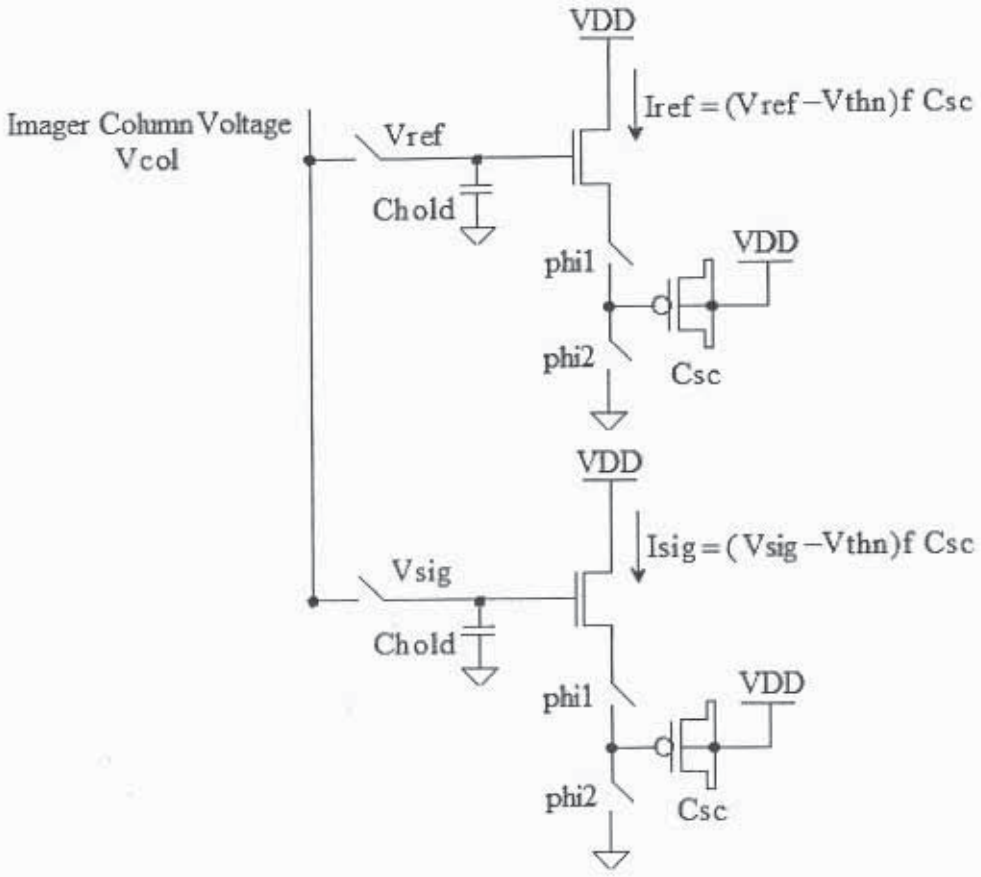

Figure 3.3. Voltage to current converter with SCR

A reference voltage has to be stored before the sense after which the signal from the pixel is sampled on to the inputs of the ADC and are then converted in to currents. MOSFET M1 is added to convert the voltages coming from the pixel in to currents so that the column voltages are not changed with the sensing circuit. The difference in the reference and intensity voltages has to be taken to minimize pixel-to-pixel variations [2].

Linearity of NMOS Source Followers

The performance of the NMOS source follower (SF) is critical for a linear conversion. Non-linearites due to variations in threshold voltage and other process parameters could lead to blurring of images and non-uniform color pictures. Figure 3.4 shows the schematic for ac analysis of the SF with body effect. The output voltage (figures 3.5, 3.6) and the gain (figures 3.7, 3.8) of the SF shown in the figures have been simulated for different widths of 20 (vout), 50 (vout11), and 100(vout22). It can be seen that increasing the width of the source follower increases the gain thus giving a good conversion but the bandwidth of the SF decreases affecting the dynamic range. Also body effect limits linearity in NMOS switches. The linearity is limited by body effect in the NMOS switches since in an n-well process body-effect cannot be eliminated, as the NMOS device body is the substrate. Figures show the ac analysis of the SF without body effect for different widths W = 20 (vout), 50(vout11), 100(vout22). Without body effect it can be seen that we get a higher gain and better conversion and again the bandwidth is affected. Increasing the width increases the parasitic capacitance (Coxn) of the MOSFET, which increases the time constant and hence decreases the bandwidth. [4] shows the analysis of the effect of source follower on the pixel's output.

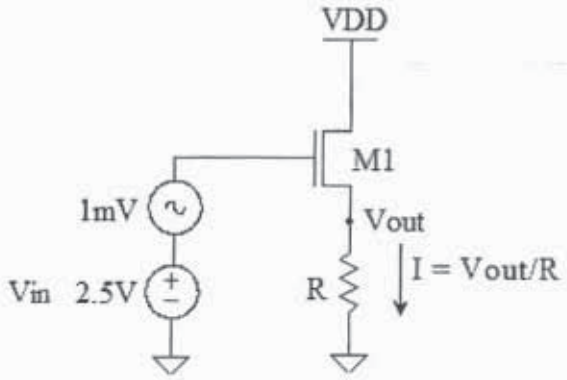

Figure 3.4. AC analysis of the SF

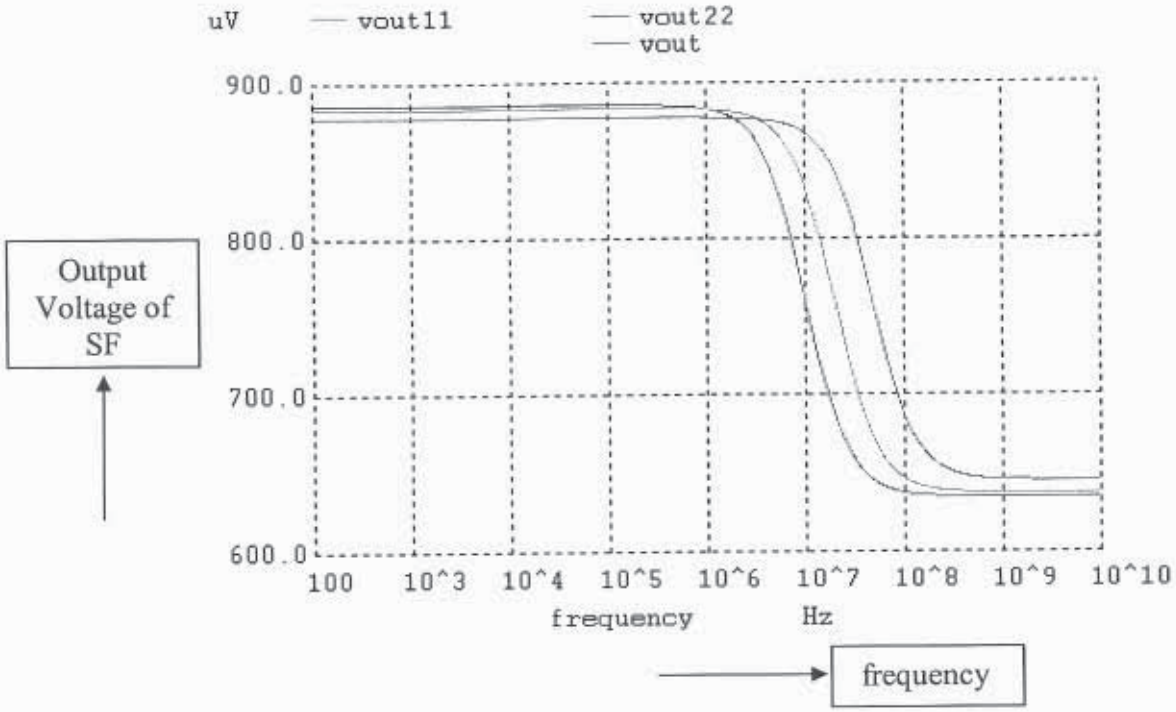

Figure 3.5. Output Voltage of the NMOS SF with body effect for W = 20, 50, 100

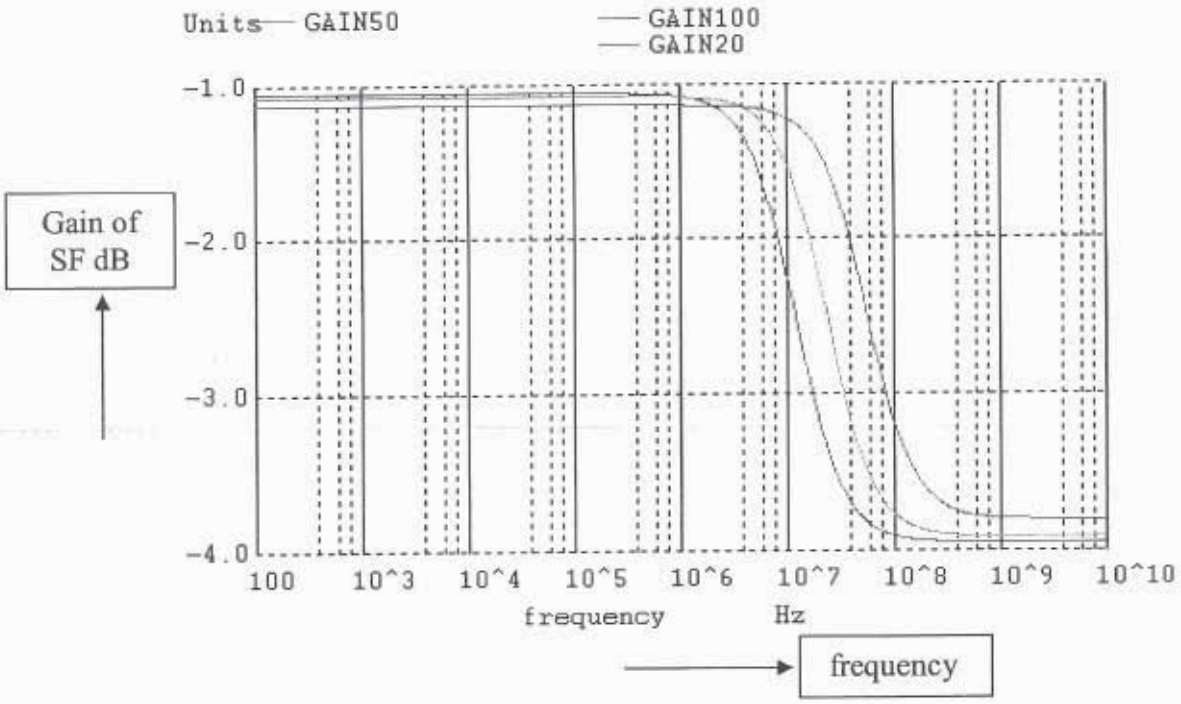

Figure 3.6. Gain of the NMOS SF with body effect for W = 20, 50, 100

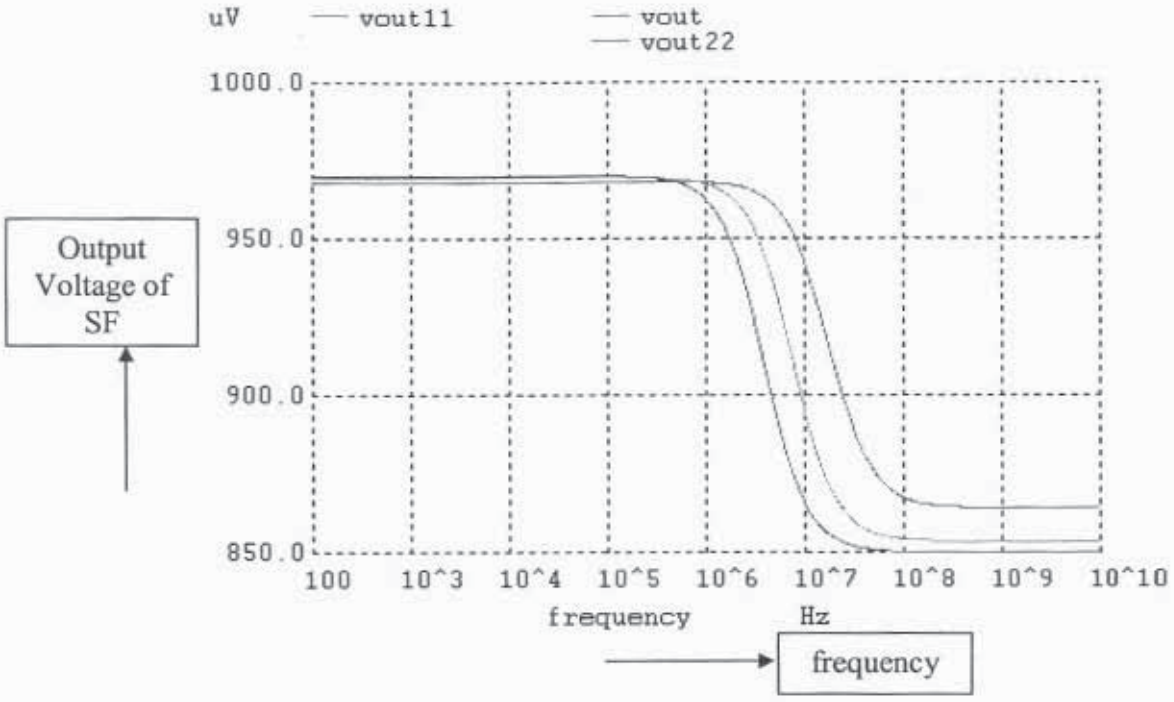

Figure 3.7. Output Voltage of the NMOS SF without body effect for W = 20, 50, 100

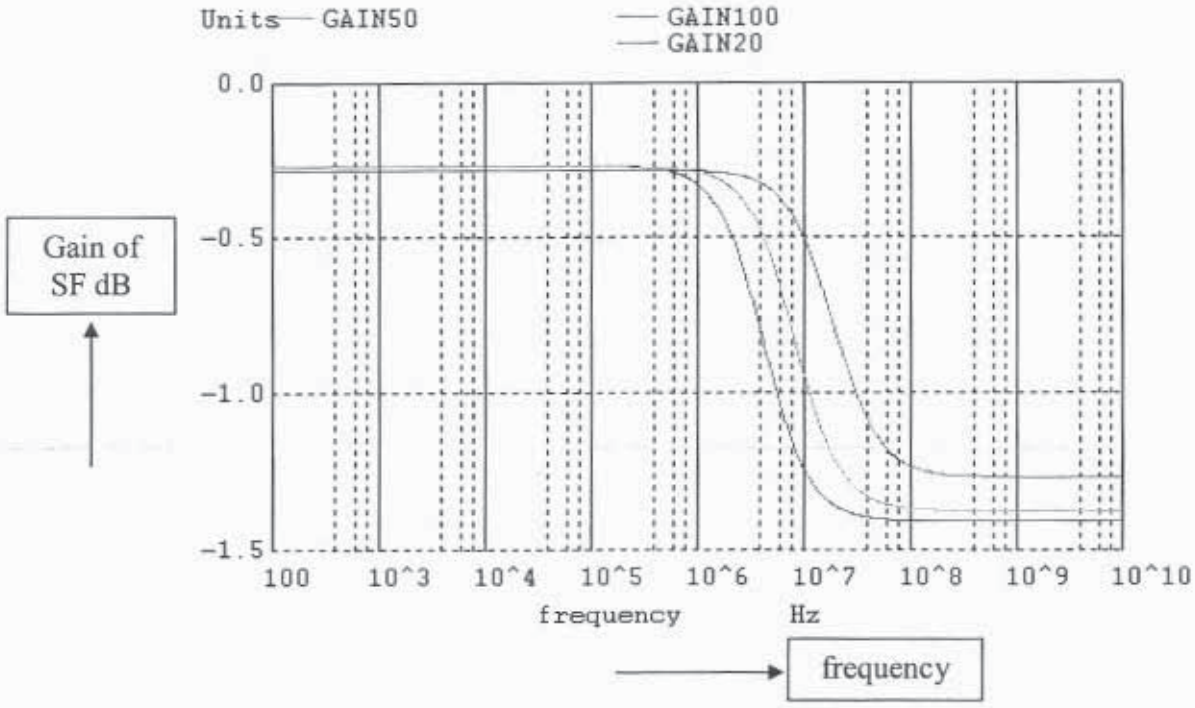

Figure 3.8. Gain of the NMOS SF without body effect for W = 20, 50, 100

Current Mirror

A simple PMOS current mirror [2] is shown in figure 3.9. M1 is a PMOS diode connected MOSFET with its source and gate tied together and M2 mirrors the current in M1. If both M1 and M2 have the same widths and lengths then their gate source voltages and drain to source voltages are equal and the currents flowing in both the MOSFETS are ideally the same. The currents will be in the ratio of the widths as given by Equation 3.1. Doubling the width of M2 will result in doubling the current Isig [2].

$$\frac{I_{ref}}{I_{sig}} = \frac{W_1}{W_2} \qquad (3.1)$$

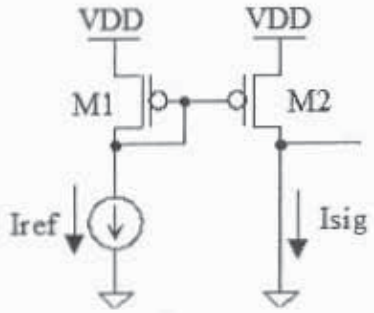

Figure 3.9. PMOS Current Mirror

Figure 3.10 shows the reference and signal currents in the current mirror of figure 3.9 with variations in VDD for a reference current of 10μA and M1 and M2 device sizes of 20/2. It can be seen from figure 3.10 that the currents Iref and Isig are equal when the source to drain voltages of M1 and M2 are the same. As Iref is a constant current source (it will draw a constant current irrespective of the source voltages) will try to hold the gates of the MOSFET's at a constant potential keeping the currents in both the branches constant ideally.

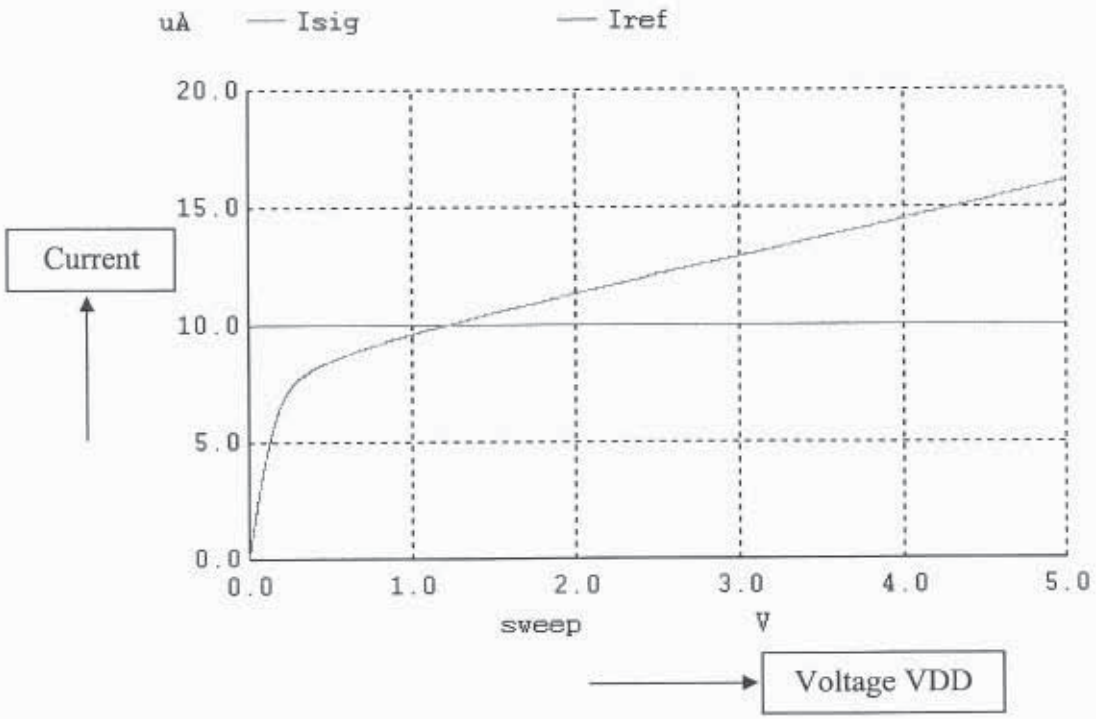

Figure 3.10. Variation of Reference and Signal currents in the current mirror

Switched Capacitor Circuit

A switched capacitor resistor [2] shown in figure 3.11a can be used for realizing large resistors greater than 1Mega ohms. NMOS or PMOS devices can be used for the switches. Phi1 and phi2 are two non-overlapping clocks that are not high at the same time for NMOS devices and should not be low at the same time for the PMOS switches. Figure 3.11b shows a switched capacitor resistor implemented with NMOS switches. Figure 3.11c shows the non-overlapping clocks (not high at the same time) required for the NMOS switches and their periods should be long enough to charge or discharge the capacitor fully. Since phi1 and phi2 are not high at the same time only one of the NMOS switches will be 'on' at a time. If v1 and v2 are not equal and if v1>v2 then when phi1 is high the capacitor is charged to voltage v1 after which phi1 goes low M1 turns off and when phi2 is high (M2 turns on) the capacitor is discharged to voltage v2 this way a charge equal to q1-q2 is transferred between v1 and v2 each clock interval [2]. The average current transferred at any given time is

$$I=\frac{Q}{T}=\frac{q_1-q_2}{T}=\frac{C_{SC}\cdot(v_1-v_2)}{T} \quad (3.2)$$

$$I=\frac{(v_1-v_2)}{R_{SC}} \quad (3.3)$$

Equating (3.2) and (3.3) we get

$$\frac{C_{SC}\cdot(v_1-v_2)}{T}=\frac{(v_1-v_2)}{R_{SC}} \quad (3.4)$$

We get

$$R_{SC}=\frac{1}{f\cdot C_{SC}} \quad (3.5)$$

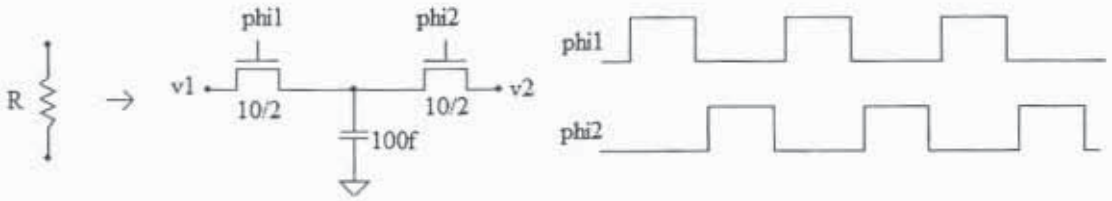

Figure 3.11. a) Switched Capacitor Resistor b) SCR with NMOS switches c) Non overlapping clocks

Hence a large resistor can be simulated with a switched-capacitor circuit [2]; the value of the resistance can be adjusted by adjusting the capacitance and the clock frequency. The advantage of using switched capacitor circuits is less layout area when a large resistor (an implanted or diffused resistor takes up large layout area) has to be realized. And with variations in process characteristics and temperature the resistance will vary; the resistance value can be adjusted by varying clock frequency with a switched capacitor circuit. But the disadvantage of using SCR's is more power consumption and the need for non-overlapping clocks, which makes it more complicated. Charge can be added or removed using switched capacitor circuits.

Figure 3.13 shows the simulation of the SCR of figure 3.12. The two non-overlapping clocks and the voltage across the capacitor have been shown. It can be seen that when phi1 is high the capacitor charges to 4V and when phi2 is high the capacitor discharges to 2V. Body effect in NMOS switches is the reason why the voltage is not charging all the way to 4V.

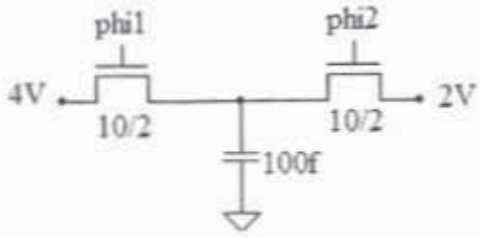

Figure 3.12. Switched capacitor circuit

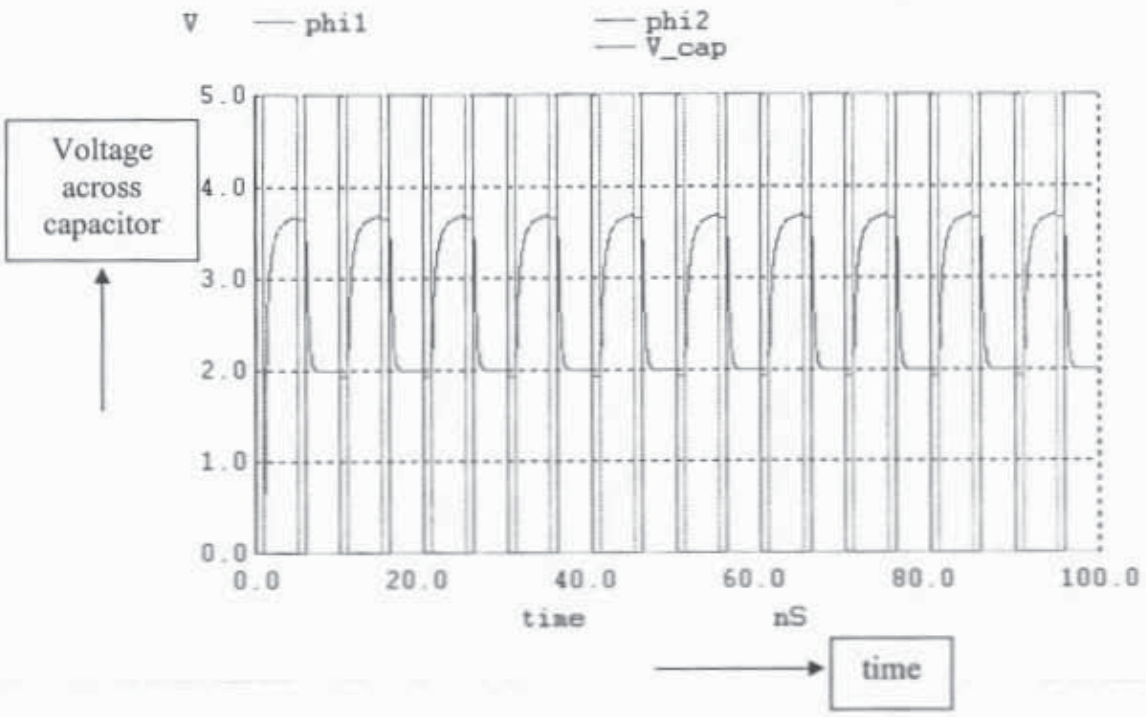

Figure 3.13. SCR Operation

Non-Overlapping Clock Generator

A non-overlapping clock generator [2] is required to generate the two non-overlapping clock phases needed for the switched capacitor circuit on chip.

Figure 3.14 shows the circuit for generating the two non-overlapping clocks that are not high at the same time, from a clock signal.

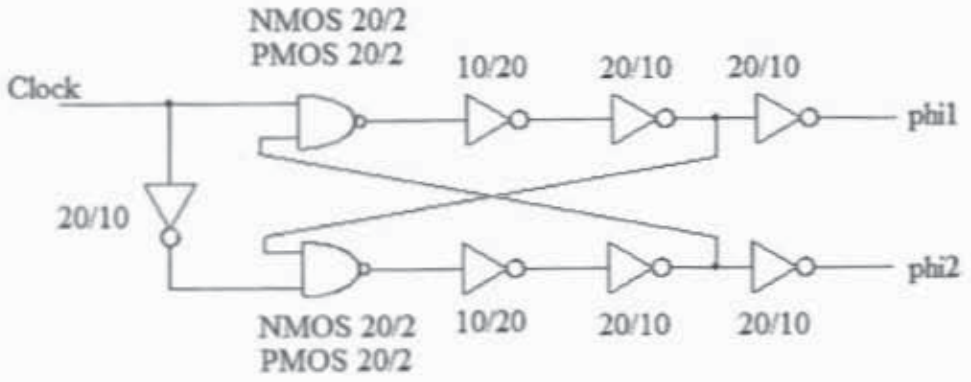

Figure 3.14. Non-Overlapping Clock Generator

Long length inverters have been used on the output of the NAND gates to increase the delay and hence the separation between the times the clock signals phi1 and phi2 are high. When clock goes high phi1goes high and phi2 goes low. When clock goes low phi1 goes low phi2 goes high. In this way the two clocks are never high at the same time.

Figure 3.15 shows the simulation of the non-overlapping clock generator seen in figure 3.14 showing the two non-overlapping clocks that are not high at the same time.

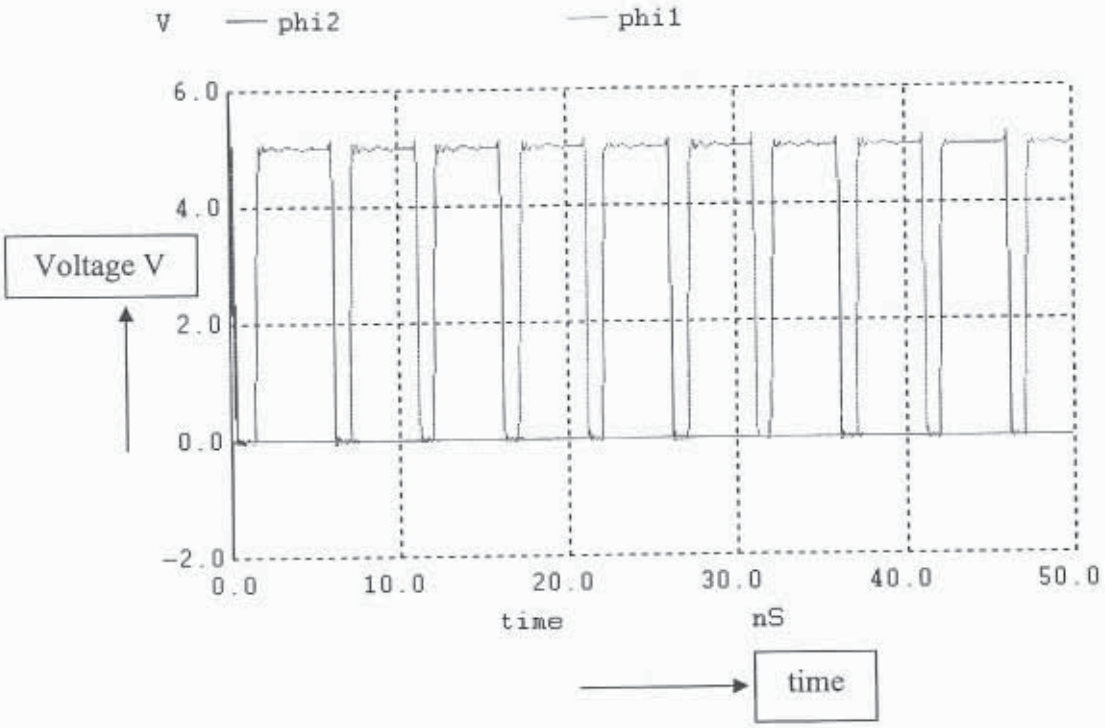

Figure 3.15. Simulation showing the Non-Overlapping Clocks generated from the generator

Feed Back Circuit

The SCR circuit in figure 3.16 shows the feedback circuit [2] for the DSM. When phi2 is high the capacitor is discharged to ground. When phi1goes high phi2 goes low shutting off the bottom NMOS, charging the capacitor to the bit line voltage, when the controlling switch M1 turns on indicating that the feedback path be enabled. The switch M1 is controlled by the comparator, which determines whether the feedback path has to be enabled or not.

Figure 3.17 shows the simulation for the feedback circuit of figure 3.16 showing the current through the bit line voltage. The bit line voltage is varied 2V to 5V. Here we can see that as Vbit increases the current also increases as Qcap= Csc ΔVbit.

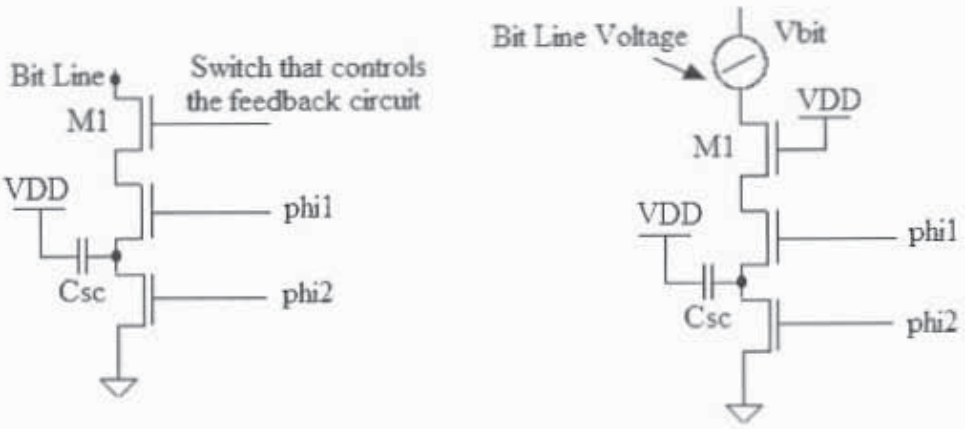

Figure 3.16. Feedback Circuit

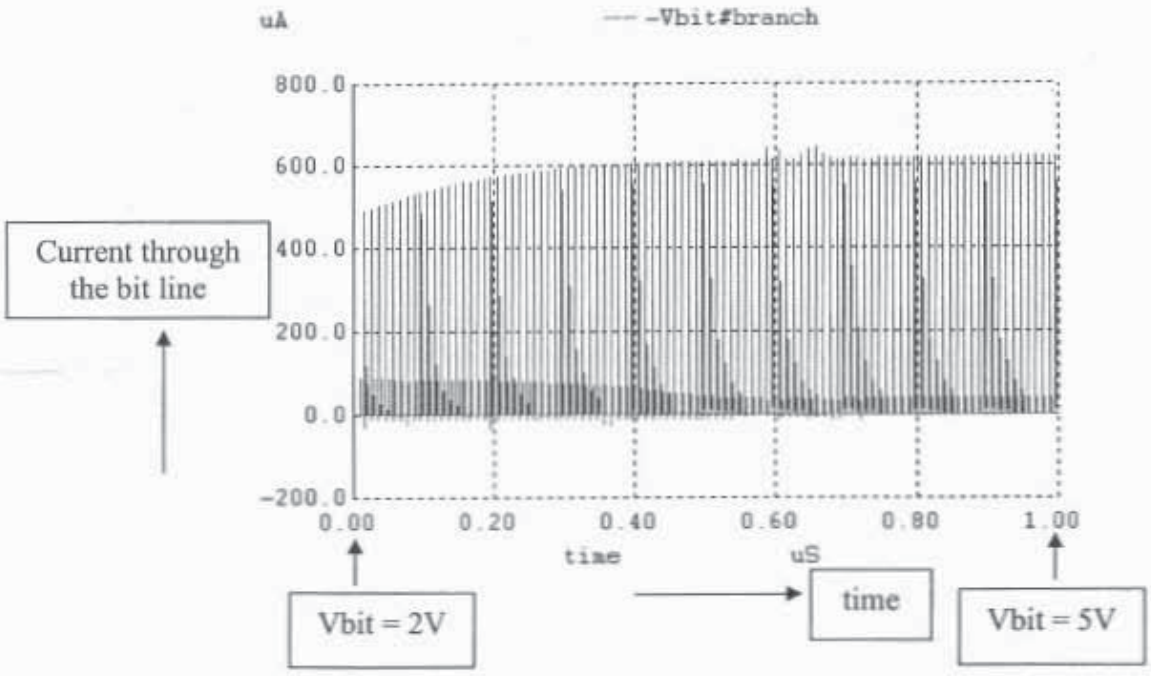

Figure 3.17. Current through the bit line voltage source

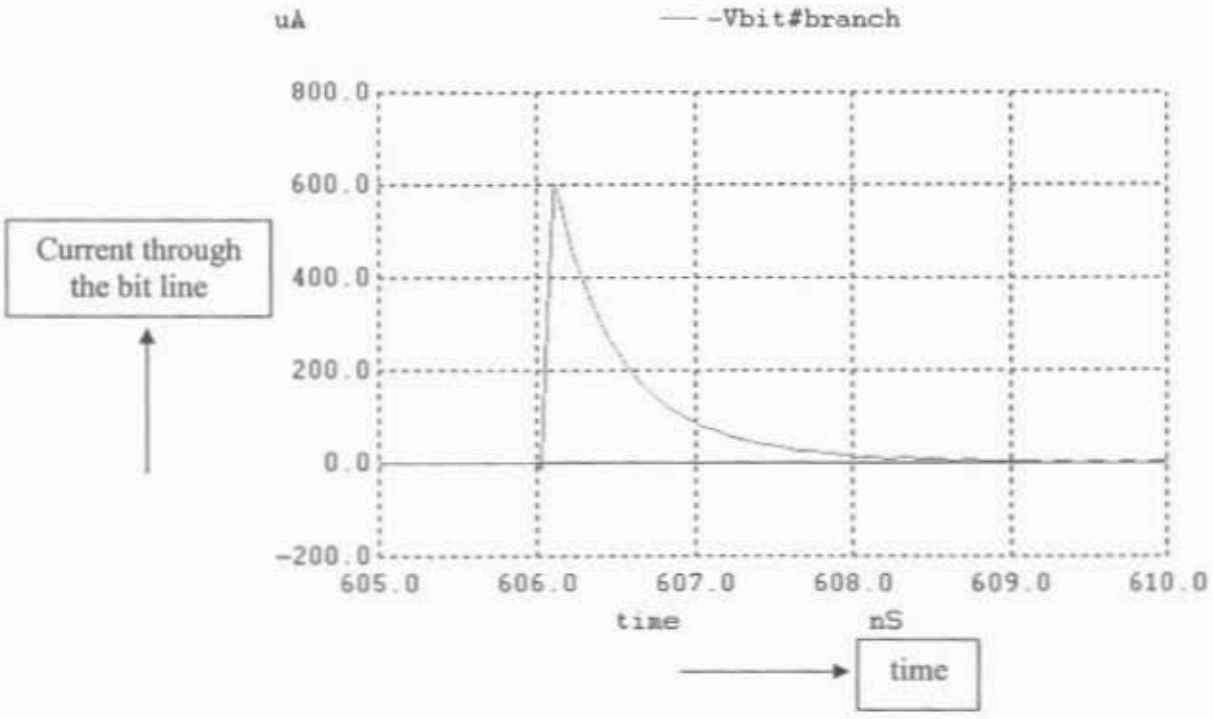

Figure 3.18. Showing a Single Current pulse

Figure 3.18 shows a single current pulse of Figure 3.17. Adding MOSFET M1 (figure 3.20) the NMOS source follower makes the charge on the SCR's independent of the bit line voltage. Now the charge on the capacitor Csc given by Qcap= Csc (Vcol-Vthn) gives a reduced voltage swing and reduced current (comparing figure 3.18 without the NMOS source follower and figure 3.21 with the NMOS source follower) and good linearity. The amount of charge on the bit line is more constant independent of the bit line voltage [2].

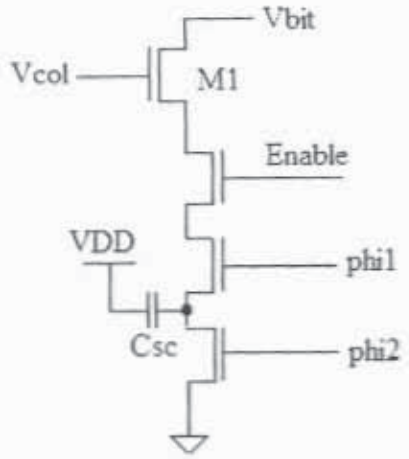

Figure 3.19. Feedback Circuit with the NMOS source follower

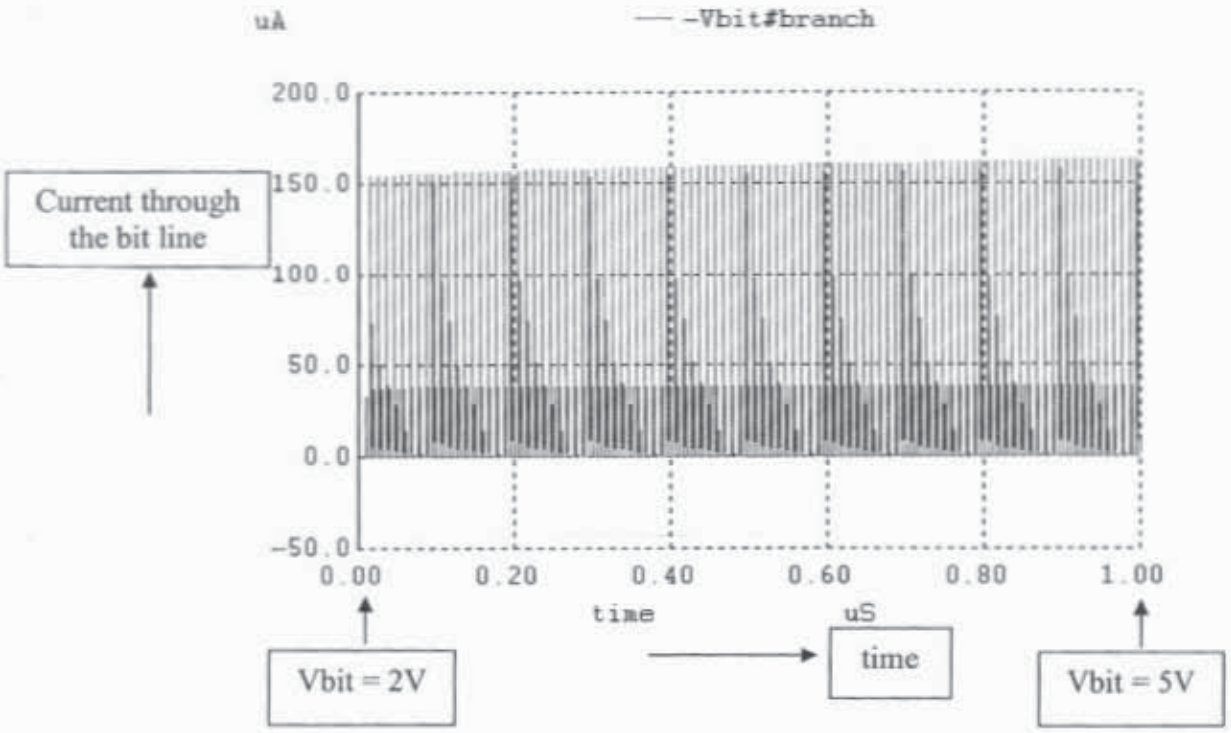

Figure 3.20. Current through the bit line voltage source

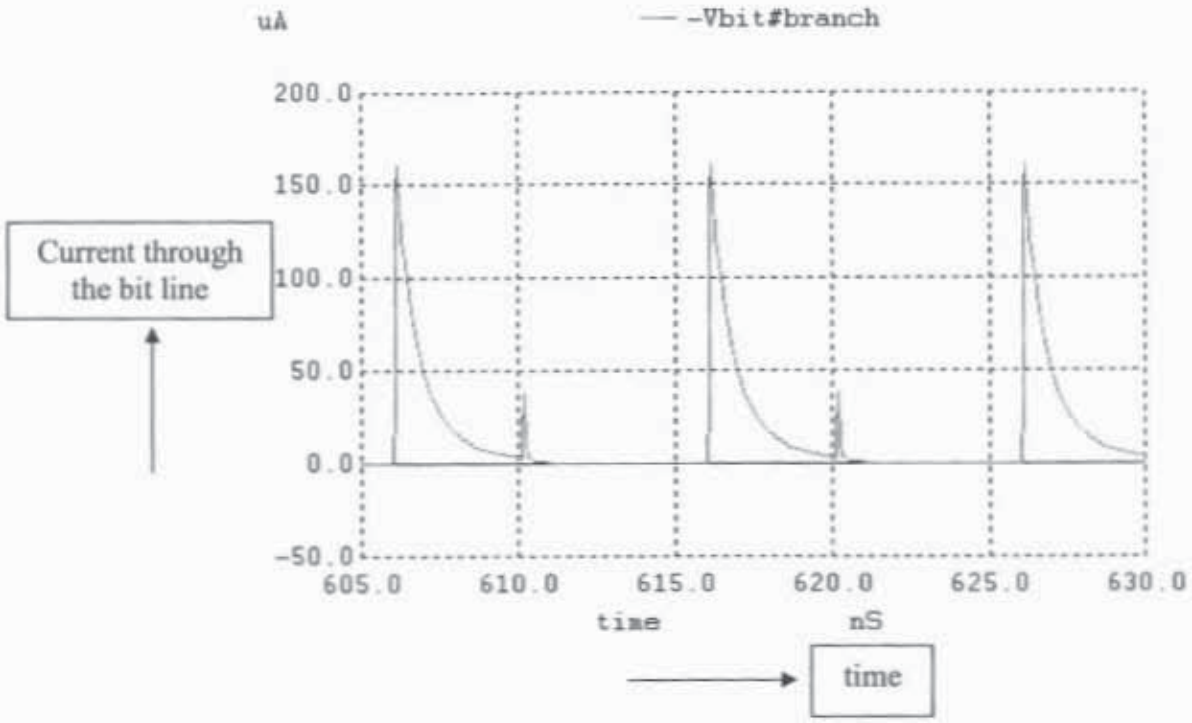

Figure 3.21. Incomplete Settling

Looking at individual current pulses of figure 3.20 in figure 3.21 we can see that there is incomplete settling i.e, the current in the bit line does not go to zero when phi2 goes high. This is due to clock feedthrough. Lowering the clock frequency of the circuit will reduce the incomplete settling of the circuit as seen in the simulation of figure 3.22. Here the time period is 20ns.

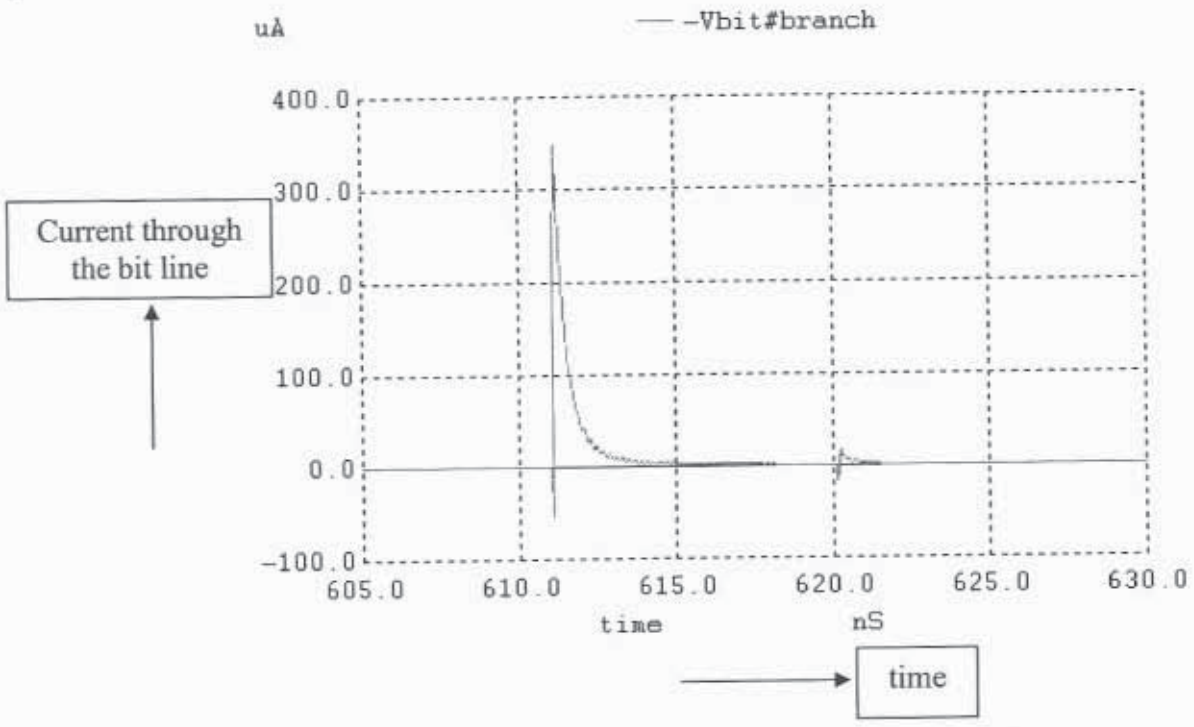

Figure 3.22. Lowering Clock Frequency to reduce Incomplete Settling

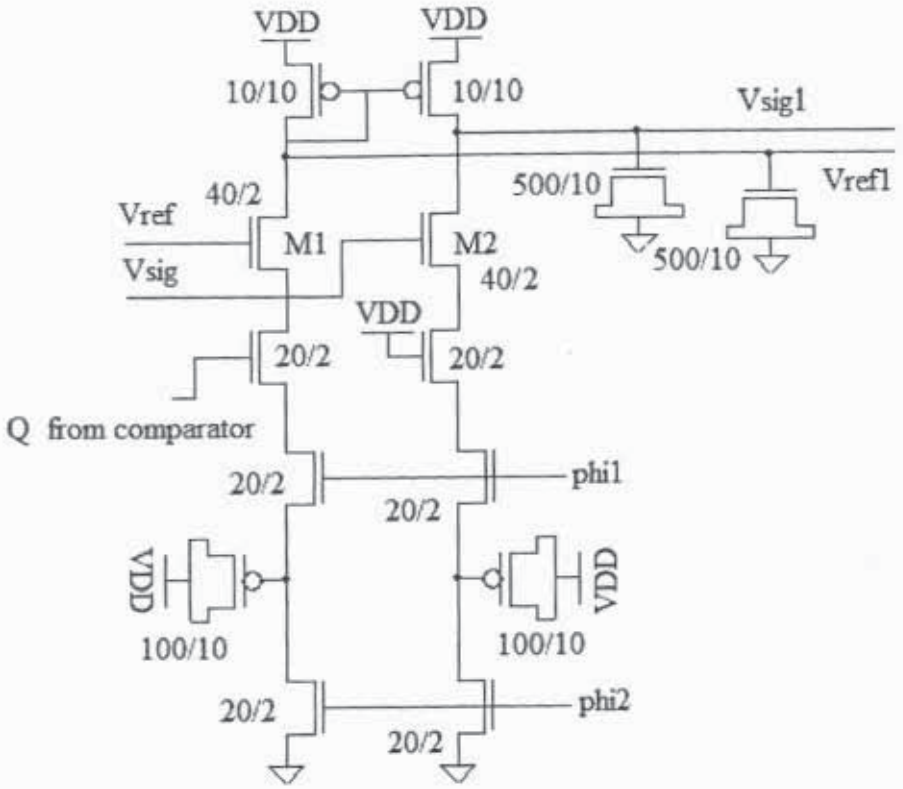

Figure 3.23. DSM Input Circuit

Figure 3.23 shows the DSM input circuit [2] consisting of NMOS source followers and the feedback circuit. The MOSFET's M1 and M2 are made very wide so that it has a Vgs very close to Vthn. If the signal from the comparator goes high the resistor (SCR) in the reference signal feedback path is enabled. If the reference signal is greater than the desired signal we want to measure, then the current in the reference path will be greater than the current in the desired signal path (since Vgs of M1 is greater than Vgs of M2). The MOSFET M4 (charge controlling switch) in the desired signal path is always enabled. The capacitor on the node Vsig1 is charged with the difference in the currents Iref-Isig.

The PMOS current mirror can ideally source the same current through each side and when Vref >Vsig M1 can sink more current due to it's higher gate voltage than M4

resulting in charging the capacitor on the node Vsig1 to a higher voltage the Q signal from the comparator goes low thus increasing the charge on node Vref1.

When switch M4 closes, the amount of charge dumped on to the capacitor in the desired signal path is

$$Q_{cap_{sig}} = C_{sc} \cdot (V_{sig} - V_{thn})$$

When switch M3 closes, the amount of charge dumped on to the capacitor in the reference signal path is

$$Q_{cap_{ref}} = C_{sc} \cdot (V_{ref} - V_{thn})$$

Figure 3.24 shows the simulation showing voltages on the nodes Vref1 and Vsig1, which ideally track each other due to the feedback.

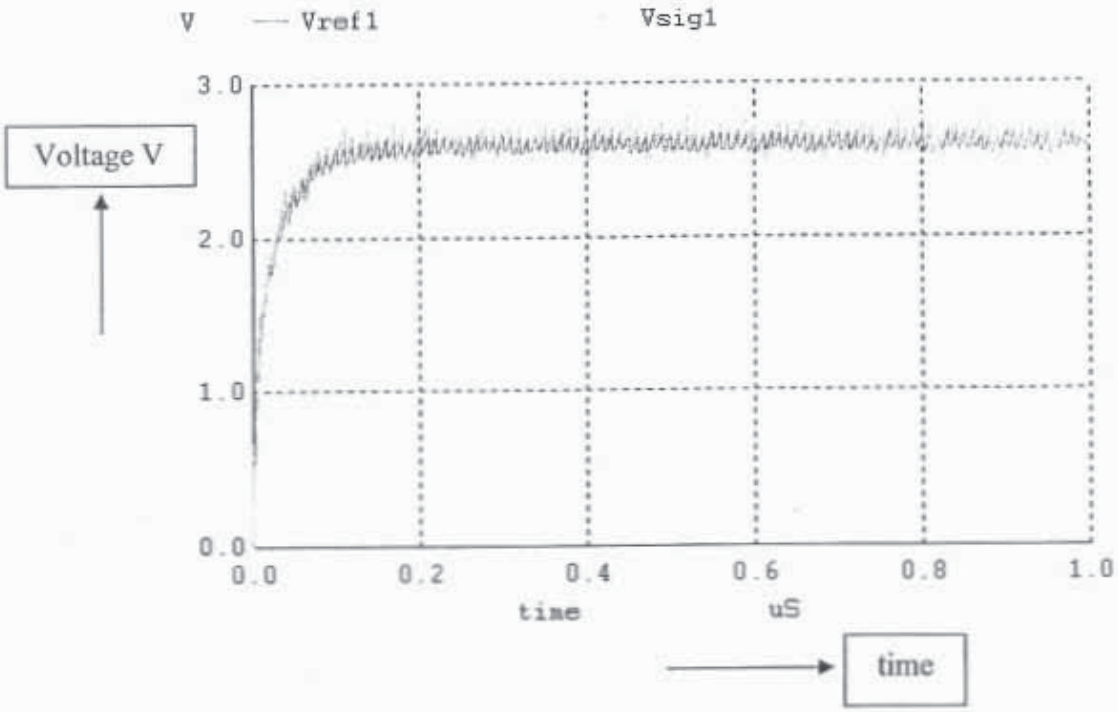

Figure 3.24. Showing the shifted reference and signal voltages

Sampling Reference and Intensity Signals

The reference signal or the black signal is sampled first followed by desired signal on to the input sampling capacitors through switches. If the signal from the pixel varies during conversion time then the ADC will produce a wrong output. To handle these changing inputs this sample hold capacitor is added. The hold settling times, linearity, clock jitter, hold-mode feed through of the S/H will affect the performance of the ADC. There should be less noise through the MOSFET sampling switches because for high precision ADC's coupling perturbations in the held signal can cause bit errors, and thus distortions in the digitized signal [20]. The two main problems with sample and hold circuits are charge injection and clock feed through which cause non-linearity and affect circuit performance particularly resolution.

The MOSFET switches should have a linear transfer function and constant on resistance independent of the input voltages in order to have the RC (time constant) for charging the capacitor a constant for all input signal amplitudes [20]. A CMOS transmission gate (TG) is used for the switches because a TG can pass both a logic high and a logic low without a threshold drop thus giving full logic level swing, it also has a lower overall resistance (since the resistances of PMOS and NMOS are in parallel) and a lower clock feed through when compared to the PMOS or NMOS pass gates. But the TG has a larger layout area; more control signals to deal with and has leakage paths to both VDD and GND.

Charge Injection and Clock Feed Through

Charge injection from MOSFET switches affects the accuracy of sample and hold circuits, switched capacitor filters and ADC circuits. There are several methods to model charge injection and to predict the amount of charge injected in switches [16]. Figure 3.25 shows the charge injection mechanism [15]. When Clk goes high the MOSFET switch is on and it is operating in the triode region and drain to source voltage is very small. When it is 'on' there are a mobile charge under the gate oxide from the inverted channel when it is off these charges are injected in to the source and drain (the voltage source and the hold capacitor) and the substrate resulting in an error component to the sampled voltage on Chold which is a function of input voltage. The amount of charge transferred to the hold capacitor when the transistor is off determines the error (which is usually in the mV range) caused by charge injection.

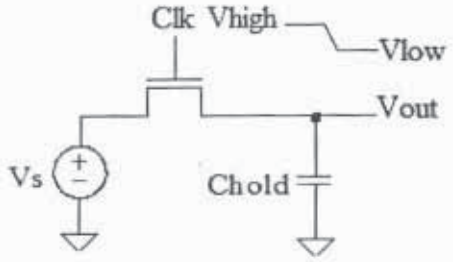

Figure 3.25. Showing charge injection

If the MOSFET is 'on' then we don't have this problem the hold capacitor will simply be charged with the input voltage through the resistance of the NMOS.

When the MOSFET is operating in triode and Clk goes high, Clk will feed through the parasitic capacitances (gate-source and gate-drain capacitances), which has no effect on the output voltage, as the hold capacitor will charge through the NMOS resistance. But a voltage change occurs on the output when Clk is low as it feeds through due to the voltage divider between the hold capacitor and the parasitic capacitance shown in figure 3.26.

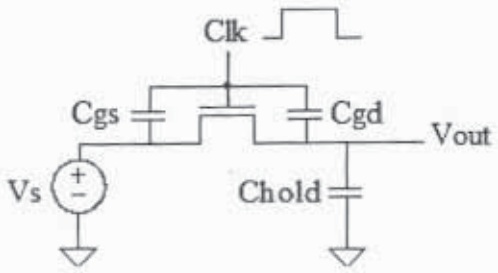

Figure 3.26. Showing clock feed through

Clock feed through [15] and charge injection can be cancelled out by using various methods. By using a transmission gate for the switch the charges released from complementary MOSFET's tend to cancel out each other to a certain extent. A dummy transistor with drain source and bulk shorted (to avoid dc current flow) and with half the channel area of the main switch can be placed in series with the main switch to reduce charge injection by one or two orders of magnitude [18]. Using fully differential topologies and providing active compensation by low sensitivity auxiliary input also reduce charge injection [16]. Several open loop and closed loop sample and hold architectures for increasing the speed of the sample and hold circuits have been proposed but they suffer from clock feed through and charge injection problems too. A high speed sample and hold technique using Miller hold capacitance to improve the

precision and reduce charge injection problem in open loop S/H circuits has been proposed [17].

Showing Charge Injection & Clock Feed Through from the TG's

Figure 3.28 shows the clock feed through on the output of the TG in figure 3.27 with PMOS & NMOS widths 30/2 & 10/2 respectively for a 2.4V input, the voltage change is around 12 mV. PMOS clock feed through is thrice the NMOS clock feed through.

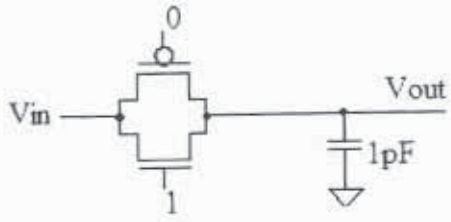

Figure 3.27. TG

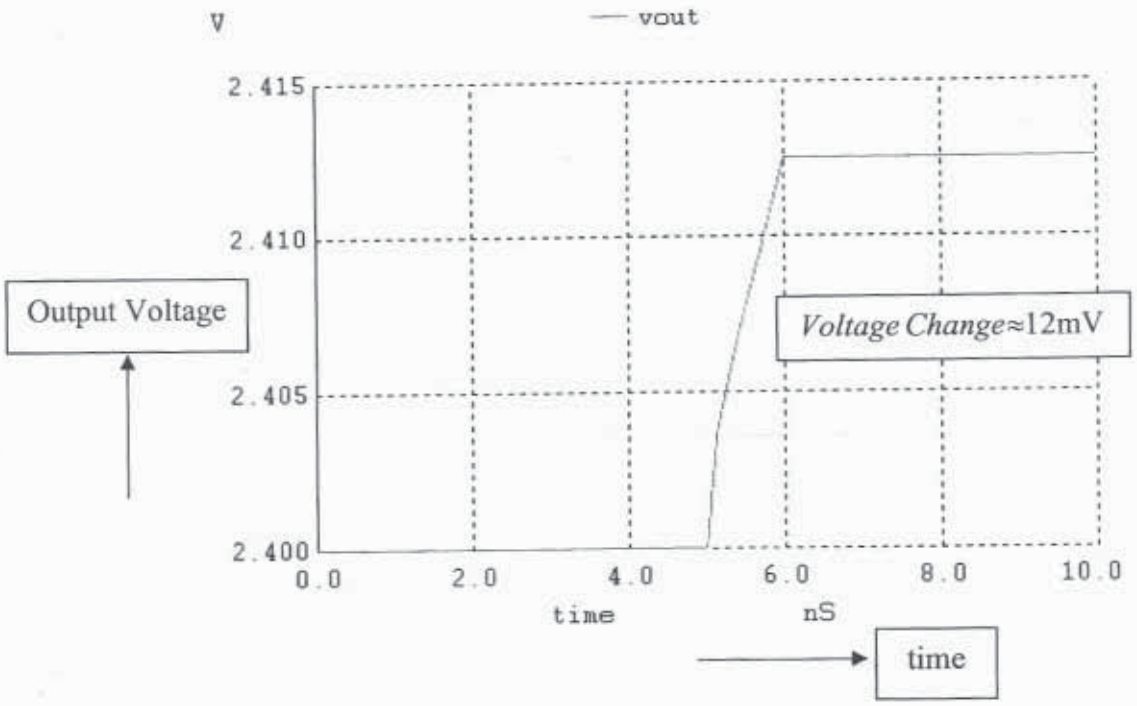

Figure 3.28. Clock Feed through of TG

Having equal width devices for both PMOS (20/2) & NMOS (20/2) reduces clock feed through (clock feed through from PMOS and NMOS are in equal and opposite directions tending to cancel each other though not perfectly) as shown in the simulation of figure 3.29. The voltage change is only around 1mV.

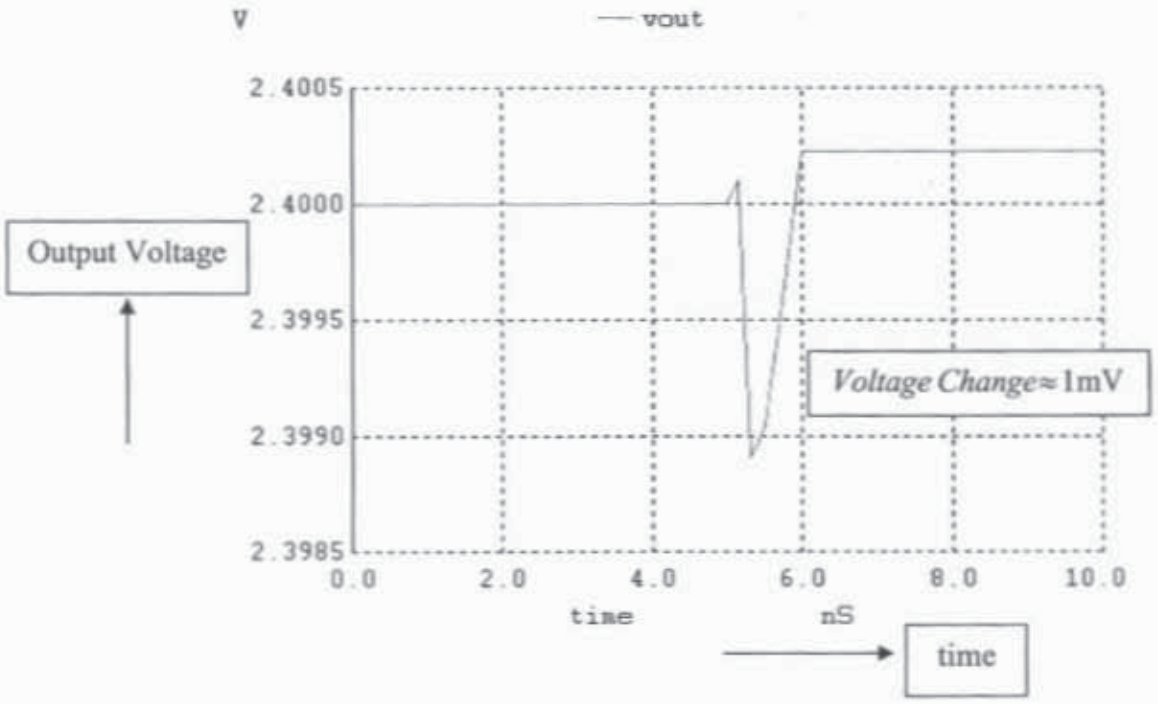

Figure 3.29. Clock Feed through of TG

Simple S/H Circuit

Figure 3.30 shows sample and hold circuit used for this design. When switch is closed the input signal is connected to hold capacitor and when it is open the input is disconnected from the capacitor and the capacitors stay charged with the required signals. The TG in the reference signal path goes high first and the reference signal is sampled on to the hold capacitor after which this TG shuts off. Then TG in the desired signal path goes high sampling the desired signal on to the hold capacitor.

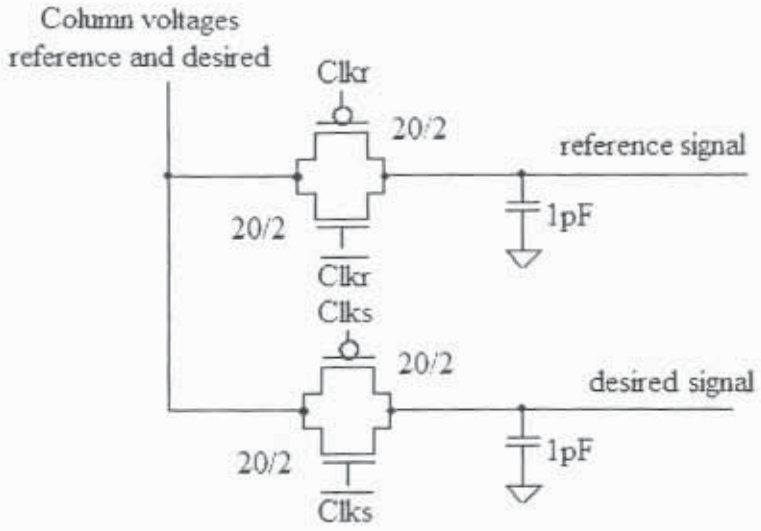

Figure 3.30. Sample & Hold Operation

Figure 3.31 shows the simulation of the circuit shown in figure 3.30 with reference (dark) signal of 2.4V and intensity signal of 2.2V.

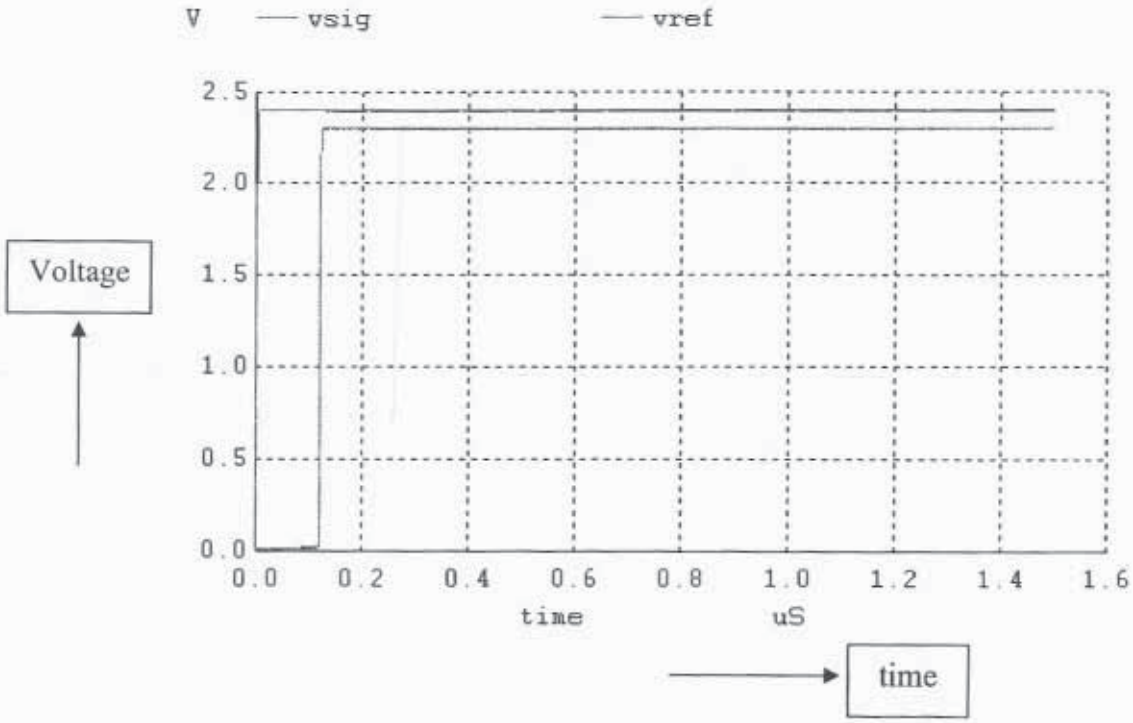

Figure 3.31. Showing reference and signal voltages after sampling

Thermal Noise

Thermal noise in a resistor is due to the random motion of electrons with variations in temperature. The sample and hold circuit [9] seen in figure 3.27 can be modeled as an RC circuit seen in fig 3.32. The hold capacitor charging through the MOSFET's parasitic resistances gives rise to a thermal noise introducing fluctuations in the reference and signal voltages measured. R is the resistance that comes from the MOSFET's parasitic resistances here Rn // Rp and C is the hold capacitor.

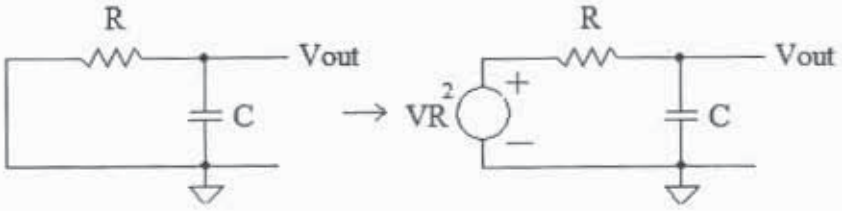

Figure 3.32. Modeling noise in a RC low pass filter [9]

The noise in the resistor can be modeled by the voltage source VR seen in fig where VR^2 = 4kTR is the thermal noise PSD of the resistor [9]

The transfer function can now be written as

$$\frac{V_{out}}{V_R}(s)=\frac{1}{1+sRC} \qquad [9]$$

The total noise power at the output can be written as

$$P_n=\int_0^{\infty}\frac{4kTR}{1+4\pi^2R^2C^2f^2} \qquad [9]$$

$$P_n=\frac{2kT}{\pi C}\cdot\left|\tan^{-1}u\right|_0^{\infty}=\frac{kT}{C}\ (V^2) \quad [9]$$

The total RMS noise voltage measured at the output can be given by

$$V_{noise,RMS}=\sqrt{\frac{k\cdot T}{C}} \qquad [9]$$

where k = Boltzmann's constant = 1.38E-23 J/K

T = Temperature in Kelvin

C = Capacitance in Farads

The noise voltage is independent of the MOSFET's resistances and is only dependant on the size of the capacitor because for bigger values of R the noise per unit bandwidth increases but the overall bandwidth of the circuit decreases due to higher time constant. Increasing the size of the capacitor will decrease the thermal noise sampled on to the capacitor but the speed of the circuit degrades. [9] Using a 1pF capacitance the value of the thermal noise at room temperature can be calculated as follows:

$$V_{noise,\,RMS} = \sqrt{\frac{(1.38e{-}23)\cdot 300}{1pF}} = 64.3\mu V$$

Setting the hold capacitor to 1pF gives an RMS noise voltage of 64.3μV at room temperature. So when the TG turns on both the input signal (reference or intensity) and the kT/C noise voltage (64.3μV) are sampled on to the hold capacitors.

Comparator Design

Figure 3.33 shows the comparator [2] with the PMOS imbalance MOSFET's used for this design.

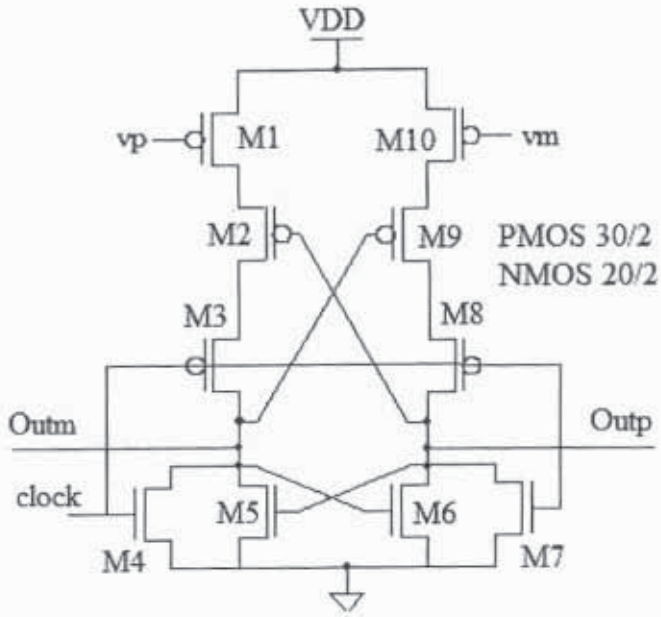

Figure 3.33. Comparator Circuit

When clock is high M3 and M8 are off, the MOSFET's M4 and M7 turn on pulling the nodes Outp and Outm low, turning M2 and M9 'on' pulling the nodes n1-n4 'high'. In this way all the nodes are actively driven 'high' or 'low'. This is important for erasing the comparator's memory, since a floating node might swing to a voltage value of the previous sense operation. Since M3 and M8 are off there is no direct path from VDD to ground so the current pulled from VDD is also very less; it does not pull current except when the clock is switching states. When clock is low an imbalance is created and the nodes vp and vm are compared. If vp>vm the current in M1 is less than the current in M10 (since Vsg of M1 is less than Vsg of M10). The node n4 will be pulled high and when clock goes low Outp will be pulled high turning M5 on and pulling Outm low (turning M6 off). The comparator pulls an average current of around 45μA. The

maximum input voltage that can be sensed is VDD-Vthp and the comparator functions for negative input voltages also as the gate voltage still above the threshold voltage of the PMOS device. For very high input voltages the input PMOS devices will be off and the imbalance cannot be created. The minimum VDD required is Vsd,M1+Vsg,M2+Vgs,M5=0.25+0.66+0.92 = 1.83V for the 0.5 micron process.

In the simulation of Figure 3.34 vp input is held at 2.3V and vm input is held at 2.1 V. Since vp>vm the node Outp will be pulled high when clock is low (Outm will be pulled low). When clock is high both the outputs are pulled low as seen in the simulation.

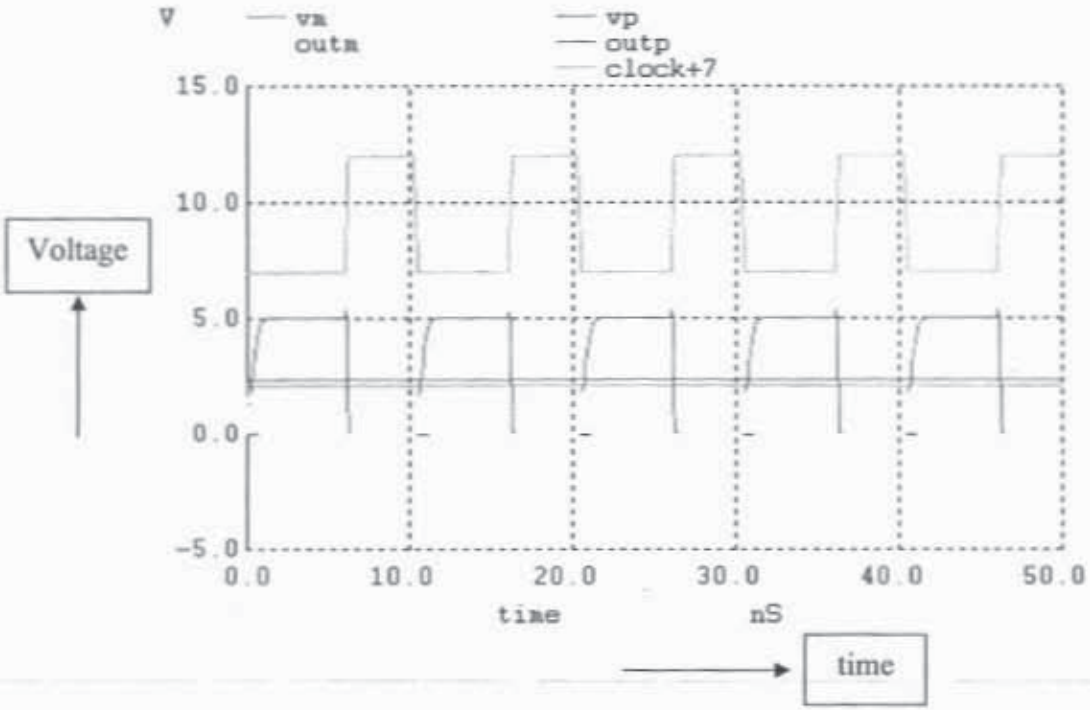

Figure 3.34. Showing the operation of the comparator in figure 3.33

Figure 3.35 shows the inputs, clock signals and outputs of the comparator with vp input swept from 2.1V to 2.3V and vm input is held at 2.2 V. When clock goes low both the outputs are pulled 'high' initially when the sensing operation starts hence the glitches

are seen in the simulation. This can be a problem for sensing since the comparator could take the wrong decision and enable or disable the feedback path when it should not and there can be a charge transfer when there should not be any.

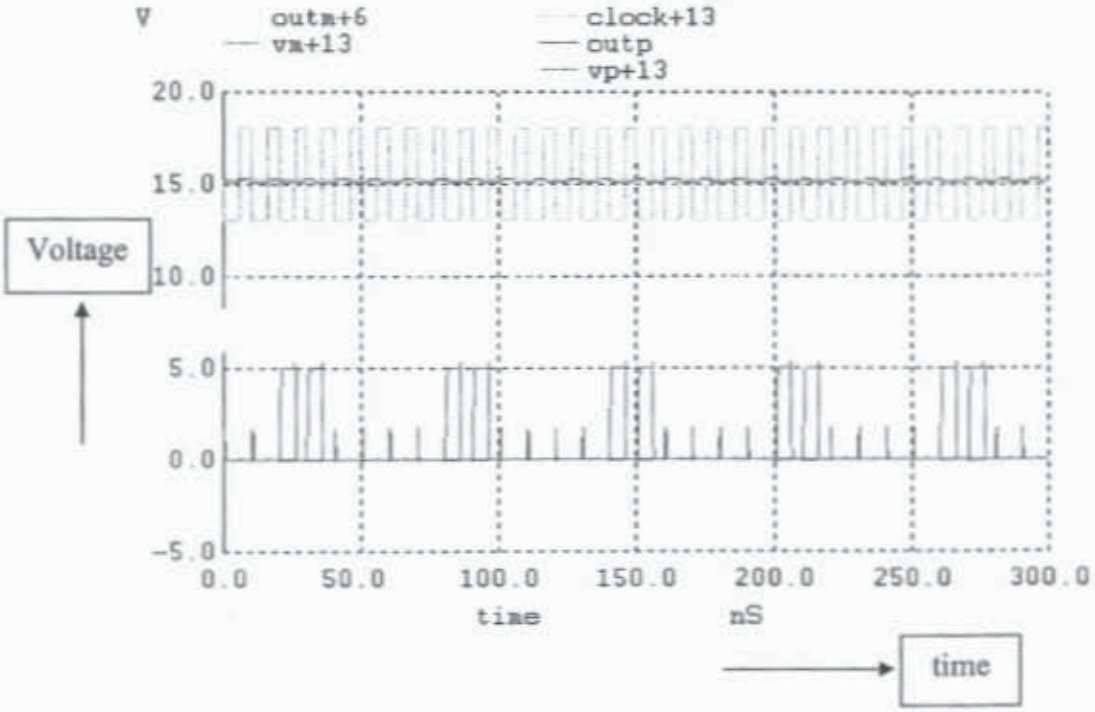

Figure 3.35. Showing the operation of the comparator in figure 3.33

Figure 3.36 shows the comparator with SR Flip-flop added on its output when clock goes high both outputs go low and the latch does not change states which make the outputs of the comparator change on the rising edge of the clock when the inputs change; Outp flows to the Qi output and the Outm flows to the Q output. Adding the flip-flop makes it easier to count the output pulses of the DSM.

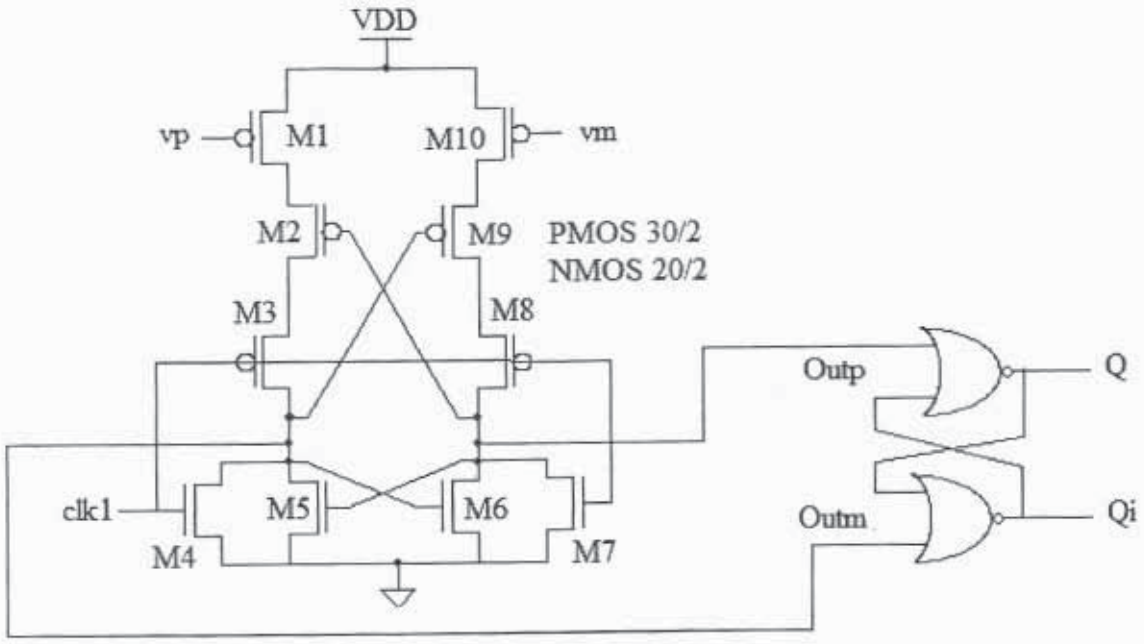

Figure 3.36. Comparator Circuit with SR Flip-flop

Figure 3.37 shows the simulation of figure 3.36. The input and output and the clock signals have been shown. The vp input is swept from 2.3 V and 2.7 V and vm is held at 2.5 V. When vp>vm, Outp goes high and the Qi output goes high (Q goes low). Outputs of the comparator Q and Qi flip when the input data changes only on the edge of clock as seen in figure 3.37.

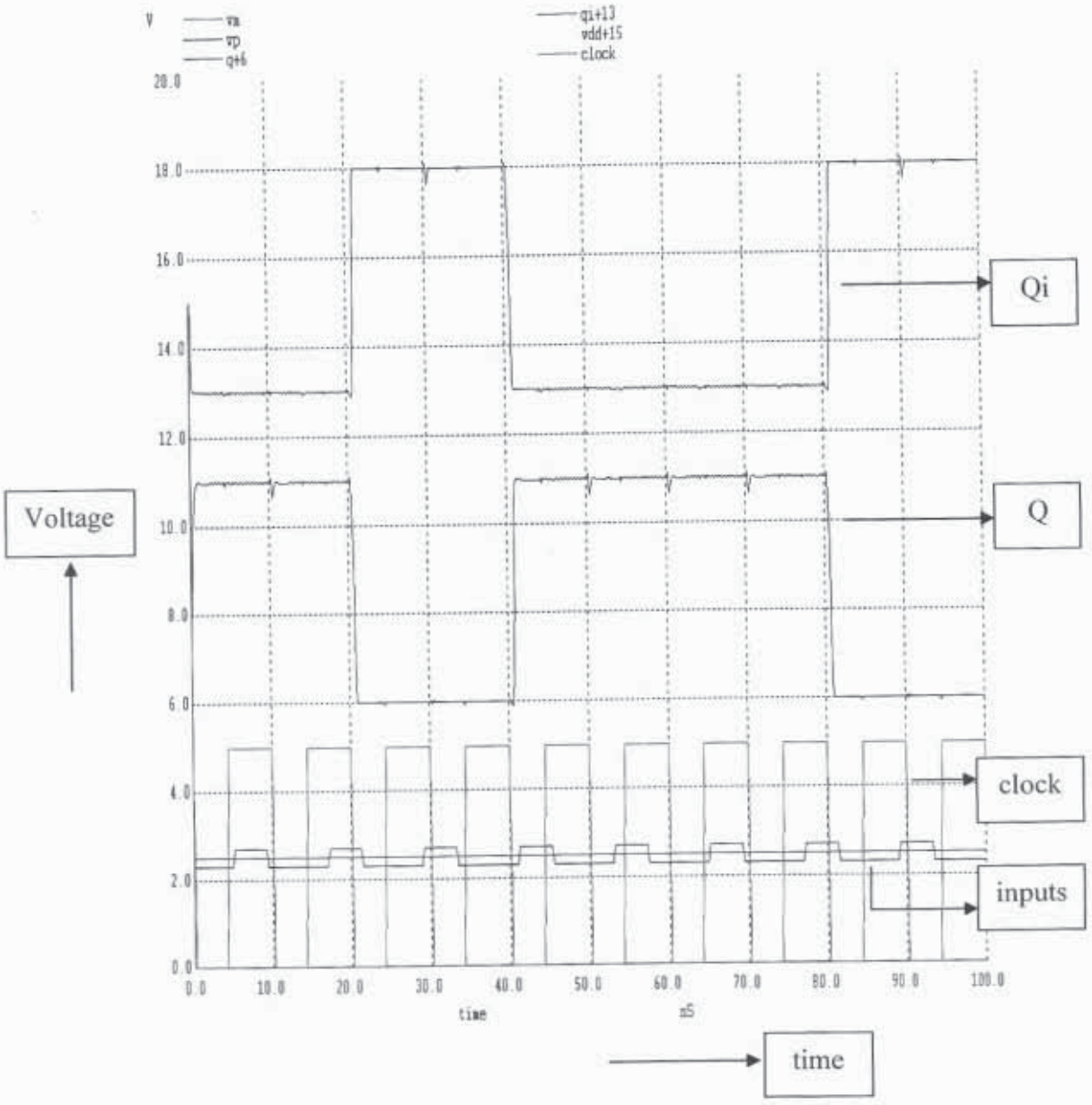

Figure 3.37. Showing the operation of circuit in figure 3.36

Sensitivity of the Comparator

The sensitivity of the comparator is around 8mV. Figure 3.38 shows the transient response of the comparator in figure 3.36 with vp input swept from 2.52V to 2.536V and vm input at 2.528V. Figure 3.38 shows the inputs, clock and the output signal of the comparator. The minimum voltage the comparator can resolve is 8mV.

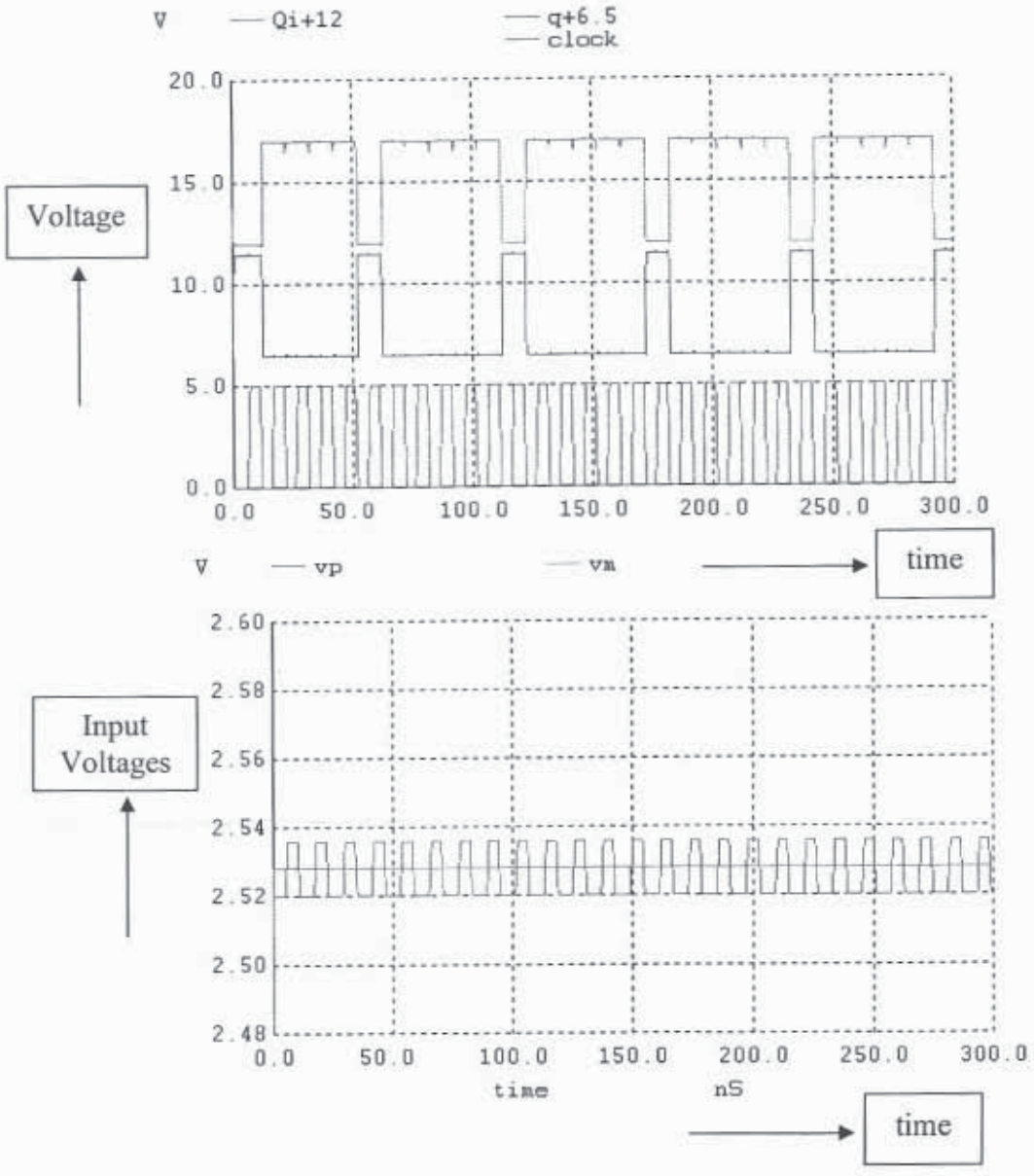

Figure 3.38. Showing the clock, inputs and outputs of circuit in figure 3.36

Simulating the Clock Feed Through Noise & Kickback Noise of the Comparator

Clock feed through noise is present when clock feeds through the input of the comparator circuit and is not a problem here since the inputs are isolated from the clock signal by two MOSFET's. However kickback noise (which is the noise feeding in to the inputs when the comparator is switching states) is present and can become a problem for the sensing circuit.

Simulating the comparator with non-ideal sources can give us the amount of kick back noise injected in to the circuit's inputs. Kick back noise associated with the comparator is around 150mV as seen in figures 3.39, 3.40.

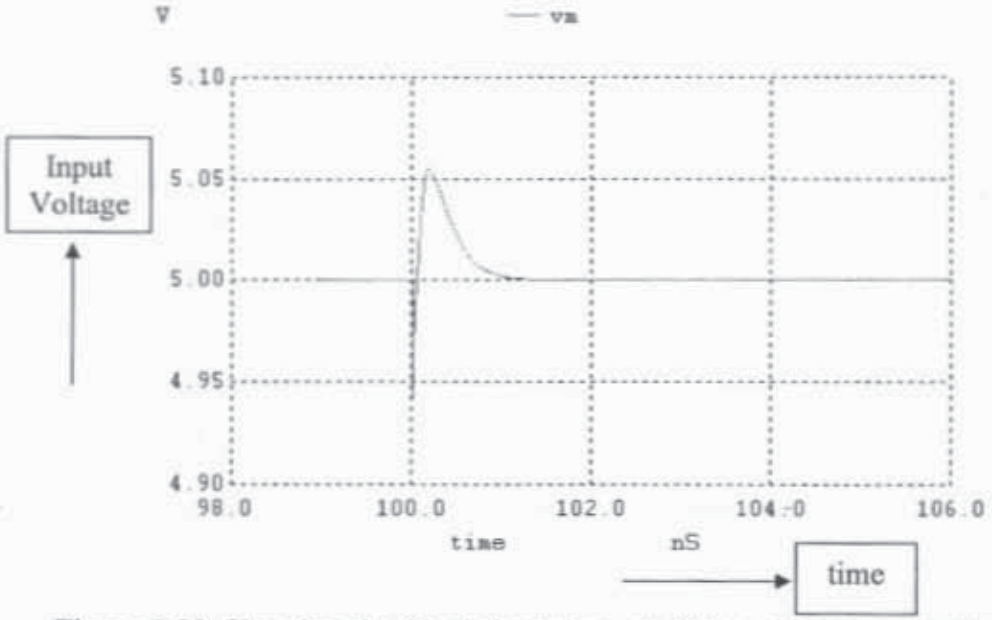

Figure 3.39. Showing the Clock feed through Noise of the comparator

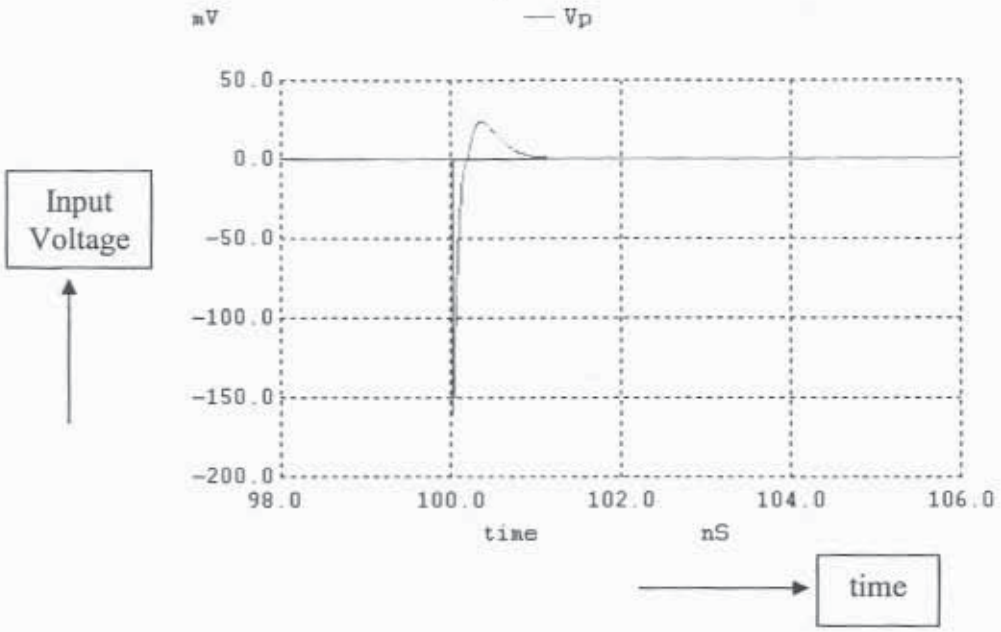

Figure 3.40. Showing the Clock feed through Noise of the comparator

Having 1pF capacitors on the input of the circuit reduces the kick back noise of the comparator to 6mV as shown in the simulation in Figures 3.41, 42. The huge capacitors average out noise so the kick back noise will not interfere with the sensing. The average current drawn from VDD for both the comparator and the flip-flop is around 77μA.

A comparator with both NMOS and PMOS input transistors could be designed so that it has a better sensitivity and wider input signal range beyond power supply rails.

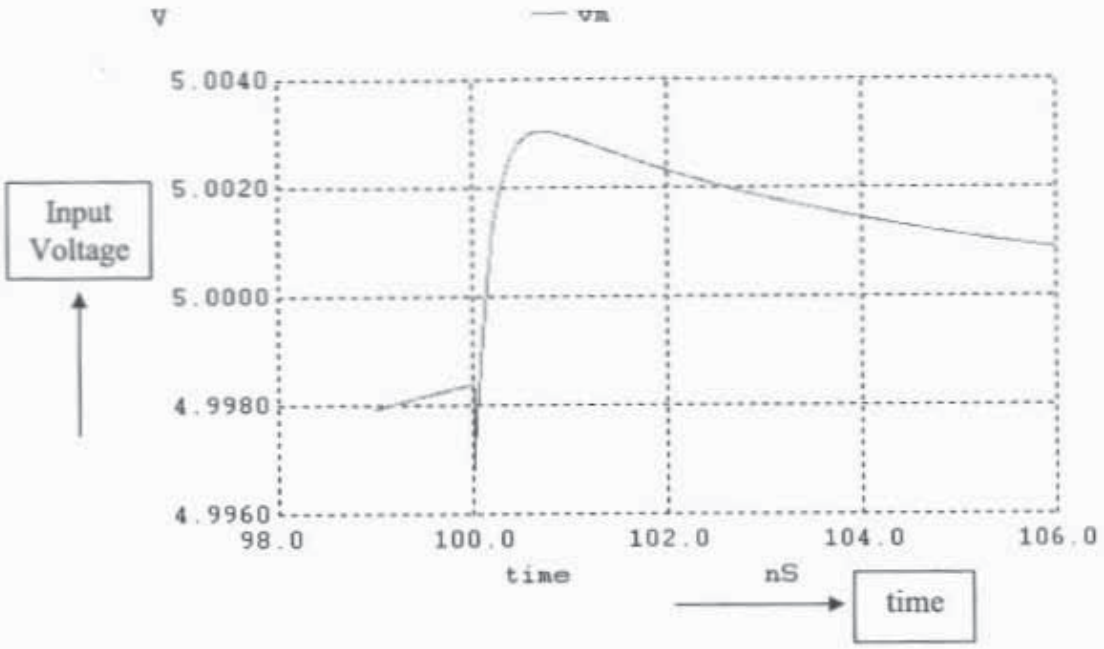

Figure 3.41. Showing the Clock feed through Noise of the comparator with capacitors

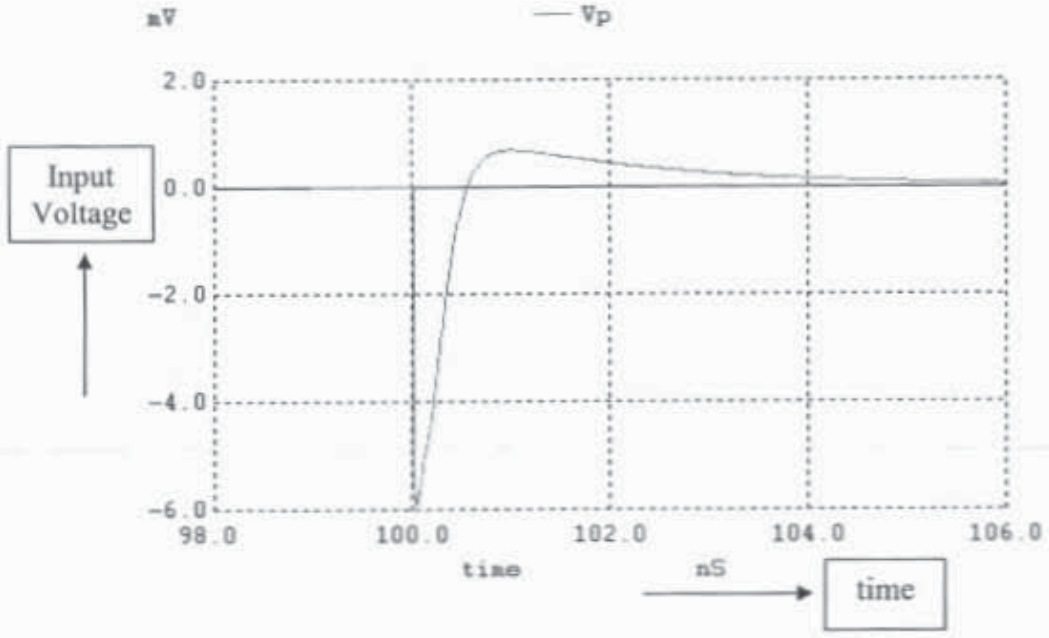

Figure 3.42. Showing the Clock feed through Noise of the comparator with capacitors

Showing the Schematic Used for the Design

The schematic for the DSM ADC [2] is shown in figure 3.43.

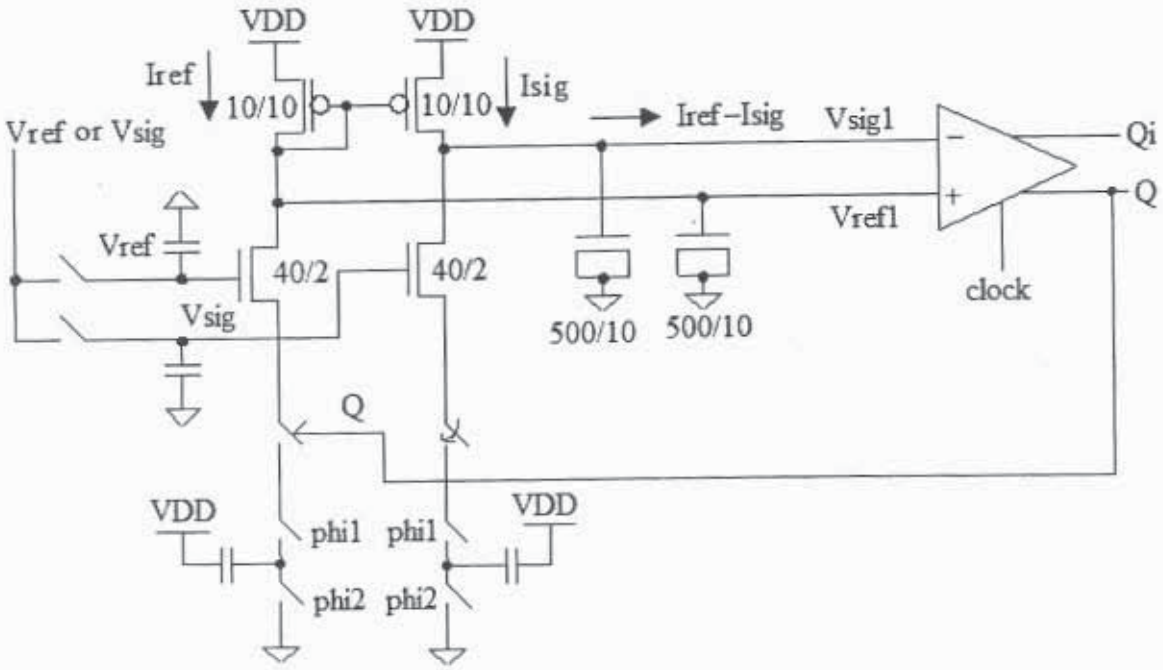

Figure 3.43. Schematic of the DSM

The current in the reference signal path is

$$I_{ref} = \frac{V_{ref} - V_{thn}}{R_{ref}} \qquad (3.6)$$

The current in the desired signal path is

$$I_{sig} = \frac{V_{sig} - V_{thn}}{R_{sig}} \qquad (3.7)$$

Let $V_{ref,shift} = V_{ref} - V_{thn}$

$V_{sig,shift} = V_{sig} - V_{thn}$

Due to the feedback path the currents in both the branches are equal, hence we can write

$$I_{ref} = I_{sig} \qquad (3.8)$$

$$\frac{V_{ref} - V_{thn}}{R_{ref}} = \frac{V_{sig} - V_{thn}}{R_{sig}} \qquad (3.9)$$

$$\frac{V_{ref,shift}}{R_{ref}} = \frac{V_{sig,shift}}{R_{sig}} \qquad (3.10)$$

where $R_{ref} = \dfrac{1}{f \cdot C_{SC} \cdot \dfrac{N-M}{N}}$ $\qquad R_{sig} = \dfrac{1}{f \cdot C_{SC}}$

N = total number of clock pulses

M = number of times Qi output goes high

Substituting for R_{ref} and R_{sig} in Equation we get

$$\frac{V_{ref,shift}}{\dfrac{1}{f \cdot C_{SC} \cdot \dfrac{N-M}{N}}} = \frac{V_{sig,shift}}{\dfrac{1}{f \cdot C_{SC}}} \qquad (3.11)$$

$$V_{sig,shift} = \frac{N-M}{N} \cdot V_{ref,shift} \qquad (3.12)$$

Using the Equation 3.12 the desired voltage signal from the pixel can be calculated.

DSM Sensing Circuit

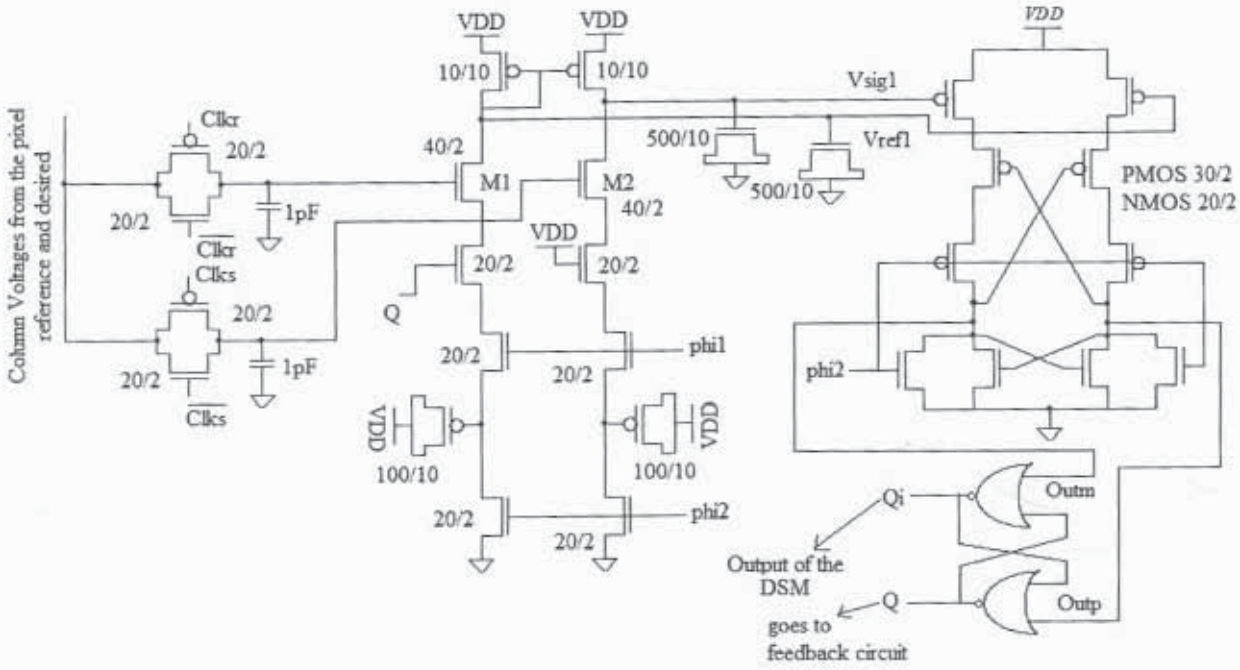

Figure 3.44. DSM Sensing Circuit

The voltages from the pixel i.e. the column voltages are sampled on to the hold capacitors. NMOS source followers are used to convert the voltages in to currents. The width of the NMOS devices is made large so that the gate to source voltage is close to the threshold voltage and will be robust with variations in VDD. The current in the reference path is mirrored using the PMOS current mirror. The switched capacitor circuit in the feedback path behaves like a resistor. Since Vref >Vsig the current that M1 can sink in the reference path is greater than the current in the desired signal path. The PMOS current mirror mirrors the reference current to the other side; the difference in currents will charge the capacitor on node Vsig1. Since there is a lower gate voltage on M2, the capacitor on node Vref1 will be at a lower voltage than the other path. Q will turn low

disabling the feedback path in the reference signal path and decreasing the current in this path resulting in increasing the node voltage Vref1, until the currents in both the paths are equal. Increasing the resistance in the feedback path will result in lowering the current flowing and will take a longer sense time. Using small resistors (increase capacitance of SCR's) will give a faster sense. The sense accuracy depends on how accurately charge can be guided into the feedback capacitors, if the clock high time is very low the NMOS switch of the SCR will be off the charge from the bit line cannot be removed precisely because less charge goes to the switched capacitors increasing the resistance and decreasing the currents flowing. This limits the accuracy of the sense hence giving non linearities.

The output Qi can be given to an up counter, which counts the number of times the switch in the feedback path, has been enabled. By averaging the number of times the capacitor in the feedback path has discharged by comparing it to the reference voltage, we can get an idea of the desired signal on the column voltage in the pixel we are trying to measure. The power consumed by one of the DSM sense-amps on the chip is only around 650μW.

Figure 3.45 shows the signals Vref1, Vsig1 and the output Q from the DSM. It can be seen from the simulation that when Vref >>> Vsig, Iref >>> Isig, the Q output goes low more decreasing the current in the reference signal path until the currents are equal. When Vref1 goes above Vsig1, Q goes back high and tries to discharge the node Vref1.

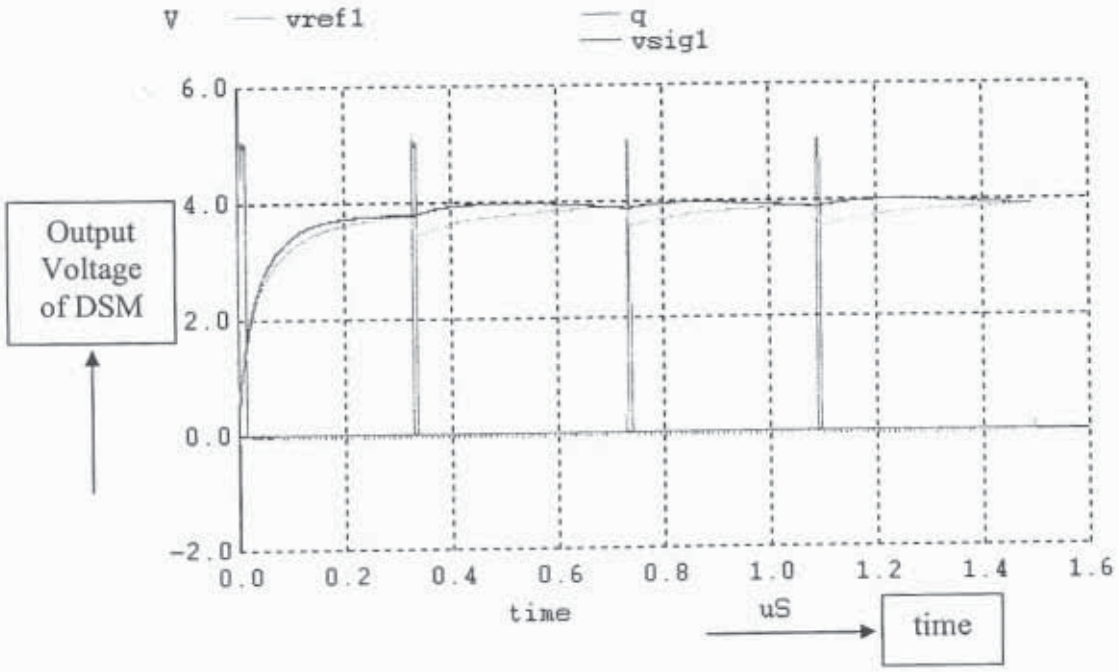

Figure 3.45. Showing the signals Vref1, Vsig1 and the output Q from the sensing circuit

Averaging reduces the amount of thermal noise sampled on to the capacitors by $\sqrt{\frac{1}{N}}$ times as indicated by Equation 3.11 [2].

$$V_{noise,\,RMS} = \sqrt{\frac{k \cdot T}{NC}} \qquad (3.13)$$

From the equation it can be seen that increasing the number of clock cycles decreases the amount of thermal noise sampled on to the capacitor and hence we get a better sense and

an improvement in the signal to noise ratio by averaging for more number of clock cycles.

CHAPTER 4: SIMULATION RESULTS, LAYOUT OF THE ADC

Showing the Output of the DSM sensing circuit

Figures 4.1, 4.2, 4.3, 4.4 shows the simulation results for the DSM circuit assuming that the counter is enabled from 0.5μs (to allow for start up and S/H operation) sense time is 1μs.

For Vref =3.2V, N=100, $V_{ref,shift}=V_{ref}-V_{thn}=3.2-0.67=2.53V$ (Hand Calculations),

a) For Vsig=3.1V, $V_{sig,shift}==V_{sig}-V_{thn}=3.1-0.67=2.43V$

From simulations, the output goes high 3 times hence M=3, (Figure 4.1) and the value of

$$V_{sig,shift}=\frac{N-M}{N}\cdot V_{ref,shift}=\frac{97}{100}\cdot 2.53=2.45V \text{ (Calculated from simulations)}$$

b) For Vsig=2.15V, $V_{sig,shift}=2.15-0.67=1.48V$ (Hand Calculations),

From simulations Output goes high 44 times hence M=44, (Figure 4.2) and the value of

$$V_{sig,shift}=2.53\cdot\frac{100-44}{100}=1.42V \text{ (Calculated from simulations)}$$

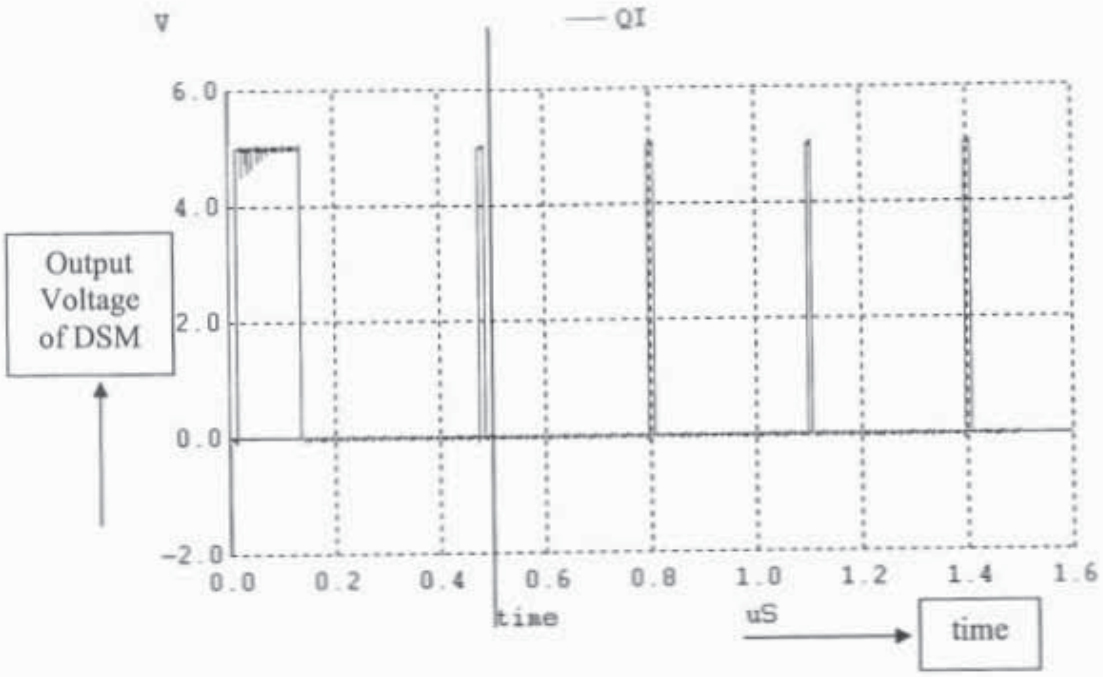

Figure 4.1. Showing the Output of the DSM sensing circuit of figure 3.44

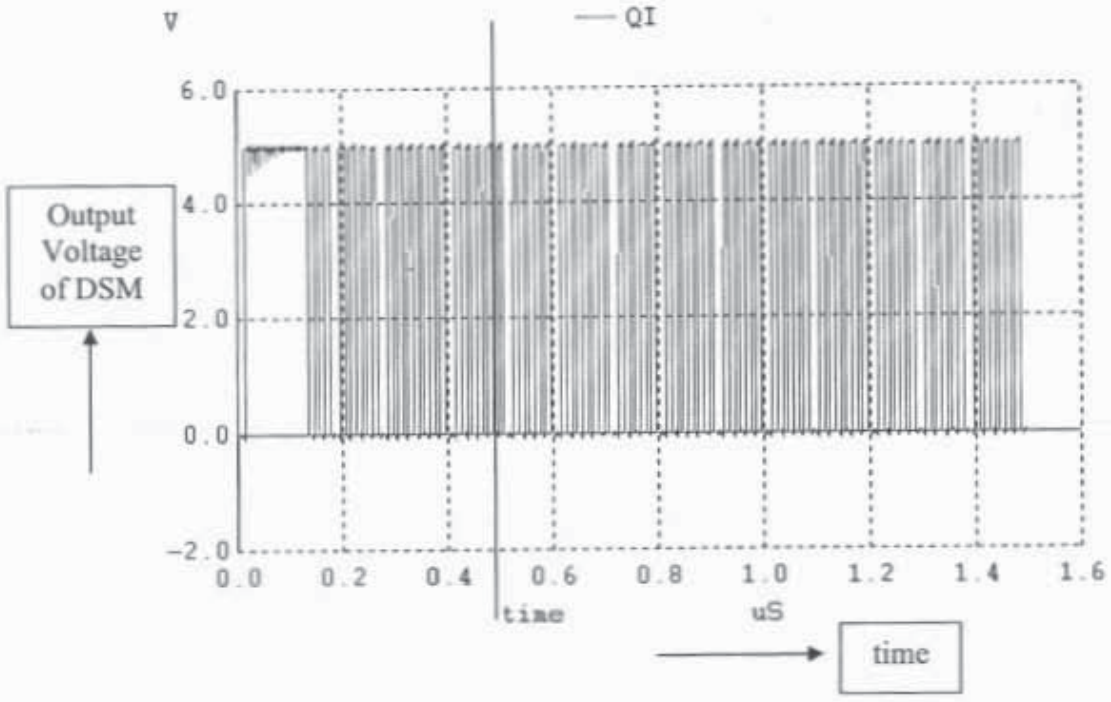

Figure 4.2. Output of the DSM sensing circuit of figure 3.44

c) For Vsig=1.6V, V_{sig_shift}=1.6–0.67=0.93V (Hand Calculations),

Output goes high 67 times hence M=67 (Figure 4.3), and the value of

$$V_{sig\_shift}=1.73\cdot\frac{100-67}{100}=0.83V \text{ (Calculated from simulations)}$$

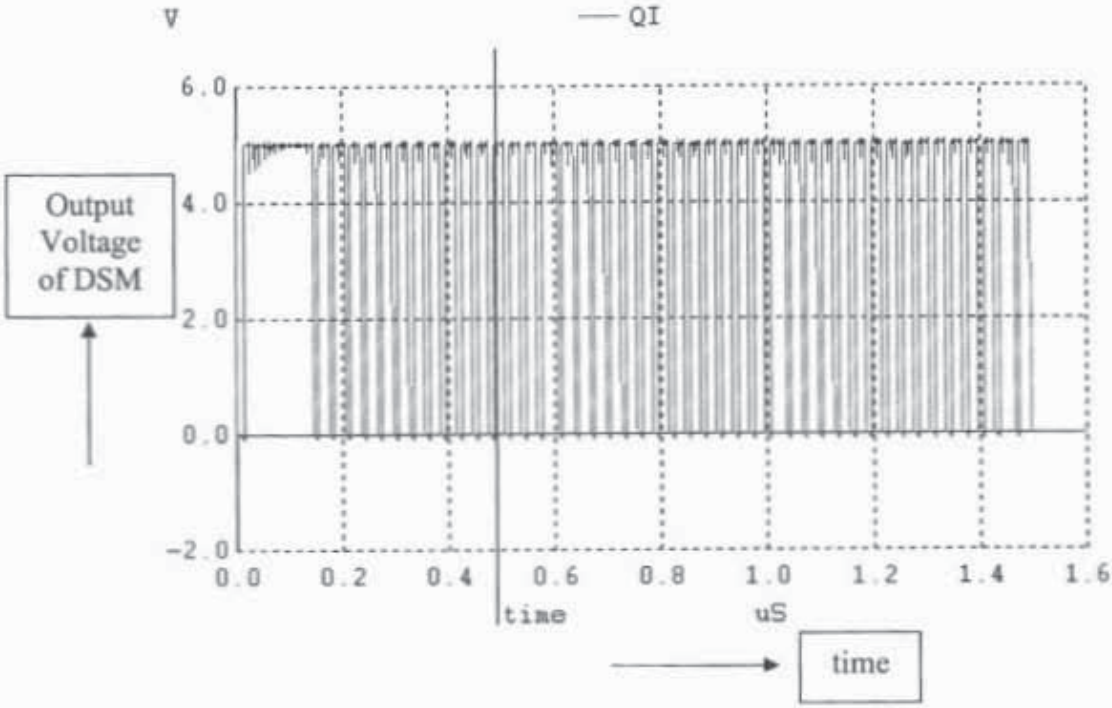

Figure 4.3. Output of the DSM sensing circuit of figure 3.44

d) For Vsig=0.8V, $V_{sig,shift}=0.8-0.67=0.13V$ (Hand Calculations),

Output goes high 96 times hence M=96, (Figure 4.4) and the value of

$$V_{sig,shift}=1.73\cdot\frac{4}{100}=0.10V \qquad \text{(Calculated from simulations)}$$

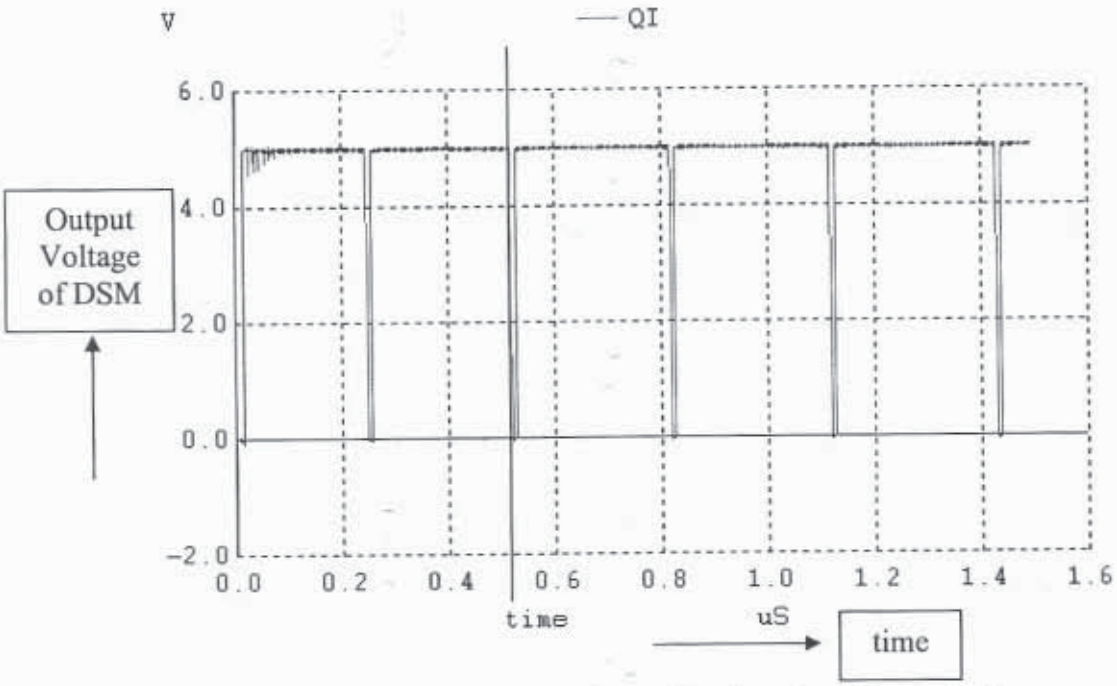

Figure 4.4. Output of the DSM sensing circuit of figure 3.44

Sensitivity to VDD and Ground Noise

The DSM ADC has been simulated with VDD noise of 100mV and ground noise of 50mV. Simulation results (Figure 4.5) show the count generated by the ADC for the signal voltages shown above in figures 4.1 (a), 4.2 (b), 4.3 (c), 4.4 (d). It can be seen that the count does not change (for Vref=3.2V, Vsig=3.1V, Count=3, Vsig=2.15V, Count=44, Vsig=1.6V, Count=67, Vsig=0.8V, Count=96) with variations in VDD and ground. The circuit is robust with VDD and ground noise due to its symmetric nature.

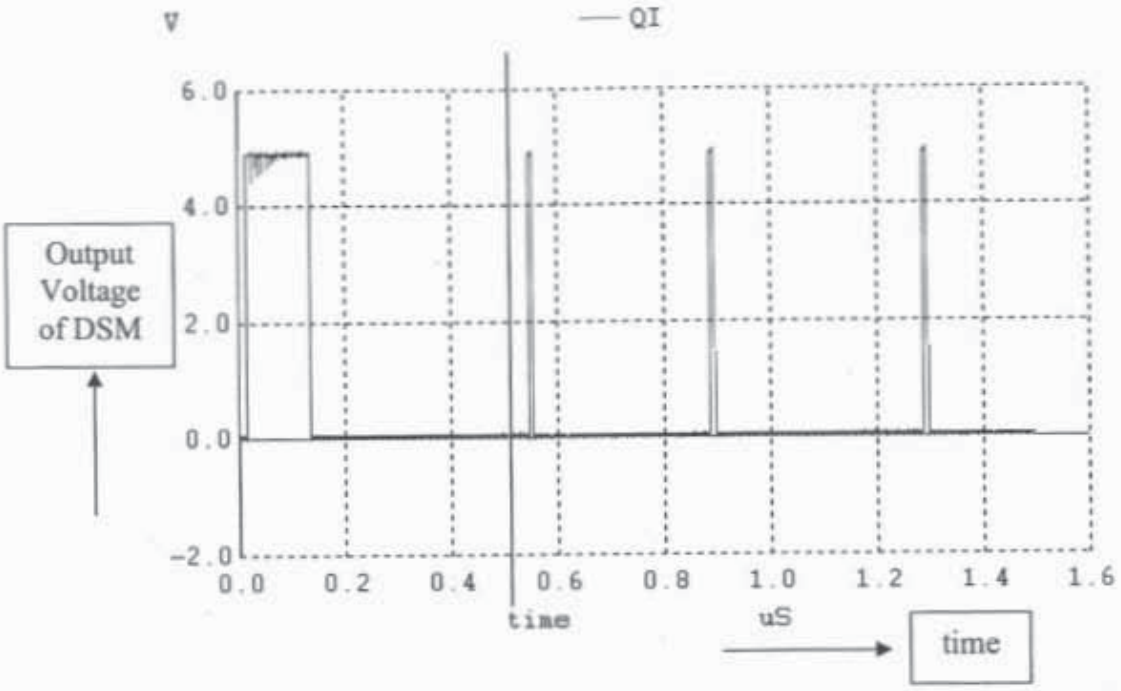

Figure 4.5. Output of the DSM with VDD and ground noise for Vsig=3.1V

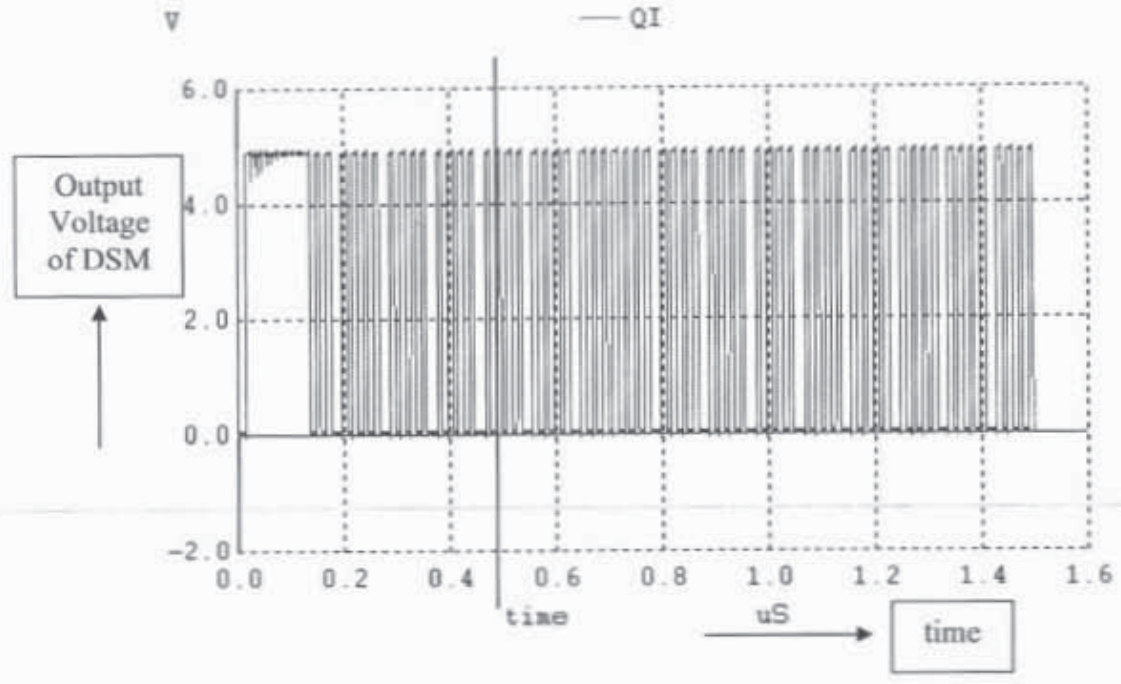

Figure 4.6. Output of the DSM with VDD and ground noise for Vsig=2.15V

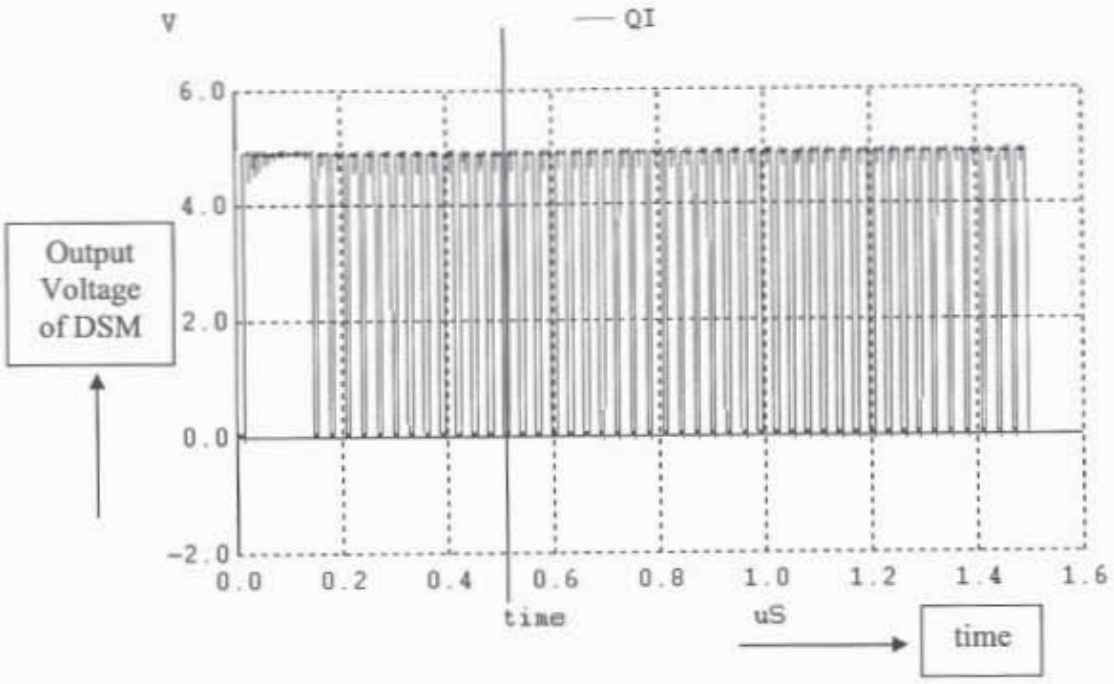

Figure 4.7. Output of the DSM with VDD and ground noise for Vsig=1.6V

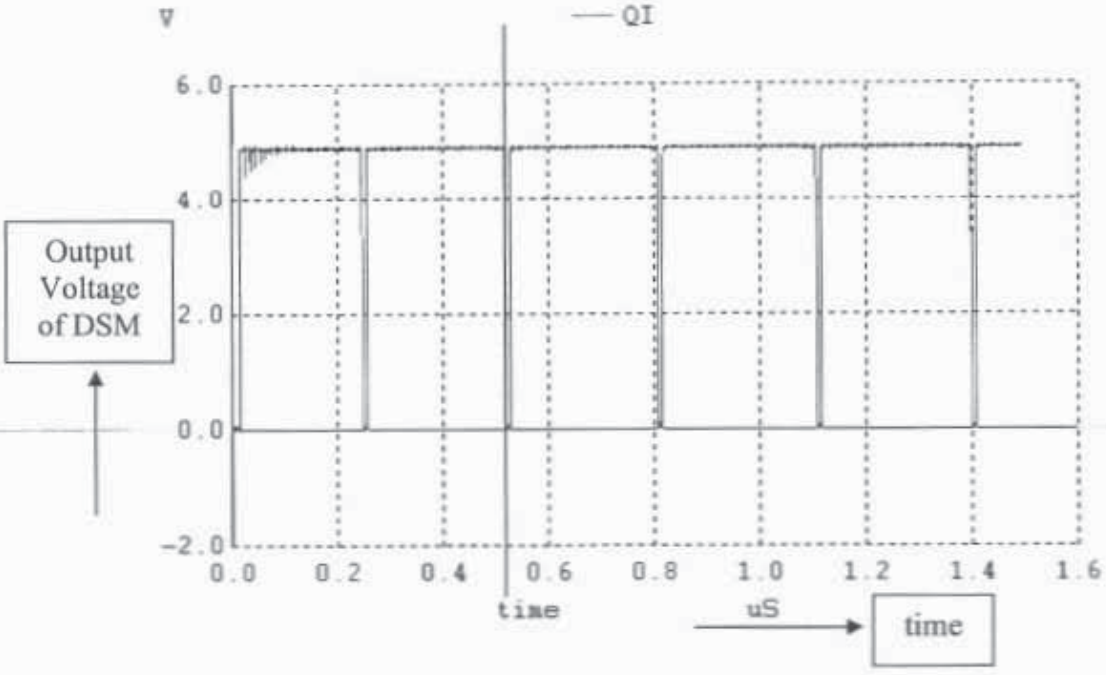

Figure 4.8. Output of the DSM with VDD and ground noise for Vsig=0.8V

Resolution of the DSM

The resolution of the DSM can be calculated by using the following equation:

$$V_{res} = \frac{V_{ref,shift}}{N} = \frac{1.73V}{100} = 17.3mV$$

As the input voltages drop from 2.4 V to 2.3 V the count difference is 7 (for a 100mV difference in the reference and desired signals) from 2.3 V to 2.2 V the code is 6, for 2.2 V to 2.1 V the code is 7, for 2.1 V to 2 V the count is 6. So the resolution can be estimated as

$$V_{res} = \frac{100mV}{6} = 16.6mV$$

So calculating the shifted reference voltage value with this resolution gives

$$V_{ref,shift} = \mathrm{N} \cdot V_{res} = 1.666V$$

$$V_{ref,shift} = V_{ref} - V_{thn}$$
$$V_{thn} = V_{ref} - V_{ref,shift} = 2.4 - 1.666 = 0.734V \text{ instead of } 0.67V$$

Calculating the shifted reference and intensity voltages with $V_{thn} = 0.734V$ gives

$a)\ V_{sig} = 2.3V, V_{sig,shift} = 2.3 - 0.734 = 1.566V\ (Calculated), V_{ref,shift} = 1.666V,$

$$V_{sig,shift} = 1.666 \cdot \frac{93}{100} = 1.549V\ (Sensed\ value)$$

$b)\ V_{sig} = 2.2V, V_{sig,shift} = 2.2 - 0.734 = 1.466V\ (Calculated), V_{ref,shift} = 1.666V,$

$$V_{sig,shift} = 1.666 \cdot \frac{87}{100} = 1.449V\ (Sensed\ value)$$

$c)\ V_{sig} = 2.1V, V_{sig,shift} = 2.1 - 0.734 = 1.366V\ (Calculated), V_{ref,shift} = 1.666V,$

$$V_{sig,shift} = 1.666 \cdot \frac{80}{100} = 1.332V\ (Sensed\ value)$$

$d)\ V_{sig} = 2V, V_{sig,shift} = 2 - 0.734 = 1.266V\ (Calculated), V_{ref,shift} = 1.666V,$

$$V_{sig,shift} = 1.666 \cdot \frac{74}{100} = 1.232V\ (Sensed\ value)$$

Table 4.1 shows the values for the Calculated and Simulated signals for a reference voltage of Vref=3V. The shifted reference voltage $V_{ref,shift} = V_{ref} - V_{thn} = 3 - 0.67 = 2.33V$

Table 4.1. Calculated and Simulated signals for constant reference voltage and different signal voltages

Difference between Reference and Desired signals	*Desired Signal*	*Count*	*Shifted Desired signal HAND CALCS* V_{thn}=0.67	*Shifted Desired signal SIMS*	*Shifted Desired signal HAND CALCS* V_{thn}=0.73	*Shifted Desired signal SIMS*
0.05	2.95	4	2.28	2.24	2.21	2.17
0.1	2.9	6	2.23	2.19	2.16	2.13
0.15	2.85	7	2.18	2.17	2.11	2.10
0.2	2.8	9	2.13	2.12	2.06	2.06
0.25	2.75	11	2.08	2.07	2.01	2.01
0.3	2.7	13	2.03	2.03	1.96	1.97
0.35	2.65	17	1.98	1.93	1.91	1.88
0.4	2.6	19	1.93	1.89	1.86	1.83
0.45	2.55	21	1.88	1.84	1.81	1.79
0.5	2.5	24	1.83	1.77	1.76	1.72
0.55	2.45	26	1.78	1.72	1.71	1.67
0.6	2.4	28	1.73	1.68	1.66	1.63
0.65	2.35	30	1.68	1.63	1.61	1.58
0.7	2.3	33	1.63	1.56	1.56	1.51
0.75	2.25	36	1.58	1.49	1.51	1.45
0.8	2.2	38	1.53	1.44	1.46	1.4
0.85	2.15	40	1.48	1.40	1.41	1.35
0.9	2.1	42	1.43	1.35	1.36	1.31
0.95	2.05	44	1.38	1.30	1.31	1.26
1	2.0	47	1.33	1.23	1.26	1.2
1.05	1.95	49	1.28	1.89	1.21	1.15
1.1	1.9	46	1.23	1.26	1.16	1.22
1.15	1.85	54	1.17	1.25	1.11	1.22
1.2	1.8	56	1.12	1.02	1.06	0.99
1.25	1.75	58	1.07	0.97	1.01	0.95
1.3	1.7	59	1.02	0.95	0.96	0.92
1.35	1.65	62	0.97	0.88	0.91	0.86
1.4	1.6	64	0.92	0.83	0.86	0.81
1.45	1.55	66	0.87	0.79	0.81	0.77
1.5	1.5	68	0.82	0.74	0.76	0.72
1.55	1.45	70	0.77	0.69	0.71	0.67

Difference between Reference and Desired signals (cont'd)	*Desired Signal (cont'd)*	*Count (cont'd)*	*Shifted Desired signal HAND CALCS(cont'd)* V_{thn}=0.67	*Shifted Desired signal SIMS (cont'd)*	*Shifted Desired signal HAND CALCS (cont'd)* V_{thn}=0.73	*Shifted Desired signal SIMS (cont'd)*
1.6	1.4	73	0.72	0.62	0.66	0.61
1.65	1.35	75	0.67	0.58	0.61	0.56
1.7	1.3	77	0.62	0.53	0.56	0.52
1.75	1.25	75	0.57	0.58	0.51	0.56
1.8	1.2	81	0.52	0.44	0.46	0.43
1.85	1.15	83	0.47	0.39	0.41	0.38
1.9	1.1	85	0.42	0.34	0.36	0.33
1.95	1.05	87	0.37	0.3	0.31	0.29
2	1	88	0.32	0.27	0.26	0.27
2.05	0.95	91	0.27	0.2	0.21	0.2
2.1	0.9	93	0.22	0.16	0.16	0.15
2.15	0.85	95	0.17	0.11	0.11	0.11
2.2	0.8	96	0.12	0.09	0.06	0.09
2.25	0.75	97	0.07	0.06	0.01	0.06
2.3	0.7	98	0.02	0.04	-0.03	0.04

Table 4.1. (continued)

Showing the Count generated by the sensing circuit

The DSM ADC (figure 3.44) has been simulated (figures) for different reference and signal voltages. The count generated by the sensing circuit has been shown in figures 4.9, 4.12, and 4.13. Here the desired intensity voltages have been varied for different reference voltages and count generated by the DSM has been plotted. The desired signal voltages (output) calculated from the count generated by the DSM and Hand Calcs has been plotted for different input voltages (figures 4.10, 4.11 4.7, 4.14-4.20)

We can see from the figure 4.9 that as the voltage difference between the reference and the intensity signal increases the count also increases linearly.

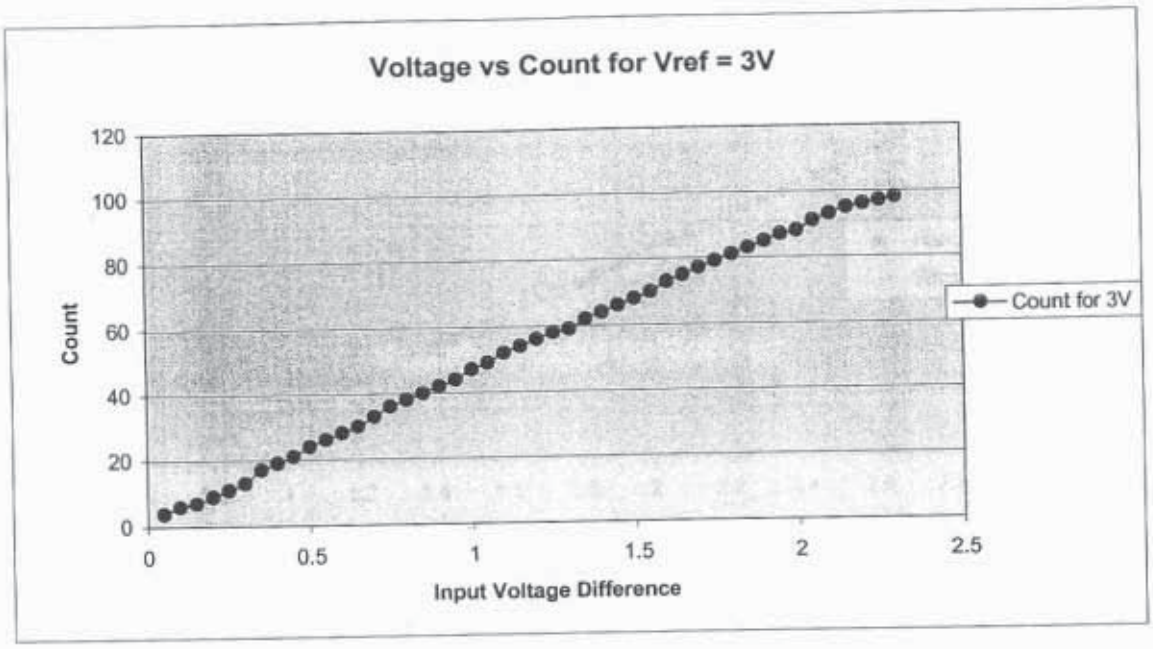

Figure 4.9. Showing the Count generated by the sensing circuit of figure 3.44

Comparison of voltages hand calcs and sims generated by the sensing circuit

A graph showing a comparison of the calculated and simulated values of the output voltages for both the threshold voltages (Vthn=0.67V, 0.73V) are shown in figure 4.10, 4.11. It can be seen that the voltages generated with the calculated threshold voltage of 0.73V (figure 4.11) are more close to the hand calculations.

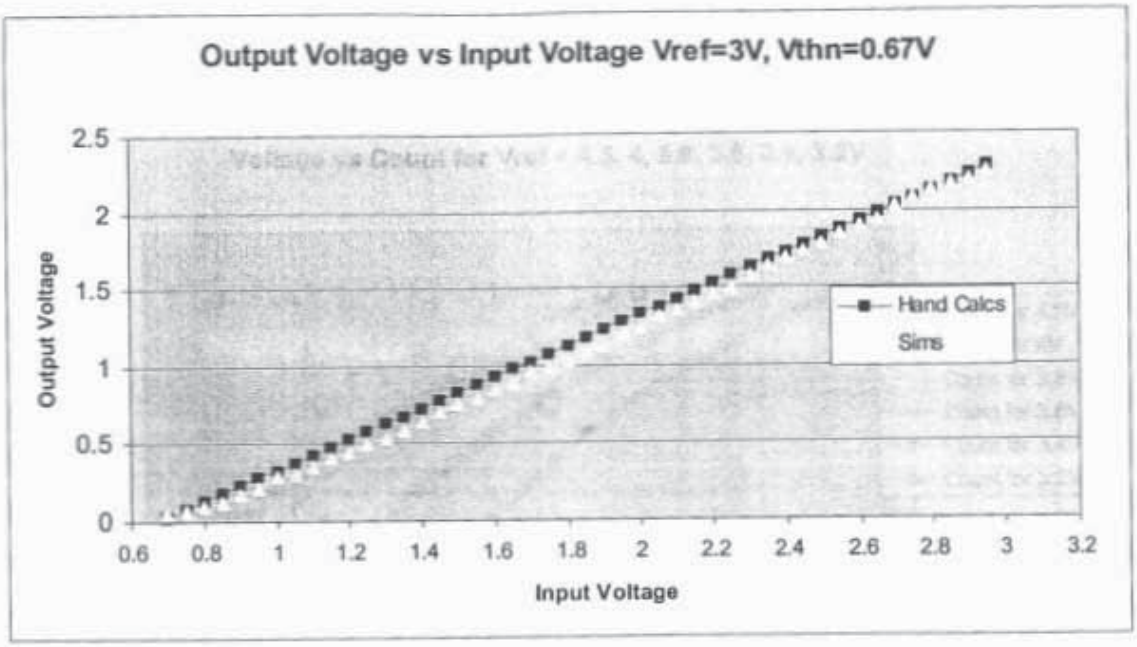

Figure 4.10. Comparison of voltages hand calcs and sims generated by the sensing circuit of figure 3.44

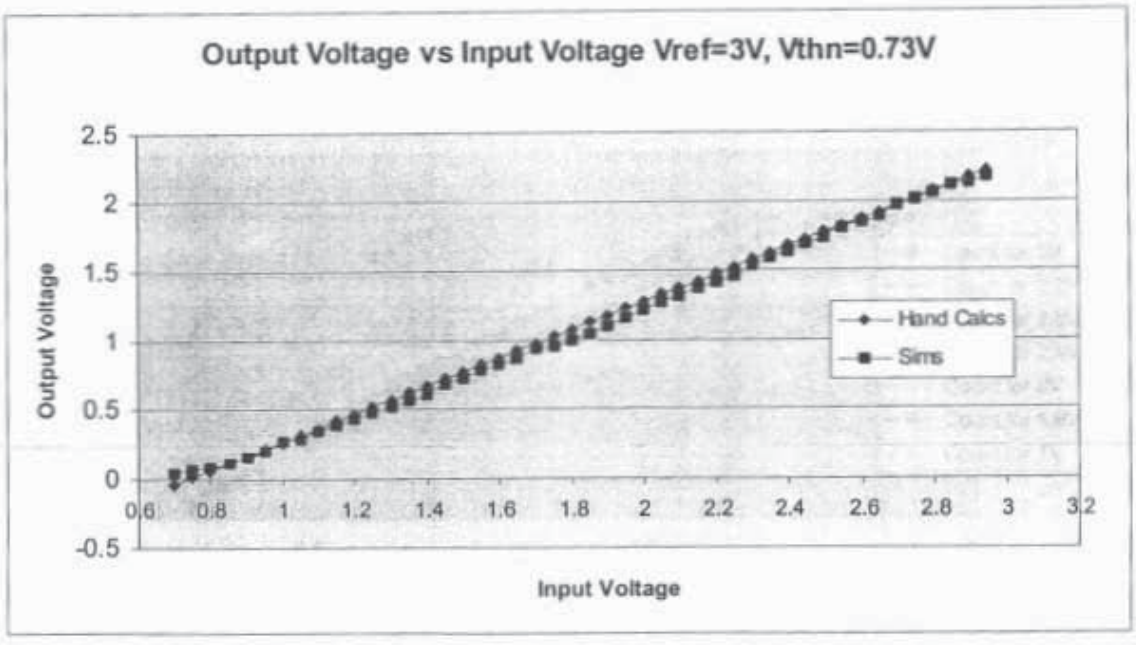

Figure 4.11. Comparison of voltages hand calcs and sims generated by the sensing circuit of figure 3.44

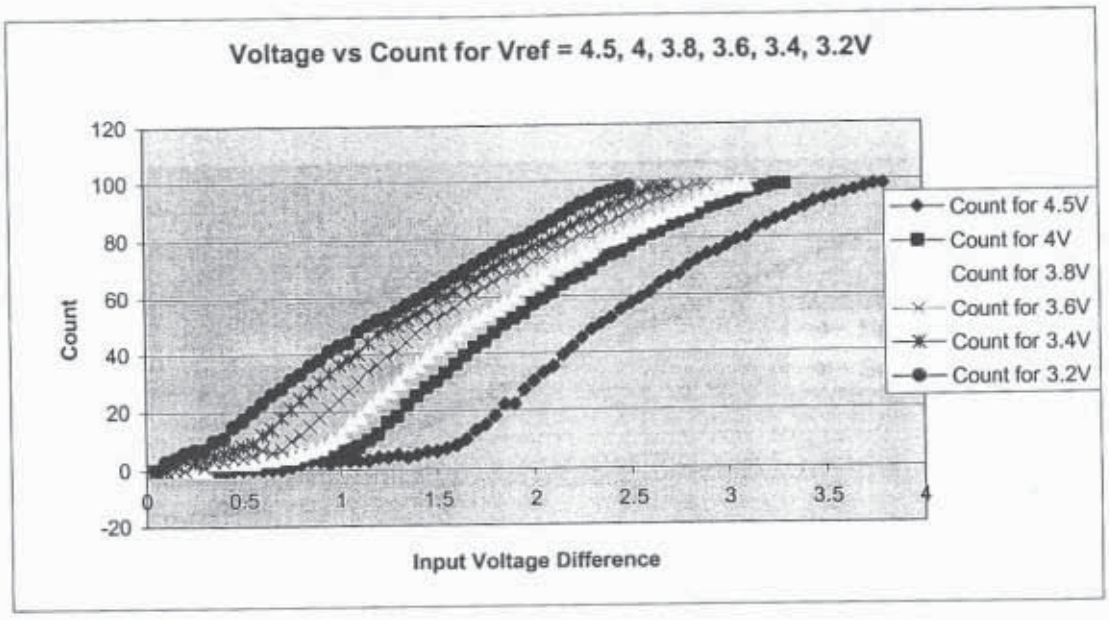

Figure 4.12. Showing the Count generated by the DSM of figure 3.44 for different reference voltages

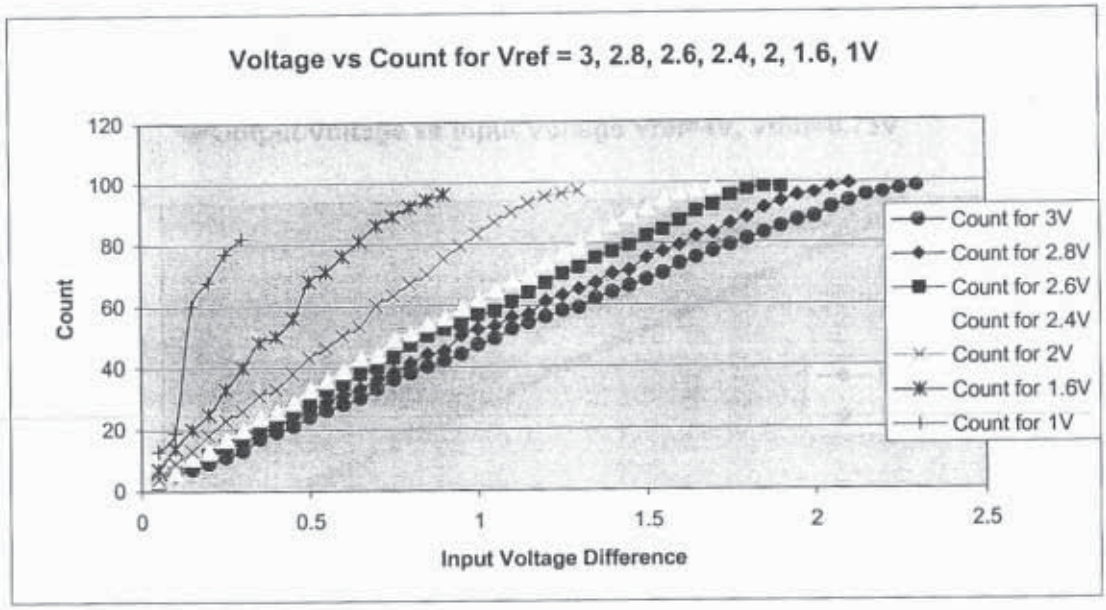

Figure 4.13. Showing the Count generated by the DSM of figure 3.44 for different reference voltages

Figures 4.14-4.20 shows a comparison of the calculated and simulated values of the output desired signal voltages for different reference voltages.

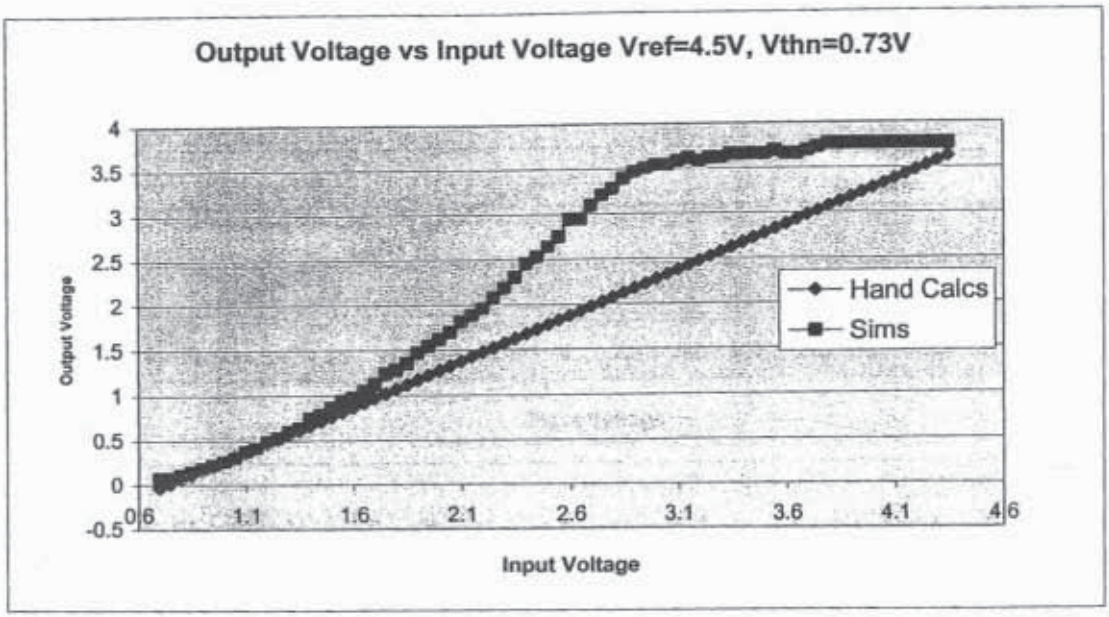

Figure 4.14. Comparison of voltages hand calcs and sims generated by the sensing circuit of figure 3.44

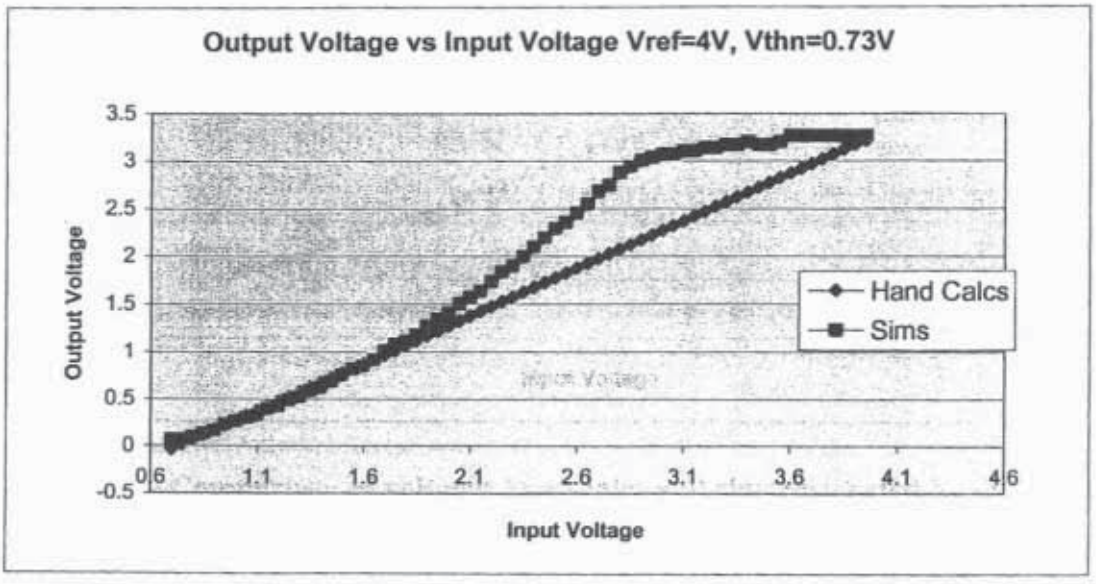

Figure 4.15. Comparison of voltages hand calcs and sims generated by the sensing circuit of figure 3.44

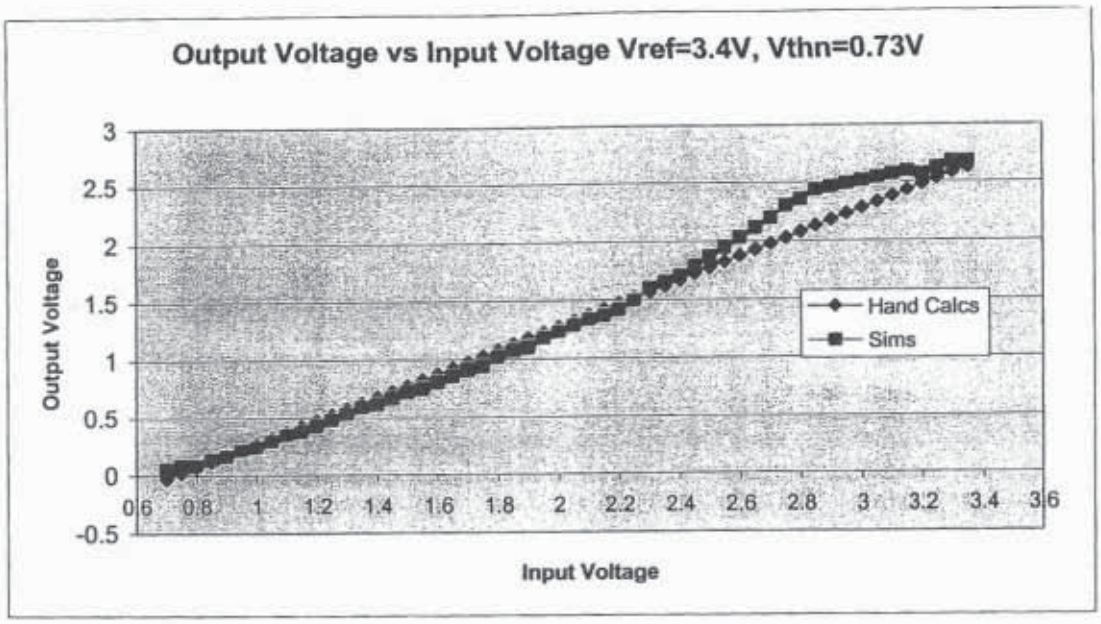

Figure 4.16. Comparison of voltages hand calcs and sims generated by the sensing circuit of figure 3.44

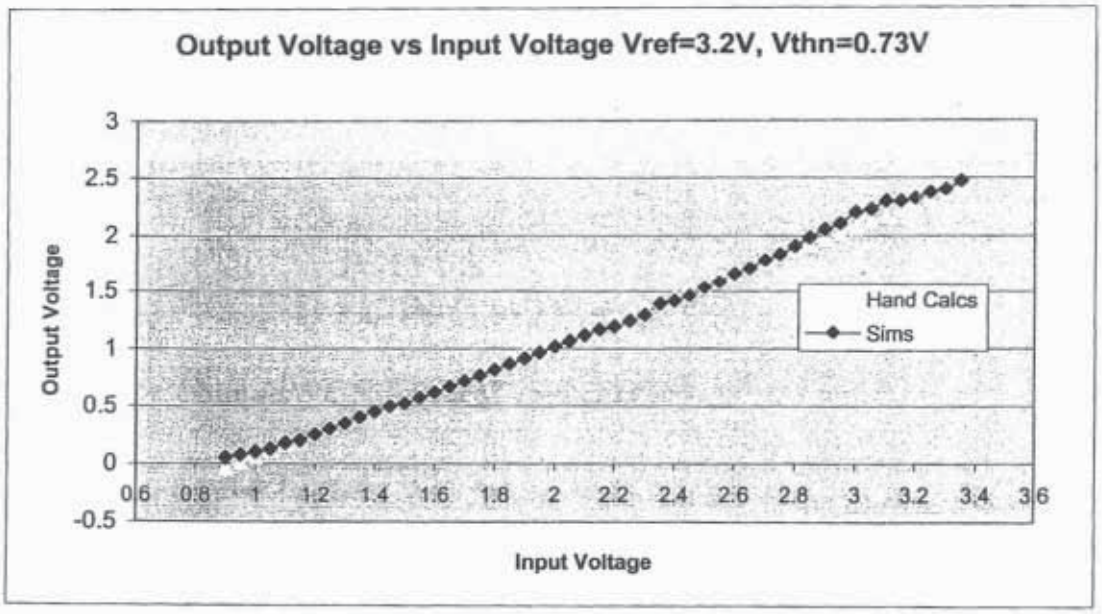

Figure 4.17. Comparison of voltages hand calcs and sims generated by the sensing circuit of figure 3.44

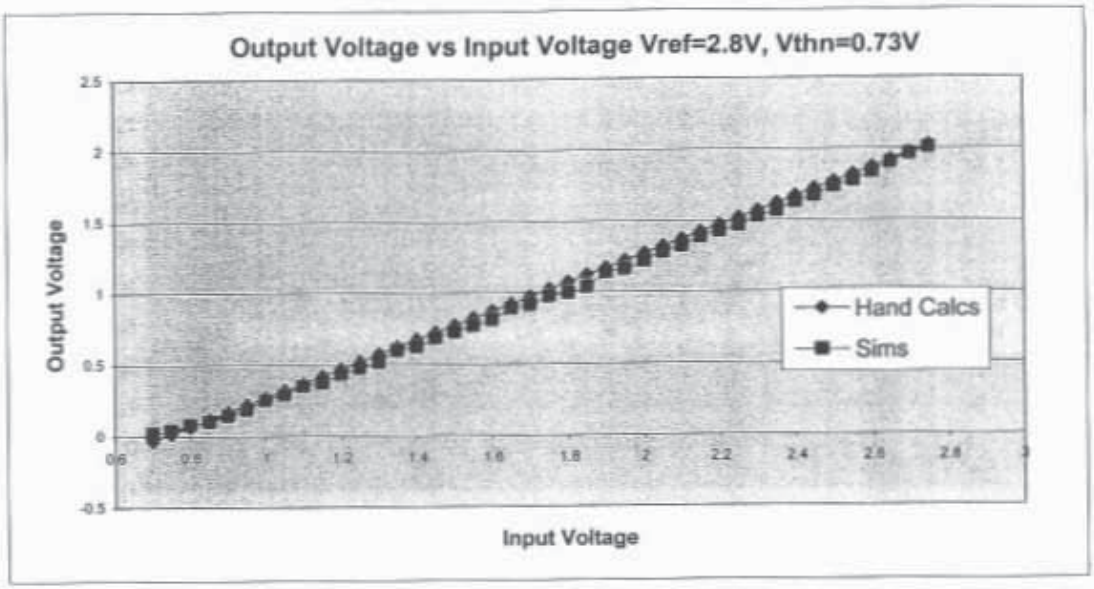

Figure 4.18. Comparison of voltages hand calcs and sims generated by the sensing circuit of figure 3.44

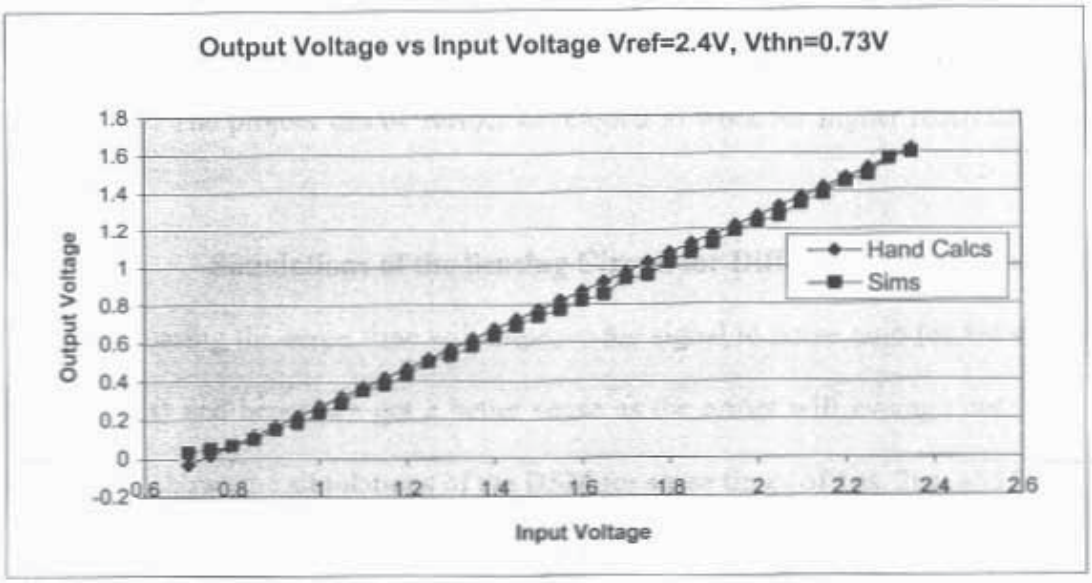

Figure 4.19. Comparison of voltages hand calcs and sims generated by the sensing circuit of figure 3.44

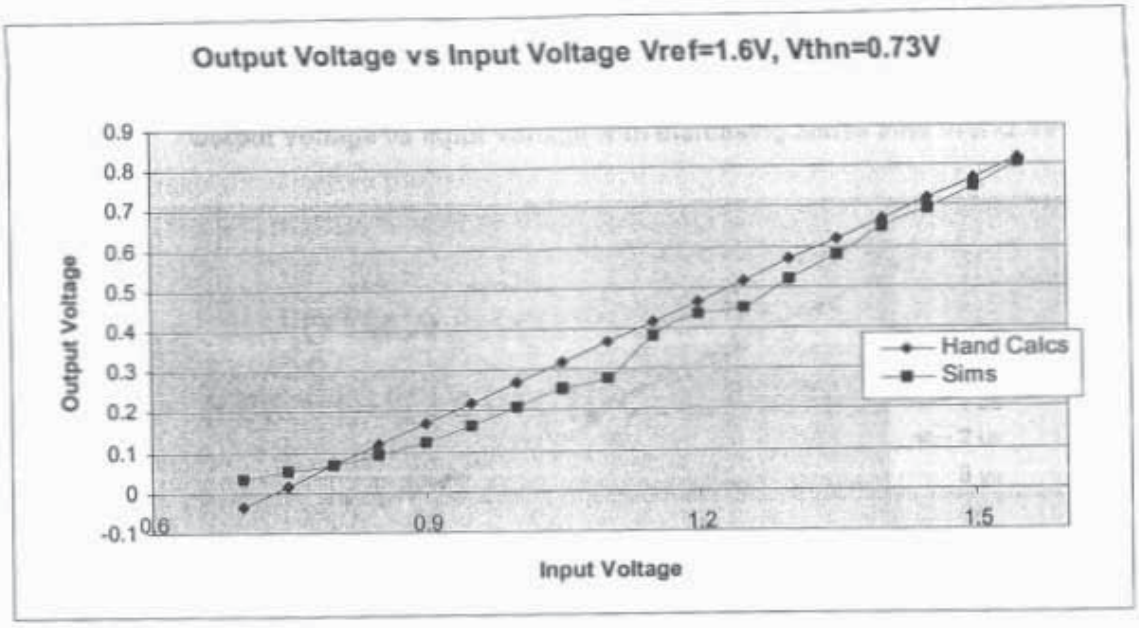

Figure 4.20. Comparison of voltages hand calcs and sims generated by the sensing circuit of figure 3.44

For reference voltages above 4.5V the comparator shuts off and we get a large non-linearity in the sense. Below 0.7V the NMOS input amplifiers shut off giving nonlinearity. The project can be further developed to work for higher reference voltages above 3.4V.

Simulations of the Sensing Circuit for Different Sense Times

Increasing the sense time will improve the signal to noise ratio (as we sample for longer times) and hence we get a better sense as the errors will average out with time. Figure 4.21 shows the simulations of the DSM for sense times of 1us, 2us, and 3us.

Simulations of the Sensing Circuit at Higher Frequencies

Figure 4.22 shows the simulations of the DSM at higher clock frequencies of 166MHz and 250MHz. The sense time is 1us then the number of samples increases to 166, 250 and the sense values get better by sampling for a longer time.

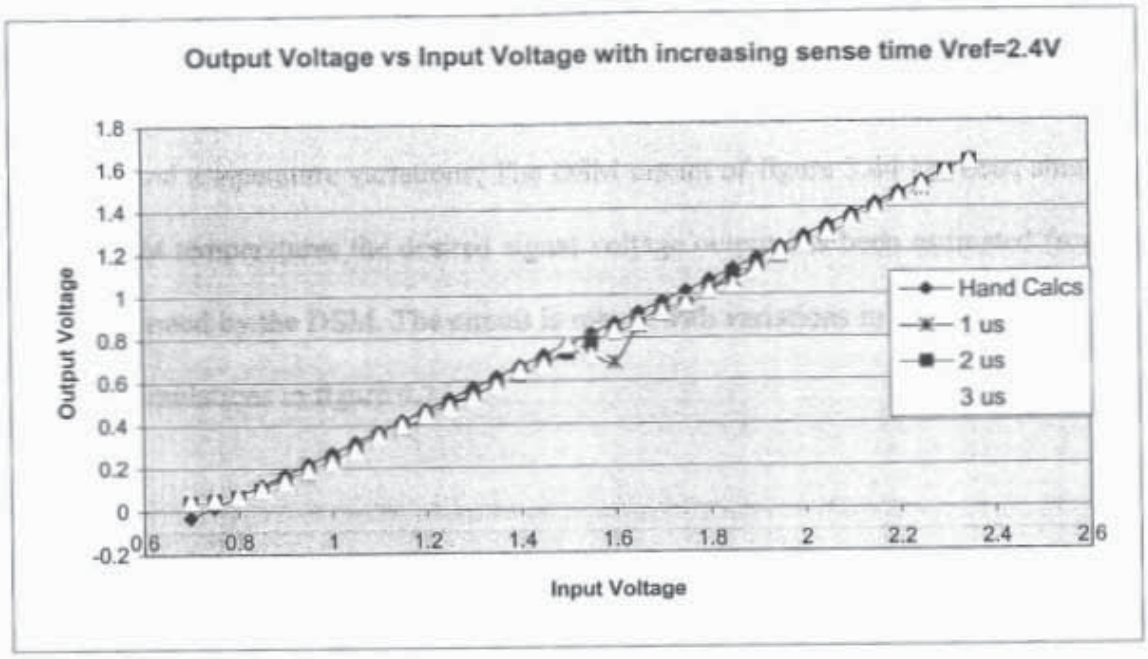

Figure 4.21. Simulations of the sensing circuit of figure 3.44 for different sense times

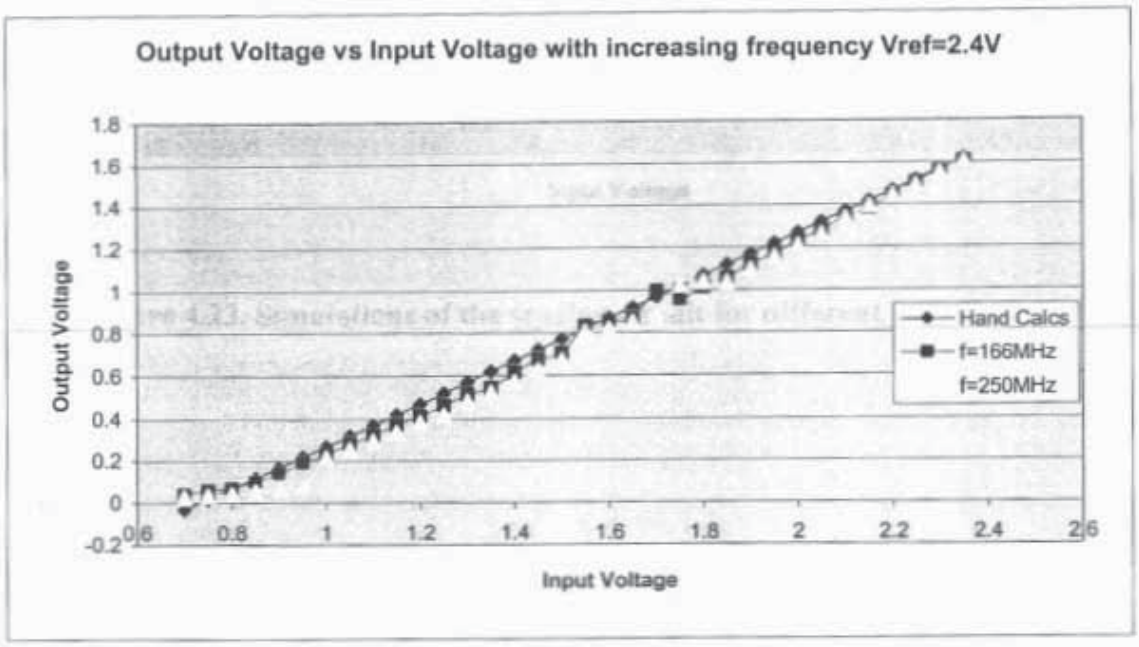

Figure 4.22. Simulations of the DSM of figure 3.44 at higher clock frequencies

Temperature Sensitivity of the Sensing Circuit

The circuit has two branches that are symmetrical which will affect the outputs similarly for VDD and temperature variations, The DSM circuit of figure 3.44 has been simulated for different temperatures the desired signal voltage output has been estimated from the count generated by the DSM. The circuit is robust with variations in temperatures as seen from the simulations in figure 4.23.

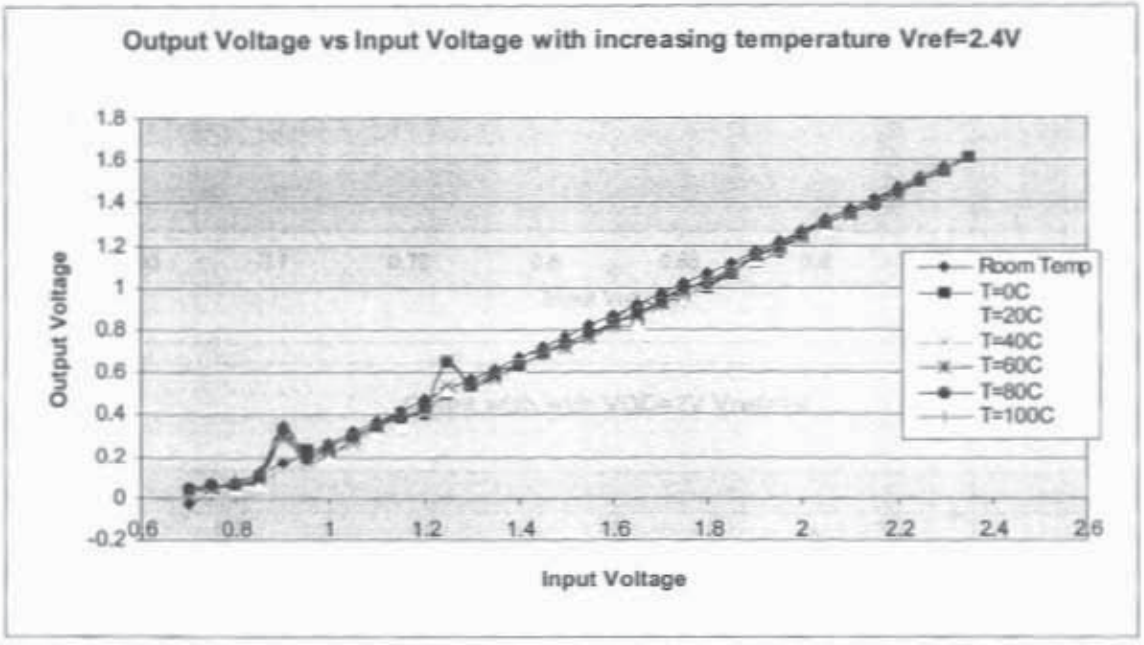

Figure 4.23. Simulations of the sensing circuit for different temperatures

Simulations of the Sensing Circuit at Lower VDD

Figure 4.24 shows the simulation results for a VDD of 2V for the 0.5um process. The design works for lower power supply voltages.

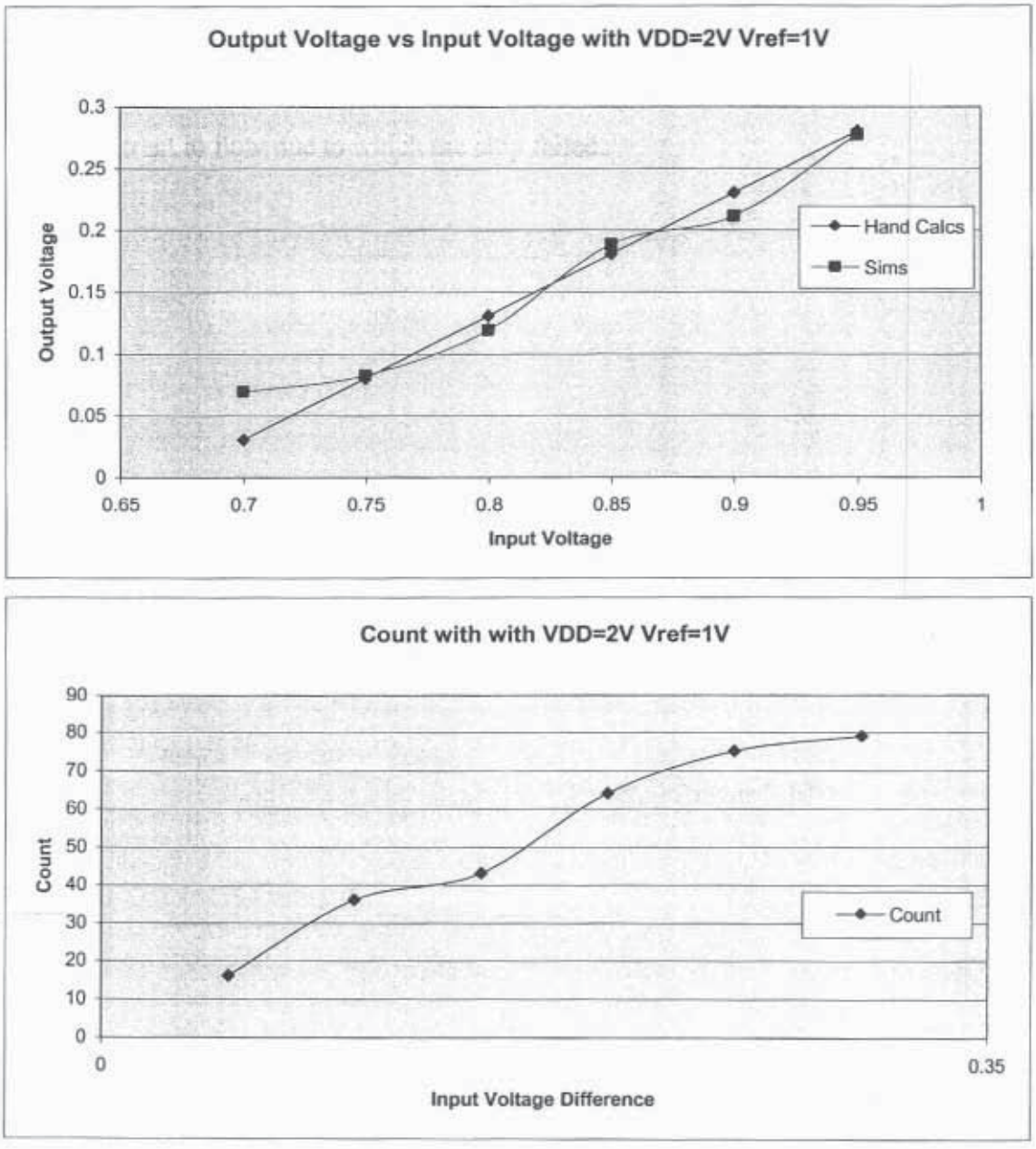

Figure 4.24. Simulations of the sensing circuit for lower VDD

Layout of the Delta Sigma ADC

The sensing circuit has been fabricated in a 0.5um process technology and several test structures of the nand gate, buffer, comparator and the input circuit have also been laid out and tested. Figure 4.25 shows the chip layout with the test structures of the circuit (figure 3.44). The ESD protection diodes in the pad frame are turning on causing huge leakage current to flow due to which the chip failed.

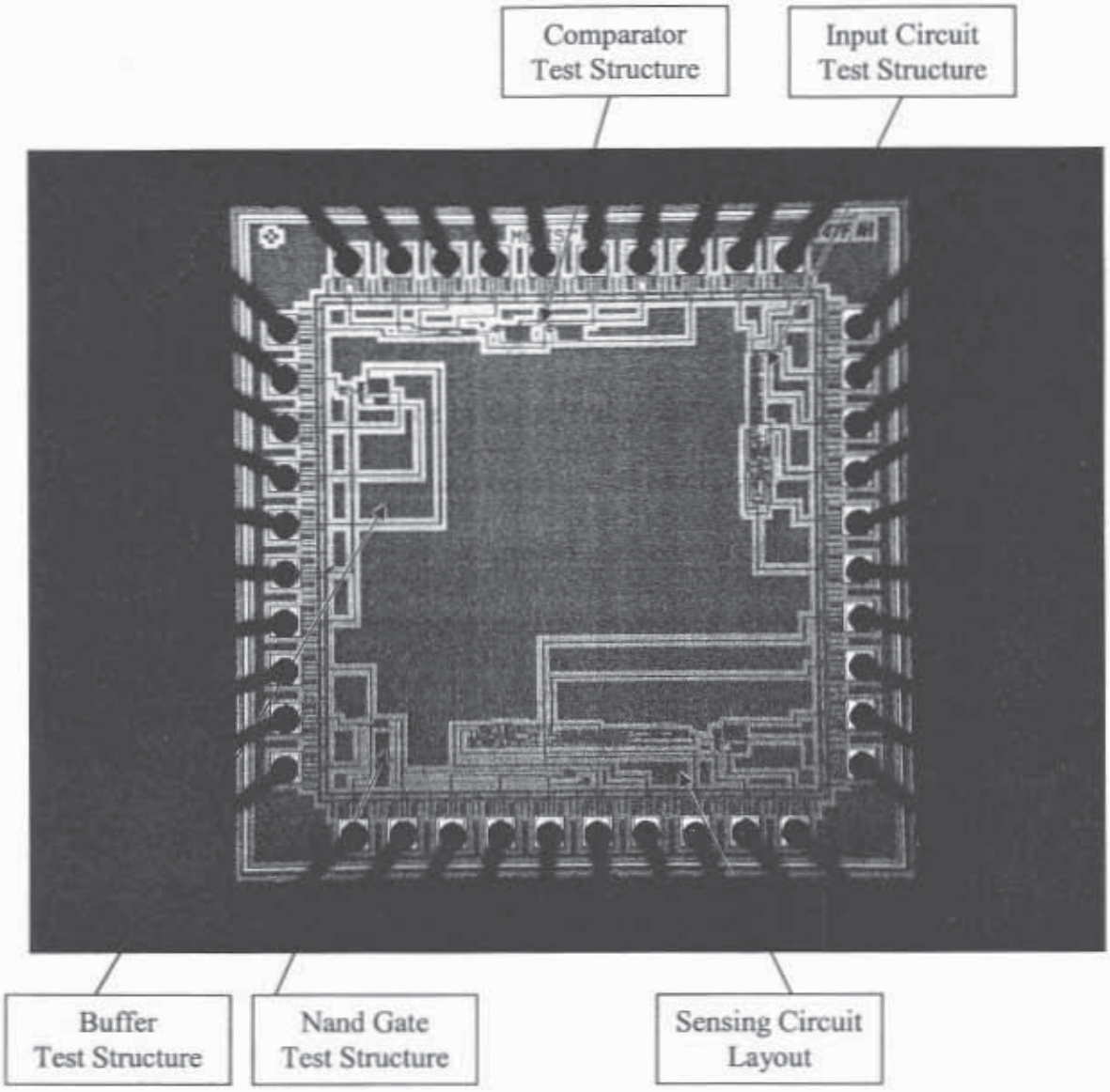

Figure 4.25: Chip Layout with the test structures of the Delta Sigma ADC

CHAPTER 5: CONCLUSIONS

A sigma delta ADC that uses averaging techniques has been designed to determine the column voltages from the CMOS pixel. A unique voltage to current converter technique for each pixel that keeps the pixel isolated from the sensing circuitry has been designed. The difference in the reference and signal currents is taken which makes the circuit robust with various process and threshold voltage variations. The circuit is symmetrical hence it is robust to ground noise or VDD noise. The ADC has a resolution of 20mV for a sense time of 1μs. Increasing the sense time increases the resolution. The output of the ADC is a digital signal from which we can determine the analog voltages coming from the pixel by counting the number of times the ADC output goes high. The digital output can be connected to a counter (which also acts as a low pass filter) that counts the number of times the ADC goes high. The voltages can then be determined from the counter's value. From the simulations it can be seen how different signal levels can be measured using the ADC. Since there are no resistors in the design the circuit is robust with process variations. Simulations show that design is robust with variations in temperatures and also works for lower supply voltages.

The project can further be developed to work for higher input voltage ranges and better linearities.

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