500MHz - 1.24GHz RF Low Noise Amplifier System Design, Simulation, and Layout
Cadence Virtuoso – TowerJazz SBC18 0.18um SiGe BiCMOS Process

By Shadden Abdalla

November 2019

Contents

Introduction:

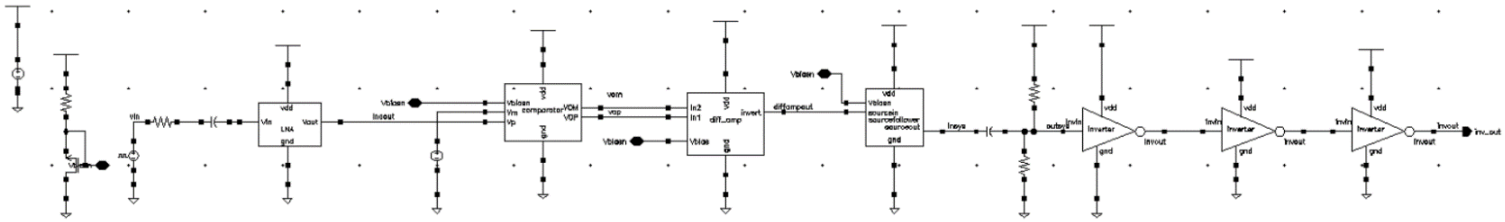
The following report details the design, simulation and layout of an RF Low Noise Amplifier and the stages that follow it. The system contains an RF Low Noise Amplifier, comparator, differential amplifier, source follower as a buffer, DC biasing system, three inverters and a biasing circuit. This system can take an input as low as 400uV and amplify the signal from rail to rail, from voltages of 0 to 3.3V. It is high speed and operates at a frequency of 500MHz.

Purpose:

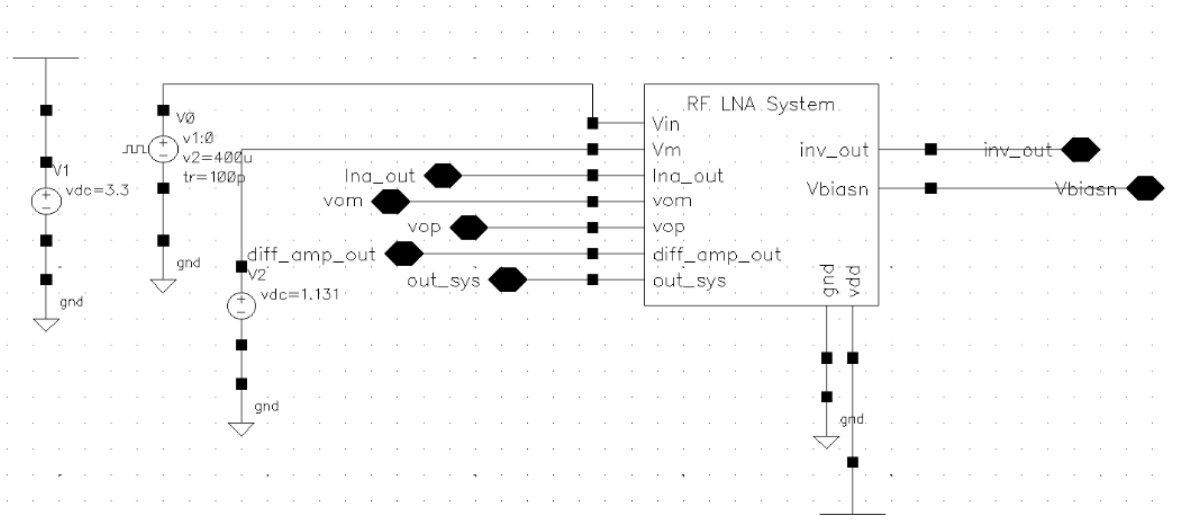
This circuit is the front-end circuit of a microchannel plate photomultiplier tube. The microchannel plate photomultiplier tube needs an input circuit that can take in a very small signal and amplify it, while also operating at a very high frequency, with a large bandwidth. The original idea for this circuit was a TIA, however, TIAs cannot output a large bandwidth. Instead, an RF Amplifier can give a large enough bandwidth that can be used for high speed LIDAR applications.

The following simulations show the operation of the circuit with an input of 0-400uV.

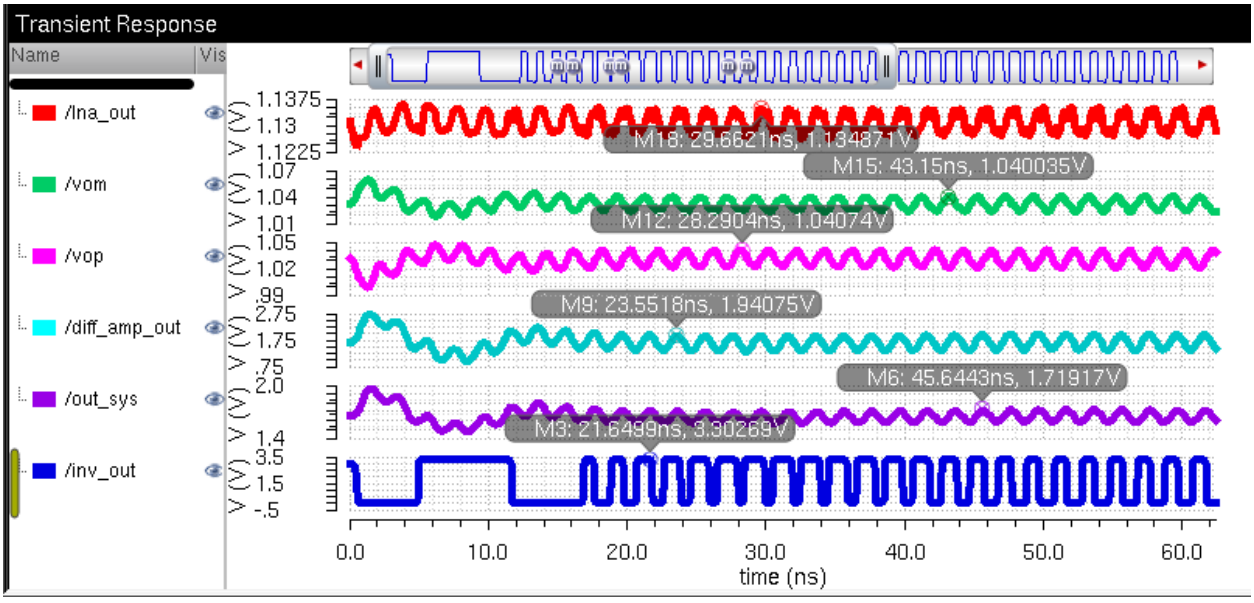
Entire System:



1: The circuit above is the entire system that makes up the amplifier.



2: The circuit above is the symbol for the entire circuit and the inputs used for testing.



3. The simulations correspond to the schematic above.

The entire system contains six stages. The components available from left to right are the LNA, comparator, differential amplifier, source follower, DC bias system, and three inverters.

OUTPUT TABLE FOR THE CIRCUIT WITH AN INPUT OF 400uV

Input Pulse Voltage (V)	LNA Output (V)	VOP (V)	VOM (V)	Differential Amplifier Output (V)	Source Follower Output (V)	DC Biasing Output (V)	Final Inverter's Output (V)
400u	1.137	1.0370	1.036	1.9500	367.17m	1.74	3.2998
800u	1.14	1.0500	1.045	2.3370	495.71m	1.87	3.2996
1m	1.142	1.0580	1.050	2.5100	566.44m	1.95	3.2996
100m	1.921	2.2810	1.3789	3.3100	990.21m	2.06	3.2997
500m	2.284	2.5514	1.4006	3.2970	976.29m	2.06	3.2998
1	2.324	2.6005	1.4198	3.3274	982.15m	2.07	3.2998
1.8	2.5212	2.6450	1.4218	3.2989	982.026	2.05	3.3001

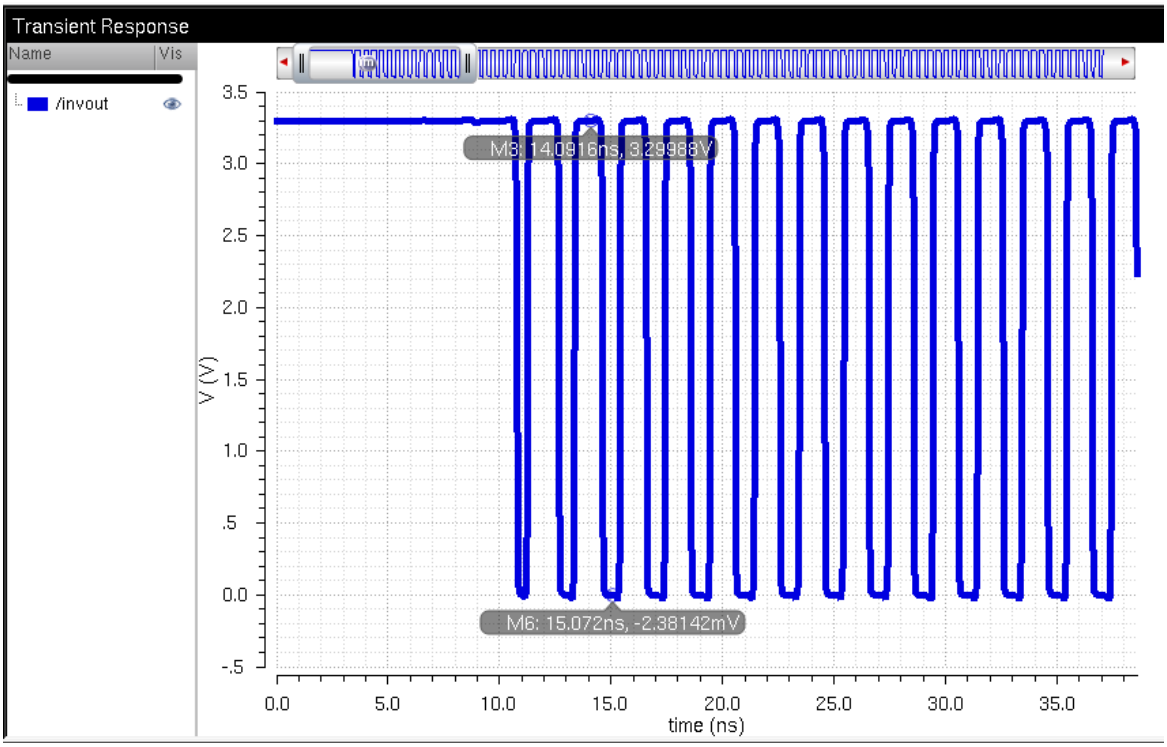
AC OUTPUTS WITH PROCESS CORNER SIMULATIONS

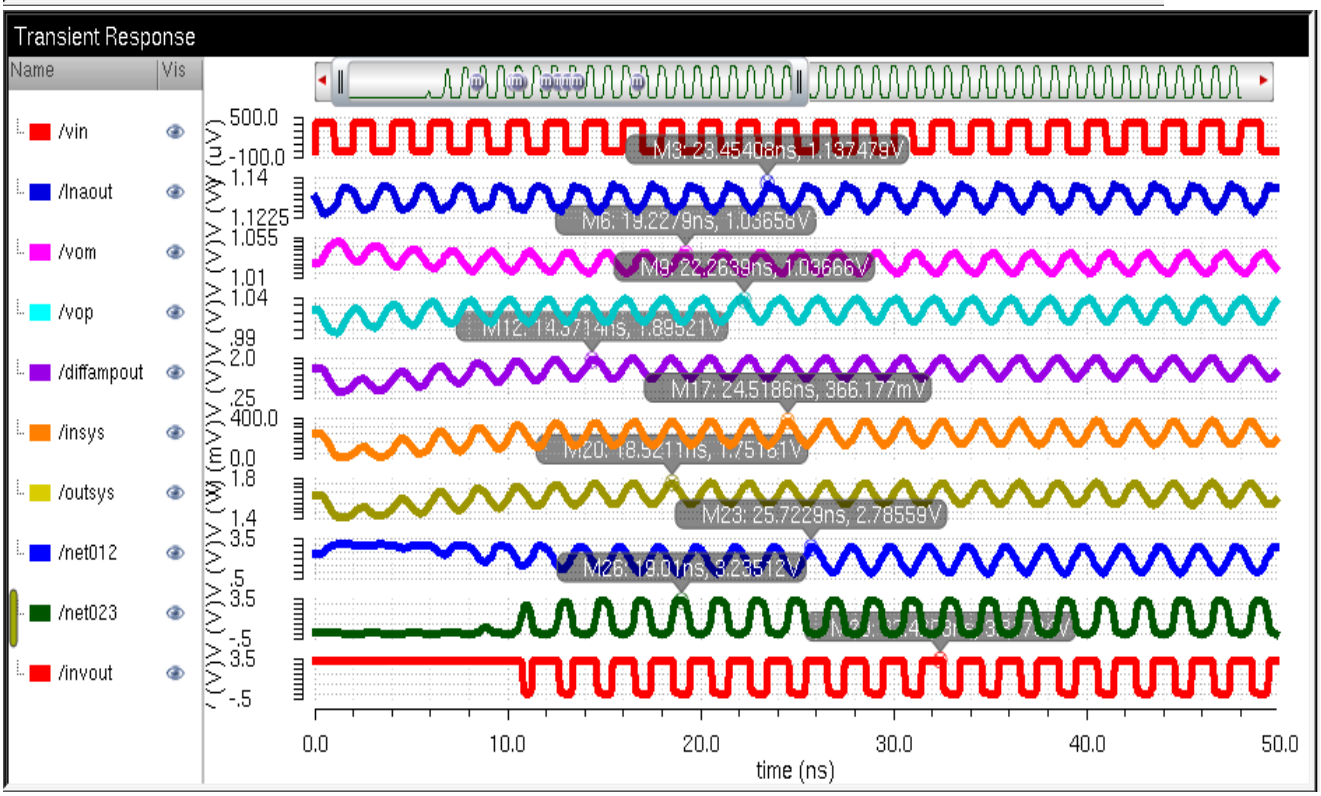
Sim #		npn	n3p3_5p0	p3p3_5p0	AC gain (dB)	Phase Margin (degrees)
1	Process Corner	Fast	Fast	Fast	26.670	86
2	Process Corner	Slow	Slow	Slow	26.670	88
3	Process Corner	Fast	Slow	Fast	26.680	87
4	Process Corner	Fast	Slow	Slow	26.602	88
5	Process Corner	Slow	Fast	Slow	23.301	83
6	Process Corner	Slow	Slow	Fast	23.301	83

Final Output of the Circuit With a 400uV Input

Below is the output of the final inverter for a simulation with an input of 400uV. The simulation shows that the output swings from rail to rail, from 0V to 3.3V.

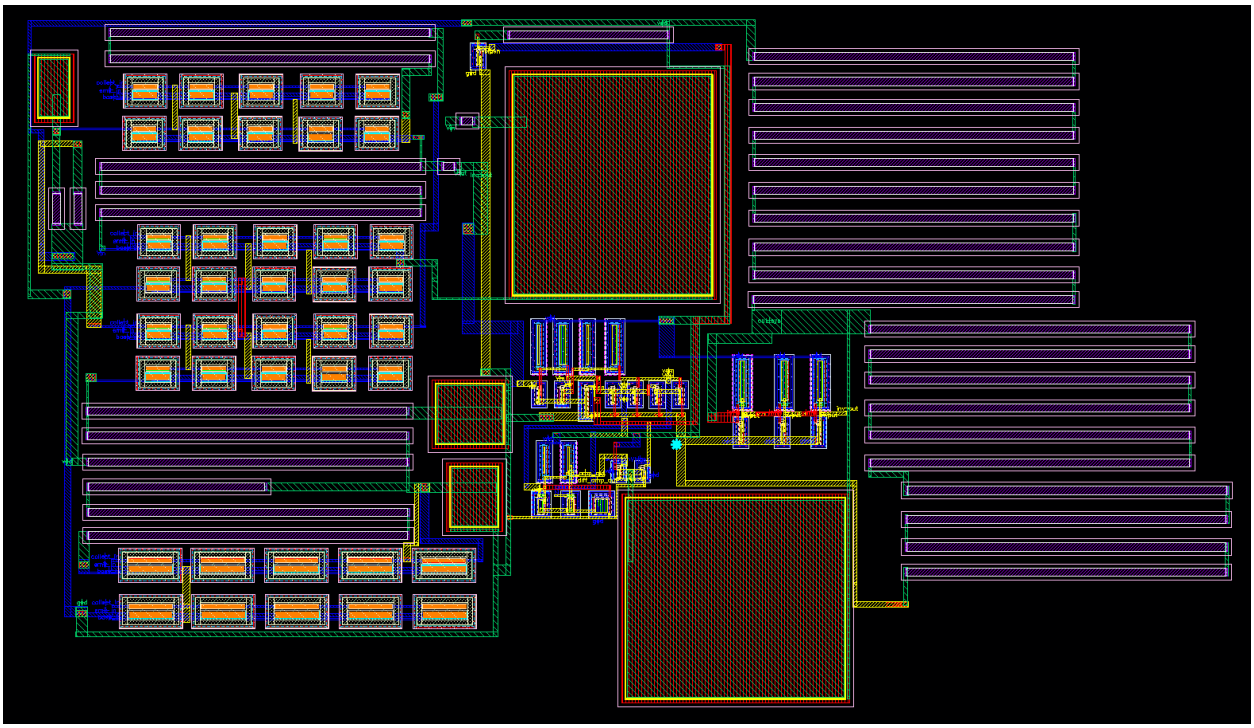
The simulation below shows only the output of the final inverter/ the final system.

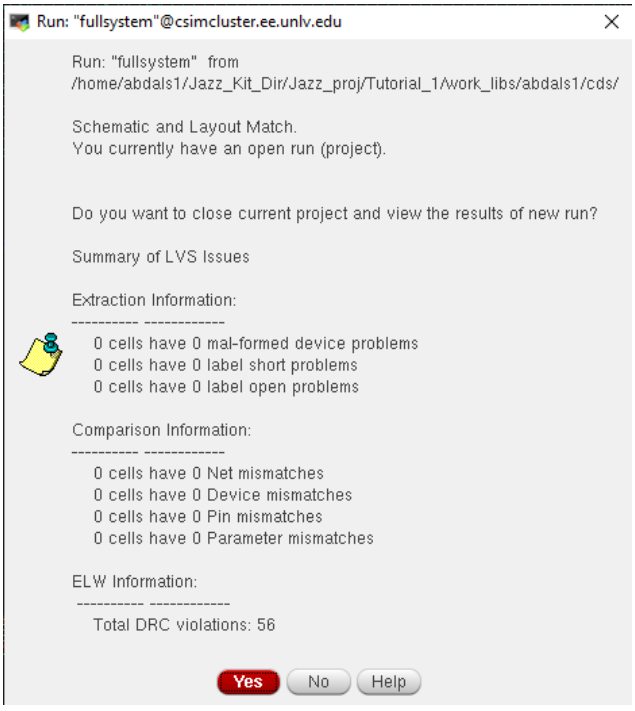




***4**: The simulation in this figure shows each stage of the system.*

Entire System Layout





The layout passes LVS.

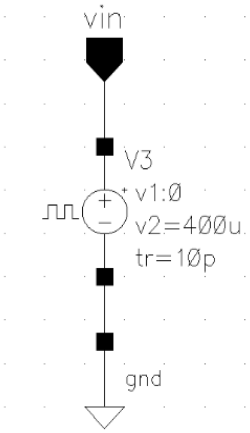
Stage 1: Heterojunction Bipolar Transistor (HBT) LNA

The design of the LNA is a cascode stage driving an emitter follower with a resistive feedback. The cascode circuit is useful because it provides a larger gain and makes a stronger circuit. The emitter follower is used as a buffer and provides more power and current to the circuit.

The circuit is made using a type of a bipolar junction transistor called a heterojunction bipolar transistor. HBTs are used as regulators that control current. HBTs use different semiconductor parts for the base and emitter. They are better than BJTs because they can operate very high frequencies, all the way up to hundreds of GHz. HBTs generate a heterojunction from different semiconductor materials that make up the device. Heterojunctions are useful because they limit the injection of holes to the emitter which will then make the transistor faster.

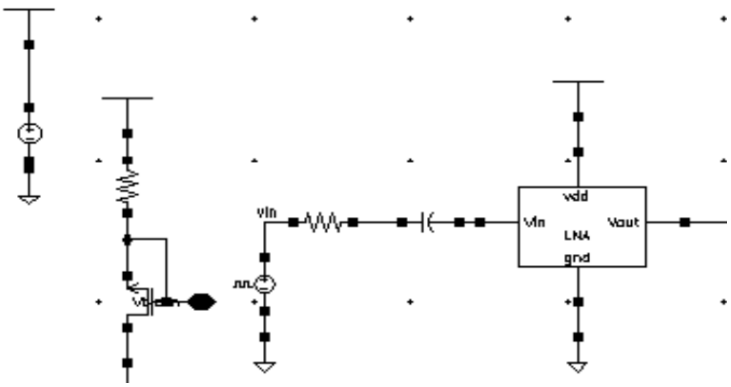
BJTs in general are a good choice for a high frequency design because the circuit needs to operate at a very high frequency and BJTs have shown some advantages at such high frequencies. BJTs have a higher gain because they have a higher gm, or transconductance. It also has better noise control than MOSFETs do. BJTs are also less susceptible to radiation which is best for a space application. Since this is not necessarily low power operation, BJTs were the most advantageous choice for high frequencies.

When the transistor turns on, electrons leave the emitter and go into the base where they diffuse until they travel to the collector to the majority carriers and add to the collector current. The holes that move and diffuse from the base to the emitter adds to the base current.

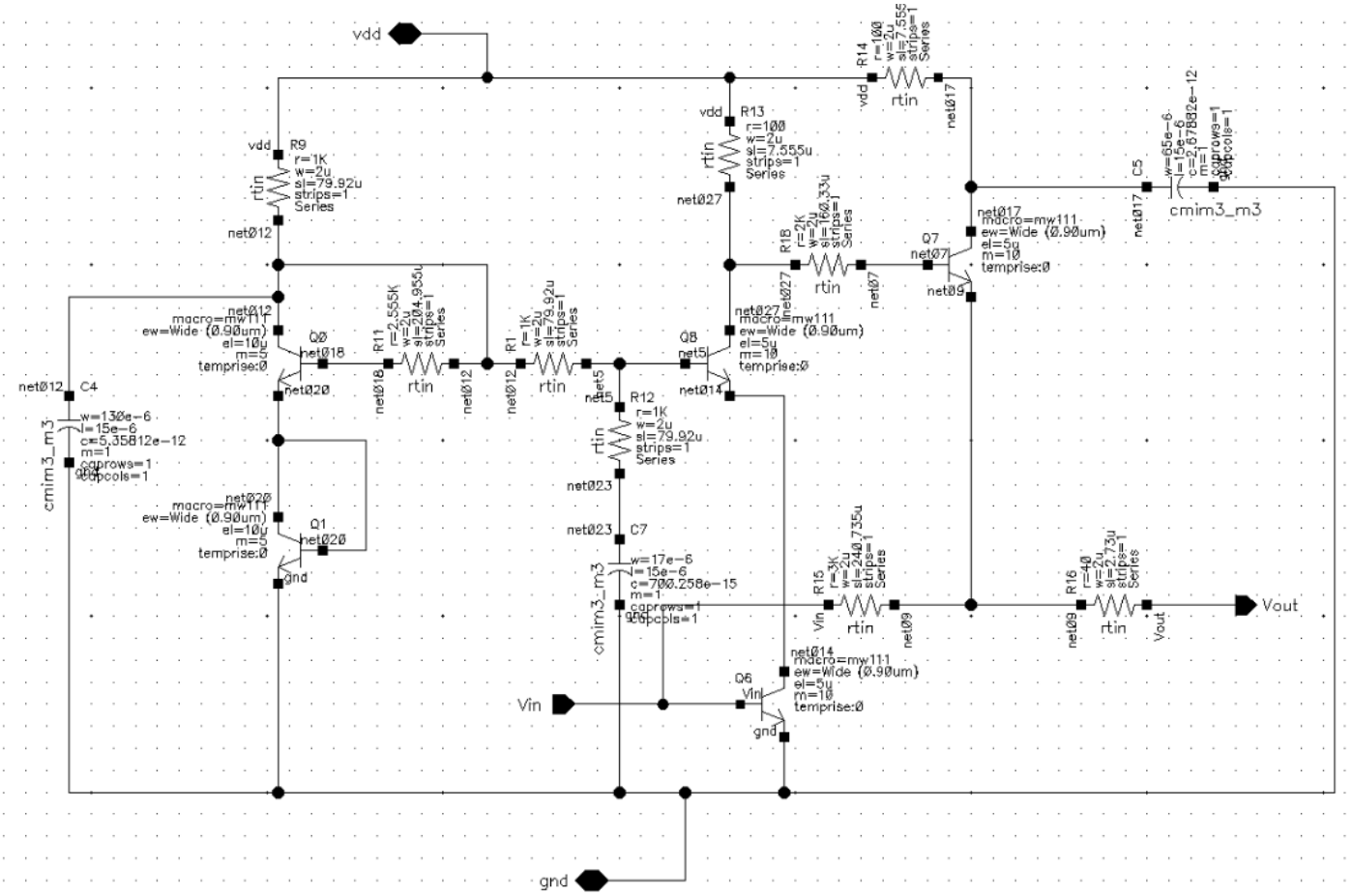


5: The input pulse.

The input of the circuit is a RC input used for testing. This enters the LNA at the Vin terminal.



6: The input pulse, biasing circuit, RC input.



The input is a pulse from 0-400uV and the output of the LNA swings around 1.13V.

Design Choice: Why Not Inductors?

Most RF LNA designs use inductors because they can filter high frequency noise well in circuits. In our TowerJazz PDK, the **TowerJazz inductors cannot be used** for simulations or layout. Only the ideal Cadence AnalogLib inductors can be used for modeling but cannot be laid out for fabrication.

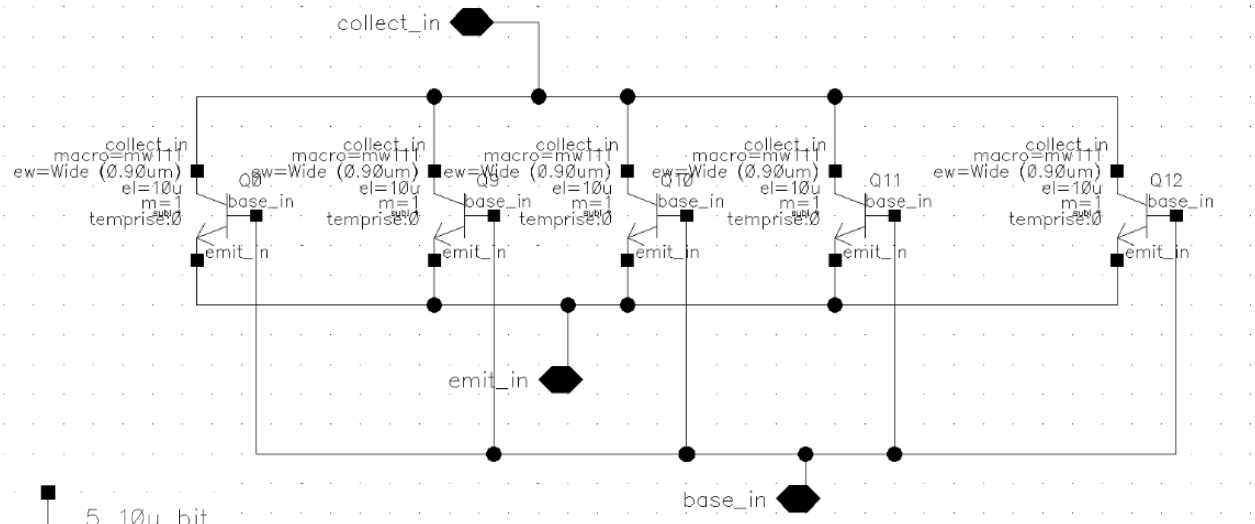
Since this circuit is to be used as the front end of a circuit for research to be submitted in March, it had to be fully made with components that can be laid out in the TowerJazz process and sent out to NASA. The original circuit that I built contained inductors and was not useful because it did not have any practical application. The lack of inductors in this process led to the usage of HBTs since they work well in high frequency situations and resist radiation well.

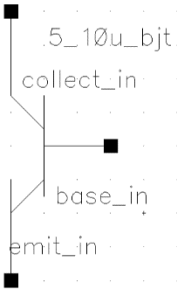
HBT Symbols

In the circuit above, the HBTs are in multiples of 5 and 10. When laying out the circuit, multiples are not allowed in the TowerJazz process. To combat this issue, I created symbols for 10 and 5 HBTs in series and placed the symbols into the circuit.

Five HBTs - Emitter Lengths of 10u

Below is the schematic of 5 HBTs with emitter lengths of 10u put in parallel. This mimics one HBT with a multiple of 5.

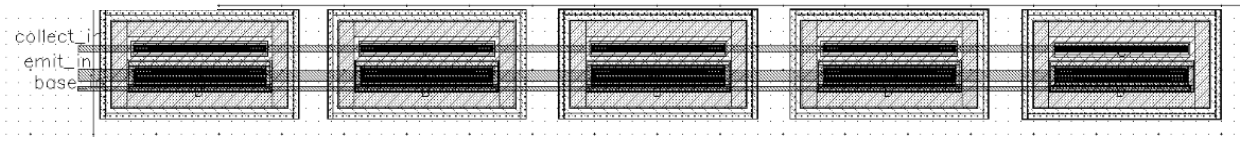




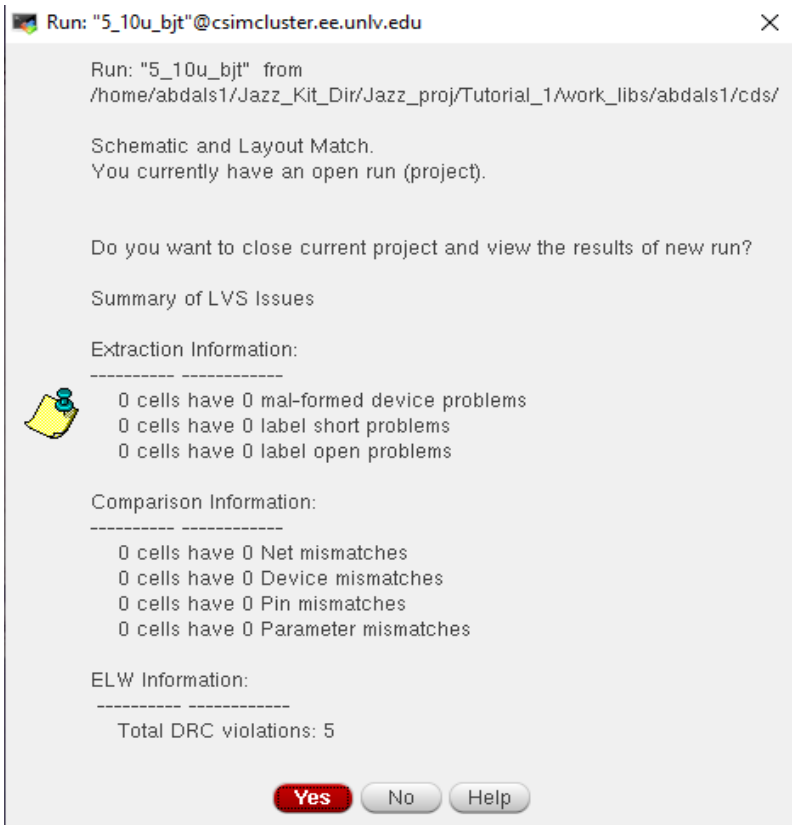
To the left is the symbol of the 10u HBT with a multiple of 5.

Below is the layout of the 10u HBT with a multiple of 5.

7: symbol of the 5 HBTs.



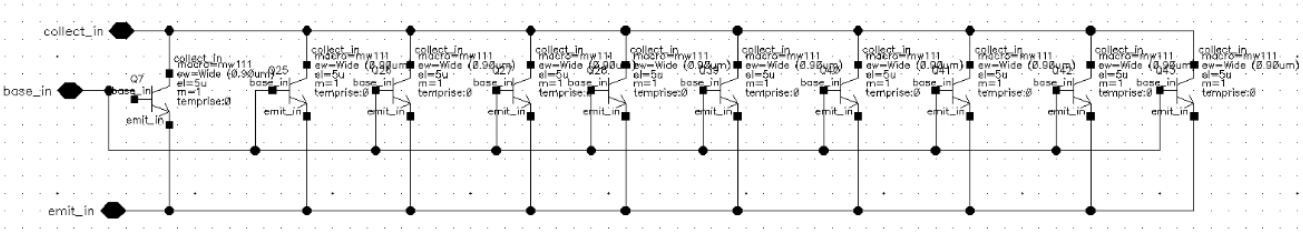
8: Layout of the 5 HBTs.



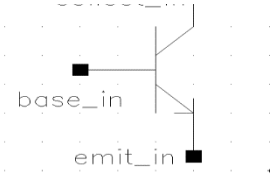
The circuit passes LVS.

Ten HBTs - Emitter Length of 5u

The following circuit is made up of 10 HBTs with emitter lengths of 5u.

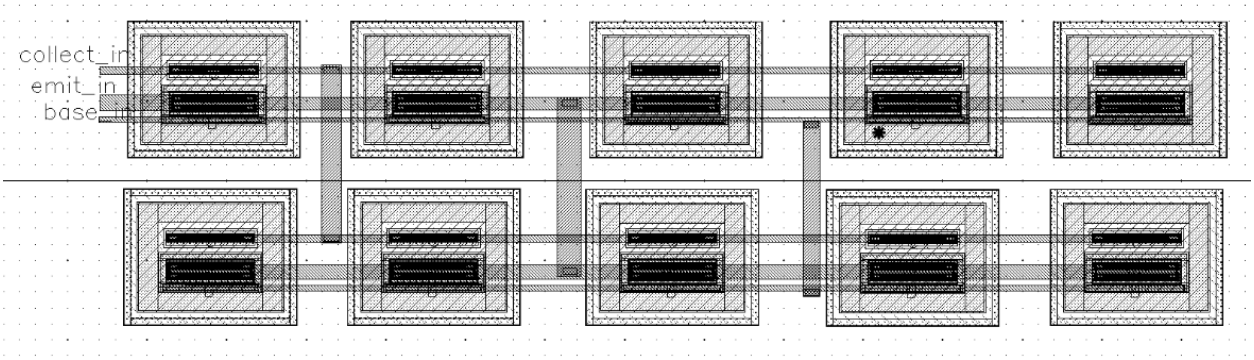


10: Schematic of the 10 HBTs.



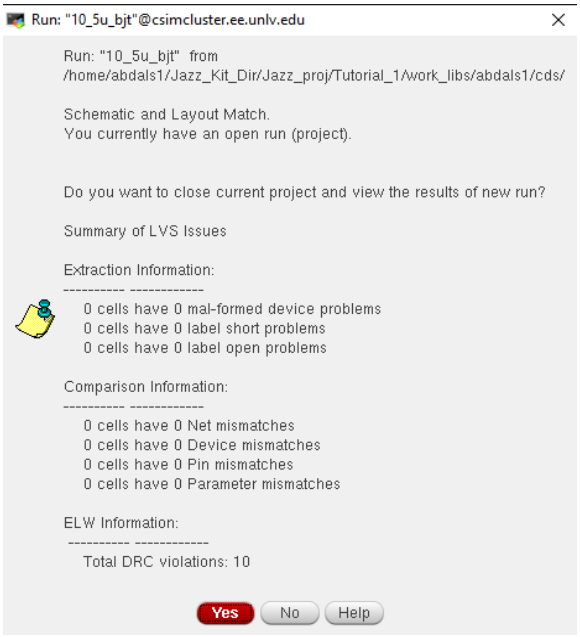
9: Symbol of the 10 HBTs.

To the left is the symbol.



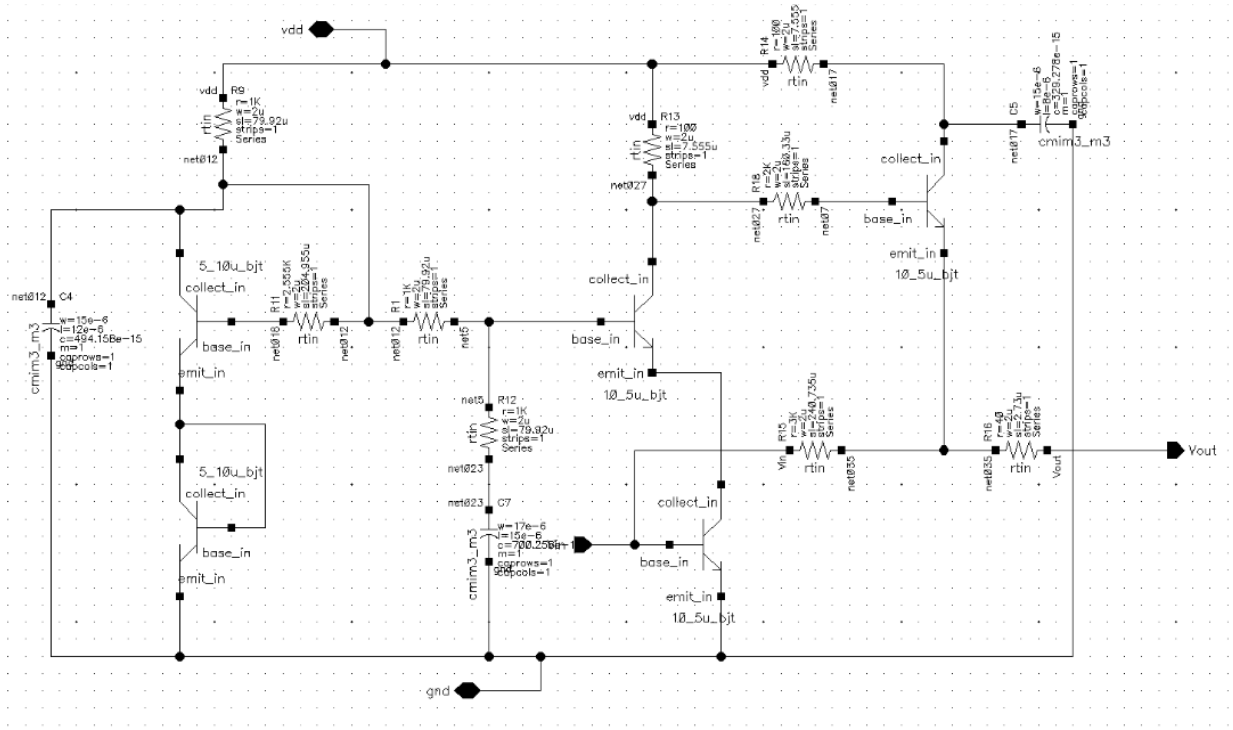
11: Layout of the 10 HBTs.

The layout above is of 10 HBTs with widths of 5u.



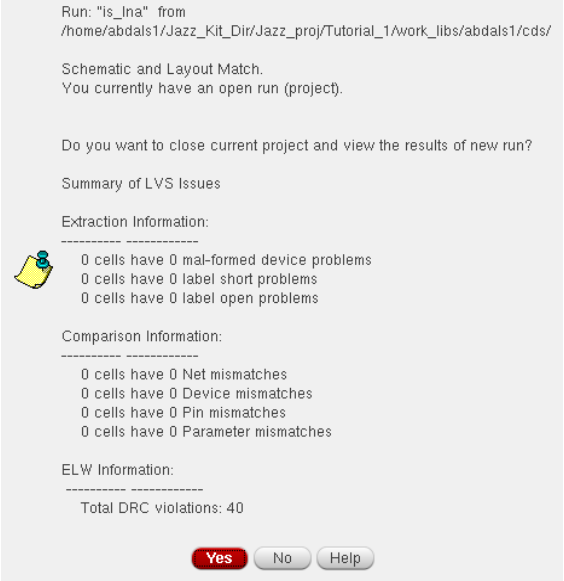
The circuit passes LVS.

Final LNA Design Using HBT Multiplier Symbols



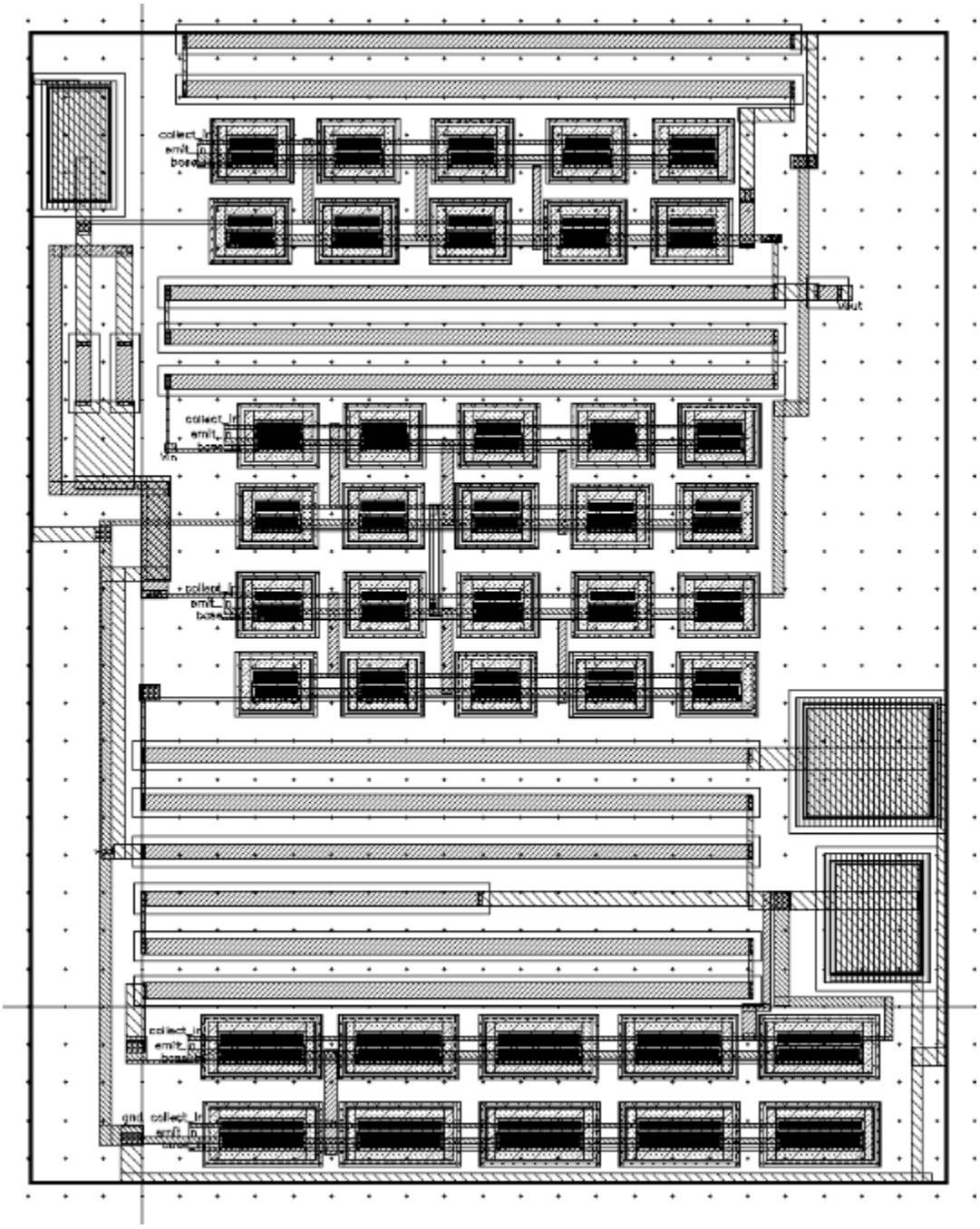
12: The final LNA Circuit using the HBT Symbols made above.

The circuit passes DRC and LVS.

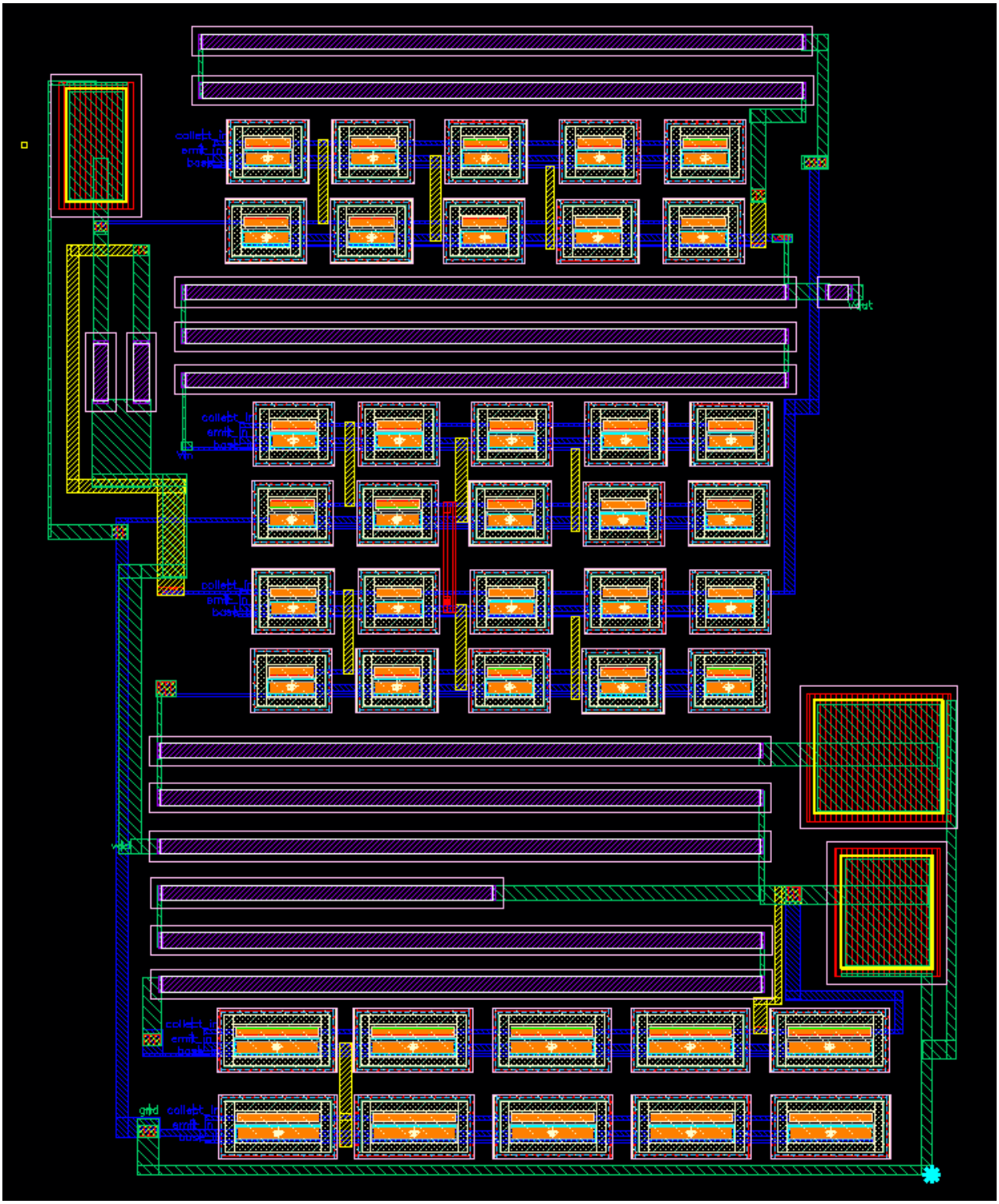


LNA Layout

Below are the monochrome and full-color images of the LNA layout using the HBT symbols.



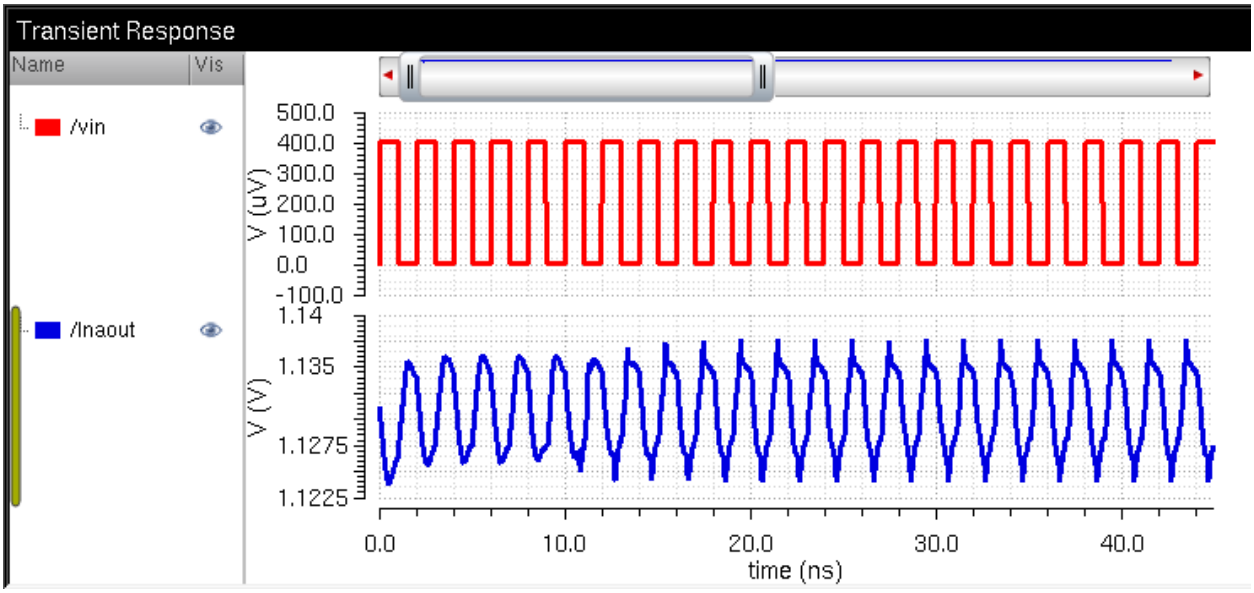
13: LNA Layout - Monochrome.



14: LNA Layout - Full Color.

LNA Simulations

The transient simulation result below shows the input pulse in red, a 400uV input signal with a 2ns period and the output in blue, swinging around 1.13V.



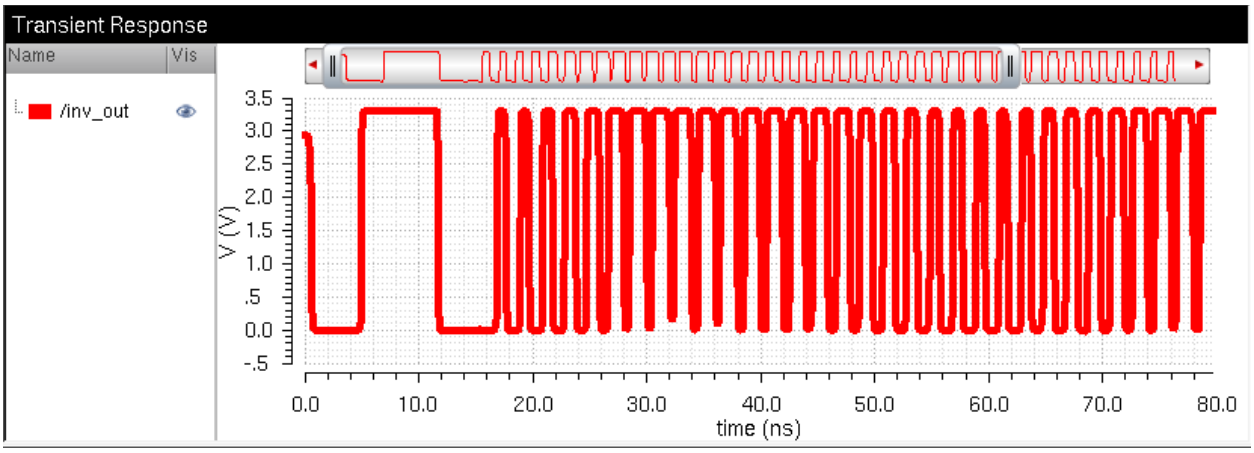
15: Transient response with a 400uV pulse input signal.

LNA Simulations with Load

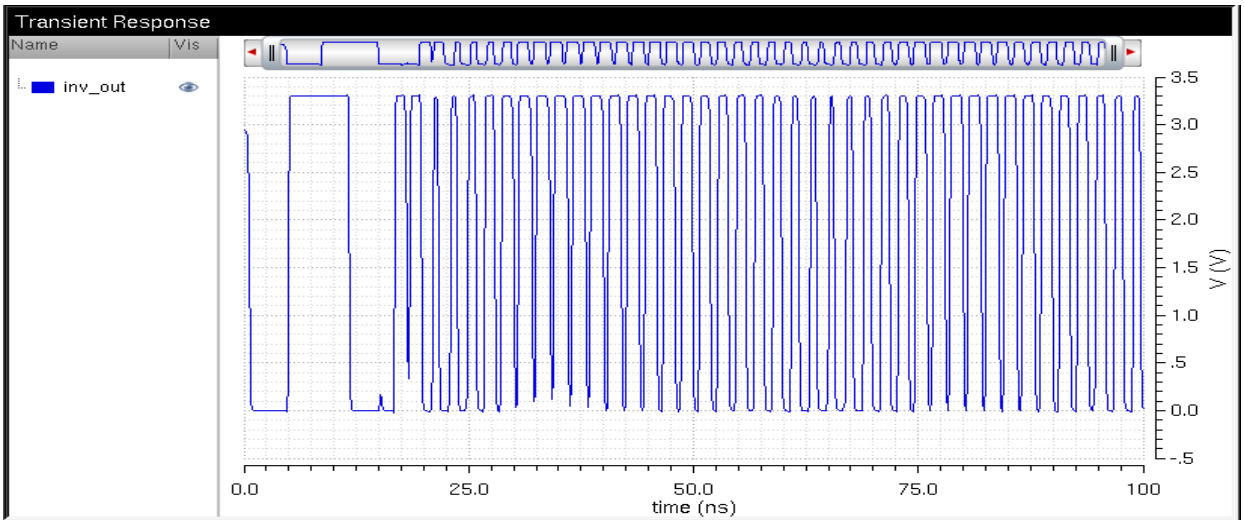
The following results show the output swing with different capacitive loads.

Capacitive Load	**Output Swing**
50fF	**0-3.3V**
100fF	**0-3.3V**
150fF	**0-3.3V**

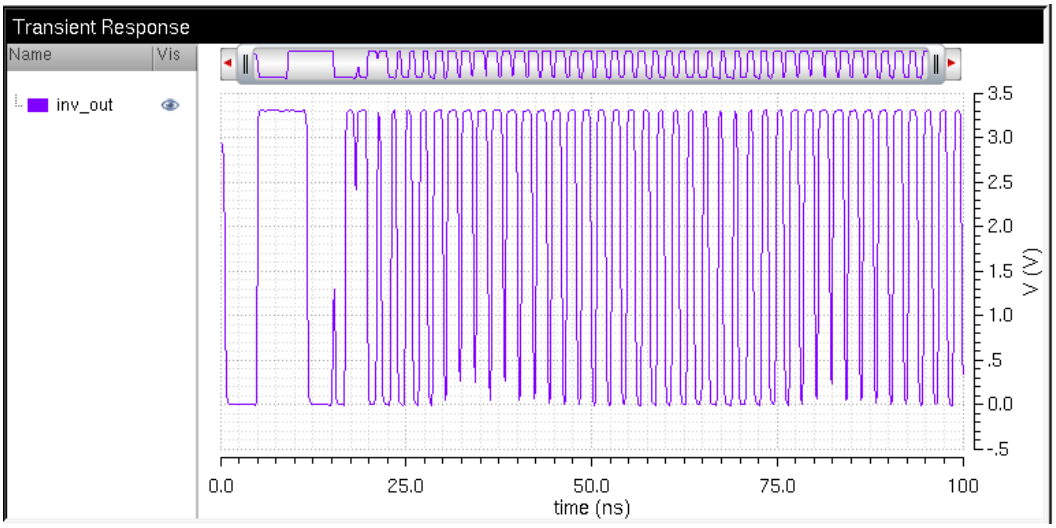
50fF


Transient Response
Name
Vis
/inv_out
3.5
3.0
2.5
2.0
1.5
1.0
.5
0.0
-.5
V (V)
0.0
10.0
20.0
30.0
40.0
50.0
60.0
70.0
80.0
time (ns)

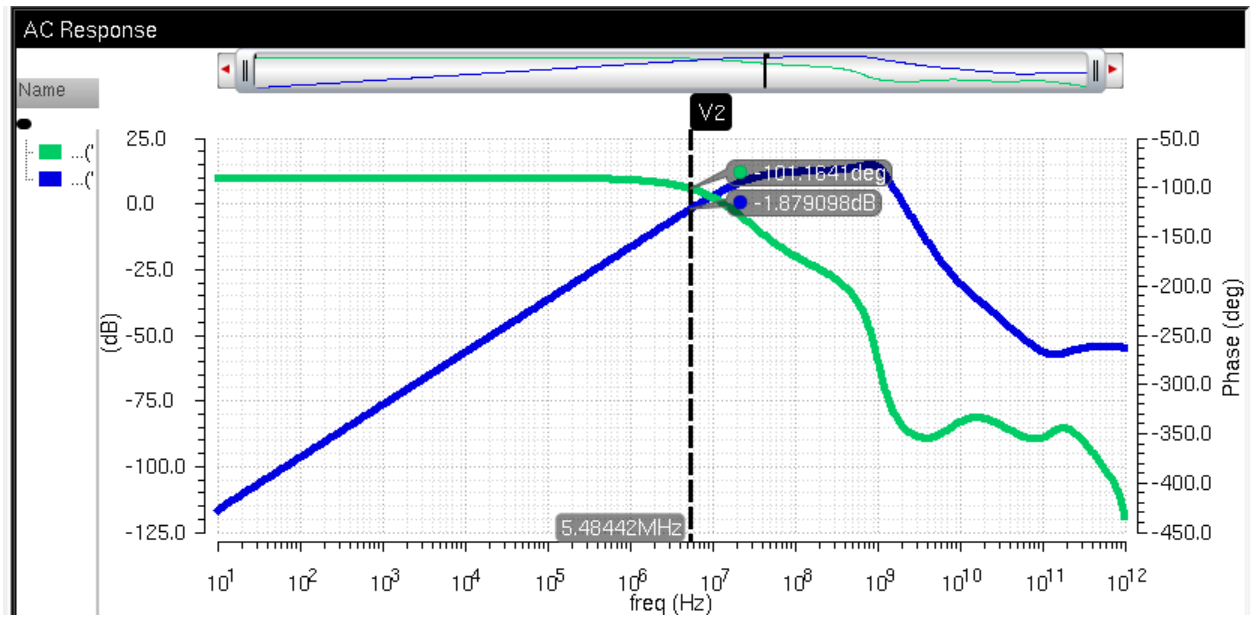
100fF


Transient Response
Name
Vis
inv_out
3.5
3.0
2.5
2.0
1.5
1.0
.5
0.0
-.5
V (V)
0.0
25.0
50.0
75.0
100
time (ns)

150fF – The circuit is not powerful enough to drive the load, and for future simulations, a buffer will be added to allow the circuit to drive a larger load.



AC Analysis



16: AC response of the LNA.

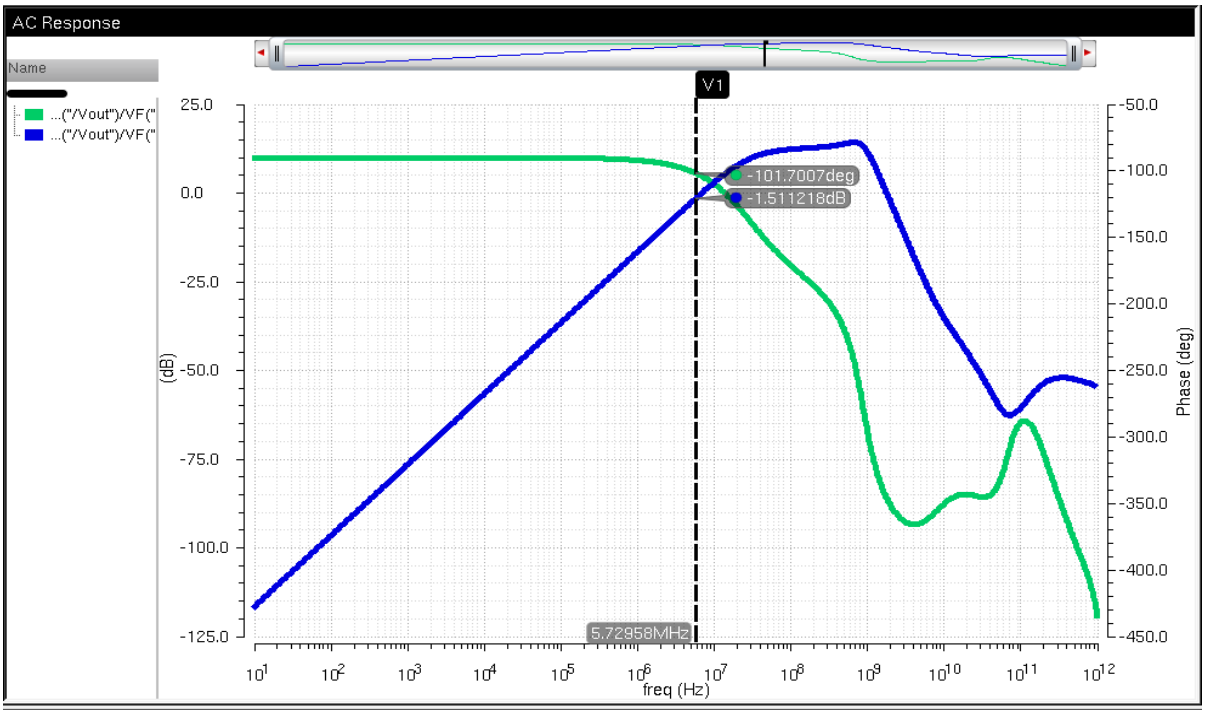
At about 0dB the phase is -101.164 which gives a phase margin of about 80 degrees.

$$180\ degrees - 101.164\ degrees\ =\ 78.836\ degrees\ of\ PHASE\ MARGIN$$

It takes some time to charge up because of the RC topology of the input of the system. The RC topology used for the input is used for simulation purposes.

AC Analysis with Inductor

To test the stability, I added an ideal AnalogLib inductor into the feedback loop. The circuit was still stable, and the inductor was removed for the final layout and simulations.



17: AC response of the LNA with an inductor in the feedback.

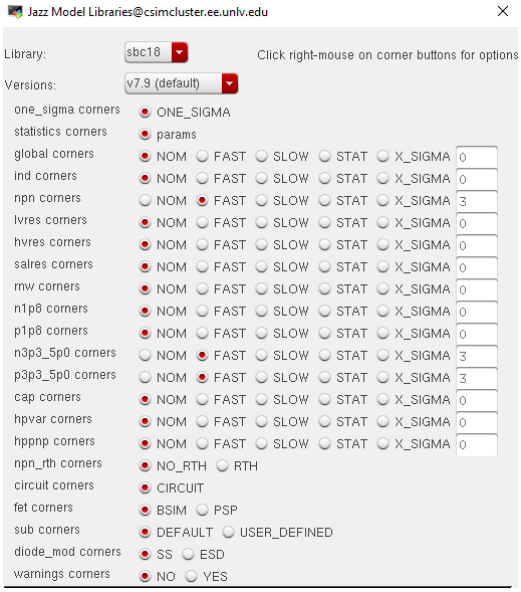
$$180\ degrees\ -\ 101.7\ degrees\ =\ 78.3\ degrees\ of\ a\ phase\ margin$$

Based on the AC response, the gain of the circuit is about 24dB with a phase margin of 78.3 degrees.

LNA Corner Simulations - Practical Operations

The TowerJazz transistors used in this circuit are “npn,” “n3p3_5p0,” and “p3p3_5p0.” To simulate the best and worst possible cases of transistor operation in practical applications, I adjusted the transistors speed from nominal to fast or slow.

Corner simulations are useful for practical circuit design because they allow us to see how the circuit can operate under any transistor condition. Since this circuit is to be used for research and will be the front end of other components, it is important to ensure that it can operate at as many conditions as possible.

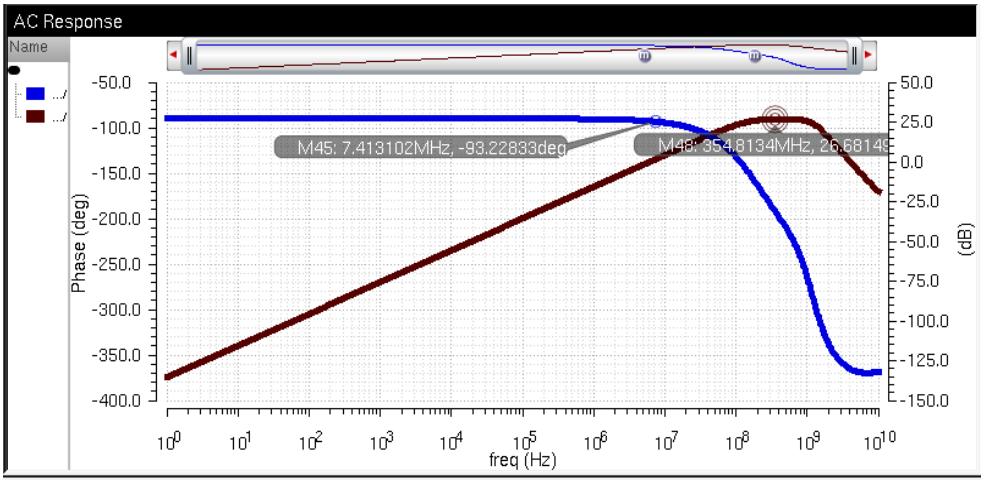


18: Corner simulation selection window.

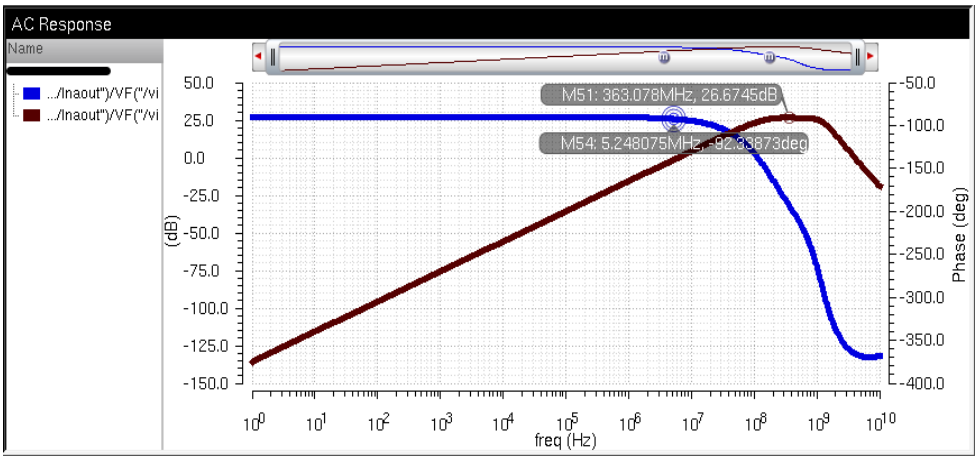
The following table details the operation of the transistors under different conditions showing their AC gain.

Sim #		npn	n3p3_5p0	p3p3_5p0	AC gain (dB)	Phase Margin (degrees)
1	Process Corner	Fast	Fast	Fast	26.670	86
2	Process Corner	Slow	Slow	Slow	26.670	88
3	Process Corner	Fast	Slow	Fast	26.680	87
4	Process Corner	Fast	Slow	Slow	26.602	88
5	Process Corner	Slow	Fast	Slow	23.301	83
6	Process Corner	Slow	Slow	Fast	23.301	83

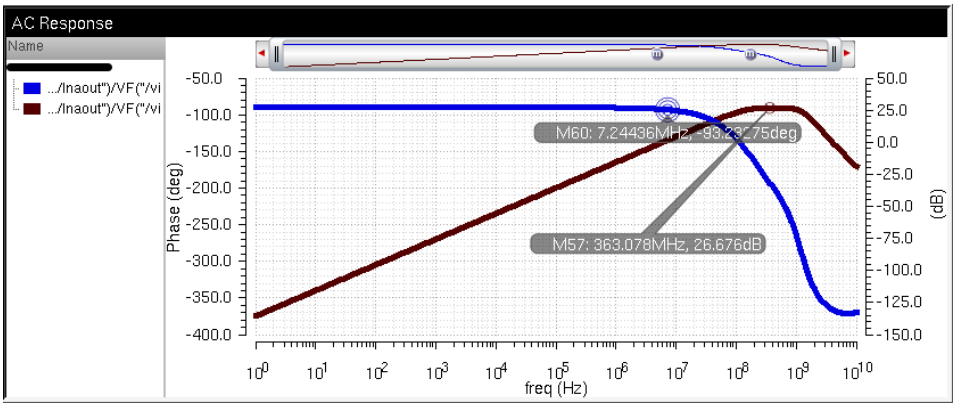
The following six simulations show the AC Response for the combination number given above.

1. 

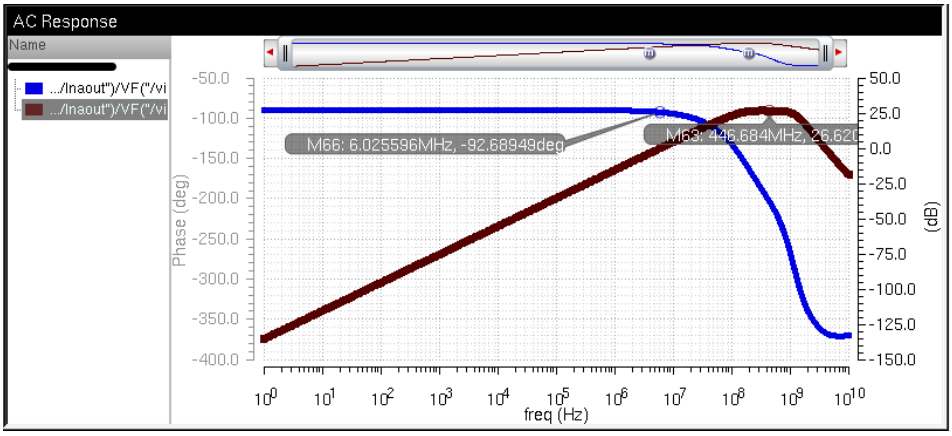
19: AC response of simulation 1.

2. 

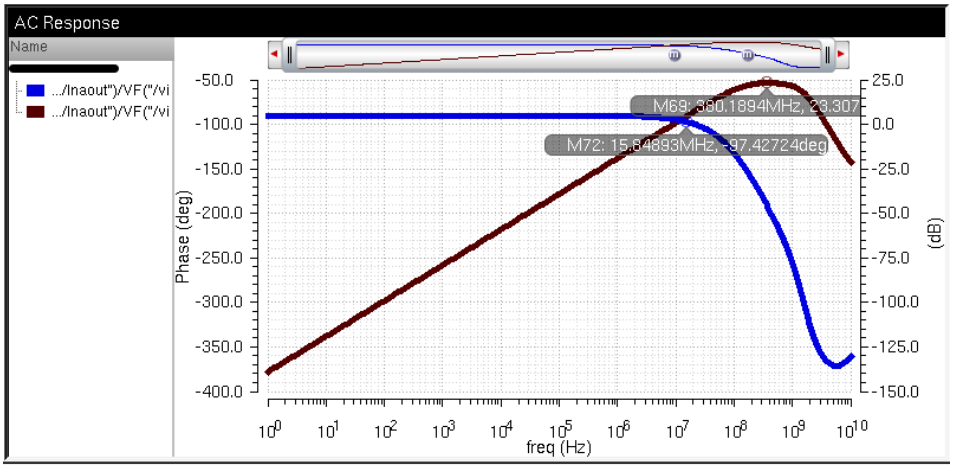
20: AC Response of simulation 2.

3. 

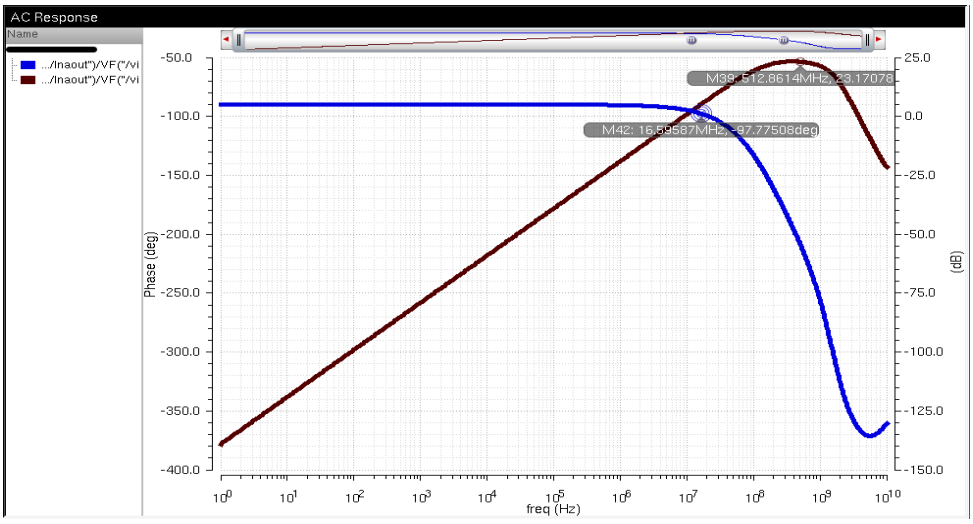
21: AC response of simulation 3.

4. 

22: AC response of simulation 4.

5. 

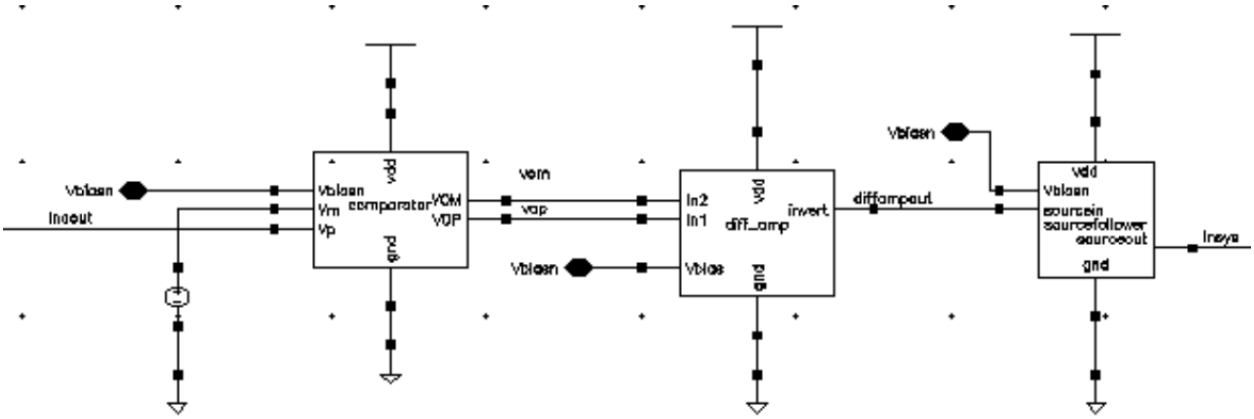
23: AC response of simulation 5.

6. 

24: AC response of simulation 6.

Stage 2: Comparator

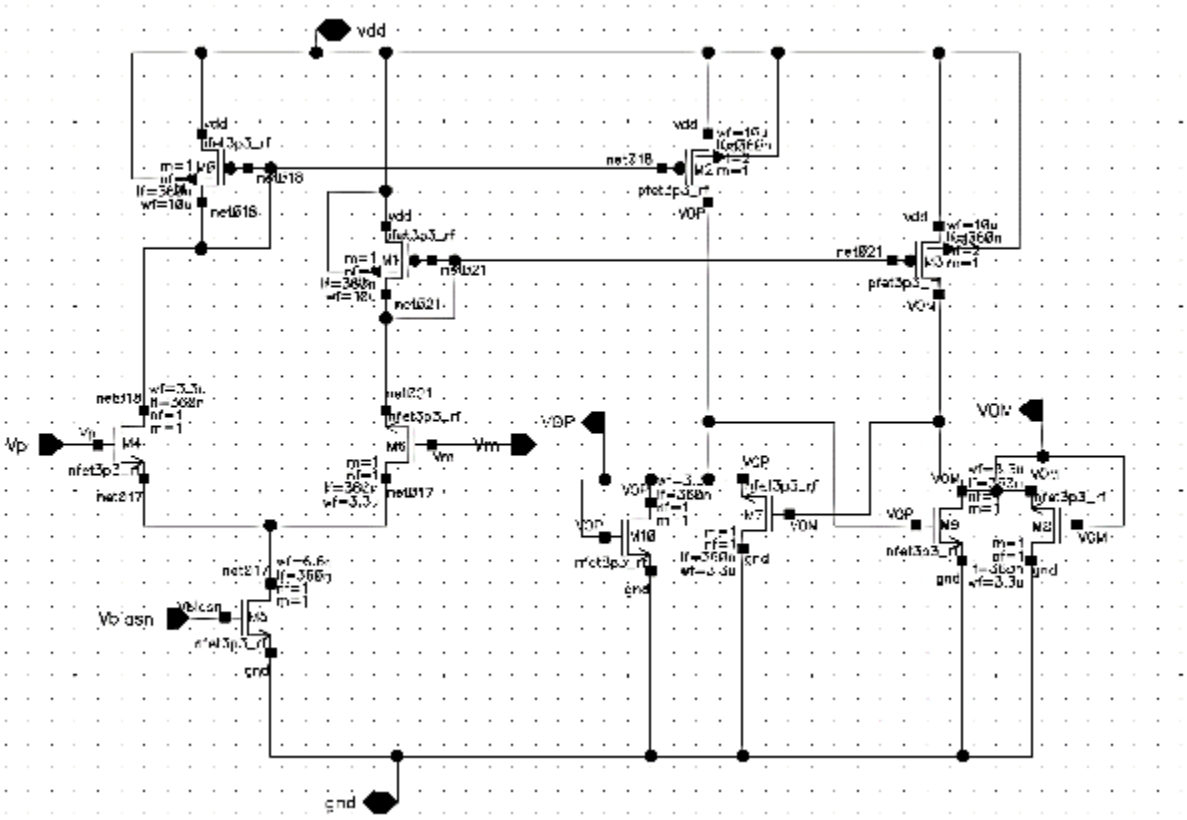
A comparator is a nonlinear analog circuit that outputs a logic 1 if VP is higher than Vm and outputs a 0 if VM is higher than VP. It compares two input voltages. In this case, the comparator reads in the output of the LNA and a DC constant voltage source that is about the same voltage as the LNA voltage. It takes in the two signals to an input preamplifier and a decision circuit. The preamplifier part of the comparator reads in the input and amplifies it to prepare it for the second stage. This amplification is useful in this design because the final goal is to amplify the signal as much as possible. It also makes the comparison at the decision end of the circuit more precise and correct. The comparator also isolates the input from the noise associated with it using the second stage and from the hysteresis contained in the second stage, using positive feedback. The topology of the preamplification stage consists of a differential amplifier with active loads. The current in the decision circuit is mirrored across the other transistors to its left. This circuit is designed with hysteresis in order to remove the noise from the signal.



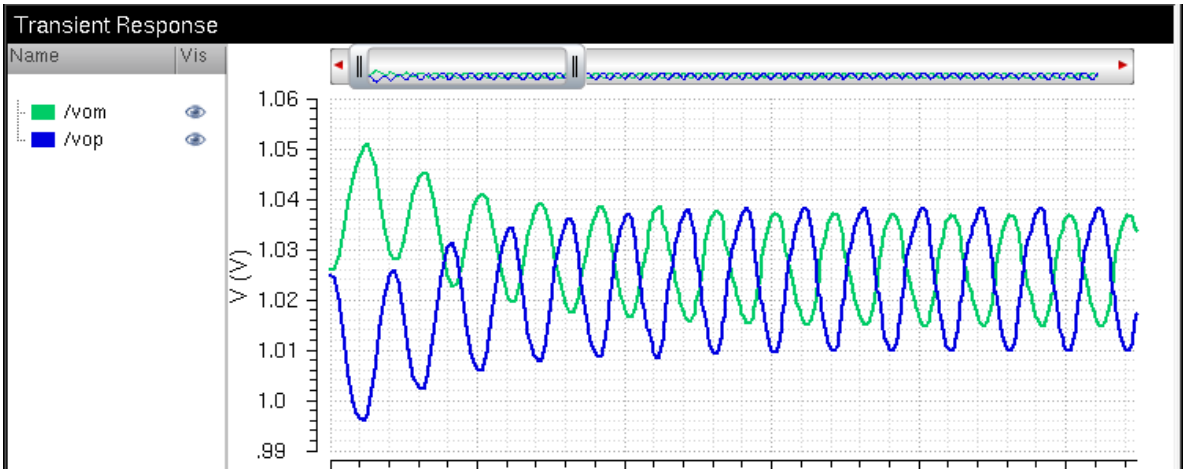
25: The comparator feeds into the differential amplifier whose output enters the source follower.

The circuit above shows the connections from the comparator to the differential amplifier. The output of the LNA and a constant voltage source of 1.131V feed into the comparator and output the VOM and VOP voltages which then enter the differential amplifier.

Below is the schematic of the comparator.



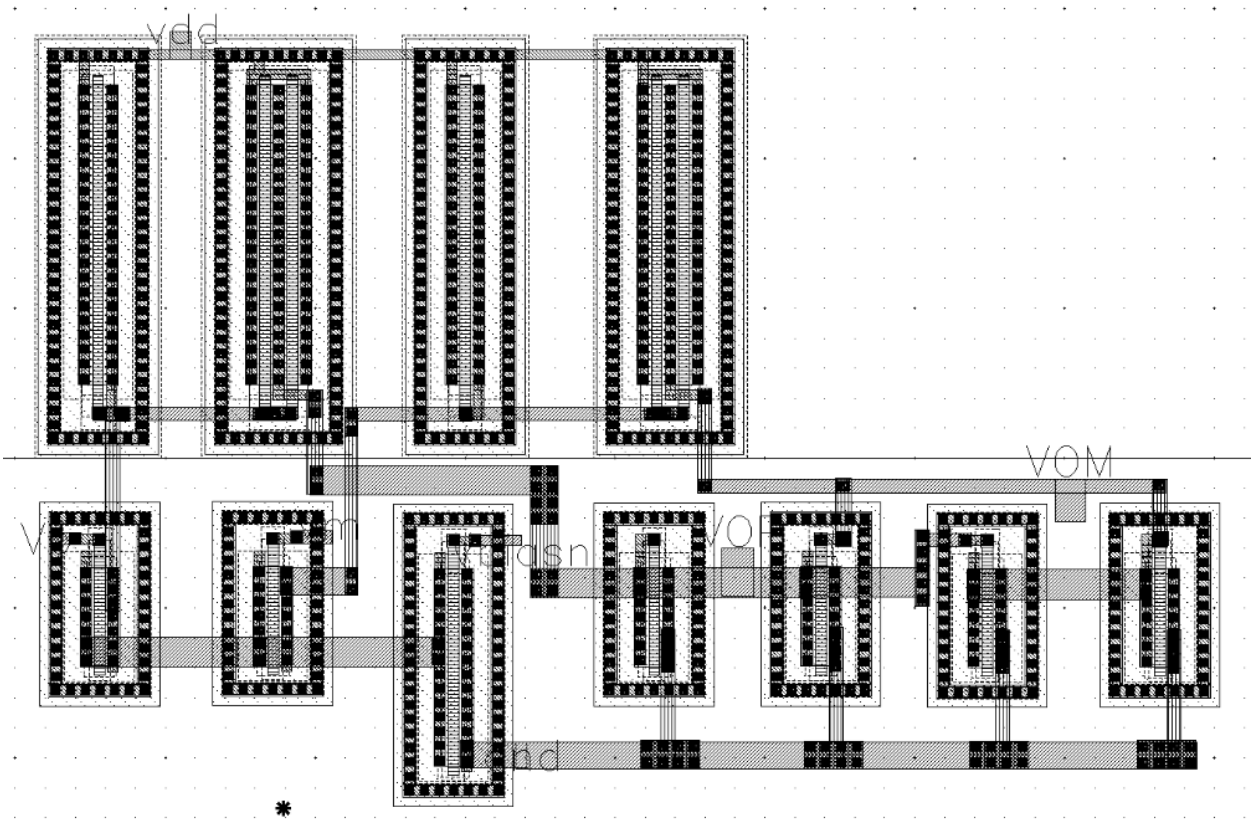
Below is transient response where the inputs are 1. The output of the LNA and 2. A DC voltage source mimicking the voltage of the LNA, at about 1.131V. Both outputs of the LNA swing around 1.02V.



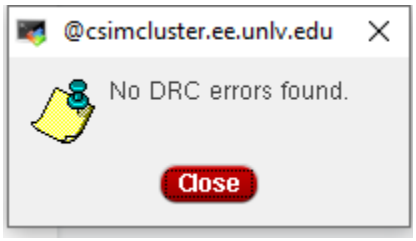
26: Transient response of comparator.

Comparator Layout

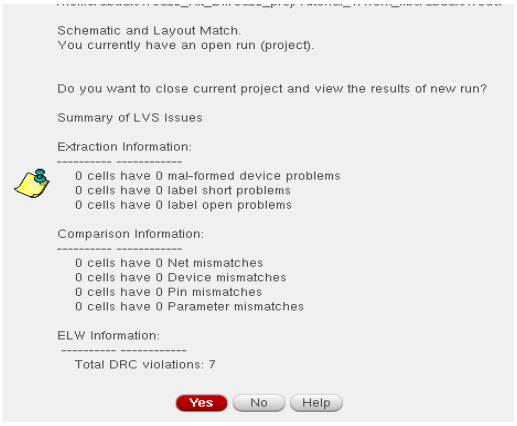
The four MOSFETS in the top row are pfet_rf devices and the seven MOSFETs in the bottom row are nfet_rf devices. They are surrounded by guard rings to protect from latch-up and parasitic substances that can arise when transistors are too close together.



27: Layout of comparator.



The layout passes DRC and LVS.

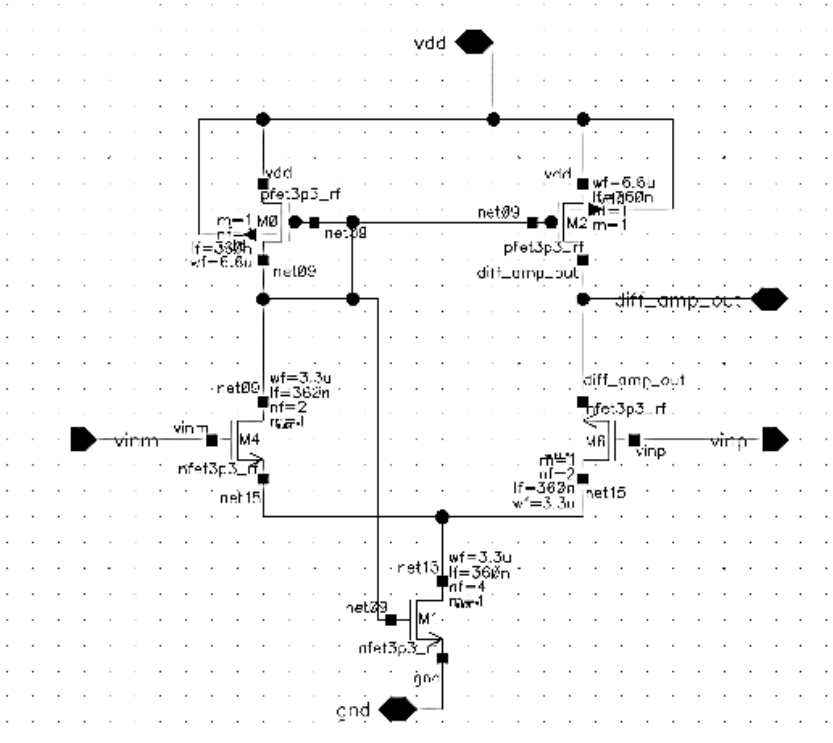


Stage 3: Differential Amplifier Input Buffer

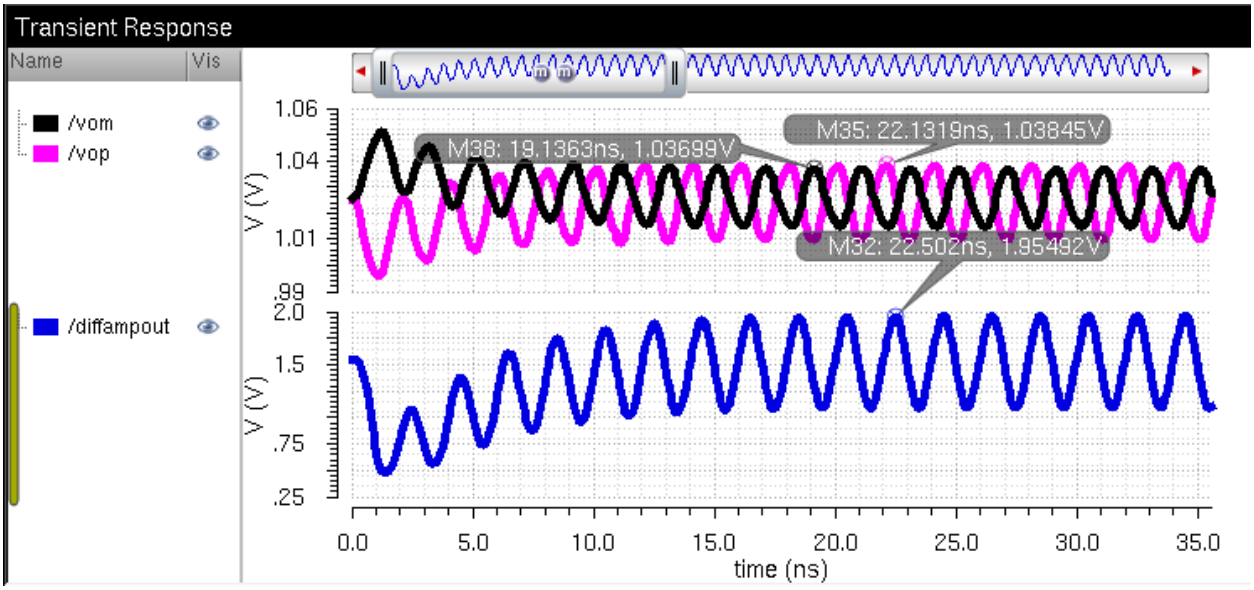
The differential amplifier amplifies the difference of the two signals from the comparator and outputs a 1.95V signal.

When Vinp is larger than Vinm, the output is a logic 1 and when Vinm is larger than Vinp, the output is a logic 0. Vinm is the best port for inputting the signal because the MOSFET above that port is diode connected which means that it has less resistance than the other transistors. When Vinp is higher than Vinm, it has a larger current than the transistor whose gate is connected to Vinm. The current is then transferred to the transistor above it and mirrored to the transistor above the one that holds Vinp. This causes Vinp to go to ground until the currents of the transistors above each other to the right size of the circuit are equal. The circuit is self-biased and does not require any extra circuitry.

Below is the differential amplifier circuit.



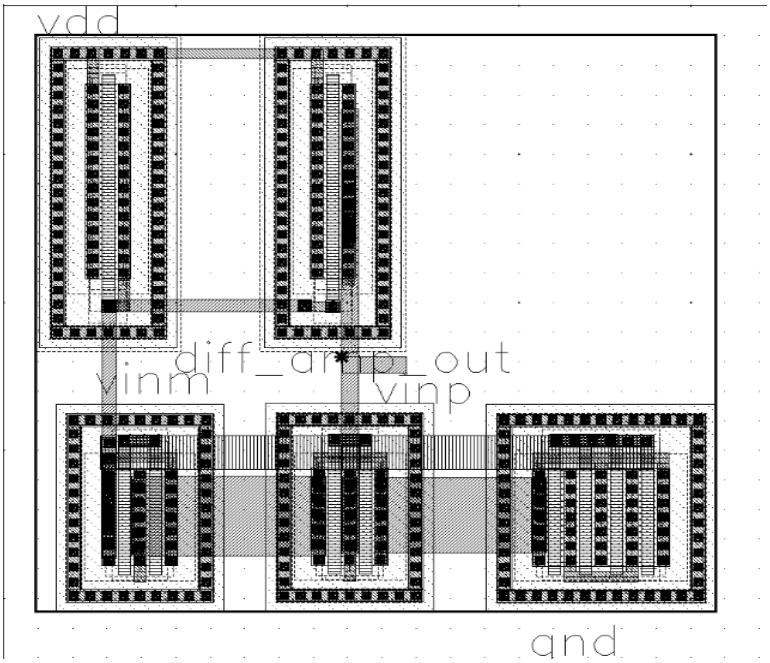
Below is the transient response when the inputs to the differential amplifier are the outputs of the comparator. The output of the differential amplifier swings up to 1.95V.

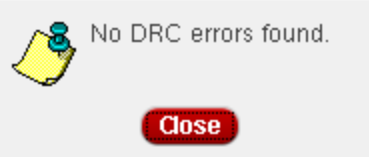


28: Transient response of differential amplifier giving the output of 1.95V.

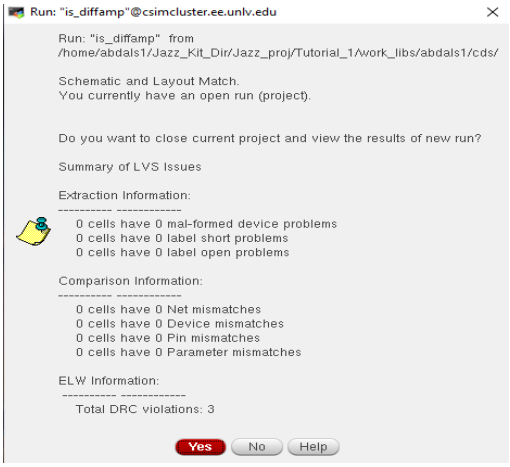
Differential Amplifier Layout

The top row is made up of pfet_rf devices and the bottom row is made of nfet_rf devices. Again, the guard rings protect the transistors from parasitics and latch-up.





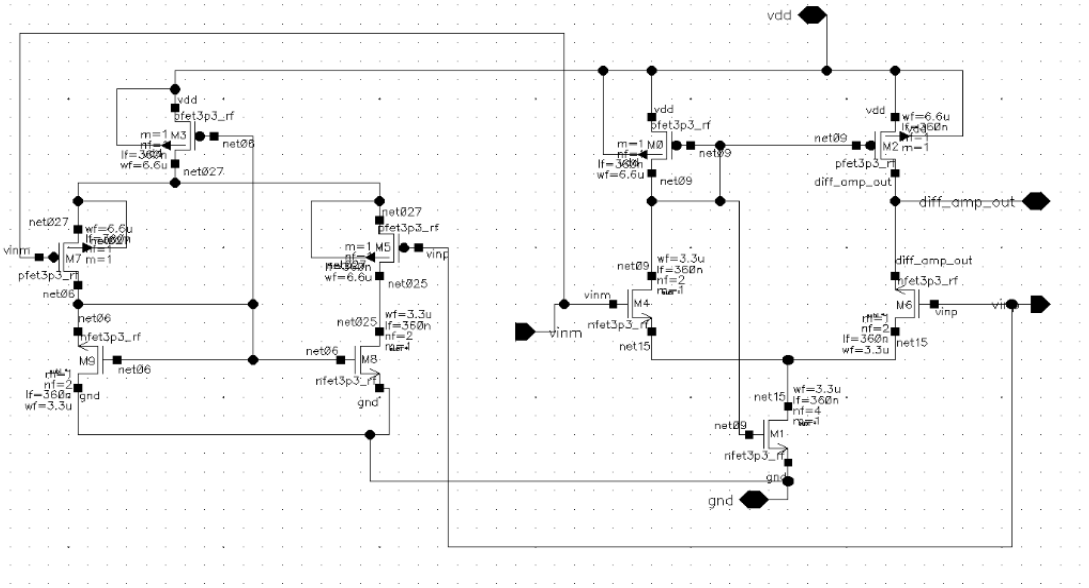
29: The Layout passes DRC.



30: The layout passes LVS.

Alternative Differential Amplifier Design: NMOS Diff Amp in Parallel with PMOS Diff-Amp

Because this is a high-speed design with varying inputs, an NMOS differential amplifier and buffer in parallel with a PMOS differential amplifier and buffer is a useful alternative design. The PMOS differential amplifier has less propagation delay and works best for smaller signals, which was the goal in this operation since a voltage as low as 400uV was used. Putting the two in parallel and using both NMOS and PMOS designs can allow for a wider range of signals while also reducing the propagation delay. This design was not used in this report because the NMOS design worked well enough, so additional circuitry was not necessary. The layout size was also taken into consideration in the design since this will be the front end of other circuitry, so the goal was to reduce layout size as much as possible.



The circuit above is the PMOS differential amplifier buffer (left) and the NMOS differential amplifier (right) in parallel.

31: Alternative differential amplifier.

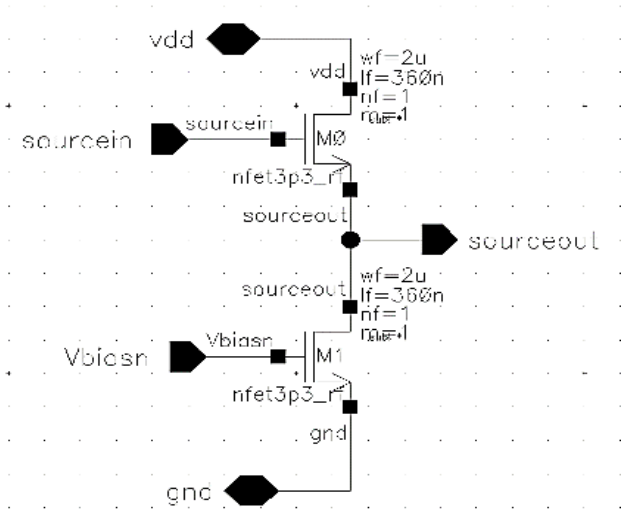
Stage 4:

NMOS- NMOS Source Follower/ Common Drain Amplifier

The source follower is used as a buffer from the differential amplifier to the inverters to increase the gain. The gain can be reduced without a source follower because of the high impedance node. The connections of the circuits following the source follower can interact poorly with a high impedance node, removing the gain.

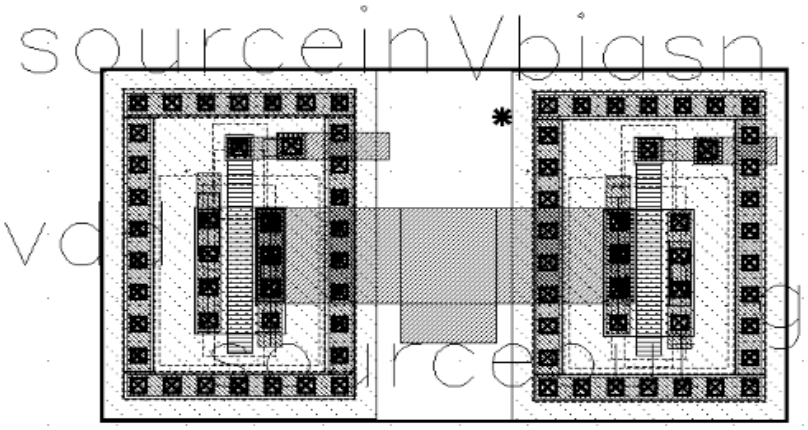
The source follower has a very low resistance because the resistance of the NMOS and the resistance of the output node is 1/gm. Both NMOS devices have the same sizes.

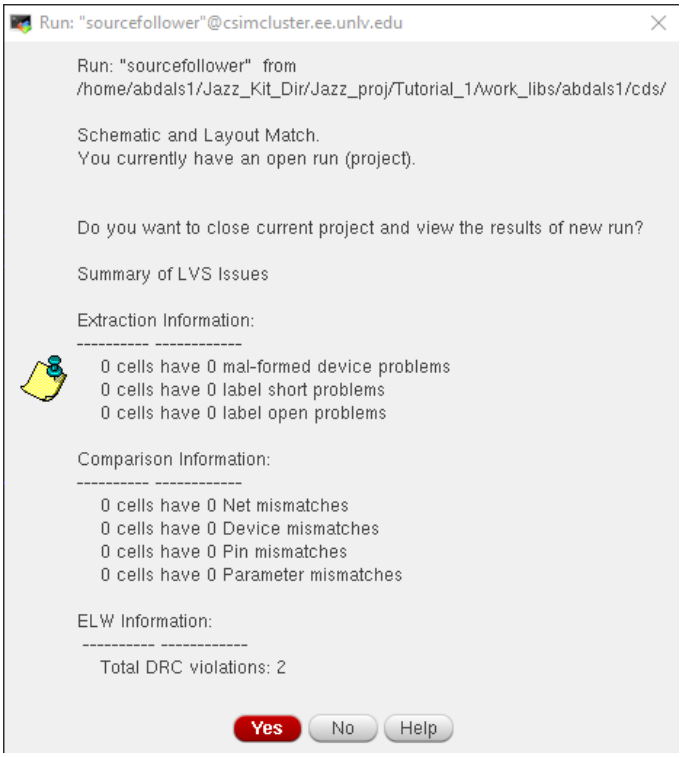
33: The source follower layout passes DRC.



32: Source follower schematic

.



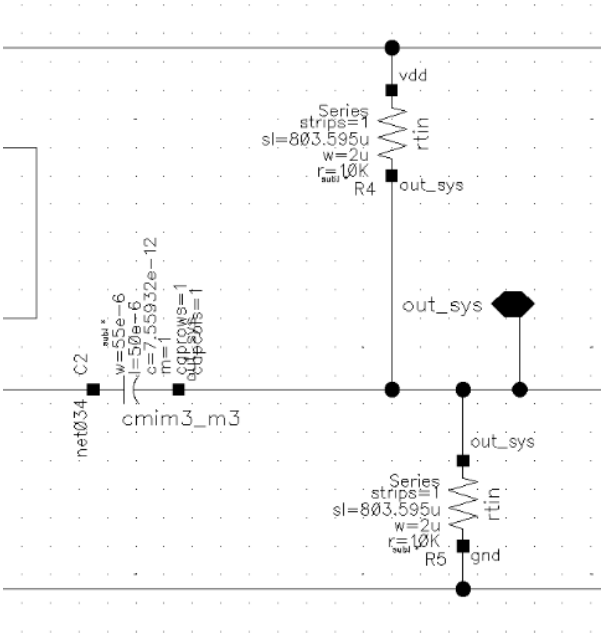


34: The layout passes LVS.

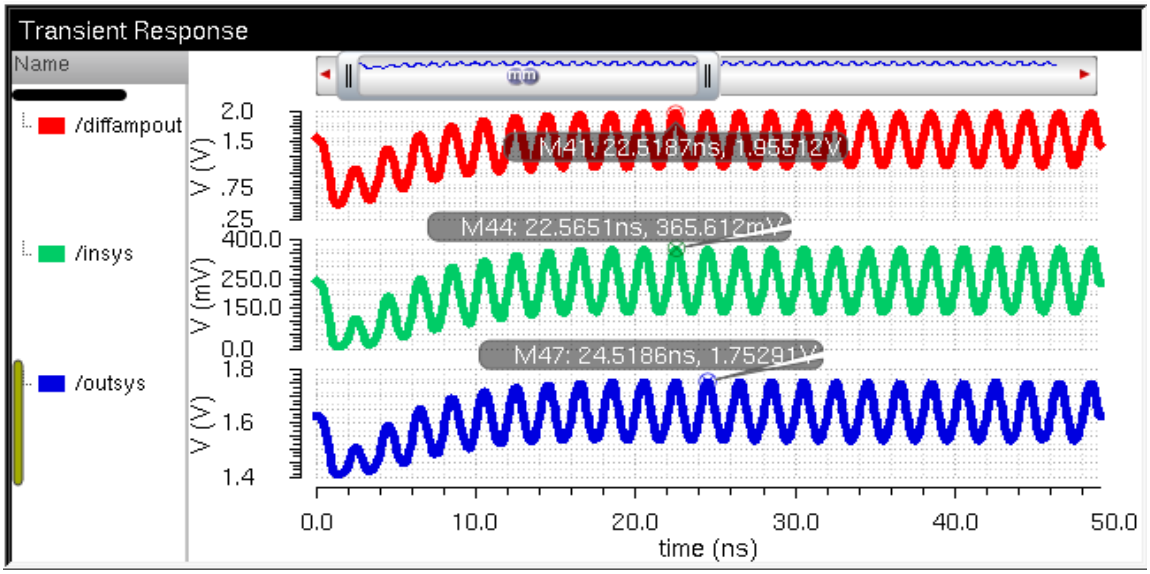
Stage 5: DC Biasing

Since the signal is not at the switching point of the inverter, I DC biased the voltage to get it near the switching point of the inverter for it to amplify, using a coupling capacitor and a voltage

divider. The voltage after the DC biasing was about 1.75V. The sizes I used are 7.559pF capacitor and two 10kohm resistors. The maximum resistor value in this process is 10kohms.



***35**: DC biasing circuit with 7.559pF capacitor and two 10k resistors in parallel.*



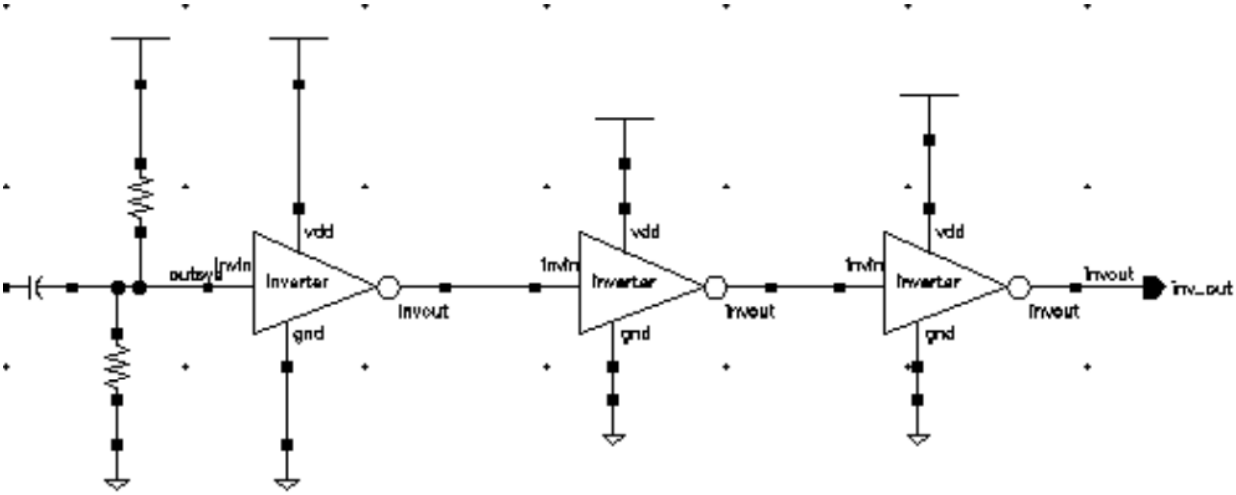
***36**: The output of the biasing circuit puts the voltage above the switching point of the inverters making the gain much larger.*

Stage 6: Three RF Inverters

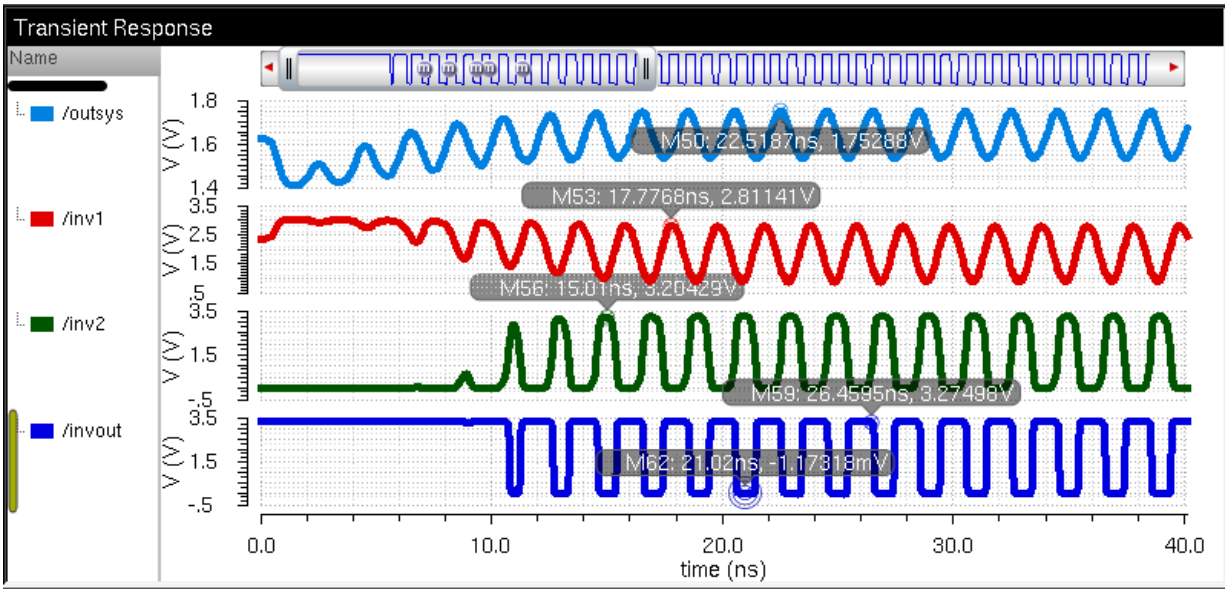
Since the voltage is above the switching point of the inverter, the inverters were able to amplify the voltage. The output voltage swings from rail to rail, from 0 to 3.3V, which is VDD.

The input from the DC biasing is 1.75V. This voltage feeds into the first inverter, and the output, inv1, is 2.811V. This voltage feeds into the second inverter and outputs 3.2V. After the third inverter, the output is 3.27V.

The final output swings from -1.17mV to 3.27V.



***37**: The three inverters in series.*



***38**: The gain of the system is large because the voltage entering the inverter is above the switching point.*

RF Inverter Design and Switching Point

The switching point of an inverter is where the output voltage is equal to the input voltage. It is the voltage where both MOSFETS in the inverter are in the saturation region. It can be found and changed using the Beta ratio of the MOSFETs in the following equation where Bn is the Beta Coefficient of the NMOS and Bp is the Beta Coefficient of the PMOS:

$$\frac{Bn}{2} * (VSP - VTHN)^2 = \frac{Bp}{2} * (VDD - VSP - VTHP)^2$$

Since the desired VSP (Switching Point Voltage) is 1.65V, we can solve for that using this equation.

$$1.65V = VSP = \frac{\sqrt{\frac{Bn}{Bp}} * Vthn + (VDD - Vthp)}{1 + \sqrt{\frac{Bn}{Bp}}}$$

The threshold voltages of this process are 0.61V for NMOS and -0.79V for PMOS.

$$1.65V = \frac{\sqrt{\frac{Bn}{Bp}} * 0.61V + (3.3V + 0.79V)}{1 + \sqrt{\frac{Bn}{Bp}}}$$

$$1.65 * \left(1 + \sqrt{\frac{Bn}{Bp}}\right) = 0.61 * \sqrt{\frac{Bn}{Bp}} + 4.09$$

$$1.65 * \sqrt{\frac{Bn}{Bp}} = 0.61 * \sqrt{\frac{Bn}{Bp}} + 2.44$$

$$1.04 * \sqrt{\frac{Bn}{Bp}} = 2.44$$

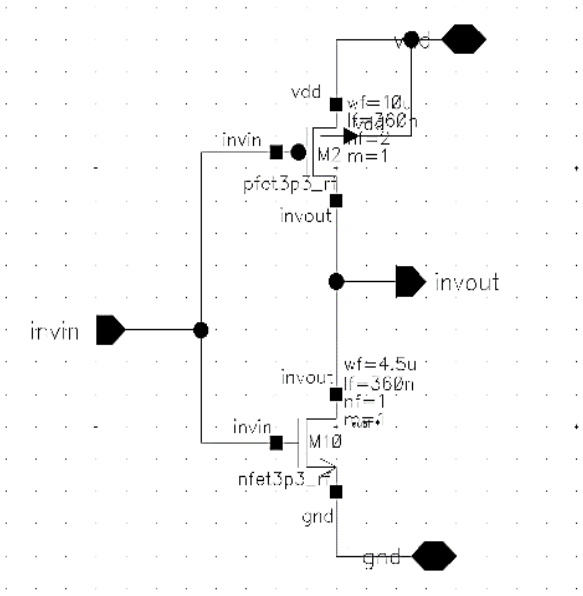
$$\sqrt{\frac{Bn}{Bp}} = 2.346$$

$$\frac{Bn}{Bp} = 5.5037 = Ratio\ of\ Beta\ Coefficients$$

Using this equation, we can estimate the values of the two beta coefficients of the two transistors to give a ratio that can give an ideal switching point of $\frac{VDD}{2}$.

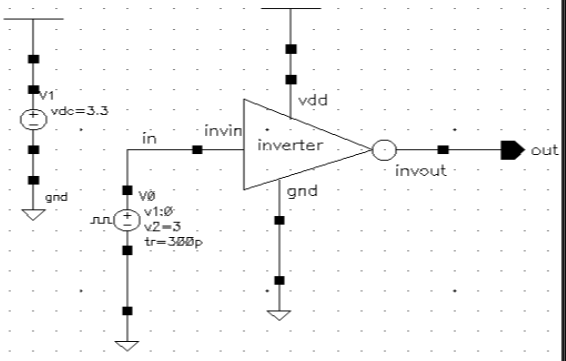
The switching point is found when running a DC sweep from 0 to VDD using 10m linear step size over the input pulse. The switching point of this inverter is 1.66V which is very close to the ideal switching point voltage of $\frac{VDD}{2} = \frac{3.3v}{2} = 1.65v$.

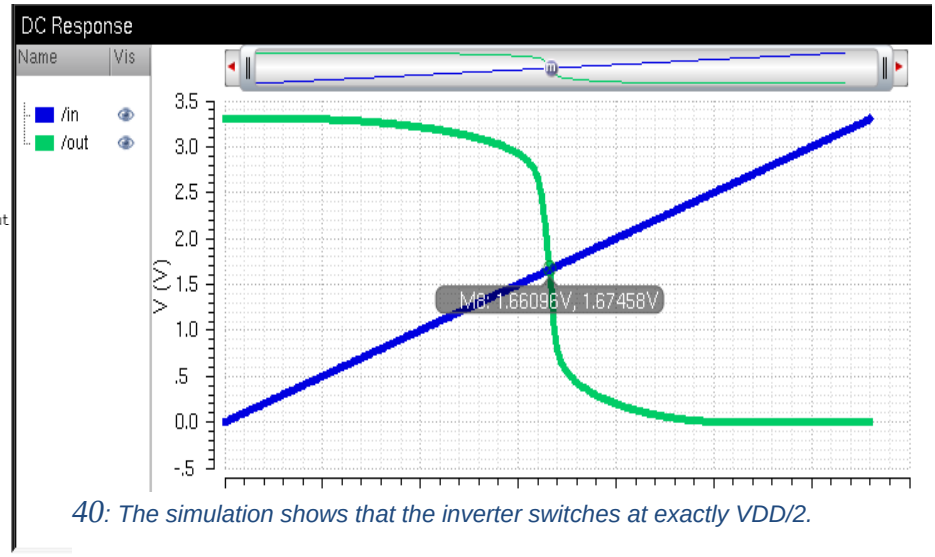
The PMOS is typically sized up because the switching resistance is less than that of the NMOS, so to get them at a proportional point, the PMOS must be larger. The sizes used in my design are PMOS: 10u/360n with a multiple of 2 and NMOS: 4.5u/360n.



39: The RF inverter schematic.

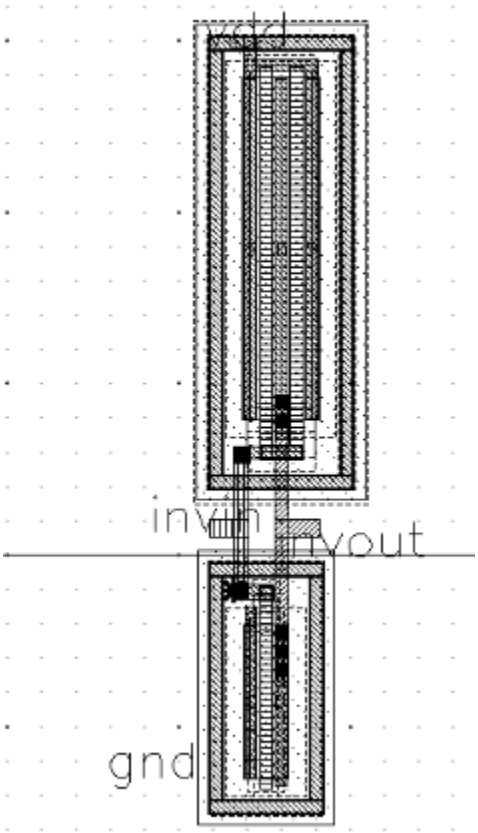
DC Sweep – Inverter's Switching Point



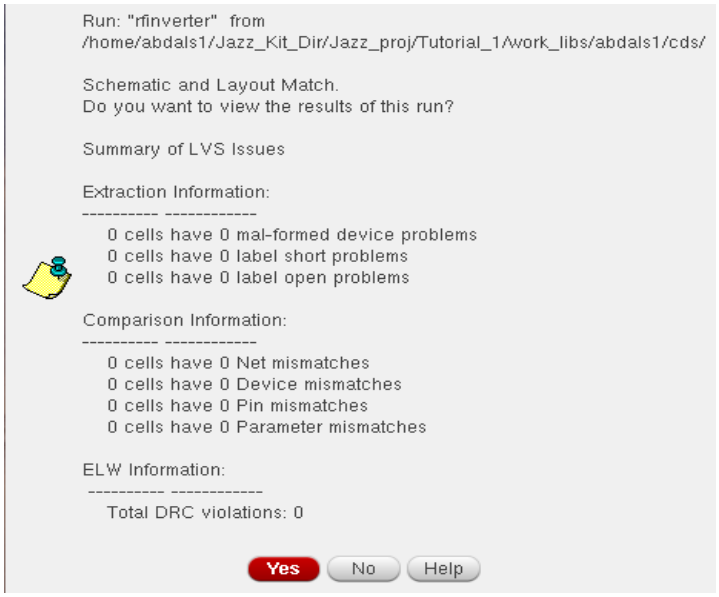


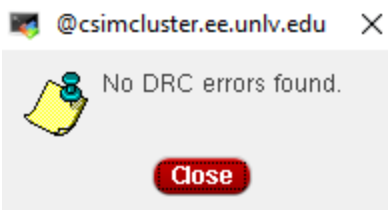
40: The simulation shows that the inverter switches at exactly VDD/2.

RF Inverter Layout



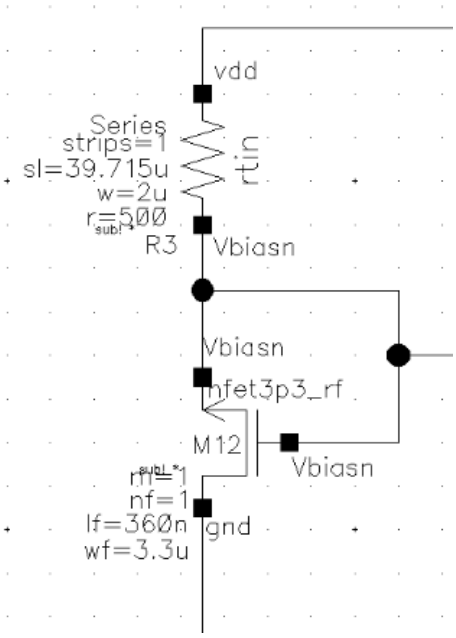
The circuit passes DRC and LVS.





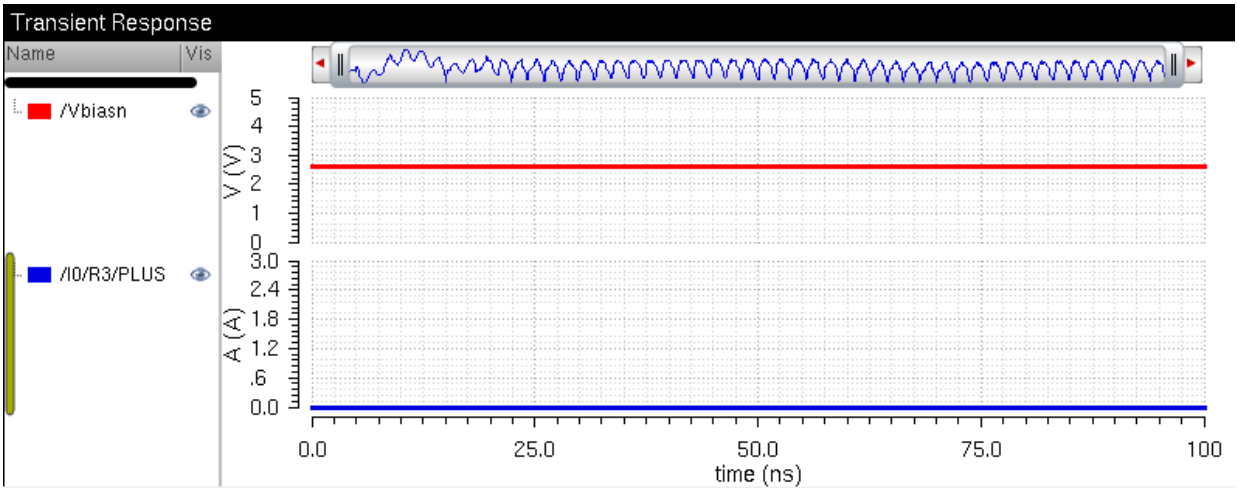
Biasing Circuit and Voltage

The comparator, differential amplifier and source follower circuits require a constant biasing voltage that was generated using a simple biasing circuit consisting of a 500ohm resistor connected to VDD and the drain of a diode connected NMOS. The size of the NMOS is a length of 360n and a width of 3.3u, which is a standard size that is not very large or too small. The biasing voltage generated by this circuit is 2.6V.



Biasing Current Through Resistor: 1.3945 mA

Voltage – Vbiasn: 2.6 V



***41**: Biasing current= 1.3945mA and the biasing voltage is 2.6V.*

DC Power Dissipation

Power dissipation is something that is of less concern in this circuit design because the circuit is to operate in space. Since the power supply will be the sun, it does not matter as much how much power dissipation there is. Using a DC operating point simulation, the power dissipated through VDD can be found. The power dissipation of this circuit is not ideal and is

quite high, however, this is something that will be improved upon in future designs and revisions of this circuit.

Since the system will be in space in the future, the power dissipation is not something that is as much of a concern as the entire operation of the circuit. Since the circuit works under the other conditions, the power dissipation is not an issue.

signal	OP("/V1" "??")
i	-20.6484m
pwr	-68.1396m
v	3.3

Conclusion and Future Work

In conclusion, the circuit achieved its purpose and was able to amplify a small signal at very high speeds. The output swung from rail to rail, from VDD to GND. The gain was about 8k. The LNA was also stable with about an 80-degree phase margin, under all corner simulations when running an AC simulation. The bandwidth was very large, and the circuit operates with frequencies as high as 500MHz to 1.24GHz. The LNA was made using HBTs because inductors were not available for use in this process and the circuit had practical applications.

An issue with the design was that the circuit was not fully able to drive a 150pF capacitive load. In the future, adding a buffer would strengthen the circuit. I would also work to reduce the layout size because the layout was much larger than expected. Since this chip will be due in March, there is time to improve the strength of the circuit.