SACHIN P NAMBOODIRI

Las Vegas, Nevada - 89119 | sachinpnamboodiri@gmail.com | (484) 560-3265 | Webpage: Sachinpn

EDUCATION

- PhD in Electrical Engineering — December 2020
  University of Nevada, Las Vegas, USA with **GPA of 3.9/4**
- Master of Science in Computer Engineering, — December 2015
  Villanova University, USA with **GPA of 3.87/4**
- Bachelor of Technology in Electronics and Communication Engineering, — May 2012
  Amrita Vishwa Vidyapeetham University, India with **GPA of 7.6/10**

TECHNICAL SKILLS

EDA tools: Cadence Virtuoso, ModelSIM, Xilinx ISE, Altera

HDLs: Verilog, VHDL

Packages/Simulation Tools: MATLAB, Spectre, NI Multisim, LTspice, Labview, and HFSS

Programming Languages**:** C/C++

Printed Circuit Board design and Layout tool**:** Eagle

Assembly level programming language**:** PIC, 8085, 8086

Architectures and Hardware: PIC16F877A microcontroller, W65C02 processor, NIOS II soft processor, USB protocol and architecture

EXPERIENCE

Research assistant, University of Nevada, Las Vegas — March 2017 – December 2020

Geiger Mode SiGe Receiver for Long-Range Optical Communications (funded by **NASA**)

- Development of a novel high speed Geiger-mode integrated optical receiver for space based LiDAR missions
- Characterizing avalanche photodiode (APD) & silicon photomultiplier (SiPM) **in TowerJazz 180nm SiGe BiCMOS process**
- Implementation of current-mode **Readout ICs (ROICs)** for 500Mb/s count rate and 24µA - 1.35mA input range
- Design of **heterojunction bipolar transistor (HBT)** based transimpendence amplifiers (TIA) and current conveyors
- Design of time to digital converters (TDC) with tunable resolution of 500ps to 700ps
- Testing and debugging in the lab that includes PCB design and lab equipment experiences

Research and Development, Villanova University — August 2013 – December 2015

The design and implementation of multiple parallel integrated neural amplifiers in submicron CMOS using area-efficient pseudo resistors for RC filtering. **(Done in collaboration with the University of Pennsylvania)**

- This system focuses in developing **brain computer interface (BCI)** with sensing and actuation to drive prosthetic limbs
- Designed a low noise ($7\mu V_{rms}$), fully compensated neural front-end amplifiers (OTA) in **IBM7RF 180nm process**
- Developed an area efficient tunable pseudo resistor useful for low frequency filter applications
- Extensive testing was conducted on the fabricated OTA chips and validated the simulation results

Electrical Engineering Summer Intern, Florida Research Instruments, FL — May 2014 - August 2014

Worked in the implementation of Non-Invasive Blood Pressure Analyzer circuit.

- Developed a new method for monitoring blood pressure using .tdms files and Labview
- Comparison of the results with the commercial Omron BP meter
- Designed experiments and reference documents to demonstrate in **Labview**
- Create lab lectures and discussion material of the same for the coursework **Biomedical System Design(ECE5255)** for **Villanova University**.

Research Associate, Humanitarian Technology Labs, Amrita University, India August 2012 - July 2013

Worked in an IEEE funded project Intelligent Automatic Navigation System for Elderly and Physically Challenged.

- Implemented (LARN) Dijkstra's algorithm in MATLAB and analyzed the performances in both intel i3 and i5 processors
- Hardware testing and verification of the complete system to validate the intelligent navigation
- Worked as teaching assistant for **Digital Design using verilogHDL (EC333)**

PUBLICATIONS

- **Namboodiri, S. P.**, Arteaga, G., Skelly, J., Mata-carlos, F., Roy, A., and Baker, R. J., "A Current-Mode Photon Counting Circuit for Long-Range LiDAR Applications," in the proceedings of IEEE 63rd International Midwest Symposium on Circuits and Systems, August 9-12, 2020.
- Vinayaka, V., **Namboodiri, S. P.**, Roy, A., and Baker, R. J., "Segmented Digital SiPM," in the proceedings IEEE 62nd International Midwest Symposium on Circuits and Systems, August 4-7, 2019
- Mellott, J. K., Monahan, E., Vinayaka, V., **Namboodiri, S. P**., Roy, A., and Baker, R. J., "Variable Fast Transient Digitizer," in the proceedings of IEEE 62nd International Midwest Symposium on Circuits and Systems, August 4-7, 2019
- V. Vinayaka, **S. P. Namboodiri**, S. Abdalla, B. Kerstetter, F. Mata-carlos, D. Senda, J. Skelly, A. Roy, and R. J. Baker, "Monolithic 8x8 SiPM with 4-bit Current-Mode Flash ADC with Tunable Dynamic Range," in the Proceedings of GLSVLSI '19: 2019 Great Lakes Symposium on VLSI, May 9-11, 2019, Tysons Corner, VA, USA. ACM, New York, NY, USA
- **S. P. Namboodiri**, H. Zhu, L. Khuon, J. Van der Spiegel and R. Caverly, " Low Cutoff Frequency Integrated Neural Amplifiers Using Symmetrical Pseudo Resistors ", in the Proceedings of 42nd Annual Northeast Bioengineering Conference, Binghamton, NY, April 5-7, 2016.

ACADEMIC PROJECTS

Design of delta-sigma KD1S ADC using **ON's 500nm CMOS process** March 2018-May 2018

- First and second order delta-sigma modulators were designed and analyzed
- Incorporation of chopping techniques to achieve high signal to noise ratio (SNR)
- SNR of 64dB and an ENOB 10.4 bits achieved for second order topology

Voltage controlled Oscillator (VCO) using **AMS's 350nm SiGe BiCMOS process** March 2018-May 2018

- Designed a cross-coupled LC oscillator
- Frequency range of 2.3GHz-2.5GHz achieved using varactor
- Phase noise of -123$dBc/\sqrt{Hz}$ at 100kHz frequency offset

Transimpedence amplifier using **AMS's 350nm SiGe BiCMOS process** March 2018-May 2018

- Designed a BiCMOS based TIA with a gain of 105dB and 150MHz Bandwidth
- Incorporation of tuning circuits to vary the transimpedence gain
- Input referred noise of 5pA/$Hz_{1/2}$ is achieved

Low Voltage Operational amplifier using **ON's 500nm CMOS process** March 2017-May2017

- Open loop gain of 80dB with a gain bandwidth product of 1MHz is achieved
- Designed with input CMR extending above VDD and ground rail
- Employed indirect compensation techniques to attain 90dB CMRR and 70 deg phase margin

Synchronous Buck converter using **ON's 500nm CMOS process** October 2016-December 2016

- Constant supply of 2.5V generated using off chip inductors and capacitors
- Performance analyzed for voltage and temperature variations
- Incorporation of Zero Voltage Switching (ZVS) for better efficiency

32-bit Parity Generator in **TSMC's 250nm CMOS process** January 2015-May 2015

- Design and analysis of XOR gate performance using different circuit topologies
- Designed the complete circuit with minimal propagation delay and power
- Layout and extraction of the complete circuit