Low Cutoff Frequency Integrated Neural Amplifiers Using Symmetrical Pseudo Resistors

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***Abstract*— This paper discusses integrated neural amplifier design in the context of using various pseudo resistor topologies to achieve low cut-off frequencies and on-chip area efficiency. Pseudo resistors are high resistance devices derived from specific MOSFET transistor topologies that are biased in the sub-threshold region. These structures can be useful for designing on-chip filters with large time constants without the space requirement normally associated with physically large passive on-chip resistor and capacitor devices. Therefore, the low cut off frequency of the neural amplifier is mainly dependent on the resistance value of the pseudo resistor structure. A test chip has been fabricated in IBM 180nm CMOS technology to analyze the amplifier's performance. It has been inferred that using symmetrical pseudo resistors give the best performance. The neural amplifier has a low cut off frequency of 0.5-1 Hz with a midband gain of 45dB and an input referred noise of 8.9μV_{rms}.**

I. Introduction

In-vivo extracellular neural-signals show small amplitude and large dynamic range (5μV-5mV) over wide bandwidth (sub-Hz to 10kHz) with high DC level variation. These requirements demand that the neural recording front-end circuits have large gain, good common-mode rejection, and DC blocking. There are many challenges associated with the design of such implantable devices. First, the noise performance associated with these devices has to be in the acceptable levels; and secondly, power consumption has to be minimized in the design of implantable devices.

Many approaches have been discussed in the literature with various solutions offered to address these issues. The design in [1] is one of the popular ones that simultaneously minimize power with acceptable noise levels.

Another important challenge associated with the design of the neural interface is the capture of signals that are in the range of sub-hertz. Sensing in the sub-hertz frequency range requires large resistor and capacitor values to provide a large circuit RC time constant. Since capacitors require a considerable amount of space on an integrated circuit (IC), large resistance values allow a reduced capacitor footprint design.

Different MOS configurations have been proposed to realize high value resistors [1, 2]. A pseudo resistor is an area efficient MOSFET device that achieves very high on-chip incremental resistance values. The pseudo resistor configuration of [1], which consists of two series connected PMOS devices, has been often used. However, the performance of this topology can vary with different technologies. References [2, 3], despite having lower power consumption and minimal noise, have low cut off frequencies in the range of tens of Hertz.

This paper considers the above issues, presents various pseudo resistor topologies that are compatible for realizing low cut off frequency, and implements an integrated neural amplifier utilizing a wide voltage range symmetrical pseudo resistor topology. Section II provides brief discussion of different pseudo resistor topologies. Section III then details the design of the neural amplifier utilizing these topologies. Section IV presents and discusses the experimental results. Section V concludes the paper.

II. Pseudo Resistors

As discussed previously, pseudo resistors can play an important role in realizing a low cut off frequency of the neural amplifier. Topology A shown in Fig 1 is the conventionally used pseudo resistor topology [1]. Even though that is the case, the performance of pseudo resistor topologies can vary as discussed above. Moreover, it should be noted that Topology A behaves differently depending on the polarity of the voltage applied [4]. This asymmetric behavior can be a reason for the varied performance. Similarly the same issue can occur for the asymmetric Topology B of Fig 1.

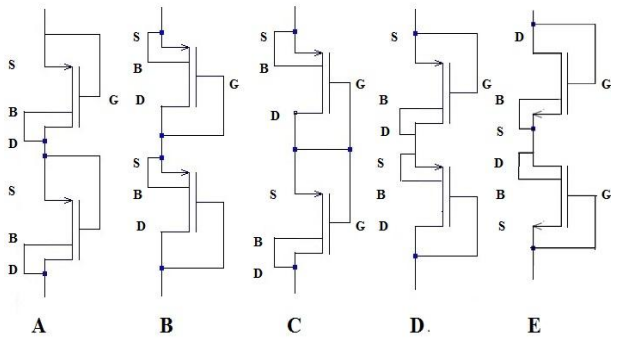

Fig. 1 Pseudo Resistor Topologies

The above discussed problems associated with pseudo resistors can be resolved by using the proposed symmetric topologies C, D and E as shown in Fig 1. These structures are similar to the previous ones except that the MOS devices are connected in opposition to each other. In these topologies, the MOS devices are placed in such a way that the complete

structure behaves symmetrically independent of the voltage polarity. It can also be observed that the neural amplifier design of Fig 2 utilizes one of these topologies, Topology C.

III. Neural Amplifier

The overall design of the neural amplifier comprises two stages as shown in Fig 2. The first stage of the overall design is a conventionally used Operational Transconductance Amplifier (OTA) design [1]. This stage helps in realizing the important factors like gain, bandwidth and noise performance. The transistors M1 to M4 are the MOSFET based pseudo resistor structures, as shown based upon Topology C, which helps in setting the low cut off frequency of the amplifier. The ratio of capacitors C1 and C2 determines the closed loop gain of the first stage. The second stage consists of a differential pair, which is mainly used to increase the overall gain of the neural amplifier. The ratio of resistors R1 and R2 determines the closed loop gain of the second stage.

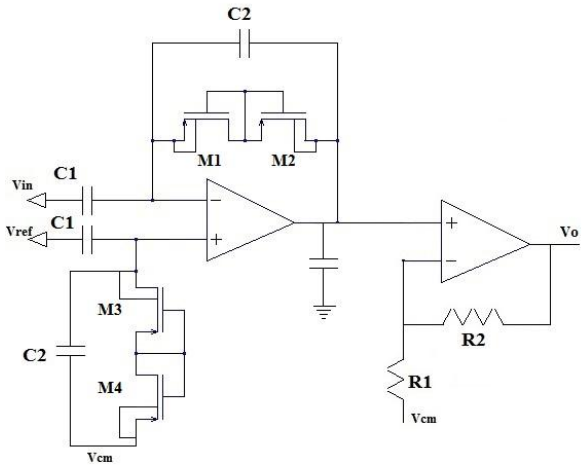

Fig. 2 Neural Amplifier Design

IV. Experimental Results

In order to analyze the performance of the neural amplifier, a test amplifier along with different pseudo resistor topologies were fabricated in the IBM 180nm CMOS process. The measurements were performed using a Keysight DSO 6012A and HP3561A signal analyzer. The amplifier worked with a supply voltage of 1.8V and a bias current of 1µA.

The measured AC response of the amplifier using Topologies A to E are shown in Fig 3. The figure shows that for Topologies A and B, the low cut off frequencies of the amplifier are in the range of 10-20 Hz. This can be due either to the difference in technology or the asymmetric behavior.

Better performance can be observed in the AC response of amplifier using Topologies C, D and E. The measured low cut off frequency of the amplifier using the Topologies C, D and E are 9 Hz, 2 Hz and 1 Hz respectively. It can be inferred that the amplifier using symmetric pseudo resistor topologies will have better performance than that of asymmetric ones. The bandwidth of the amplifier in Fig 2, was measured to be in the range of 5 KHz and the input referred noise was measured to be around 8.9µV_{rms}.

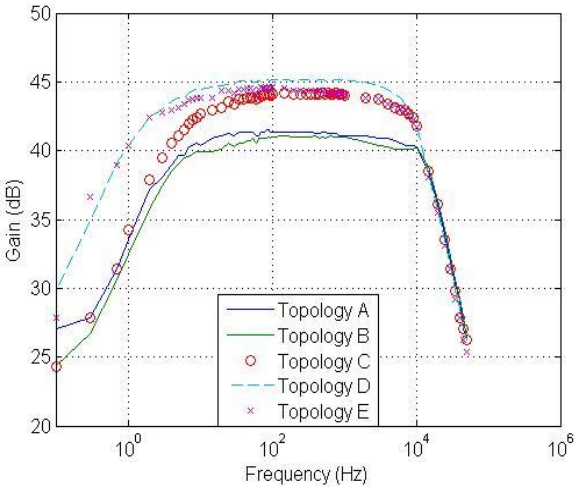

Fig. 3 Measured AC response of neural amplifier

V. Conclusion

The performance of the neural amplifier with various pseudo resistor structures has been studied. Measurement results using implementations in IBM 180nm CMOS technology confirm the behavior of these topologies. The low cut off frequency was found to be less for the amplifier designs using symmetrical pseudo resistor structures. The low cut off frequency with values as low as 1Hz were measured for such topologies. The measured midband gain of the amplifier is around 45 dB with a noise of 8.9µV_{rms}. The proposed symmetric topologies will be useful for on-chip filters that require very low cut off frequency.

VI. References

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