CMOS synchronous Buck switching power supply

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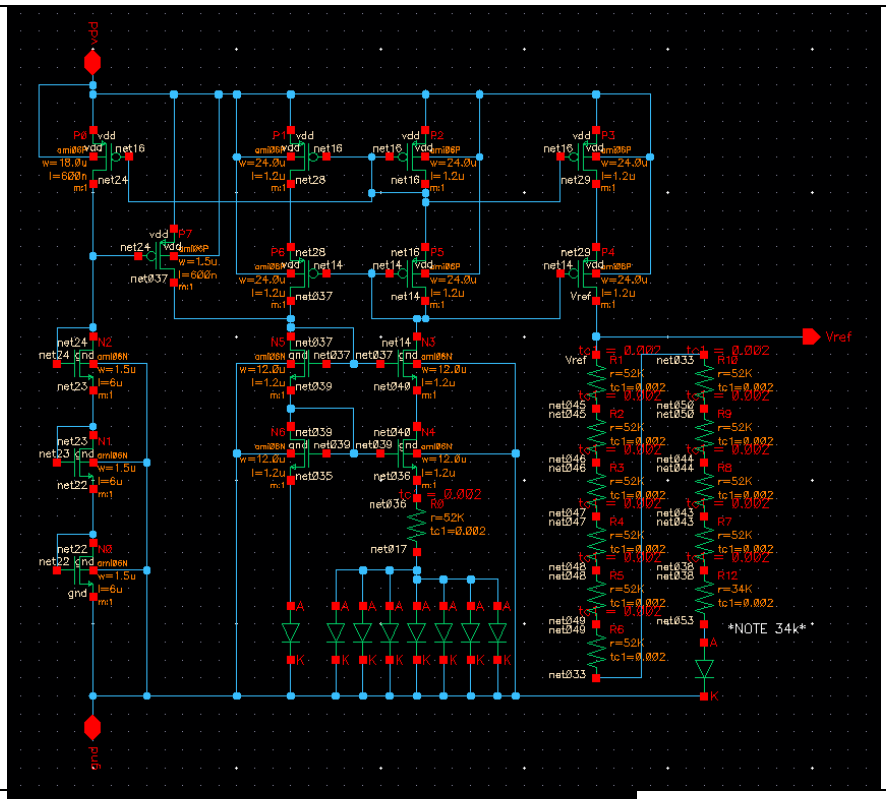
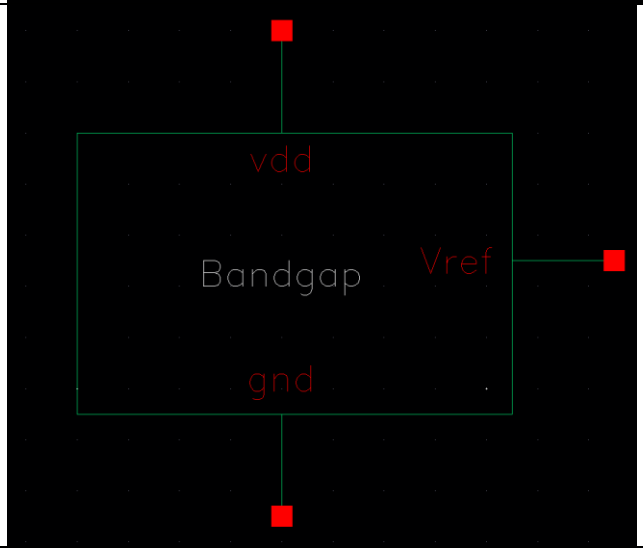
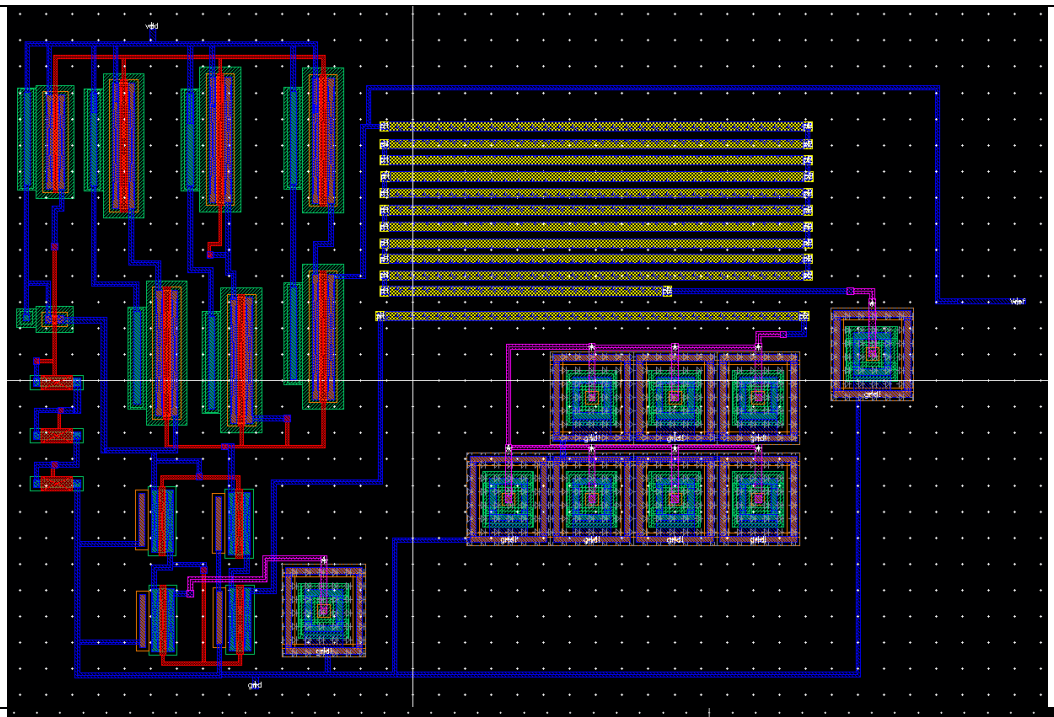
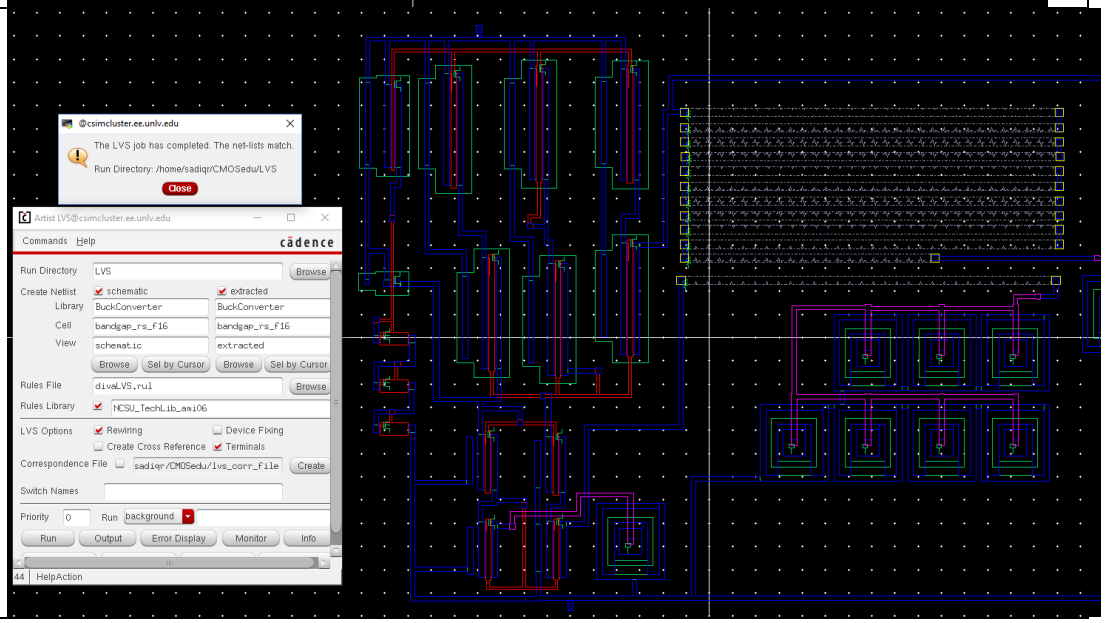
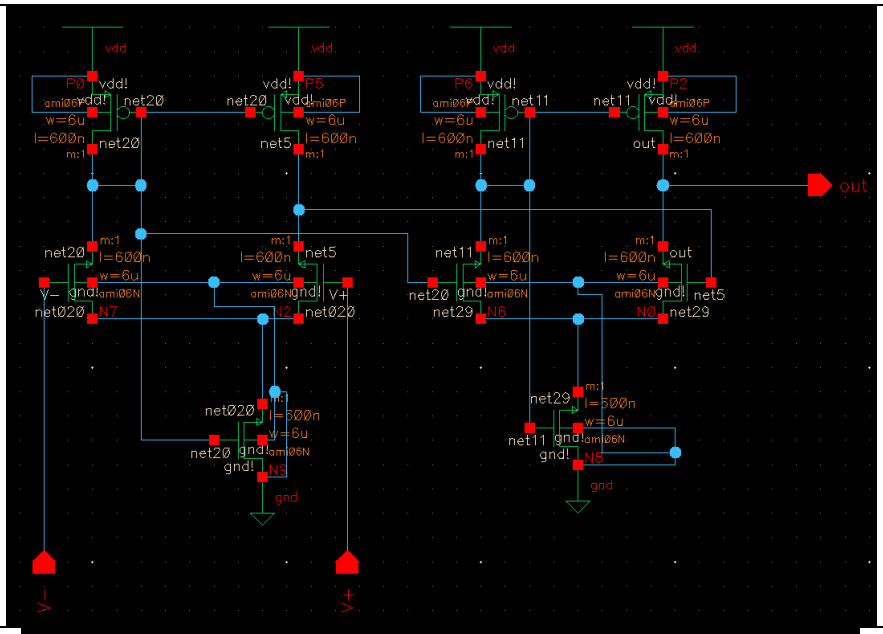
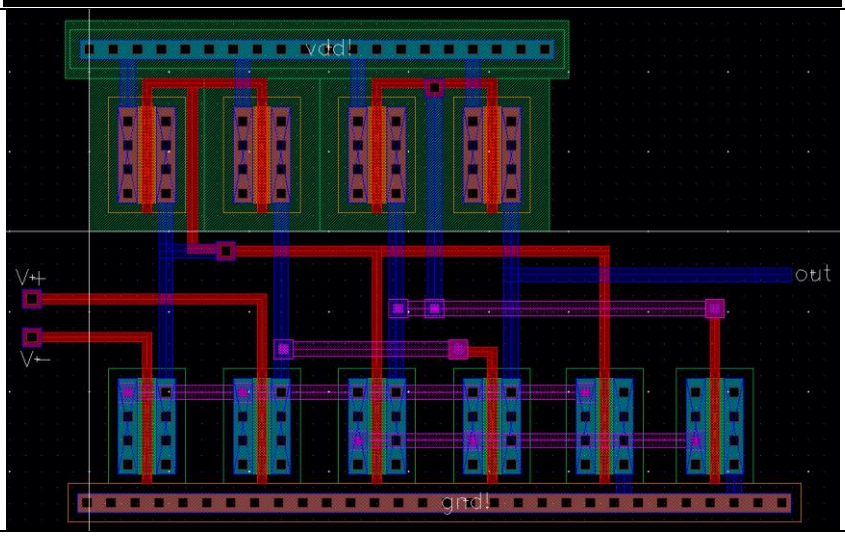
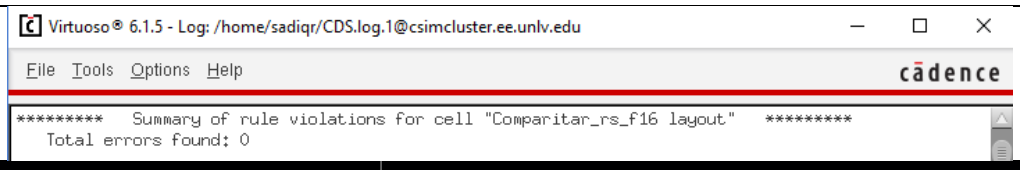
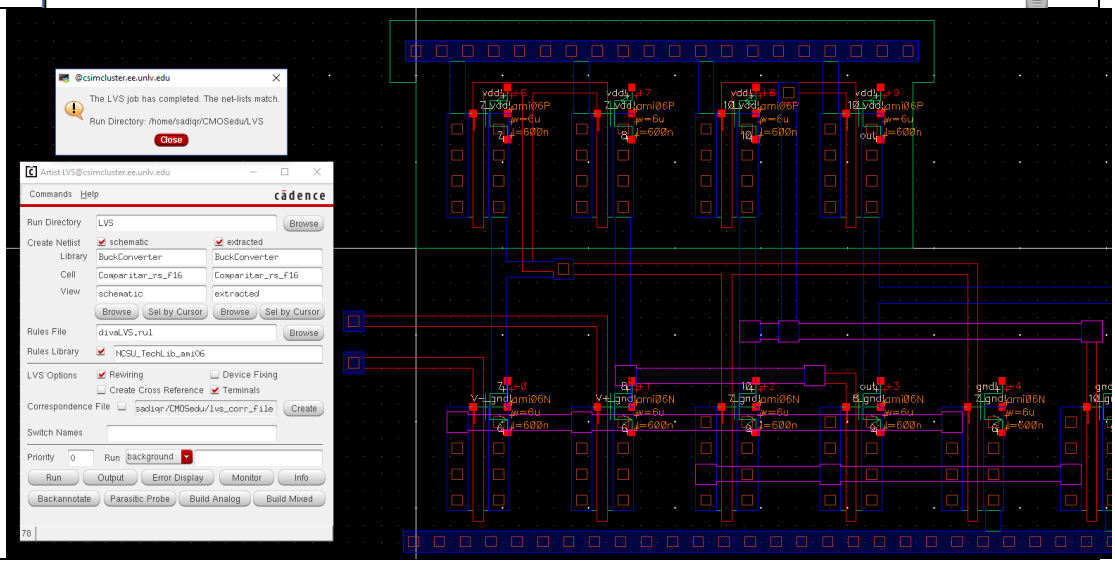
Part 1: This part of the project is to lay out a bandgap. We previously built our bandgap in HW #13 which supplied a constant 1.25 volts. The bandgap that was built should not vary in voltage no matter the temperature of the simulation. The reference voltage stays constant in a bandgap and isn't affected by temperature or varying vdd. Below is the bandgap schematic along with the layout and symbol that will be used in the project.

Schematic:	
Symbol:	

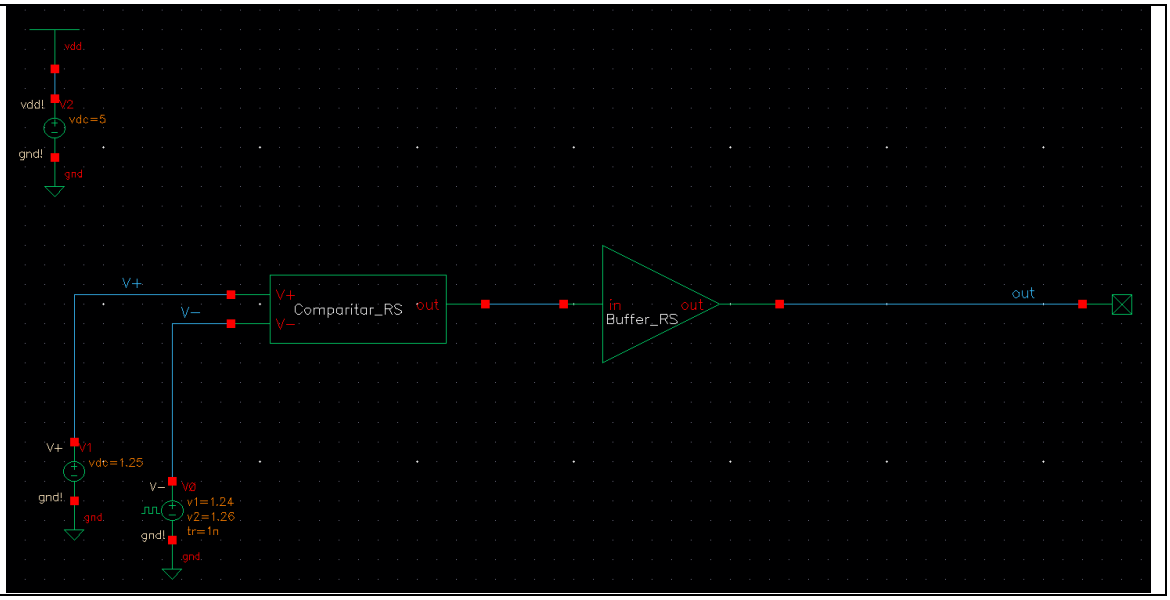
Layout:	
Extracted & LVS:	

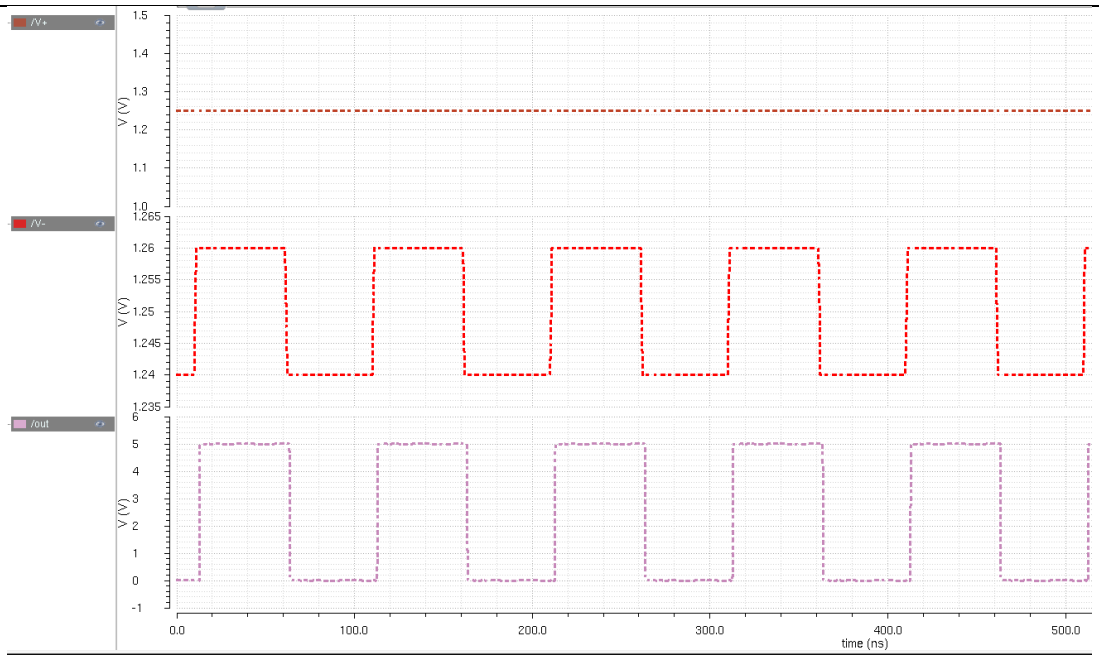
Part 2: This part consists of creating a comparator. The comparator is put into the schematic to help detect voltage when it is below or above 1.25V which is being fed in from our bandgap and feedback voltage. There are two input connections for the comparator. There is the V+ and V-. The V+ will be fed a constant 1. 25 V produced from the bandgap. The job of the comparator is to input two different voltages. If V+ > V-, it will output high. If V+ < V-, it will output low.

Schematic		
Symbol		
Layout		

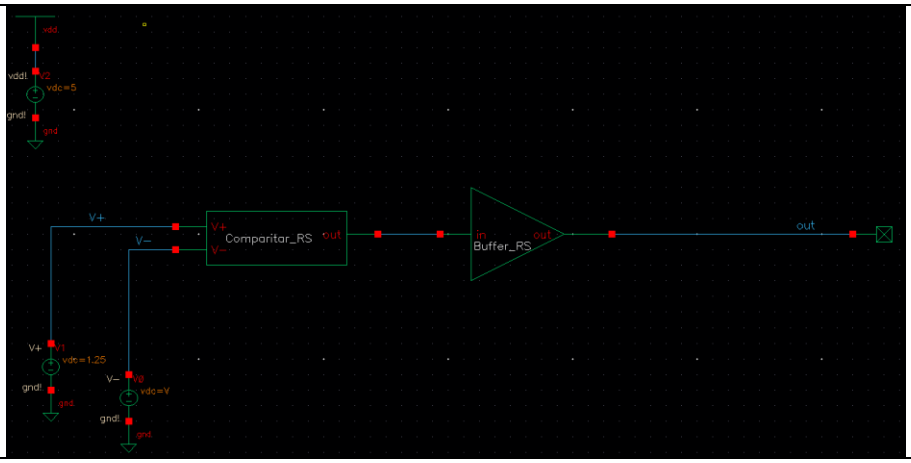
DRC	
Extracted & LVS	

The V- will be fed an impulse voltage that varies between 1.24V and 1.26 V so that we can see closer to what happens around the 1.25V mark. The logic output will be a high or low represented in 5V and 0V(ground). To simulate the comparator I will be using a constant 1.25V source that will be representing the bandgap input and then there will be a vpulse going through V- to show the the range between 1.24V-1.26V.

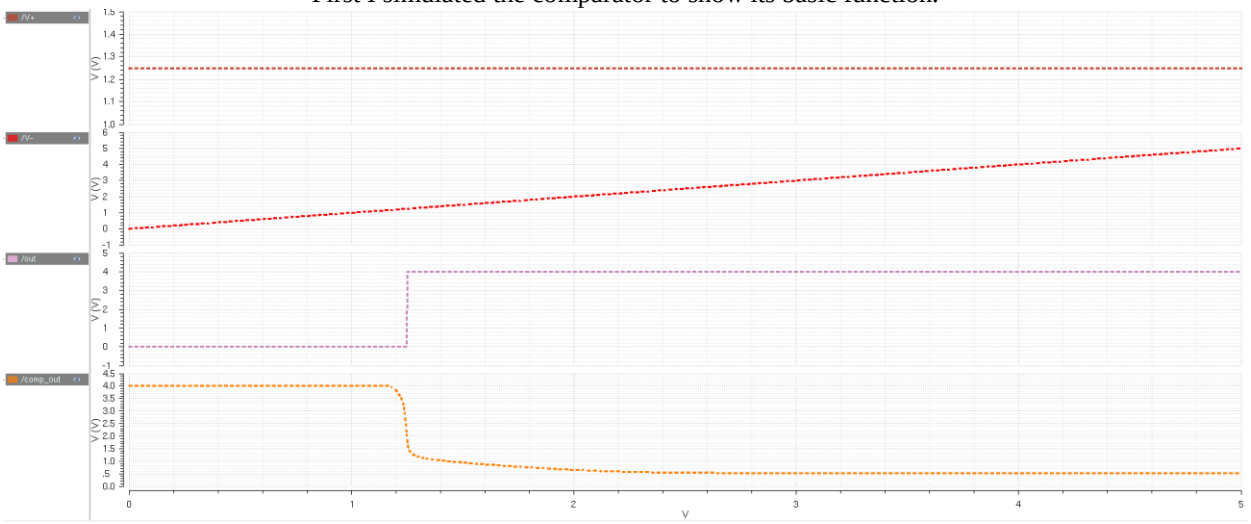
Test Schematic for Comparator	

Simulation	

After that we check for the switching point and gain of the comparator. For my comparator V+ equals Vref. For this analysis there is a constant 1.25V put into V+. For V- we put a variable, V, that is set to a value of 0. From that we are able to sweep the

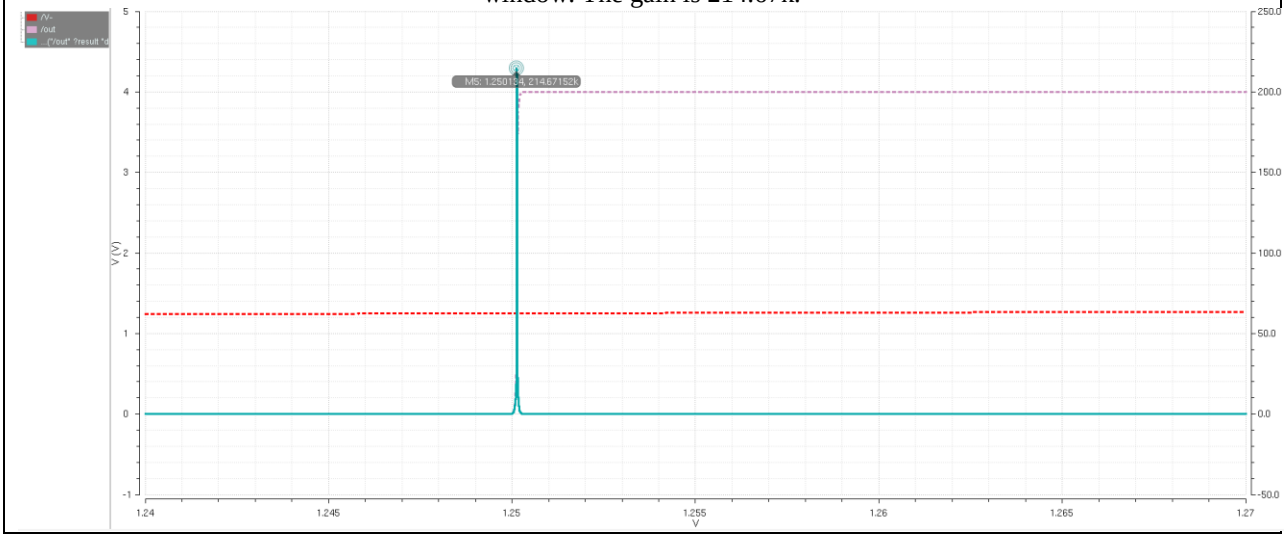
This is the schematic that was used for simulating for the switching point and gain.	

First I simulated the comparator to show its basic function.



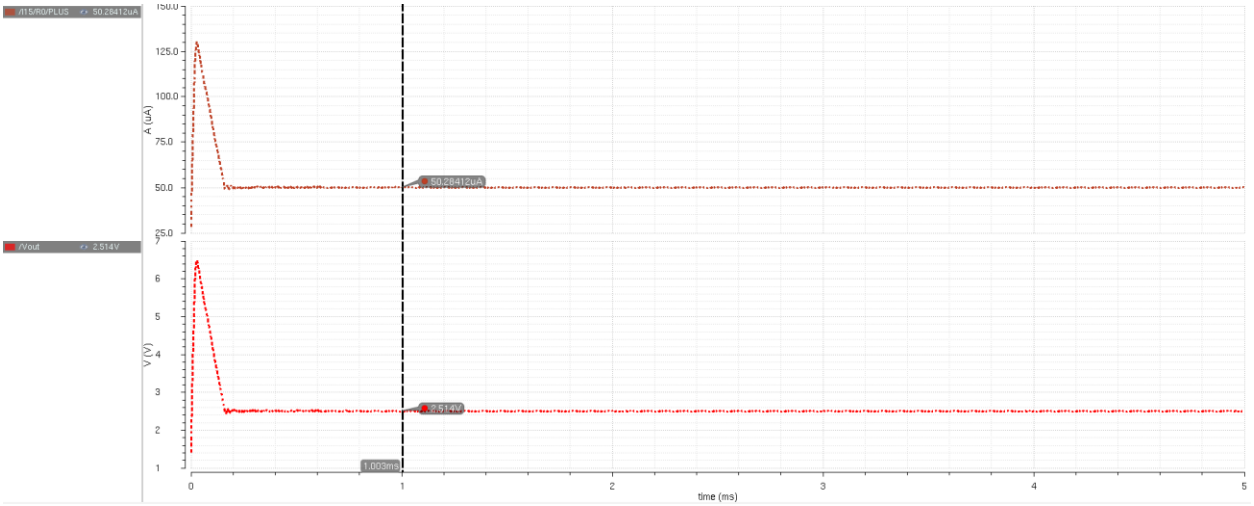
As seen above the V- goes from 0-5V. The V+ stays constant 1.25V because of the bandgap. The comp_out(right out the comparator) and out(output after buffer) should be opposites of each other because I have a three stage buffer.

This simulation shows the gain of the inverter that will be input into the SR latch. The gain can be obtained by taking the derivative of the output signal. This can easily be done through the calculator on cadence simulation window. The gain is 214.67k.



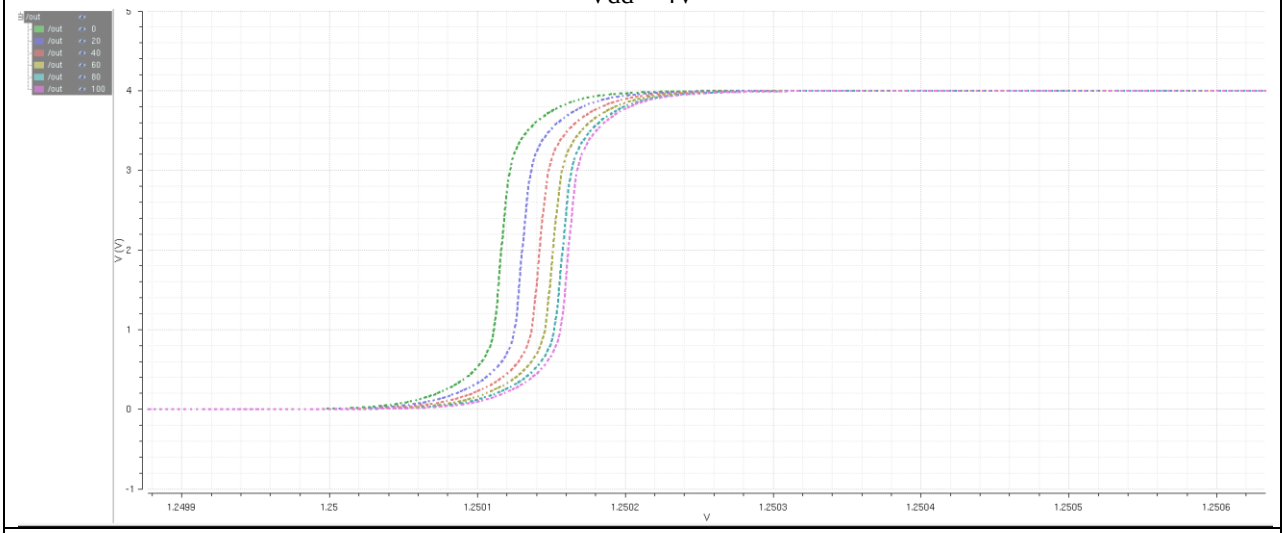
The requirement for the comparator was to draw no more than 50µA and no less than 10 µA. My comparator pulls 50 µA constantly. This can be derived mathematically taking the output voltage, 2.5V, and the two resistors that are set at 25k ohms each in series and equating

$$I_{drawn} = \frac{2.5V}{25K+25K} = 50\mu A$$

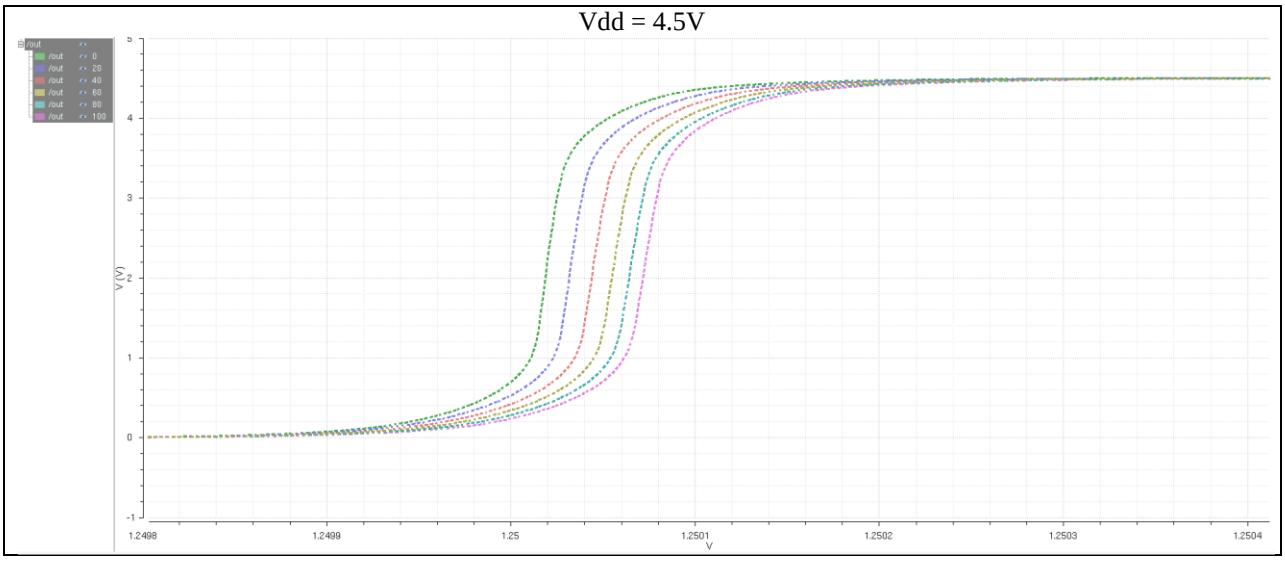


Now we do the simulations for varying the vdd values along with changing the temperature for the comparator and see the changes. Vdd will vary values 4, 4.5, 5, 5.5. The temperature will be 0-100 degrees Celsius in increments of 20 degrees Celsius. It can be seen that the middle of the "no man's land" begins to decrease as the vdd is increased.

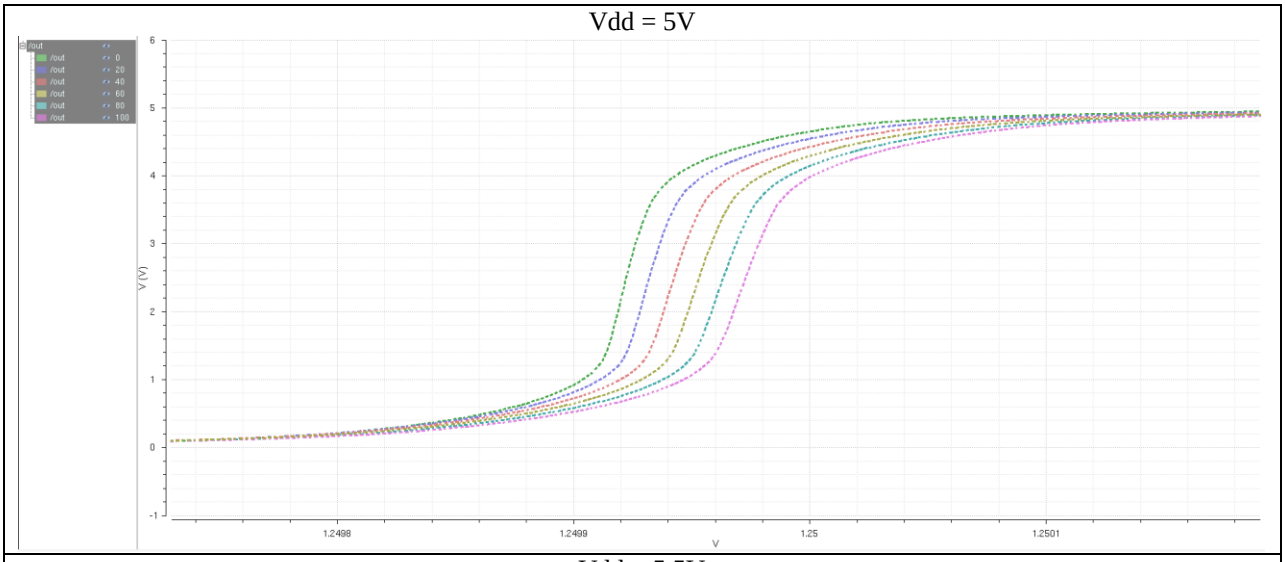
Vdd = 4V



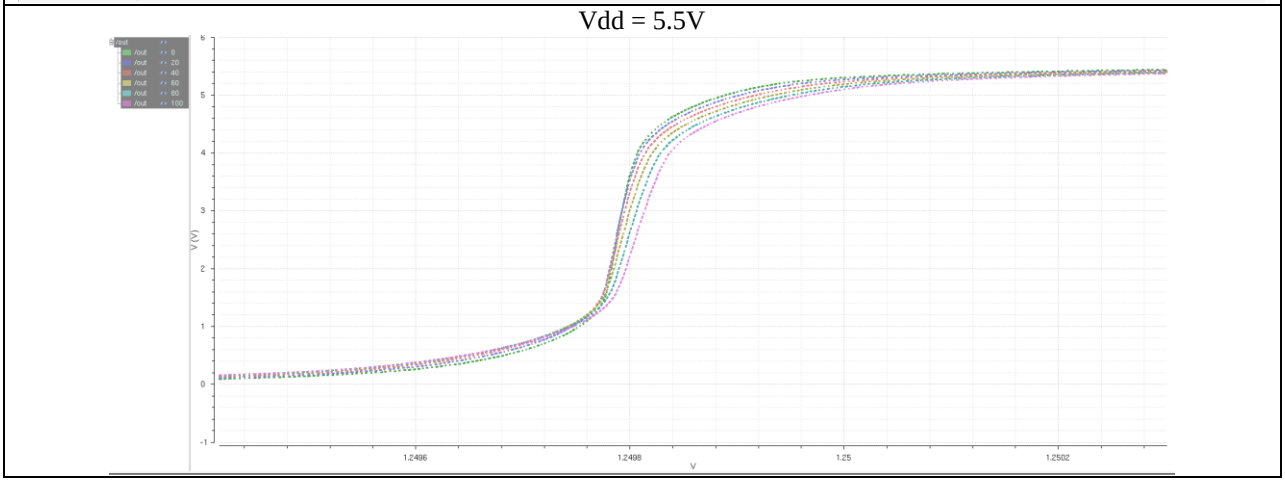
Vdd = 4.5V



Vdd = 5V



Vdd = 5.5V

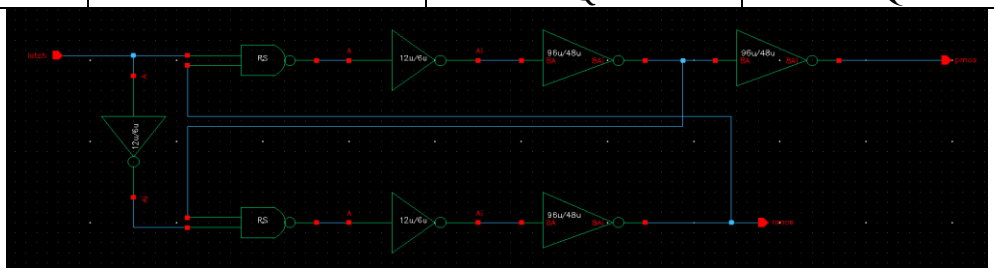


Part 3: We begin to construct a switching regulator which is also known as a SR latch. The SR latch consists of 2 NAND gates and an even number of inverters. The design is to offset the outputs from the latch so that when one of the outputs is on, the other is low. It plays a roll of a non-inverting clock. This comes after our comparator and buffer and before our switching PMOS and NMOS. The reason for the different sizes of inverters in the latch is to amplify current that will be supplied to the NMOS and PMOS. The sizes have to be big enough so that the it can control the current and pass it on. My sizes were 12u/6u and the next stages were multiples of 8, so 96u/48u Below is the SR latch along with the components that were used inside.

SR Logic:

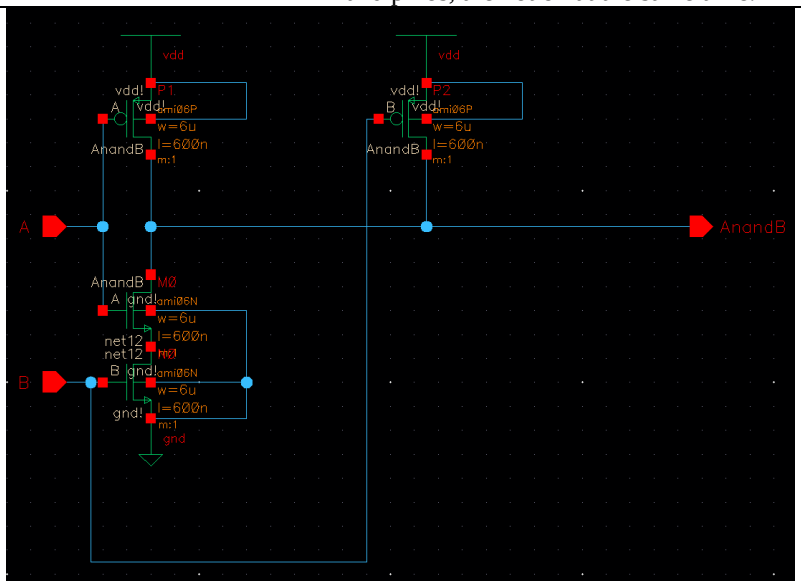
S	R	Q	Q’
0	0	1	1
1	0	1	0
0	1	0	1
1	1	Q	Q’

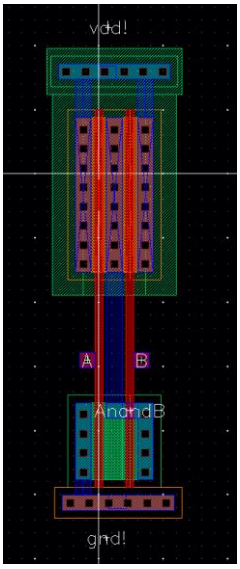
Schematic

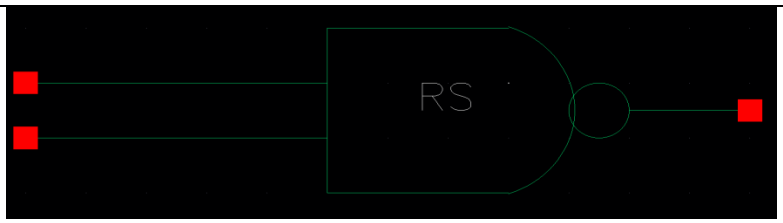
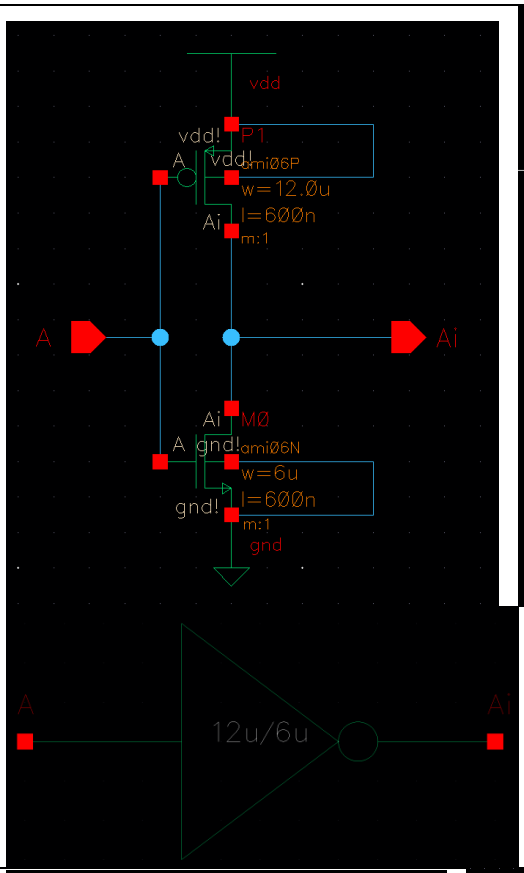
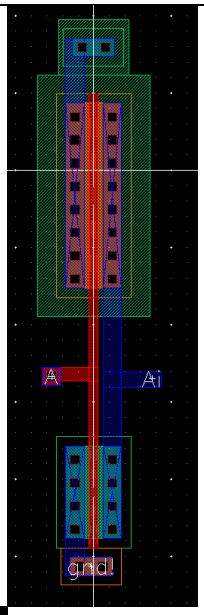
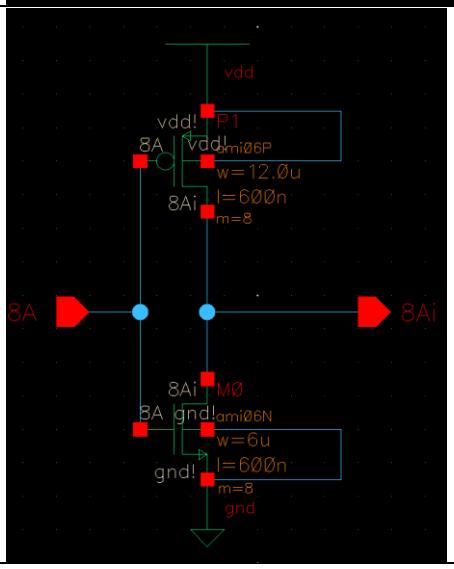
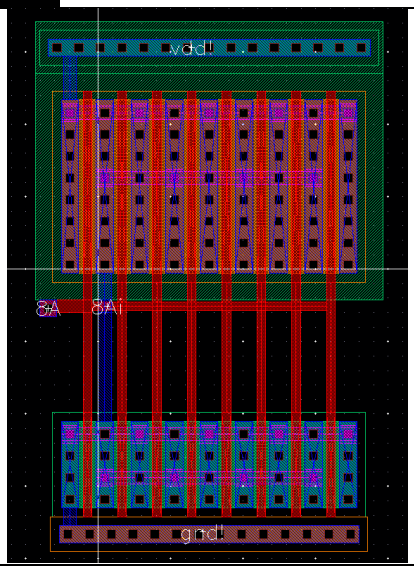


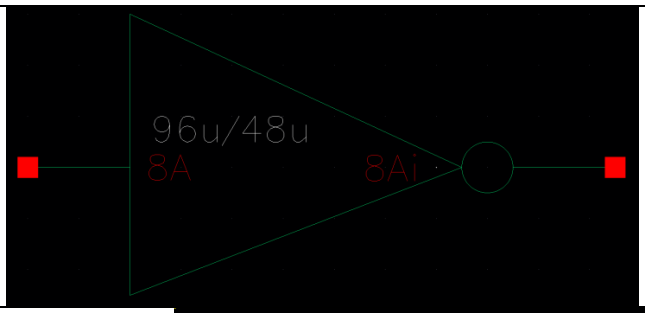
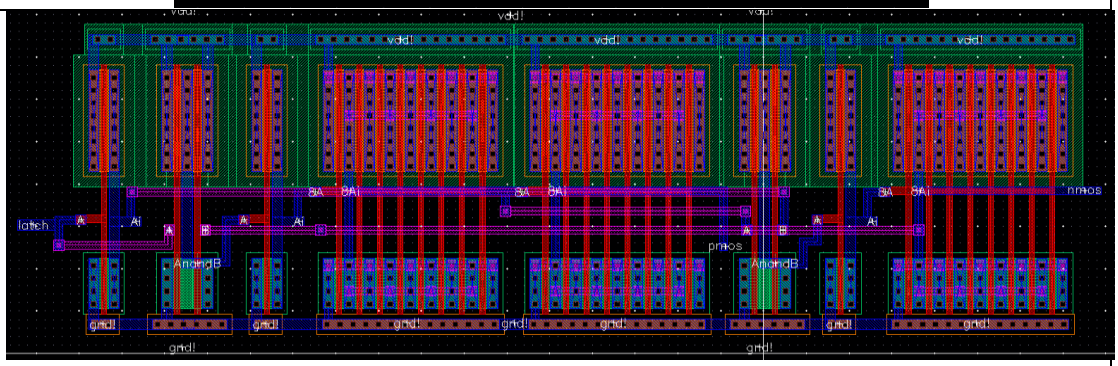
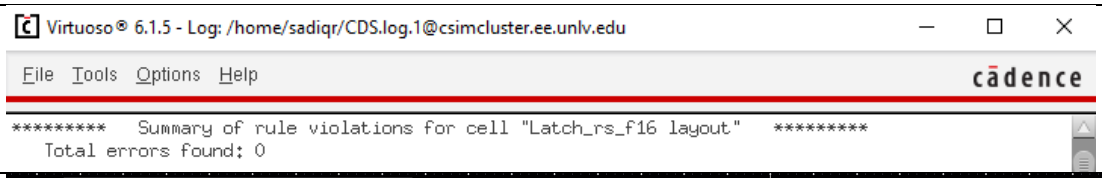
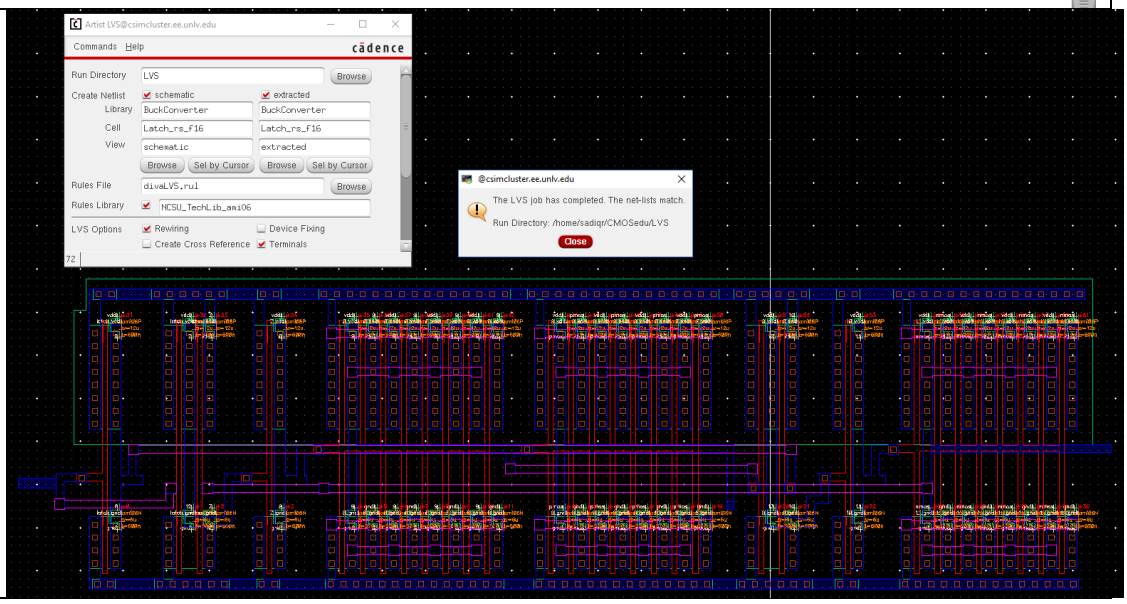
There is an initial inverter that is 12u/6u that is input into our second NAND gate. After the NAND gates there are inverters that were selected to have multiples of 8. First two inverters, top and bottom, are 12u/6u. The next two, top and bottom are 98u/48u. The final third inverter on the top row is 96u/48u as well. The extra inverter up top is to create a delay so that both the outputs, labeled nmos and pmos, are not on at the same time.

NAND gate

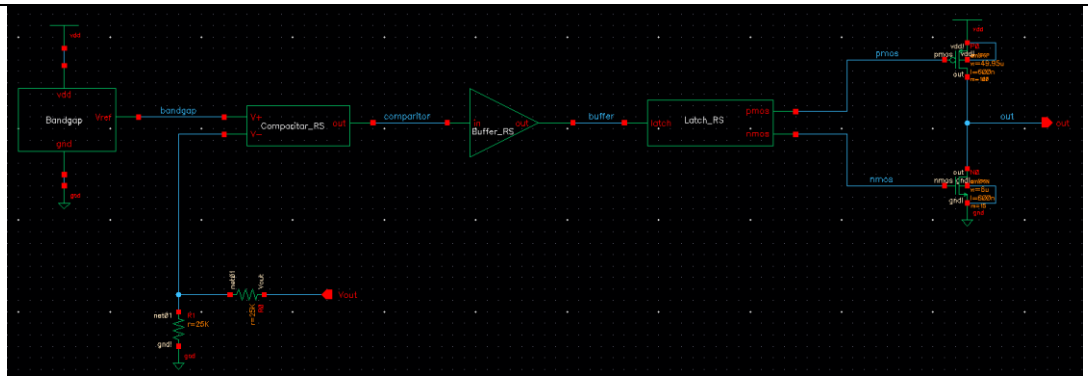
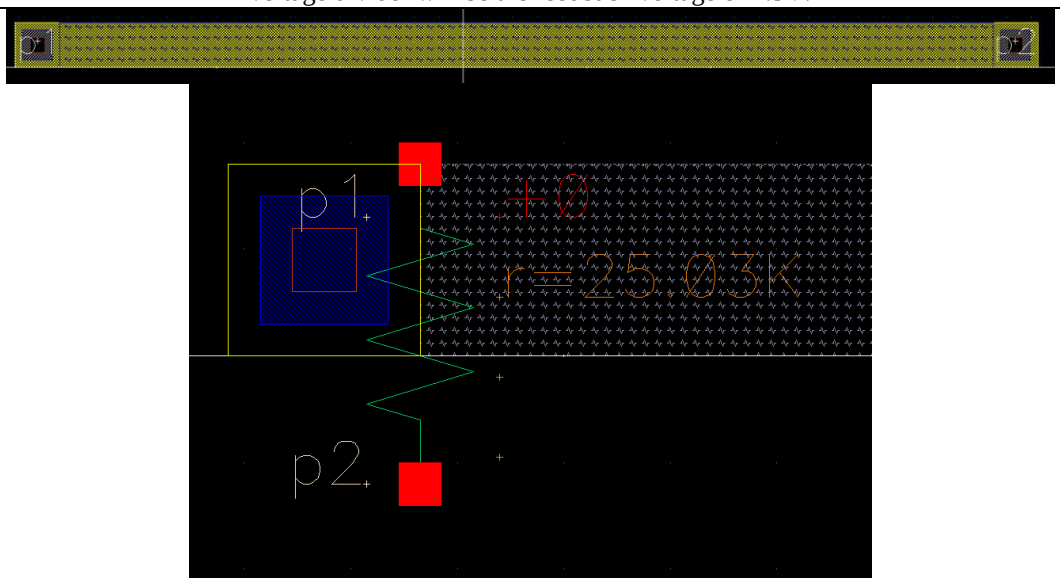




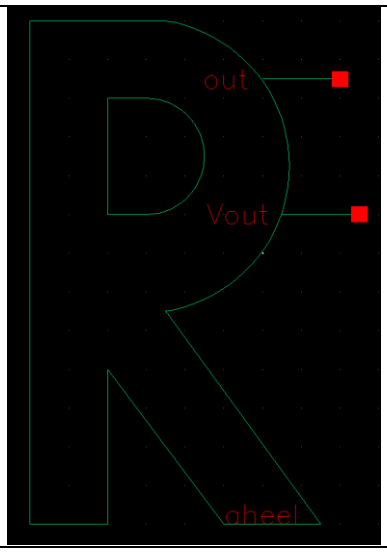
	
12u/6u inverter	 
96u/48u inverter	 

	
Symbol	
Layout	
DRC	
Extract & LVS	

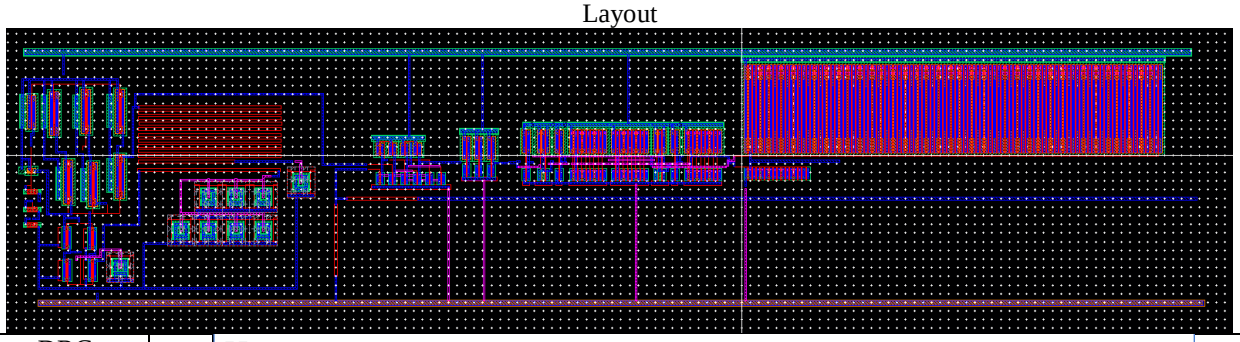
Part 4: Now we construct the synchronous Buck switching power supply. The Buck converter will consist of a bandgap, comparator, buffer, SR latch, driving PMOS, driving NMOS. All those components will then be fed into an inductor and capacitor. There has to be enough current running through the buck converter to support a final 2.5V constant supply which will then be fed back into a voltage divider that consists of two resistors with both valued at 25k ohms. This will be the on chip portion. The off chip portion will consist of an inductor and capacitor. Those will dictate the final Vout to be maintained at 2.5V.

Schematic	 As observed, there is an out pin that will be going into the inductor. The Vout pin connected to the voltage divider will be the feedback voltage of 2.5V.
25k ohm resistor used in schematic	 To obtain the 25k ohm resistor, I used the equation given below to calculate my length. The width is set at 1.8 μ $l = \frac{25k}{1192} * 1.8\mu = 37\mu$

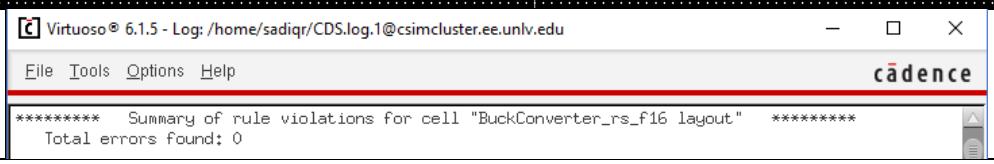
Symbol



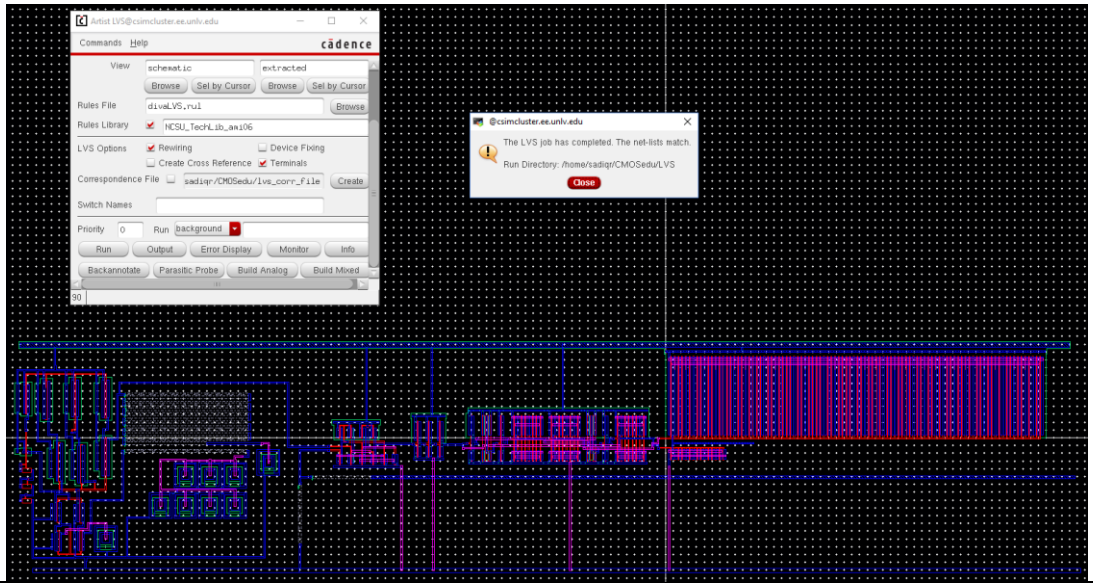
Layout



DRC



Extract & LVS



Now we can add our inductor and capacitor to our Buck converter. The values for the capacitor and inductor were calculated for, but for this particular design, they did not work well and dropped efficiency very low. Because of this, the capacitor and inductor values were changed to various amounts, until a good efficiency was shown. Along with playing with the inductor and capacitor values, the PMOS and NMOS had to be tweaked a little as well.
To start off the calculations for the inductor and capacitor, a frequency range was chosen between 100k Hz and 10M Hz. From this the period was derived

$$100k\ Hz: \frac{1}{T} = 100k => 10\mu s$$
$$10M\ Hz: \frac{1}{T} = 10M => 100ns$$

Also we can derive our duty cycles for when vdd = 4 and vdd = 5.5.

$$D = \frac{2.5V}{4V} = .625$$
$$D = \frac{2.5V}{5.5V} = .4545$$

From that the inductor value can be calculated for using the equation $L = \frac{D*T*V_{dd}-V_{out}}{I_{max}-I_{min}}$

$$L = \frac{.4545(100n)(5.5-2.5)}{1.1mA - .9mA} = 681.7\mu H$$

$$L = \frac{.625(10\mu)(4V-2.5V)}{110mA - 90mA} = 468.7\mu H$$

Now we calculate for time which can be taken from $T = \frac{.2m(681.7\mu)}{.4545(1.5)} = 14.54\mu s$
To calculate for the capacitor we use the given equation $C = \frac{I*T}{V}$

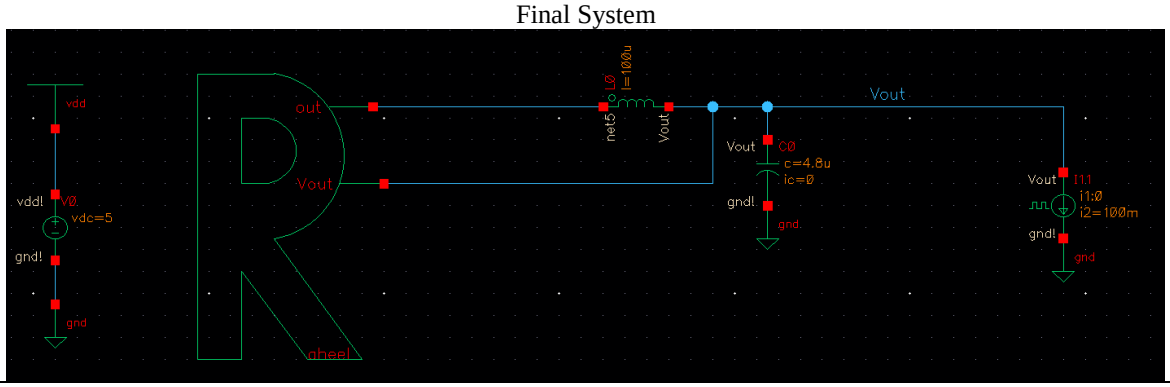
$$C = \frac{14.543\mu s * 100mA}{2.5V} = 5.8\mu F$$

So the initial calculated values for the inductor and the capacitor were 5.8 μF and 681.7 μH. I began by implementing these values to work with my Buck converter. Unfortunately they did not fit well with the design and messed a lot of things up, especially the efficiency. To fix the efficiency and achieve the final design, the final PMOS and NMOS still had to be chosen. Those were chosen at an arbitrary value. The PMOS was set at 50u/.6u with a multiple of 100 and the NMOS was set to 6u/.6u with a multiple of 15. These values were not the initial values chosen. These values were a result of a lot of trial and error. The inductor, capacitor, PMOS, and

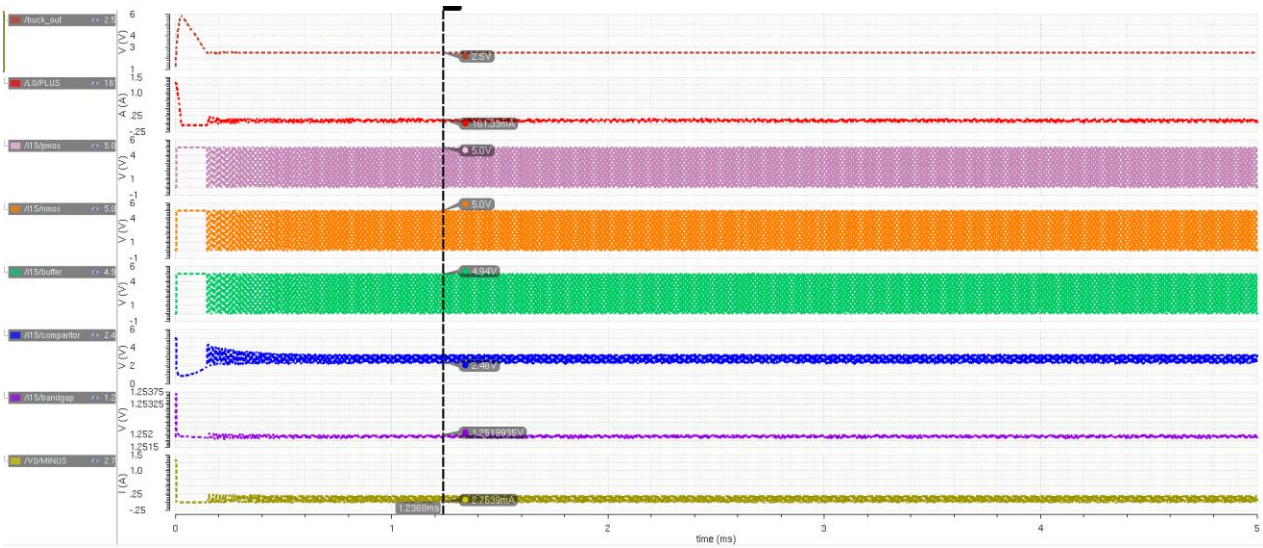
NMOS had work hand in hand to bring up the efficiency of the design. The weaker the PMOS is the less current was supplied to the inductor and capacitor which would end in lower efficiency. The stronger the NMOS were the more current came through, but then the inductor and capacitor had to set at the right values to accommodate for the current out of the buck converter.

The original values calculated for the system were 5.8 μF and 681.7 μH, but since the system would not work well under these values, the values had to be changed a little. From changing the values, the final values for the inductor and capacitor came out to be 100μH and 4.8μF.

Final System



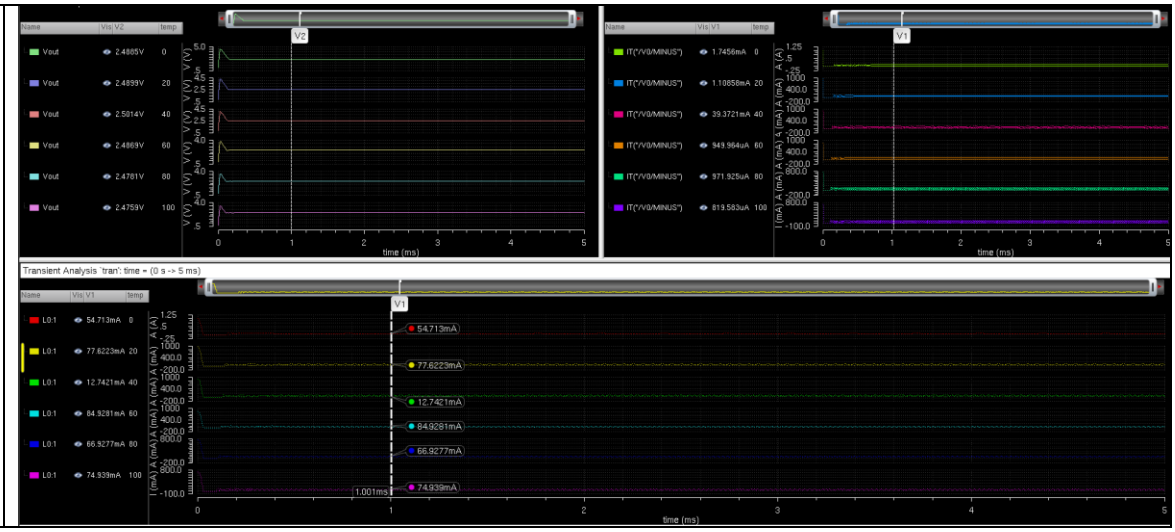
Below is the simulation that shows how everything is operating through the whole system under a pulsing current between 0mA-100mA. It can be seen that everything works as it should be. The output of the bandgap(purple) shows that it outputs a constant 1.25V. Then the comparator(blue) shows that there is an oscillating output voltage, but the average will stay around 2.5V. After that it is input into the buffer which oscillates between 5V-0V. Then we can see that the PMOS(pink) and NMOS(orange) end up receiving a high and low, which is 5V and 0V, through the latch and thus outputting a final constant 2.5V through the whole system.

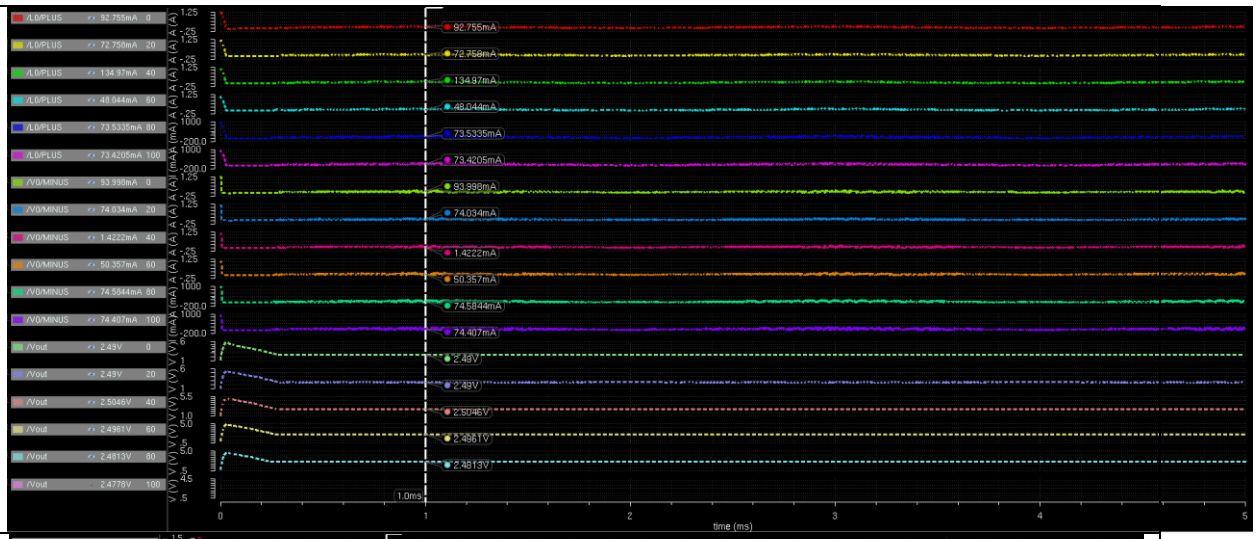
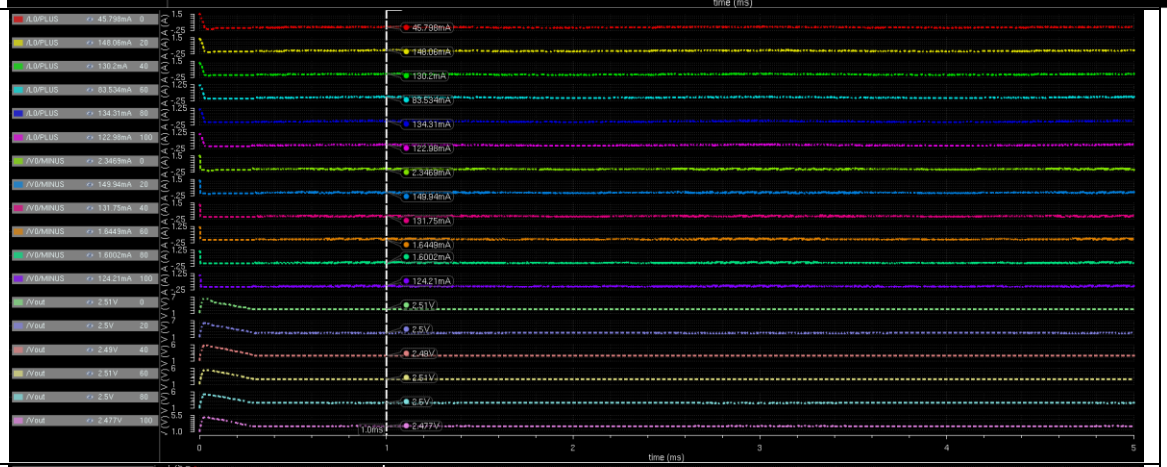
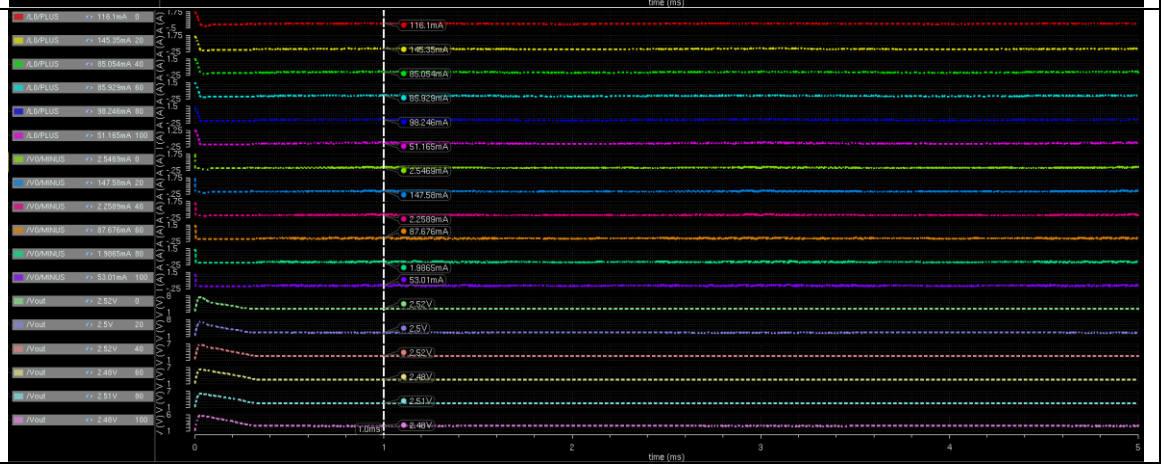


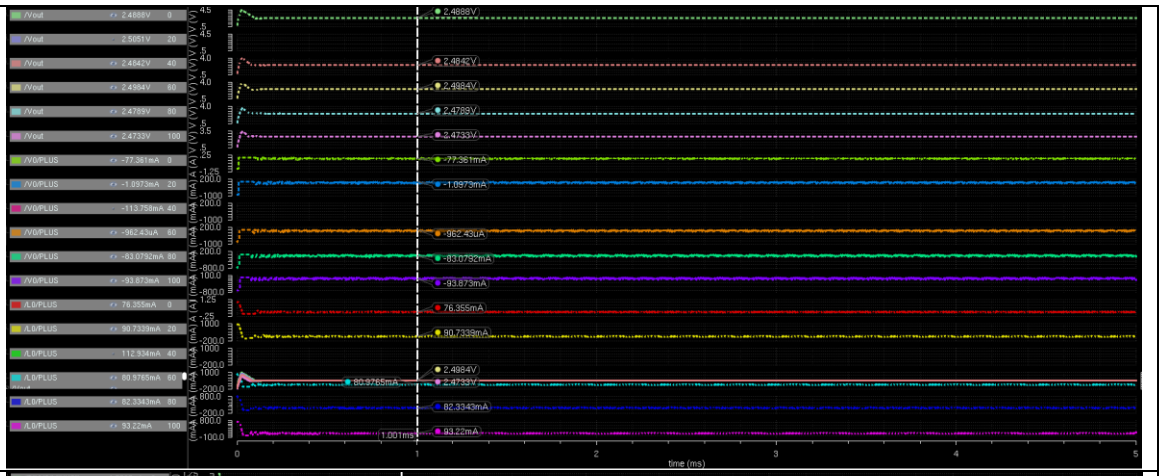
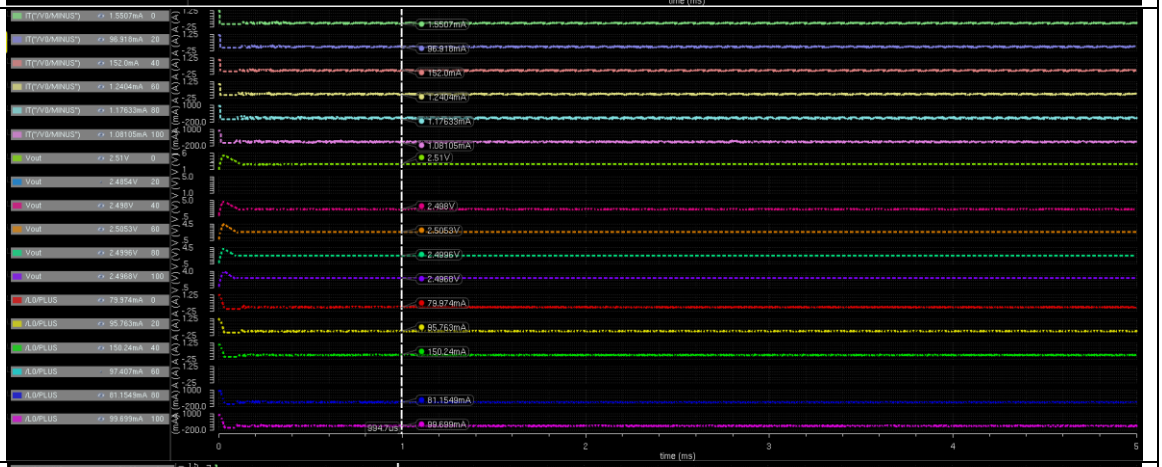
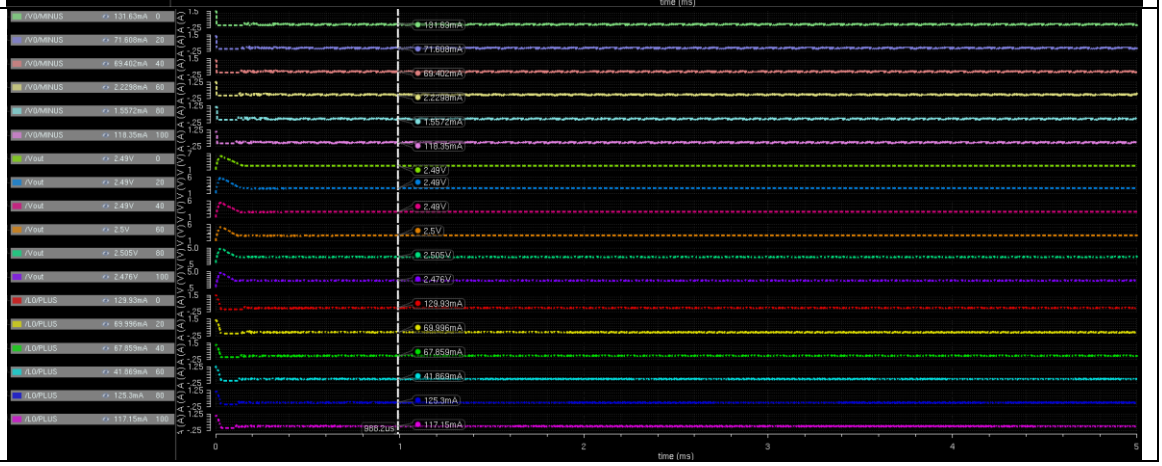
Then I began to do simulations for vdd at values of 4V, 4.5V, 5V, and 5.5V. Those were simulated at different current loads of 100mA and 50mA along with temperature changes from 0-100 degrees Celsius in increments of 20 degrees Celsius. Being plotted below are three things. The first is the initial current that is coming out the Buck converter and entering the inductor. Then also selected is the current that is coming out of the main vdd source. The last thing plotted is the Vout which should stay constant at 2.5V and will be feeding back into our comparator fed through a voltage divider.

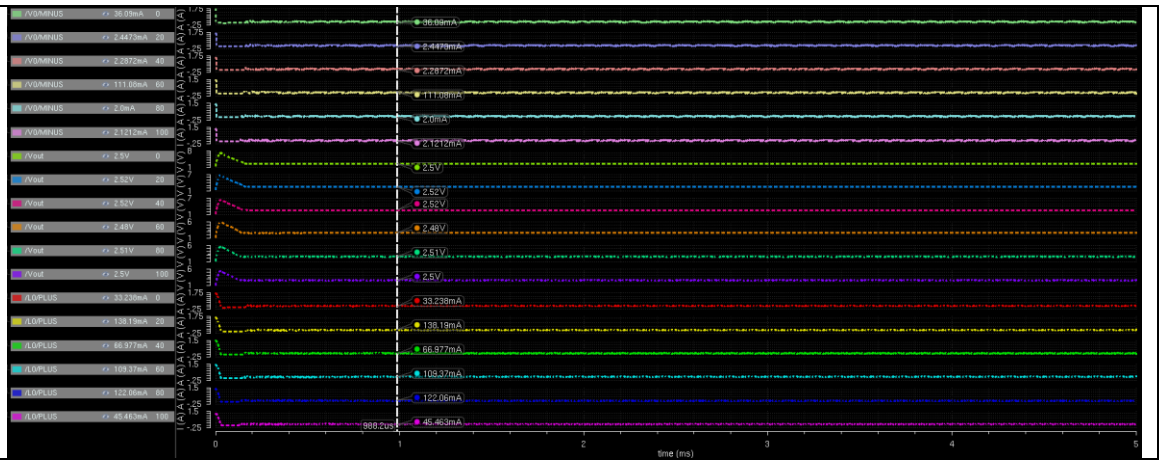
We can observe below that the current going into the inductor, becomes less rippled the higher we go in load and vdd. It has a smaller initial dip before stabilizing. The current also becomes higher as the vdd gets higher. That means that the resistance is getting lower as the vdd is getting higher. This is proven by V=IR.

It is noticed below that as the vdd is increased, there seems to be an increase of ripple at the start of the Vout. Also the current being supplied into the inductor rises along with the vdd. With the 50mA load the system seems to be less efficient than at 100mA. Also at different temperatures the values of of the current seem to rise, but after hitting 80 degrees celcius they seem to fall back down. The rise of current through the vdd at higher temperatures results in lower effieciency. Therefore it the system is more efficient and at peak performance at lower temperatures.

4V with 50mA load	

4.5V with 50mA load	
5V with 50mA load	
5.5V with 50mA load	

4V with 100mA load	
4.5V with 100mA load	
5V with 100mA load	

5.5V with 100mA load	

Efficiency is calculated using E = $\frac{V_{out} * I_{load}}{V_{dd} * I_{Avg}} * 100$

- Highest efficiency achieved was when vdd was 4V with 100mA load at 0 degrees Celsius which was 86.5%.
- Lowest efficiency achieved was when vdd was 5.5V with 50mA load at 60 degrees Celsius which was 78.4%.

4V with 50mA load

I_load	Vdd	Vout	I_avg	Efficiency	temp
50	4	2.5	37.27	83.8%	0
50	4	2.5	37.26	83.9%	20
50	4	2.5	37.23	83.9%	40
50	4	2.5	37.17	84.1%	60
50	4	2.5	37.1	84.2%	80
50	4	2.5	37.01	84.4%	100

4.5V with 50mA load

I_load	Vdd	Vout	I_avg	Efficiency	temp
50	4.5	2.5	33.8	82.2%	0
50	4.5	2.5	33.94	81.8%	20
50	4.5	2.5	33.87	82.0%	40
50	4.5	2.5	33.78	82.2%	60
50	4.5	2.5	33.67	82.5%	80
50	4.5	2.5	33.54	82.8%	100

5V with 50mA load

I_load	Vdd	Vout	I_avg	Efficiency	temp
50	5	2.5	30.83	81.1%	0
50	5	2.5	31.06	80.5%	20
50	5	2.5	31.21	80.1%	40
50	5	2.5	31.13	80.3%	60
50	5	2.5	30.98	80.7%	80
50	5	2.5	30.84	81.1%	100

5.5V with 50mA load

I_load	Vdd	Vout	I_avg	Efficiency	temp
50	5.5	2.5	28.3	80.3%	0
50	5.5	2.5	28.64	79.4%	20
50	5.5	2.5	28.86	78.8%	40
50	5.5	2.5	28.98	78.4%	60
50	5.5	2.5	28.94	78.5%	80
50	5.5	2.5	28.77	79.0%	100

4V with 100mA load

I_load	Vdd	Vout	I_avg	Efficiency	temp
100	4	2.5	72.29	86.5%	0
100	4	2.5	72.39	86.3%	20
100	4	2.5	72.45	86.3%	40
100	4	2.5	72.5	86.2%	60
100	4	2.5	72.52	86.2%	80
100	4	2.5	72.56	86.1%	100

4.5V with 100mA load

I_load	Vdd	Vout	I_avg	Efficiency	temp
100	4.5	2.5	64.28	86.4%	0
100	4.5	2.5	65.29	85.1%	20
100	4.5	2.5	65.24	85.2%	40
100	4.5	2.5	65.2	85.2%	60
100	4.5	2.5	65.1	85.3%	80
100	4.5	2.5	65.03	85.4%	100

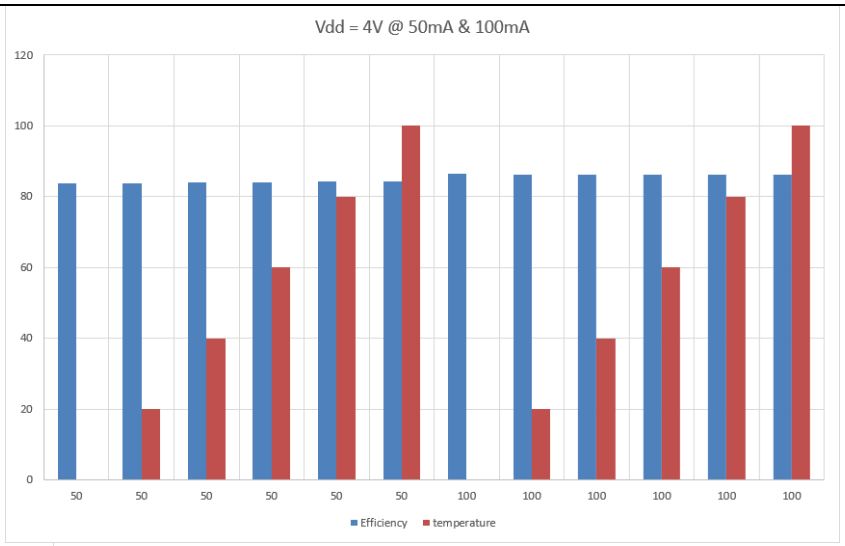
5V with 100mA load

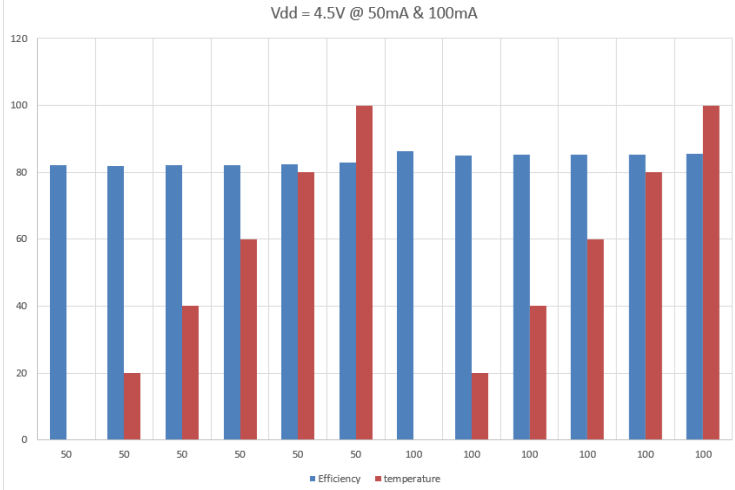
I_load	Vdd	Vout	I_avg	Efficiency	temp
100	5	2.5	59.6	83.9%	0
100	5	2.5	59.58	83.9%	20
100	5	2.5	59.49	84.0%	40
100	5	2.5	59.4	84.2%	60
100	5	2.5	59.23	84.4%	80
100	5	2.5	59.03	84.7%	100

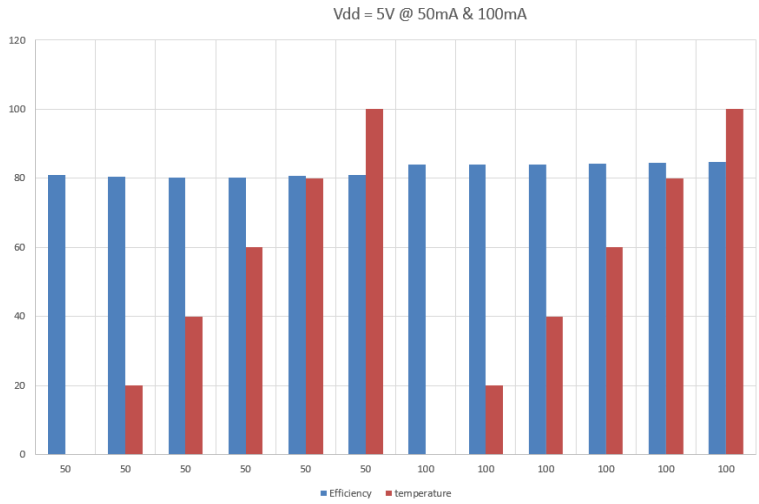
5.5V with 100mA load

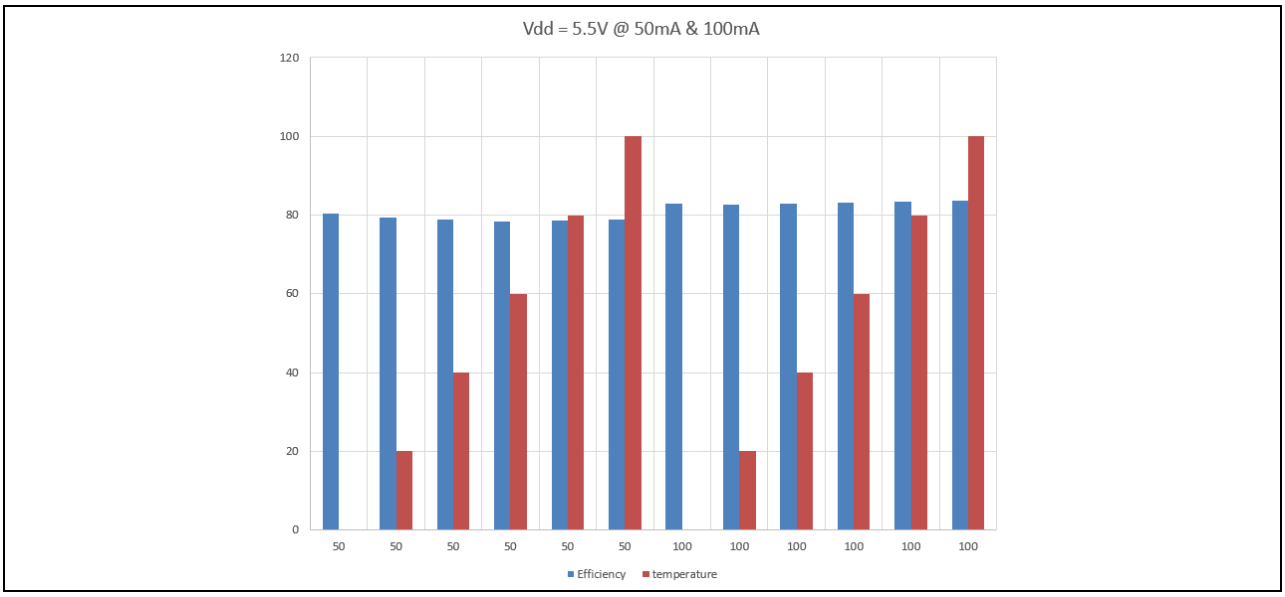
I_load	Vdd	Vout	I_avg	Efficiency	temp
100	5.5	2.5	54.84	82.9%	0
100	5.5	2.5	54.93	82.7%	20
100	5.5	2.5	54.84	82.9%	40
100	5.5	2.5	54.72	83.1%	60
100	5.5	2.5	54.52	83.4%	80
100	5.5	2.5	54.3	83.7%	100

Here are the plots for I_{load} vs. Efficiency varying at different temperatures.

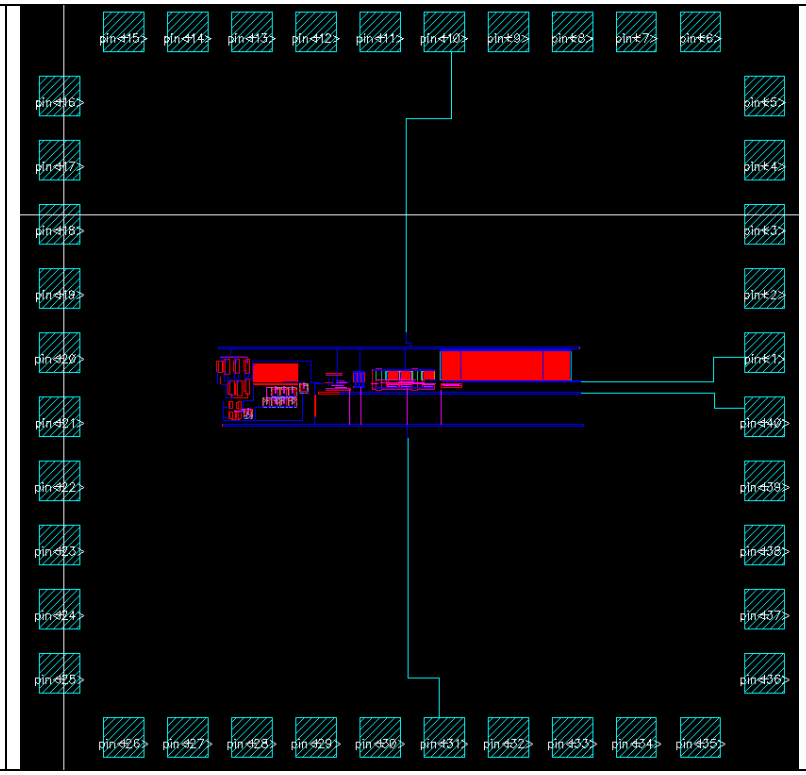




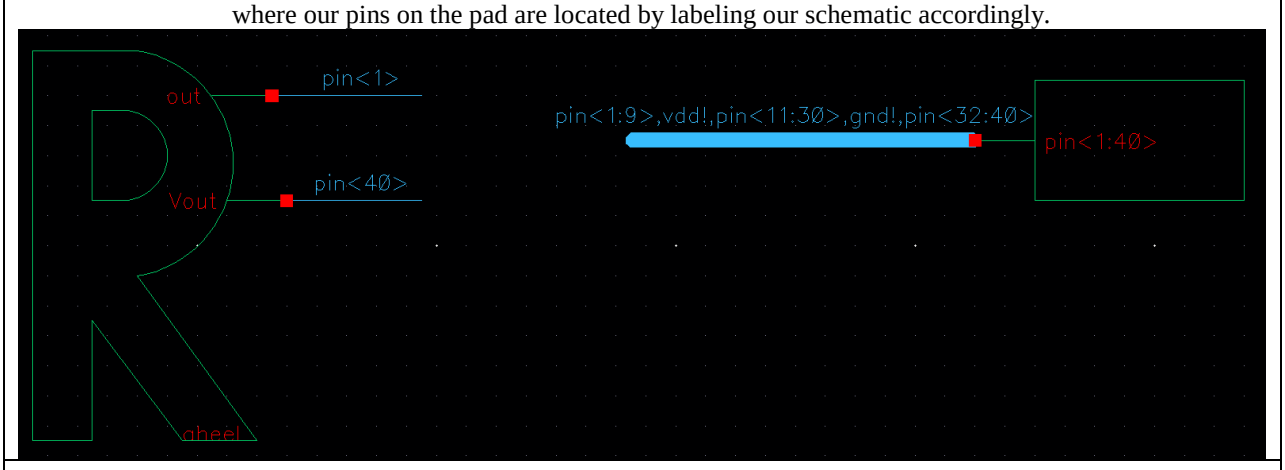


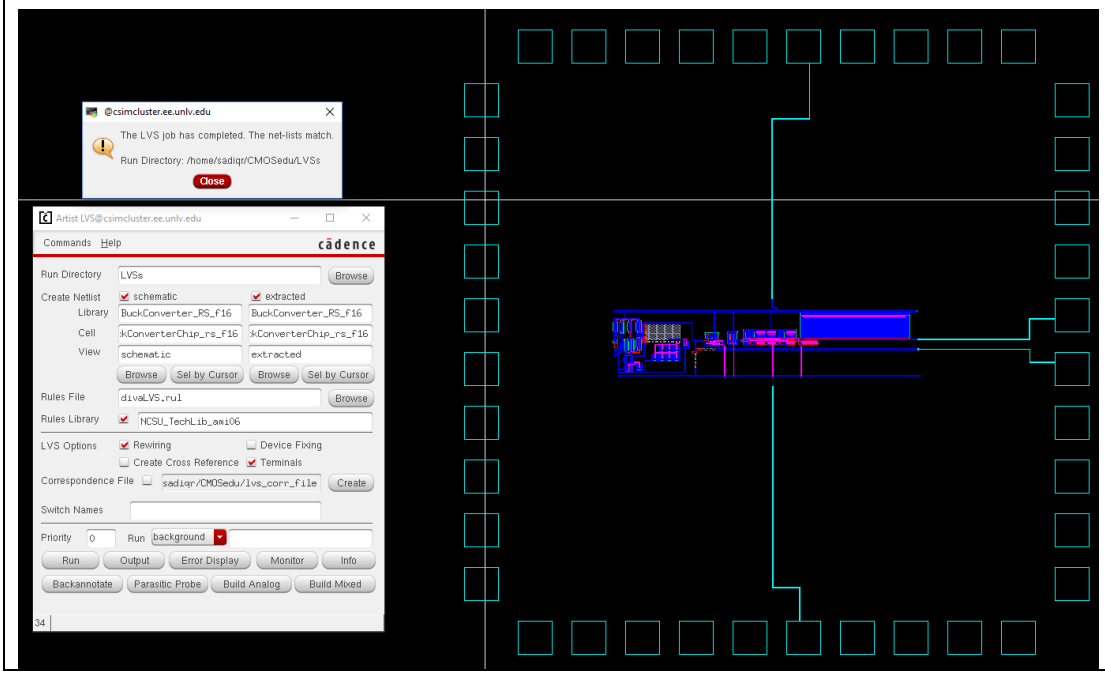


Now the Buck converter can be laid out on a padframe. This is to show if we were to fabricate the chip, how the connections would look.

Buck Converter connected to padframe	

This schematic is created to show the LVS for the pad frame that contains the Buck converter. As seen we show where our pins on the pad are located by labeling our schematic accordingly.





Out	Pin<1>
Vout	Pin<40>
vdd!	Pin<10>
gnd!	Pin<31>