Stacking Power MOSFETs

PMOS Configuration

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Test 1a – IFR9640

- PMOS Configuration; 5 Stack PMOS
- MOSFET:
  - IFR9640, VDS = -200 V, RDS(on) = 0.5 Ohms
- Capacitance Values:
  - 150 pF, 300 pF, 450 pF, 600 pF
- Max Voltage:
  - 1000 V

Test 1a – Calculations

Csg = 1200 pF
Cdg = 81 pF

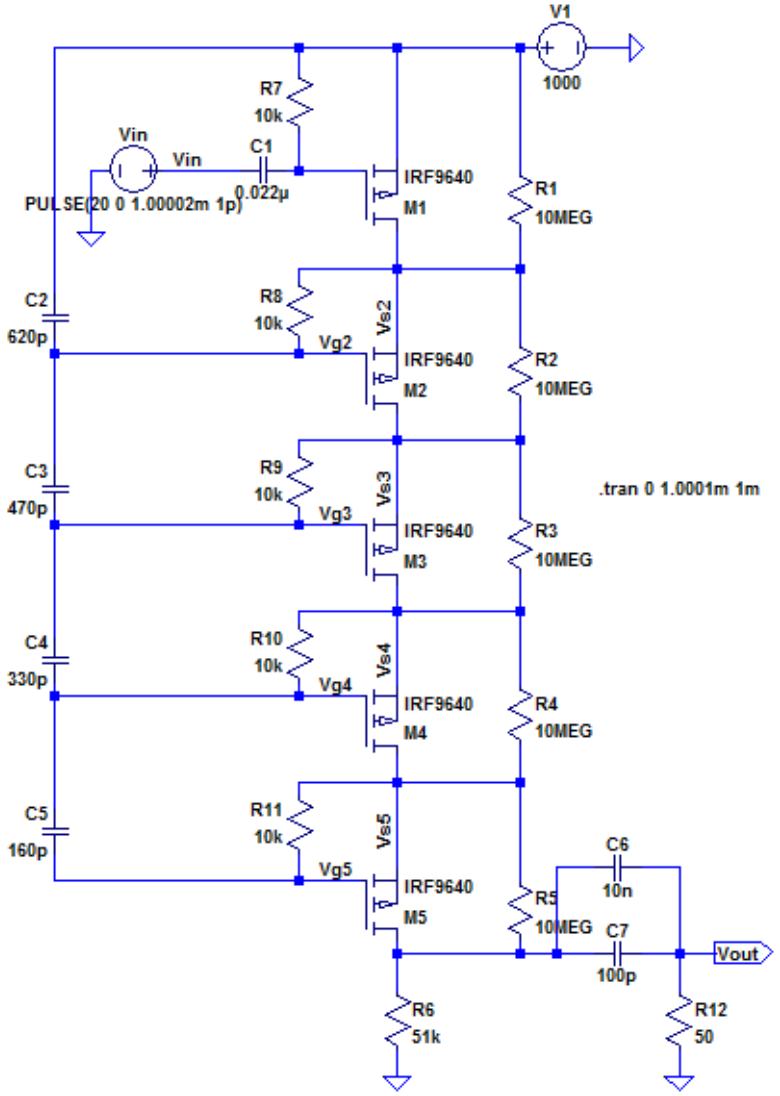
Vd = 500 V
Vsg = 20 V
Av = 25

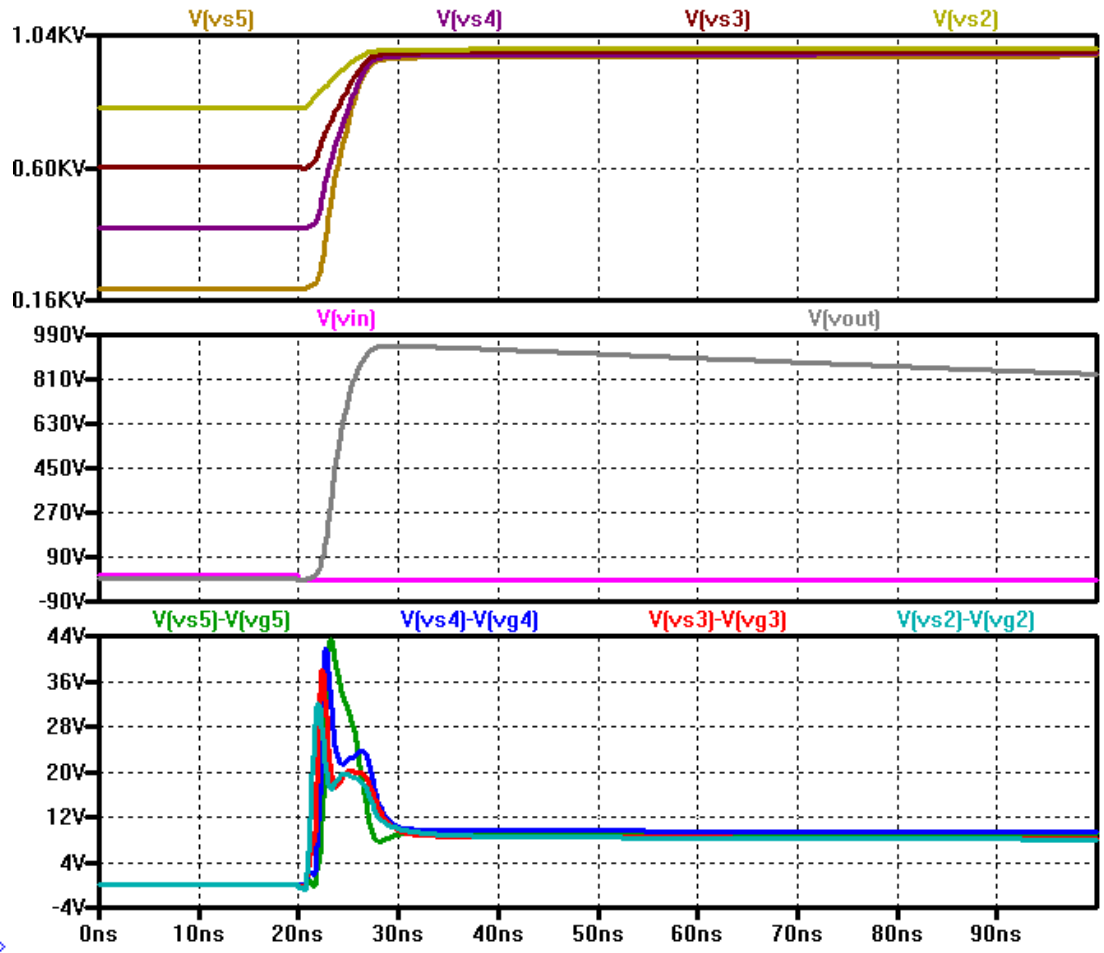
C'sg = Csg + Av * Cdg
= 1200 pF + 25 * 81 pF
= 3225 pF

Vsg = Vd * C2 / (C2 + C'sg) *Solve for C2*
C2 = [(Vsg / Vd) * C'sg] / [1 – (Vsg / Vd)]
= [(20 / 500) * 3225p] / [1 – (20 / 500)]
= 135 pF

*To ensure the MOSFETs turn on, increase C2 to **150 pF**

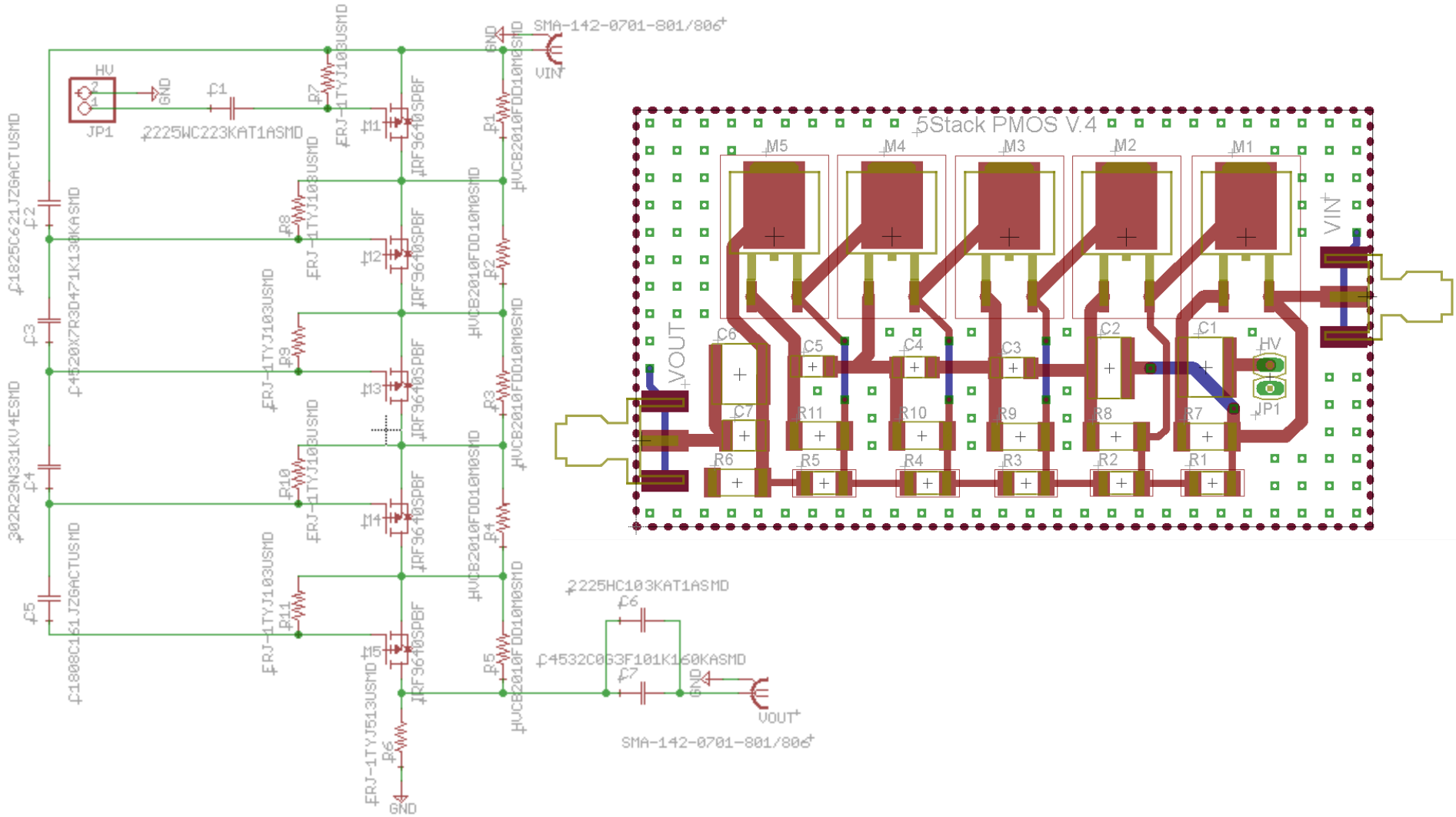
Test 1a – Simulation & Values



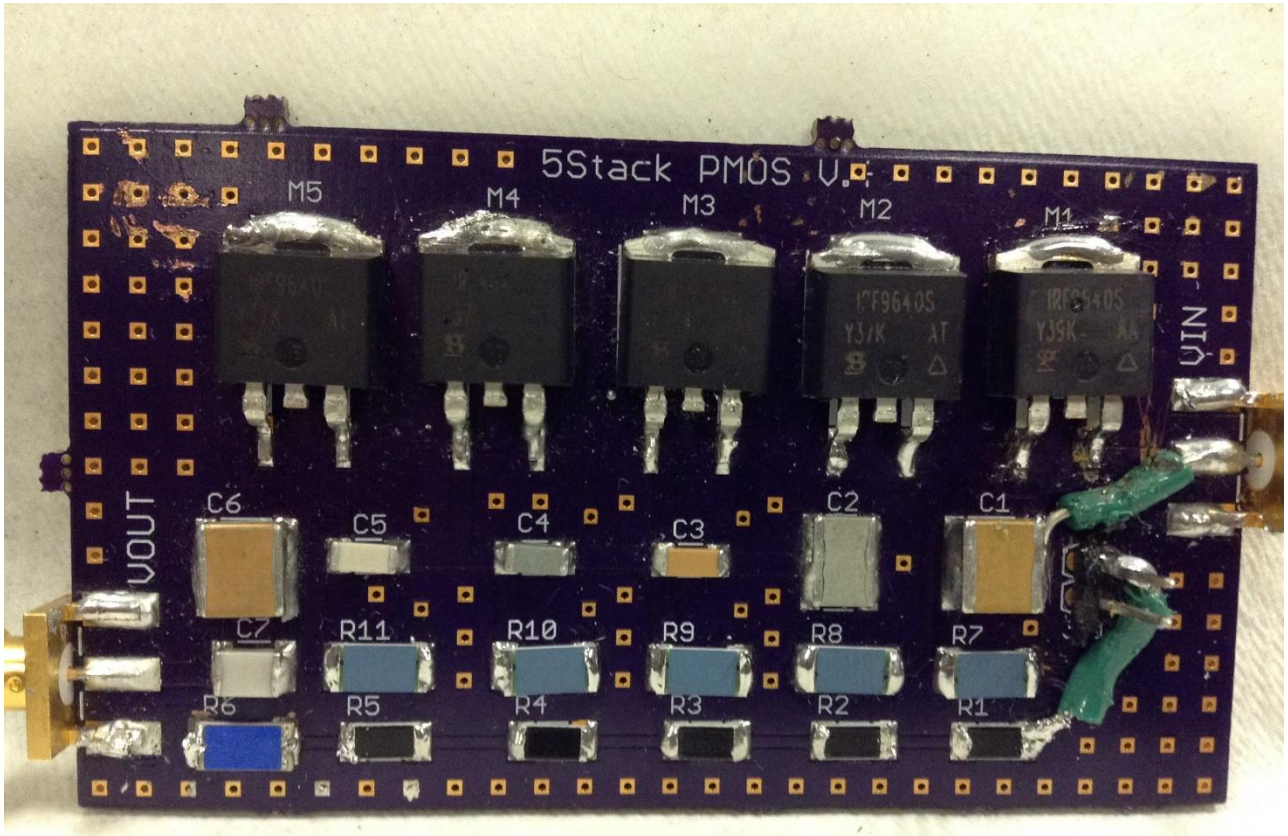


*Values reflect parts available

Test 1a – PCB Layout

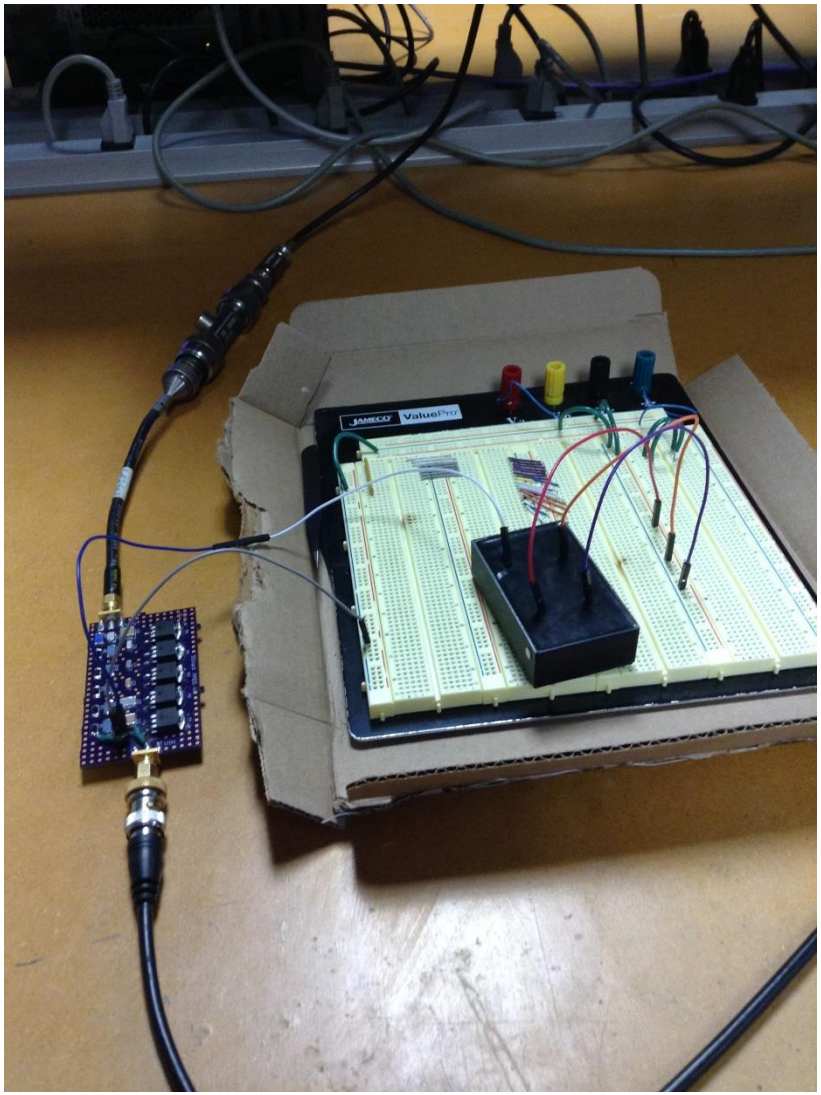


Test 1a – Chip



* The VIN and HV were switched in the PCB and needed to be rewired

Test 1a – Setup



Test 1b – FQD4P40

- PMOS Configuration; 5 Stack PMOS
- MOSFET:
  - FQD4P40, VDS = -400 V, RDS(on) = 3.1 Ohms
- Calculated Capacitance Values:
  - 50 pF, 100 pF, 150 pF, 200 pF
- Max Voltage:
  - 2000 V

Test 1b – Calculations

Csg = 845 pF
Cdg = 26 pF

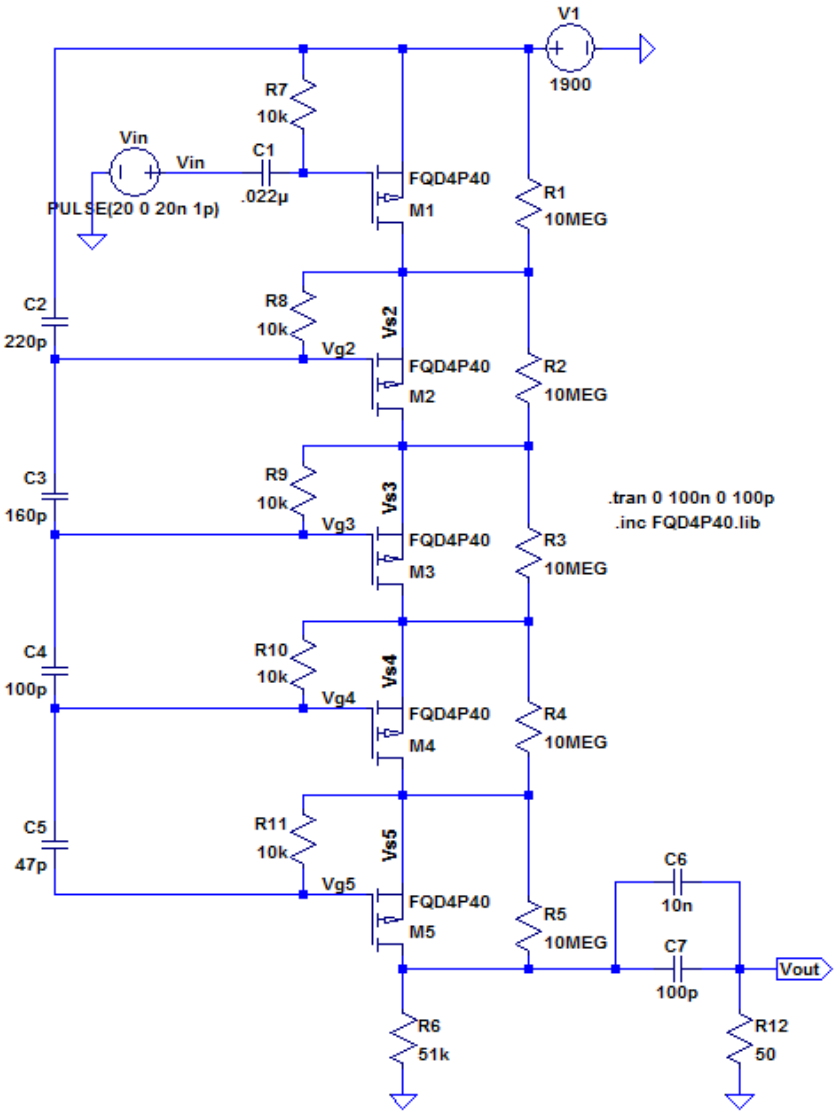
Vd = 500 V
Vsg = 20 V
Av = 25

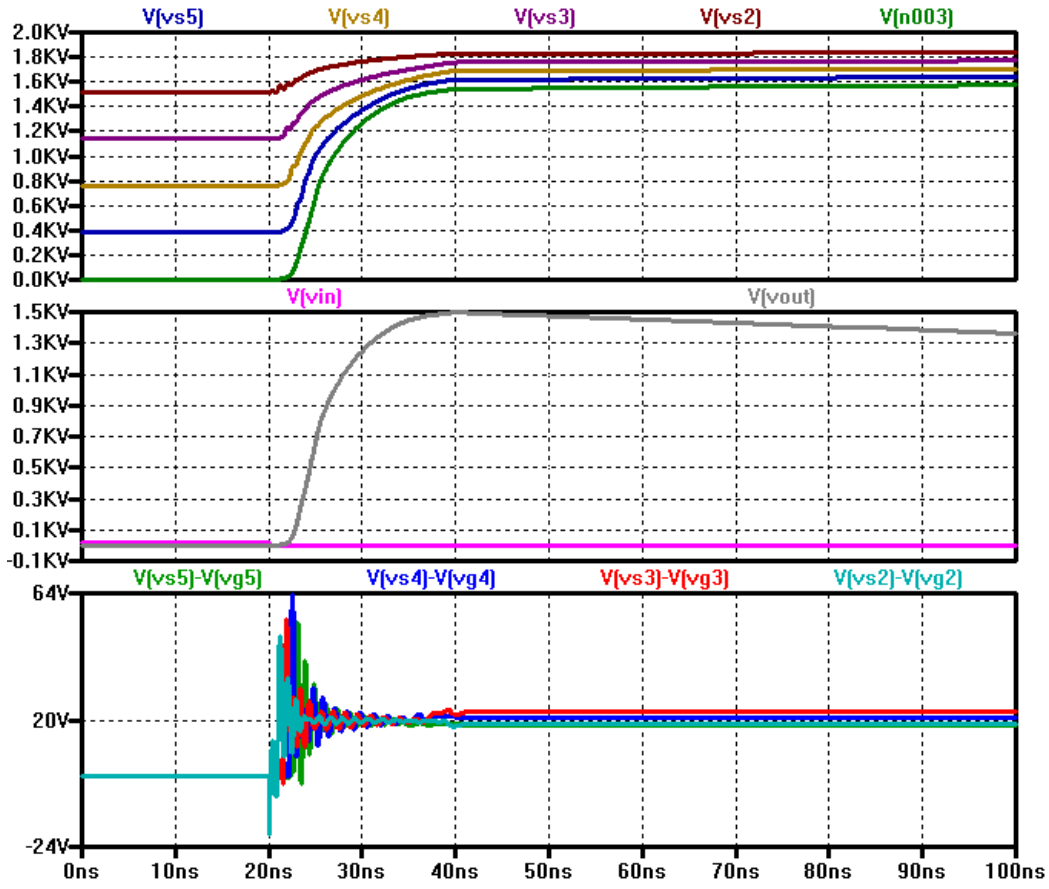
C'sg = Csg + Av * Cdg
= 680 pF + 25 * 15 pF
= 1055 pF

Vsg = Vd * C2 / (C2 + C'sg) *Solve for C2*
C2 = [(Vsg / Vd) * C'sg] / [1 – (Vsg / Vd)]
= [(20 / 500) * 1055p] / [1 – (20 / 500)]
= 44.0 pF

*To ensure the MOSFETs turn on, increase C2 to **50 pF**

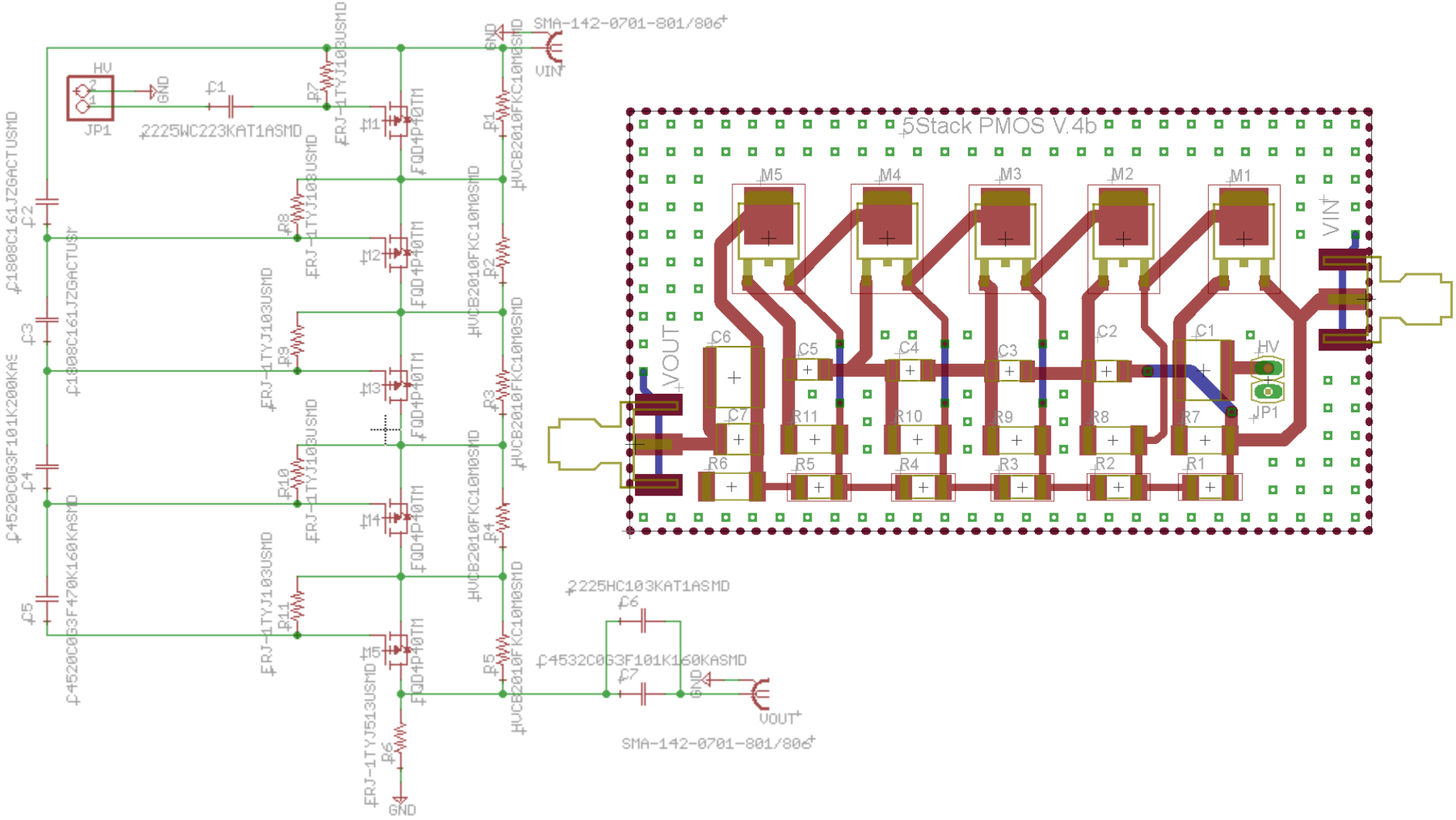
Test 1b – Simulation & Values



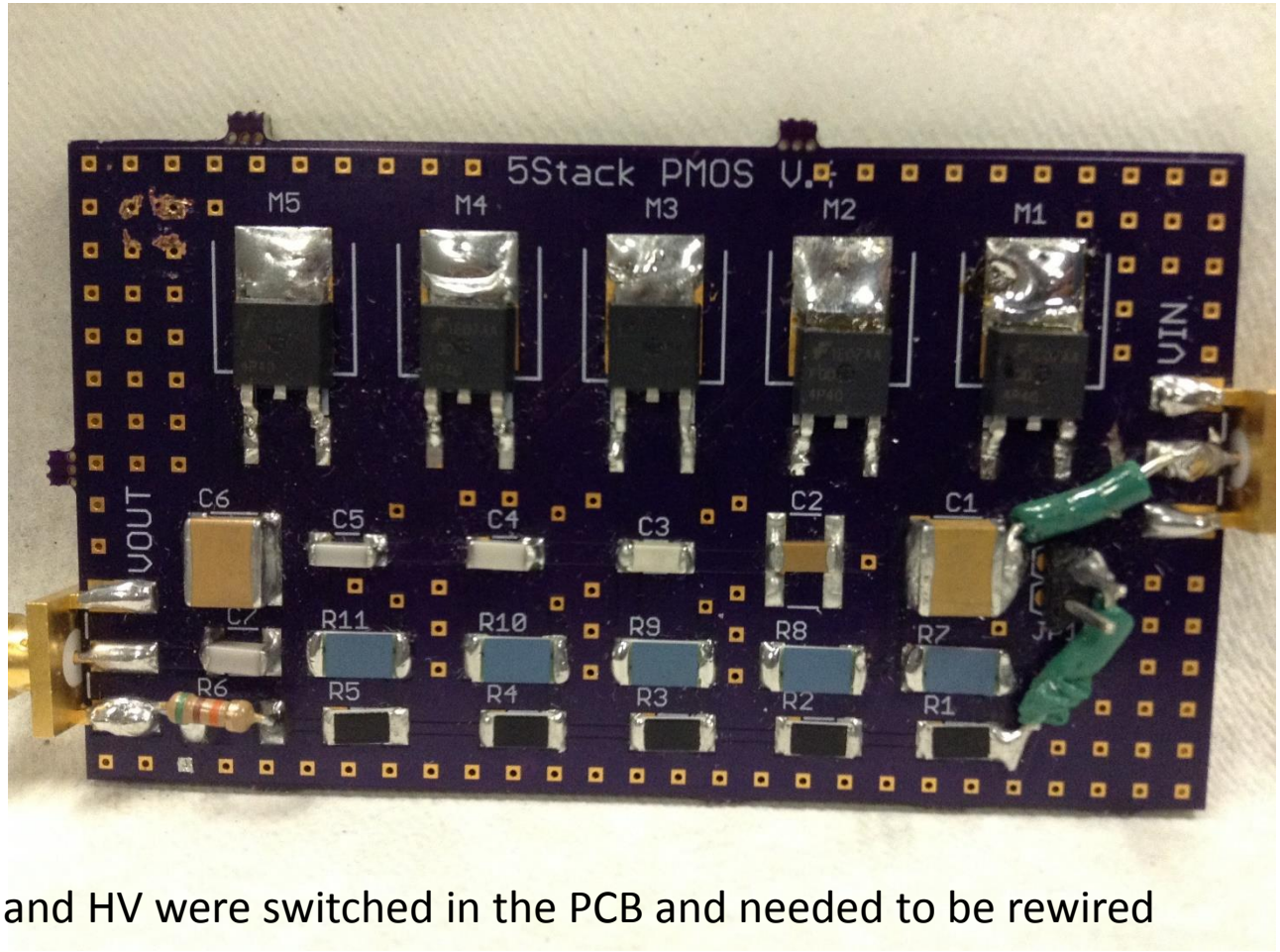


*Values reflect parts available

Test 1b – PCB Layout



Test 1b – Chip



* The VIN and HV were switched in the PCB and needed to be rewired

Test 1 – Conclusion

- No results were able to be gathered from either type of MOSFET
- The first MOSFET that is attached to the high voltage repeated blew up while testing
- An extra capacitor near the high voltage is needed in the design
- The board will be re-fabricated appropriately to accommodate changes