Stacking Power MOSFETs

NMOS Configuration

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Test 4

- NMOS Configuration
- MOSFET:
  - STP8NM60
- Calculated Capacitance Values:
  - 50pF
- Max Voltage:
  - 1000 V
- Changes:
  - Switched to a stack of two to get better results

Test 4 – Calculations

Cgs = 440 pF
Cgd = 10 pF

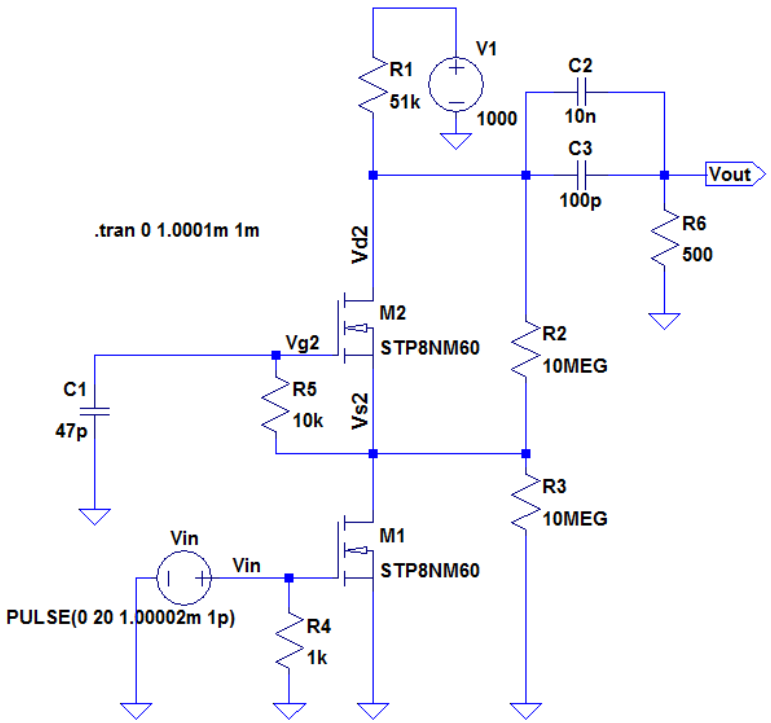
Vd = 500 V
Vgs = 20 V
Av = 25

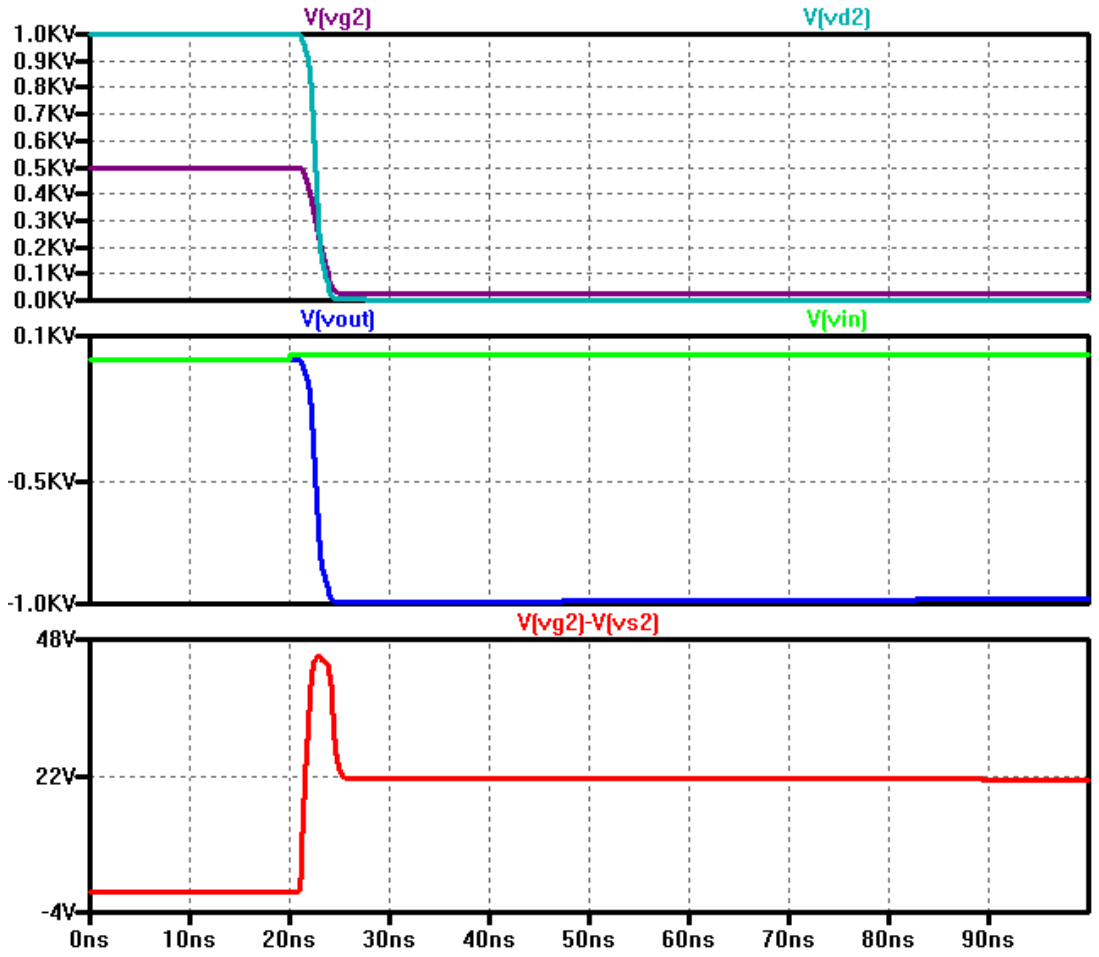
C'gs = Cgs + Av * Cgd
= 440 pF + 25 * 10 pF
= 690 pF

Vgs = Vd * C2 / (C2 + C'gs) *Solve for C2*
C2 = [(Vgs / Vd) * C'gs] / [1 – (Vgs / Vd)]
= [(20 / 500) * 690p] / [1 – (20 / 500)]
= 28.75 pF

*To ensure the MOSFETs turn on, increase C2 to **50 pF***

Test 4 – Simulation & Values

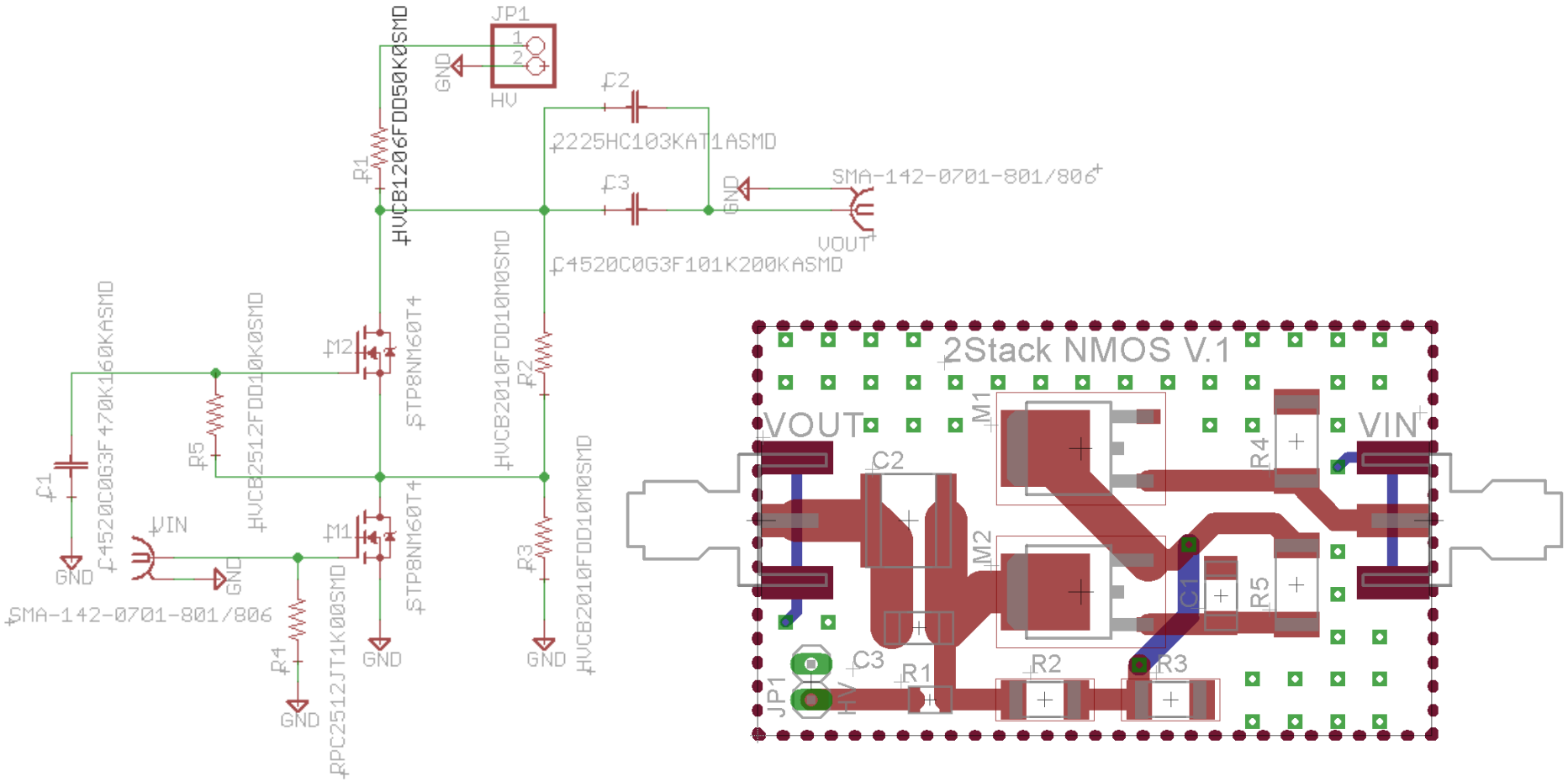




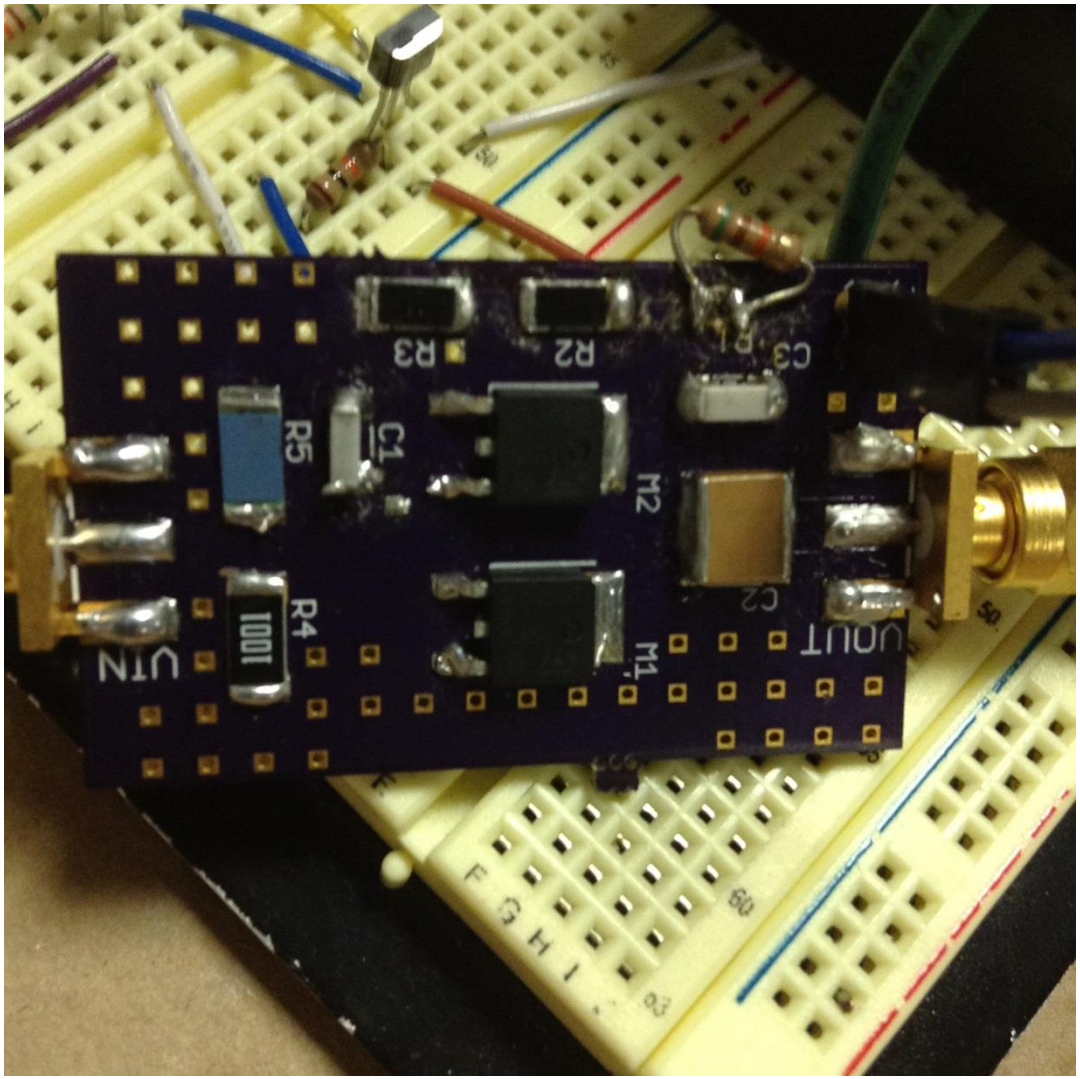
*Values reflect components available

*Simulation are the same as the previous test

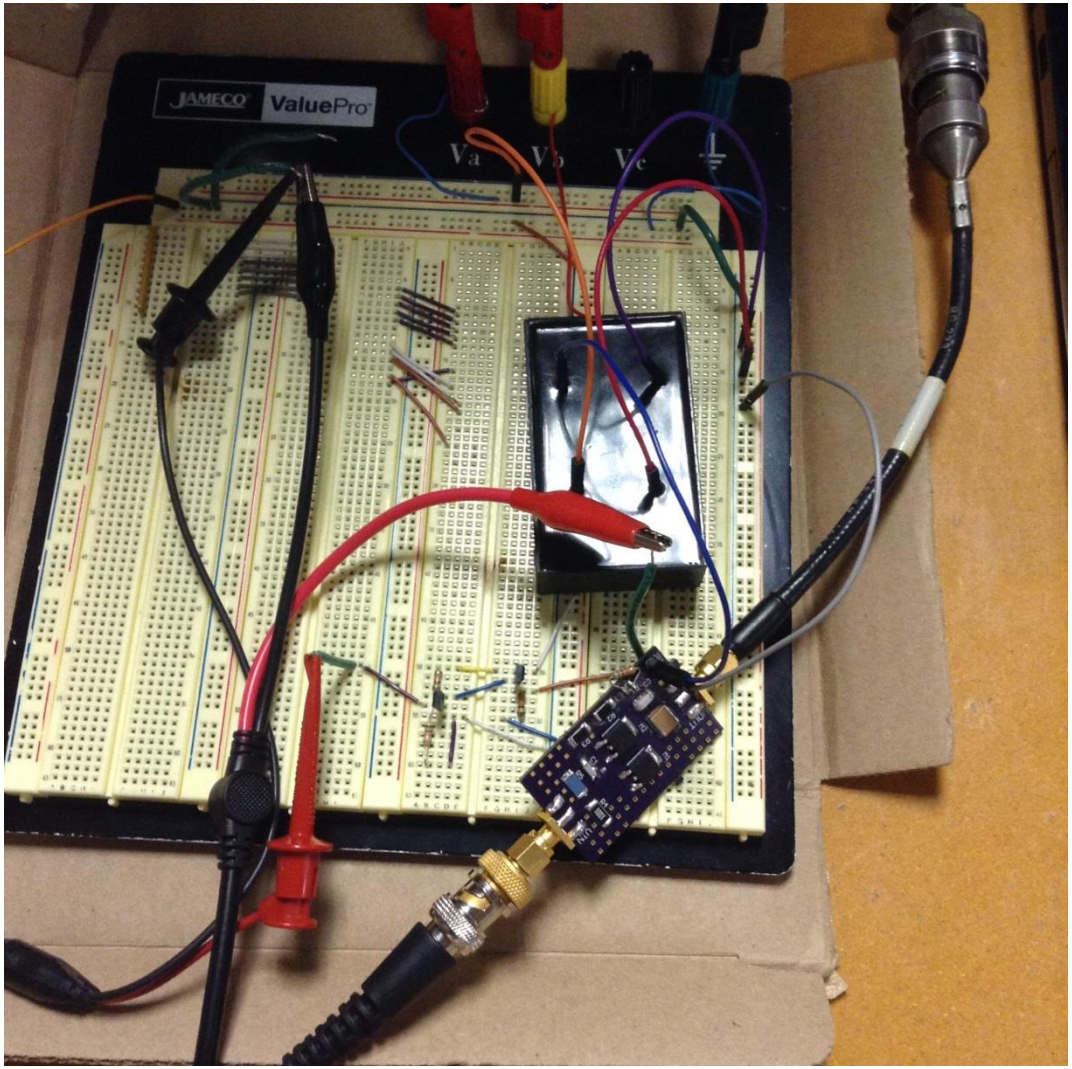
Test 4 – PCB Layout



Test 4 – Chip

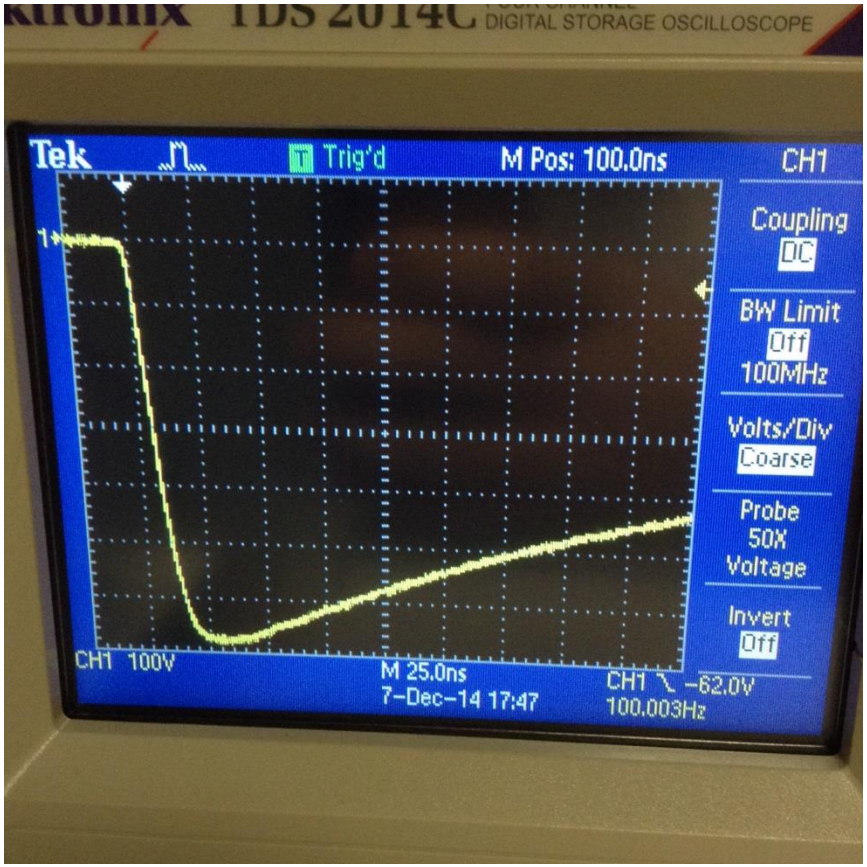


Test 4 – Setup



Test 4 – Sample 1 Results

- Vin = 651 V
- Switching = ~650V, or 100%
- Voltage Across (Difference):
  - M1: 623 V (-38)
  - M2: 284 V (-339)
- Results came out nicely
- A pulse generator was created to provide a 15V pulse which helps out a lot
- The board seemed to output a higher voltage



Test 4 – Conclusion

- By using a 2 stack instead of a 5 stack, less ringing would occur due to a shorter circuit path
- A pulse generator made a huge difference since before, our equipment only allows for 5V to 10V pulses

Test 4 – Retest

- A retest was done on the 5 stack with the 15V pulse instead of the 10V pulse previously use
- Results were cleaner