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ECG 722: Mixed-Signal Circuit Design

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Project Specifications:

This report details a K-Delta-1-Sigma (KD1S) modulator design that was used to replace the ADC shown in Figure 9.32 of the CMOS Mixed Signal Design textbook using a continuous-time topology (no switched-capacitors and no non-overlapping clock signals). An overview of the specifications of the proposed design are seen in the table below. The following sections will detail the main components of the KD1S, and then analyze both first and second order topologies and evaluate their performances.

Overview of Project Performance:

First Order Design:

1st Order, 8-Path KD1S				
Average Dynamic Power Consumption = 57 mW				
OSR	64		128	
Mode	Serial	Parallel	Serial	Parallel
$F_{s,new}$	792 MHz	99 MHz	792 MHz	99 MHz
SNR	40.41 dB	28.50 dB	46.92 dB	40.75 dB
Neff	6.42 Bits	4.44 Bits	7.50 Bits	6.47 Bits
Bandwidth	6.19 MHz	6.18 MHz	3.09 MHz	3.09 MHz

Second Order Design:

2nd Order, 4-Path KD1S				
Average Dynamic Power Consumption = 80 mW				
OSR	32		64	
Mode	Serial	Parallel	Serial	Parallel
$F_{s,new}$	395 MHz	99 MHz	395 MHz	99 MHz
SNR	40.79 dB	32.75 dB	46.34 dB	43.03 dB
Neff	6.48 Bits	5.14 Bits	7.40 Bits	6.85 Bits
Bandwidth	6.18 MHz	6.17 MHz	3.09 MHz	3.09 MHz

Design of the Clock Generator:

A fundamental design consideration regarding the KD1S surrounds the generation of the clock signals. This design required the incorporation of a ring oscillator that could generate eight equally spaced edges to be used to clock the circuit (so as to be able to run eight paths). The symbol used for the clock generator is shown in Figure 1 below, and will be seen in many of the schematics throughout this paper.
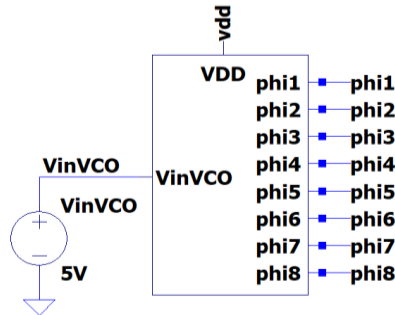

Figure 1– Clock Generator Symbol

The schematic used for this design is shown in Figure 2, and illustrates a differential ring oscillator. It should be noted that a differential ring oscillator was chosen over a single-ended ring oscillator because of the amount of clock cycles required - a single-ended oscillator would produce and odd number of clock cycles, while the differential oscillator produces an even number of clock cycles. Thus, an even number of paths is required for this design to operate correctly. It should be noted that in the complete design, the compliment of each of these signals was also taken for use in the feedback control, discussed in a later section.
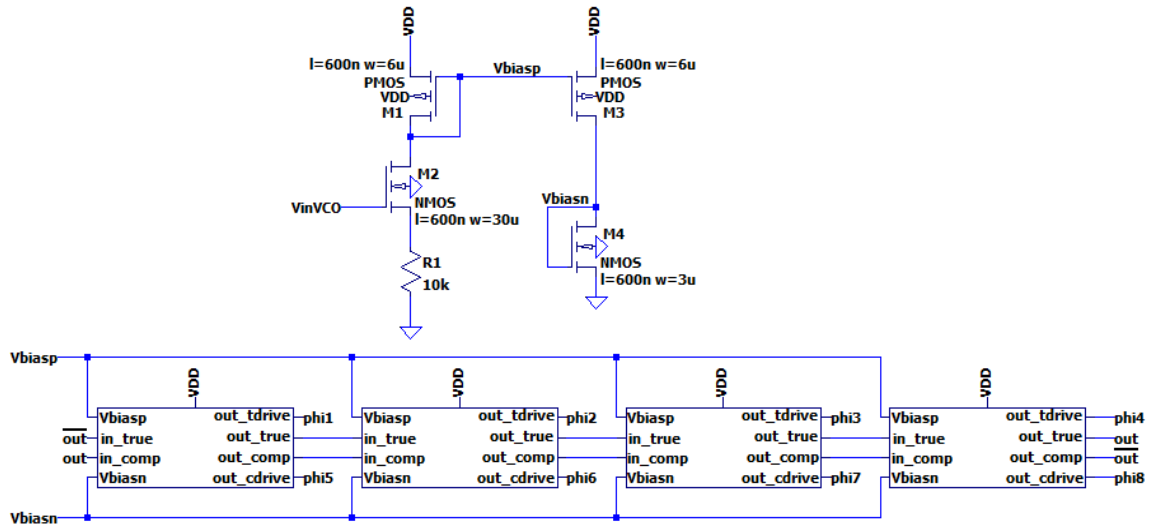

Figure 2 – Clock Generator Circuit (With Biasing Circuit)

Details of the clock generation specify the way that the eight non-overlapping clock signals were made. There are four delay elements as well as a biasing circuit seen in the higher-level view of the clock generator in Figure 2. This circuit was chosen because it is self-biasing and takes up a small amount of space in comparison to other biasing circuits (though the use of a wide NMOS was optimized). Additionally, it allows for fairly easy changes in its supplied voltages (Vbiasp and Vbiasn), as these can be changed by varying the resistor or Vinco in the current mirror. An important feature that this design possesses is its ability to adapt varying oscillation frequencies (the oscillation is voltage controlled). This was done with the inclusion of the current starved (CS) inverter, which is the first in the row of inverters used, as well as the biasing circuit. The current in this inverter relies on the top PMOS and bottom NMOS device (the ones with bigger widths). To be more specific, as the voltage of the biases is increased, the current through the inverter increases, which also causes the oscillation frequency to increase (because charge times are decreased, meaning that operation can happen quicker). Similarly, if the voltage biases are decreased, the current through the inverter decreases, which results in a higher charge time and therefore lower oscillation frequency. The complete circuitry showing one delay stage is shown in Figure 3 below.
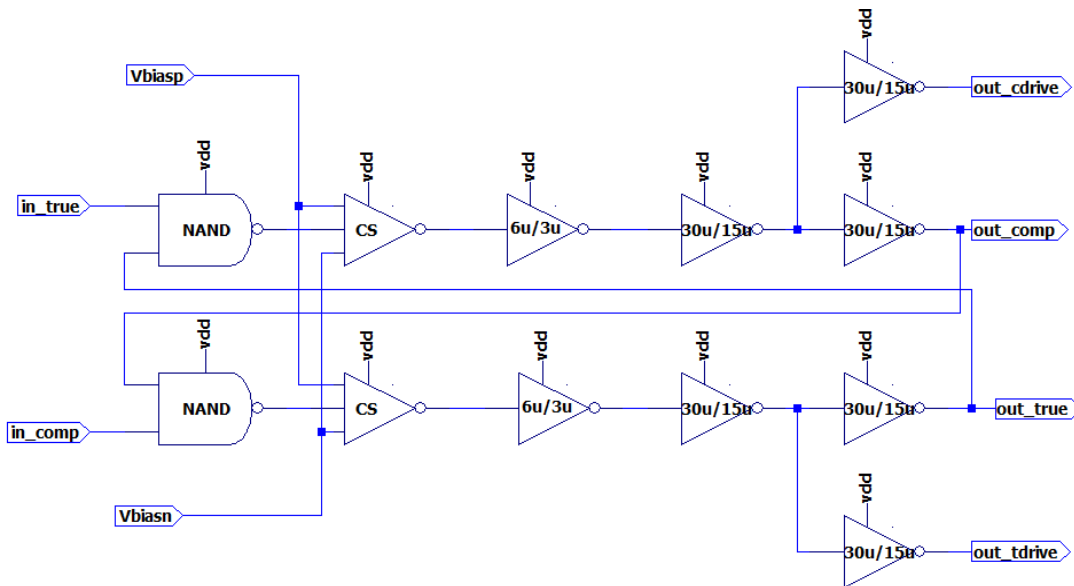

Figure 3- One Delay Stage

The operation of the clock generation for an eight-path cycle is shown in Figure 4. It is clear that each signal is non-overlapping. The circuit relies on the time that the clock goes high, so

the distance between each of the high signals is important to note. Moreover, for a k-path topology, the design would need k different clock edges. For example, for an eight path topology, eight clock edges would be required; thus, for a 10 ns (100 MHz) sampling period, each cycle would have to be spaced 1.25 ns from each other.
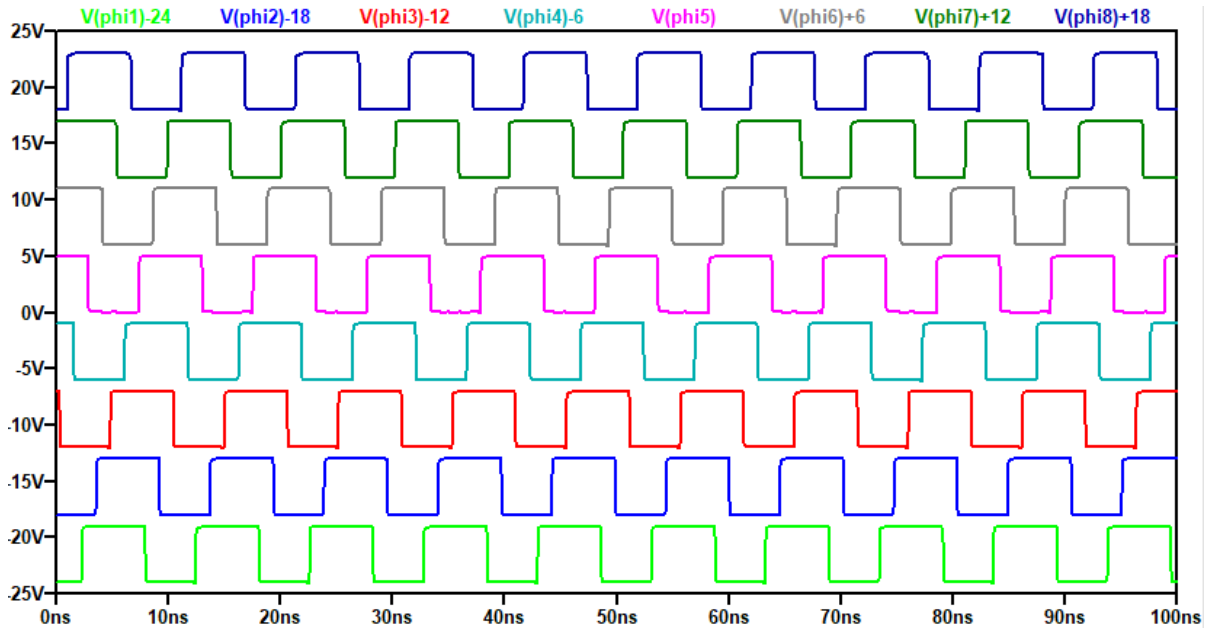

Figure 4 – Eight Clock Edges

Timing:

Another critical factor about this circuit is the timing of the signals. The following simulation shows how the timing for one path of the circuit would go. To explain further, the timing of the first path on a four-path design will be detailed, but the same concept can be applied to all of the paths using different clock signals. the first thing that would be clocked is the left transmission gate in the path. For this path, the red signal (phi4i) would go high, passing the signal through. Then, the comparator will be clocked (blue, phi1) and it will have some time to make a decision. Then, the right-side transmission gate will be clocked, allowing for the signal to pass through the feedback path.
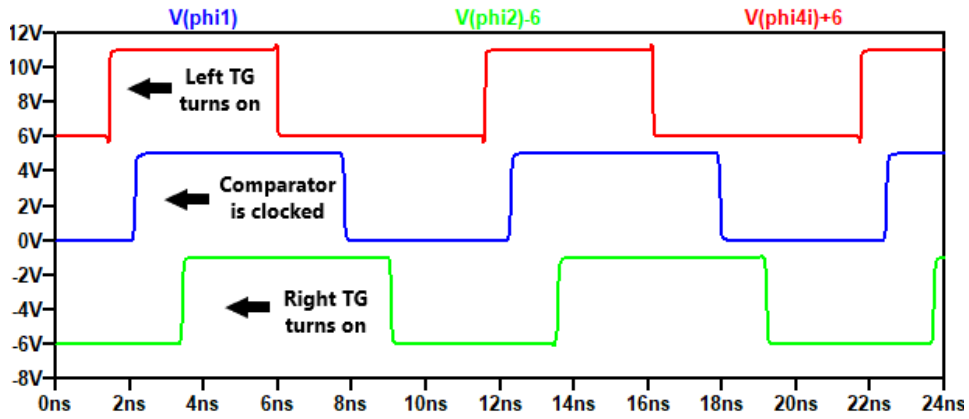
Figure 5 - Showing the Order of a Paths Signals

Since the circuit relies on this jagged clocking system, there is only a small window of time where all of the signal in a path are high, allowing feedback into the op amp. The following simulation shows this, where the high signals represent the amount of time where each of the four paths are allowing the feedback through. This is also further described in the transmission gate section.
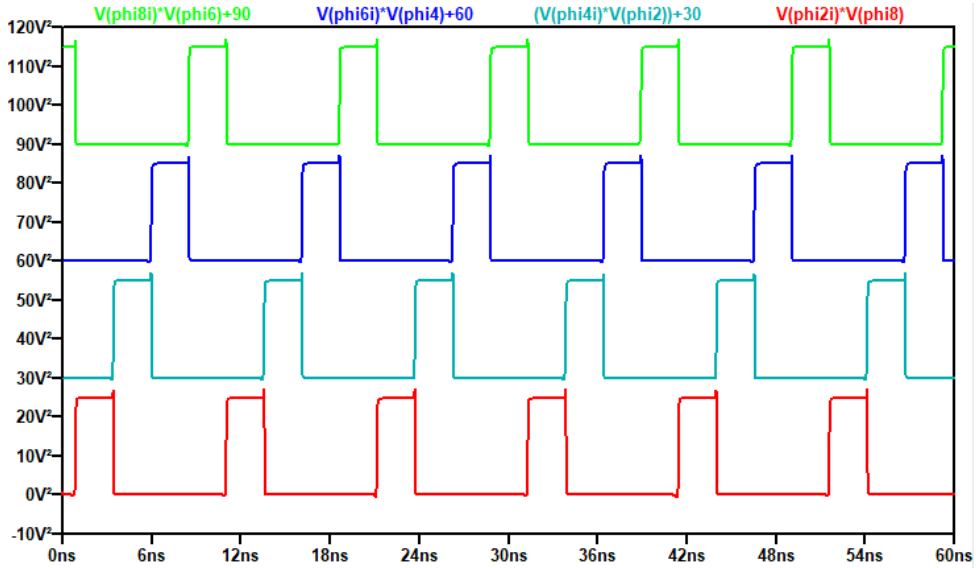

Figure 6- Showing the Paths Passing Windows

Design of the Comparator:

The comparator is another critical component in the design of the KD1S. As with most applications, the comparator in this design must be able to make fast and accurate decisions when each of the clock edges go high/low. The symbol used for each of the comparators is shown in Figure 7 below.
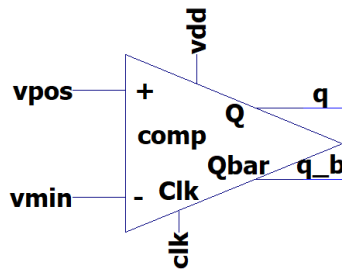

Figure 7– The Comparator Symbol

The multiple-path nature of the KD1S also calls for multiple comparators. For example, in an 8-path design, there would be eight clock signals and eight comparators; this means that the comparators will have to be able to make decisions at eight times the sampling frequency. It should be noted that this modulator averages the results of each path, meaning that glitches and inaccurate decisions will also be averaged out; however, a limit on the amount of inaccurate decisions is obviously a good thing. Thus, a fast comparator is prioritized in this design. The design used for each of the comparators to achieve these standards is shown in Figure 8 below.
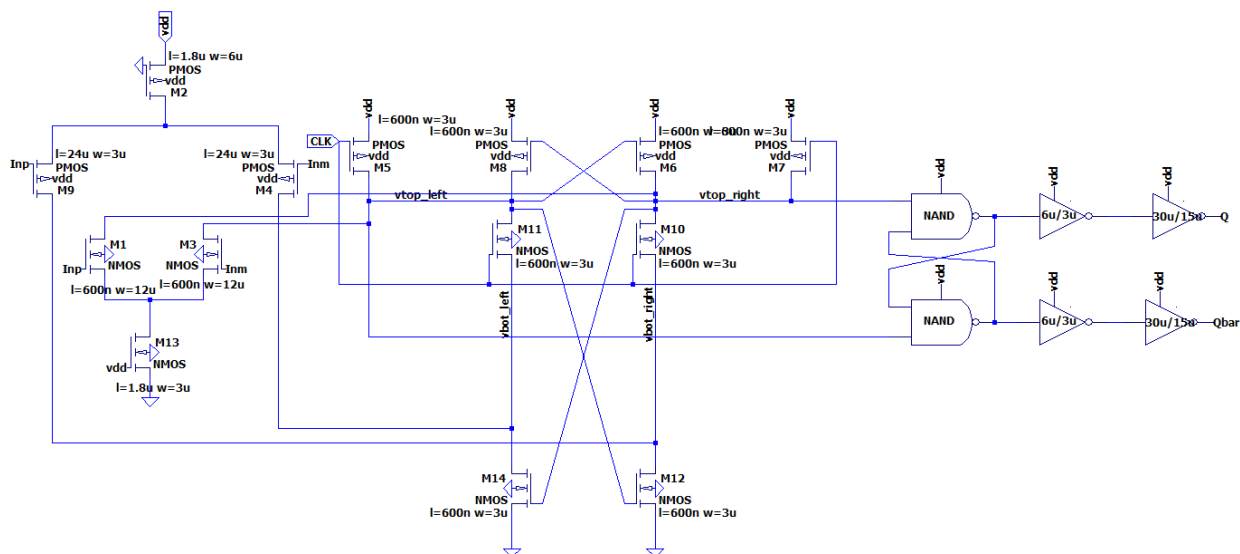

Figure 8 – The Comparator Design

Something to keep in mind with this comparator is that it needs to be able to resolve small differences in a small amount of time. The circuit chosen adopts a cross coupled inverter latch with a positive feedback loop. It makes use of an input stage to create a wide input voltage swing. Additionally, the NAND gates seen on right side of the circuit were implemented to eliminate overlapping output signals. Lastly in the circuit, there are larger inverters that were placed to drive the full output.

The following simulation shows the comparator making a sample decision. As shown, the rising edge makes a very quick and accurate solution. There is some delay on the decision on the falling edge, but the comparator overall works well enough for this application.
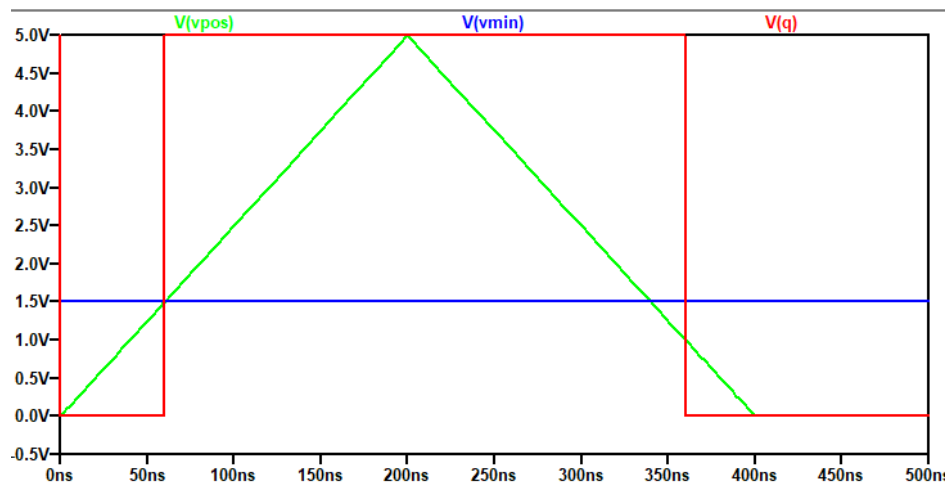

Figure 9 - Simulating the Comparator

Design of the Amplifier:

Another important piece of the KD1S is the amplifier (or amplifiers) that is chosen. This piece of the circuit acts as the integration performer, which allows for the averaging to occur during the cycles. The following figure shows the symbol for the op amp that is used throughout this report.
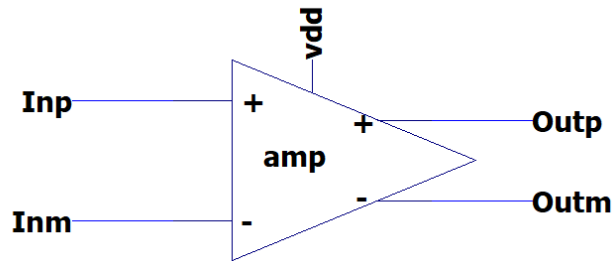

Figure 10 – Op Amp Symbol

The chosen feedback path, discussed later in this report, has the ability to detect mismatches and nonlinearities that may be present in the path; this allows for the use of a less accurate op amp (that will perform relatively similar). Additionally, the gain of the op amp does not have to be that large. A simple self-biased op-amp could be used. Thus, the topology for the op amp shown in Figure 11 was used.
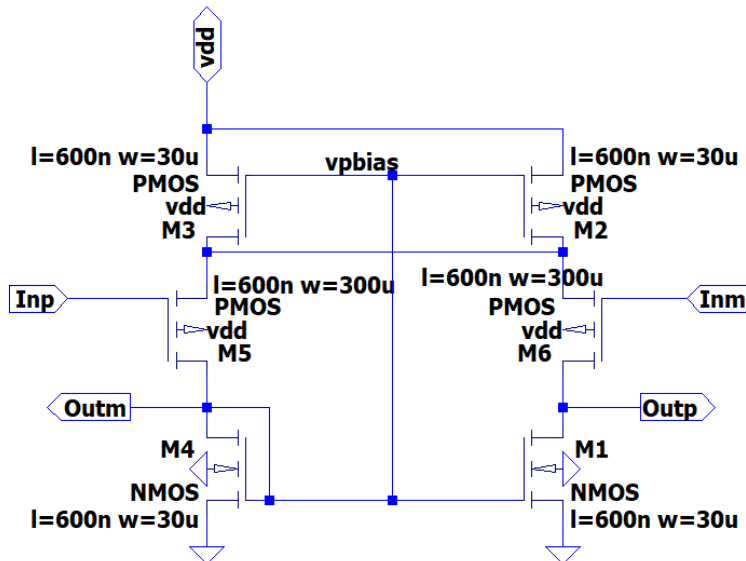

Figure 11 – Op Amp Topology

To simulate the op amp, one of the inputs was swept over five volts and the other was kept at VCM, as that is one of the inputs to the op amp in the final design. It is shown that the amplifier has a gain value of around 20, which was sufficient for this design. Additionally, an AC simulation was run, and its output shows the signal settle on 27 dB, and the frequency start to drop off at around 100-200 MHz, but operating as expected throughout the frequencies in question. These simulations are shown in Figures 12a and 12b.
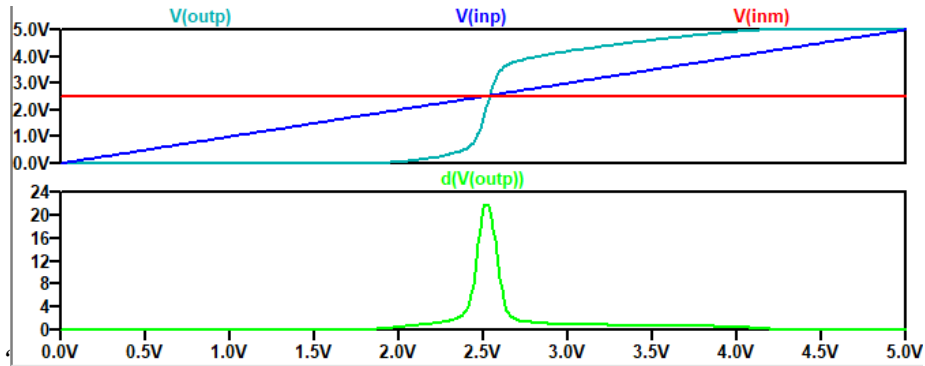

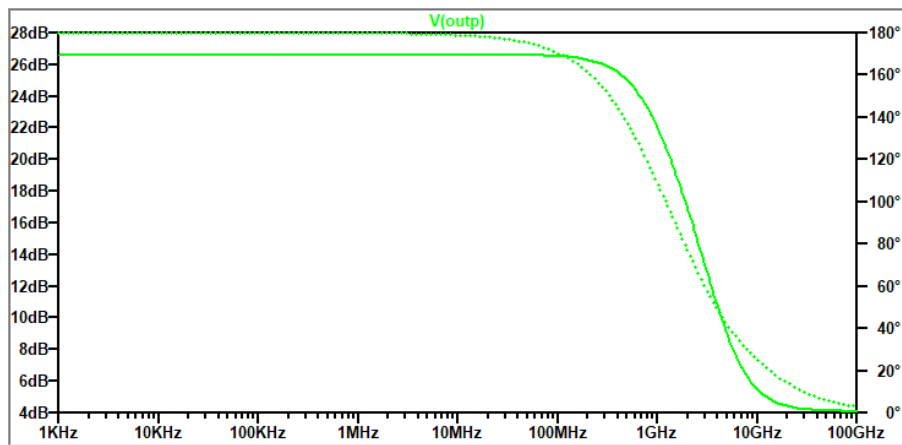
Figure 12a – Simulating the Op Amp

Figure 12b – Simulating the Op Amp

Feedback Signal Control:

Finding an appropriate feedback signal controller was the last main element for this design. Both high and low voltage signals would need to be passed, so a transmission gate of parallel NMOS and PMOS devices was designed. The clock signals Minimum devices were not used for these devices because sizing them up allows for a minimum voltage drop across them, which is useful for the circuitry. The figure below shows the symbol that was used for the transmission gates (that will be used throughout the report) at well as the full circuitry.
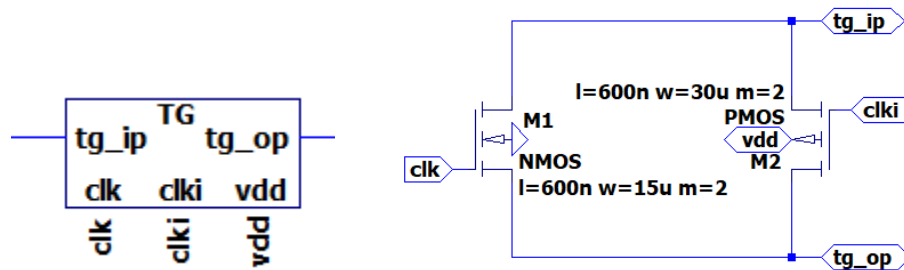

Figure 13 – Transmission Gate Symbol and Schematic

These transmission gates are designed to take in both a clock signal and a clock signals compliment. Thus, when the clock goes HIGH, the NMOS will turn on. Since the clock is HIGH, the compliment of the signal is LOW, turning the PMOS on. Hereby, an effective pass gate is created at each clock edge. Note that each transmission gate has different clock signals/complements attached in the feedback path; also note that the transmission gates that are in the same path are the clock signals that are closest to each other. This allows for the first clock to run, pass through, and then the second clock to run and pass through in the feedback.

Finding Ideal Values

Before running simulations, it is important to know what values are to be expected (at least approximately). Thus, this section will detail some hand calculations and formulas for the Signal to Noise Ratio (SNR) and effective number of bits (N_{eff})

The ideal SNRfor the first order topology is

$$SNR_{ideal}=6.02N+1.76-5.17+30logK$$

and the ideal SNR for the second order topology is

$$SNR_{ideal}=6.02N+1.76-12.9+50logK$$

where K is the OSR and N is the number of bits that the comparator (ADC) uses (N = 1).

The effective number of bits can be calculated by:

$$Neff = \frac{SNR_{ideal} - 1.76}{6.02}$$

Using these formulas, the following ideal values can be calculated.

First Order Ideal Values			
OSR	32	64	128
SNR$_{ideal}$	47.8	56.8	65.8
N$_{eff}$	7.64	9.1	10.6

Second Order Ideal Values			
OSR	32	64	128
SNR$_{ideal}$	70.1	85.2	97.3
N$_{eff}$	11.4	13.9	15.8

Figure 9.32 Simulated Values:

1st Order, 8-Path KD1S				
Power Consumption = 66 mW				
OSR	64		128	
Mode	Serial	Parallel	Serial	Parallel
F$_{s,new}$	1825 MHz	212 MHz	1825 MHz	212 MHz
SNR	38.01 dB	34.51 dB	41.02 dB	38.99 dB
Neff	6.01 Bits	5.43 Bits	6.52 Bits	6.25 Bits
Bandwidth	14.28 MHz	14.27 MHz	7.13 MHz	7.13 MHz

First Order Design

This section of the report shows the fist proposed design to replace the ADC in Fig. 9.32 using the components mentioned above. It is a first order, 8-path design of the continuous time KD1S. Figure 14 shows the schematic and Figure 15 shows the simulated waveform.
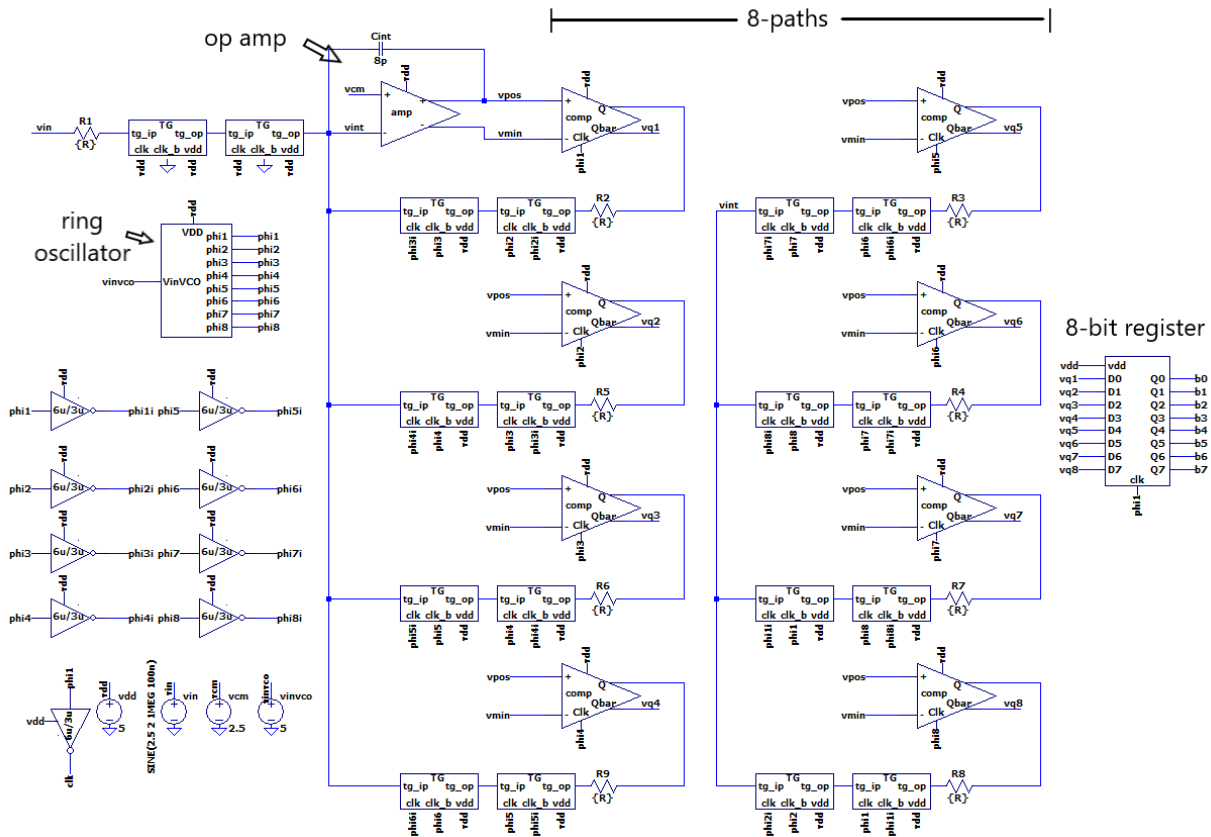

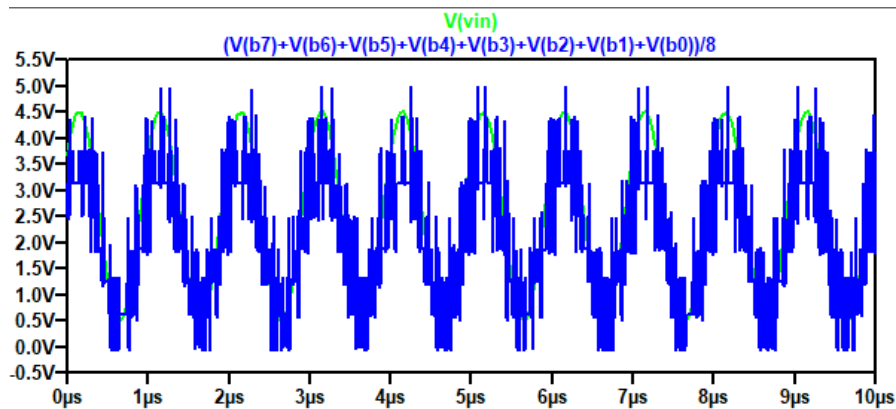*Figure 14 – First Order, 8-Path Schematic*

Figure 15 – First Order, 8-Path Waveform

As shown from the waveform, the output is averaged over the eight different "b" outputs of the register. Overall, the design works as expected, but definitely has some undesirable transient spikes which are somewhat expected with nonideal designs. A future design would want to address these issues. To further inspect them, a ramp input was inputted to the design to test how the output looked. Figure 16 shows the results. The transient spikes are still abundant and there are a few small dead zones that would want to be addressed with this design in future work.
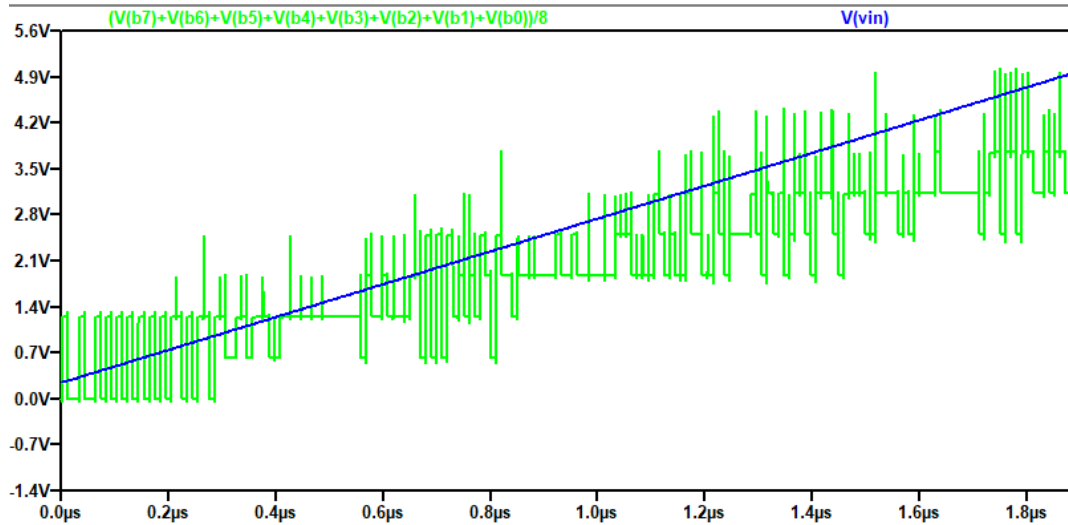

Figure 16 – First Order, 8-Path Ramp Function Simulation

The next test performed on the first proposed circuit was finding the power consumption. Since this circuit only uses one op amp, it is expected to consume less power than a second order op amp. It proves to consume about 57 mW, which is indeed less than the second order design.
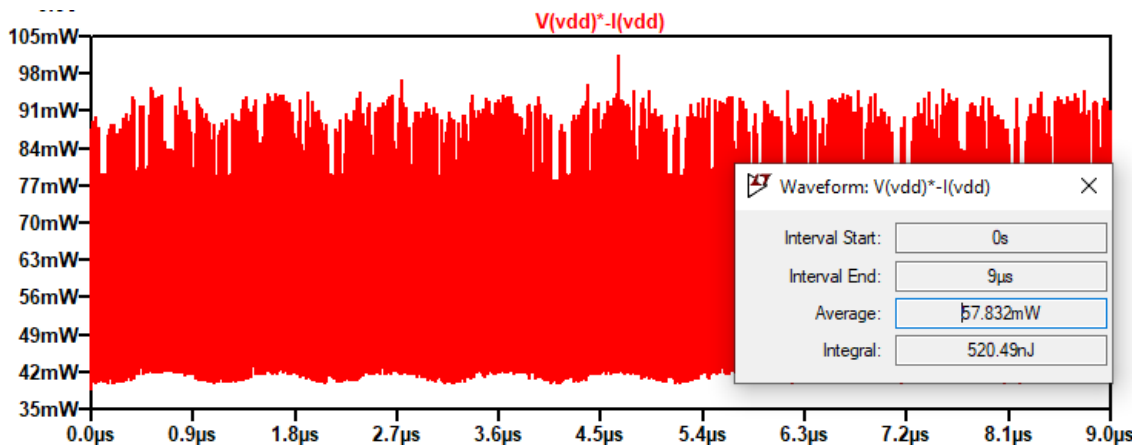

Figure 17– First Order, 8-Path Power Consumption

The following images show the spectrum of the circuit, simulated through MATLAB. The plots created from the script confirm that as the OSR is increased, the noise decreases in the bandwidth of interest. This is to be expected and is probably due to it being pushed to higher frequencies.
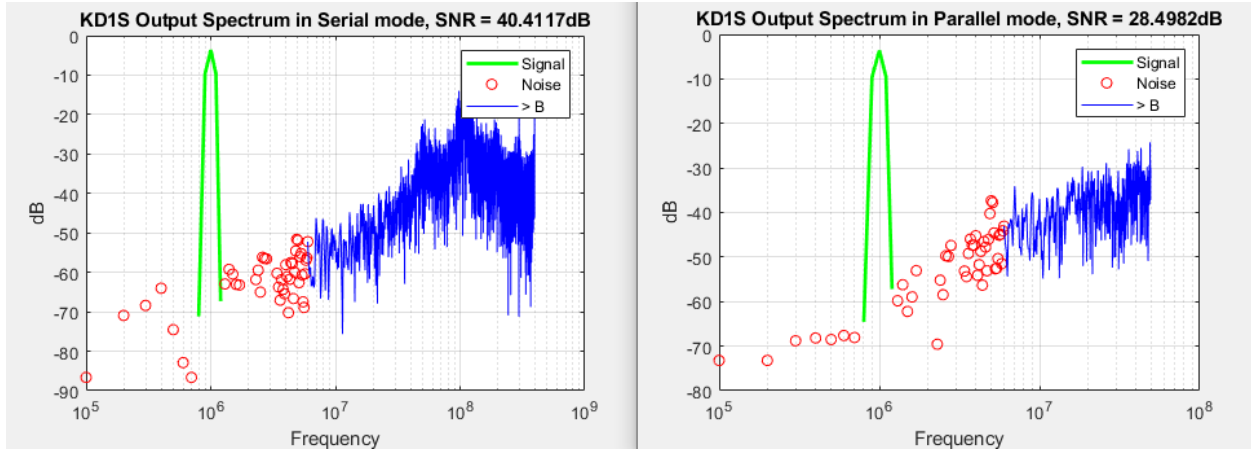

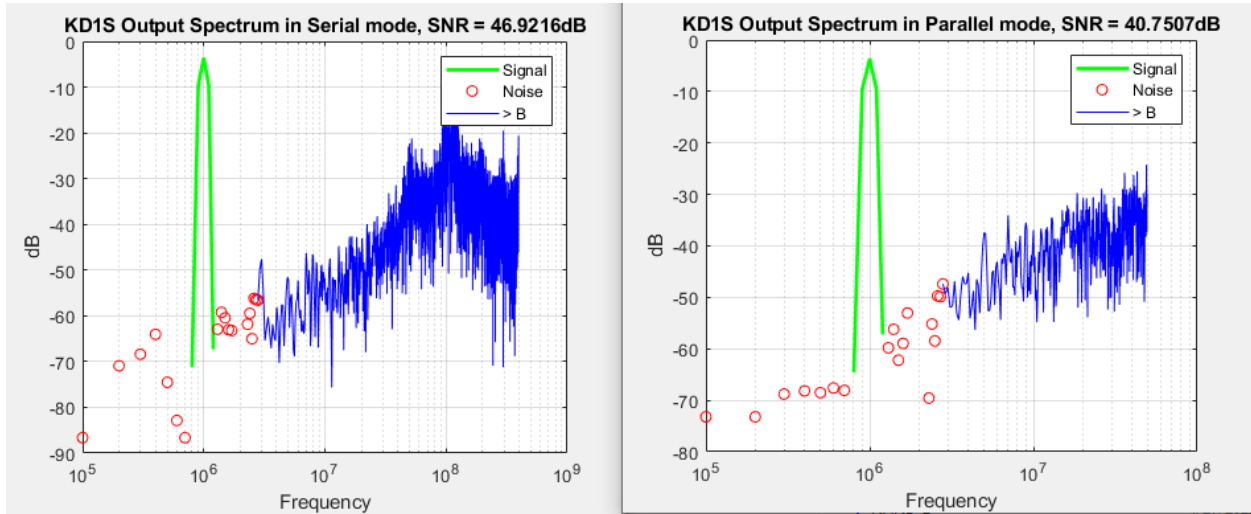*Figure 18 - MATLAB Spectrum Files, First Order, 8-Path, OSR = 64*

Figure 19 - MATLAB Spectrum Files, First Order, 8-Path, OSR = 128

Second Order Design

This section of the report shows the second proposed design to replace the ADC in Fig. 9.32 using the components mentioned above. It is a second order, 4 path design of the continuous time KD1S, and is the recommended design in comparison. Figure 20 shows the schematic and Figure 21 shows the simulated waveform.
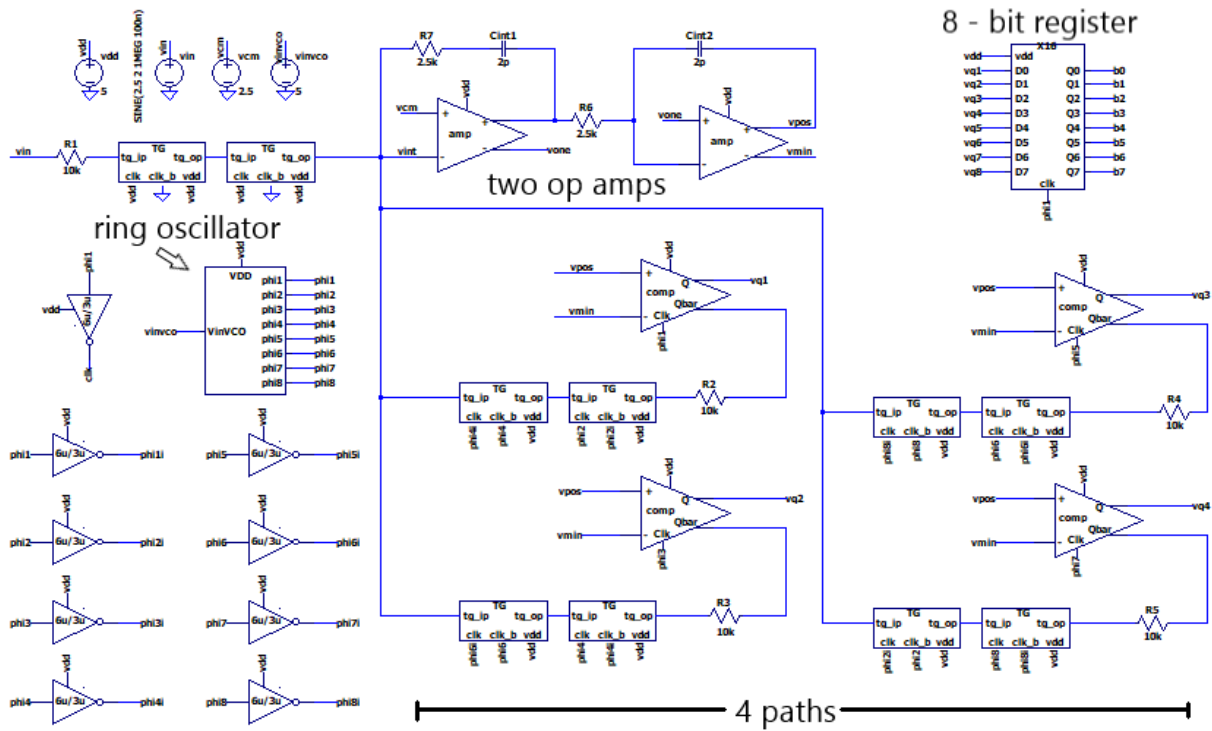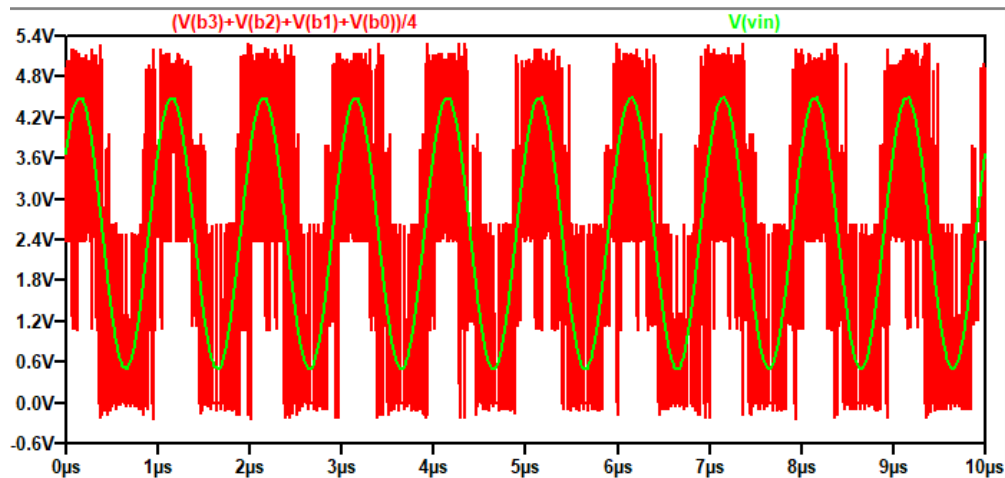

Figure 20 – Second Order, 4-Path Schematic

Figure 21 – Second Order, 4-Path Waveform

Again, the output of the waveform is showing an averaged value per time unit over the eight different "b" outputs of the register. This design works slightly better than the eight-path design with all things considered. To further inspect the circuit, a ramp input was inputted to test how the output looked. Figure 22 shows the results. The dead zone error seems to be fixed in this version, however, the transient spikes seem slightly worse.
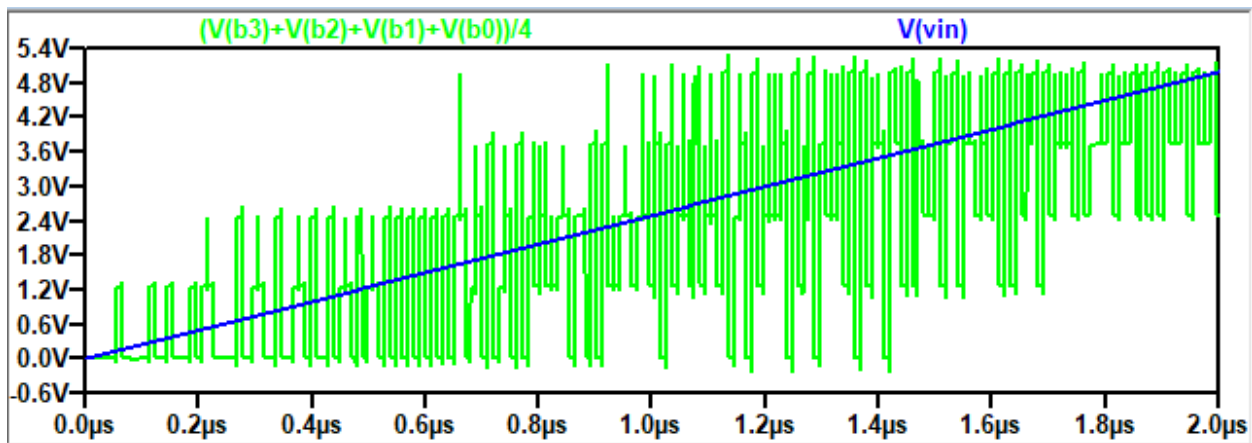

Figure 22 – Second Order, 4-Path Ramp Function Simulation

Next, the power consumption was tested for. The op amp is the part of the design that consumes the most power; this design was expected to consume more power overall because it makes use of an extra op amp. It proves to consume about 80 mW, which makes it the higher power consumer of the two proposed designs designs.
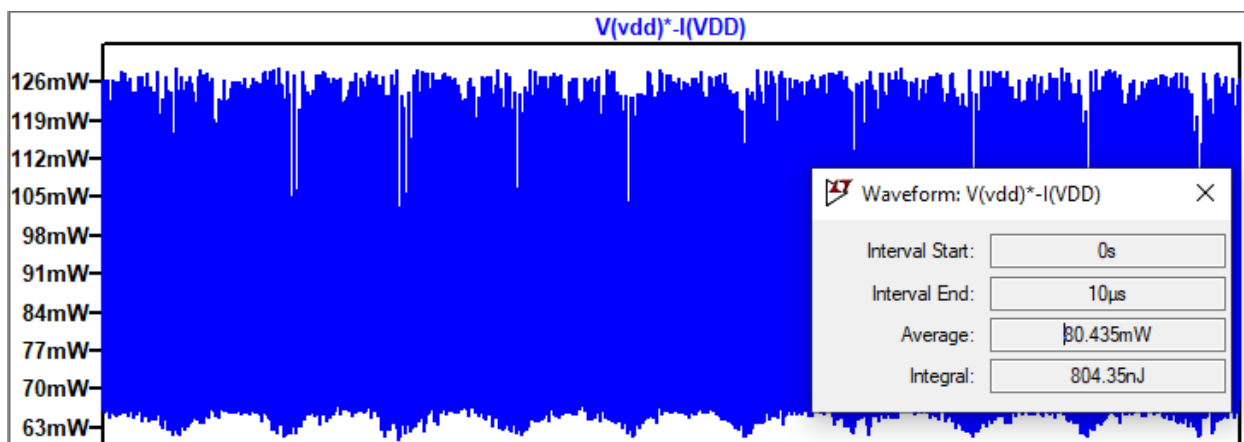

Figure 23– Second Order, 4-Path Power Consumption

The following images show the spectrum and SNR of the circuit in both parallel and serial modes, simulated through MATLAB. The plots created from the script confirm that as the OSR is increased, the noise decreases in the bandwidth of interest. This is to be expected and is probably due to it being pushed to higher frequencies. Additionally, the MATLAB code showed the number of effective bits, bandwidth, and sampling frequency, all of which is described in Table 1.
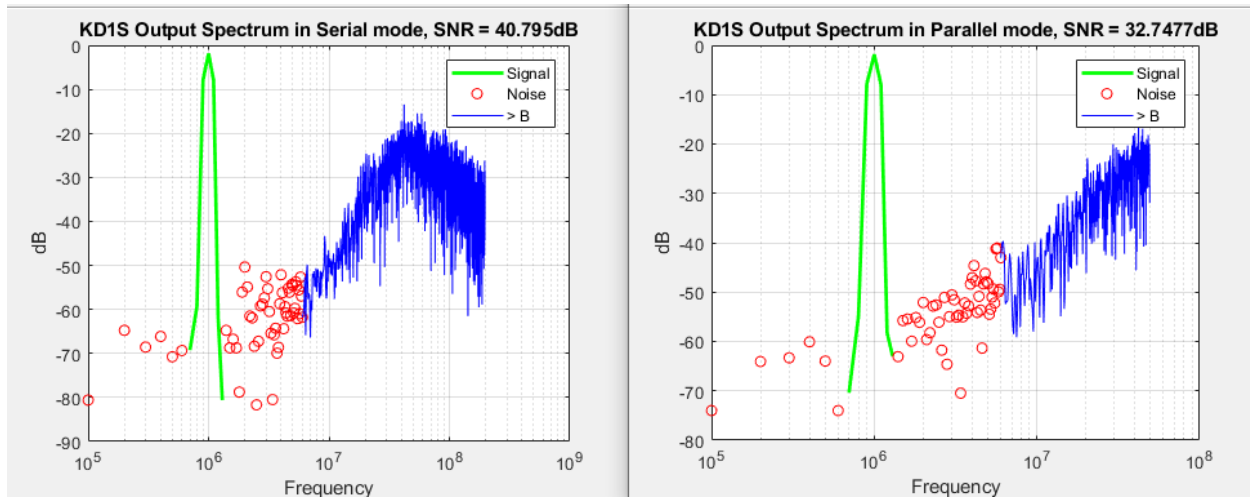

Figure 24 -MATLAB Spectrum Files, Second Order, 4-Path, OSR = 32
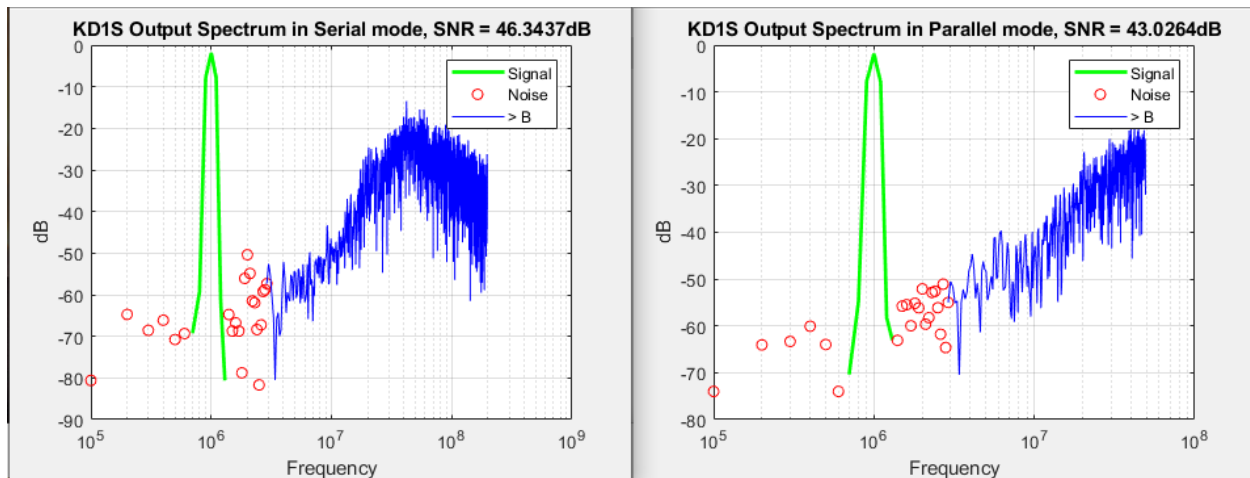
Figure 25 - MATLAB Spectrum Files, Second Order, 4-Path, OSR = 64

Again, the noise is reduced when the OSR is increased, confirming that the circuit is operating properly. Since this design includes the second integrator, it is expected that more noise shaping will occur. It is clear from these simulations that although a lower sampling rate was used in the second order design, the design generally works better than that of the first order eight path design.

Summary and Analysis of Results

Summary:

The first proposed design of this paper was the first order, 8-path CT KD1S. Though this design worked, it was outperformed in many categories by the second proposed design, which was the second order, 4-path design. While the power consumption on the first design was smaller, the filtering technique of the second one performed better and is the final chosen design for this project. In comparison to the simulation from Figure 9.32, the SNR, N_{eff}, ect. values that were found for the chosen design are definitely within the ballpark of the example given in the book. However, the proposed design does perform slightly worse than the book design due to the lack of nonideal components and simulation error that is bound to occur.

Design Tradeoffs:

This design, as with every other design, had associated design tradeoffs that came with making decisions for each component. For instance, a tradeoff that was made in the final decision for the proposed design involved picking a design that filtered better over a design that consumed less power. Obviously, if a design has opposite constraints, the first order design can be used; however, for most practical designs, the second order, four path design would probably be a better fit.

Additional tradeoffs were made with the oscillator, the op amp, and the comparator. As mentioned previously, this differential ring oscillator was chosen because it allows for adjustment in frequency (it is voltage controlled). The tradeoff associated with this is that the duty cycle associated was just over fifty percent, which can cause some errors. Furthermore, the op amp did not prove to need exceptionally high gain, so a simple topology was used as opposed to a more complex one. This comes with the con of a higher error term, but it saves layout space and power consumption while still allowing for the design to work properly. As for the comparator, a very accurate design is useful for this application. This leads to a better SNR and N_{eff}, as the operation of each of the feedback paths relies on this. Having a sensitive and accurate comparator comes at the cost of layout space and extra devices, but was a tradeoff that seemed necessary given its pros.

Future Work and Conclusion

Future work for this design should probably begin with the clock generator, as getting the duty cycle to fifty percent would aid in the optimization of the results. Additionally, changes to the clock generator could allow for a sixteen-path design to be investigated, which could be valuable in some applications. If a sixteen-path design was similarly implemented, it could account for better SNR.

Two designs were proposed in this report for replacement of the ADC in Figure 9.32 of the textbook. Though the chosen design does not fully meet the same specs as the given ideal discrete time design from the book, it does work relatively well for the application. The specs are outlined in Table 1, and they are in the same range as the values simulated for the given design.