Jazmine Boloor
EE 421: Digital Electronics
Dr. R. Jacob Baker
December 2020

The following report details a switching power supply controller chip for a flyback switching power supply (SPS). It was designed to meet the following specifications using On Semiconductor's 500nm process:

- The design is a chip to be used on a printed circuit board.
- The output of the circuit should be nominally 12.5V and be able to supply well beyond 2A of current and work with other load currents including 0, 10mA. 200mA, ect.
- The design should use the C5 Process.
- The design should use the bandgap voltage reference circuit.
- A report should be submitted characterizing the design, specifically design considerations and associated schematics, and tables characterizing the behavior (especially power from the 5V supply)
    - Clear and concise images of some simulations used to generate the data you entered in your tables.
    - For example, how does your design work at VDD = 4V and temperature of 100C? Characterize your design with changes in temperature and VDD
- Your report should also detail where you think someone trying to improve your design (future work) should focus their time and efforts.

The following tables summarize the most efficient range of power, efficiency, and temperature results for this design. The report will encompass more extensive results, with more test values for each section (including larger and smaller loads and temperatures). Additionally, tradeoffs and design choices will be discussed.

Load Current	**R_{Load}**	**Average Current Supplied by Power Supply**	**Average Power Dissipated by Power Supply**	**Efficiency of Power Supply**
VDD = 5 V				
100 mA	125 Ω	7.818 mA	39.09 mW	94.05 %
2.5 A	5 Ω	190.3 mA	951.5 mW	96.60 %
VDD = 4 V				
100 mA	125 Ω	7.725 mA	30.9 mW	95.18 %
2.5 A	5 Ω	199.8 mA	79.92 mW	92.00 %

Table 1: Power and Efficiency from Supply

Load Current	R_{Load}	Average Current into SPS Chip	Average Power Consumed by SPS Chip	Average Current Exiting SPS Chip	Average Power Dissipated by SPS Chip
VDD = 5 V					
100 mA	125 Ω	3.353 mA	16.765 mW	1.511 uA	
2.5 A	5 Ω	2.079 mA	10.395 mW	164.4 nA	
VDD = 4 V					
100 mA	125 Ω	3.353 mA	1.511 mA	1.535 uA	
2.5 A	5 Ω	2.079 mA	1.575 mA	4.282 uA	

Table 2: Power Consumed and Dissipated from Chip

Temperature	Average Power Supplied by Power Supply (Load = 2.5A) (VDD = 5 V)	Average Power Supplied by Power Supply (Load = 100 mA) (VDD = 5)
0	977 mW	39.2 mW
30	988 mW	39.1 mW
60	989 mW	38.62 mW
90	1.04 W	39.32 mW
120	1.108 W	40.8 mW

Table 3: Change in Power Consumed with Increasing Temperature

The Flyback SPS Design:

The Flyback Switching Power Supply (SPS) is a very commonly used SPS in consumer electronics. Its use of two different ground planes – one for AC and one for DC – increases the safety factor of the design so much so that they can be used for common items such as computer chargers. The AC line side of the SPS can operate with a very large current, but this current is controlled significantly on the DC side because of the transformer. This means that the DC side – the side the consumer will have access to – will be far less dangerous than if there were not separate ground planes. Figure 1 below shows the external circuitry of the Flyback SPS, including the symbol view of the controller chip designed.

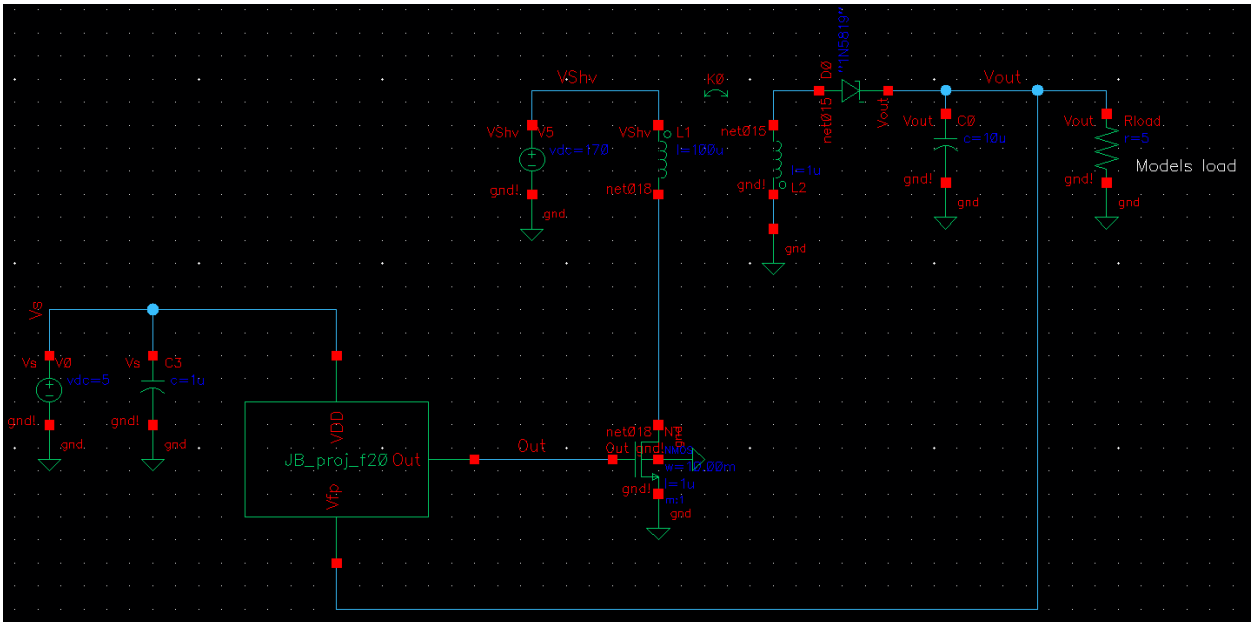


Figure 1 – Flyback SPS

The Transformer and MOSFET:

The NMOS shown in the schematic in Figure 1 is used to operate the transformer through its switching abilities. To be more specific, the output of the controller chip (discussed later in the report) will either turn the NMOS on or off. If the transistor is turned on, it will pull current through the primary of the transformer, supplied from the 170 V source. This constant voltage application will linearly increase the energy stored in the primary. One the transistor is turned off, the energy stored in the primary will transfer to the secondary side, causing a current to flow. This will leave miniscule energy in the transformer primary, which will rebuild the next time the NMOS switch turns on.

The Schottky Diode, Filter Capacitance, and Load

The Schottky diode portrayed in Figure 1 is used on the smaller voltage, DC side of the SPS. It allows current to conduct from the secondary side of the transformer toward the output of the circuit. This will only be on after the NMOS switch turns off and the energy from the primary of the transformer moves to the secondary. The capacitor was chosen to be 10uF, as it filtered the output with an acceptable level of hysteresis while keeping cost relatively low. The load resistance was varied, but optimal values were found between 5Ω and 1.25kΩ. These resistance values along with a Vout centering around 12.5V will create load currents ranging

from 10mA to 2.5A. Other values for this load resistance, both smaller and larger, will operate the device, but do so at a much smaller efficiency.

The SPS Controller Chip Design:

The SPS controller chip utilizes five main components: a bandgap reference circuit, a comparator, a NAND gate, a ring oscillator, and a buffer. The symbol view design of the chip is displayed in Figure 2. The complete operation of each component is detailed in each of the following sections of this report. In short, this chip takes in a voltage from the external circuitry shown in Figure 1, Vout, and sends it through a one-tenth divider. Vout should fluctuate around 12.5 V (with hysteresis), so the one tenth divider will create a voltage around the same range as the bandgap reference voltage. This voltage will enable or disable the ring oscillator (decided by the NAND gate). Then, this voltage will go through a buffer to square the signal. This voltage, high or low, will decide whether the NMOS in Figure 1 will turn on or off. The rest of the external circuitry is further discussed in the Flyback SPS section of this report.

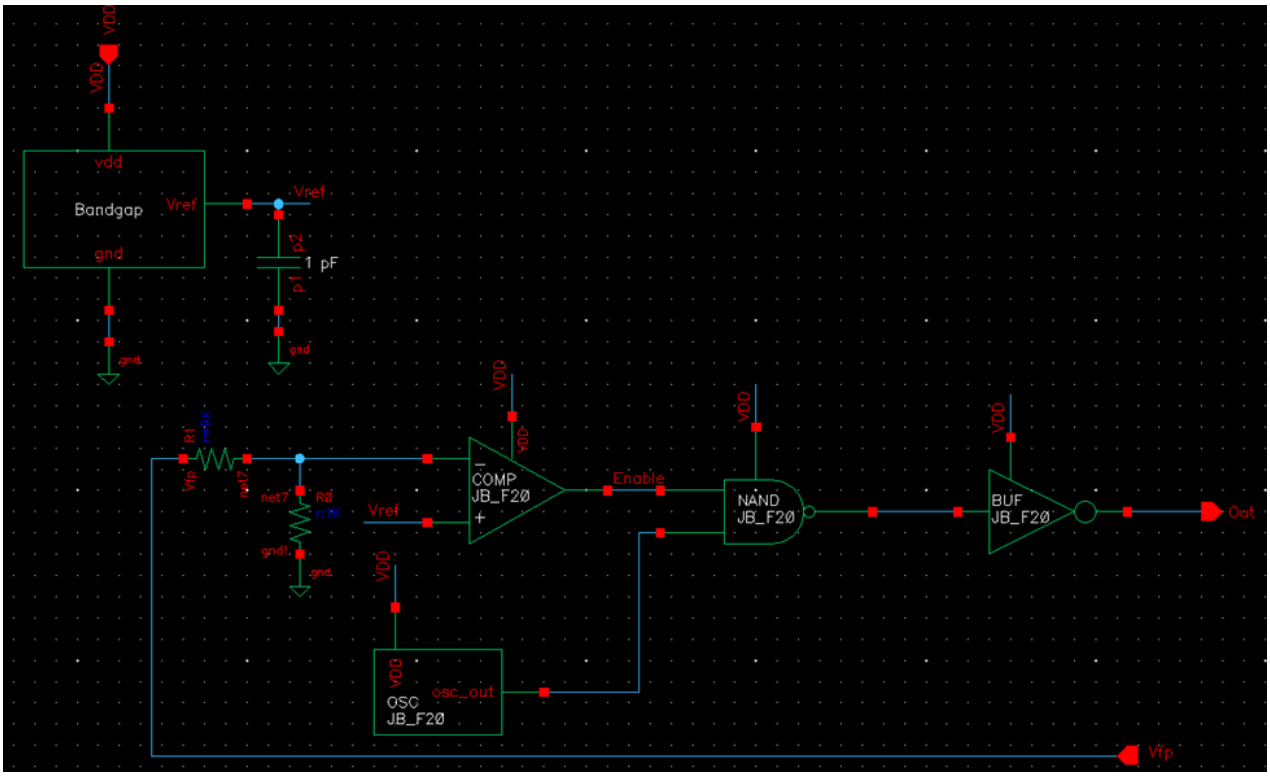


Figure 2: The SPS Chip

The Bandgap Reference Circuit:

The Bandgap Design:

A bandgap reference circuit is a voltage reference circuit that generates a near constant voltage for a wide range of temperatures and power supply voltages. This bandgap, shown in Figure 3, levels at 1.25V, showing minuscule changes in various settings. Its durability made it an ideal circuit to compare the output of the SPS to. This is the voltage seen in Figure 2 and 3 as Vref. The following simulations more specifically characterize this design. Note that the schematic design on the bandgap circuit was provided for this project.

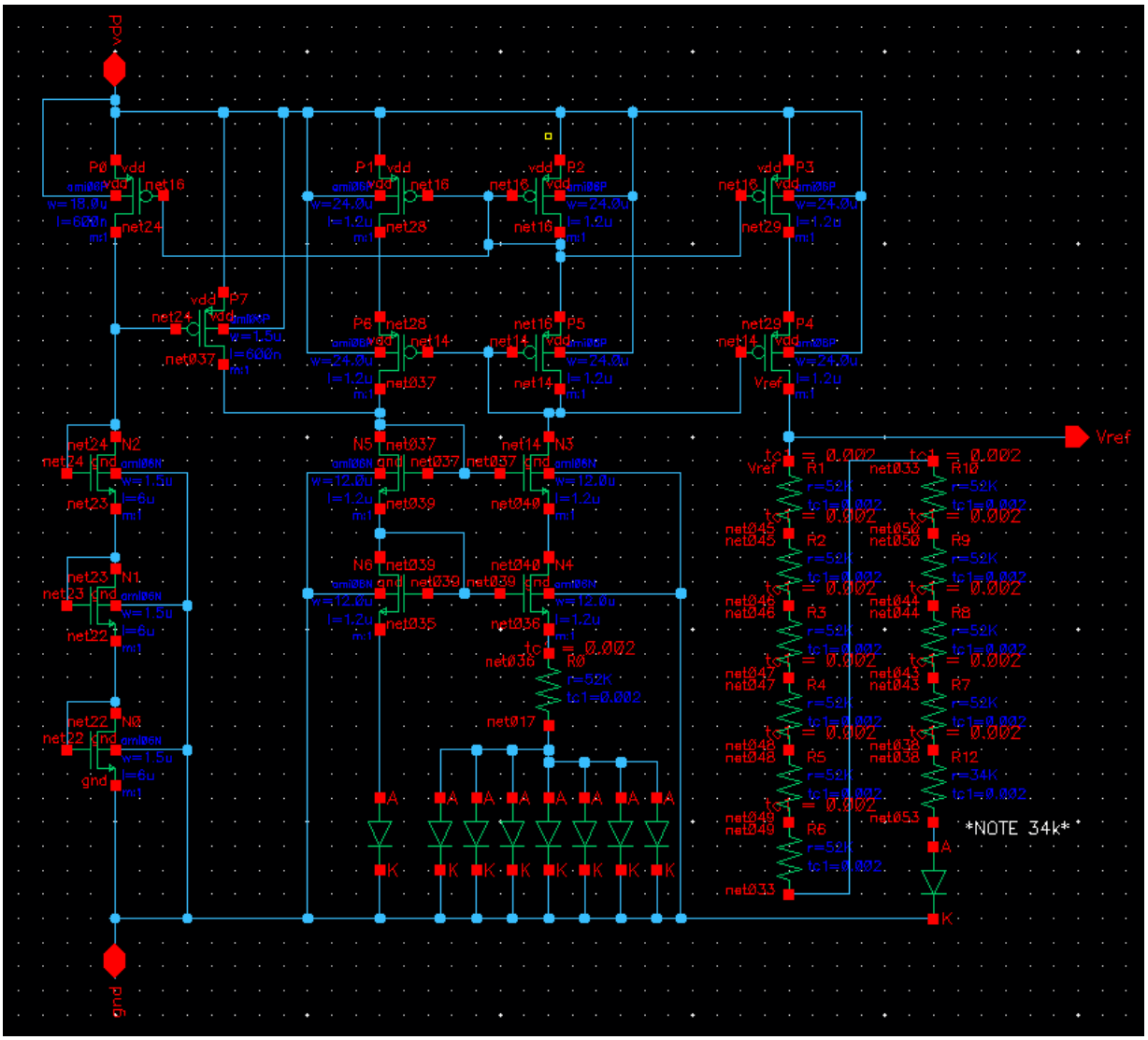


Figure 3: Bandgap Reference Circuit

Vref with Increasing VDD

Figure 4 shows the simulation of Vref as VDD changes. The pink simulation shows that Vref increases at a rather fast pace when VDD is swept across 3-3.5 V. After this point, it flattens out to a value that increases at a much smaller pace. Thus, it is observed that when VDD is 3.5 V or higher (until at least 6V, according to the simulation), Vref shows a voltage of around 1.25V. Moreover, 3.5V is the lowest value for VDD that will not cause a relatively large drop in output voltage.

The yellow simulation (the current at the input node of the bandgap) shows that the bandgap is drawing a current of around 3.25 uA for a VDD of 5V. As VDD is increased, the current draw also increases; as VDD is decreased, the current draw also decreases.

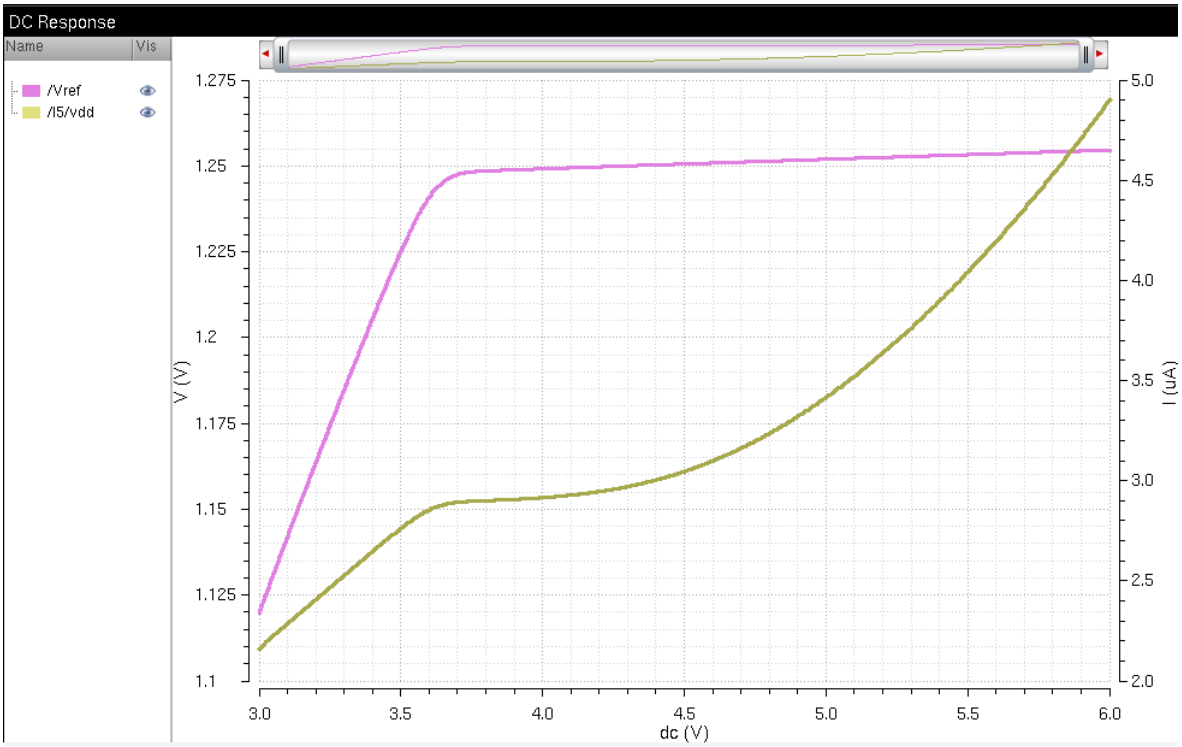


Figure 4: Vref with Increasing VDD

Vref with Varying Temperature

The simulation displayed in Figure 5 shows the Vref-temperature curve of the bandgap. The temperature is swept from 0˚C to 100˚C. This causes a voltage decrease from about 1.253V to 1.245V. Thus, Vref only changes about 0.07V for a 100˚C change in temperature.

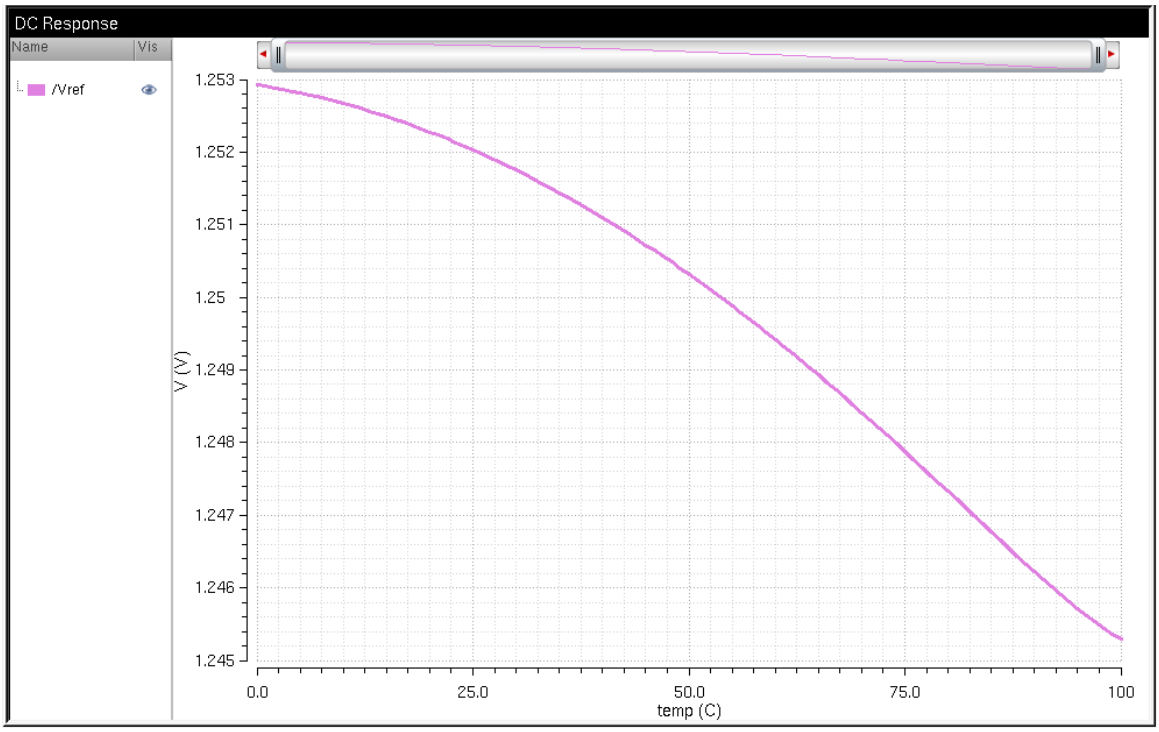


Figure 5: Vref with Varying Temperature

Vd with Varying Temperature

Figure 6 illustrates that as temperature increases, the forward bias potential of the diode, Vd, decreases linearly. The temperature is swept from 0˚C to 100˚C, and the voltage drops from around 765mV to 575mV. Thus, for the 100˚C change in temperature, there is approximately a 190mV change in forward bias potential in the diode. Furthermore, this shows that as temperature increases, less and less voltage will be needed to forward bias the diode; as temperature decreases, more and more voltage will be needed to forward bias the diode. The simulation also displays a forward bias voltage at room temperature (around 20-22˚C) to be around 700-725 mV.

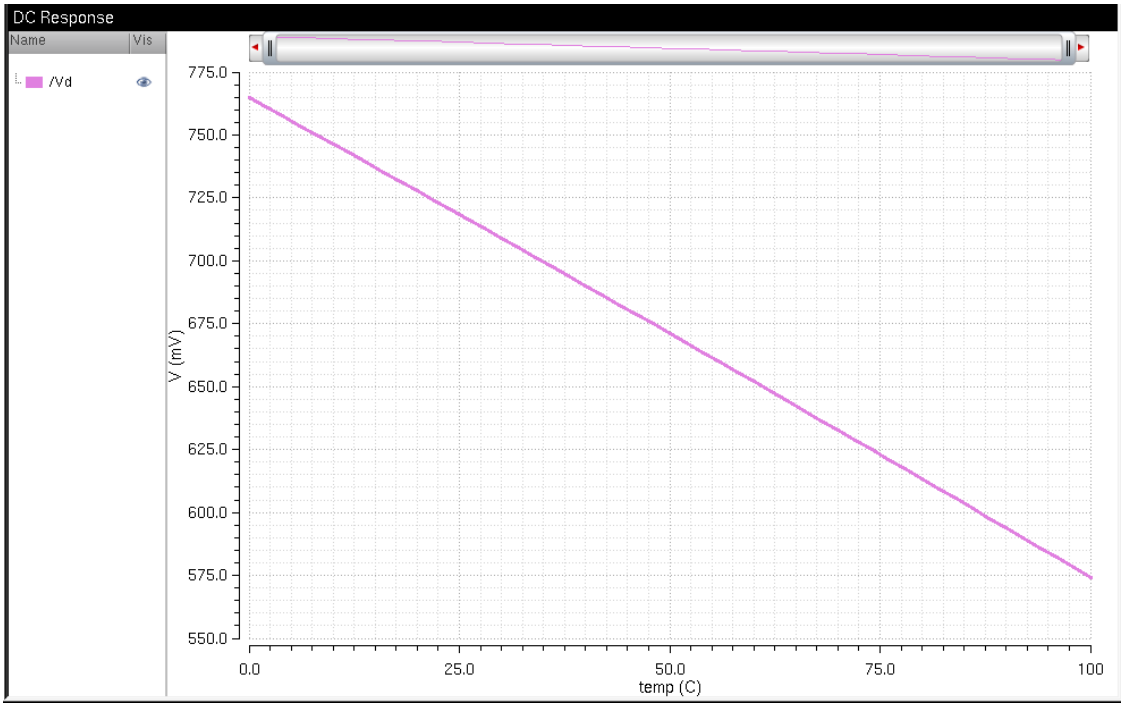


Figure 6: Vd with Varying Temperature

IV Curve of the Diode

The simulation depicted in Figure 7 displays that when the voltage potential across the diode is less than its forward bias potential, it does not conduct current. The sharp uptake in the current occurs when the diode turns on, which will happen when the diode is forward biased. The forward bias potential of this diode can be seen around 700mV, depicted on the image. At this voltage, the diode begins conducting current.

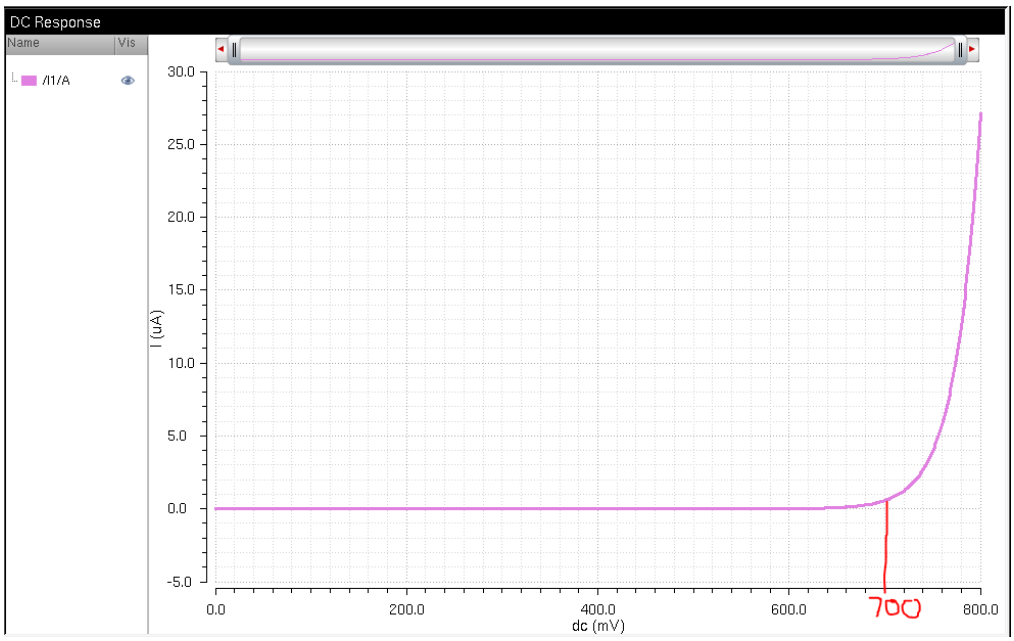


Figure 7: IV Curve of the Diode

Layout of the Bandgap

Figure 8 shows the layout of the bandgap circuit. The Layout Versus Schematic (LVS) verification concluded that the layout matches the schematic shown in Figure 3.

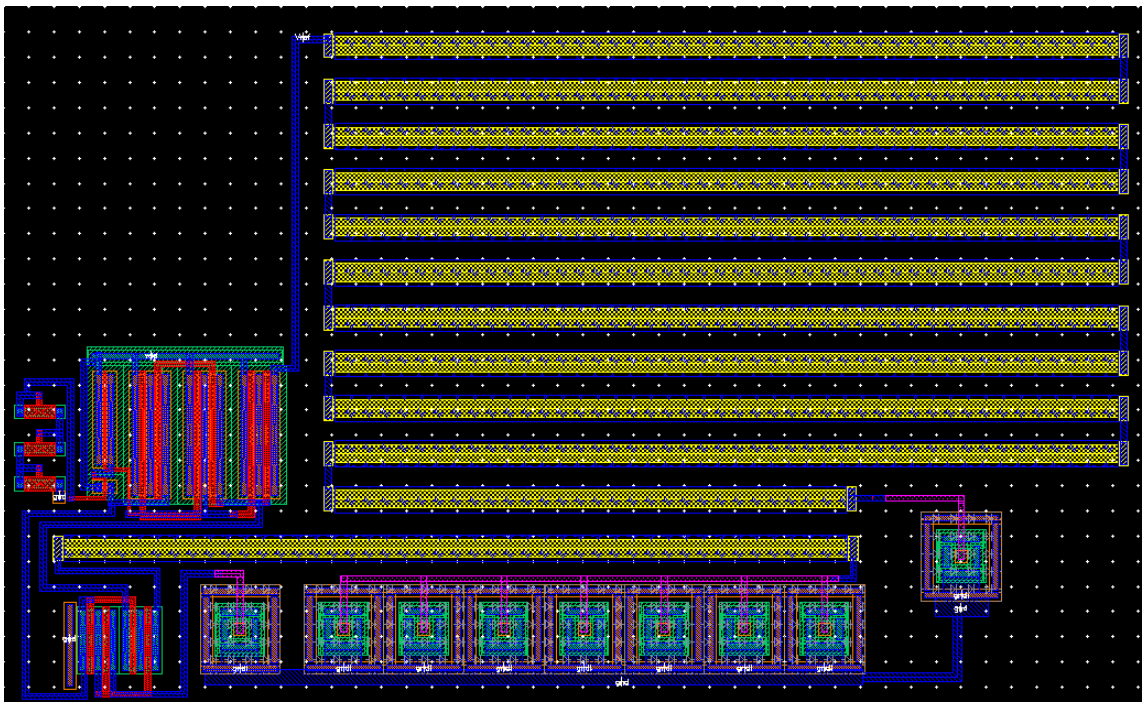


Figure 8: Layout of Bandgap

The Comparator:

The Comparator Design:

The comparator shown in Figure 9 utilizes three N-flavor difference amplifiers and two inverters all in parallel. Cascading three diff-amps came with optimal performance for a wide range of voltage levels. The diff-amps use NMOS devices that are 10/1 and PMOS devices that are 10/1, with exception of the tail NMOS devices which measure 10/2. The decision of the device sizes came with associated tradeoffs between power, speed, and layout size. The lengths of the tail transistors were doubled to save a small amount of power, though this came at the cost of layout area and speed. The length increase was justified because the performance of the device had unnoticeable differences. In addition to this, the W/L ratio for devices with equal resistances in the C5 process are 10/1 for NMOS and 20/1 for PMOS. Decreasing the width of the PMOS devices to 10/1 changed the resistance of the devices, therefore changing the switching voltages. Modifying these switching voltages did not significantly change the output of the comparator, and it came with the benefit of less power consumption and smaller layout area. In short, the tradeoff between power, speed, and layout size was weighed to pick transistor sizes for the diff-amps.

The two inverters on the right side of Figure 9 were used to smooth the square waves that the comparators output. Though the cascaded diff amps reach voltages levels that are close to VDD and GND, they do not fully reach either of these values. These inverters better ensure that output of this comparator does in fact reach full logic levels. The first inverter was made PMOS stronger (meaning the PMOS device had a large width), measuring 40/1. This is to move the switching point closer to VDD, better ensuring that the correct value is being passed. The second inverter was sized with a 20/1 PMOS and 10/1 NMOS, providing a switching point around VDD/2. The main purpose of this inverter was to better square the signal. At this point, the output of the comparator was square and correct for all tested loads within range, so the use of any extra inverters was unnecessary. Thus, the final design of the comparator encompasses these components, illustrated in Figure 9 below.

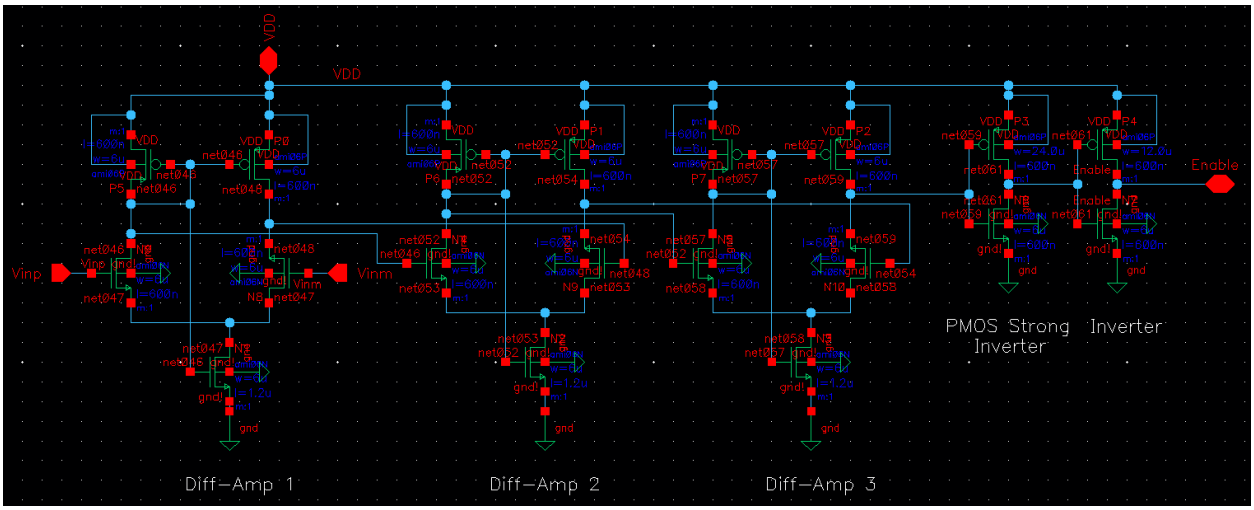


Figure 9: Comparator with Three Diff-Amps and Two Inverters

The Comparator Operation:

This circuit operates by taking a voltage, Vinp, and comparing it to another voltage, Vinm. If the voltage on Vinp is less than the voltage on Vinm, the diff-amp will output low (GND); if the voltage on Vinp is greater than the voltage on Vinm, the comparator will output high (VDD). The operation of this comparator was integral to the design of the SPS chip because it was the controller that enabled the power MOSFET to turn on/off to either increase/decrease Vout when necessary. The SPS design accounts for hysteresis in its output, and this comparator ensures that it does not go above or below a reasonable amount.

The first difference amplifier in the comparator takes in two voltages: one that stems from the bandgap reference circuit and one that stems from Vout on the design shown in Figure 1. The bandgap reference voltage is 1.25V, while Vout is around 12.5 volts, so it is sent though a one-tenth voltage divider (1kΩ and 9kΩ) before it is inputted into the comparator. The design of this Flyback SPS accounts for a certain range of hysteresis on Vout (below 400 mV) because of the small 10uF capacitor discussed in the previous section. This hysteresis will obviously cause a voltage fluctuation around Vout (around 1.22 V to 1.27 V after the voltage divider for a 5Ω load, less for a larger resistive load). Again, this voltage is then compared to the bandgap reference. Specifically, the bandgap reference voltage (1.25 V) is inputted to the plus terminal of the comparator and 1/10 of Vout is inputted into the minus terminal. This is clearly illustrated in the Figure 2 schematic.

When the plus terminal is less than the minus terminal, voltage low is outputted from the comparator. When the plus terminal is greater than the minus terminal, voltage high is outputted from the comparator. Figure 10 shows a test simulation of the comparator. The plus terminal was held at a constant voltage of 1.25 V, (acting as the bandgap reference voltage), and the minus terminal varied from 1.23 V to 1.37 V, (acting as the Vout/10 voltage). Net059 is the output of the diff-amps before they are sent through the inverters, hence the curve they inherit. Moreover, it is clear that the final output is square and ranges from GND to VDD. The layout for the comparator is also shown below in Figure 11. The diff-amps and inverters are both labeled for simplicity in viewing.

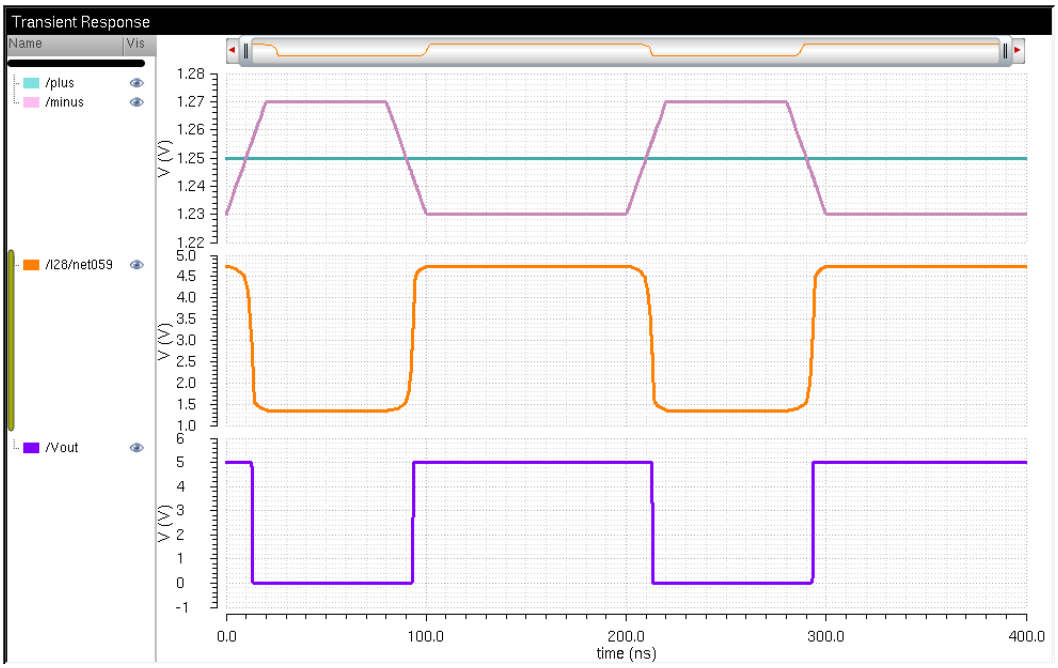


Figure 10: Simulation of Comparator

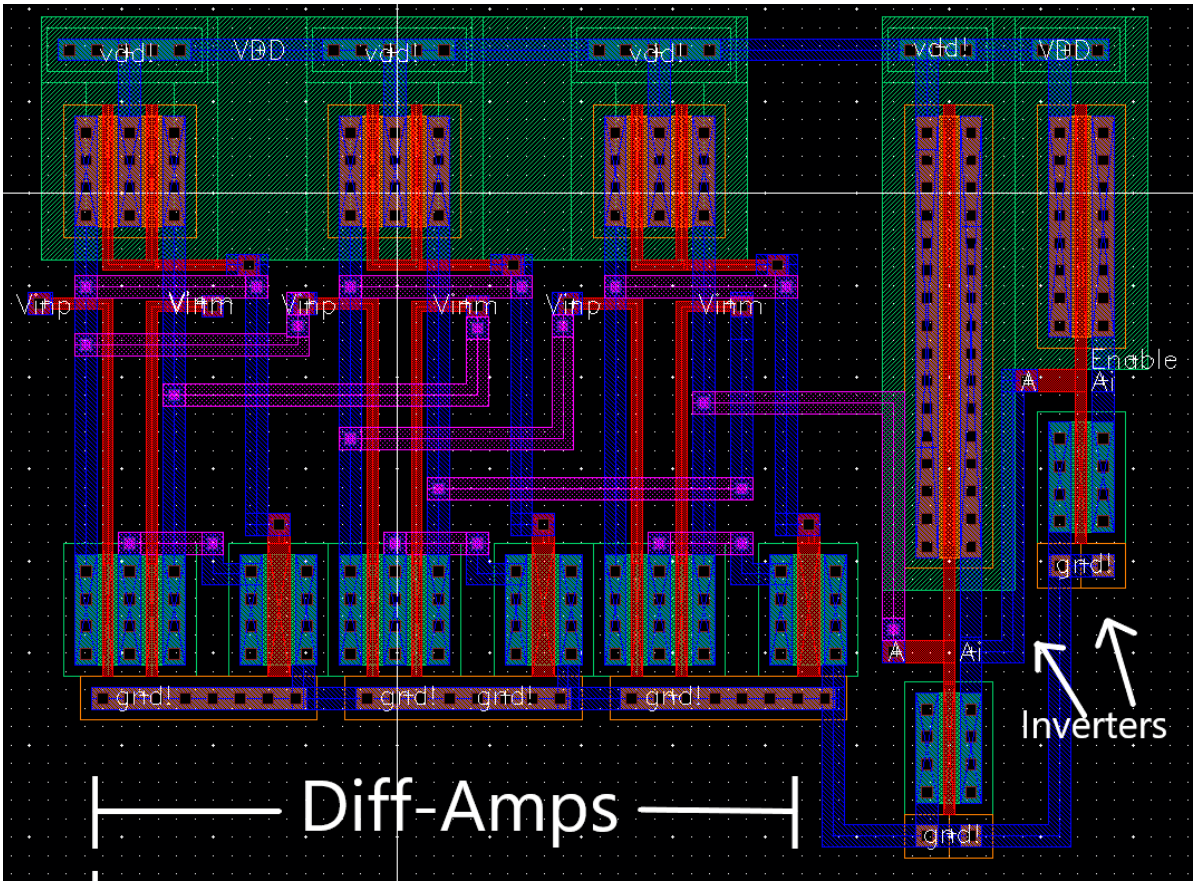


Figure 11: Layout of Comparator

The Ring Oscillator and NAND Gate:

Ring Oscillator Design:

The ring oscillator for this design was to oscillate at a frequency of 5 MHz. This translates to a 200 ns period, as

$$t = \frac{1}{f} \quad \rightarrow \quad 200\ ns = \frac{1}{500MHz}$$

To do this, a series of slow inverters and weak inverters will be used. Figure 12 shows the final design of the ring oscillator. The slow inverters use 10/10 devices for both the NMOS and PMOS, and the small inverters use 10/1 NMOS and 20/1 PMOS devices. In total, thirty slow inverters and seven small inverters were used. Figure 13 shows the output of the oscillator having a period of 198.2 ns. This translates to a frequency of 5.045 MHz, which was within a reasonable range for the frequency.

$$t = \frac{1}{f} \quad \rightarrow \quad 198.2\,ns = \frac{1}{5.045MHz}$$

In addition to the reasonable oscillating frequency, the output also shows very short, clean rise and fall times. The layout of this design is portrayed in Figure 14.

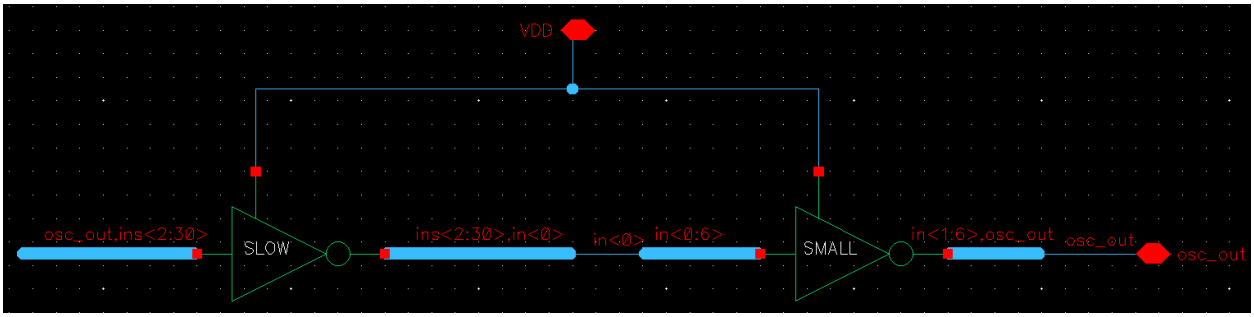


Figure 12: Schematic of ring oscillator using 30 slow inverters and 7 small inverters.

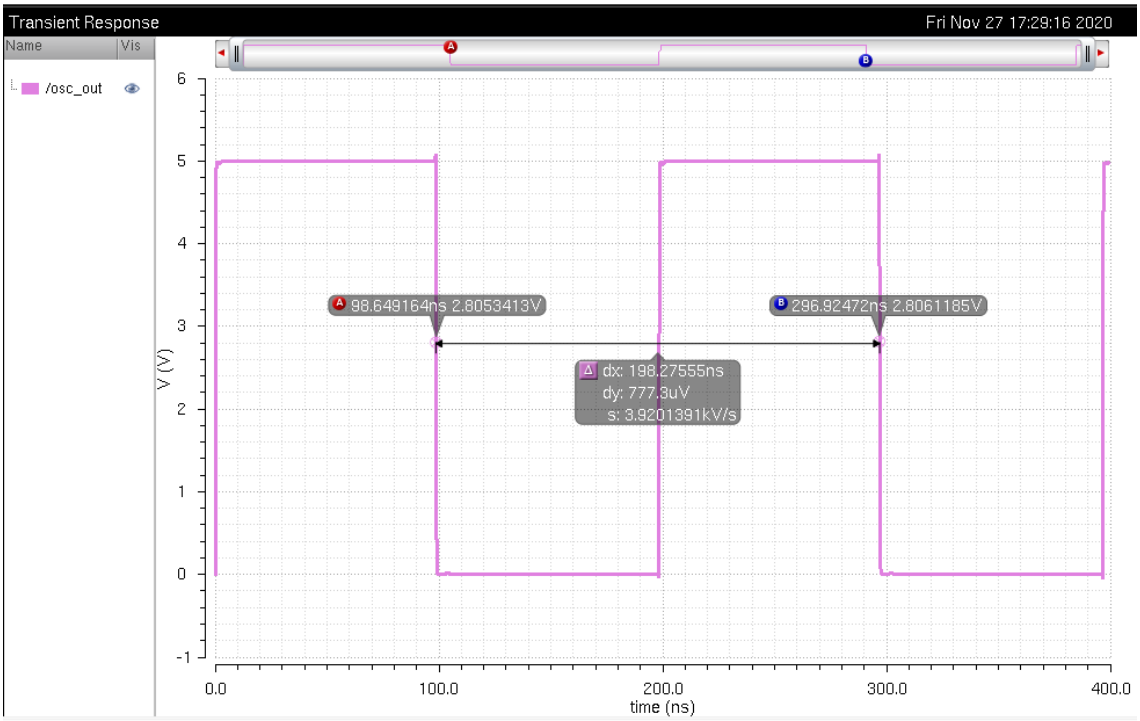


Figure 13: Ring Oscillator Output

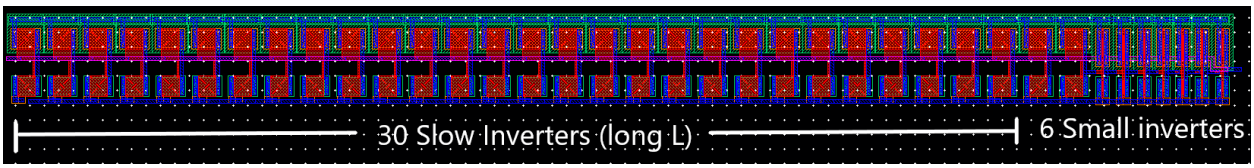
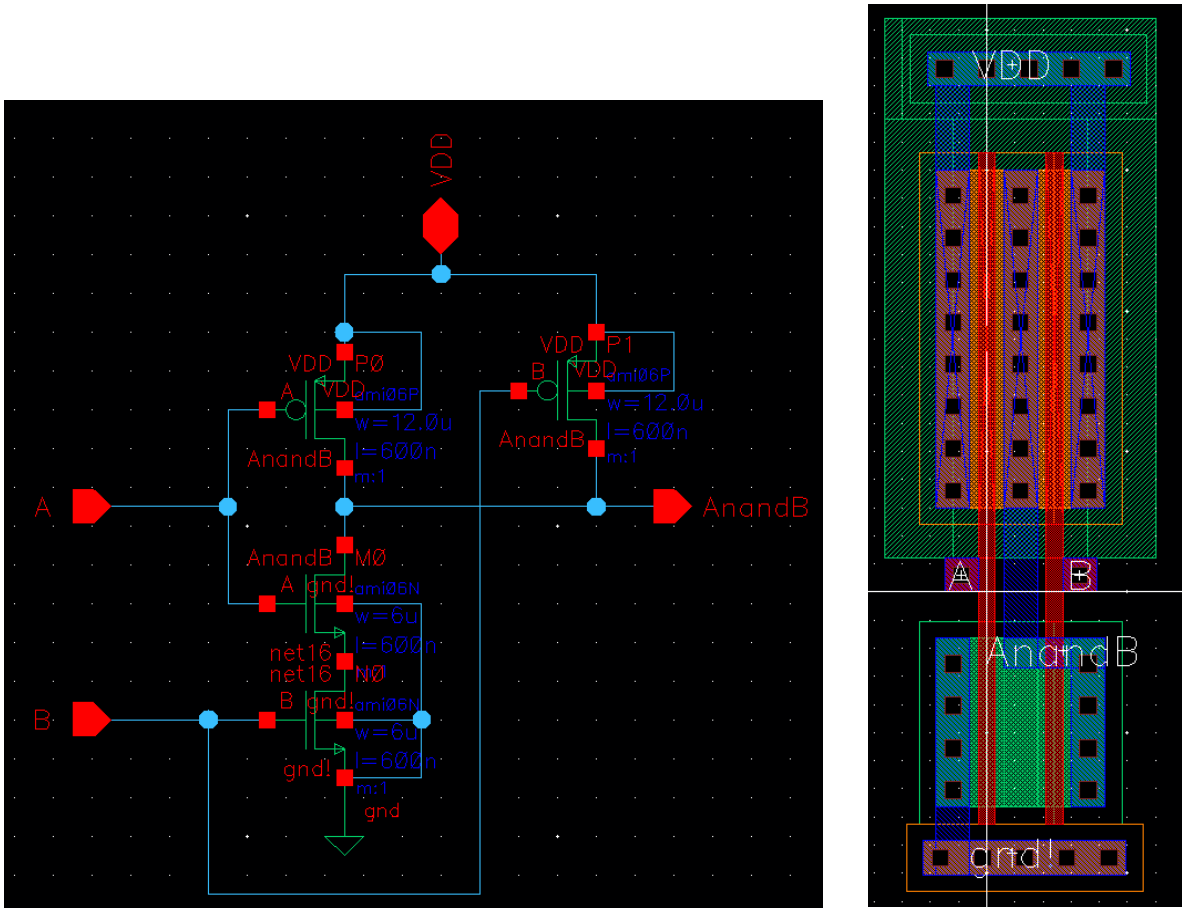


Figure 14: Ring Oscillator Layout

NAND Gate Design:

The NAND gate was designed with 10/1 NMOS and 20/1 PMOS. Figures 13 and 14 show the schematic and layout of this gate, respectively. Using this simplistic design approach both allowed for expected results and did not consume a considerable amount of power. Furthermore, Figure 15 shows the simulation warrants the correct output.



Figures 13 and 14: NAND Gate Schematic and Layout

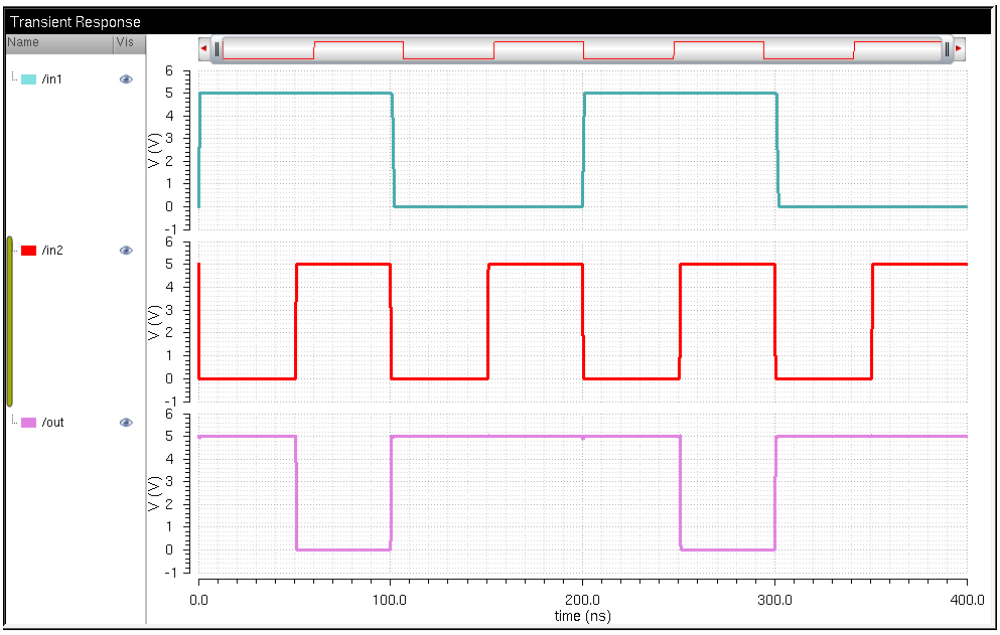


Figure 15: NAND Gate Simulation

Operation of NAND Gate and Ring Oscillator:

The NAND gate and ring oscillator work in conjunction with the buffer on the chip to operate the SPS. Table 4 displays the truth table for the NAND gate. This operation is integral to how the design works. To be more specific, when the Enable input is low, the output of the NAND gate is always high. This means that it does not depend on the B input, therefore it does not depend on the ring oscillator. When the Enable input is high, the output of the NAND gate is the inverted B input, meaning it is dependent on the oscillator.

Input One (Enable)	Input Two (Ring Oscillator)	Output
0	0	1
0	1	1
1	0	1
1	1	0

Table 4: NAND Gate Truth Table

The Buffer:

The Buffer Design:

The buffer in this design had the main requirement of being able to drive the NMOS seen in Figure 1. Since this is such a large device (with an equivalent capacitance of around 5pF), a three-stage inverter will be used (with the last stage having 8 devices in parallel). The first inverter consists of a 10/1 PMOS and 20/1 NMOS. To find the input capacitance of this first inverter, the following calculation can be made:

$$Cin_1 = Cox_n + Cox_p$$

$$Cin_1 = \frac{3}{2} * \frac{2.5\,f}{\mu^2} F * 0.6\mu * 6\mu + \frac{3}{2} * \frac{2.5\,f}{\mu^2} F * 0.6\mu * 12\mu$$

$$Cin_1 = \left(\frac{3}{2}\right) * 9\ fF + \left(\frac{3}{2}\right) * 27\ fF$$

$$Cin_1 = 40.5\ fF$$

With that being calculated, the input capacitance of the next inverters can be found using similar steps. Choosing an A of four and a final stage multiplier of eight, the following calculations can be made:

$$Cin_2 = Cin1 * A,\ \ Cin_3 = Cin_2 * A * M$$

$$Cin_2 = (40.5\ fF) * 4\ ,\ \ Cin_3 = (40.5\ fF) * 4^2 * 8$$

$$Cin_2 = 162\ fF\ ,\ \ \ Cin_3 = 5.2\ pF$$

This was enough to drive the MOSFET switch. Therefore, the buffer will use three stages: 12u/6u, 48u/24u, and 48u/24u with a multiplicity of eight. Obviously, the multiplicity of eight inverters in parallel will draw a significant amount of power in comparison to other devices on the chip, but the ability to drive the large MOSFET in the external circuitry of Flyback SPS was integral. The very large inverters allowed for this. Therefore, the tradeoff between device amount/size vs. power consumption and layout area was made. The schematic and layout for this buffer is shown in Figure 16 and 17, respectively.

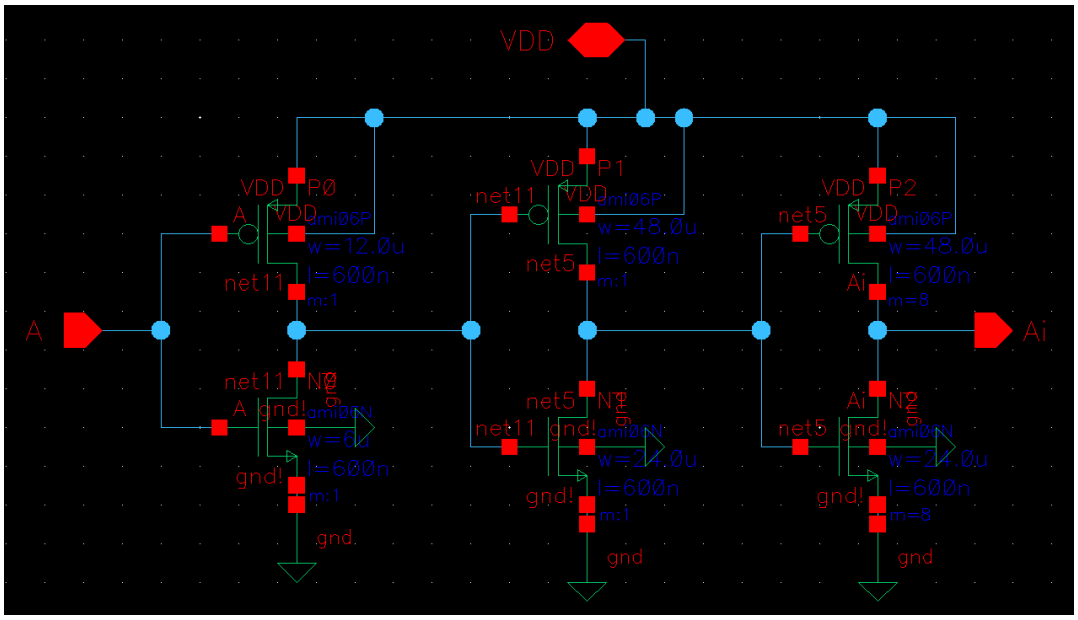


Figure 16: Schematic of Three Stage Buffer

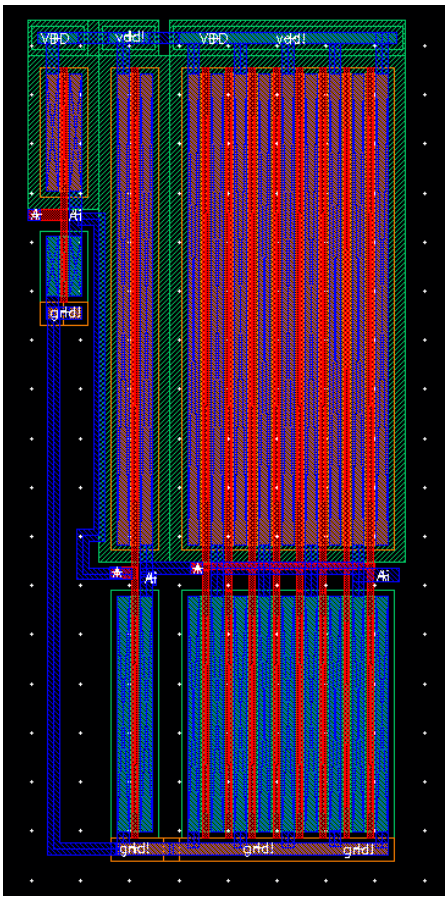


Figure 17: Layout of Three Stage Buffer

Final Layout:

Layout Specifications:

The layout of this chip, shown in Figure 18, took up a layout area of 176 um x 426 um. It passed both the Design Rule Check (DRC) and Layout Versus Schematic (LVS) verifications. Furthermore, the LVS verification also passed when comparing the MOSFET parameters.

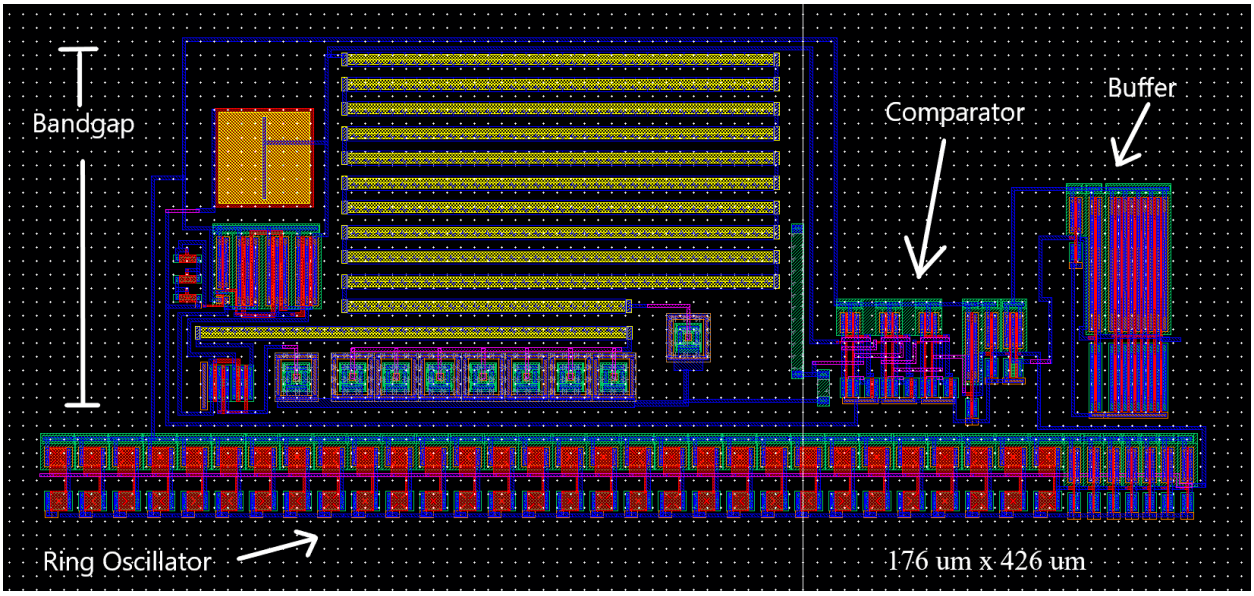


Figure 18: Full Layout Measuring 176 um x 426 um

Operation of the SPS Chip:

Vout and Out:

The output voltage from the external circuitry that is inputted to the chip is called Vout, and the output of the chip is called Out. Figure 19 displays these signals under a 2.5 A load and five volt VDD. The results are to be expected – Vout spends some time shooting up (in which the ring oscillator is on constantly), and then ripples around 12.5 V (while the Out oscillation turns on and off). Figure 20 shows this same simulation with temperature effects, and Table 5 shows the calculated results of the hysteresis change with temperature over this 2.5 A load as well as a 100 mA load.

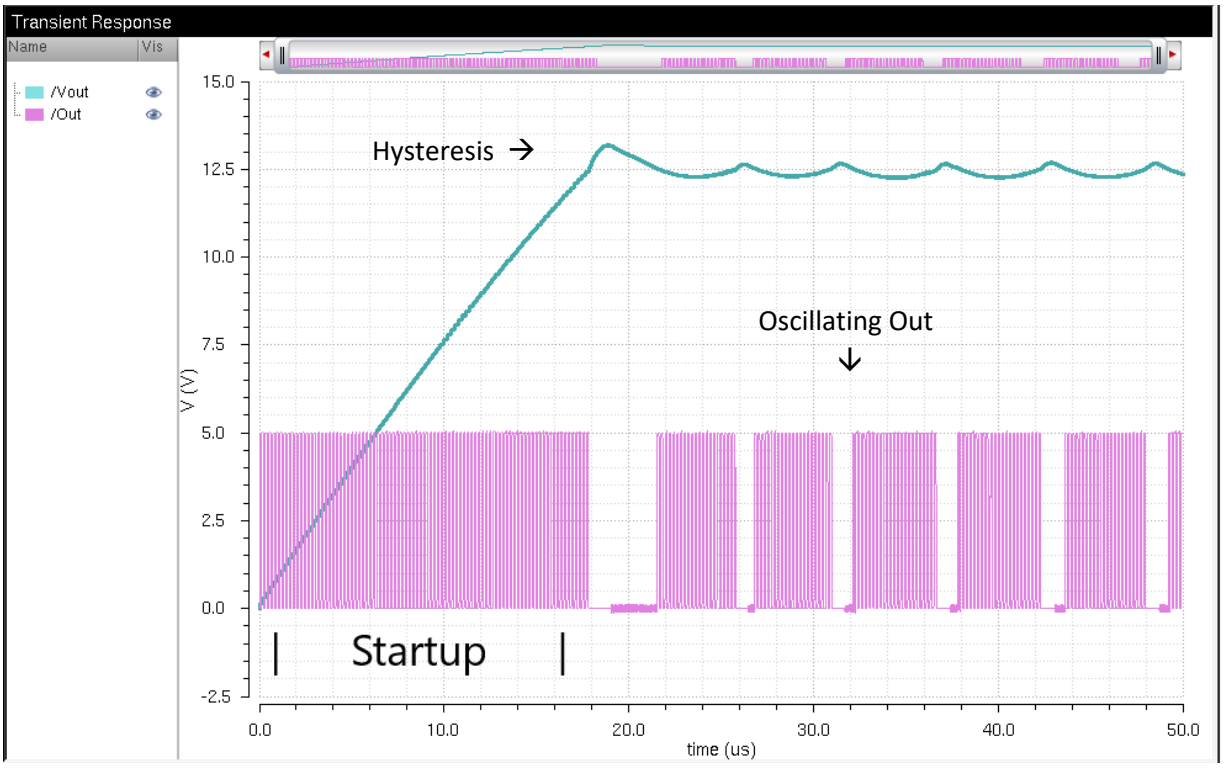


Figure 19: Simulation of Vout and Oscillating Output

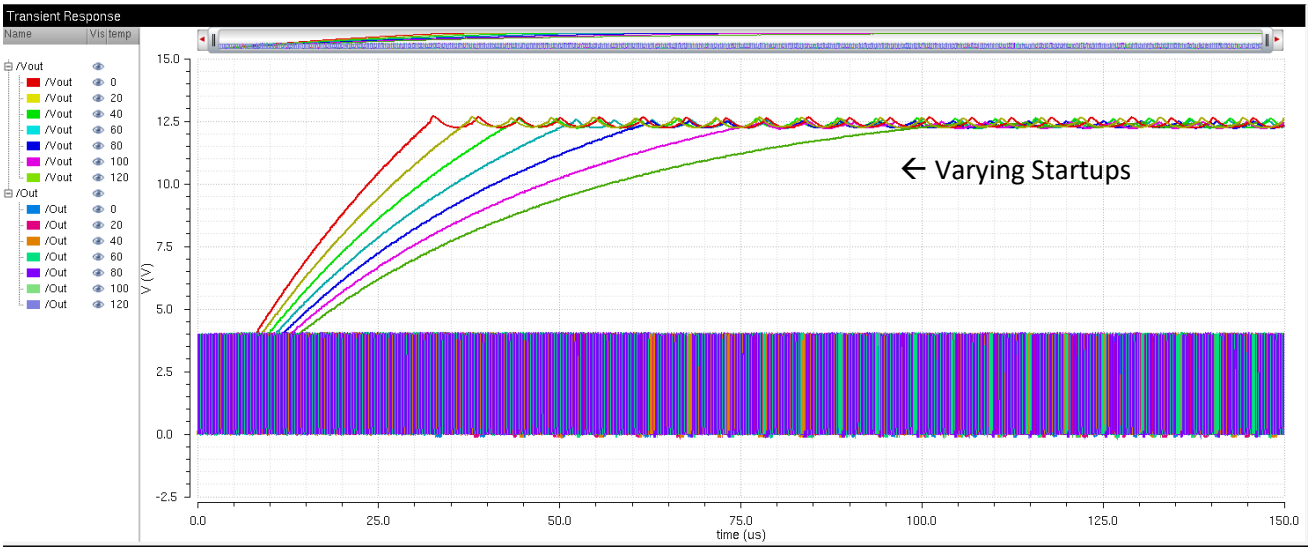


Figure 20: Temperature Changing Simulation of Vout and Oscillating Output

Temperature	Hysteresis Peak to Peak Load = 2.5 A, (VDD = 5 V)	Hysteresis Peak to Peak Load = 100 mA (VDD = 5 V)
0	434.1 mV	15.08 mV
30	430 mV	20.93 mV
60	356.1 mV	29.3 mV
90	300.6 mV	37.46 mV
120	242.1 mV	47.61 mV

Table 5: Temperature Effects on Hysteresis Peak to Peak Voltage (Load = 2.5 A, VDD = 5)

Current/Power Supplied to the Power Supply:

The current supplied to the power supply is an integral calculation to make. It decides the power consumption and efficiency of the project. Figure 21 shows the simulation of the current supplied to a 2.5 A load under a VDD of 5 V. This simulation was clipped after the startup of the circuit, (when in steady state), and averaged. For this load, the average current was 190.3 mA. To calculate the average power and efficiency, the following calculations can be made:

$$P_{AVG} = I_{AVG} * VDD$$

$$P_{AVG} = 190.3\,mA * 5$$

$$P_{AVG} = 951.5\,mW$$

$$Efficiency\ (\%) = \frac{(Vout * I_{LOAD})}{VDD * AVG(I(VDD)}$$

$$Efficiency\ (\%) = \frac{12.5\,V * 2.5\,A}{170\,V * 190.3\,mA}$$

$$Efficiency\ (\%) = 96.60\ \%$$

These calculations were repeated for several different scenarios. Tables 6 and 7 show the current and the power supplied by the power supply under varying loads for a VDD of 5V and for a VDD of 4V, respectively. It is obvious that the greater the current load, the greater the power (this is to be expected).

Tables 8 and 9 show the calculated current/power into and out of the chip under different VDDs. This current/power seems to decrease as the load current increases.

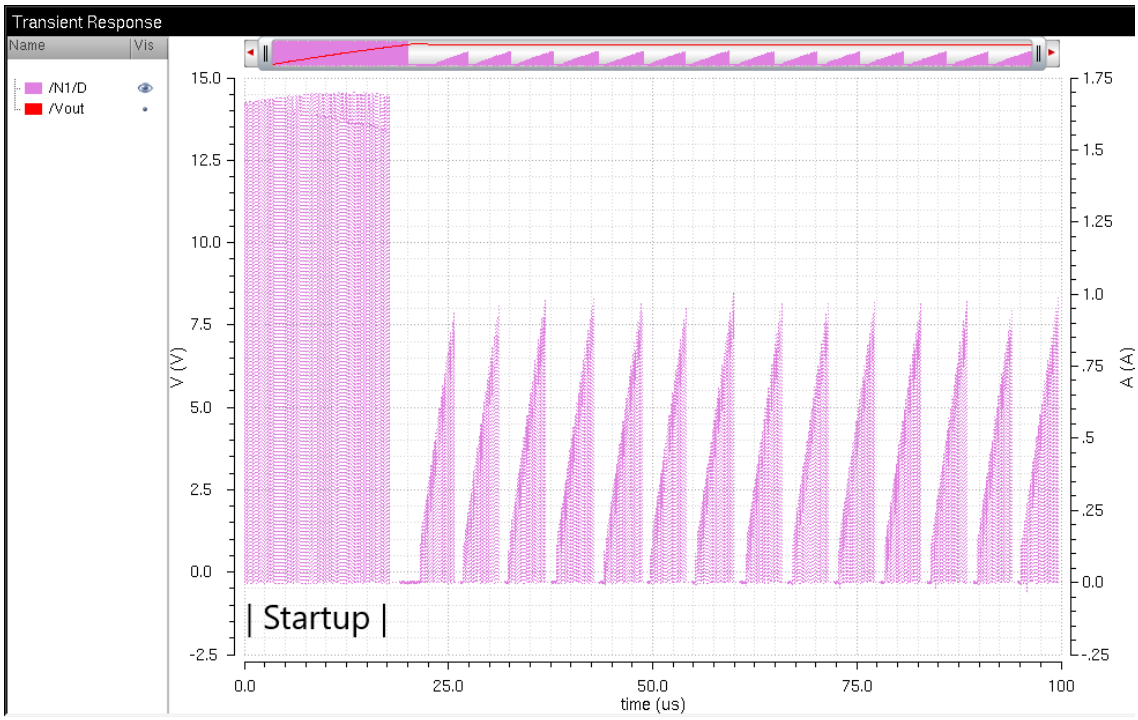


Figure 21: Simulation of Current Supplied to the Power Supply with 5 Ω Load, VDD = 5V

VDD = 5 V				
Load Current	**R_{Load}**	**Average Current Supplied by Power Supply**	**Average Power Dissipated by Power Supply**	**Efficiency of Power Supply**
0 mA	∞, (tested at 10k)	1.8967 nA	9.48 nW	< 40 %
10 mA	1.25 k Ω	854.0 uA	4.27 mW	86.10 %
100 mA	125 Ω	7.818 mA	39.09 mW	94.05 %
500 mA	25 Ω	39.19 mA	196.0 mW	93.80 %
1 A	12.5 Ω	78.35 mA	396.75 mW	93.85 %
2.5 A	5 Ω	190.3 mA	951.5 mW	96.60 %
5 A	2.5 Ω	396.6 mA	1.98 W	92.70 %

Table 6: Power Supplied by Power Supply and Efficiency Under Varying Loads (VDD = 5V)

VDD = 4 V				
Load Current	**R_{Load}**	**Average Current Supplied by Power Supply**	**Average Power Dissipated by Power Supply**	**Efficiency of Power Supply**
0 mA	∞, (tested at 10k)	< 836.3 uA	< 3.34 mW	< 40 %
10 mA	1.25 k Ω	865.1 uA	3.46 mW	85.0 %
100 mA	125 Ω	7.725 mA	30.9 mW	95.18 %
500 mA	25 Ω	38.74 mA	15.5 mW	94.9 %
1 A	12.5 Ω	77.8 mA	31.12 mW	94.51 %
2.5 A	5 Ω	199.8 mA	79.92 mW	92.00 %
5 A	2.5 Ω	447.5 mA	1.79 W	82.1 %

Table 7: Power Supplied by Power Supply and Efficiency Under Varying Loads (VDD = 5V)

VDD = 5 V					
Load Current	**R_{Load}**	**Average Current into SPS Chip**	**Average Power Consumed by SPS Chip**	**Average Current Exiting SPS Chip**	**Average Power Dissipated by SPS Chip**
10 mA	1.25 k Ω	3.074 mA	15.37 mW	295.1 nA	1.4755 uW
100 mA	125 Ω	3.353 mA	16.765 mW	1.511 uA	7.555 uW
500 mA	25 Ω	3.461 mA	17.305 mW	457.6 nA	2.288 uW
1 A	12.5 Ω	2.777 mA	13.885 mW	167.6 nA	838 nW
2.5 A	5 Ω	2.079 mA	10.395 mW	164.4 nA	822 nW
5 A	2.5 Ω	2.008 mA	10.04 mW	2.888 uA	14.44 uW

Table 8: Power Consumed and Dissipated by SPS Chip Under Varying Loads (VDD = 5V)

VDD = 4 V					
Load Current	**R_{Load}**	**Average Current into SPS Chip**	**Average Power Consumed by SPS Chip**	**Average Current Exiting SPS Chip**	**Average Power Dissipated by SPS Chip**
10 mA	1.25 k Ω	1.545 mA	6.044 mW	230.7 nA	922.8 nW
100 mA	125 Ω	1.511 mA	6.544 mW	1.535 uA	6.14 uW
500 mA	25 Ω	1.636 mA	7.5 mW	2.864 uA	11.456 uW
1 A	12.5 Ω	1.875 mA	6.3 mW	4.959 uA	19.836 uW
2.5 A	5 Ω	1.575 mA	5.76 mW	4.282 uA	17.128 uW
5 A	2.5 Ω	1.44 mA	4.604 mW	42.87 nA	171.45 nW

Table 9: Power Consumed and Dissipated by SPS Chip Under Varying Loads (VDD = 4V)

Temperature Effects on Current/Power Supplied to the Power Supply:

The 27˚ simulation showed a 951.5 mW power supplied to the power supply. Figure 22 and Table 10 below show that along a 120˚ change in temperature, a 256.5 mW variation in power was found under a load of 2.5 A and VDD of 5 V. The simulation was clipped at 50us to ensure that the startup currents were not included in averages.

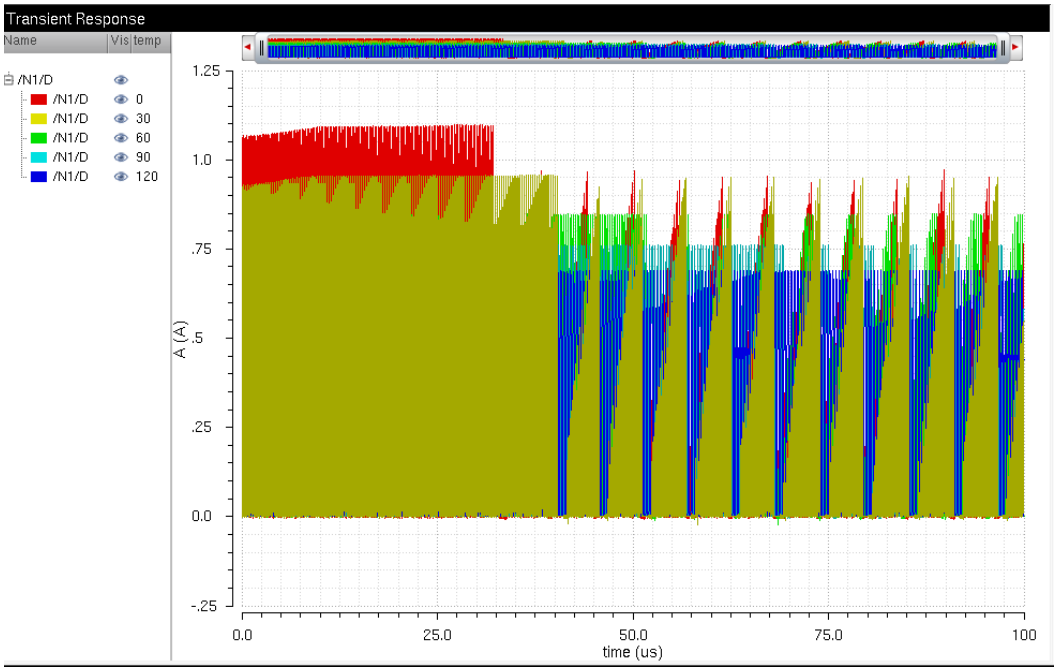


Figure 22: Simulation of Varying Temperature - Load = 2.5 A, VDD = 5

Temperature	Average Current Supplied by Power Supply	Average Power Supplied by Power Supply
0	195.4 mA	977 mW
30	197.6 mA	988 mW
60	207.6 mA	1.04 W
90	221.5 mA	1.108 W
120	239.7 mA	1.198 W

Table 10: Corresponding Average Current/Power for Figure 22 – Varying Temperature

Summary / Design Tradeoffs

The design of this Flyback SPS circuit works within the design requirements and beyond. It can operate using 10 mA through 5mA loads with over 85% efficiency, and work under and over those load currents at the cost of efficiency. The following table discusses tradeoffs that were considered while designing the chip.

Element	Tradeoffs associated
External Circuitry	A 10 µF filtering capacitor was chosen it kept the output at an acceptable level (for most loads) while keeping cost relatively low. This came at with the tradeoff of hysteresis. Vout ripples, depending on the load, up to 400 mV. **This means that the tradeoff of efficiency for cost was made.**
Bandgap	A considerable amount of layout area comes from the bandgap reference circuit. **A smaller reference voltage circuit would reduce layout size but would come at the cost of efficiency and accuracy.** The bandgap has a very high efficiency for a vast amount of conditions, making it a good choice for this sensitive SPS.
Comparator	The comparator utilizes three difference amplifiers and two inverters. A design with less transistors may consume power, but that may come at the cost of less accuracy. Additionally, the sizes of the transistors

	can be lessened in order to save power. This is seen with the tail transistors on the diff-amps, as their lengths are double the minimum value. **The decision of the transistor amount and sizing came with associated tradeoffs between power, speed, and layout size**
Ring Oscillator / NAND Gate	The ring oscillator used 37 total stages to create an oscillation frequency close to 5 MHz. This is obviously a lot of stages; however, it came with a very accurate frequency. **Therefore, the tradeoff between accuracy and power/layout size was made.**
Buffer	The design used a three-stage buffer with a final stage multiplicity of 8. The final stage was obviously very large, but this was integral to the design so it could drive the large NMOS on the external circuitry. The large buffer consumed a considerable amount of power and added to the layout size but was necessary for proper operation. **The decision to optimize efficiency in exchange for layout size and power consumption was made.**

Future Work/Improvements and Conclusion:

The design of this Flyback SPS chip performs beyond its design requirements. However, there is always room for improvement. The following list details the future work that can be done to further optimize its performance.

Decrease Power Consumption:

Power consumption was a factor that I tried to keep to a minimum while designing. Still, the chip uses a decent amount of power. To optimize the design, a smaller comparator, buffer, and/or ring oscillator can be used. A decrease in the number of transistors would obviously consume less power. Additionally, each MOSFET used could have an increased length/width, so as to also consume less power. Increasing these transistor parameters would limit the amount of current that can pass through it. Limiting the current through the transistors would cause the power consumption to go down because power is directly related to current. As the current passing through decreases, the power consumed will also decrease (if VDD is constant). This would

come at the cost of speed and layout area, so the tradeoff between these three things must be assessed for different applications. Additionally, a smaller biasing circuit with similar efficiency would greatly improve the power consumption. The bandgap reference circuit consumes a considerable amount of power, so using a smaller circuit here could improve the design. However, this circuit is incredibly stable at various temperatures and conditions. Therefore, another tradeoff for this chip would be using a smaller voltage reference circuit at the cost of efficiency and accuracy.

Decrease Layout Area:

This chip takes up a layout area of 176 um x 426 um. A very considerable amount of this layout area comes from the bandgap reference circuit. As mentioned in the previous paragraph, to improve this design, consideration of the use of a smaller voltage reference circuit may be a good idea. The bandgap has a very high efficiency for a vast amount of conditions, so changing it may be an option only when the accuracy/efficiency can be sacrificed by some amount (maybe in a project that is emphasizing low power and small layout size rather than a perfectly performing device). In addition to this possible improvement, the ring oscillator could also be enhanced. This design uses a 37-stage ring oscillator, including both the small and slow inverters. This is a very considerable amount of layout area and is the piece of the project that takes up the most amount of space after the bandgap. A smaller ring oscillator may want to be looked into to decrease layout area, however, may come at the cost of accuracy. This ring oscillator has an oscillating frequency of 5.045 MHz, which is very close to the ideal 5 MHz that the design required. However, if the oscillating frequency could be increased, the number of inverters used in this design could be significantly decreased. This would come at the cost of efficiency of the design but may be a good enhancement in faster designs.

Conclusion / Final Remarks:

This chip works exactly how it is intended to. The figures and tables provided throughout this report characterize the design based on the guidelines outlined on the first page. The chip responds well to changes in VDD, and relatively well to changes in VDD. It works optimally with a current load between 100 mA and 2.5 A, but will continue to function to bigger/smaller loads. Additionally, simulations make it apparent that the circuit does not respond significantly for ± 30˚ changes in temperature. Changes are evident beyond that margin, but the circuit

continues to work (less efficiently). Overall, the design works well and meets the design requirements.