Jazmine Boloor
EE 420: Engineering Electronics II – Analog IC Design
Dr. R. Jacob Baker
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The following Op-Amp was designed to meet the following design specifications using On Semiconductor's 500nm process:

- Can operate with a VDD down to 3V while driving 1000pF (max) and 100 (min) load
- DC open-loop gain > 60 dB under all load and VDD conditions
- Gain-bandwidth product should be > 5 MHz
- Slew-rate with maximum load > 1V/microsecond
- Quiescent current draw should be less than 2 mA with no load

The following summary tables encapsulate the main results of the design.

Overview of General MOSFET Parameters in this Design			
Parameter	**NMOS**	**PMOS**	**Comments**
Bias Current I_D	8µA	8µA	Approximate
W/L	100/1 (60µ/0.6µ)	200/1 (120µ/0.6µ)	
V_{DSsat} / V_{SDsat}	75mV	75mV	Using 2.5% of VDD
V_{GS} / V_{SG}	745mV	995mV	
V_{THn} / V_{THp}	670mV	920mV	From .txt file for C5 process
KP_n / KP_p	28.4µA/V^2	14.2µA/V^2	
$t_{ox} = \varepsilon_{ox}/t_{ox}$	139Å	139Å	From .txt file for C5 process
C'_{ox}	2.49nF/µm^2	2.49nF/µm^2	
C_{oxn} / C_{oxp}	89.64nF	179.28nF	
C_{gsn} / C_{sgp}	11.9fF	34.6fF	From LTspice Error Log
C_{gdn} / C_{dgp}	11.9fF	34.6fF	From LTspice Error Log
G_{mn} / G_{mp}	221µA/V	212µA/V	From LTspice Error Log
R_{on} / R_{op}	1.1 Meg	950k	Approximate
λ_n / λ_p	0.113H	0.131	Approximate

Open Loop Gain		
Load	**VDD = 3V**	**VDD = 5V**
No load	83.7dB	77.9dB
Purely Capacitive Load	83.7dB	77.9dB
Purely Resistive Load	67.2dB	61.9dB
Full Load	67.2dB	61.9dB

Bandwidth Product		
Load	**VDD = 3V**	**VDD = 5V**
No load	9.9MHz	9.6MHz
Purely Resistive Load	7.9MHz	7.8MHz
Purely Capacitive Load	7.0MHz	7.4MHz
Full Load	5.9MHz	5.8MHz

Slew Rate		
Load	**VDD = 3V**	**VDD = 5V**
No load	6.5V/µs	6.5V/µs
Full Load	4.37V/µs	6.08V/µs

Quiescent Current Draw	
VDD	**Current Draw**
3V	0.168mA
4V	0.209mA
5V	0.265mA

Power Consumption/Dissipation		
VDD	**Quiescent Power Consumption**	**Power Dissipation (No Load)**
3V	0.50mW	398µW
4V	0.84mW	608µW
5V	1.33mW	877µW

Input Common Mode Range	
V_{cmMax}	VDD + 595mV
V_{cmMin}	1.1 V

Power Supply Rejection Ratio (No Load) at 1kHz		
VDD	**PSRR+**	**PSRR-**
3V	78.25dB	103.9dB
4V	76.24dB	103dB
5V	73.88dB	101.8dB

Common Mode Rejection Ratio at 100k	
VDD	**CMRR**
3V	76.29dB
4V	73.20dB
5V	70.27dB

Selecting Device Parameters:

V_{TH}, V_{DSsat} / V_{SDsat} and V_{GS}/V_{SG}

The values for the threshold voltages of the NMOS and PMOS devices, V_{THn} and V_{THp}, can be found within the LTspice model file. They are defined as V_{THn} = 670mV and V_{THp} = 920mV. These values can also be illustrated through simulation, as shown below in Figure 1. V_{DSsat} and V_{SDsat}, or the overdrive voltages, were selected to be 2.5% of the minimum VDD (2.5% of 3V is 75mV). General design usually calls for an overdrive voltage of 5% of VDD, but considering VDD is going down to 3V, a smaller percentage was opted for in order to maximize the abilities of the gain. Once these values are known, V_{GS} and V_{SG} can be calculated by adding the threshold voltage and the overdrive voltage.

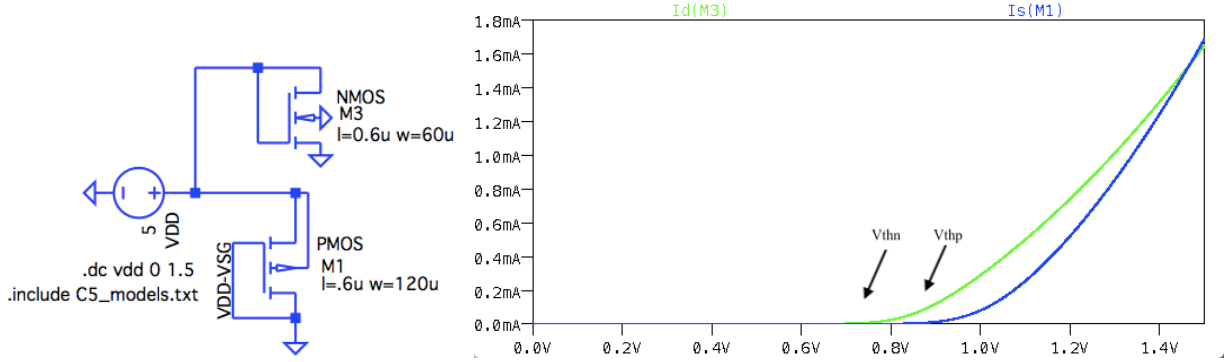

Figure 1: showing V_{THn} and V_{THp} through simulation

Selecting MOSFET W/L

Though general design parameters usually call for using 2-5 times the minimum length for a device, the minimum length for both the NMOS and the PMOS devices was used to maximize open loop gain. Using this length and aiming for a drain current of 8µA, the NMOS and PMOS devices were sized 100/1 and 200/1, respectively. The schematics that follow will use lengths and widths titled NL, NW, PL, and PW – these values correspond to 60u, 0.6u, 120u, and 0.6u, respectively.

The Biasing Circuit

Beta Multiplier Reference

The first step in creating the biasing circuit was creating initial reference voltages. This was done through the implementation of the beta multiplier reference circuit shown in Figure 2. The figure also shows the start-up circuit that was used to quickly start the flow of current in the circuit. To better ensure stability through changes in VDD, a decoupling MOSFET capacitor was added to the PMOS bias voltage, Vbiasp. The body of each PMOS device was tied to its source in attempt to minimize the body effect. This reference voltage would be used to bias the rest of our reference voltages, so its stability is fundamental to the design.

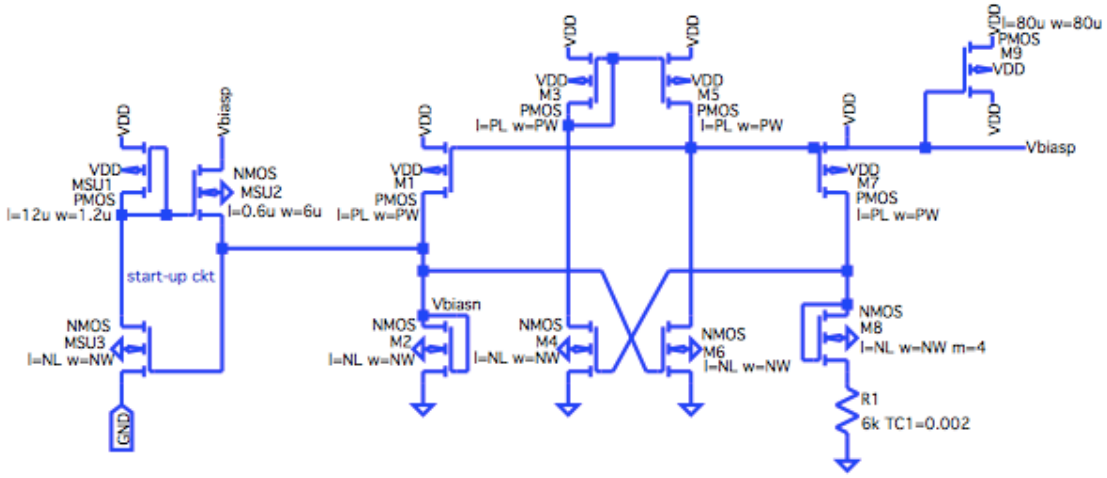

Figure 2: Beta Multiplier Reference Circuit

Creating Bias Voltages

The biasing circuit shown in Figure 3 was chosen to eliminate variance in the reference voltages as VDD changes. It does this by optimizing the stable nature of wide swing cascode current mirrors. Keeping all of these bias voltages stable is integral for the design, as these voltages are used to bias the op-amp. Figure 4 shows that the bias voltages are indeed reasonably stable both throughout VDD (3V-5V), and throughout its surrounding voltages.

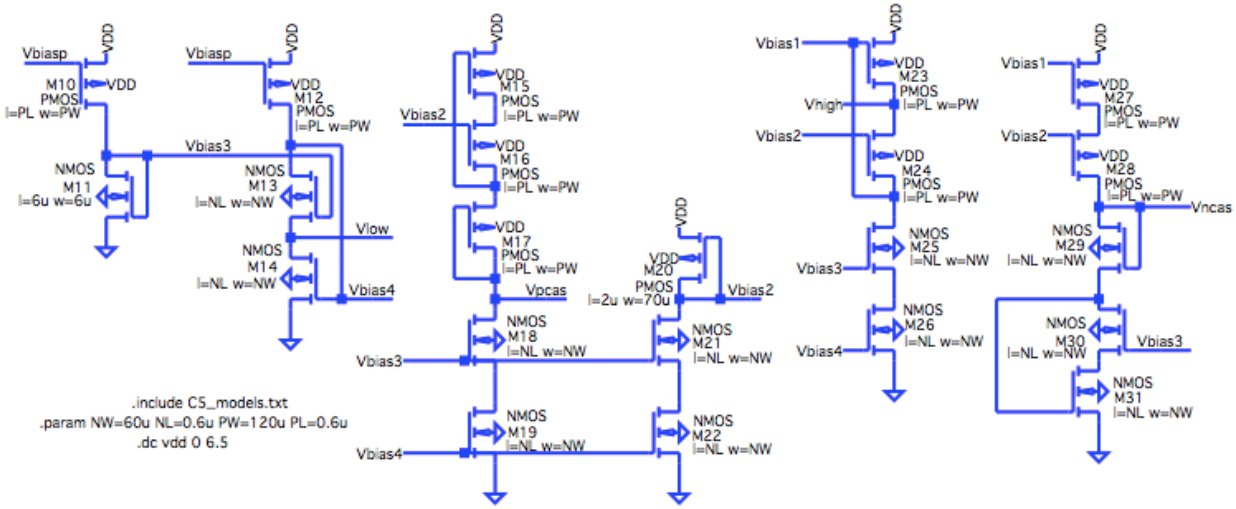

Figure 3: Biasing Circuit

It should be noted that the current throughout the system stays relatively constant at around 8µA. The following reference voltages are given by the biasing circuit:

Vbias1 = 0.893V	Vlow = 0.301V
Vbais2 = 1.03V	Vhigh = 0.123V
Vbias3 = 1.13V	Vncas = 1.38V
Vbais4 = 0.630V	Vpcas = 1.95V

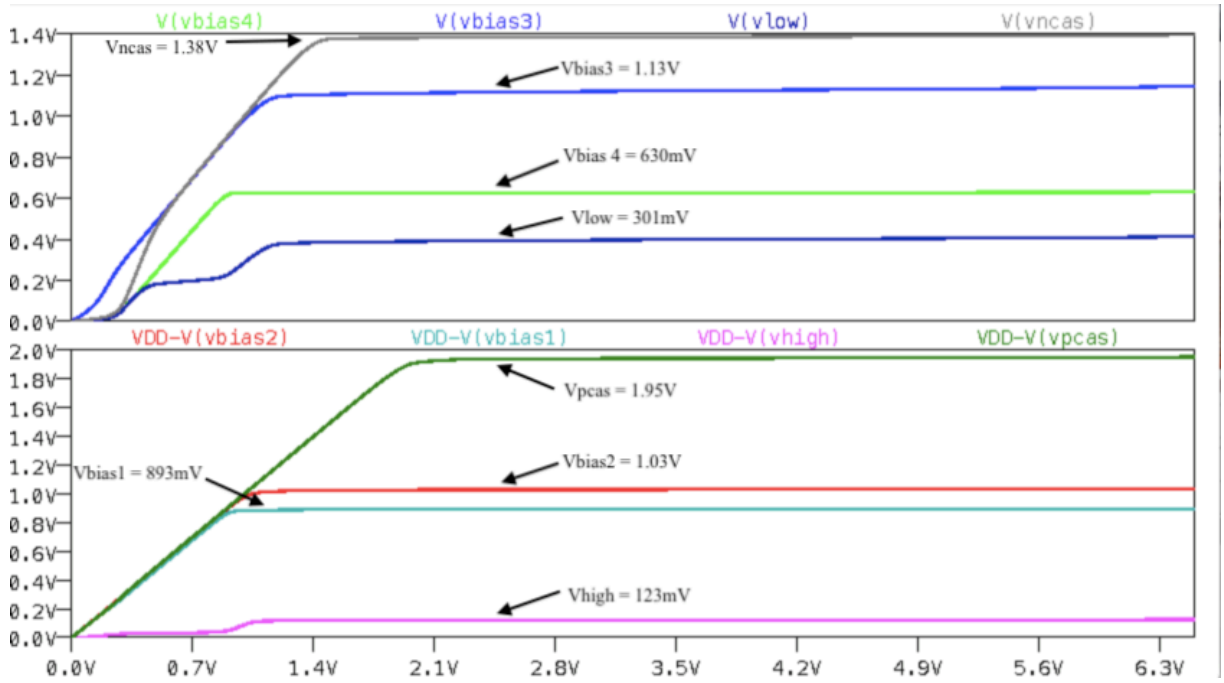

Figure 4 – Bias Voltages and their stability (showing stability for VDD around 2V to 6.5V+)

The Op-Amp Design

The Output Swing

An important aspect of any design is its output swing, or the range of values that the output of the system can span from while all the devices are working properly. The output swing of this op-amp ranges from:

$$V_{outMax} = VDD - V_{SDsat}$$

$$V_{outMin} = V_{DSsat}$$

\Plugging in values for V_{SDsat} and VD_{Ssat}:

Output Swing Values	
V_{outMax}	VDD - 75mV
V_{outMin}	75mV

The Overall Structure

The design shown in Figure 5 below shows a wide swing folded cascode op-amp with an NMOS and PMOS differential amplifier input stage. This op-amp topology is especially useful in creating a high unity-gain frequency and higher output resistance. As shown in the summary tables, the W/L of most of the MOSFETs used throughout the design are 100/1 and 200/1 for NMOS and PMOS. The use of minimum length devices constricts the amount of current that can source and sink, but using this small of a length greatly decreased the power consumption of the Op-Amp. Additionally, it allowed for a higher gain, which was one of the main design specifications. The width was determined based on the slew rate restriction, as making the width longer would create a longer slew rate.

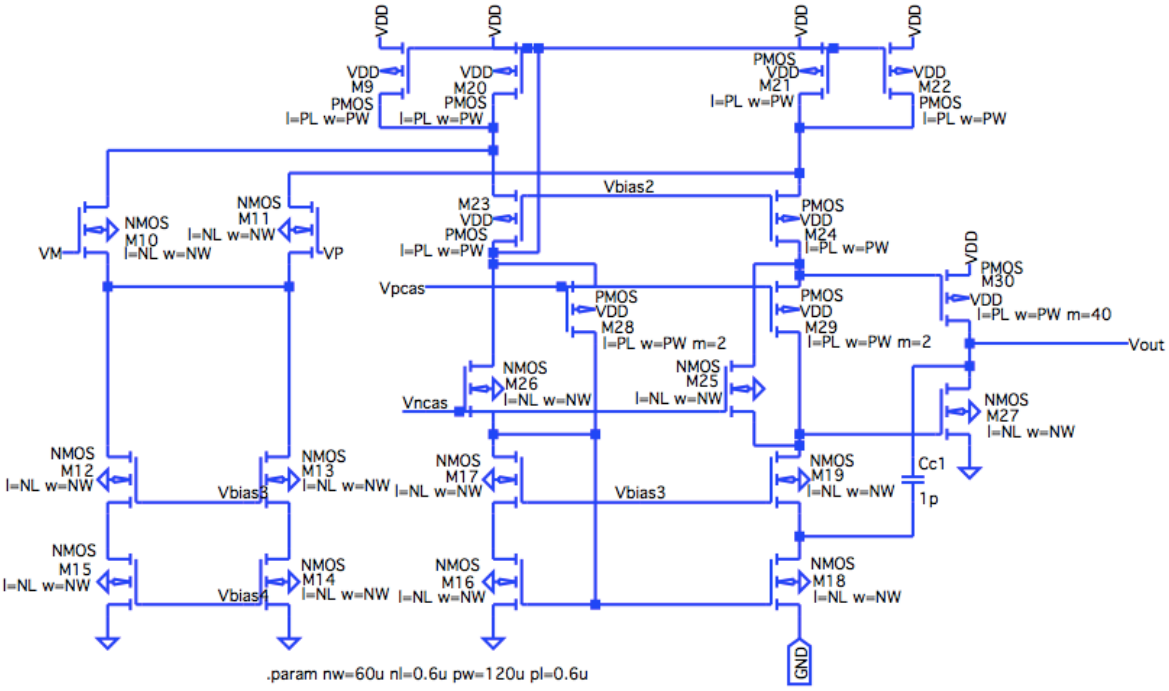

Figure 5 – Design of the Op-amp

The Common Mode Range

The Common Mode Range (CMR) is an important parameter to calculate in the op-amp because it describes the region the MOSFETs in the differential amplifier are operating in. These MOSFETs are reliant on the CMR– as the input voltage is approaching ground, the PMOS input stage will be activated; as the input voltage is approaching VDD, the NMOS input stage will be activated. The use of the folded cascode in the design allows for a larger common mode range, which allows for a larger region of proper MOSFET operation.

As with any range of values, there is a V_{cmMax} and V_{cmMin} value. When the input voltage of the differential amplifier lies outside of this range, the MOSFETs will either move into the

triode region or turn off, both of which are undesirable. To calculate these values for maximum and minimum common mode voltage, the following equations can be used:

Maximum:

$$VDS \geq VGS - VTHN, \quad solving\ for\ VG:$$
$$VG \leq VD + VTHN, \quad substituting\ VD:$$
$$VG \leq VDD - VDSSAT + VTHN, \quad equating\ VG\ to\ VcmMax:$$
$$VcmMax \leq VDD + 595mV$$

Using similar logic, the minimum voltage can be found using the equation

$$VcmMin \geq 2VSDSAT + VSG, \text{ or } VcmMin \geq 1.1V.$$

The Op-Amp Operation – Design Requirements

DC Open-Loop Gain and Gain-Bandwidth Product

The first requirements that the op-amp had to meet was having an open loop gain of over 60dB and a gain-bandwidth of over 5MHz under all load and VDD conditions. The following simulations show the design meeting these requirements. Note that only select simulations are shown, but several other tests using different loads/VDD values were performed and their results are shown in the summary tables on pages 1-2.

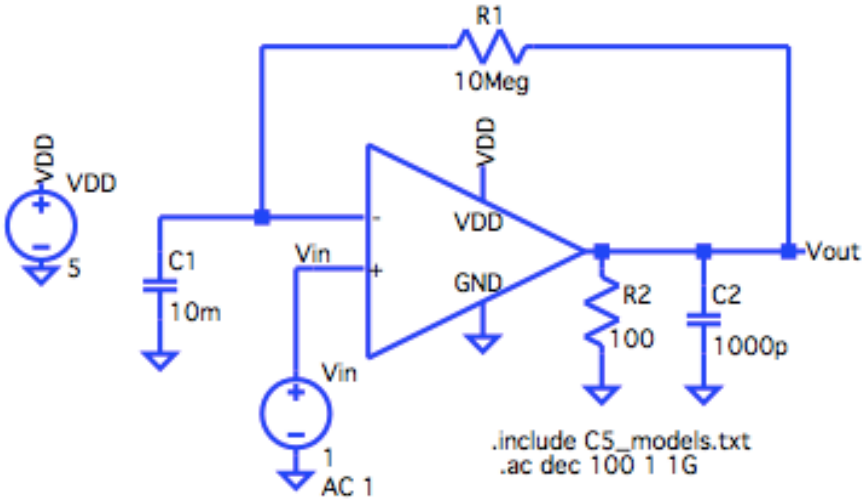

Figure 6a - Schematic used to calculate the open loop gain under various loads and VDD values

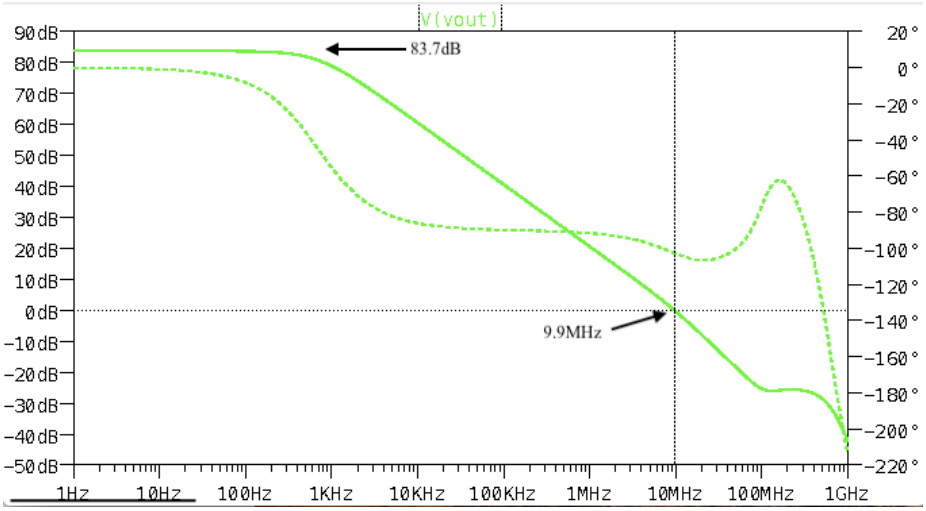

Figure 6b - Simulation for the open loop gain under a VDD of 3V with no load

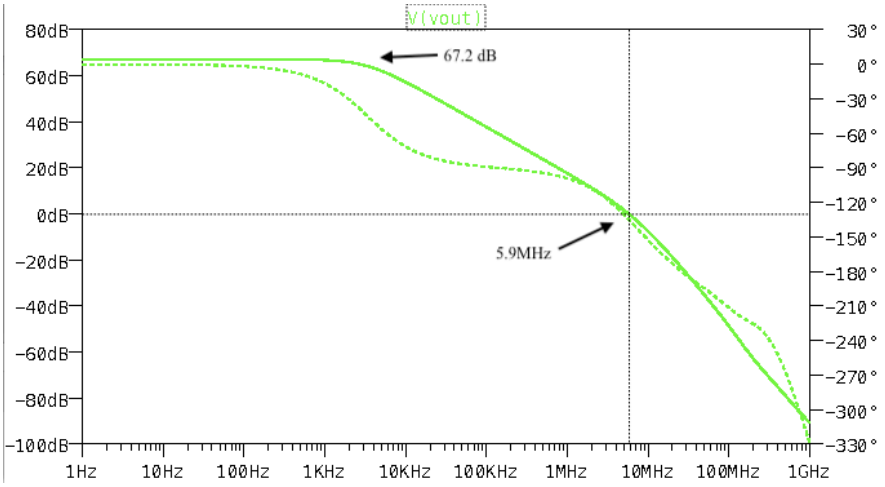

Figure 6c - Simulation for the open loop gain under a VDD of 3V with full load

Slew Rate

The required slew rate for the op-amp was 1V/microsecond with a full load. The slew rate is a measure of how fast the output can respond to the input. An ideal system would immediately respond to the input, but factors such as the MOSFET widths and power consumption in this system cause a delay in response. Since the MOSFETs used possess relatively wide widths, the slew rate is thereby also relatively high and reaches beyond the requirement by a considerable amount. The widths of devices are so integral to slew rate in this design because of the positioning of the PMOS devices being above the NMOS devices – a PMOS device with a large width can source a lot of current, and an NMOS device with a large width can sink a large amount of current. It is an intuitive system – larger width devices allow for the system to move current faster.

The slew rate can be calculated by seeing the change in voltage over the change in time, shown in the equation below. The points of the output used in the following calculation and simulation (Figure 7b) were those at around 10% and 90% of the output signal at full load and maximum VDD. Note that only the value of the slew rate at full load is shown in the calculation and simulation, but more conditions are shown in the summary tables.

$$Slew\ Rate = \frac{\Delta V}{\Delta t} = \frac{1.8V - 0.40V}{2.3\mu s - 2.07\mu s} = 6.08V/\mu s$$

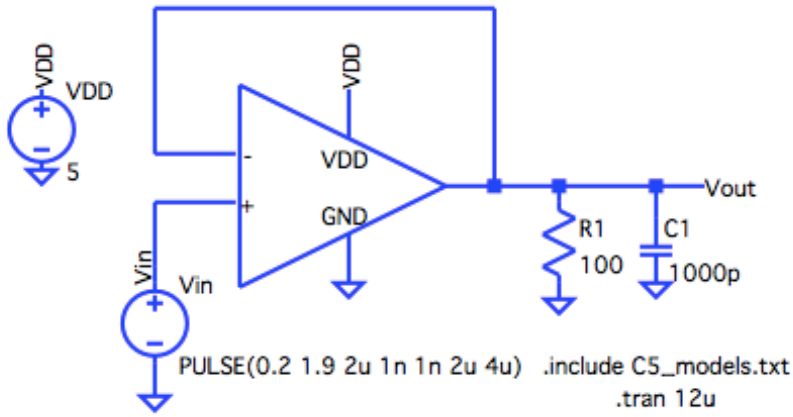

Figure 7a – Schematic used to calculate slew rate (full load and max VDD)

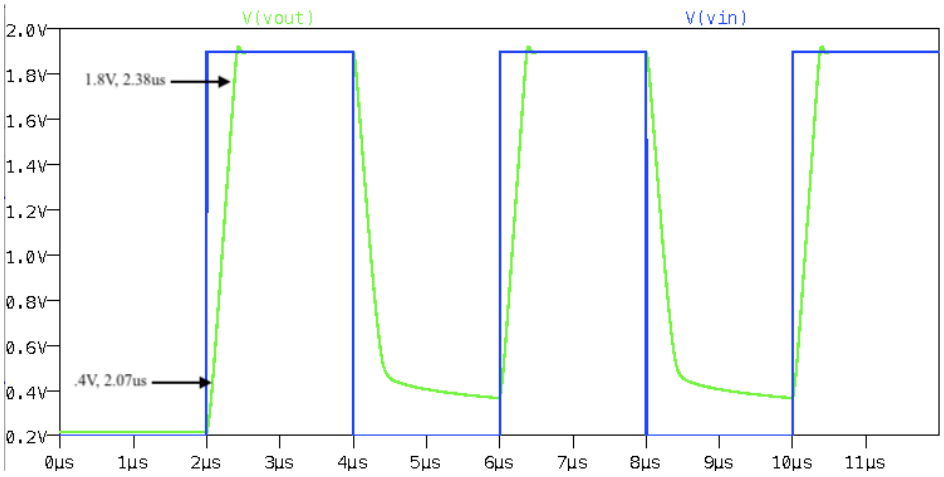

Figure 7b – Slew rate measured at 10% to 90% of output amplitude (full load and max VDD)

Quiescent Current Draw

The last formal requirement that the op-amp had to meet was having a quiescent current draw of less than 2mA. The quiescent current is the current that the op-amp draws when it is under no load conditions. Factors that can cause this current to rise include large device widths, a large bias current, and a large output stage. However, each of these factors has its own drawbacks – smaller device widths allow for less current sourcing/sinking, a smaller bias current would change the length/widths of the devices, and a smaller output stage would slow the slew rate.

The quiescent current was tested through the following LTspice simulation. It illustrates that the current is well below the minimum requirement of 2mA, showing .265mA at 5V.

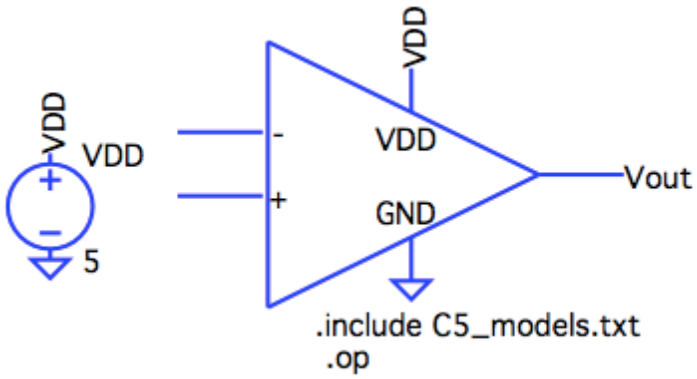

Figure 8a – Quiescent current draw at 5V (no load)

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Operating Bias Point Solution:
V(vdd)                     5   voltage
V(vout)              4.99175   voltage
V(n001)                    0   voltage
V(n002)                    0   voltage
I(Vdd)       -0.000265185   device_current
```

Figure 8b – Quiescent current draw at 5V (no load)

Note that when the device is operated at the lowest VDD, 3V, the quiescent current is 0.168mA. Therefore, the range of quiescent current for the required VDD values is 0.168mA to 0.265mA.

```
Operating Bias Point Solution:
V(vdd)                     3   voltage
V(vout)               2.9954   voltage
V(n001)                    0   voltage
V(n002)                    0   voltage
I(Vdd)       -0.000167787   device_current
```

Figure 8c – Quiescent current draw at 3V

The Op-Amp Operation – Other Results

Quiescent Power Consumption

Figure 9 shows the quiescent power consumption of the op-amp at different values for VDD. It shows that the design has a generally small amount of quiescent power consumption, which is to be expected after finding that the quiescent current is small; to calculate the power, VDD is multiplied by this current. Note that these values are shown both in the simulation below and in the summary tables on pages 1-2.

A sample calculation can be seen with the following equation for VDD = 3V:

$$P = IV$$
$$P = (0.167mA) * (3V)$$
$$P = 501mW$$

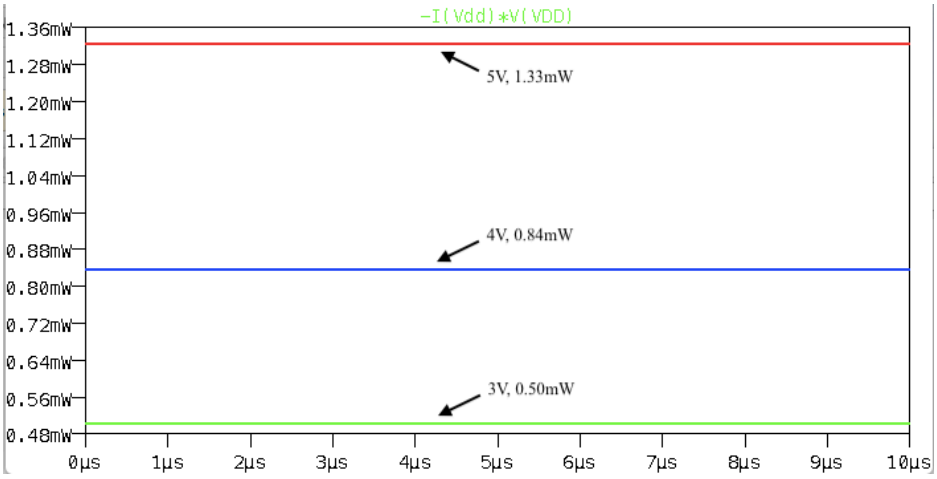

Figure 9 – Quiescent power for different VDD values

Power Dissipation Under No Load

The total power dissipated by the op-amp can be calculated by the same P = IV formula used above. This time, the value of the current will be equal to the value that is running through the entire circuit. There are six PMOS devices that source current into the circuit. Five of these devices are sourcing the bias current of 8µA, making a total of 40µAof current in these branches. The last branch is sourcing 8µAthrough 40 devices in parallel, creating 40 times the current. So, the current through the last branch is equal to 320µA, making the current through the entire system approximately 360µA. With this in mind, the power dissipated through a single branch can be estimated by multiplying 360µAwith a chosen VDD. Note that this calculation is an approximation, as the current throughout the system slightly varies from the values calculated.

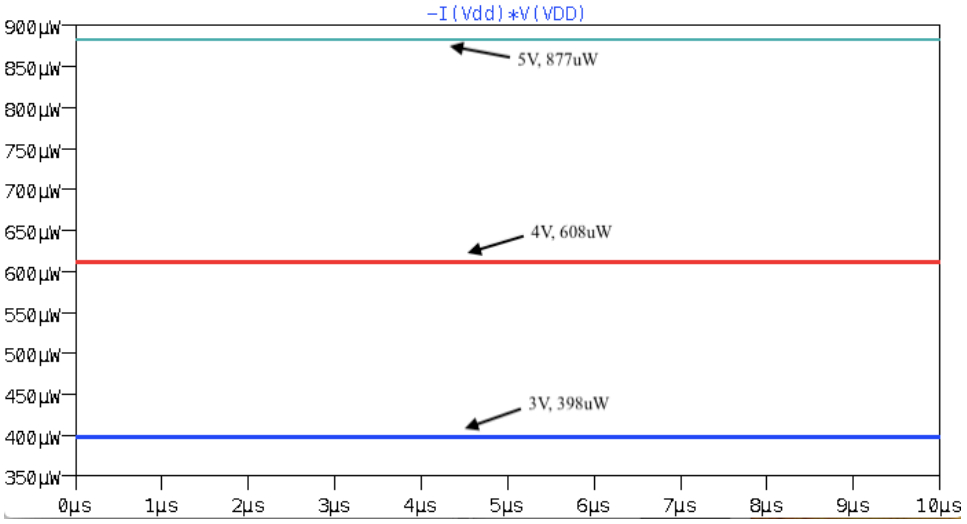

Figure 10 – Power dissipation for different VDD values

Power Supply Rejection Ratio (PSRR)

The Power Supply Rejection Ratio (PSRR) describes the amplifiers ability to reject noise at power supply or ground busses. In other words, op-amps should ideally have a high PSRR to reject unwanted signals from entering. The following simulations test the positive and negative PSRR. Note that only select values are simulated below, but all values for PMRR+ and PMRR- can be found in the summary tables on pages 1-2.

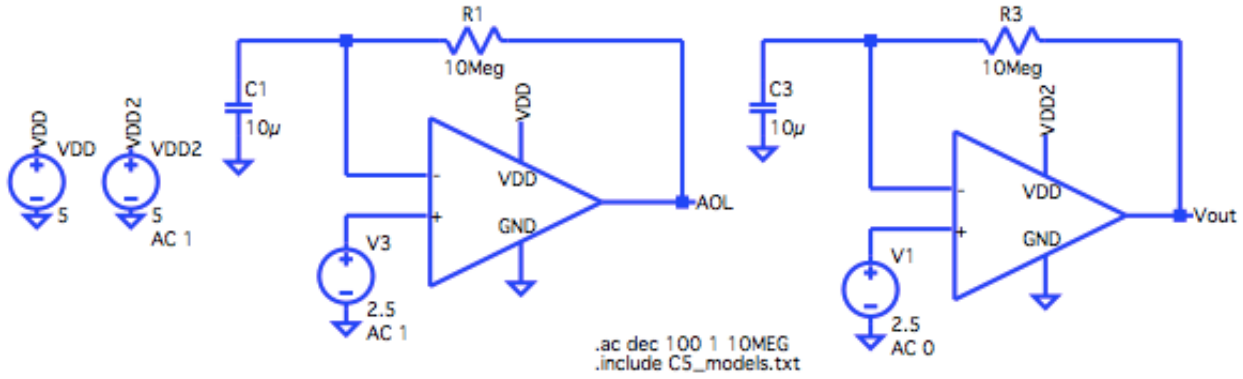

Figure 11a – schematic for PSRR+

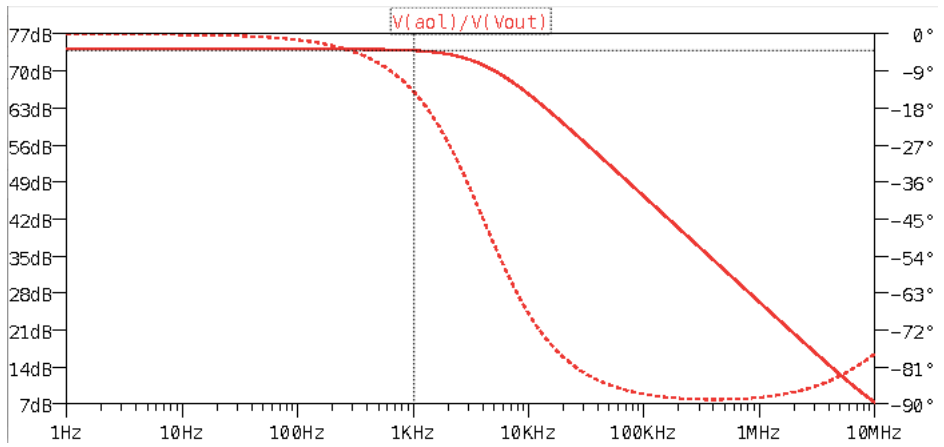

Figure 11b – schematic for PSRR+ at VDD = 5V; 73.88dB at 1kHz

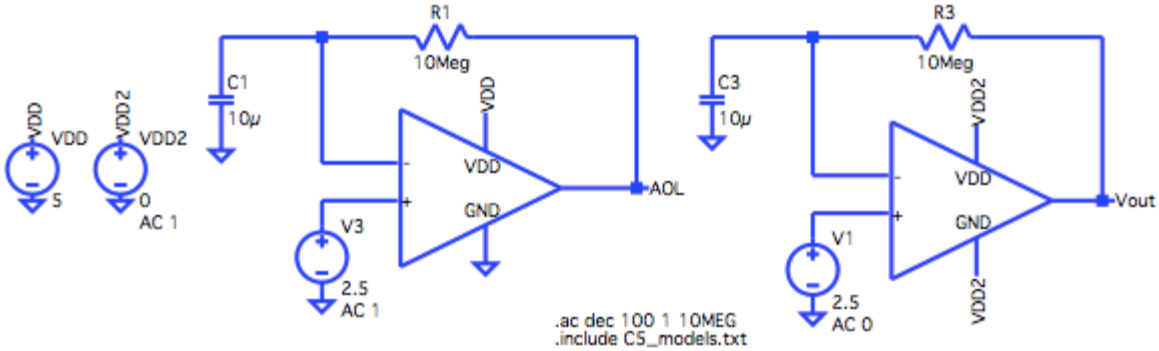

Figure 12a – schematic for PSRR+

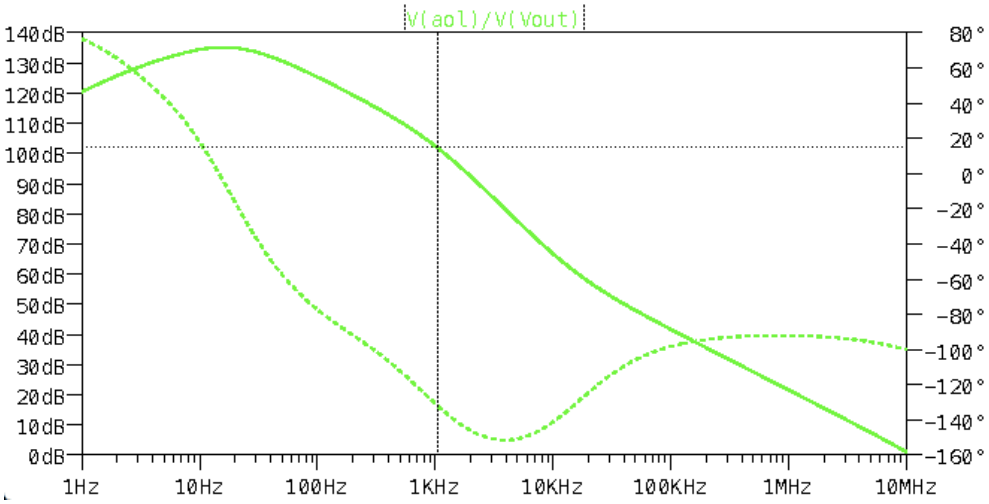

Figure 12b – response for PSRR- at VDD = 5V; 101.8dB at 1kHz

Common Rejection Ratio (PSRR)

The Common mode rejection ratio is the measure of the ability of the system to clean common mode voltage, which is unwanted noise. It is measured by taking the ratio between the common mode gain and the differential mode gain. The following equation relates the two gains:

$$CMRR = 20 * \log \left| \frac{Ad}{Ac} \right|$$

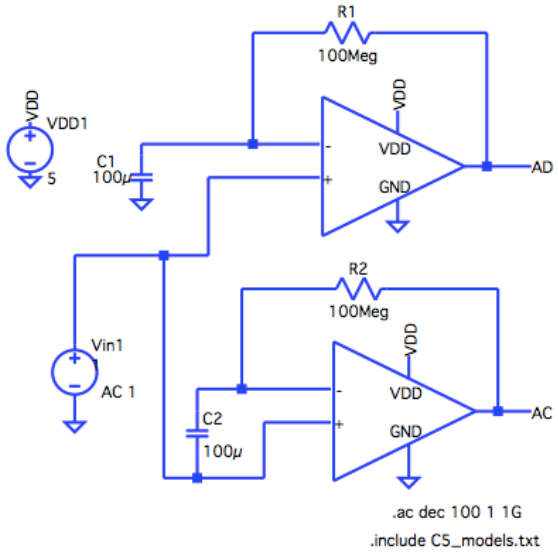

Figure 13a – schematic for finding CMRR

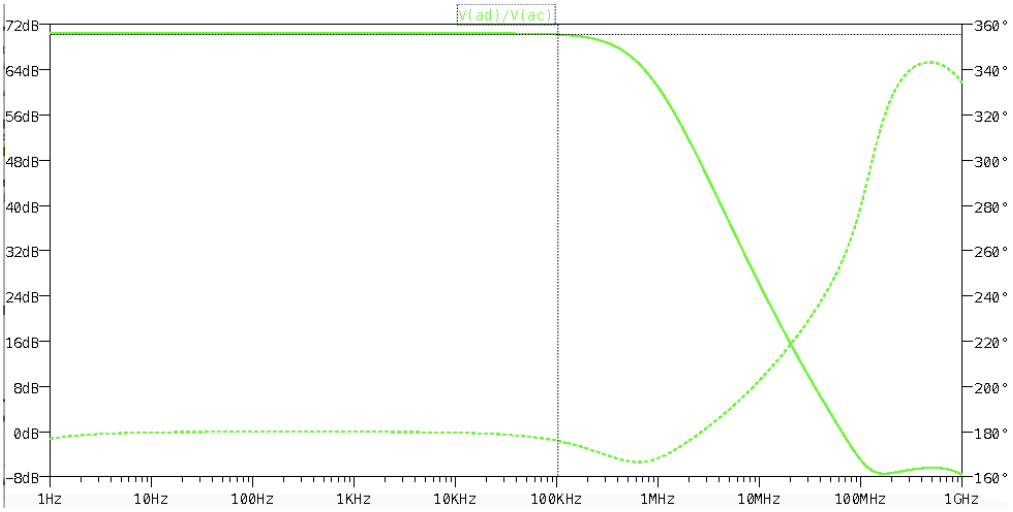

Figure 13b – response for CMRR- at VDD = 5V; 70.27dB at 100kHz

Design Trade-Offs and Possible Modifications

Overall, this op-amp performs beyond most of the requirements that were listed. The main goal for this project was to create a high gain op-amp that took low voltage and lower power operation into account. It can be seen both in the summary tables and throughout the report that the amplifier does precisely that.

As with any design, there are always ways in which things can be modified to fit different design requests. Below is a list of parameters that could be changed to meet different design requirements to make it more fit for different scenarios. Along with each of these changes, also listed is the design tradeoff that would occur.

- *Enhancing the gain:* When driving a full load, this amplifier meets the requirements of 60dB only by a small margin. The first improvement to the design that should be made is an increase in this value so that it will work for all loads with a larger margin of error. The use of minimum length devices (L=1) was beneficial to my design because it allowed for a very fast op-amp (which can be seen in my slew rate). The drawback of using the minimum length device in this design (and in op-amp design in general), is the considerable reduction in the open loop gain. The use of devices that are 2-5 times the minimum length would result in a consider gain enhancement, but would have drawbacks in other areas.
- *Improving the CMRR:* The common mode rejection ratio is a proportion of A_D over A_c. With this in mind, it is intuitive that increasing the value of A_D or decreasing the value of A_C will improve the CMRR. AD is directly related to the differential amplifier that includes 40 NMOS devices in parallel – to increase the gain at this branch of the op-amp, the width could be increased. Increasing the width of these parallel devices will in turn increase their transconductance, as seen in the equation

  $$gm = \sqrt{2IDKp(\frac{W}{L})},$$

  where gm is the transconductance. The increase in this value will thereby increase the ratio given through the CMRR equation, which will improve the results. Of course, the design tradeoff for increasing the width of all forty of these devices is that it requires more power consumption. This design has a relatively low power consumption, so this may be a desirable tradeoff in many designs.
- *Improving the Input Common Mode Range:* It can be seen that the common mode range for this amplifier has a relatively high minimum value (V_{cmMin} = 1.1V). This is the value that the differential amplifier needs to stay above in order to stay in saturation and work properly. In order to lower this value, the V_{DSsat} of each MOSFET could be lowered. In this design, V_{DSsat} was chosen to be 2.5% of the minimum VDD, which is 75mV. This percentage was chosen with general design rules in mind (which call for 5% of VDD), so it can obviously be changed to fit different designs. However, as with so many other parameters in the design of an op-amp, there are design trade-offs associated with doing

so. Lowering the V_{DSsat} of the MOSFETs will improve the common mode minimum voltage at the cost of the device stability. Since the V_{DSsat} value is the minimum voltage required to keep the MOSFET operating in saturation, decreasing this value will force the device closer to the edge of saturation, which could cause undesirable operation (such as MOSFETs falling into the triode region).