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EE 421: Digital IC Design

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Boost Switching Power Supply

The Boost SPS (Switching Power Supply) is a power supply circuit that can output a constant voltage of higher potential than the VDD used to power the circuit. For this project, the Boost SPS was designed to output a constant **Vout = 5 V** for **VDD** ranging from **3.75 V to 4.75 V**, and this **5 V** output is able to supply a constant voltage to loads that draw no current **(0 mA)** up to loads that draw **20 mA** of current. Below are tables summarizing overall efficiency and performance of the design.

Summary of Results

Summary of Results at Different Temperatures (Load Current = 20 mA, VDD = 4.25 V)

Temperature (ºC)	Avg. Vout (V)	Min. Vout (V)	Max. Vout (V)	VRipple (V)	Avg. I(VDD) (mA)	Efficiency
0	5.004	5.003	5.005	0.002	26.34	0.894
25	5.001	5.000	5.002	0.002	26.15	0.899
50	4.994	4.993	4.994	0.001	25.65	0.916
75	4.984	4.984	4.985	0.001	25.30	0.927
100	4.975	4.974	4.975	0.001	25.17	0.930

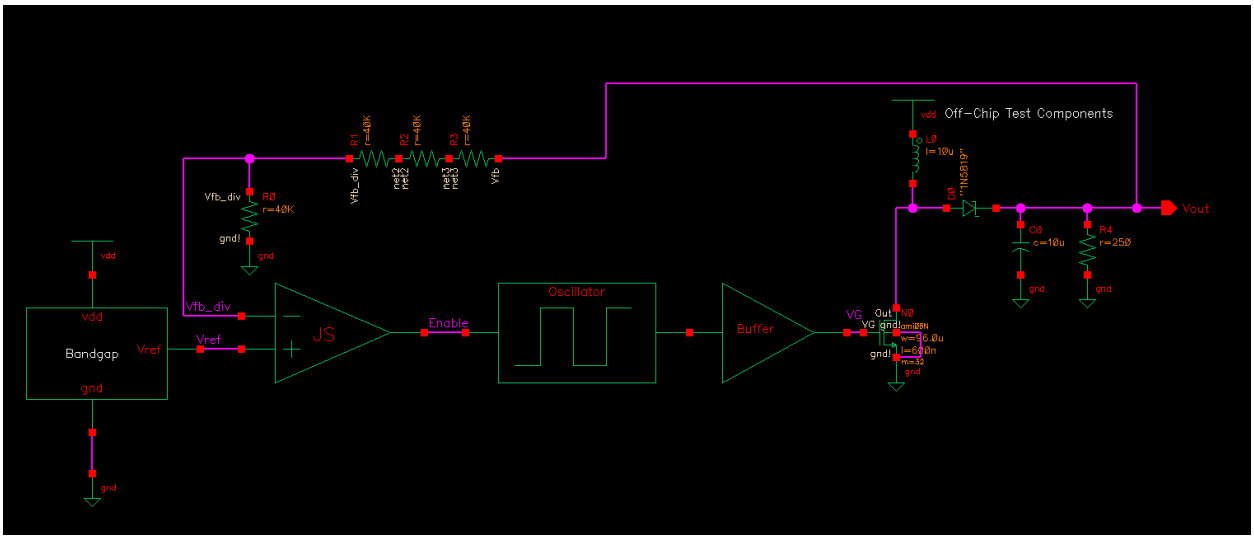
Summary of Results for Different Power Supply Voltages (Load Current = 20 mA, Temp = 27 ºC)

VDD (V)	Avg. Vout (V)	Min. Vout (V)	Max. Vout (V)	VRipple (V)	Avg. I(VDD) (mA)	Efficiency
3.75	4.994	4.993	4.994	0.001	29.08	0.916
4.00	4.997	4.996	4.998	0.002	27.48	0.909
4.25	5.001	4.999	5.002	0.003	25.94	0.907
4.50	5.004	5.002	5.006	0.004	24.78	0.897
4.75	5.008	5.005	5.011	0.006	23.78	0.887

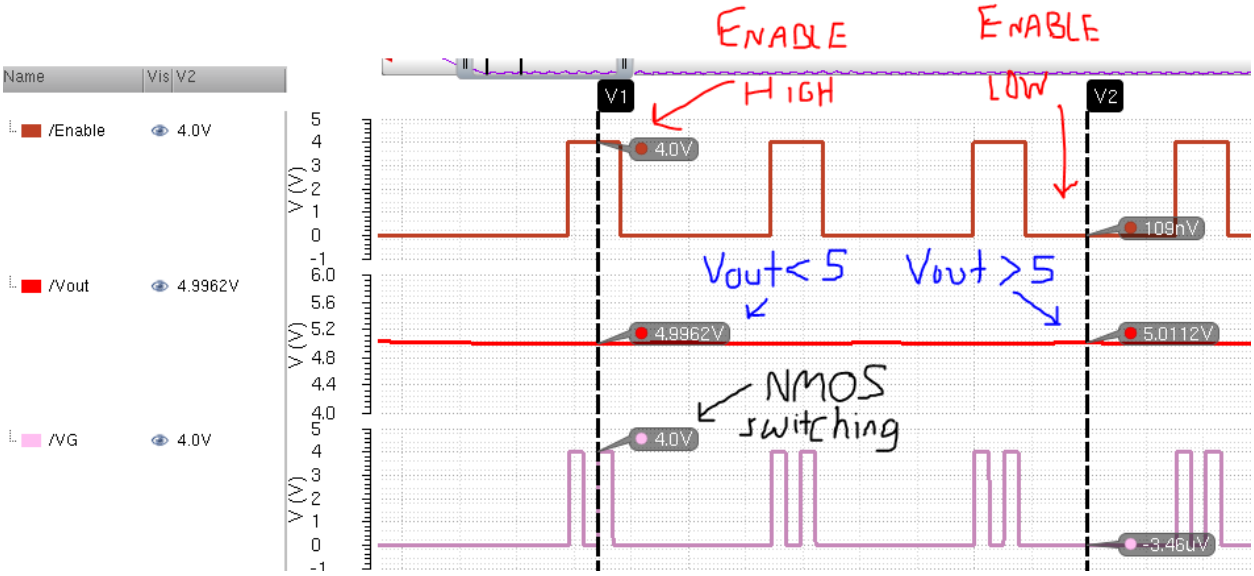
Design Tradeoffs

Component	Description of Tradeoff
Comparator Diff-Amps	• The transistor sizes (NMOS and PMOS) used in the diff-amps that make up the comparator were chosen to be 6u/0.6u. • **Pros:** Smaller layout, simplicity, less power consumption • **Cons:** Longer delay through diff-amps, larger Rp
Oscillator	• The transistor sizes (NMOS and PMOS) used in the inverters that make up the oscillator were chosen to be 6u/6u (weak). • **Pros:** Concise layout, delay for lower frequency (5.05 MHz) • **Cons:** Large switching resistances, greater power consumption
Buffer Stages	• The transistors used to makeup the buffer stages were chosen to have larger widths with smaller multipliers rather than larger multipliers and smaller widths. • **Pros:** Much smaller layout size, high gain • **Cons:** N/A
NMOS Switch	• The NMOs used as a switch and link between on-chip logic and off-chip components was chosen to have a very large width-to-length ratio. • **Pros:** Very low switching resistance, small voltage drop across switch, can supply large currents off chip • **Cons:** Large layout size, large input capacitance

Shown here is a high-level view of the schematic, including on-chip logic and off-chip components.



The portion of the simulation below shows the operation of the boost SPS. When the output **Vout < 5 V,** we see that the **Enable** signal goes high to enable the oscillator. When the output **Vout > 5 V,** the **Enable** signal goes low and turns off the oscillator. We can see that while **Enable** is high, the gate of the large NMOS device (modeled by **VG** in the simulation) is switching on and off, allowing the off-chip inductor to release energy into the load through the diode. When the inductor is all out of energy, the load capacitor is there to maintain **Vout = 5 V.**



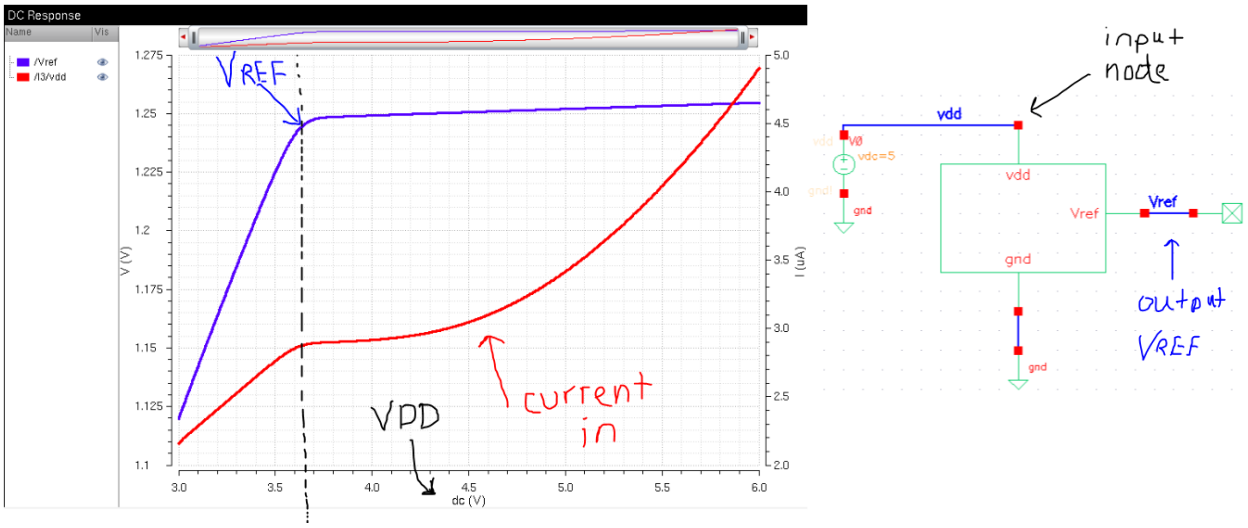
This report discusses and shows in detail the design process of each individual component and circuit listed previously. Each component of the SPS was designed, tested and simulated, and laid out in Cadence.

Part 1: Bandgap Voltage Reference Circuit

The bandgap voltage reference circuit is a circuit that outputs a (near) constant voltage regardless of change in **VDD (power supply voltage)** and change in temperature. The bandgap in the boost switching power supply will be used to output a reference voltage of **1.25 V**, and this reference voltage will serve as an input to the comparator (discussed later on).

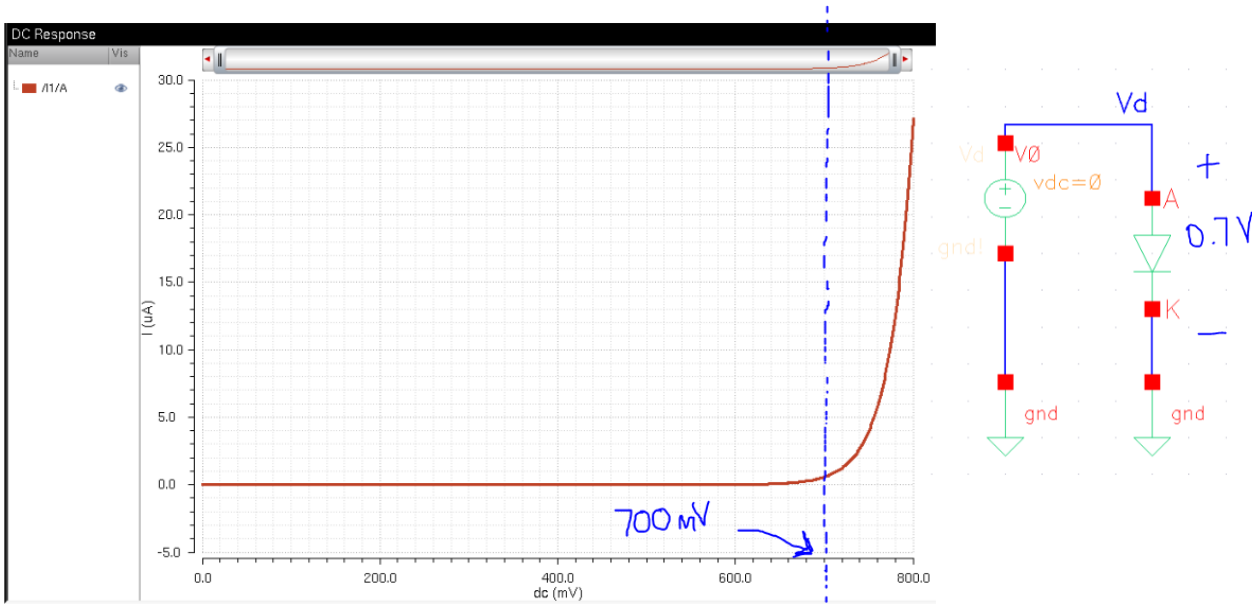
The following simulations provide insight regarding the operation of the bandgap reference circuit, including plots that show the output voltage **(Vref)** for varying power supply voltage and varying temperature, and plots that show the built-in potential of the parasitic pn-junction diode as temperature changes, and the amount of current conduction through the diode for varying voltage across it.

Bandgap Simulation for Increasing VDD Values



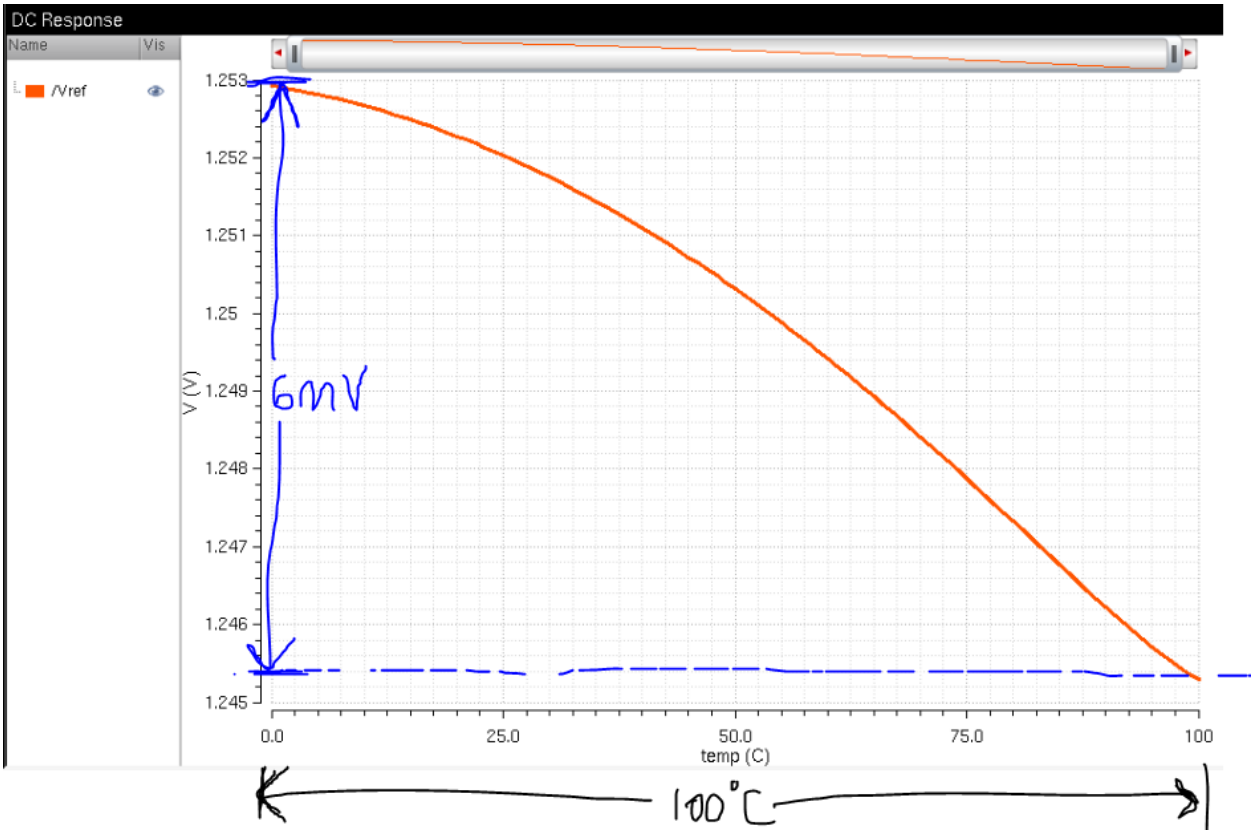
This simulation shows the output voltage of the bandgap reference circuit **(Vref in blue)** along with the current that flows at the indicated node. We observe from the plot that for voltages less than roughly **3.7 V** on **VDD**, the **Vref** output is increasing linearly until it reaches around **1.25 V**, where it remains steady for an observable voltage range of **3.7 V < VDD < 6V**, roughly. We can also observe from the plot that as **VDD** increases, current flowing into the bandgap also increases. Regardless of **VDD** and current increases, **Vref** remains right around **1.25 V** with only millivolts of variance.

Bandgap Simulation for Built-In Diode Potential



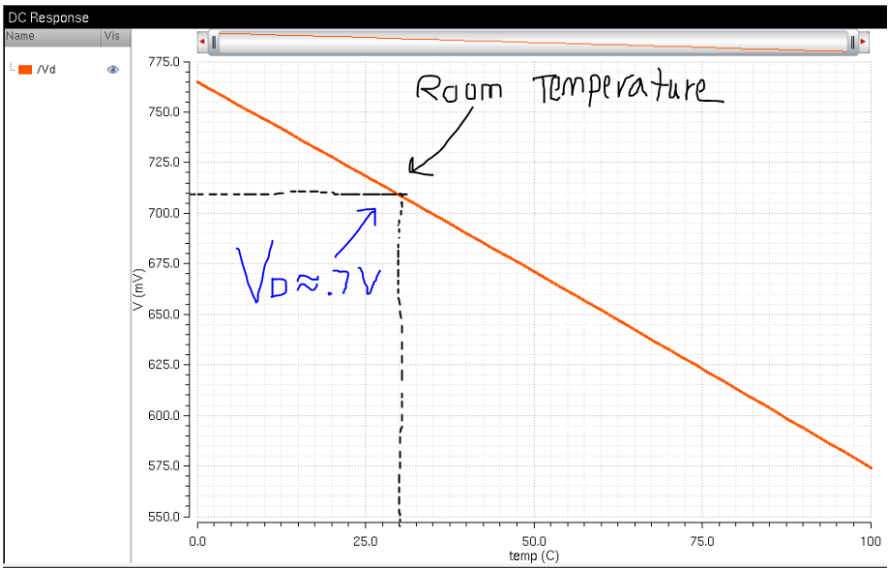
We know from electronics and further studies of pn-junction diodes that the built-in potential is roughly **700 mV or 0.7 V**. For a diode to turn on, the voltage across it must be greater than its built-in potential. This simulation plots the current through the circuit as the input voltage, or the voltage across the diode, is increased from **0 V to 800 mV**. We can observe from the simulation that at just about **700 mV**, the diode begins to conduct current, and this is exactly what we would expect to happen. Once the diode's built-in potential is overcome, it begins conducting current.

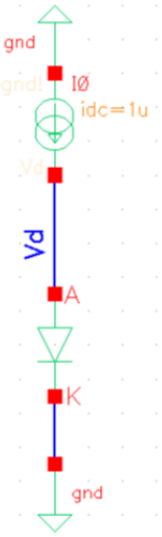
Bandgap Simulation for Increasing Temperature



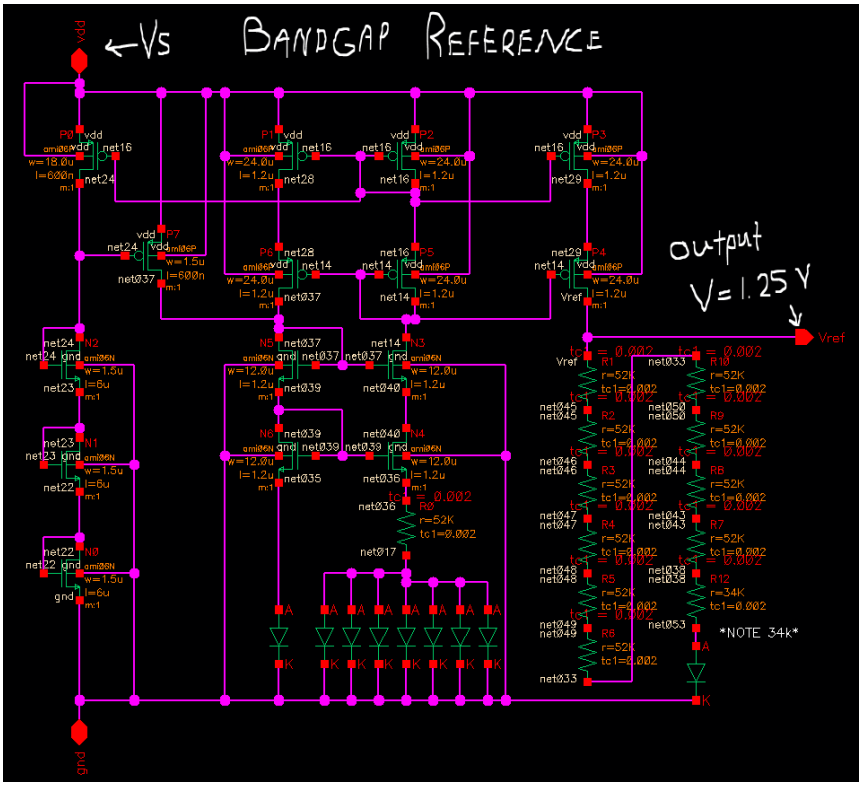
This simulation sweeps the temperature from **0 ºC to 100 ºC**, from the freeing point of water to the boiling point of water. We are observing the output voltage of the bandgap circuit, **Vref,** as temperature increases. Taking a look at the graph, we observe that at **Temp = 0 ºC, Vref** is roughly **1.253 V**, and at **Temp = 100 ºC, Vref** is roughly **1.246V**. This a notably small change in output voltage over such a wide temperature range. Vref only changes about **7 mV** over a one hundred degree temperature sweep (in Celsius).

Bandgap Simulation for Built-In Diode Potential

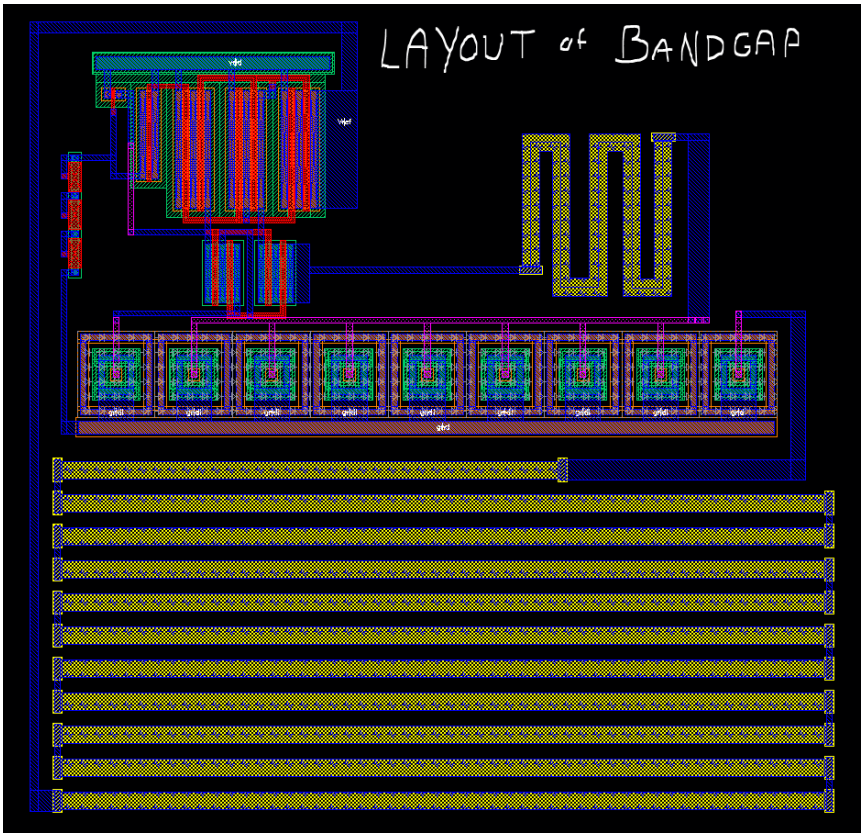




Sending a constant current through the diode in this simulation allows us to observe how the built-in potential of the diode changes as temperature changes. We know that at room temperature, the built-in potential is roughly **700 mV**, as is shown in the plot. From the graph, we can observe that as temperature increases, the built-in potential of the diode decreases linearly. This means that as temperature increases in the bandgap circuit, it would take a smaller potential to forward bias the diode. We can also observe that as temperature decreases, built-in potential increases, and it would take a higher potential to forward bias the diode.



Schematic View of Bandgap Voltage Reference Circuit



Layout View of Bandgap Voltage Reference Circuit

This layout passes DRC and LVS verifications.

Part 2: Comparator and Feedback Divider

The comparator, made up of cascaded diff-amps with buffers on the output, is a component that takes in two inputs, and depending on which input is of greater potential, will either output **VDD** (a logic 1) or **ground** (a logic 0). We want our comparator to output a logic 0 when **Vout** (the final output voltage of the SPS) is greater than **5 V**, and to output a logic 1 when **Vout** is less than **5 V**. Designing for this operation, our plus terminal input will be **Vref**, the output of the bandgap reference circuit, and our minus terminal input will be **Vfb (feedback voltage),** one-fourth of **Vout**, so that it can be compared to the **Vref of 1.25 V**.

The comparator is used to sense changes in **Vout.** We need to send **Vout** through a resistive divider in order to pull a voltage into the comparator that can be compared with **Vref.** This voltage divider circuit, according to project specifications, should draw no more than **50 µA** of current, and no less than **10 µA** of current.

Selecting Resistor Values

We want current flowing through the divider between **50 µA and 10 µA.** To be safe, we will pick a value right in the middle of the current range, say **30 µA.**

$$V = IR \rightarrow R = \frac{V}{I} \rightarrow R_{total} = \frac{5V - 0V}{30\ \mu A}$$

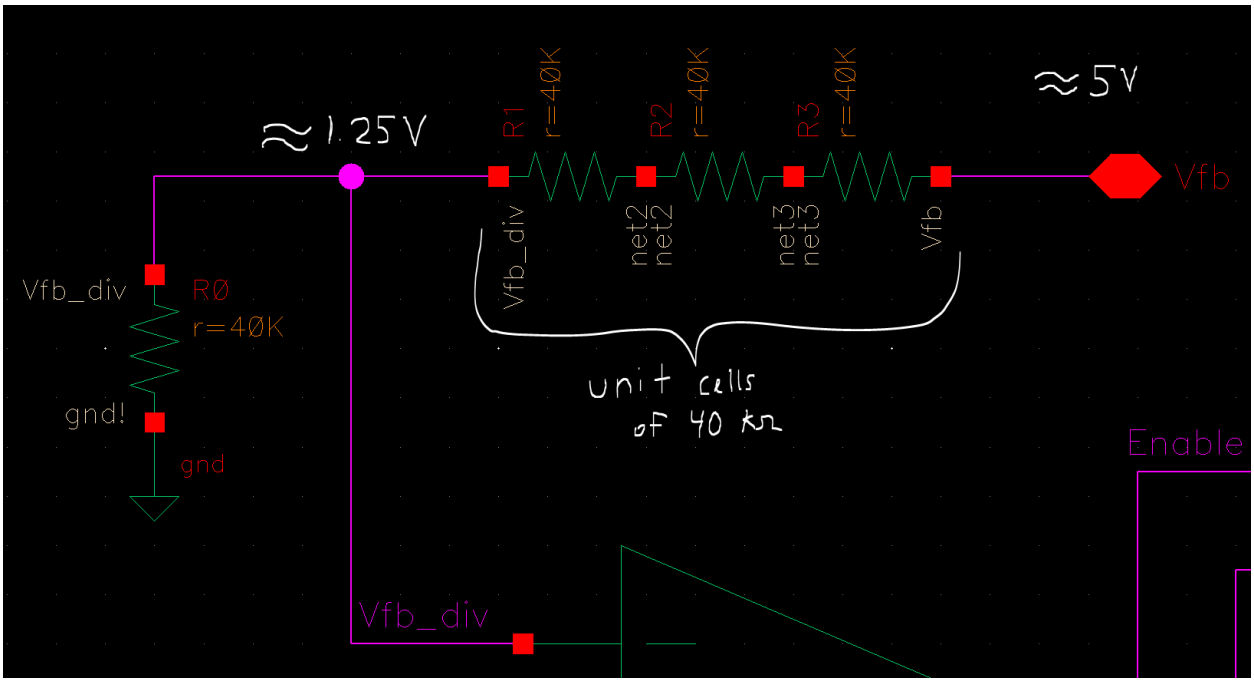
$$\boldsymbol{R_{total} = 166.666\ k\Omega}$$

For nicer resistance values, since we know we are well within the range, we can round the total resistance down to an even **R = 160 kΩ.** In order for **Vref** to be comparable to **Vout**, we need a resistive **3-to-1 divider**.

Using unit cells will give:

$$R_1 = \frac{R_{total}}{4} = \frac{160\ k\Omega}{4} = \boldsymbol{40\ k\Omega}$$

$$R_2 = 3R_1 = 3(40\ k\Omega) = \boldsymbol{120\ k\Omega}$$

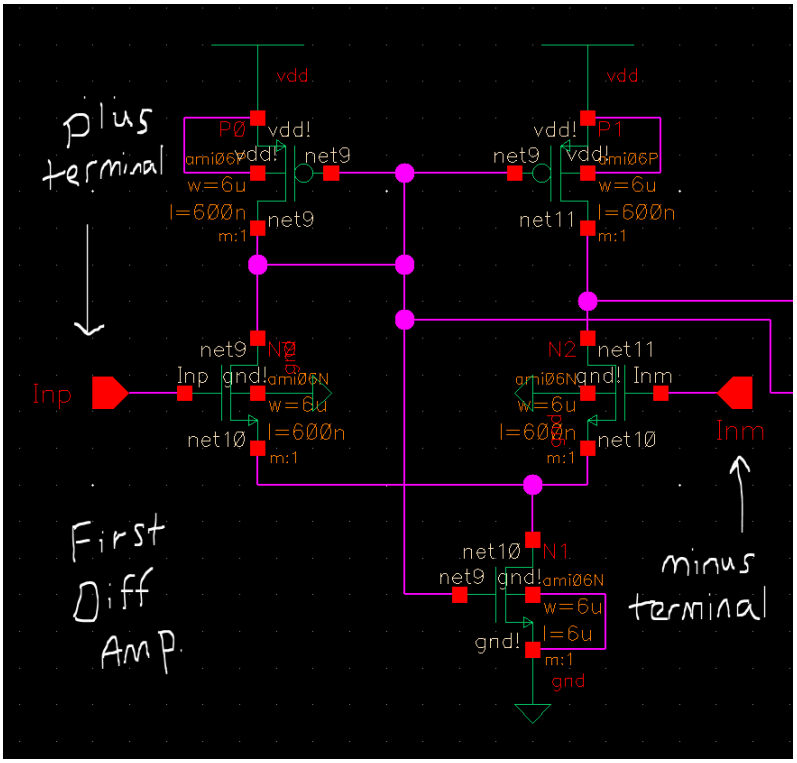


Above, we see that the resistive divider output, **Vfb_div,** is being fed into the minus terminal of our comparator. If the output voltage goes above **5 V,** then the comparator will output a logic 0 because the potential on the minus terminal will be greater than **Vref,** the potential on the plus terminal.

For the diff-amps that make up the comparator, W/L ratios for both the PMOS and the NMOS were selected to be 10/1 for simplicity. Here we find our first **tradeoff.** We know that in the C5 process, using a PMOS device with twice the width of the NMOS device (with both devices having equal lengths) will result in the devices having equal switching resistances, **Rn** and **Rp.**

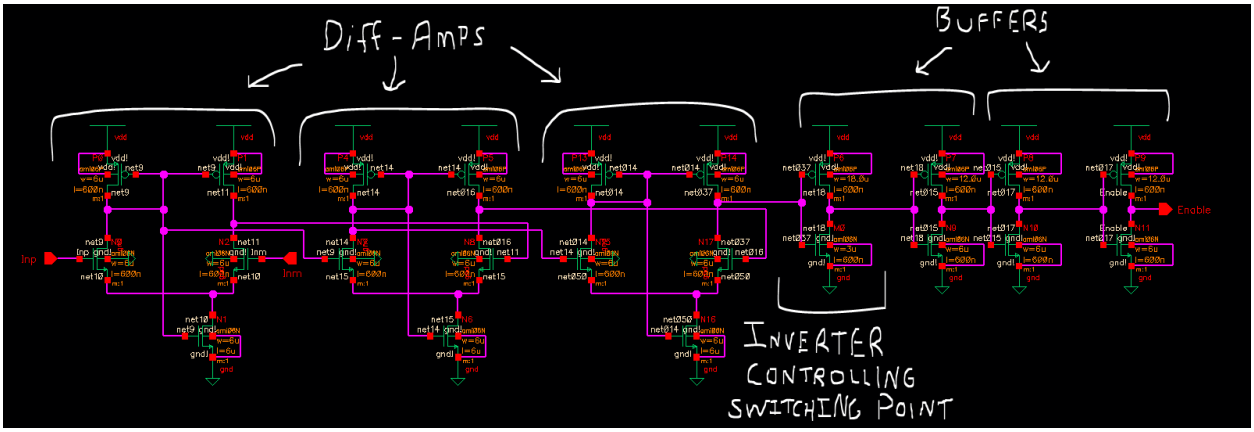
In this case, we sacrifice equal switching resistances for less power consumption, simplicity, and smaller layout size. Using 10/1 PMOS devices keeps **Rp** at 4k for each PMOS (where **Rp** would be 2k for 20/1 device, more current would flow, and more power would be dissipated). Furthermore, 10/1 PMOS devices take up half as much layout space as 20/1 PMOS devices do. It is also simpler for a designer to use devices that are the same size.

Shown below is the first diff-amp in our comparator. The comparator is made up of three cascaded diff-amps, with the second and third diff-amps being identical to the one shown below.



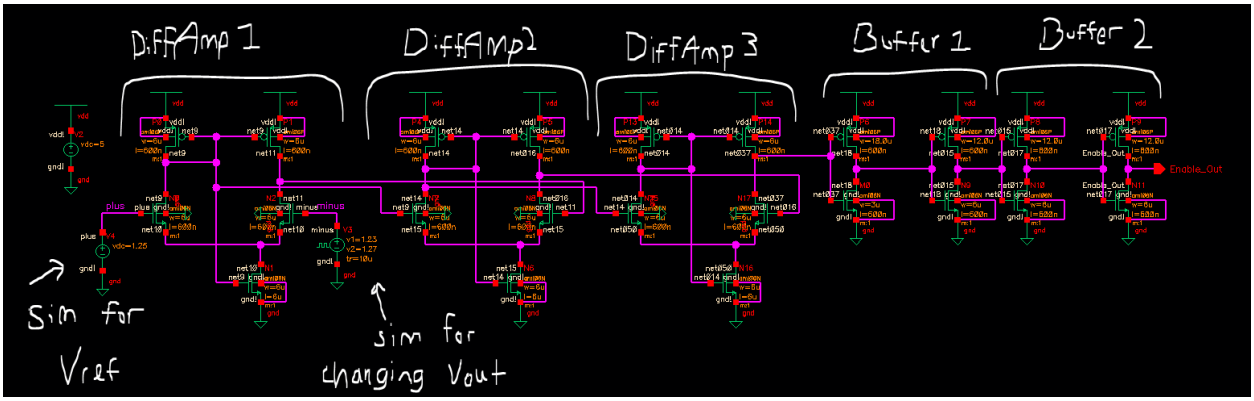
Schematic View of First Differential Amplifier (Diff-Amp) in Comparator

Shown here is the full comparator schematic, with diff-amps and buffers labeled. The first inverter (which makes up part of the first buffer) is used to control the switching point of **Enable,** the output of the comparator.

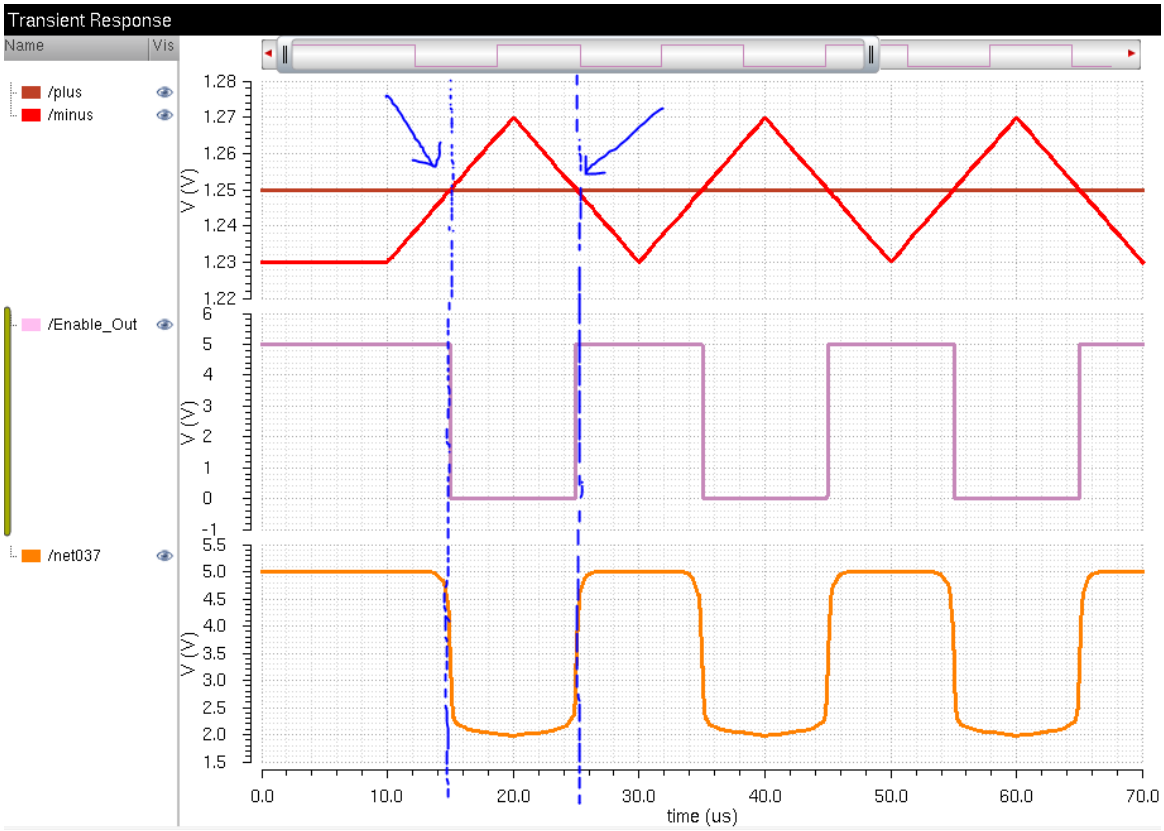


Full Comparator Simulation

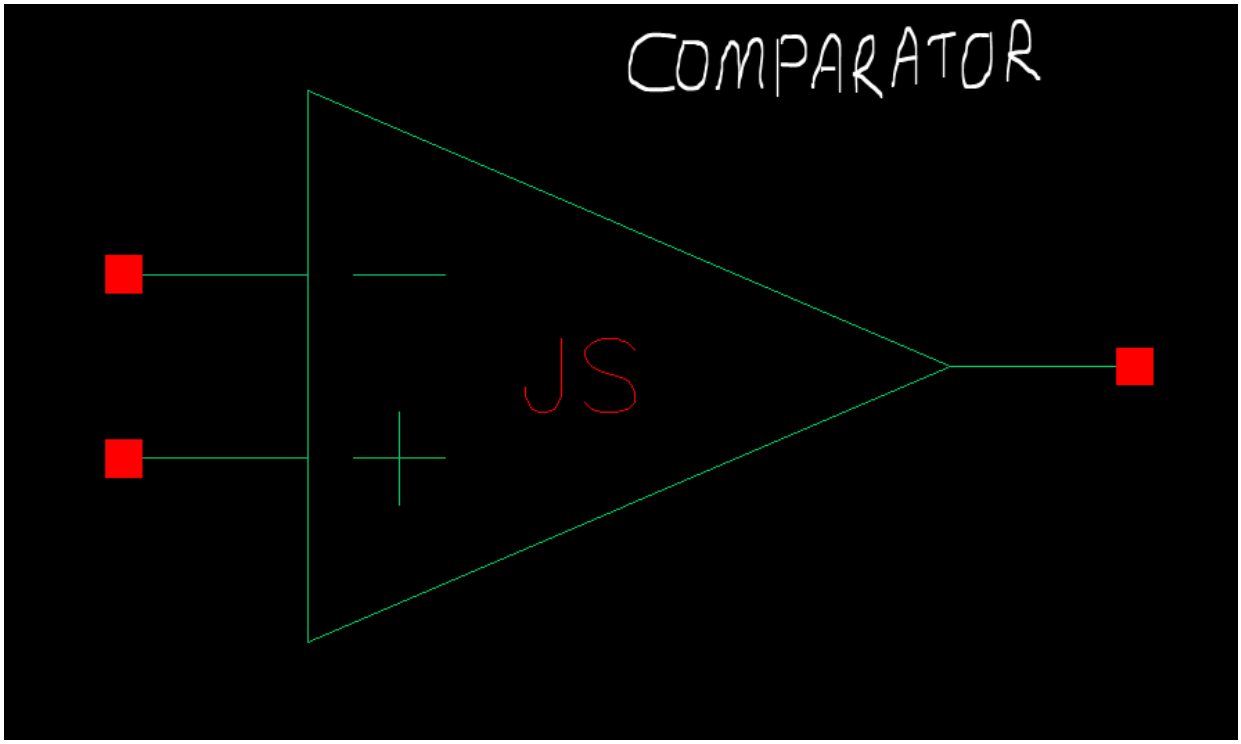
The comparator works by taking in values on two terminals (for my schematic the terminals are labeled **plus** and **minus**) and "comparing" them, outputting a logic 1 (**VDD**) if the potential is greater on the **plus** terminal, and outputting a logic 0 (**ground**) if the potential is greater on the **minus** terminal.



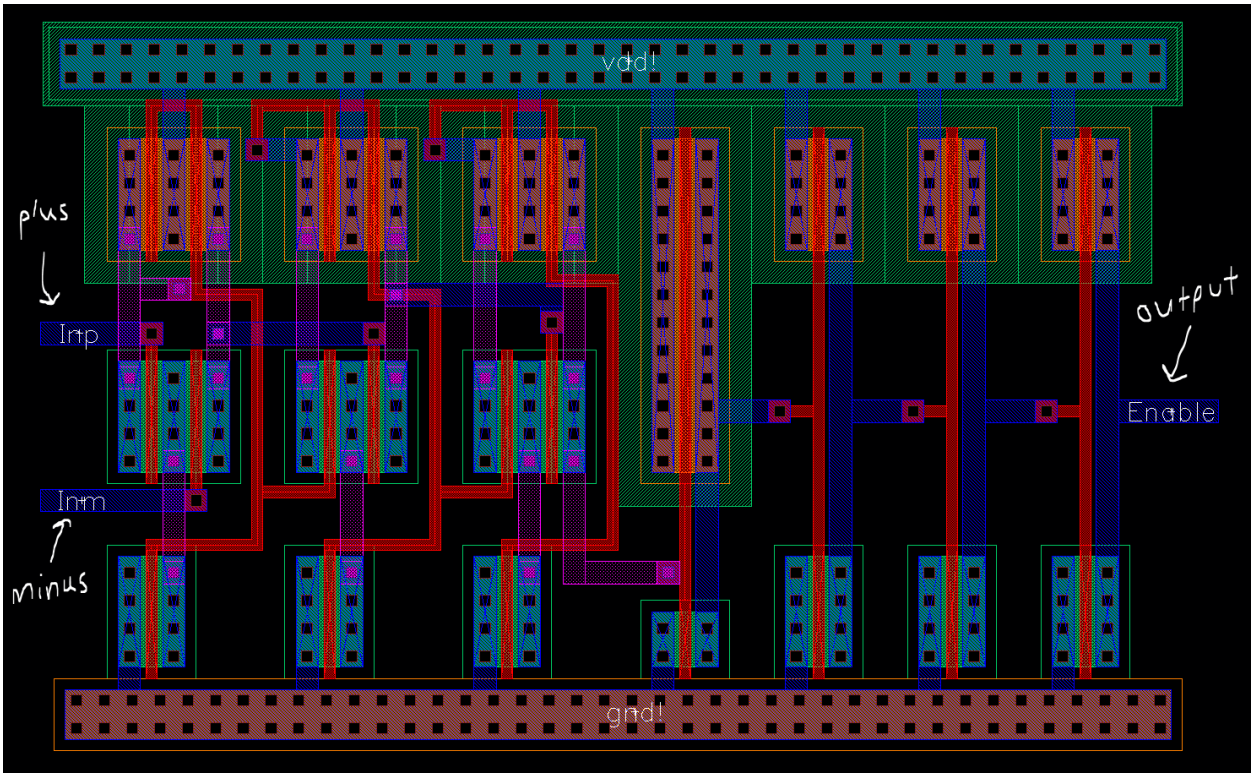
For this simulation, we will use a DC voltage source with a voltage of 1.25 V to model **Vref**, the output of the bandgap reference circuit. We will also use a pulse voltage source (with rise time and fall time set to half of the period) to model linear changes in **Vfb,** the feedback voltage from **Vout**. We see in the plot below that the comparator is working properly.



Comparator Symbol



Comparator Layout



The above layout passes both LVS and DRC verification.

Part 3: Oscillator Circuit and Frequency

The oscillator in the Boost SPS is used to control the duty cycle and frequency of the circuit's operation. The oscillator is implemented as a ring oscillator made up of cascaded "weak" inverters (long L devices) controlled by a NAND gate. The NAND gate takes in the **Enable** signal from the comparator as one input, and the output of the final inverter in the ring oscillator as the other input. In order to understand how the NAND gate "controls" the oscillator, we need to look at the NAND gate truth table.

NAND

A	B	Out
0	0	1
0	1	1
1	0	1
1	1	0

Shown here is the NAND gate truth table. For our oscillator, the **Enable** input will be our **A** input and the oscillator feedback will be our **B** input.

NAND

A	B	Out
0	0	1
0	1	1
1	0	1
1	1	0

When **Enable** is low, the output of the NAND gate is always high. Therefore when **Enable** is low, the NAND gate "shuts the oscillator off" effectively, because the output of the NAND gate does not change regardless of the **B** input.

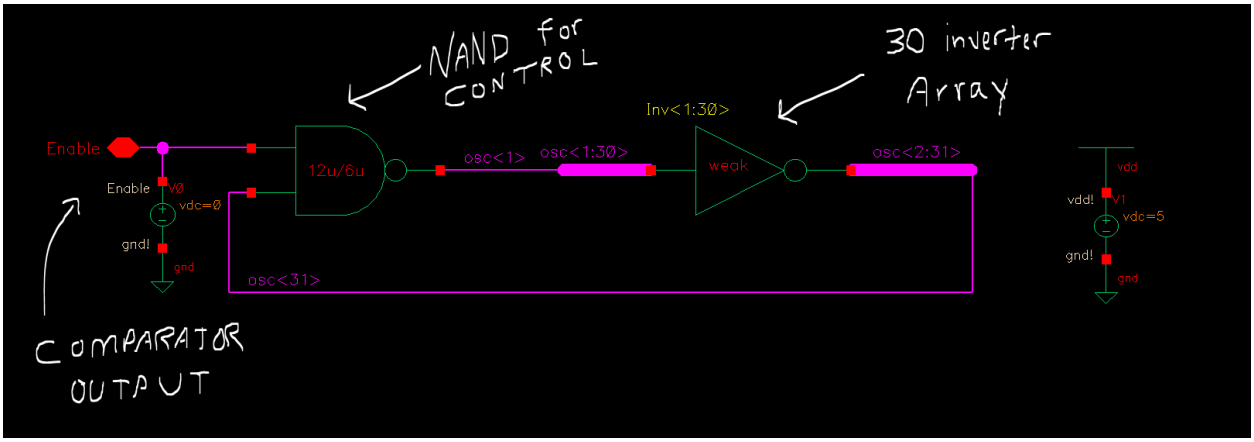
NAND

A	B	Out
0	0	1
0	1	1
1	0	1
1	1	0

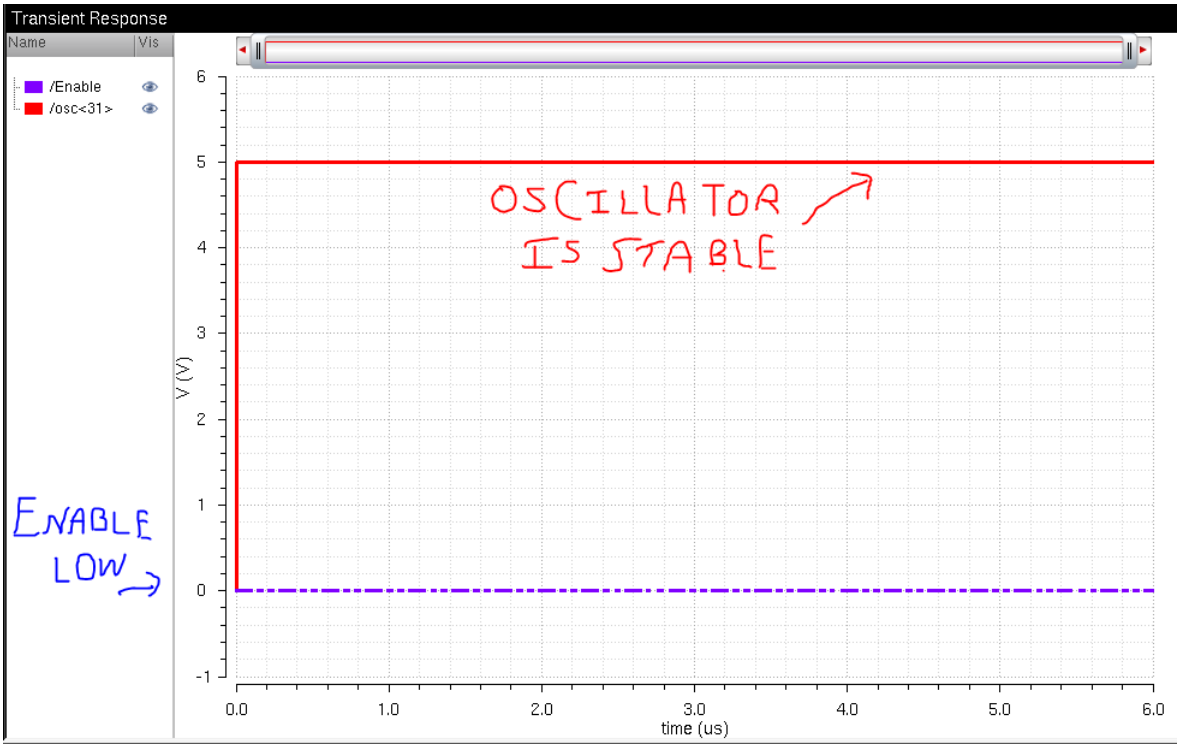
When **Enable** is high, the output of the NAND gate is **B',** the inverse of **B.** Therefore when **Enable** is high, the NAND gate acts like an inverter, and we expect the oscillator to oscillate.

When Enable is Low

As was mentioned previously, when **Enable** is low, we expect to see the oscillator “off”, or not oscillating.



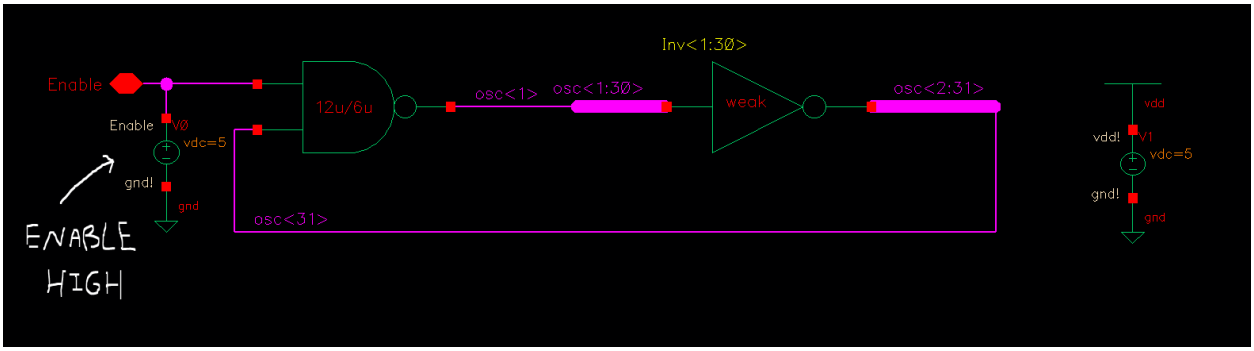
The above schematic models the behavior of the oscillator when **Enable** is low, placing a 0 V DC voltage source on the **Enable** input.



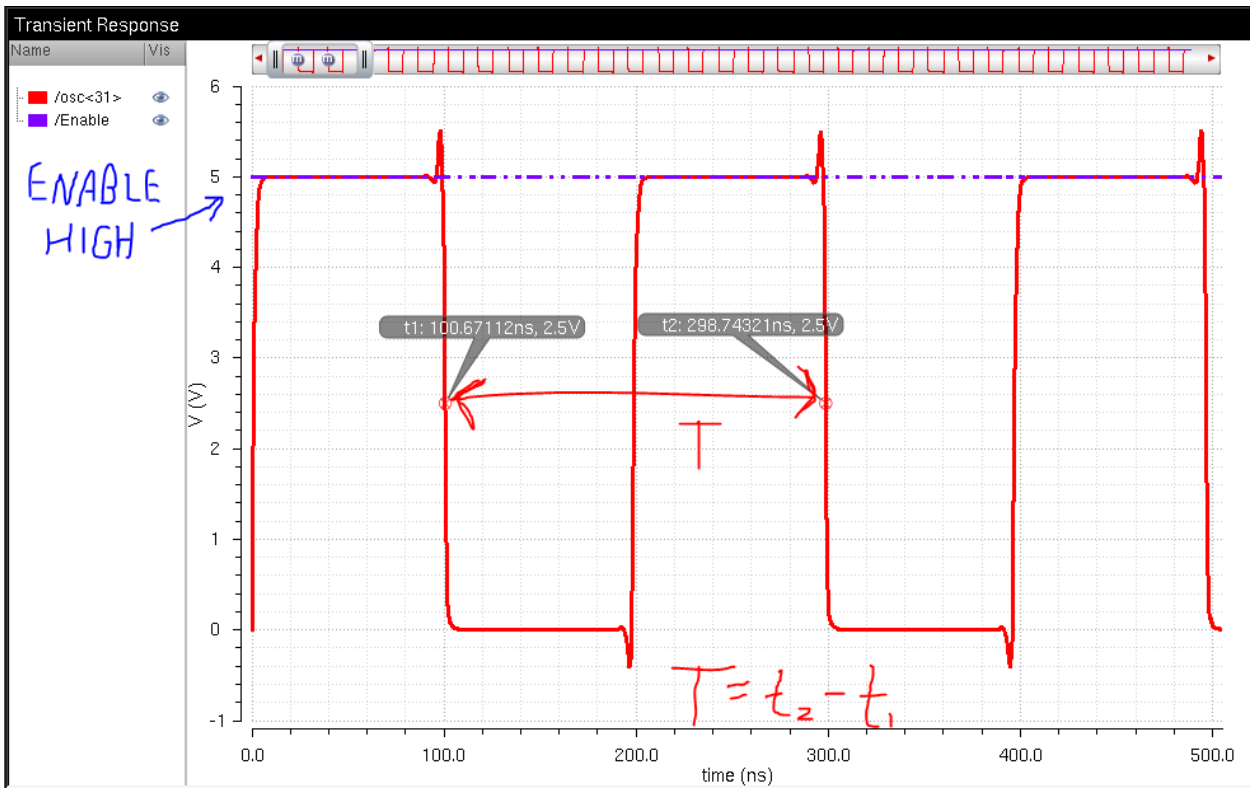
As was expected from the NAND truth table, when **Enable** is low, the output of the NAND, or **osc<1>,** is high. Therefore **osc<31>** is also high, and the oscillator does not oscillate.

When Enable is High

When **Enable** is high, we should see the oscillator oscillating.



Enable high is modeled using a 5 V DC voltage source.



We see in this simulation that the oscillator oscillates with a period T of 198 ns (around 200 ns).

$$f_{osc} = \frac{1}{T} = \frac{1}{198\ ns} = 5.05\ MHz$$

The circuit will operate at a frequency of 5.05 MHz due to the frequency of the oscillator when **Enable** is high.

Selecting Oscillator Device Parameters

I wanted to design my oscillator to have a frequency between 1 MHz and 10 MHz, but to also have a reasonable number of inverters for smaller layout size. In order to create greater delay between inverters and conserve layout space, weak inverters (long L devices) were used. A typical NMOS in the C5 process has a W/L ratio of 10/1 (6 um / 0.6 um). In order to weaken the inverter, we can bump the length up one order of magnitude and use 10/10 (6 um / 6 um) devices. For the C5 process, **C'ox = 2.5 fF / um^2, R'n = 20k** and **R'p = 40k.** The delay through these inverters will be large due to the following.

$$R_n = R'_n \frac{L}{W} = R'_n = 20k$$

$$R_p = R'_p \frac{L}{W} = R'_p = 40k$$

Because the MOSFETs are weak, the L/W is equal to 1, and the effective switching resistances are relatively large, increasing the overall delay through the oscillator. Increased delay results in larger cycle time or period T, which then results in a lower frequency. For the remaining calculations, it is necessary to calculate **tPLH** and **tPHL** of each inverter in the oscillator. The propagation times and capacitances needed to solve for frequency are given by

$$C_{oxp} = C'_{ox} * W_p * L_p = \frac{2.5\ fF}{\mu m^2} * 6\ \mu m * 6\ \mu m = 90\ fF$$

$$C_{oxn} = C'_{ox} * W_n * L_n = C_{oxp} = 90\ fF$$

$$C_{TOT} = \frac{5}{2}\left(C_{oxp} + C_{oxn}\right) = \frac{5(180\ fF)}{2} = 450\ fF$$

$$t_{PLH} = 0.7 * R_p * C_{TOT} = 0.7 * 40k * 450\ fF = 12.6\ ns$$

$$t_{PHL} = 0.7 * R_n * C_{TOT} = 0.7 * 20k * 450\ fF = 6.3\ ns$$

Per the CMOS book, the frequency of the ring oscillator is given by

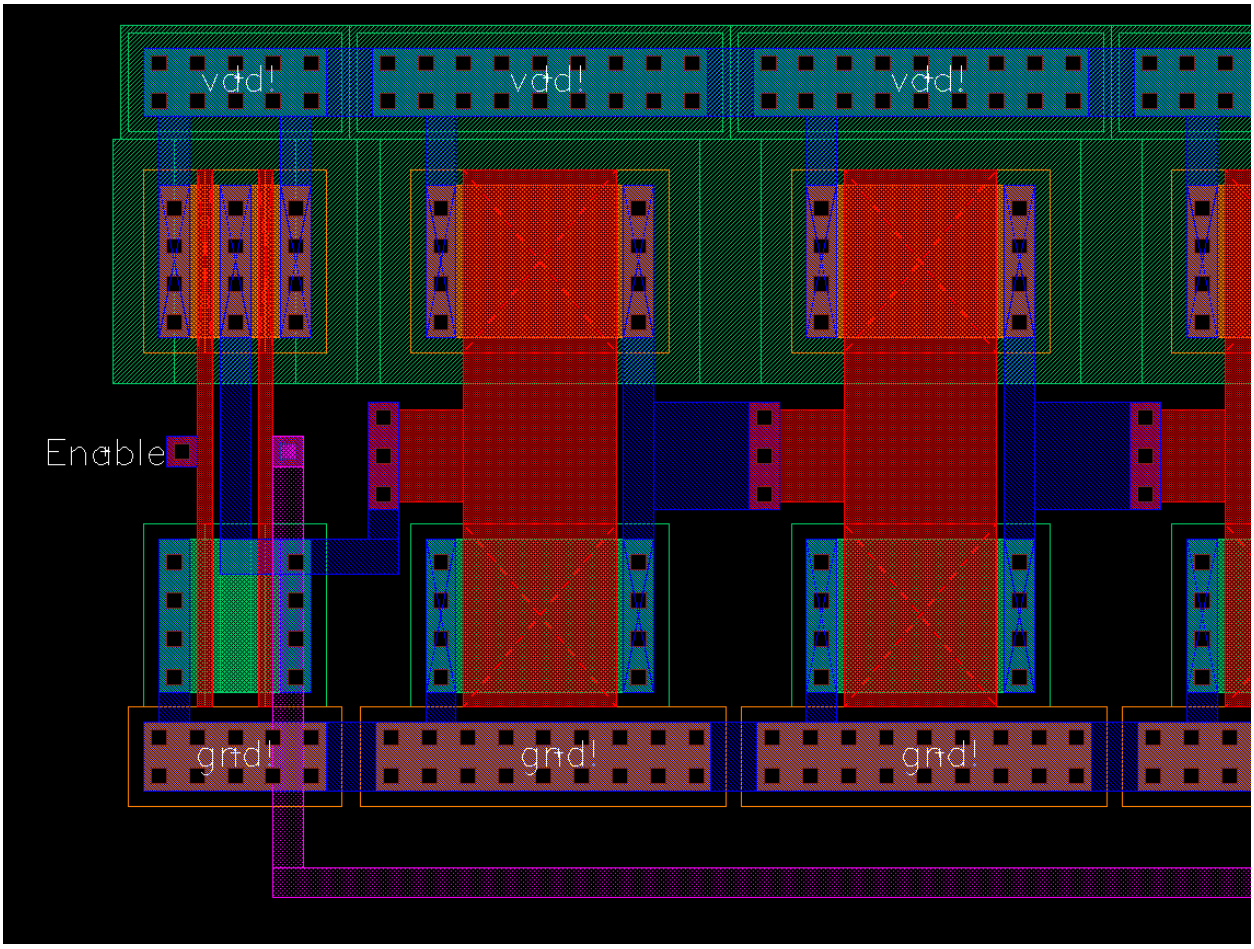
$$f_{osc} = \frac{1}{n * (t_{PHL} + t_{PLH})} \leftrightarrow n = \frac{1}{f_{osc} * (t_{PHL} + t_{PLH})} = \frac{1}{2\ MHz * (18.9\ ns)} = 27\ inverters$$

For a nice round number, I used 31 inverters in my ring oscillator. I ended up with a frequency of 5.05 MHz which is still in the range I was looking for, but not close to the 2 MHz I calculated for.

Oscillator Layout

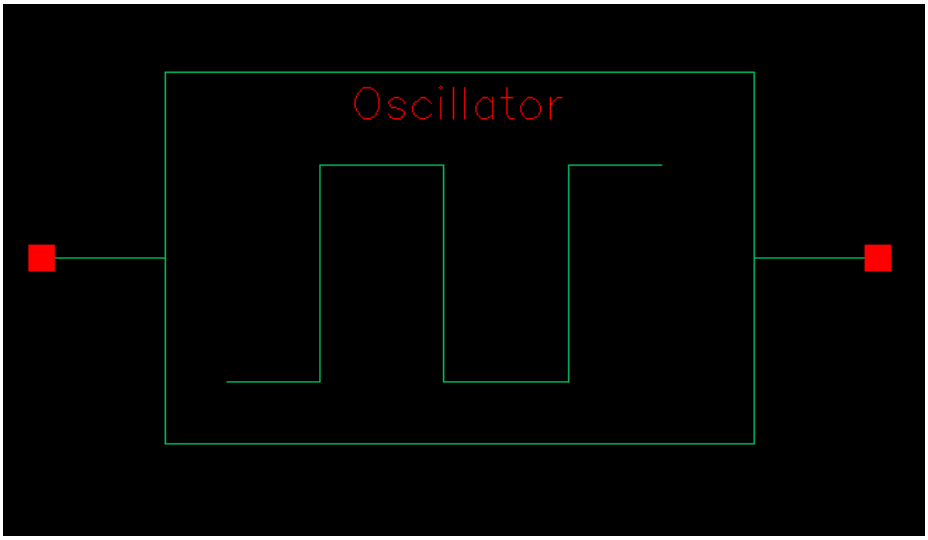
The complete oscillator layout is shown below. The first stage of the oscillator is the control NAND gate, labeled at the front end of the oscillator. One input to the NAND gate is **Enable**, the output of the comparator. The other input to the NAND gate is **osc<31>**, the output of the final inverter in the oscillator.

Below is a zoomed in view of the oscillator layout. We can observe the long L devices used in the oscillator, as well as the inputs to the NAND gate.



The above layout passes both LVS and DRC verifications.

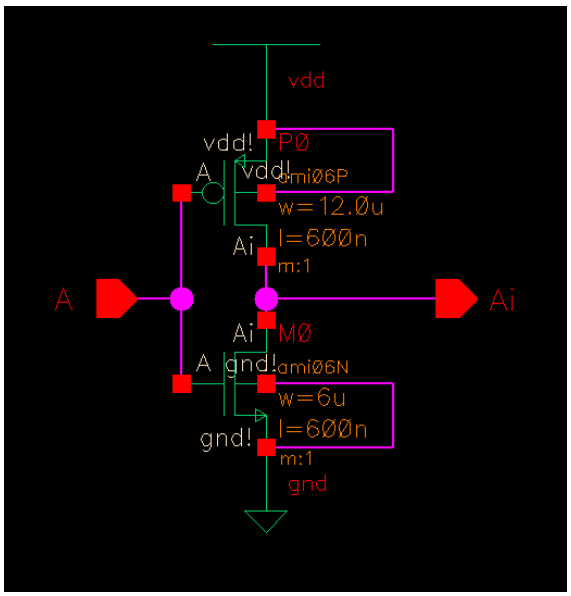
Oscillator Symbol View

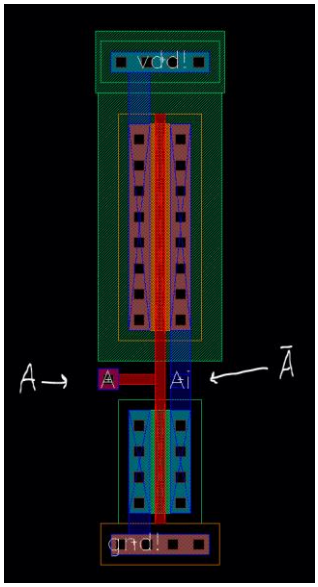


Part 4: Buffers for Driving NMOS Switch

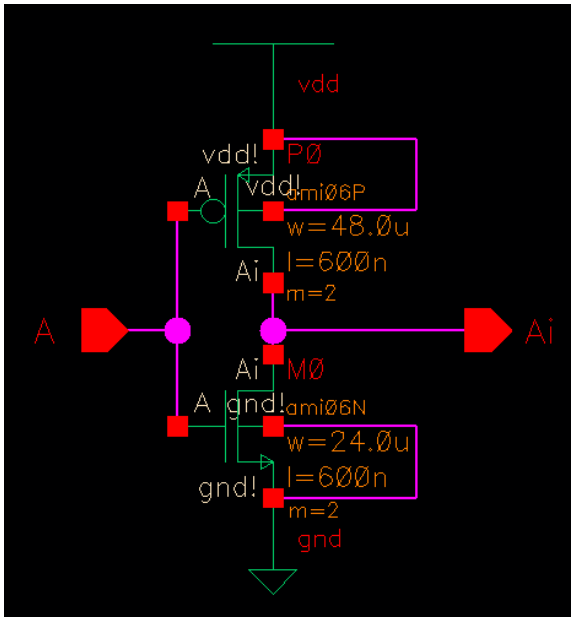
A large NMOS device will act as a switch between the oscillator signal and the off-chip components, opening and closing, connecting and disconnecting the bottom of the inductor to and from ground. Because the NMOS links off-chip components to on-chip circuitry, it needs to have a very low effective switching resistance, or have a large width. This large width, though it makes the resistance of the NMOS low, makes the capacitance of the NMOS very large. The following inverters make up the buffer that is used to drive the switching NMOS.

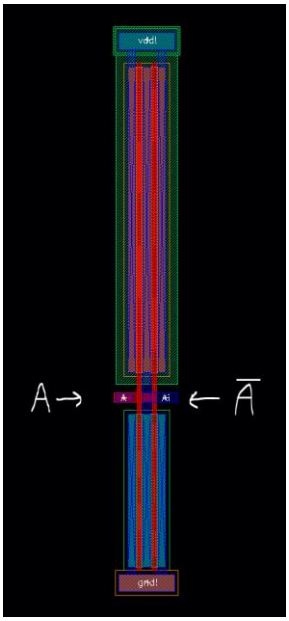
First Stage: 12u/6u Inverter, Multiplier of 1



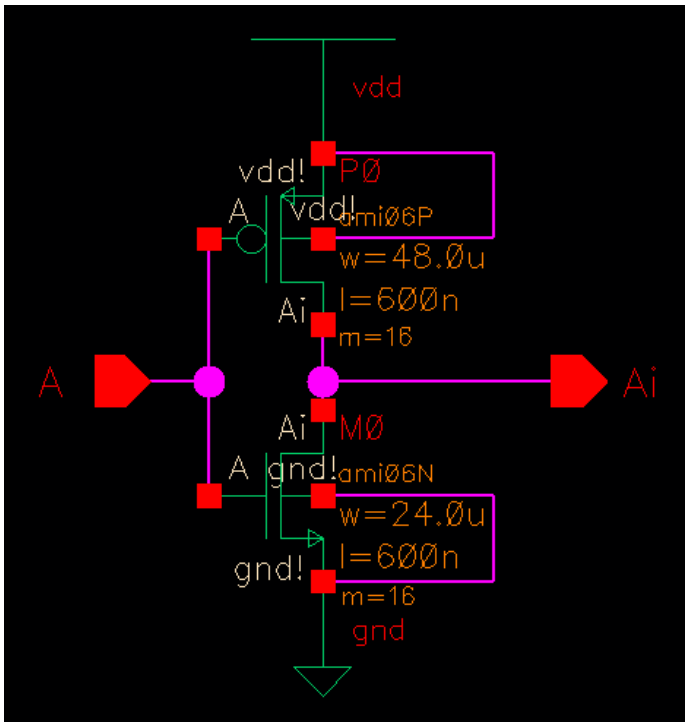


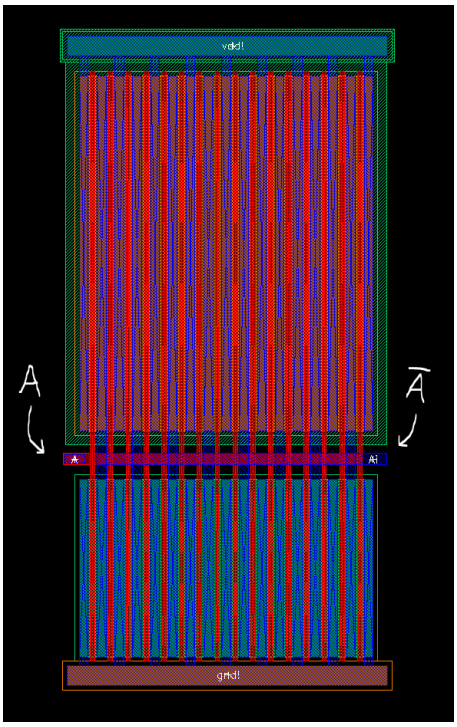
Second Stage: 48u/24u Inverter, Multiplier of 2 (Effectively 8x First Stage)





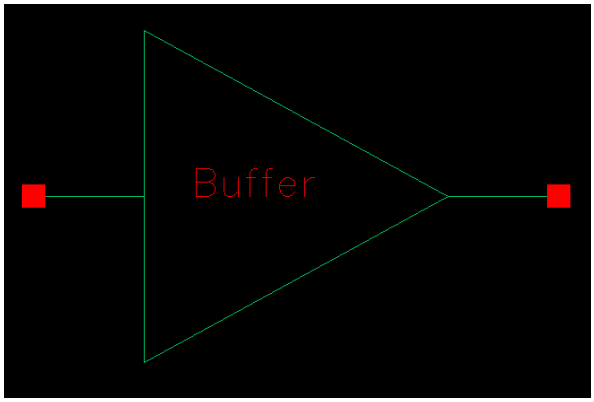
Third Stage: 48u/24u Inverter, Multiplier of 16 (Effectively 64x First Stage)





The layouts shown above for the three stages of the buffer circuit all pass LVS and DRC verification.

Buffer Circuit Symbol View and Calculations



To calculate the number of stages in the buffer, we need to take into consideration the NMOS switch characteristics. The NMOS switch was chosen to have w = 96.0 um and l = 0.60 um with a multiplier of 32 for a final width of 3072 um. The number of stages can be found by

$$N(lnA) = ln(\frac{C_{Load}}{C_{in}})$$

A is the multiplier at each stage, Cload is the input capacitance of the NMOS device, and Cin is the input capacitance of the first inverter in the buffer. We want A to be 8, so that the later stages of the buffer will be able to drive the signal off-chip. We can find the load capacitance by

$$C_{Load} = C'_{ox} * W_n L_n = \frac{2.5\ fF}{\mu m^2} * 3072\ \mu m * 0.6\ \mu m = 4.6\ pF$$

For our first stage (12u/6u inverter),

$$C_{ox,n} = C'_{ox} * W_n L_n = \frac{2.5\ fF}{\mu m^2} * 6\ \mu m * 0.6\ \mu m = 9\ fF$$

$$C_{ox,p} = C'_{ox} * W_p L_p = \frac{2.5\ fF}{\mu m^2} * 12\ \mu m * 0.6\ \mu m = 18\ fF$$

Cin can be found by

$$C_{in} = \frac{3}{2}\left(C_{ox,n} + C_{ox,p}\right) = \frac{3}{2}(9\ fF + 18\ fF) = 40.5\ fF$$

Finally the number of stages need can be calculated by

$$N(ln8) = ln\left(\frac{C_{Load}}{C_{in}}\right) \Longrightarrow N = \frac{1}{2}\left(ln\frac{4.6\ pF}{40.5\ fF}\right) = 2.36$$

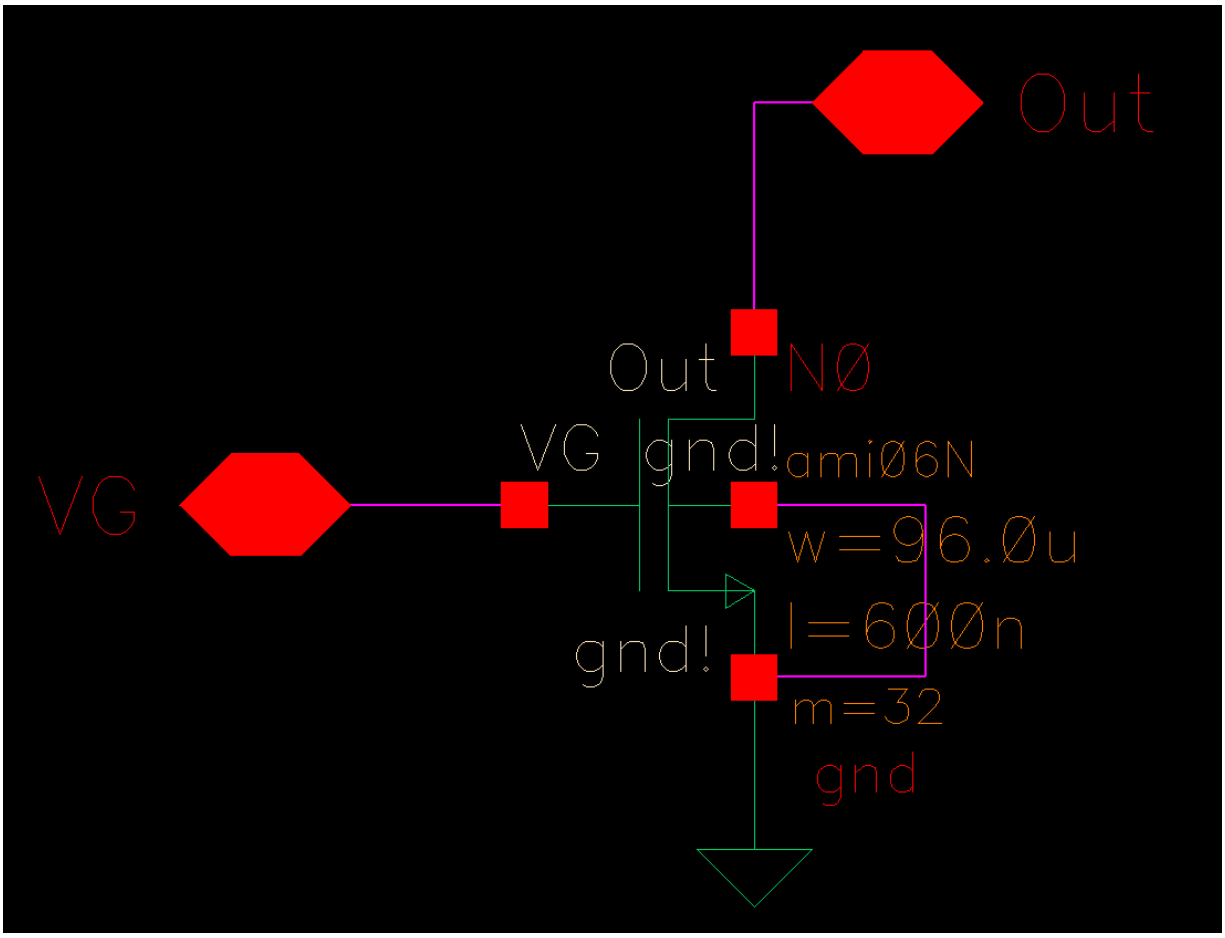
Therefore, rounding up, and with a multiplier of 8, 3 stages should be used.

Part 5: NMOS Device For Switching

As was mentioned previously, the switching NMOS device is the link between the on-chip circuitry and the off-chip components. In order to have a very low resistance connection from the on-chip circuitry to the off-chip components, we need a strong (large W) NMOS device. This is because effective switching resistance is given by

$$R_n = R'_n \frac{L}{W}$$

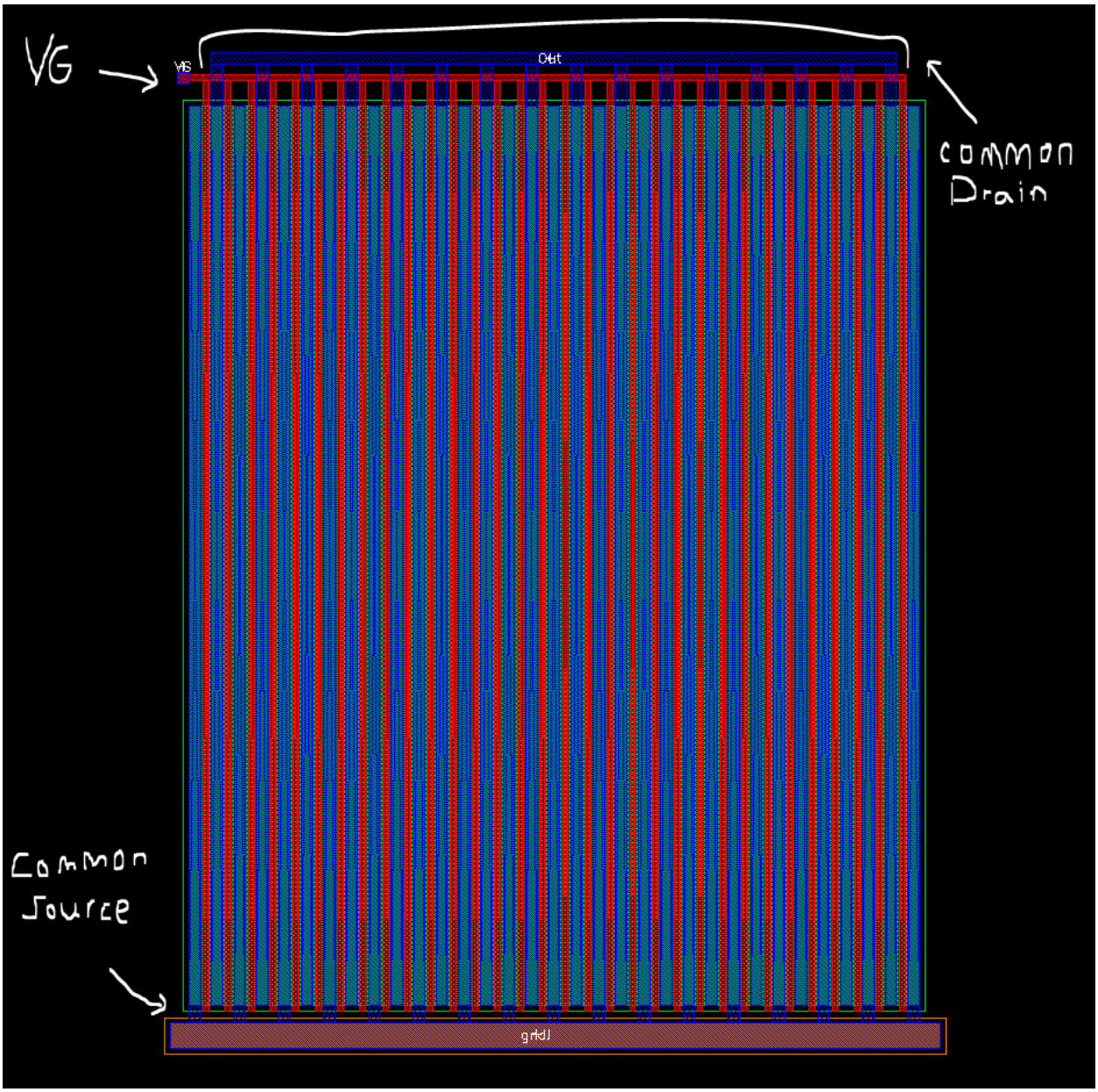
Therefore if W is much larger than L, **Rn** will be very low.



The **VG** input to the gate of the NMOS is the output of the buffer stage. The **Out** pin on the drain of the NMOS is the signal that goes off the chip. When **VG** is high, the switch is closed, and when **VG** is low, the switch is open.

Below is the layout of the NMOS. Though the effective switching resistance is very low due to the large W/L ratio, the layout size is quite large, and so is the resulting capacitance of the device. This is another **design tradeoff.**

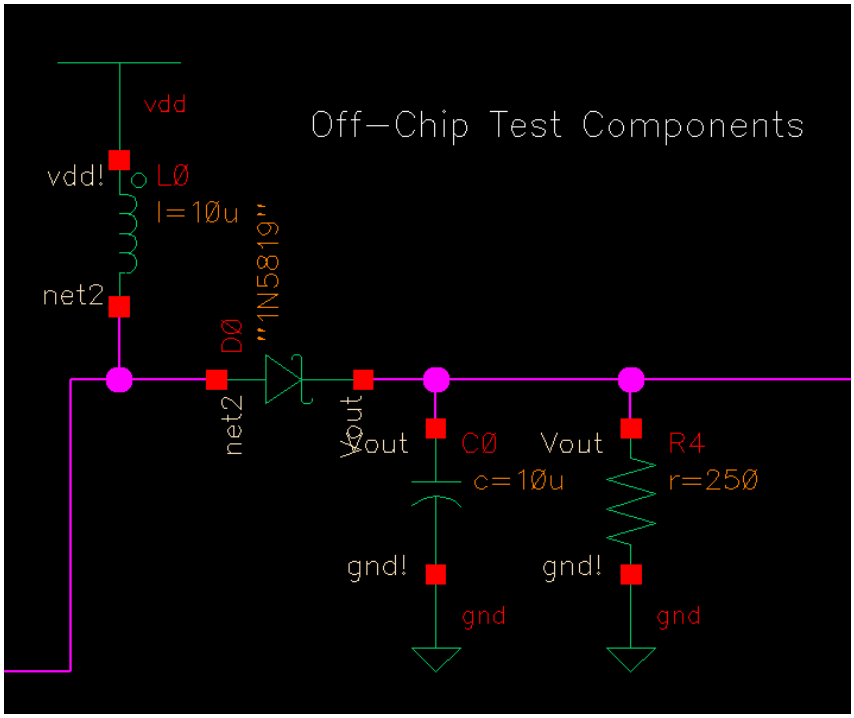
The NMOS below has “32 fingers” or a multiplier of 32, with a width of 96 um, and a length of 0.6 um.



This layout passes both LVS and DRC verifications.

Part 6: Off-Chip Inductor, Diode, Capacitor, Load

The off-chip components need to be selected so that the ripple voltage on the output is minimal. We want to output a constant 5 V DC.



Inductor Connected to VDD

The inductor needs to be able to supply enough current to the output when the NMOS switch opens. The duty cycle (D) of the on-chip signal is 50%, or 0.50. Our load resistance is 250 Ω, and our load current is 20 mA. We can use these values and the following formula from the CMOS textbook to calculate the maximum average current through the inductor.

$$I_L = \frac{V_{OUT}}{(1-D)R} = \frac{I_R}{1-D} = \frac{20\ mA}{0.50} = 40\ mA$$

We can then set the maximum change in the inductor current to 5% of the maximum average current through the inductor, or

$$\Delta i_L = 40\ mA * 0.05 = 2\ mA$$

Finally, we can solve for the appropriate inductor size in terms of maximum change in inductor current by

$$L = \frac{V_{OUT} * D * (1-D)}{f * \Delta i_L} = \frac{5\ V * 0.50 * 0.50}{5.05\ MHz * 2\ mA} = 124\ \mu H$$

It is important to note that these equations assume continuous current flow through the inductor. The above value for the inductor is too high because our inductor is not always conducting current. The value was adjusted according to ripple voltage, and made smaller until the ripple voltage on the output was less than 25 mV at a final inductance of 10 µH.

Schottky Diode

The Schottky diode has a low built-in potential. We want the drain of the NMOS switch at a potential close to Vout ideally, and the Schottky diode drop is only between 200-300 mV. The Schottky diode is in place to prevent current from flowing back to the drain of the NMOS switch from the output node.

Capacitor

Our capacitor needs to be able to supply charge to the load for a time long enough that the output voltage will not fall too far before the inductor starts charging it again. The minimum capacitance can be calculated using the duty cycle, load resistance, frequency, power supply voltage, and ripple voltage (we want a small ripple voltage, less than 10mV), by

$$C_{min} = \frac{D}{R * f * (\Delta V_{OUT}/V_{OUT})} = \frac{0.50}{250\ \Omega * 5.05\ MHz * (0.010/5)} = 0.2\ \mu F$$

Simulating with this 0.2 uF capacitor to begin with left me with large ripples in my output. I concluded that my ripple voltage would decrease if my capacitor were bigger because the bigger capacitor takes longer to discharge and would be able to power the load longer. Editing my capacitor until my ripple was minimal led me to a final capacitance of 10 uF.

Resistor Modeling Load

The load resistor can vary in different simulations to model loads that draw smaller or larger amounts of current. We want our circuit to be able to supply 5 V to loads that draw up to 20 mA of current.

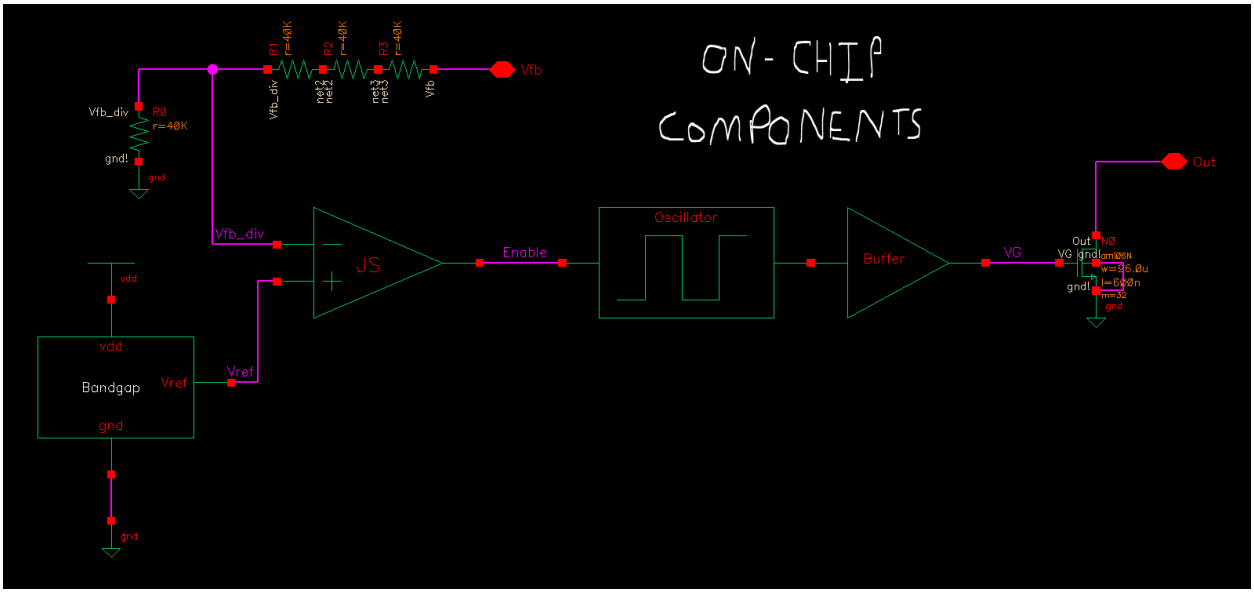
$$R = \frac{V}{I} = \frac{5\ V}{20\ mA} = 250\ \Omega$$

Another simulation was run modeling a load that pulls only 5 mA. The load resistor can be modeled by

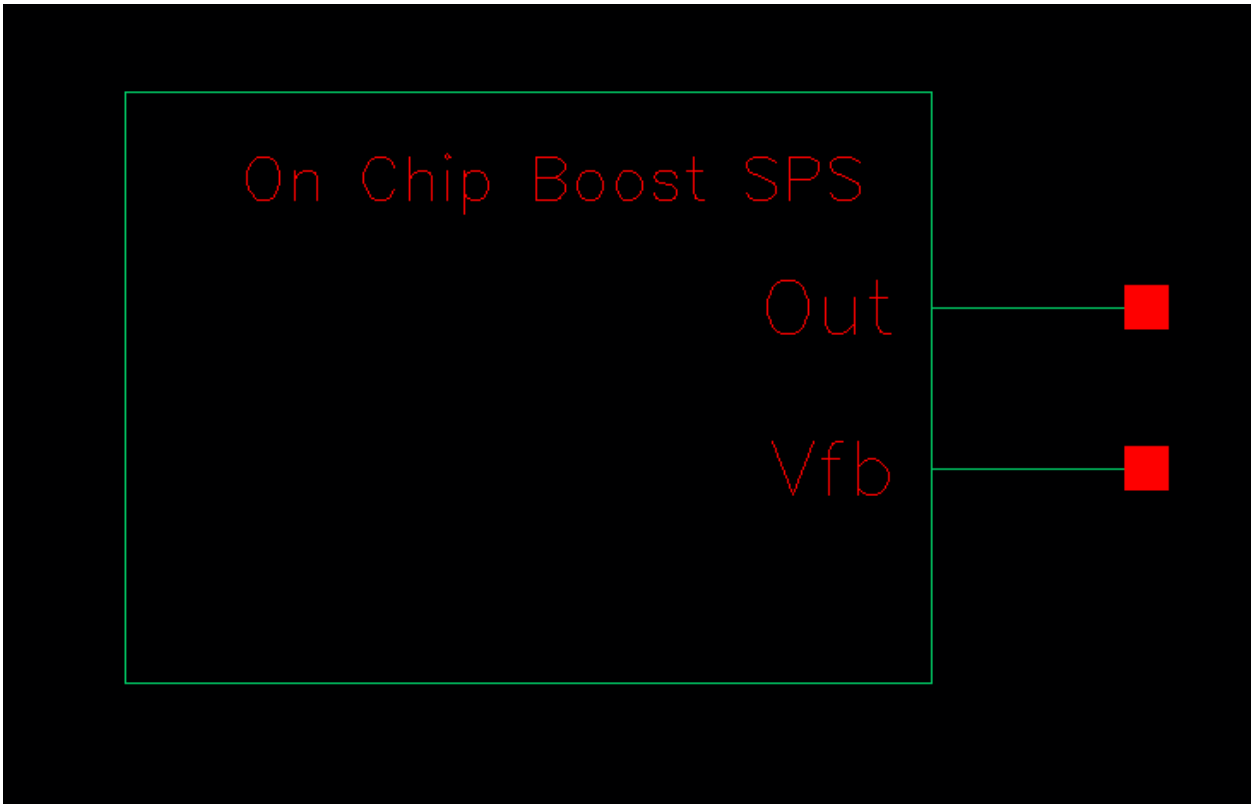
$$R = \frac{V}{I} = \frac{5\ V}{5\ mA} = 1\ k\Omega$$

Full Boost SPS

Below is the schematic of the on-chip boost SPS. Symbols for the oscillator, buffer, bandgap and comparator circuits were instantiated to keep the schematic clean.

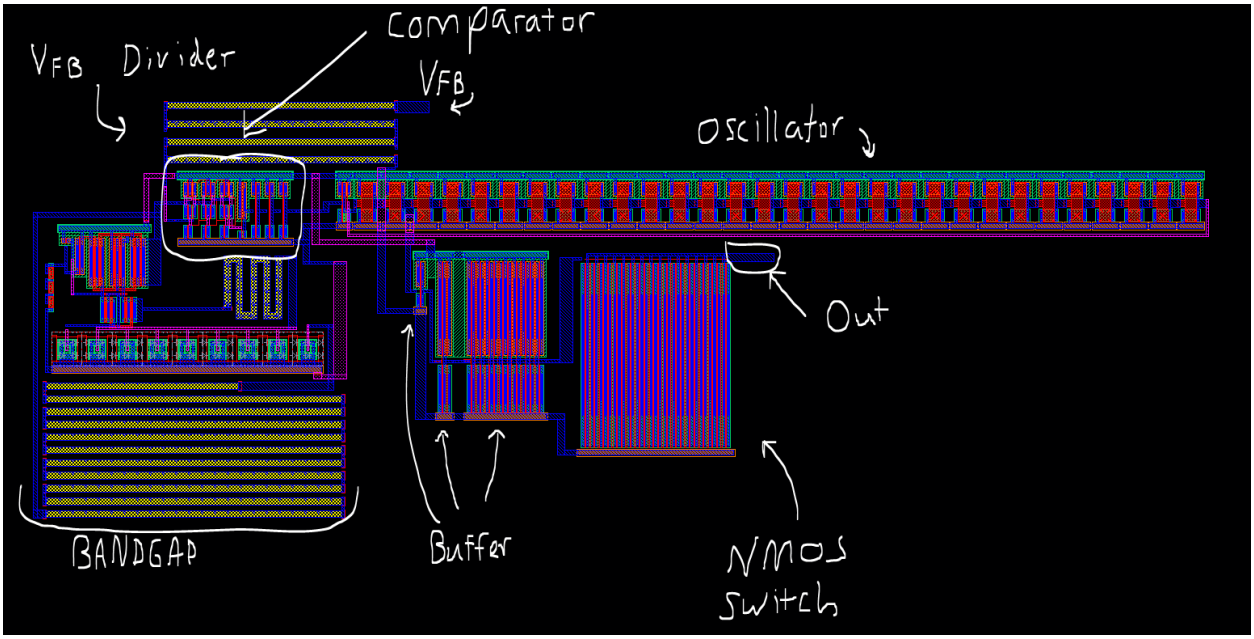


The schematic above is represented by the symbol view below of the full boost SPS.

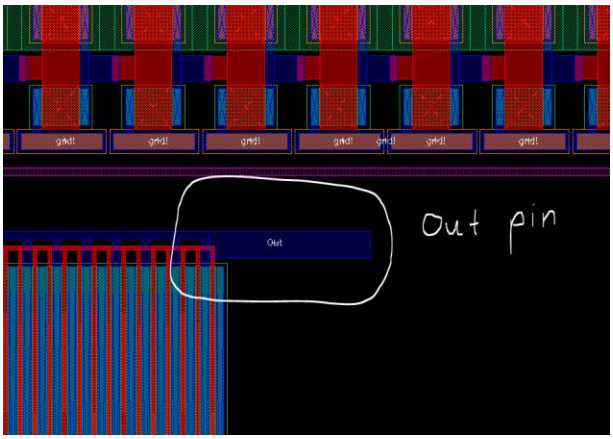


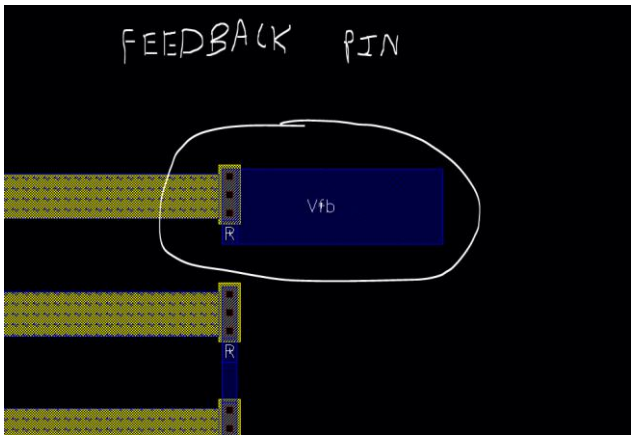
Layout View of Boost SPS

Below is the full layout of the on-chip circuitry.



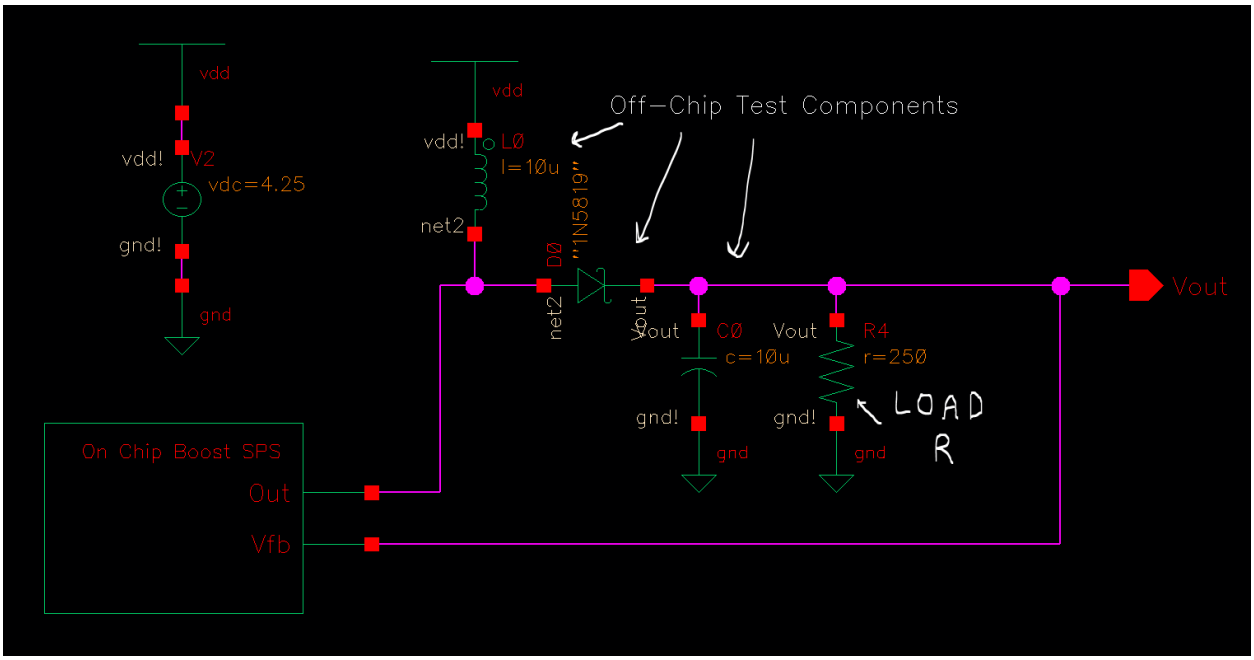
The on-chip circuitry has only two pins aside from vdd! and gnd!; **Out**, the drain of the NMOS switch, and **Vfb,** the pin that takes in **Vout** to the divider. These pins are shown below.

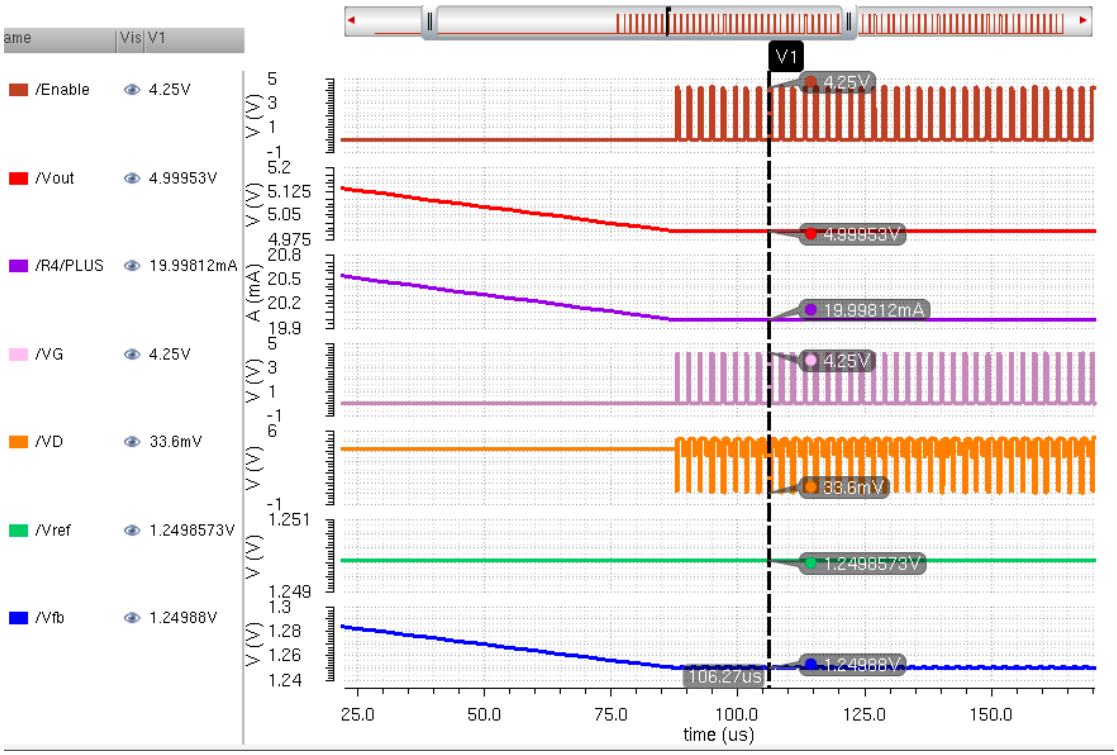




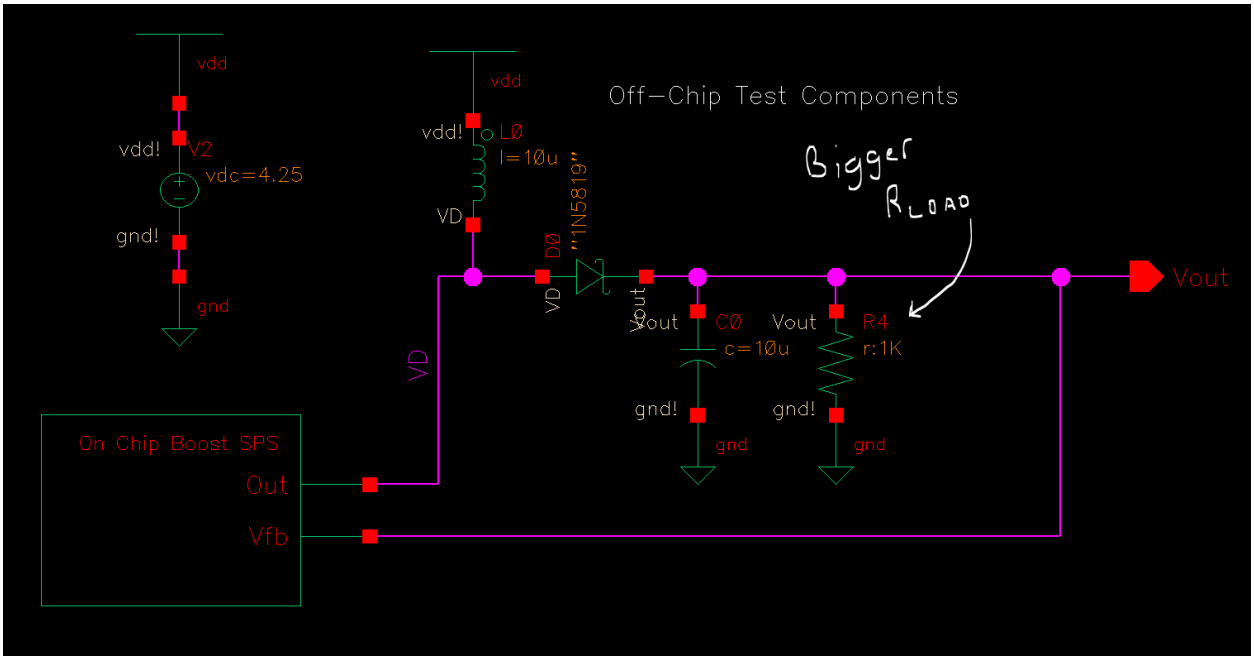
The above layout passes both LVS and DRC verification.

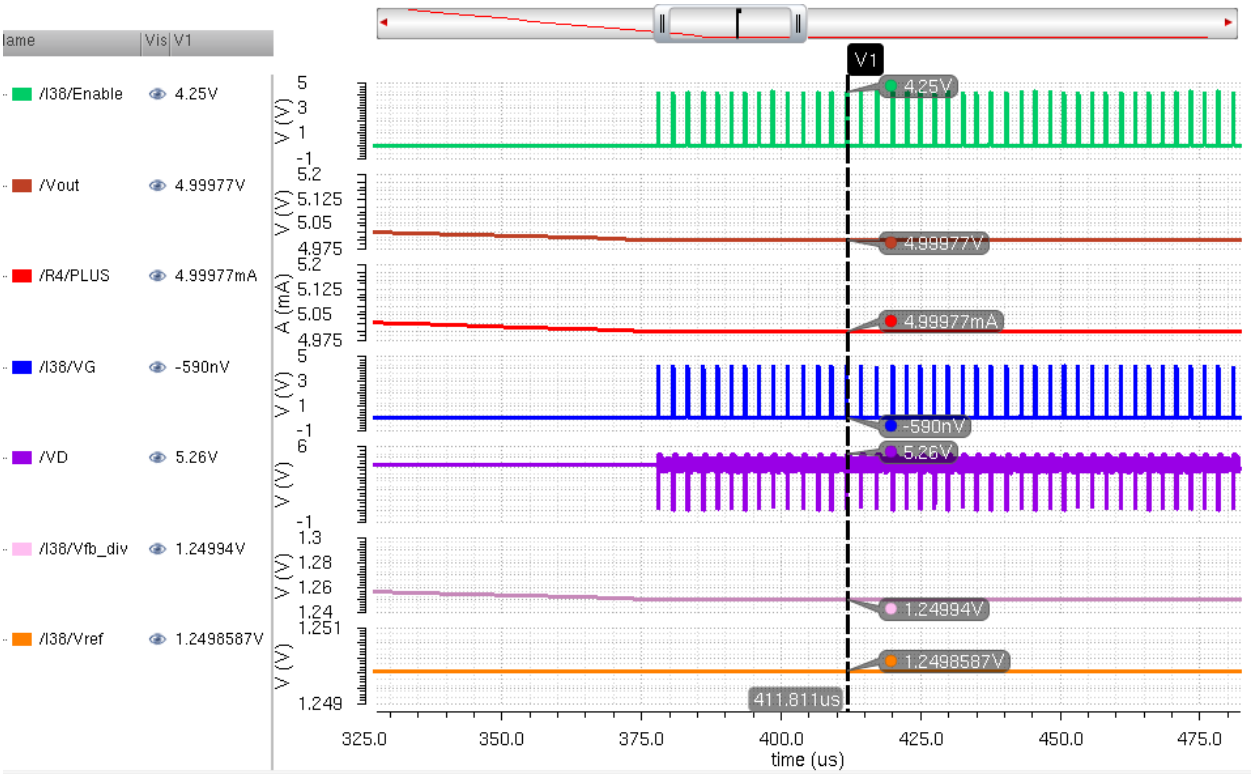
Simulations and Operation





We see in the above simulation that node R4/PLUS, the load current, is roughly 20 mA in steady state. We also see that **Enable** oscillates, as it should, as **Vout** ripples very slightly. This shows that the comparator is doing its job.

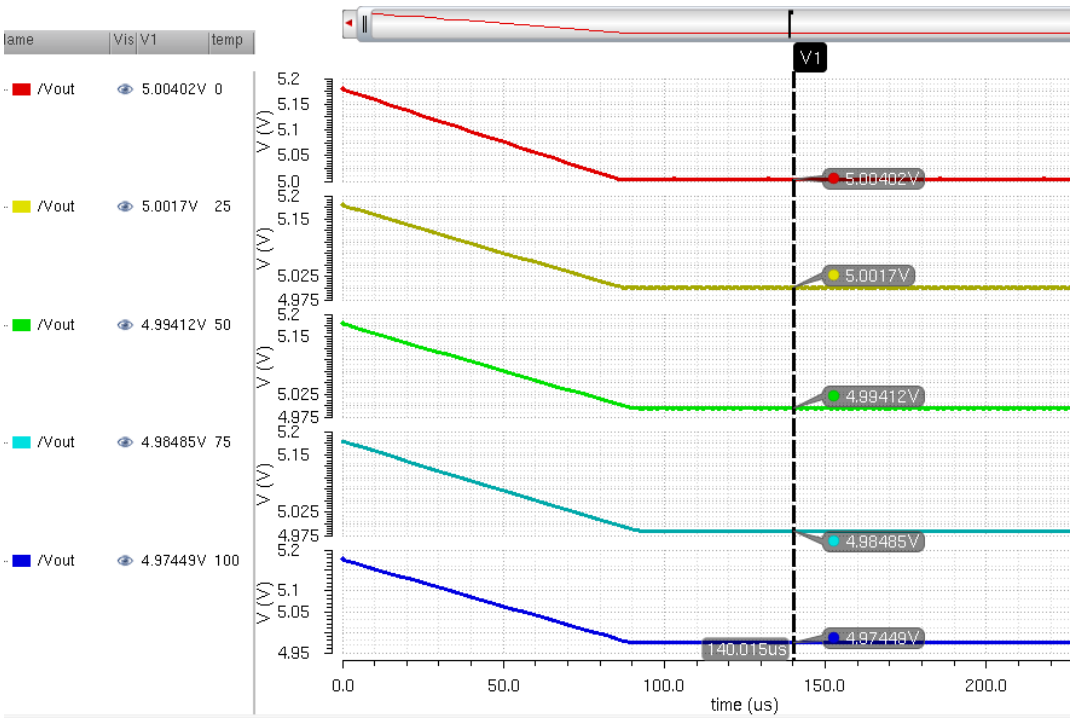




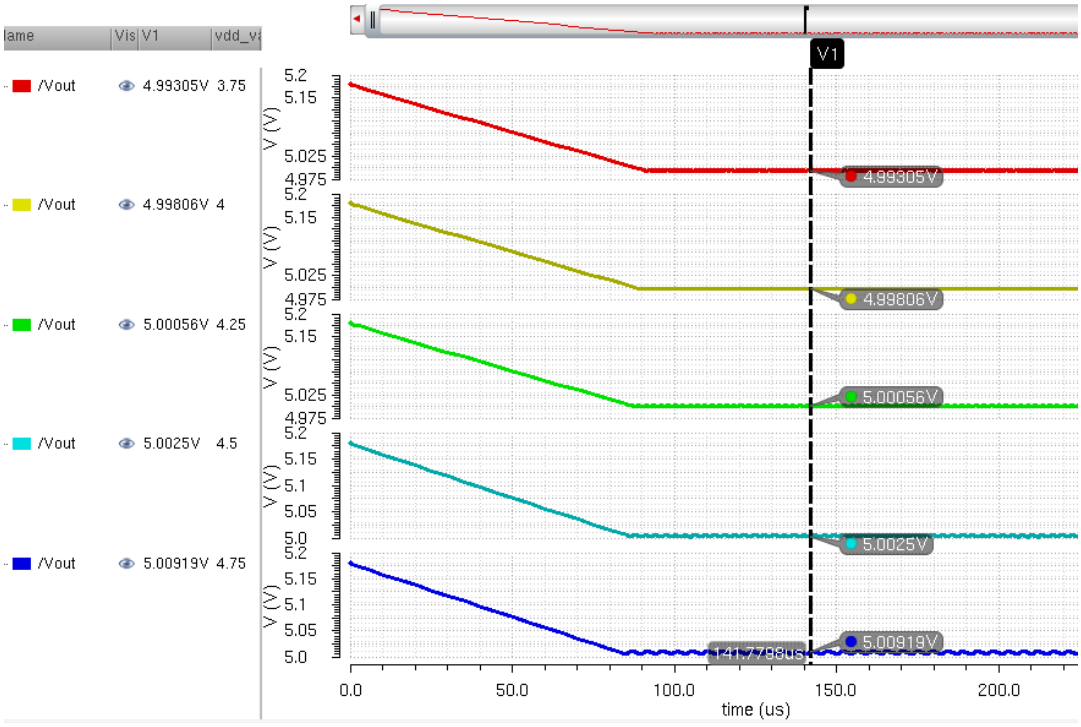
Similar to the previous simulation, but for load current of 5 mA, we see **Enable** oscillating to keep **Vout** right around 5 V.

Parametric Analyses For Varying Temperature, Power Supply Voltage

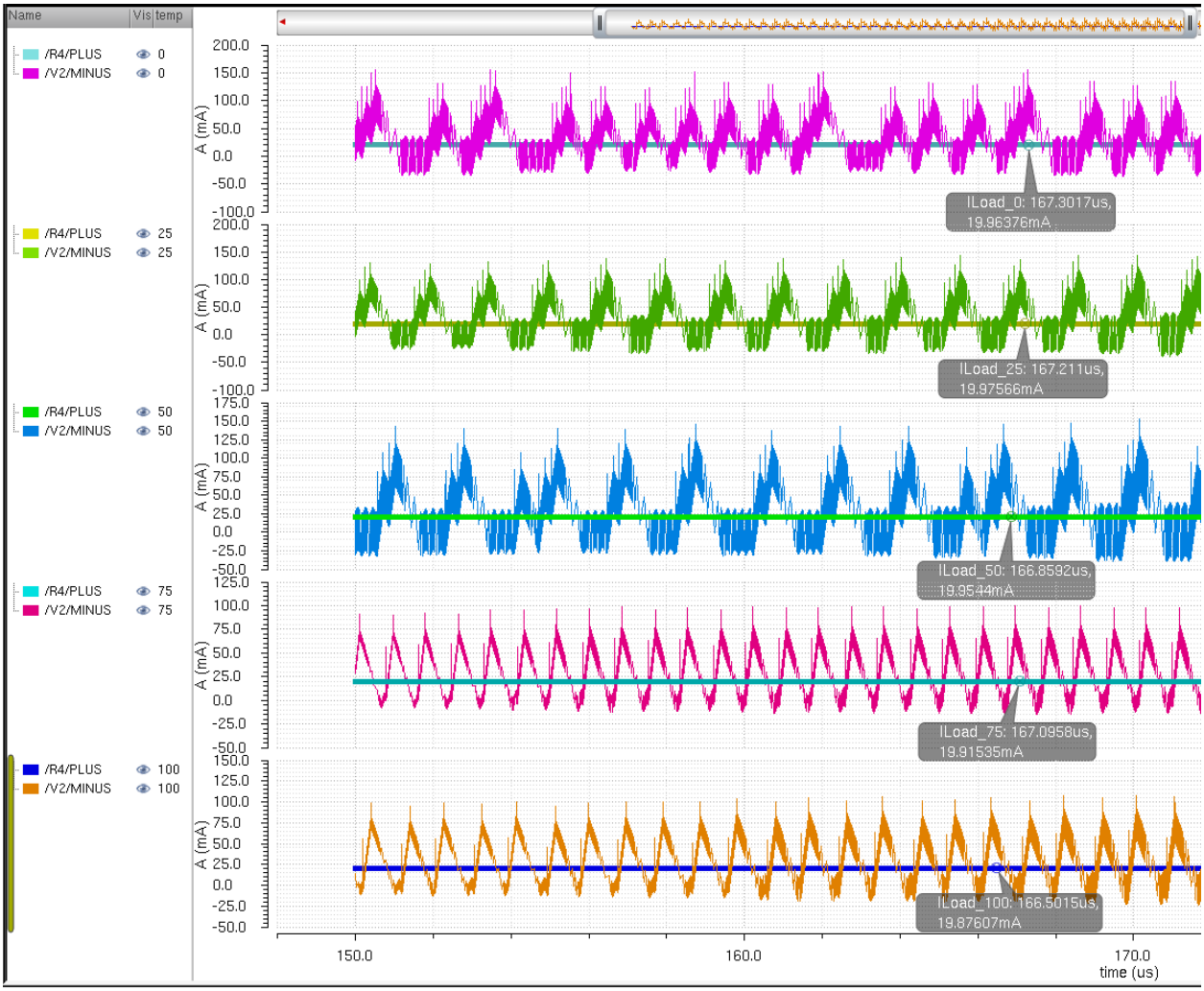
Varying Temperature Simulations



Varying VDD



Power Supply and Load Currents for Varying Temperatures (VDD = 3.75 V)



Efficiency of the circuit can be calculated by

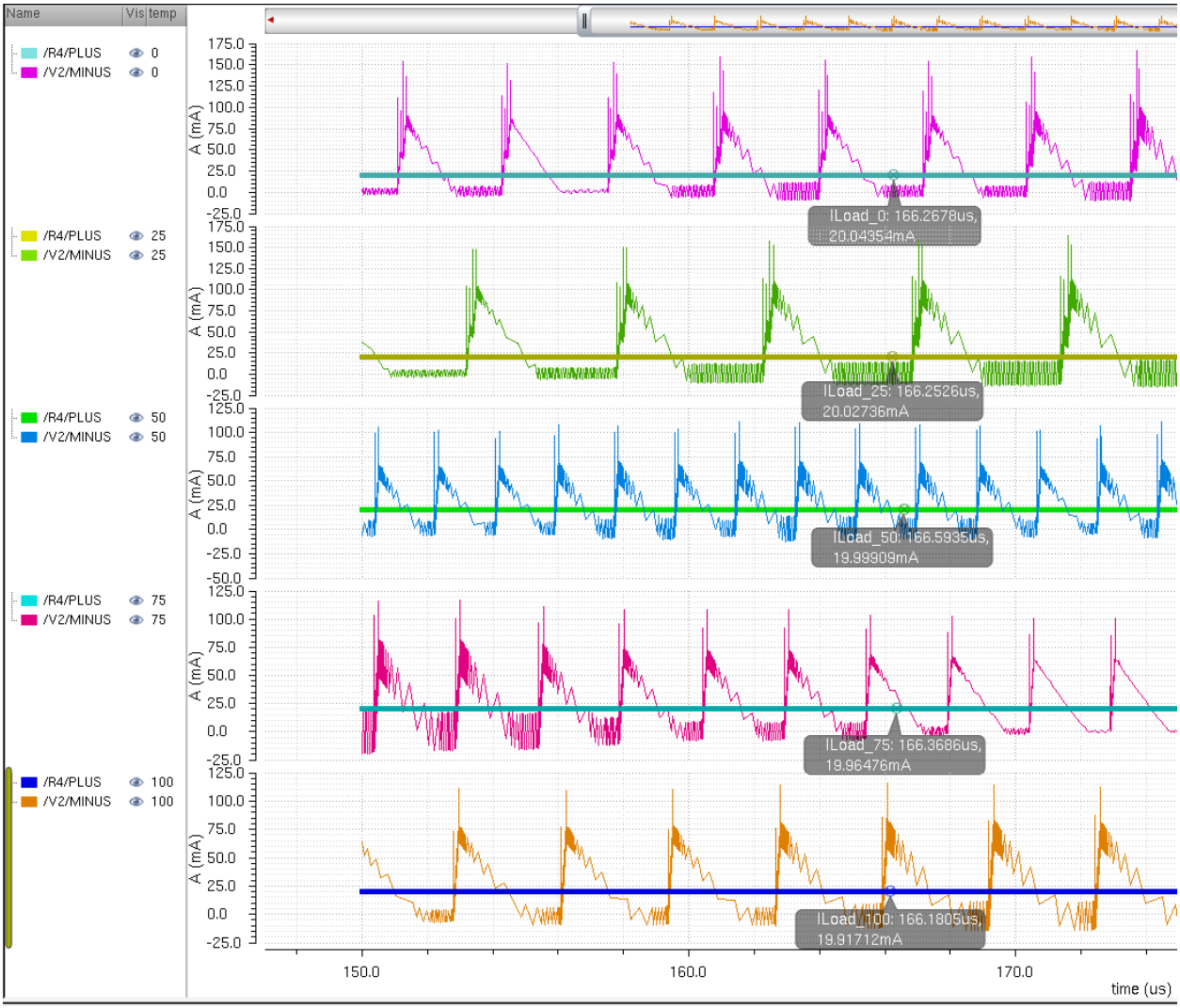
$$E = \frac{V_{OUT} * I_{Load}}{V_{DD} * (AVG(I(V_{DD})))}$$

Using the calculator in Cadence to find the load current and the average power supply voltage, the following results were obtained.

Currents and Efficiency for Varying Temperature (VDD = 3.75 V)

Temp. (ºC)	Vout (V)	Iload (mA)	I(vdd) (mA) Average	Efficiency
0	5.004	19.963	29.86	0.893
25	5.002	19.976	29.31	0.910
50	4.994	19.954	28.88	0.923
75	4.985	19.915	28.64	0.931
100	4.974	19.876	28.80	0.926

Power Supply and Load Currents for Varying Temperatures (VDD = 4.75 V)

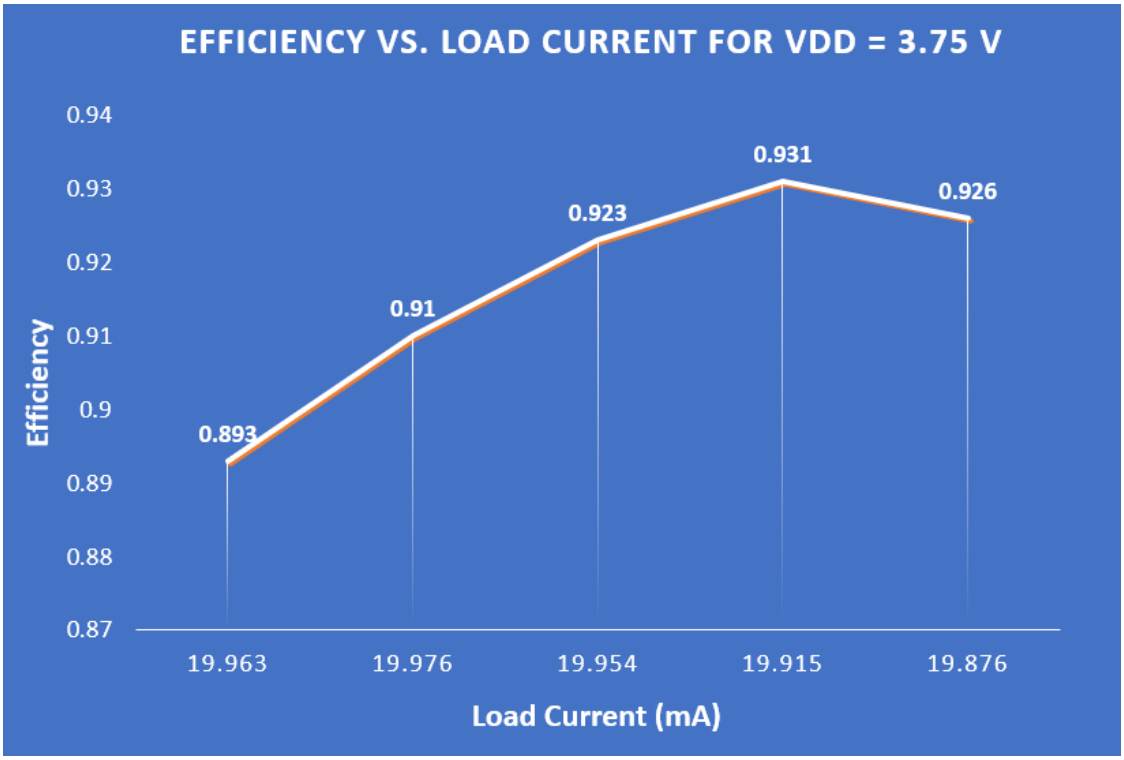


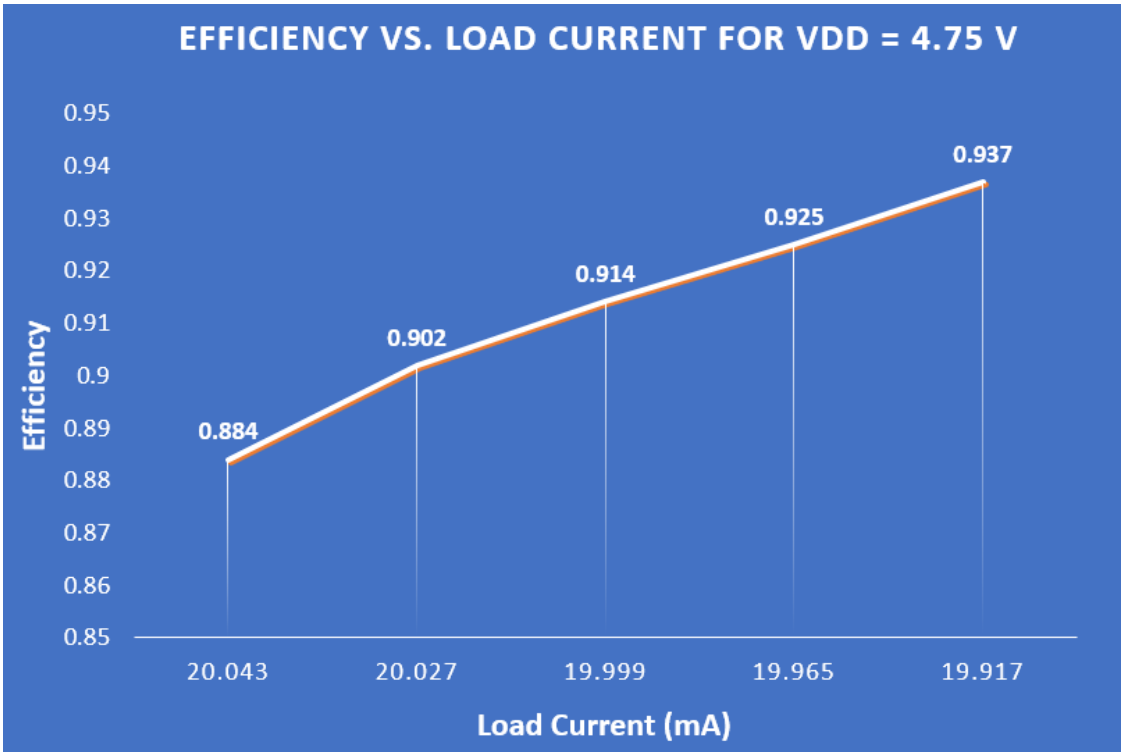
Using the calculator in Cadence to find the load current and the average power supply voltage, the following results were obtained.

Currents and Efficiency for Varying Temperature (VDD = 4.75 V)

Temp. (°C)	Vout (V)	Iload (mA)	I(vdd) (mA) Average	Efficiency
0	5.004	20.043	23.81	0.884
25	5.002	20.027	23.34	0.902
50	4.994	19.999	23.03	0.914
75	4.985	19.965	22.77	0.925
100	4.974	19.917	22.47	0.937

Plots for Efficiency vs. Load Current





Layout Pin Diagram