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EE 493: Independent Study

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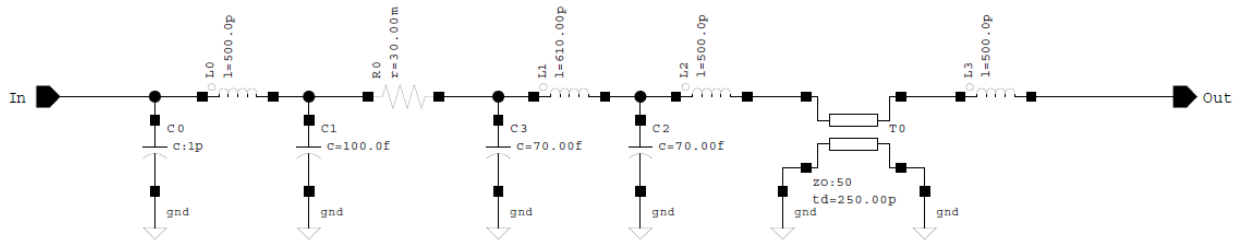
1.5 GHz RF Amplifier for Optical Application

The central topic of this study was research in the design of CMOS radio-frequency integrated circuits. Research was conducted on a number of subtopics within CMOS radio-frequency integrated circuit design, and integrated circuit design in general. Subtopics include schematic design and simulation using the TowerJazz PDK in Cadence, research regarding on-chip resistors, capacitors, and inductors in RF applications, and low noise amplifier (LNA) design. The final product of the study, the design of a 1.5 GHz RF amplifier, was made possible as a result of the application of new knowledge in each of these subtopics. A summary of the performance of the amplifier is given below.

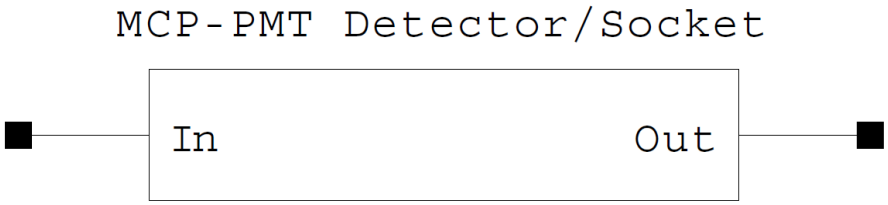
Summary of Amplifier Performance			
TIA Gain Peak (dB)	88.6 dB	**TIA Gain Peak (Ω)**	27.06 kΩ
Low Frequency Gain (dB)	49.0 dB	**Low Frequency Gain (Ω)**	282 Ω
Gain at 1.5 GHz (dB)	54.5 dB	**Gain at 1.5 GHz (Ω)**	532.5 Ω
TIA Power Consumption	3.36 mW	**TIA Current Consumption**	1.87 mA
Comparator Power Consumption	12.54 mW	**Comparator Current Consumption**	6.97 mA
Total Power Consumption	**15.9 mW**	**Total Current Consumption**	8.84 mA

Amplifier Input (MCP-PMT Detector and Socket)

The amplifier is to be used for applications in photonics and optics, in which the input is a current pulse from a micro-channel plate detector (MCP). The MCP intensifies the effect of exposure to photons by multiplying electrons, and the result is a current pulse. In Cadence, the MCP-PMT Detector and Socket circuitry were implemented with reference to a model designed by Rich Hare from the NASA Langley Research Center. The model schematic can be seen below, along with its symbol.



For all simulations, the input to the MCP-PMT Detector and Socket is modeled by a current pulse source, pulsing from 0 to 50µA. The rise time and fall time of the pulse was set to 250ps, and the "on time" of the pulse, or time that the current remains at 50µA, is 75ps. The total pulse width is 575ps. All values were taken from Rich Hare's model pulse source. A symbol for the model was created and is seen below.

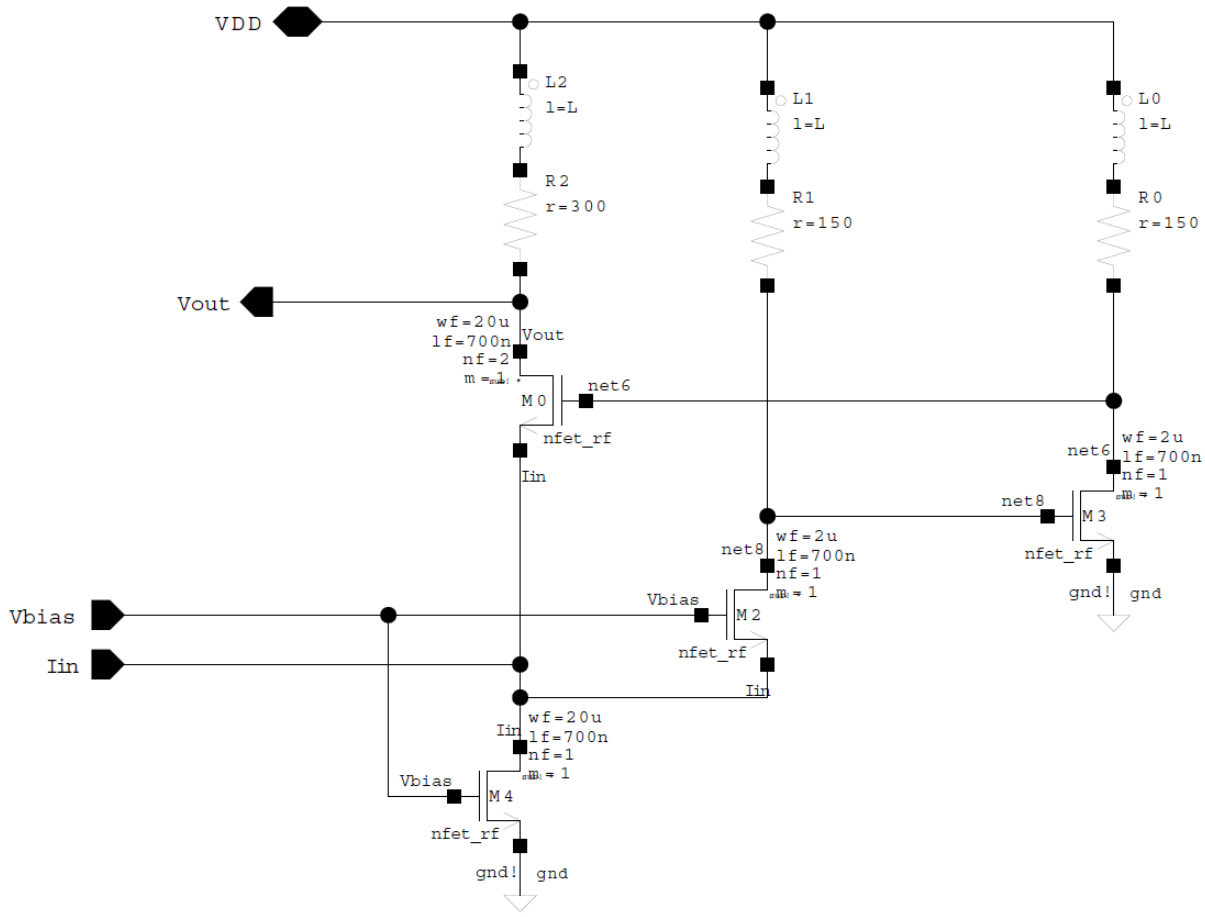


We can observe from the schematic of the model that the transmission line instance is characterized by an impedance of 50Ω. This means that for optimal performance and to avoid reflection, the input impedance of the TIA should be 50Ω as well. Obtaining a 50Ω input impedance while maintaining significant gain was an obstacle that was not overcome in this design. Input impedance of the final TIA was over 100Ω, which causes reflection issues when the current input pulses high. These issues will be seen in simulations to come.

The MCP-PMT model is important to consider, since it models real-life parasitics which can not be avoided during testing. Modeling these parasitics and countering them in design is very important. In the simulations to come, we will examine the output of the amplifier both with and without the MCP-PMT model connected, and compare and contrast the results.

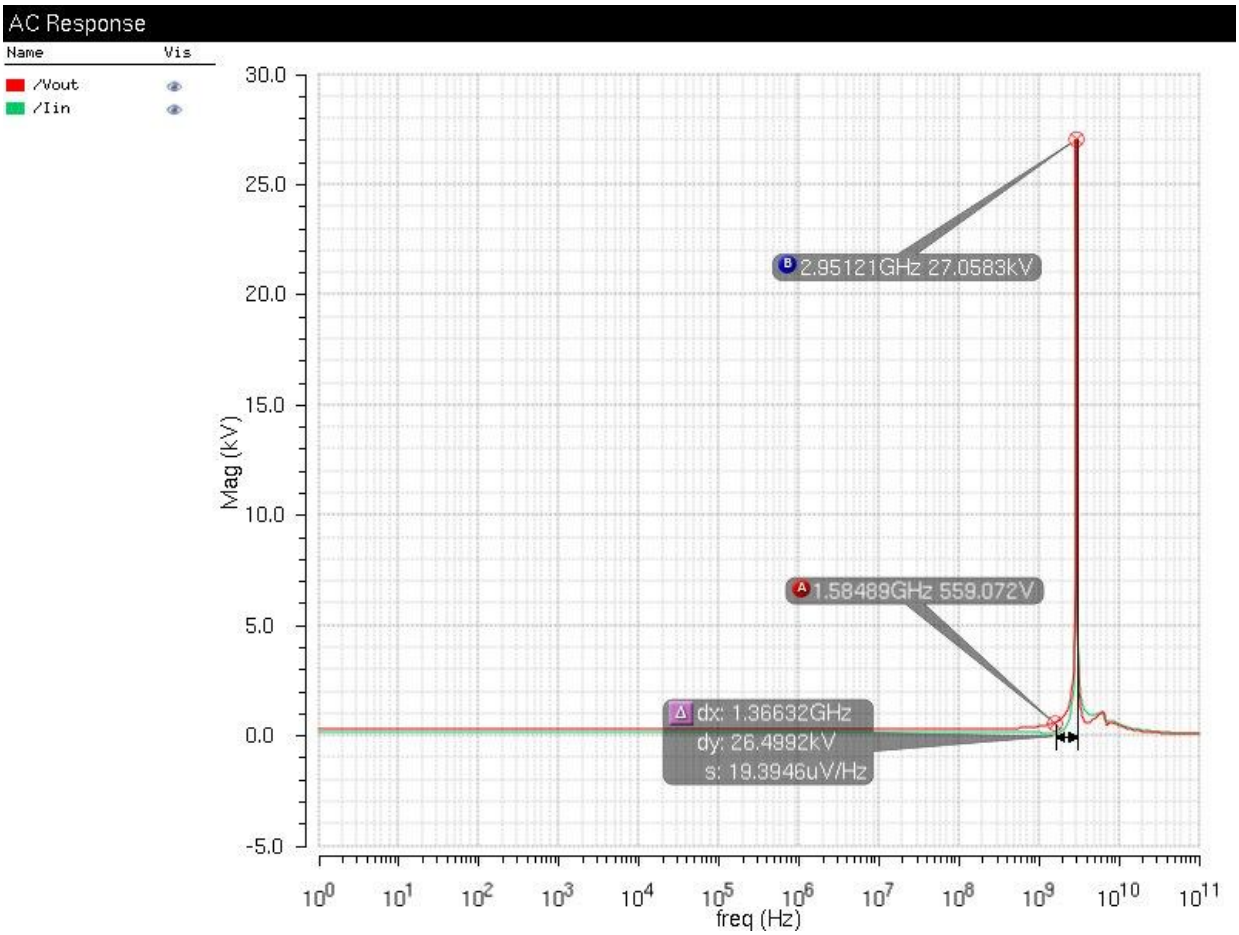
First Stage: RF Transimpedance Amplifier

The first stage of the amplifier, which is AC coupled to the input, is a single-ended common-gate feedforward transimpedance amplifier. The topology was pulled from the *IEEE Journal of Solid-State Circuits*, Volume 39. The original design was for a low-power 20-GHz TIA, designed in a process with minimum length of 80nm, and a VDD of 1V. For the TowerJazz process, the minimum length is 180nm, and VDD is 1.8V. The design was modified to perform at 1.5 GHz for applications with Freedom Photonics projects. The schematic of the TIA can be found below.



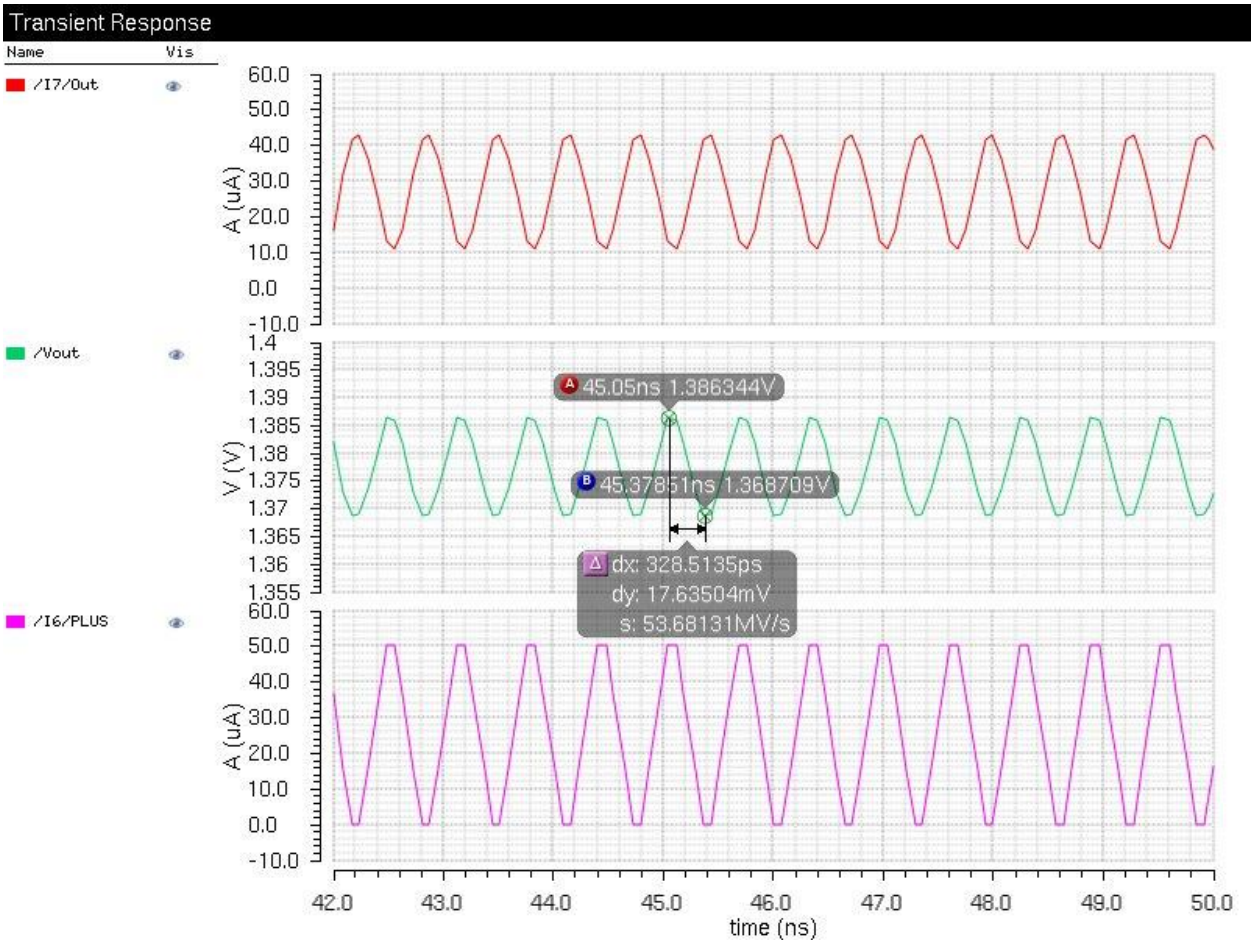
In order to shift the gain peak down in frequency, the inductances of L0, L1, and L2 were set to 40nH, and the maximum length of RF MOSFETS were used (700nm). R0, R1, and R2 model series resistances of the inductors. Though not pictured above, the bias voltages for MOSFETs M2 and M4 were set equal and valued at 1V. For comparison, simulations were ran with the input current pulse source connected directly to the TIA input, and also with the input current pulse source connected to the MCP-PMT model, and the output of the MCP-PMT model connected to the input of the amplifier.

Here, we can observe the AC response of the TIA. Notice that the gain peak of 27k occurs at a frequency of 2.95 GHz. Since we are operating at 1.5 GHz, another point was plotted to show that the gain at our operating frequency is roughly 560. Hand calculations on the page to follow from the transient response reinforce that this is the gain at our operating frequency.



In this RF transimpedance amplifier, the inductors, L0, L1, and L2 from the schematic above, play a large role in determining the gain and the center frequency. From gain equations for the devices in the TIA found in the article from which the topology was pulled, we see that increasing the inductances decreases the gain of the output device. Since the gain of the output device is directly proportional to the gain of the entire TIA, increasing inductance decreases the gain of the circuit overall. However, it was also determined that increasing inductance shifts the center frequency of the gain peak downward. This gain-frequency tradeoff was a very important design consideration. In order to get enough gain to operate at 1.56 GHz, it was absolutely necessary to use larger inductors (40nH). Anything larger than this would be unreasonably large on a chip in the TowerJazz process, and would kill the gain even more. Using values of 40nH for the inductors leaves us with an output voltage of roughly 20mV from the TIA, and was determined to be the best size for this application.

The simulation below shows the transient response of the TIA with the current source connected to the input of the MCP-PMT model, and the output of the MCP-PMT model connected to the input of the TIA. Note that the current into the MCP swings from 0 to 50µA, while the current into the TIA only swings from 10µA to 40µA. This decrease in current is a result of reflection from the transmission line, which does not occur when the MCP model is omitted.



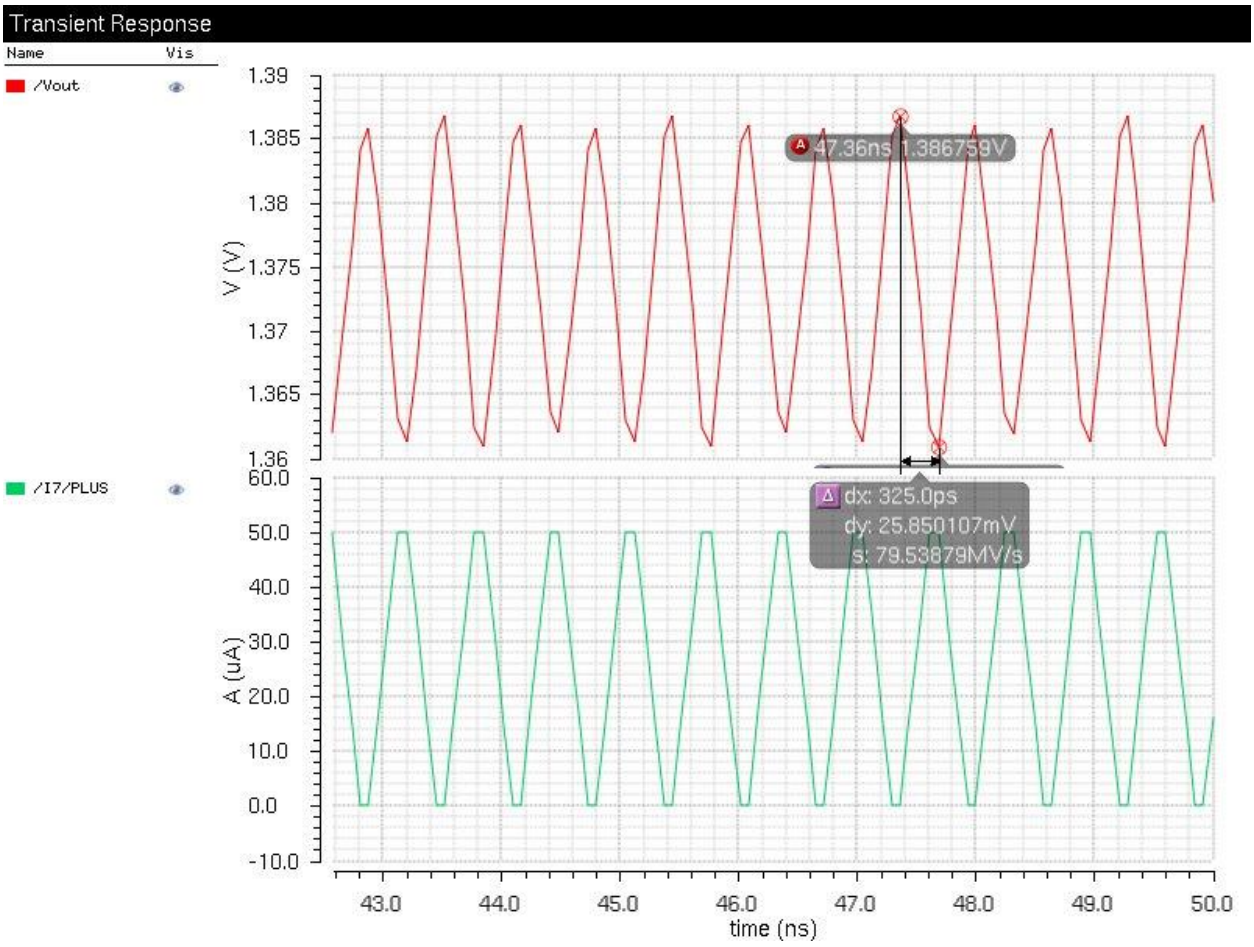
We can also take note of the output voltage, which has a peak-to-peak value of 17.6mV. With an output voltage swinging at 17.6mVpp and an input current swinging at 30µApp, we can calculate the gain of the TIA at a frequency of 1.56 GHz to be as follows.

$$A_{TIA} = \frac{v_{out}}{i_{in}} = \frac{17.6mV}{30\mu A} = 586.6\Omega$$

$$A_{TIA} = 586.6\Omega$$

One major obstacle in designing the TIA was the difficulty in trying to shift the gain peak down in frequency. The only options were increasing load capacitance and increasing inductance values, both of which massively add to layout area, and still did not quite shift the gain peak down to 1.5GHz. This lack of gain will be made up for in the pre-amplifier stage of the comparator.

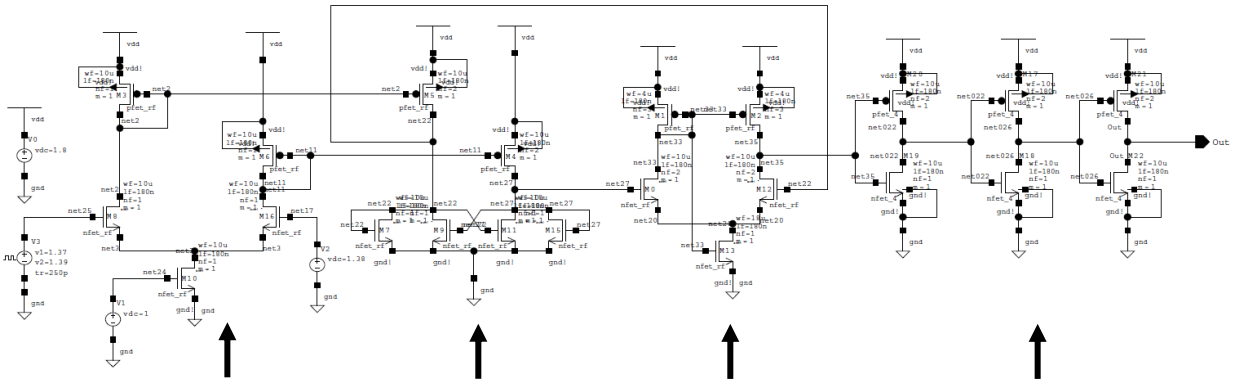
Here we can observe the results of the transient simulation for the TIA with no MCP model connected. Since the input to the TIA now swings from 0 to 50µA, the output voltage now swings 25.8mV.



As was mentioned previously, matching the input impedance of the TIA to the impedance of the transmission line in the model was an obstacle which was not overcome during design. Better impedance matching between the model and the TIA input would lead to cleaner signals with larger peak to peak values. Larger peak to peak values in the TIA stage would mean that the gains of the devices in the comparator stage could be lowered to conserve power. The next stage to be discussed is the comparator stage.

Second Stage: CMOS Comparator

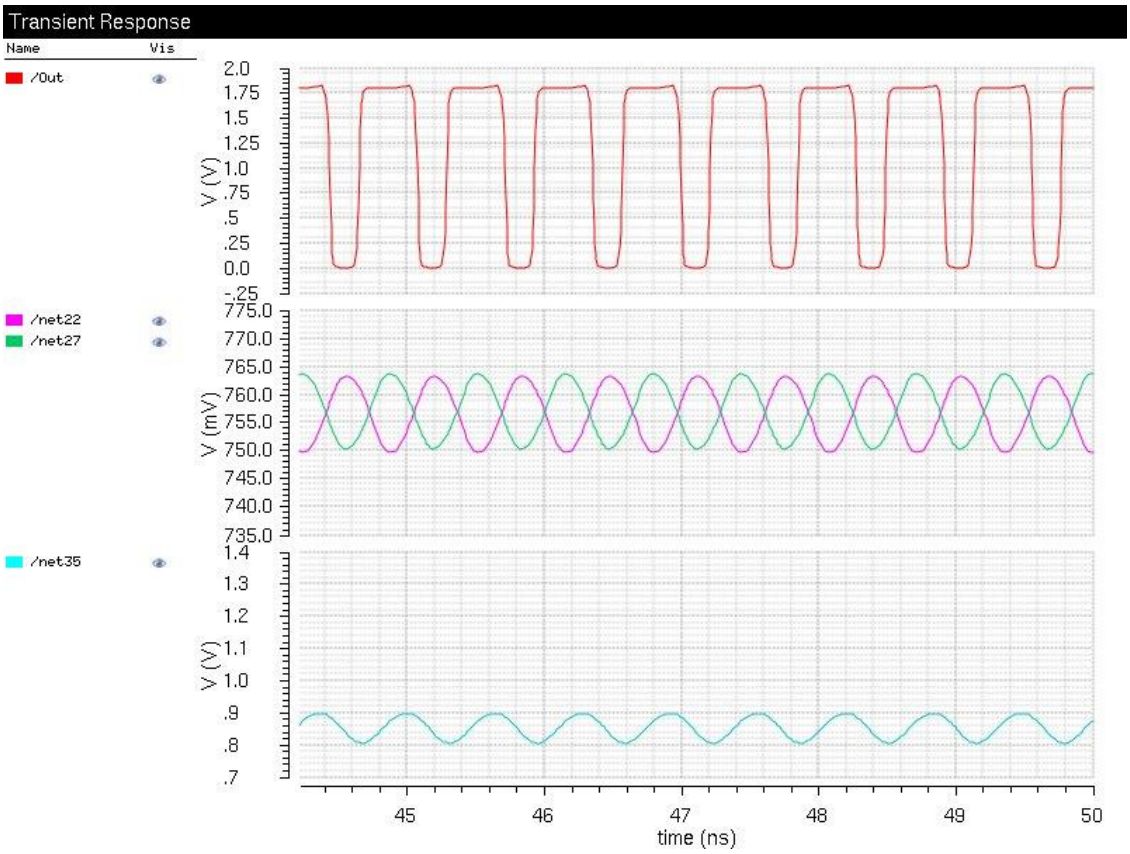
The second stage of the amplifier is the CMOS comparator to convert the output of the TIA stage into digital logic, which swings between VDD (1.8V) and ground (0V). The topology for the comparator was pulled from figure 27.8 of the *CMOS: Circuit Design, Layout, and Simulation,* Fourth Edition, and consists of three substages: a pre-amplifier, a decision circuit, and an output buffer. The schematic can be seen below.



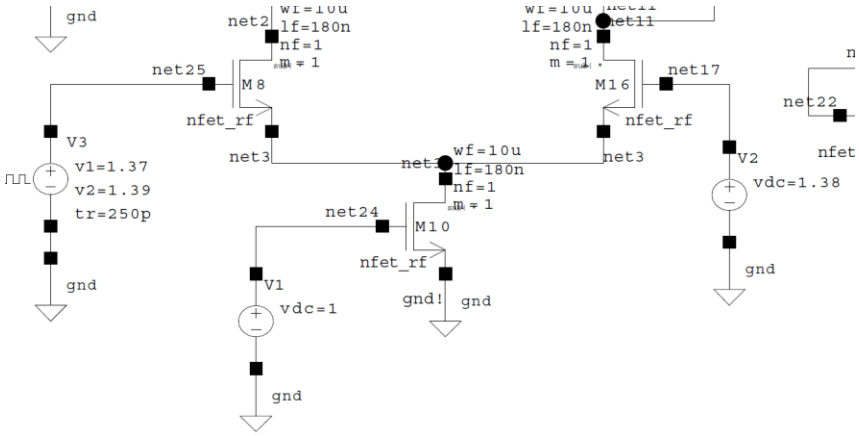
The first differential amplifier acts as a pre-amplifier for the decision circuit, amplifying the difference between the output of the TIA and the DC value which the output of the TIA swings around. The pre-amplifier stage is important because it improves the overall sensitivity of the comparator. Having a pre-amplifier stage with high gain is important and allows the decision circuit to output the correct value for very small differences in input signals. This is exactly what we need, since the output voltage of our TIA is under 20 mV. The output buffer stage consists of a differential amplifier, followed by three cascaded inverters, which allow the final signal to swing between VDD (1.8V) and ground (0V).

In the design of the comparator, several considerations needed to be thoroughly examined. To ensure high speed, the lengths of all devices were set to minimum L. Though the inverters were designed using normal MOSFETs and not RF MOSFETs in the TowerJazz process, their length is still 180nm. It was also important to be sure that the first stage of the comparator had no high impedance nodes other than the inputs to ensure high speed operation. Also, a tail device could be added to the decision circuit to shift the output of the decision circuit up, but since the DC value of the output of the decision circuit was already reasonably high, the tail device was removed.

In the simulation below, we can see the output of the comparator swings between 1.8V and 0V. Nets 22 and 27 represent the outputs of the decision circuit, and therefore, the inputs to the output buffer diff-amp. Net 35 is the output of the final diff-amp, and the input to the cascaded inverters. The switching point of the inverters was manipulated such that the output of the final diff-amp would swing around the switching point voltage.

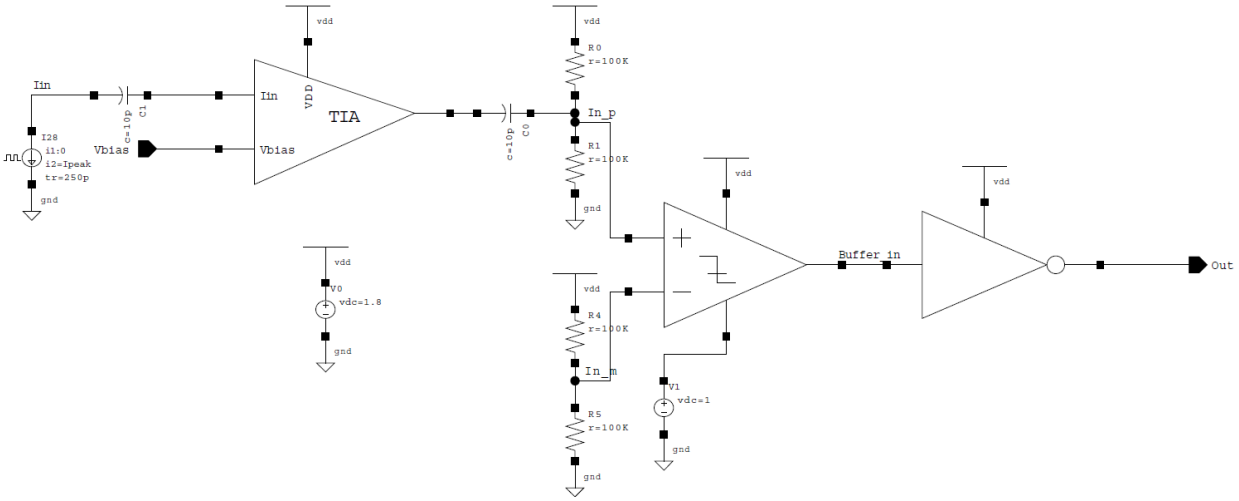


The first input to the comparator was modeled by a 20mVpp pulse voltage source with a relatively slow rise/fall time to model the output of the TIA for simulations. The second input to the comparator was the common mode voltage of the first input pulse source.

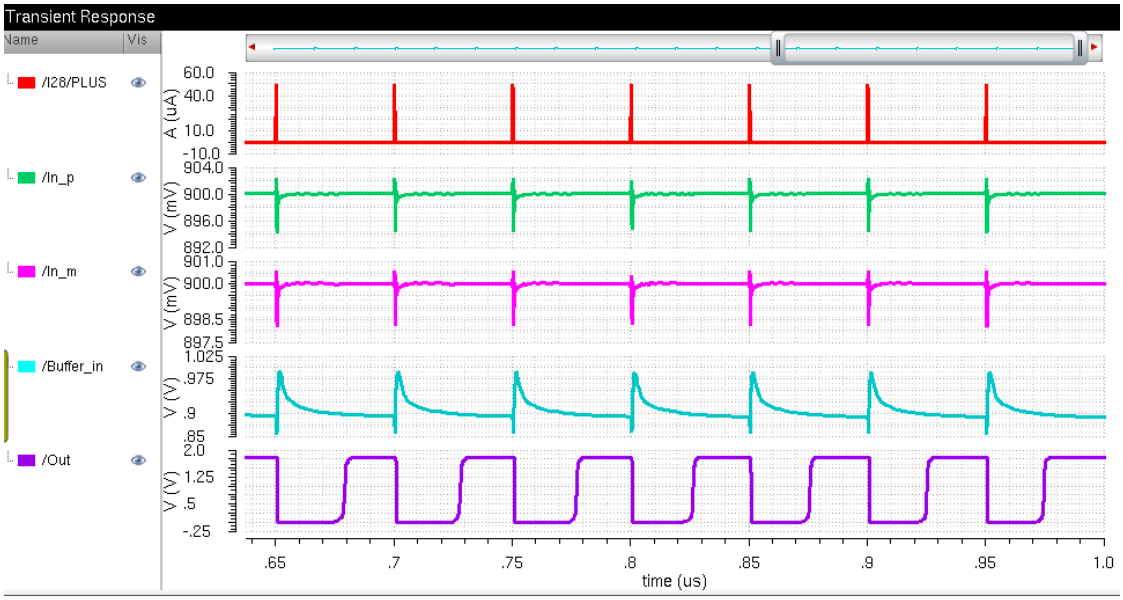


Complete Amplifier

To make the final schematic more concise, symbols were created for the TIA, the comparator, and the output buffer/inverter cascade.

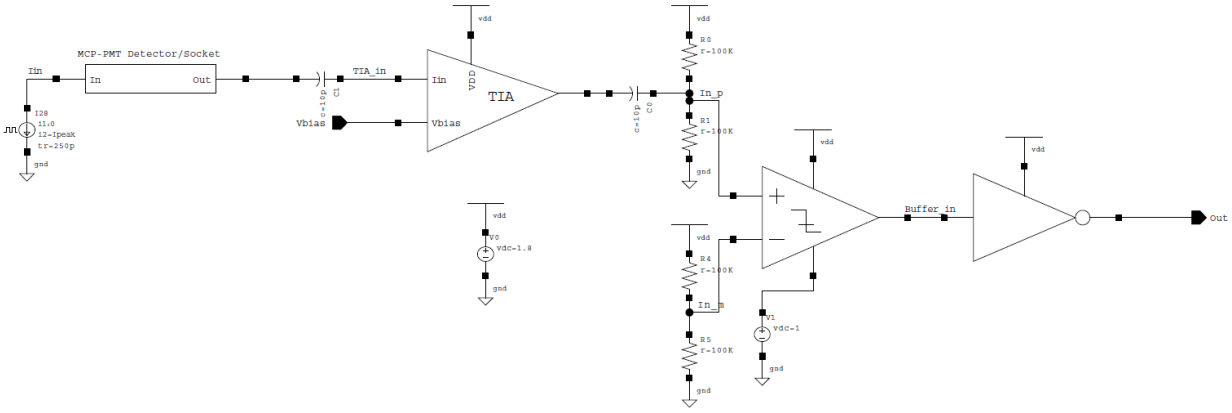


Note that in order to ensure that the input to the comparator swings around VDD/2, a resistive divider was used to force the minus input of the comparator to exactly 900mV, and the output of the TIA was AC coupled to the plus input of the comparator, which is also forced to a DC voltage of 900mV through use of a resistive divider. The input current source was AC coupled to the input of the TIA, but this is unnecessary in this particular schematic, which excludes the MCP model. The capacitor is there to AC couple the output of the MCP model to the input of the TIA. We can observe simulation results below, for a current pulse source with a pulse duration of 575ps (rise/fall times of 250ps, on time of 75ps), pulsing every 50ns.

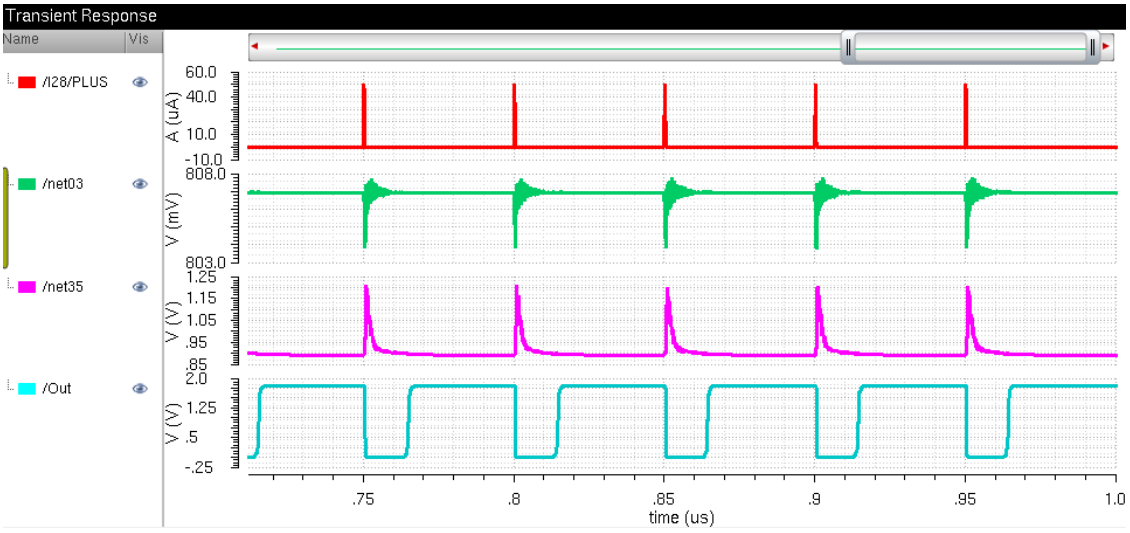


The red trace in the plot above shows the current pulse input to the TIA. As was mentioned previously, pulses have a total width of 575ps, and occur every 50ns. We can see that the output pulses low when the input pulses high, and remains low until the input to the buffer crosses the inverter switching point, which is roughly VDD/2, or 900mV. The switching point of the inverter was set so that the output waveform would have a duty cycle of 50%.

The output of the circuit without the MCP connected is more ideal, and less realistic than the output with the MCP connected. For the simulation above, we saw that a 575ps current pulse of at 50µA for 75ps results in a voltage pulse that lasts 25ns at 1.8V (with inverse logic, a voltage pulse that lasts 25ns at 0V, and is high for the remainder of the period). The schematic below is a modified, more realistic version of the amplifier, with the MCP-PMT Detector and Socket model connected from the current source to the input of the TIA through an AC coupling capacitor.



Below are results of the transient simulation of the amplifier including the MCP-PMT model. We can observe that the output still swings from ground (0V) up to VDD (1.8V), but with a duty cycle of nearly 75%. This is because the input to the cascade of inverters, or the output of the comparator before buffering, is not centered around the switching point. The same input current pulse source was used to generate 50µA pulses every 50ns.



Future Work and Improvements

Many aspects of the design can be improved or worked on further. The most significant parts of the study which can use the most improvement are the layout of the design, the AC response of the TIA, the power and current consumption of the amplifier, and the TIA input impedance.

Layout of the Design: Since radiation-hard layout was required for the layout of the circuitry designed in this study, a technique of layout which I have no familiarity with quite yet, no layout was done for any of the cells in the Cadence design library. In the future, I can research the layout techniques surrounding radiation-hard layout, and lay these circuits out in Cadence so that they can be fabricated on a chip.

AC Response of TIA: The AC response of the TIA is something that certainly needs some improvement. If the gain peak could be shifted down even further in frequency while maintaining a high gain at the operating frequency, the output voltage swing of the TIA would be much higher and much less current would need to be consumed by the comparator in order to make decisions and output logic voltage signals. Perhaps, as mentioned earlier, this TIA topology cannot be brought down much further in frequency, since it was originally designed for a 20 GHz application. In that case, a different TIA topology would need to be adopted in order to meet specifications.

Power/Current Consumption: The entire circuit consumes nearly 9mA of current and just less than 16mW of power as a result. Future work could be done to limit the current drawn by each branch of the current mirror between the preamplifier and decision circuit in the comparator. Perhaps the gain of the differential amplifiers in the comparator could also be increased to output larger signals that make switching of the inverters easier so we do not need three stages of inverters cascaded to get a clean digital signal out.

TIA Input Impedance: The MCP-PMT model has a transmission line, mentioned previously, with a characteristic impedance of 50Ω. Ideally, this means we would want the input impedance of our TIA to be 50Ω as well for the best possible matching and the least possible reflection between the transmission line and the input impedance of the amplifier. In order to bring the gain up, the input device of the TIA was increased in width, increasing the overall input impedance at the input node of the TIA. This gain-input-impedance tradeoff was a necessary one in order to meet specifications. In the future, it would be desirable to bring the input impedance down to 50Ω so that reflection does not occur and our output does not ring slightly when the input current pulses occur.

Simulation Results: For the sake of time, AC analyses, DC analyses, and transient analyses were run on the final design and analyzed, but not in great detail. Overshoot percentage, settling time, rise time and fall time were not calculated or analyzed. In the future, these time response characteristics can be analyzed in detail for a more thorough analysis of the amplifier and a more complete report of its performance.

Summary of Independent Study

Over the course of this independent study, I have familiarized myself with some of the design techniques and applications for CMOS RF integrated circuits. I have also learned the ins and outs of schematic design and simulation in the TowerJazz process in Cadence. Since layout of these devices requires knowledge of radiation-hard layout techniques, no layout was done during the design of the amplifier circuit discussed previously. Chapters from *The Design of CMOS Radio-Frequency Integrated Circuits*, such as Chapter 4 on RF considerations for the layout of resistors, capacitors, and inductors, and Chapter 2 on the importance of and design of low noise amplifiers, were read through and studied throughout the semester. The main takeaway from these chapters was that low noise amplifier design in RF circuits can best be performed using inductors as impedances for amplifiers, as opposed to resistors. Resistors introduce thermal noise, which we try to limit in low noise amplifiers. Inductors give us the control over the real part of the impedance without the thermal noise that comes with using resistors.

As a student who was entirely new to radio-frequency circuits in general to begin the semester, I have learned a lot about RF design and RF circuits. The task given to me was to design an RF amplifier to operate around 1.5 GHz with high enough gain to output digital logic from a comparator for each current pulse. Many different topologies were researched and tested in an attempt to meet the specifications of the project. IEEE research papers presented me with the single-ended regulated-cascode topology, which after testing, was disregarded, since the gain peak could not be shifted down in frequency low enough for the application. The single-ended common-gate regulated-cascode topology was designed and tested in Cadence, and found to be the best option, since it presented the best control over gain and center frequency of the gain peak. Manipulation of component parameters and control over individual device gain and speed made this topology the most versatile and the best choice for the application. Other topologies from *The Design of CMOS Radio-Frequency Integrated Circuits, by Thomas Lee,* such as the single-ended LNA and the differential LNA, were explored, and also decided against. The comparator topology was selected from figure 27.8 of the *CMOS: Circuit Design, Layout, and Simulation,* Fourth Edition. This comparator was chosen because it is a high speed comparator capable of switching at high frequencies while discriminating between signal levels in the range of millivolts. The output buffer sizes were selected to adjust the switching point of the inverters.

As a whole, this independent study has helped to expand my knowledge of radio-frequency circuit design and analysis, and integrated-circuit design and analysis in general. I feel far more confident and efficient using Cadence than I did before the semester began. I have become well-versed in the simulation techniques used in cadence, and learned to use parametric analyses to sweep more than one parameter at a time. Those these simulations may take a long time to complete, they can be very helpful in design that requires precise component value selection for optimal performance.