ECG 795 Final Project Report

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Abstract

This project details the design of a high-speed communication system with 72 pairs of differential signaling lines (144 lines in total) on a large PCB. The design uses LVDS signaling with a signal swing of 800mV. The transmitter chip is an Intel Arria 10 FPGA which sends data at a rate of 1Gbps, and the receiver is a CMOS high-speed comparator with a self-biased differential amplifier output stage designed for high-speed decision-making. Data being sampled has an aperture time of 555ps (55.5% of the ideal bit width of 1ns). With all independent and proportional noise sources considered, the signaling system has a net margin of 146mV, and a probabilistic MTBF of over eleven thousand years. The data is clocked at the receiver by a pair of single-edge triggered D flip flops after passing through the comparator. The design uses a synchronous timing convention with a clock frequency of 1GHz to clock data on every rising edge of the clock signal. The final stage of the system is an output buffer designed to eliminate noise in the output signals introduced by clock feedthrough in the D flip flops. Since the Arria 10 comes packaged in an FBGA package, via parasitics [8] (for routing purposes) and ball grid array contact parasitics [6] are modeled on the line. Since each signal line is in a homogeneous medium and traces are adequately spaced, a low total crosstalk coefficient of 0.0135 was obtained (forward crosstalk coefficient is zero due to homogeneous medium). Therefore, crosstalk control is not necessary in this design.

Overall Design Approach

CMOS circuitry was designed and implemented at the far end of the communication channel to reliably recover data. A high-speed comparator consisting of an externally biased diff-amp (for preamplification), a decision circuit, and a self-biased diff-amp (for postamplification) receives the data. This circuitry can resolve small differences in voltage at high speeds, so it is a perfect fit for noisy data coming in at 1Gbps from a long PCB trace. A pair of inverters is used on the output of the comparator to eliminate noise and restore full logic levels. The outputs of the comparator are fed into single edge-triggered D flip flops, where the data is clocked by a 1GHz clock signal. Though the comparator eliminates noise introduced by the line and package parasitics, the D flip flops introduce noise of their own in the form of clock feedthrough. An output buffer is used to eliminate clock feedthrough and produce clean, square output signals.

Board Specifications

The package for the selected FPGA [5], the Intel Arria 10 GX (240 I/O, 72 LVDS pairs), is a 484-pin Fine-pitch Ball Grid Array (FBGA) package, whose pitch is 1mm (39.4 mil), and whose ball diameter is 0.5mm at a minimum, or 0.7mm at a maximum (worst case) [10]. Assuming worst case, a trace width of 4 mils was chosen to route traces out of the package [9] to the signal layers, with a minimum space between traces of 15 mils. Assuming all 484 pins need to be routed, an 8-layer board is sufficient. There are 72 pairs of LVDS lines for a total of 144 individual signaling lines. The six internal layers are reserved for signals (so that all signal line media is homogenous), the top layer for power, and the bottom layer for ground. The board is a standard 62 mil-thick (1.6mm) PCB, and uses 1 oz copper for each of the 8 board layers (see Figure 1 below).

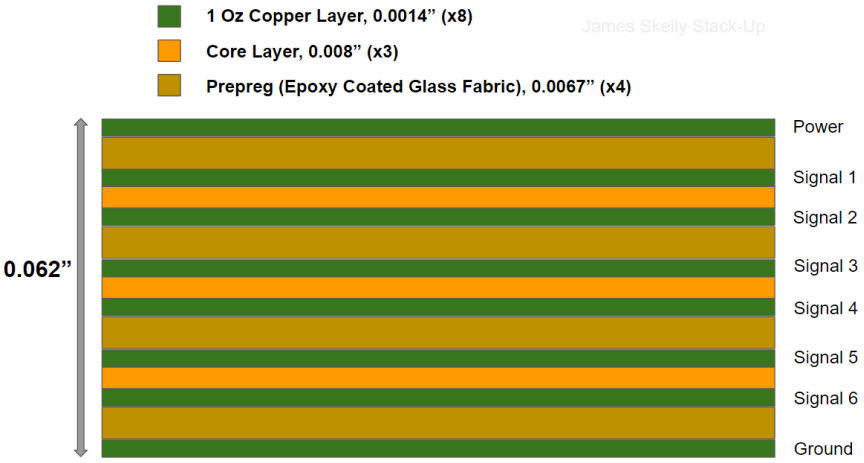

Figure 1: Board parameters and layer stack-up.

An electrical model of the line modeled in LTSpice (below) is helpful in analyzing the reliability of the system. Since the Arria 10 FPGA and the theoretical receiver IC use the same style of package (FBGA) [10], the package, via, and bonding parasitics [3], [6], [7] are modeled on both the near end and far end of the PCB trace. The trace itself is modeled by a lossy transmission line spice model, characterized by the values for R, L, C, and length calculated for a 48.5cm PCB trace. The signals at the end of the line model, Vp and Vm, are the inputs to the CMOS comparator.

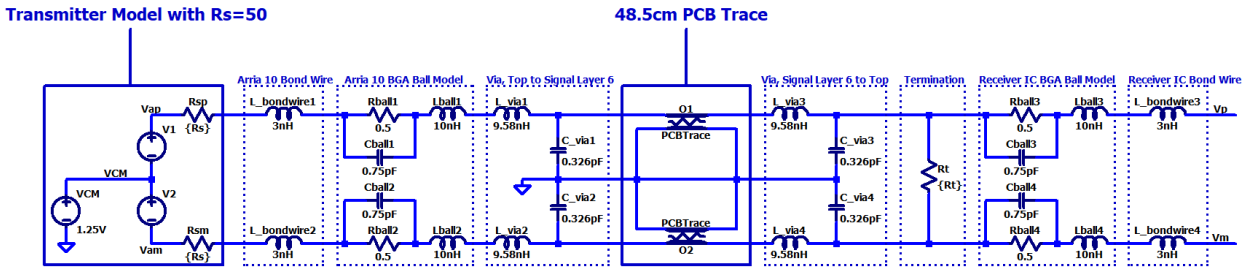

Figure 2: Electrical model of worst-case PCB trace including package, via, and bonding parasitics.

Impedance of the line was obtained by first calculating capacitance using parallel plate capacitance equations (to determine the total unwanted capacitance to any given line in the system) and inductance using the properties of traces in homogeneous mediums (Table A2). Capacitances accounted for include the capacitance to lines running parallel to a trace on the same signal layer, and the capacitance to lines running parallel on the signal layer above and below the trace of interest. For the worst-case scenario, the trace on the layer just above the ground plane was analyzed. A table of the values obtained is found below.

Capacitance to Parallel Line (Same Layer)	3.63	pF/m
Capacitance to Parallel Line (Layer Above)	19.47	pF/m
Capacitance to Ground Plane	106.13	pF/m
Differential Capacitance (Cd)	3.63	pF/m
Stray Capacitance (Cc)	129.37	pF/m
Capacitance of Line	133	pF/m
Resistance of Line	4.65	Ω/m
Inductance of Line	368	nH/m
Mutual Inductance	10.04	nH/m
Odd-Mode Line Impedance	51.18	Ω
Z_0 of Line	52.60	Ω
Velocity of Signal On Line	0.143	m/ns
Delay of Line	2.8	ns
Coefficient of Capacitive Crosstalk (k_{cx})	0.027	-
Coefficient of Inductive Crosstalk (k_{lx})	0.027	-
Coefficient of Forward Crosstalk	0	-
Coefficient of Reverse Crosstalk	0.0135	-

Table 1: Calculated parameters used to characterize system (equations from Table A2).

Signaling

The system uses LVDS signaling with a signal swing of 800mV. For high-speed signaling (data rates exceeding 700Mbps), it is recommended by the Intel Arria 10 Device Datasheet [5] that a common mode voltage of 1.25V is used. Since the channel supports data rates of 1Gbps, the system is modeled with a common mode voltage of 1.25V. Bipolar differential signaling (voltage mode) is used for noise immunity and largest possible signal swing to limit the effects of independent noise sources. To achieve a signal swing of 800mV, the Arria 10 will be modeled to output differential signals in which a “logic 1” is the case where Vp=1.45V, Vm=1.05V (Vp-Vm=400mV), and a “logic 0” is the case where Vp=1.05V, Vm=1.45V (Vp-Vm=-400mV). Note that the signals swing around the common mode voltage of 1.25V, and there are two signal levels (logic 1 and logic 0). A waveform diagram on the page to follow illustrates the signaling method.

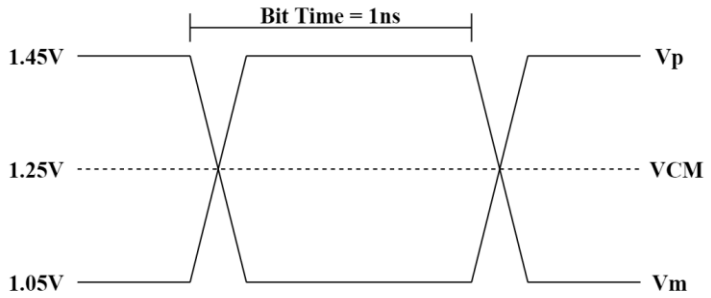

Figure 3: Waveform diagram showing signal levels, common mode voltage, and ideal bit time.

Rise time of a signal on the Arria 10 datasheet [5] (see Appendix, Table A1) for LVDS signaling is defined to have a maximum rise time of 130ps and a minimum rise time of 20ps. Since the slowest possible rise time should be used for worst case analysis, spice models will be made to have a rise time of 130ps to simulate the worst-case performance of the system and its parasitics. The lossy transmission line introduces noise, time delay, and attenuation to the system. These effects can be limited by the implementation of a two-tap equalizer, which sends "full-force" lone pulses and "lessened-force" repeated pulses. However, given that the system works reliably without the implementation of the equalizer, a large cost is avoided by neglecting to use equalization in the design. Since the crosstalk coefficient is very low, crosstalk control is also an unnecessary cost.

Timing and Synchronization

The clock signals used throughout the board are mesochronous, and the board design attempts to match delays from one clock input to the others using delay elements and identically sized traces. Each clock signal is periodic and oscillates at 1GHz. The comparator is asynchronous and makes a decision whenever the signals at the input differ by a voltage greater than its sensitivity (obtained from simulation to be around 40mV). Synchronization of the clock with the data is modeled in spice (below) using a parameterized time delay, td_clk. The time delay can be modified manually in simulation so that the clock signal rising edge is in the center of each bit.

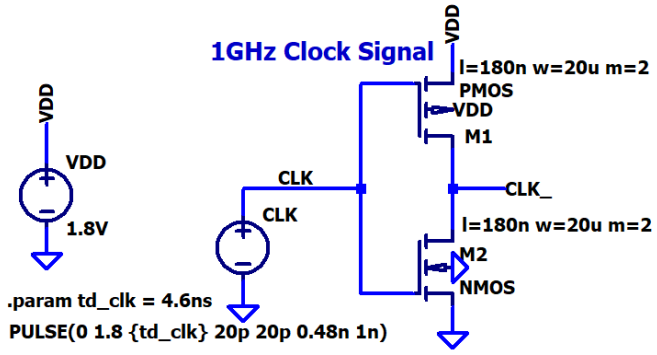

Figure 4: LTSpice model showing how clock delay can be parametrized for synchronization.

Since the receiver IC has a massive layout area due to the need for over 144 pins for receiving, a digital phase-locked loop (DPLL) could be designed to implement a per-line closed loop timing convention for the system with no extra cost added to the IC fabrication cost. The spice model in figure 4 above helps to model the system as if a DPLL has been implemented and has already locked once data transmission/reception begins. Since some DPLL topologies require a minimum number of transitions in order to lock, the transmitter would have to send alternating ones and zeros before sending any real data (which may contain long strings of 1s or 0s) to ensure that the loop is locked and the receiver samples the middle of each bit of data.

Noise Budget, BER

The table below outlines the noise budget for the system, considering both independent and proportional noise sources. Values were calculated using noise analysis and characterization of PCB traces discussed previously. The CMOS comparator used for the receiver was approximated to have a combined offset and sensitivity of 40mV using 180nm BSIM model devices. Transmitter offset was approximated to be 10mV but is not specified in the transmitter specifications table for the Arria 10 FPGA (Table 1A). Since all signal trace media are homogeneous, forward crosstalk cancels completely and yields a coefficient of 0. Reverse crosstalk is low enough to neglect because of trace spacing. The values in Table 2 (below) show that the system will operate reliably despite line parasitics.

Voltage Swing	800mV
Gross Margin	400mV
Reverse Crosstalk Coefficient	0.0135
Forward Crosstalk Coefficient	0
Worst-case (ISI) Reflections (20% mismatch)	0.111
Attenuation Coefficient	0.130
Kn	0.255 (204mV)
Receiver Offset, Sensitivity	40mV
Transmitter Offset	10mV
Bounded Noise Total	254mV
Net Margin	146mV
Power Supply Noise	5mV
Total Gaussian Noise	$15mV_{RMS}$
VSNR	9.73
BER	2.77e-21
MTBF (in seconds)	361 billion
MTBF (in years)	11,459

Table 2: Calculated noise budget, bit error rate, and MTBF for system (equations from Table A2).

Timing Budget

Values concerning the transmitter in Table 3 were obtained from the Arria 10 datasheet [5] (Table 1A). Values concerning the receiver are approximate and were estimated based on the timing budget found in the *Digital Systems Engineering* textbook [2]. The aperture time is, as we know, the sum of the setup and hold times. We know that if we want to operate at 1Gbps, our bit time is 1ns, and due to the timing budget, we cannot have an aperture time exceeding 555 ps. All known sources of jitter are listed in the table. Since no PLL was implemented and the timing convention used is synchronous, neither transmitter nor receiver skew are cancelled, meaning they both contribute to the total timing uncertainty.

Transmitter Clock Jitter	20 ps
Receiver Clock Jitter	20 ps
Transmitter Jitter	160 ps
Receiver Jitter	30 ps
Trace Delay	2.8 ns
Data Rise Time, Fall Time (Worst Case)	130 ps
Transmitter Skew	15 ps
Receiver Skew	30 ps
Clock Rise Time, Fall Time	20 ps
Total Uncertainty	425 ps
Aperture Time (Max)	555 ps
Bit Time	1 ns

Table 3: Calculated timing budget, maximum aperture time for system.

Power and Cost Analysis

There are two main components of the design which consume power: the receiver circuitry and the transmitter circuitry/line parasitics. Figure 5 shows the transmitted Vp voltage signal (blue), the current drawn by the Vp voltage source of the transmitter model (black), and the product of the two, yielding a power plot (red). This plot represents the average power supplied to the positive half of the differential pair. The Vm voltage source supplies the same average power per cycle.

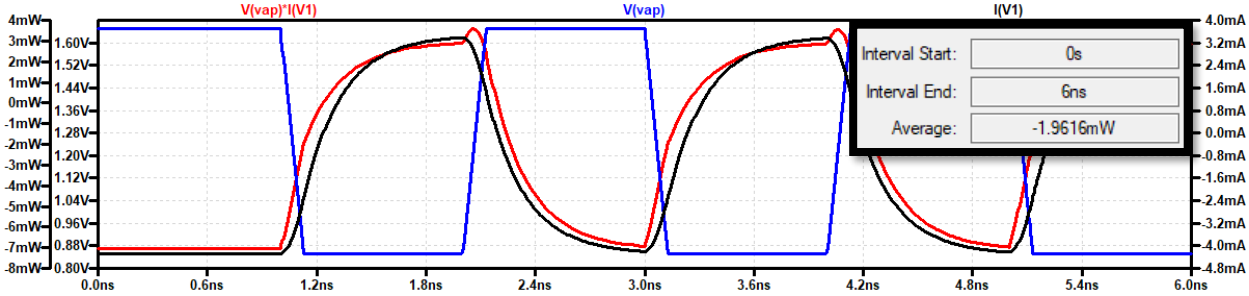

Figure 5: LTSpice simulation results for average power dissipated by transmitter with alternating ones and zeros.

Figure 6 shows the power dissipated in the receiver circuitry. The plot consists of 1.8V DC VDD (blue), the current drawn from VDD over a few cycles (black) and the product of the two, yielding power dissipation (red). A complete power analysis of the system is given by Table 4.

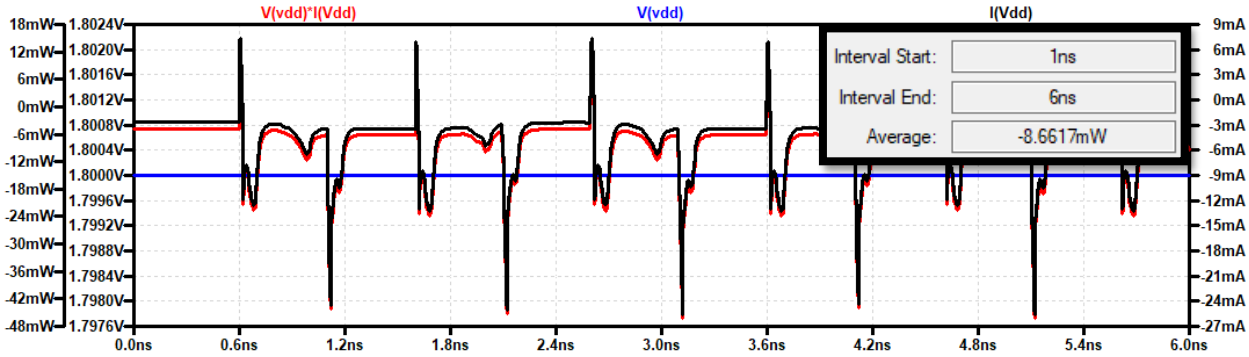

Figure 6: LTSpice simulation results for average power dissipated by receiver with alternating ones and zeros.

Average Power Supplied by Vp	1.96mW
Average Power Supplied by Vm	1.96mW
Average Power Supplied by Transmitter	3.92mW
Average Current Drawn by VDD	4.61mA
Average Power Dissipated by Comparator	6.132mW
Average Power Dissipated by D Flip Flops	1.306mW
Average Power Dissipated by Clock Generator	0.517mW
Average Power Dissipated by Output Buffers	0.367mW
Average Power Supplied by VDD	8.66mW
Total Average Power Dissipated by One Link	12.58mW
Total Average Power Dissipated by Design	**905.8mW**

Table 4: Power analysis of system. Values are listed in terms of magnitude.

Table 5 shows a cost analysis of the board by link and total, including the transmitter FPGA and a price estimate for the theoretical receiver IC, containing 72 comparators, 144 D flip flops, and 144 output buffers. A 160-pin BGA IC on DigiKey was used to price match the receiver for analysis. Note that even 20% mismatched termination resistors are ordered on a reel with quantity of 5000.

PCB Area	73.1 in^2
Cost of 8-layer Board	\$0.75/in^2
Calculated Cost of Board	\$54.84
Arria 10 FPGA Cost (484-pin BGA Package)	\$410.00
Receiver IC Cost (160-pin BGA Package)	\$33.56
Termination Resistor Cost (0603 100Ω, ±20%)	\$62.50
Cost Per Link of System	\$7.79
Total Cost of System	**\$560.90**

Table 5: Cost analysis of system.

Receiver Circuitry

The receiver is designed to take in the noisy data, make a correct decision, clock the data after a decision is made and output clean square waves with full logic levels (VDD=1.8V). Figure 7 shows a schematic of the receiver, where Vp and Vm, the inputs to the comparator, are the signals out of the electrical model of the PCB trace.

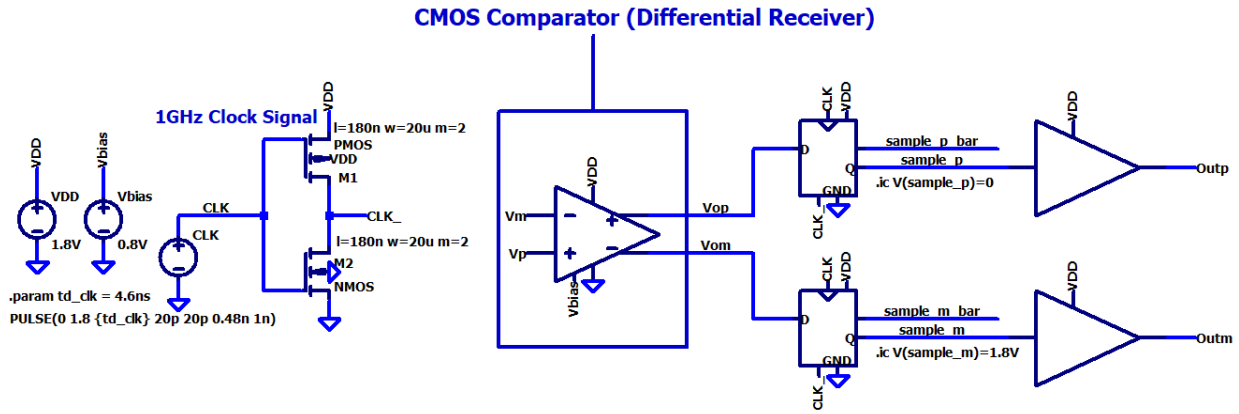

Figure 7: LTSpice schematic of receiver circuitry, consisting of comparator, DFFs, and output buffers.

The CMOS comparator was designed using 180nm BSIM device models. The design is based on a comparator found in Dr. R. Jacob Baker's CMOS textbook [1]. The circuit consists of a differential amplifier input stage for preamplification, a decision circuit, a self-biased differential amplifier for postamplification, and an output buffer to regenerate differential signals.

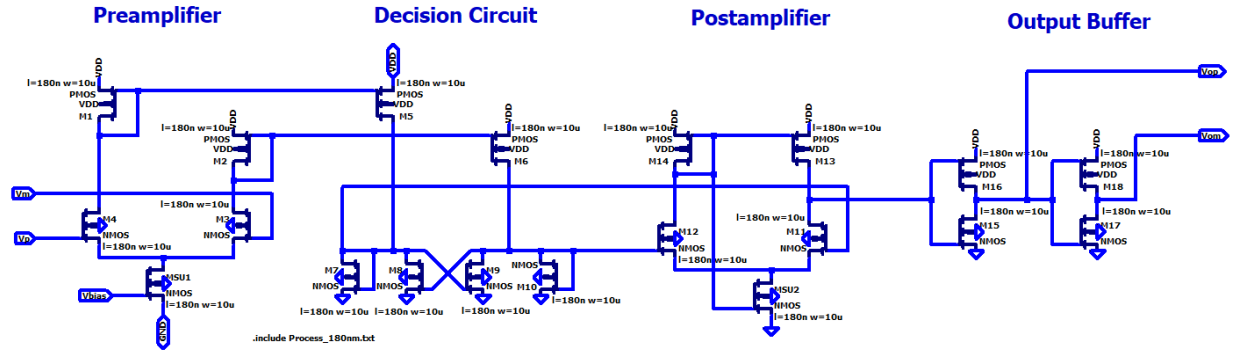

Figure 8: LTSpice schematic of CMOS comparator with preamp, decision circuit, postamp, and output buffer.

Simulation results for the receiver circuitry are found in the appendix in Figure A1. The waveforms plotted are the inputs to the line (top), the inputs to the comparator (middle), and the outputs of the final output buffers (bottom).

Eye Diagram and TDR, TDT Simulations

Using worst-case modeling of the line in LTSpice, Figure 7 and Figure 8 (below) were obtained, where Figure 7 shows the eye diagram at the input of the comparator and Figure 8 shows the eye diagram at the output of the comparator. Note the full logic levels at the comparator output.

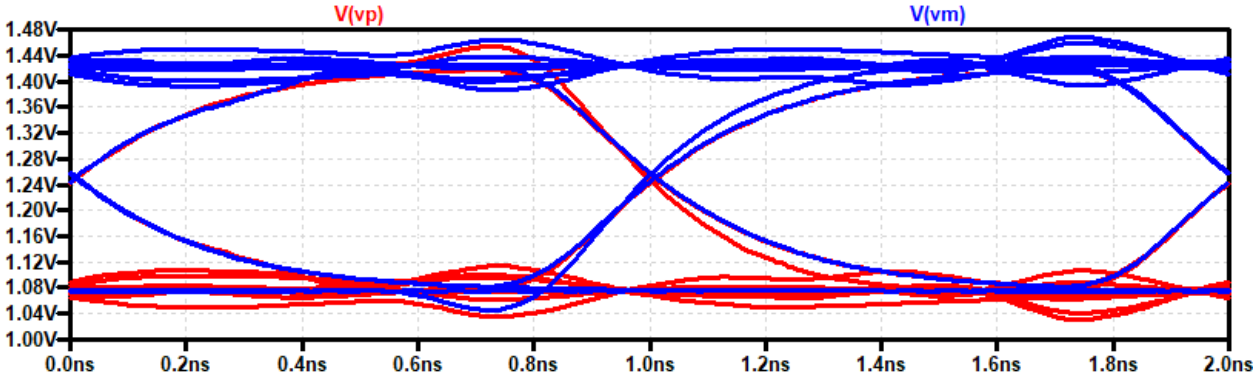

Figure 7: LTSpice eye diagram at input of CMOS comparator circuit.

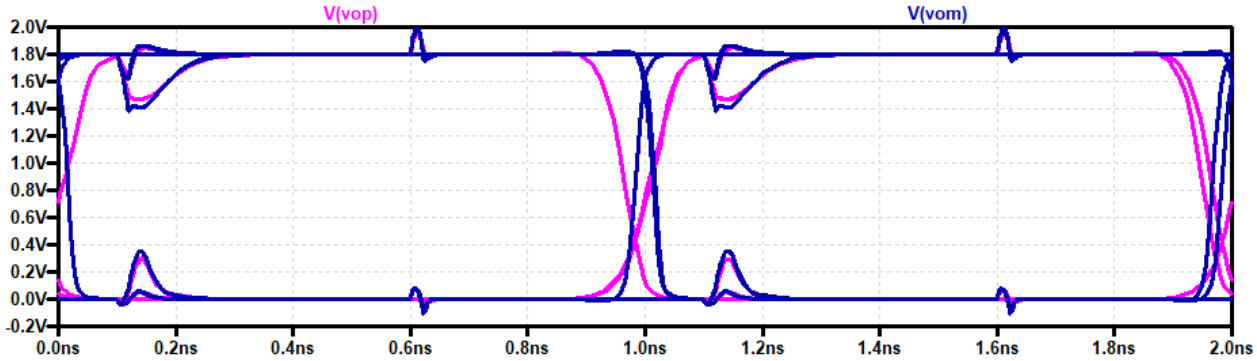

Figure 8: LTSpice eye diagram at output of CMOS comparator circuit (DFF inputs).

A fast voltage pulse from 0 to 1V with a rise time of 20ps was used as an input to the line to obtain the TDR (black) and TDT (red, blue) waveforms of Figure 9 (below).

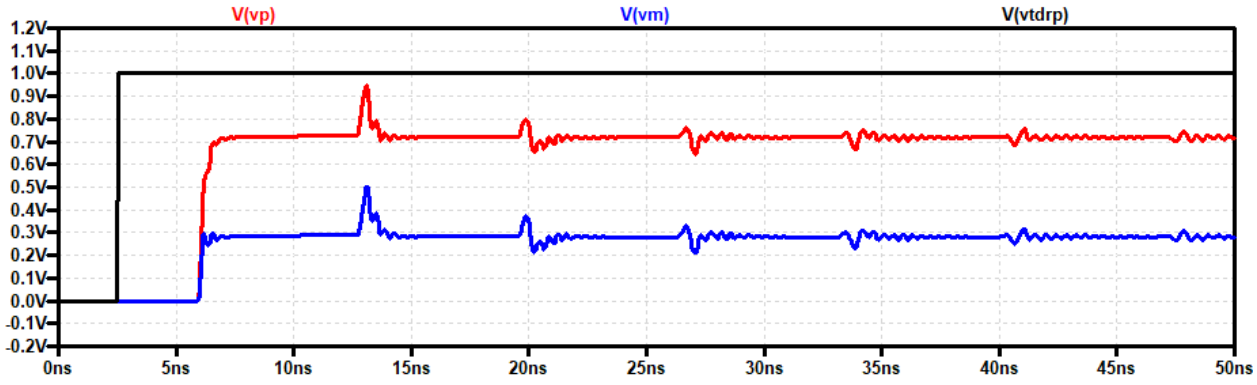

Figure 9: Pulse wave input and TDT (waveforms at receiver) for worst-case link model in LTSpice.

Conclusion and Future Improvements

The system operates reliably with an aperture time over half of the ideal bit width (555ps out of 1ns bit width) at a data rate of 1Gbps. The designed CMOS circuits on the receiver end of the links square up the signals and produce full logic levels at the output of the receiver from noisy input signals at the end of the lengthy PCB traces. The system costs just over $500 and on average, consumes less than 1 Watt of power in total.

Though the system operates reliably, there are key improvements that could be made, both to improve the operation of the circuit and to create a more accurate representation of the system. The main modeling improvements to be made include modeling vias as small transmission lines, modeling the transmitter using something other than an ideal voltage source, and using a voltage-controlled voltage source to model larger attenuation. The document used to calculate and represent via parasitics [3] highlights how a via can represented using a transmission line model. Since the size of the via is significant in an 8-layer board, this modification would result in a more accurate model of the line. Since the on-chip transmitter for the Arria 10 FPGA is, of course, not ideal, a more accurate model with a larger output impedance and limited current supply would contribute to creating a more accurate depiction of the line as well. Using a lossy transmission line model in LTSpice introduced around 100mV of attenuation, but it is likely that in reality, attenuation would be greater. This can be modeled with a voltage-controlled voltage source with a gain of less than 1 to yield a more accurate eye diagram and noise budget.

The main improvements to be made to the design pertain to the comparator output and the synchronization of the clock signal with the data. The comparator output stage uses two inverters in series and taps the input and output of the second inverter to regenerate differential signals from the single-ended output of the comparator. This is not necessarily a good way to regenerate differential signals. A different method could send the single ended output to two DFFs as the CLK input, one whose D input is tied high and the other whose D input is tied low. The outputs of the DFFs would then be differential signals depending on the single-ended output of the comparator, less the delay/phase shift introduced by the inverter currently being used. The other improvement to be made is the design and implementation of a digital phase-locked loop for synchronization and implementation of a per-line closed loop timing convention. The current system uses a variable delay in spice so that the user can manually “lock” the CLK to data, but a feedback system like a DPLL is a more robust and would add hardly any cost to the system.

Appendix

This appendix consists of plots, tables, schematics, device models, and equations used to obtain the data found in the tables in the body of the report.

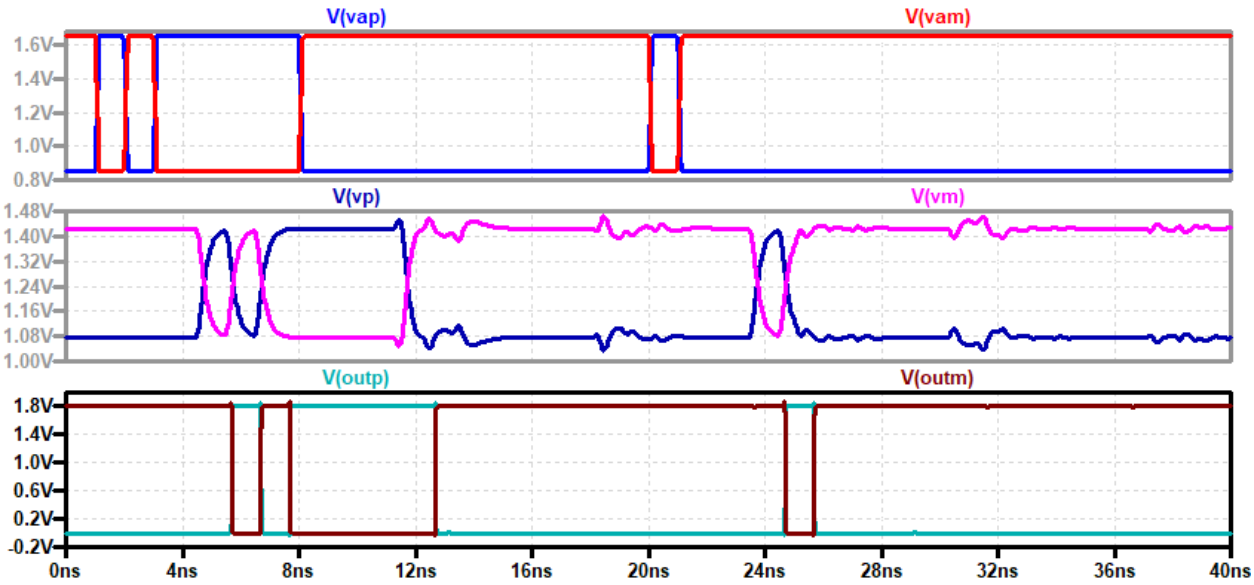

Figure A1: Simulation showing system inputs (top), comparator inputs (middle), and system outputs (bottom).

Intel® Arria® 10 Device Datasheet
A10-DATASHEET | 2020.03.20

Table 34. Transmitter Specifications

Symbol/Description	Condition	All Transceiver Speed Grades			Unit
		Min	Typ	Max	
Supported I/O Standards	—	High Speed Differential I/O (57)			—
Differential on-chip termination resistors	85-Ω setting	—	85 ± 20%	—	Ω
	100-Ω setting	—	100 ± 20%	—	Ω
V_{OCM} (AC coupled)	V_{CCT} = 0.95 V	—	450	—	mV
	V_{CCT} = 1.03 V	—	500	—	mV
	V_{CCT} = 1.12 V	—	550	—	mV
V_{OCM} (DC coupled)	V_{CCT} = 0.95 V	—	450	—	mV
	V_{CCT} = 1.03 V	—	500	—	mV
	V_{CCT} = 1.12 V	—	550	—	mV
Rise time (58)	20% to 80%	20	—	130	ps
Fall time (58)	80% to 20%	20	—	130	ps
Intra-differential pair skew (59)	TX V_{CM} = 0.5 V and slew rate setting of SLEW_R5 (60)	—	—	15	ps

Table A1: Arria 10 FPGA Transmitter Specifications

	EQUATION	DESCRIPTION
1.	$C = \frac{w\varepsilon}{s} + \frac{2\pi}{ln(2s/r)}$	• **Capacitance per meter used to characterize impedance of PCB trace.**
2.	$BER = e^{-(VSNR^2/2)}$	• **Bit error rate calculated from VSNR.**
3.	$L = \frac{\mu\varepsilon}{C}$	• **Inductance per meter used to characterize impedance of PCB trace.**
4.	$\mu = 4\pi \cdot 10^{-7}\ H/m$	• **Permeability of free space.**
5.	$\varepsilon_0 = 8.85 \cdot 10^{-12}\ F/m$	• **Permittivity of free space.**
6.	$\varepsilon = \varepsilon_r \varepsilon_0$	• **Relative permittivity calculation used to calculate permittivity in FR-4.**
7.	$C = C_C + C_D$	• **Representing capacitance per meter in terms of stray and coupled capacitance.**
8.	$\frac{L}{M} = \frac{C}{C_D} = \frac{1}{k_{cx}} = \frac{1}{k_{lx}}$	• **Relating inductances to capacitances for odd mode impedance calculation.**
9.	$k_{rx} = \frac{k_{cx} + k_{lx}}{4}$	• **Calculation of reverse crosstalk coefficient.**
10.	$R = \frac{\rho L}{A}$	• **Resistance per meter of PCB trace.**
11.	$Z_0 = \sqrt{L/C}$	• **Impedance of PCB trace.**
12.	$Z_{ODD} = \sqrt{(L - M)/(C + C_D)}$	• **Odd mode impedance of PCB trace.**

Table A2: Equations used for calculating system parameters.

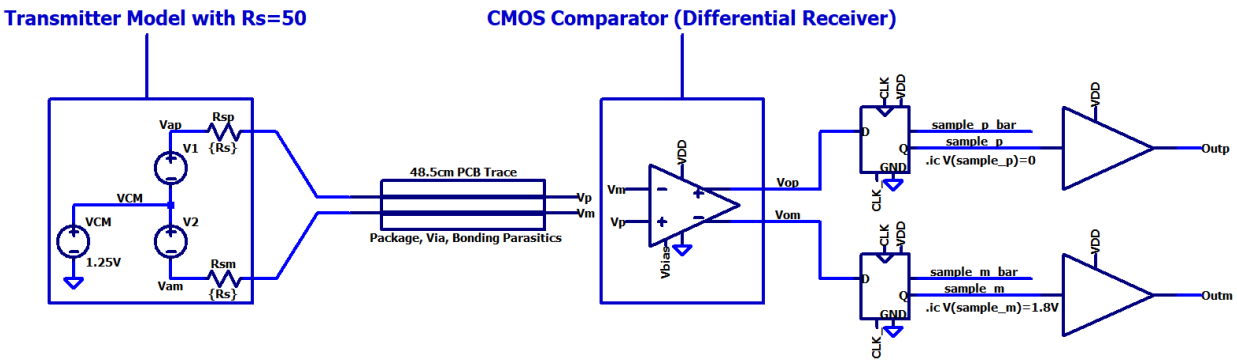

Figure A2: Full LTSpice schematic of system.

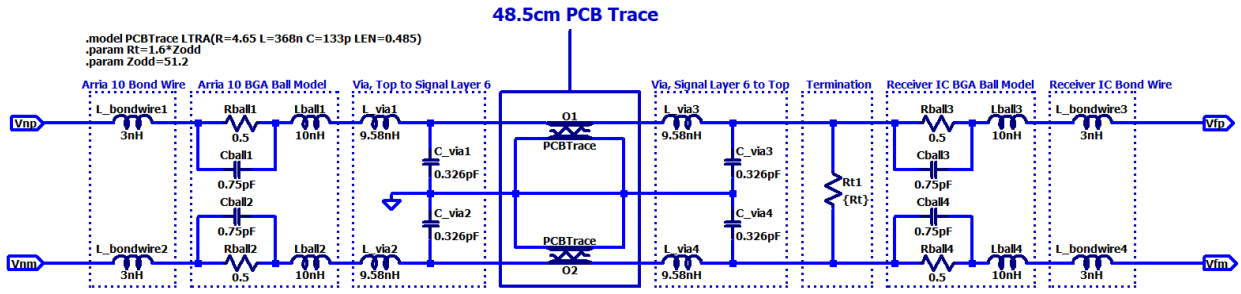

Figure A3: PCB trace, package, via, and bonding parasitics.

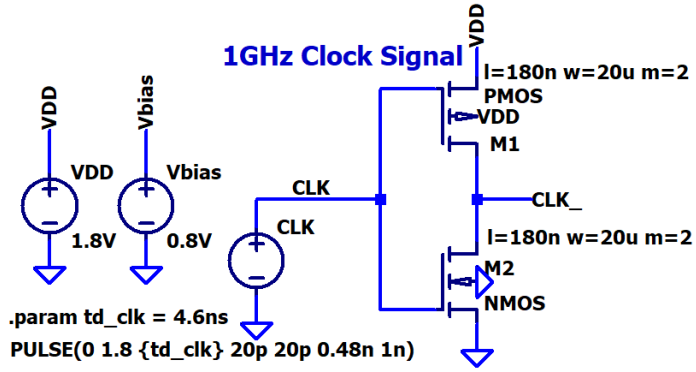

Figure A4: Clock generator circuit schematic.

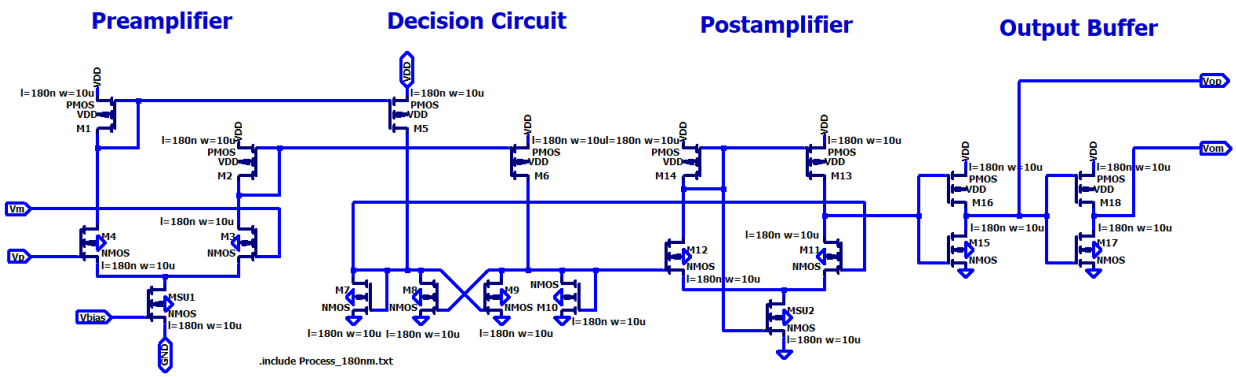

Figure A5: Comparator schematic.

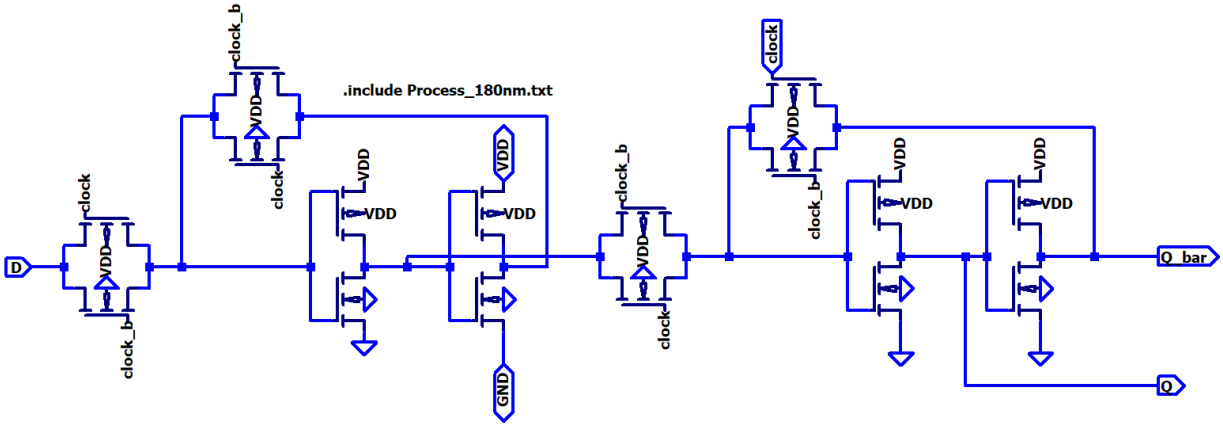

Figure A6: D flip flop schematic.

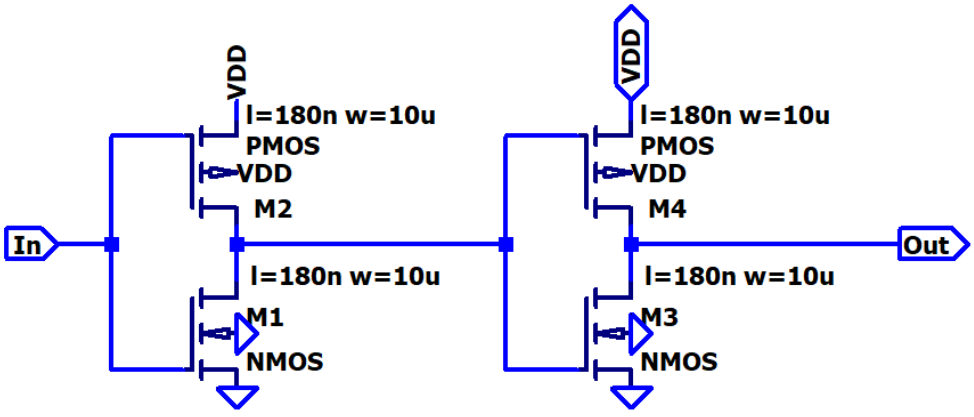

Figure A7: Output buffer schematic.

Device Models (180nm BSIM)

```
* NMOS Model 180nm
.model NMOS NMOS
+Level = 49

+Lint = 4.e-08 Tox = 4.e-09
+Vth0 = 0.3999 Rdsw = 250

+lmin=1.8e-7 lmax=1.8e-7 wmin=1.8e-7 wmax=1.0e-4 Tref=27.0 version =3.1
+Xj= 6.0000000E-08         Nch= 5.9500000E+17
+lln= 1.0000000            lwn= 1.0000000              wln= 0.00
+wwn= 0.00                 ll= 0.00
+lw= 0.00                  lwl= 0.00                   wint= 0.00
+wl= 0.00                  ww= 0.00                    wwl= 0.00
+Mobmod=  1                binunit= 2                  xl=  0
+xw=  0                    binflag=  0
+Dwg= 0.00                 Dwb= 0.00

+K1= 0.5613000             K2= 1.0000000E-02
+K3= 0.00                  Dvt0= 8.0000000             Dvt1= 0.7500000
+Dvt2= 8.0000000E-03       Dvt0w= 0.00                 Dvt1w= 0.00
+Dvt2w= 0.00               Nlx= 1.6500000E-07          W0= 0.00
+K3b= 0.00                 Ngate= 5.0000000E+20

+Vsat= 1.3800000E+05       Ua= -7.0000000E-10          Ub= 3.5000000E-18
+Uc= -5.2500000E-11        Prwb= 0.00
+Prwg= 0.00                Wr= 1.0000000               U0= 3.5000000E-02
+A0= 1.1000000             Keta= 4.0000000E-02         A1= 0.00
+A2= 1.0000000             Ags= -1.0000000E-02         B0= 0.00
+B1= 0.00

+Voff= -0.12350000         NFactor= 0.9000000          Cit= 0.00
+Cdsc= 0.00                Cdscb= 0.00                 Cdscd= 0.00
+Eta0= 0.2200000           Etab= 0.00                  Dsub= 0.8000000

+Pclm= 5.0000000E-02       Pdiblc1= 1.2000000E-02      Pdiblc2= 7.5000000E-03
+Pdiblcb= -1.3500000E-02   Drout= 1.7999999E-02        Pscbe1= 8.6600000E+08
```

```
+Pscbe2= 1.0000000E-20     Pvag= -0.2800000           Delta= 1.0000000E-02
+Alpha0= 0.00              Beta0= 30.0000000
+kt1= -0.3700000           kt2= -4.0000000E-02        At= 5.5000000E+04
+Ute= -1.4800000           Ua1= 9.5829000E-10         Ub1= -3.3473000E-19
+Uc1= 0.00                 Kt1l= 4.0000000E-09        Prt= 0.00

+Cj= 0.00365               Mj= 0.54                   Pb= 0.982
+Cjsw= 7.9E-10             Mjsw= 0.31                 Php= 0.841
+Cta= 0                    Ctp= 0                     Pta= 0
+Ptp= 0                    JS=1.50E-08                JSW=2.50E-13
+N=1.0                     Xti=3.0                    Cgdo=2.786E-10
+Cgso=2.786E-10            Cgbo=0.0E+00               Capmod= 2
+NQSMOD= 0                 Elm= 5                     Xpart= 1
+Cgsl= 1.6E-10             Cgdl= 1.6E-10              Ckappa= 2.886
+Cf= 1.069e-10             Clc= 0.0000001             Cle= 0.6
+Dlc= 4E-08                Dwc= 0                     Vfbcv= -1
```

*** PMOS Model 180nm**

```
.model PMOS PMOS
+Level = 49

+Lint = 3.e-08 Tox = 4.2e-09
+Vth0 = -0.42 Rdsw = 450

+lmin=1.8e-7 lmax=1.8e-7 wmin=1.8e-7 wmax=1.0e-4 Tref=27.0 version =3.1
+Xj= 7.0000000E-08         Nch= 5.9200000E+17
+lln= 1.0000000            lwn= 1.0000000             wln= 0.00
+wwn= 0.00                 ll= 0.00
+lw= 0.00                  lwl= 0.00                  wint= 0.00
+wl= 0.00                  ww= 0.00                   wwl= 0.00
+Mobmod=  1                binunit= 2                 xl= 0.00
+xw= 0.00
+binflag=  0               Dwg= 0.00                  Dwb= 0.00

+ACM= 0                    ldif=0.00                  hdif=0.00
+rsh= 0                    rd= 0                      rs= 0
```

```
+rsc= 0                    rdc= 0

+K1= 0.5560000             K2= 0.00
+K3= 0.00                  Dvt0= 11.2000000          Dvt1= 0.7200000
+Dvt2= -1.0000000E-02      Dvt0w= 0.00               Dvt1w= 0.00
+Dvt2w= 0.00               Nlx= 9.5000000E-08        W0= 0.00
+K3b= 0.00                 Ngate= 5.0000000E+20

+Vsat= 1.0500000E+05       Ua= -1.2000000E-10        Ub= 1.0000000E-18
+Uc= -2.9999999E-11        Prwb= 0.00
+Prwg= 0.00                Wr= 1.0000000             U0= 8.0000000E-03
+A0= 2.1199999             Keta= 2.9999999E-02       A1= 0.00
+A2= 0.4000000             Ags= -0.1000000           B0= 0.00
+B1= 0.00

+Voff= -6.40000000E-02     NFactor= 1.4000000        Cit= 0.00
+Cdsc= 0.00                Cdscb= 0.00               Cdscd= 0.00
+Eta0= 8.5000000           Etab= 0.00                Dsub= 2.8000000

+Pclm= 2.0000000           Pdiblc1= 0.1200000        Pdiblc2= 8.0000000E-05
+Pdiblcb= 0.1450000        Drout= 5.0000000E-02      Pscbe1= 1.0000000E-20
+Pscbe2= 1.0000000E-20     Pvag= -6.0000000E-02      Delta= 1.0000000E-02
+Alpha0= 0.00              Beta0= 30.0000000
+kt1= -0.3700000           kt2= -4.0000000E-02       At= 5.5000000E+04
+Ute= -1.4800000           Ua1= 9.5829000E-10        Ub1= -3.3473000E-19
+Uc1= 0.00                 Kt1l= 4.0000000E-09       Prt= 0.00

+Cj= 0.00138               Mj= 1.05                  Pb= 1.24
+Cjsw= 1.44E-09            Mjsw= 0.43                Php= 0.841
+Cta= 0.00093              Ctp= 0                    Pta= 0.00153
+Ptp= 0                    JS=1.50E-08               JSW=2.50E-13
+N=1.0                     Xti=3.0                   Cgdo=2.786E-10
+Cgso=2.786E-10            Cgbo=0.0E+00              Capmod= 2
+NQSMOD= 0                 Elm= 5                    Xpart= 1
+Cgsl= 1.6E-10             Cgdl= 1.6E-10             Ckappa= 2.886
+Cf= 1.058e-10             Clc= 0.0000001            Cle= 0.6
+Dlc= 3E-08                Dwc= 0                    Vfbcv= -1
```

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