James Skelly

ECG 722: Mixed-Signal Circuit Design

Dr. R. Jacob Baker

Continuous Time K-Delta-1-Sigma (KD1S) ADC Design

The continuous time K-delta-1-sigma ADC design discussed in this report (designed in the C5 process, minimum L of 600nm, VDD = 5V) achieved an SNR of 47.3dB (serial) and 42.9dB (parallel) corresponding to an effective number of bits of 7.56 and 6.82, respectively, with a bandwidth of 2.23MHz sensing a 1MHz input signal whose amplitude is 1.5V, consuming just 48.9mW of power on average. It also achieved an SNR of 37.0dB (serial) and 30.4dB (parallel) corresponding to an effective number of bits of 5.86 and 4.75, respectively, with a bandwidth of 4.46MHz. The topology used was a 4-path 2nd-order KD1S modulator topology and its performance was compared against both continuous and discrete time 8-path 1st-order KD1S modulator topologies.

Summary of Performance

Kpath	Order	F,osc (fs,new=K*F,osc)	Bandwidth	Serial SNR	Serial Neff	Parallel SNR	Parallel Neff	Serial SNDR	Parallel SNDR
No Feedback Control									
1	1	77MHz	3.22MHz	31.7dB	4.97	31.7dB	4.97	25.5dB	25.5dB
4	1	101MHz	3.17MHz	46.1dB	7.36	43.6dB	6.94	30.6dB	30.8dB
Transmission Gate Feedback Control									
4	2	71MHz	4.46MHz	37.0dB	5.86	30.4dB	4.75	32.4dB	29.3dB
4	2	71MHz	2.23MHz	47.3dB	7.56	42.9dB	6.82	43.8dB	40.7dB
8	1	71MHz	4.46MHz	40.1dB	6.49	30.2dB	4.72	38.0dB	29.0dB
8	1	71MHz	2.23MHz	44.5dB	7.10	44.5dB	7.10	41.9dB	39.5dB
Dicrete Time KD1S Modulator For Comparison									
8	1	200MHz	6.25MHz	53.1dB	8.52	52.7dB	8.45	42.1	43.1
4-Path 2nd-Order CT KD1S Average Power Consumption							48.5mW		
8-Path 1st-Order CT KD1S Average Power Consumption							35.4mW		
8-Path 1st-Order DT KD1S Average Power Consumption							63.7mW		

Design Tradeoffs

Category	Description of Tradeoff
Amplifier Used in Integrator	• Amplifier used in integrator was selected to be a wide-swing differential amplifier with sufficient gain for integration operation in delta-sigma modulation. • **Pros:** Simple topology, low power consumption, small layout space, high-speed. • **Cons:** Lower gain than other amplifiers resulting in higher gain error term.
Voltage-Controlled Oscillator	• A voltage-controlled ring oscillator was used to generate the clock signals for this design rather than a ring oscillator with fixed oscillation frequency. • **Pros:** Very little increase in layout area (added current-starved inverter and small biasing circuit in oscillator) for increase in adjustability of oscillation frequency. • **Cons:** Duty cycle of oscillator is not 50%, posing challenges.
Clock Generator	Delay element-based ring oscillator used instead of inverter-based ring oscillator to generate clock signals for K paths. • **Pros:** Clock signal rising edges are equally spaced in time during each cycle. • **Cons:** Using delay elements rather than inverters adds devices and therefore increases layout area and power consumption.
Comparator	• A clocked comparator with high sensitivity and wide input range was used to compare the integrator output to the common mode voltage in each of the paths for feedback control. • **Pros:** Sensitivity allows the comparator to make the correct decision more often resulting in better SNR and better regulation of the summing node. • **Cons:** More hardware and larger layout area than other comparator topology, added complexity with pre-amplifier stage.
Transistor Sizes	• Transistors used throughout the design were selected to have minimum length for the C5 process (600nm) and width was selected based on the current required for that particular circuit. • **Pros:** Small L transistors have higher speed and smaller layout area. • **Cons:** Small L transistors have less gain so larger W and therefore more power is required for a given circuit to have any significant drive.

Analysis of Design and Performance of Individual Components

I. Transmission Gate and Feedback Paths

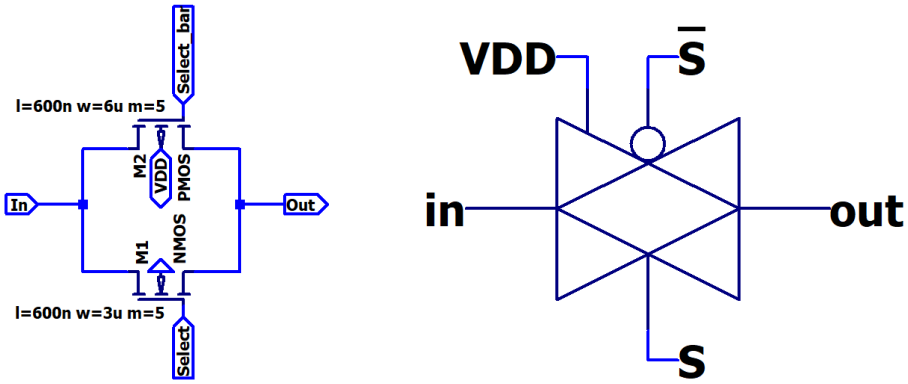

Figure 1: Transmission Gate (TG) Schematic and Symbol Views

Figure 1 shows a transmission gate designed to place in the feedback path for feedback signal control in the KD1S modulator discussed in this report. A particular clock signal from the clock generator is used to clock the NMOS in the TG, and that signal's complement is used to clock the PMOS in the TG so that when the NMOS gate goes high, the PMOS gate goes low, turning them both on so that the TG can pass whatever signal is at its input through to its output. When the NMOS gate goes low, the PMOS gate goes high, so both devices are off and the transmission gate will not let the signal through.

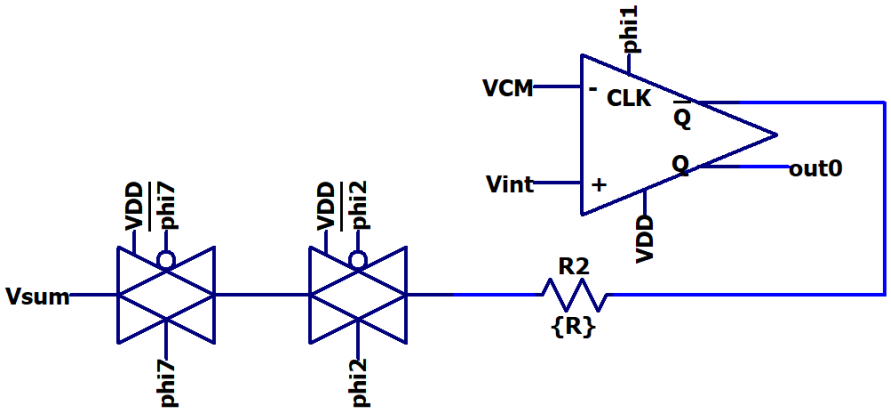

Figure 2: A Clock-Controlled Feedback Path to the Vsum Node of the Integrator

Though the transmission gate is constructed using twice as much hardware as a pass gate, the full power rails can pass through a transmission gate, where pass gates lose a threshold voltage of input range in either direction. A clock-controlled feedback path used in the KD1S modulator design is shown in figure 2 above.

II. Clock Generator Circuit

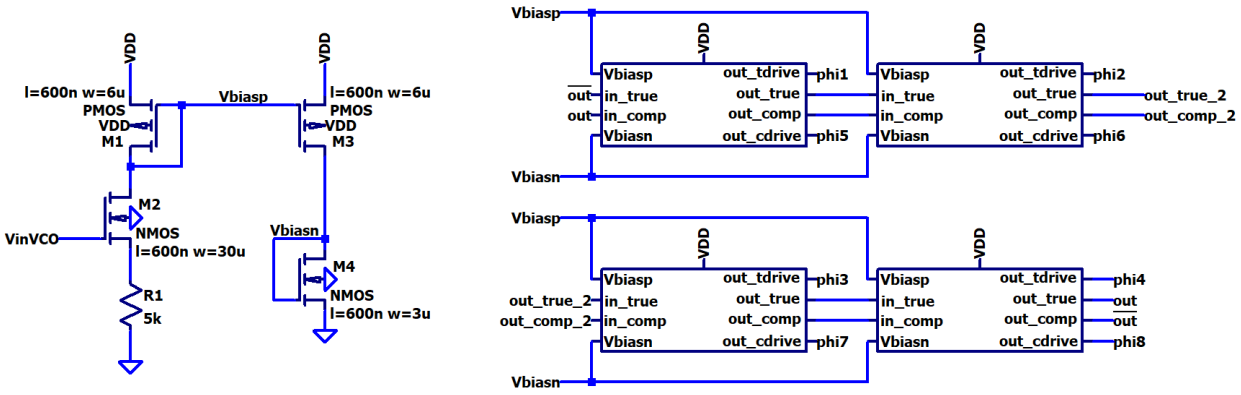

Figure 3: Self-Biased Voltage-Controlled Ring Oscillator for Generating Clock Signals

Figure 3 above shows the schematic view of the ring-oscillator topology used for generating K clock signals used in the design of the KD1S ADC. The delay element used to generate the phase-shift between successive clock signals is shown in figure 4 below. The delay element consists of a NAND gate as the first device in a cascade of inverting devices which also contains 3 regular CMOS inverters and a current-starved inverter (biased below by *Vbiasp* and *Vbiasn*).

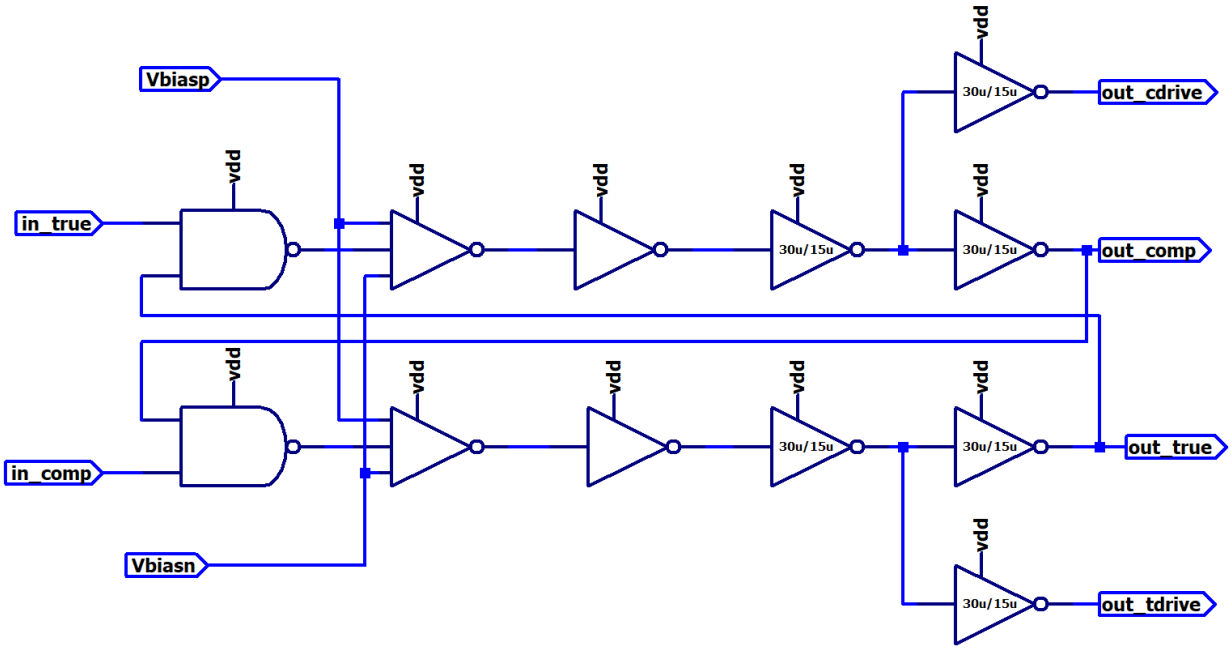

Figure 4: Voltage-Controlled Delay Element Used in Clock-Generating Ring Oscillator

The biasing voltages previously mentioned set the current flowing in the current-starved inverter. The delay through the current-starved inverter is directly affected by the biasing voltages, and the biasing voltages are set by VinVCO. Since VinVCO controls the delay through the current-starved

inverter, the oscillation frequency of the ring oscillator can be adjusted by adjusting VinVCO. This makes the design more robust since a range of oscillation frequencies are available by changing a single voltage input.

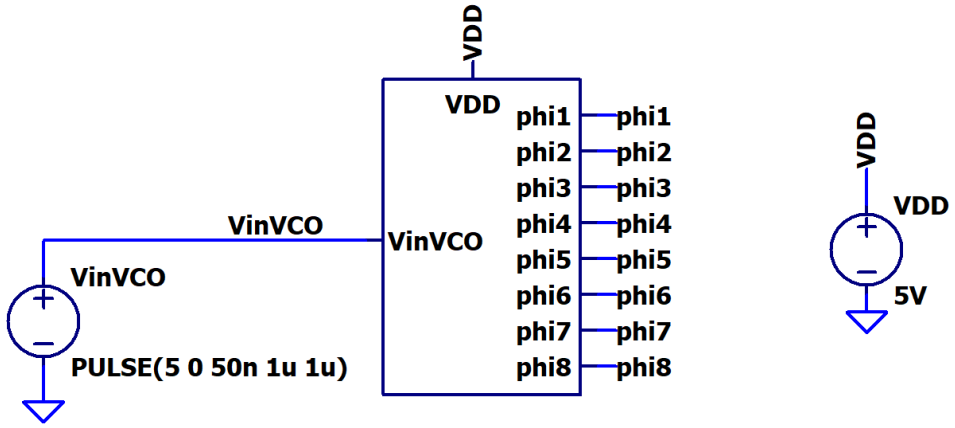

Figure 5: Clock Generator Symbol View in Test Schematic for VCO Gain

A symbol view for the clock generator circuit was created to test the clock generator's input-output relationship. For a DC voltage input, the 8 clock signals used to clock the 8 paths can be observed with nonoverlapping rise times. A slow ramp input is fed into the oscillator to measure the gain of the voltage-controlled oscillator. The gain is in units of Hz/V since an input signal yields an output frequency.

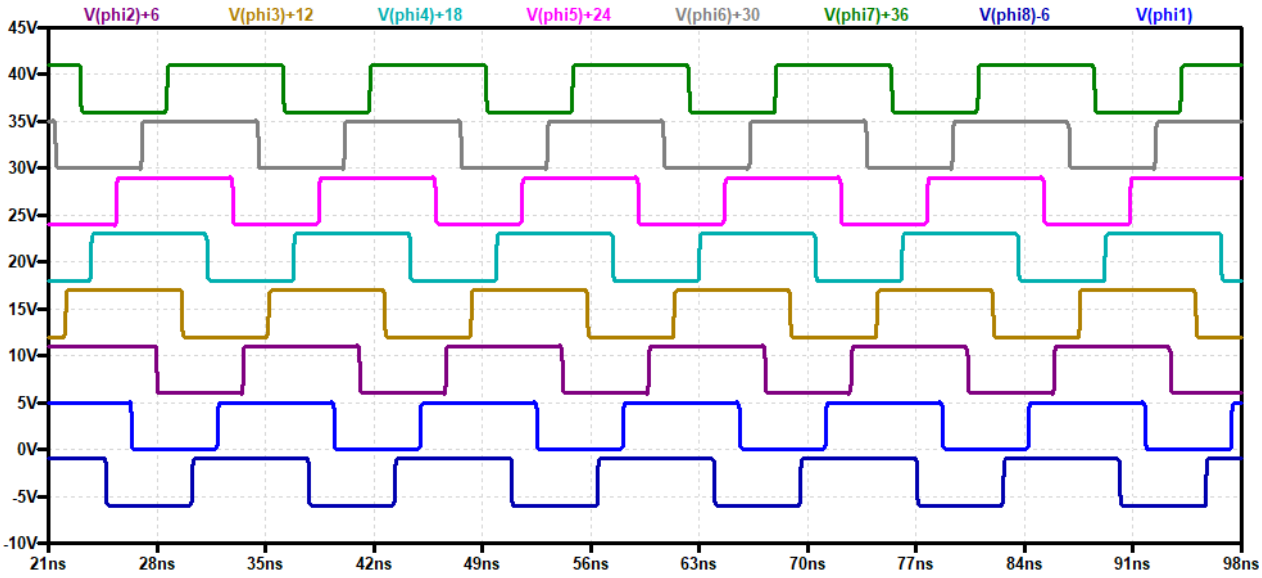

Figure 6: Clock Signals Generated to Clock 8 Feedback Paths for K=8

In figure 7 below, we can see have the frequency is adjustable for the oscillator as VinVCO is swept over the full power rail voltage range. Note that the frequency of oscillation is at a maximum when VinVCO is at a maximum. This is because maximizing VinVCO maximizes the gate-to-

source voltage of M2 in figure 3, increasing the current flowing in both branches of the current mirror, thereby decreasing the delay through the current-starved inverter. Note also that the oscillations stop around 750mV because M2 shuts off when VinVCO falls below the threshold voltage of the device. The decrease in frequency as VinVCO is linear because the resistor connected to M2's source linearizes the drain current in each branch of the biasing circuit.

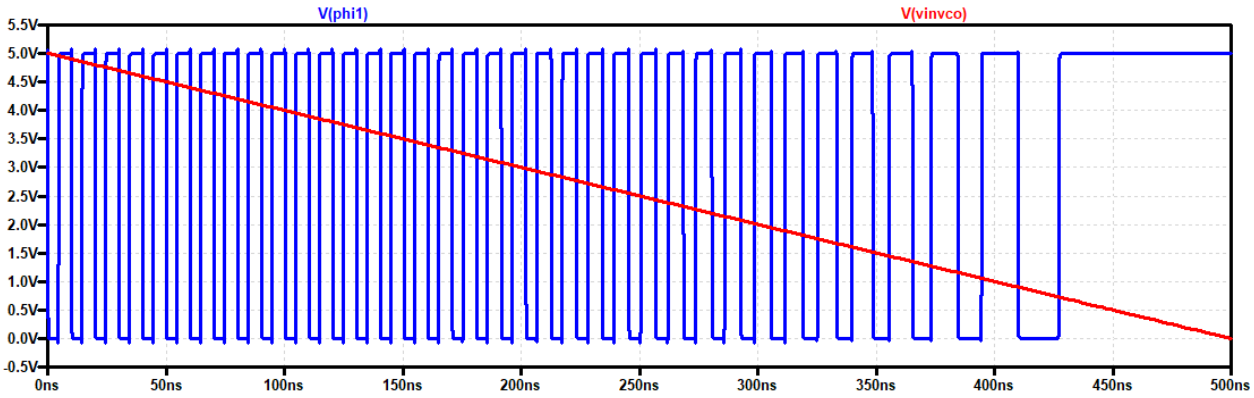

Figure 7: Simulation Results for Measuring Gain of VCO

The gain of the VCO can be measured by

$$K_{VCO} = \frac{f_{max} - f_{min}}{V_{max} - V_{min}} = \frac{101MHz - 30.4MHz}{5V - 0.7V} = 16.5MHz/V$$

The equation above indicates that we can obtain a sampling frequency (K=1) as high as 100MHz if VinVCO is connected to VDD, and as low as 30.4MHz if VinVCO is set to a voltage just larger than the threshold voltage of an NMOS in the C5 process, though it is probably not a good idea to bias the input device so near to the threshold voltage, as any slight decrease in that bias voltage could result in oscillations stopping and ruin the operation of the entire circuit. It is best to operate well above the device threshold voltage. Nonetheless, the robustness of the oscillator circuit is demonstrated.

Figure 8 on the page to follow shows the timing window when clock signals phi_n, phi_{n+1}, *and* phi_{n+6} are all high at the same time. This is the window created when clocking switches (or practically, transmission gates) in the feedback path, controlling how long the comparator output signal is fed back. Trouble arises, however, as a result of the window overlap, shown in figure 10.

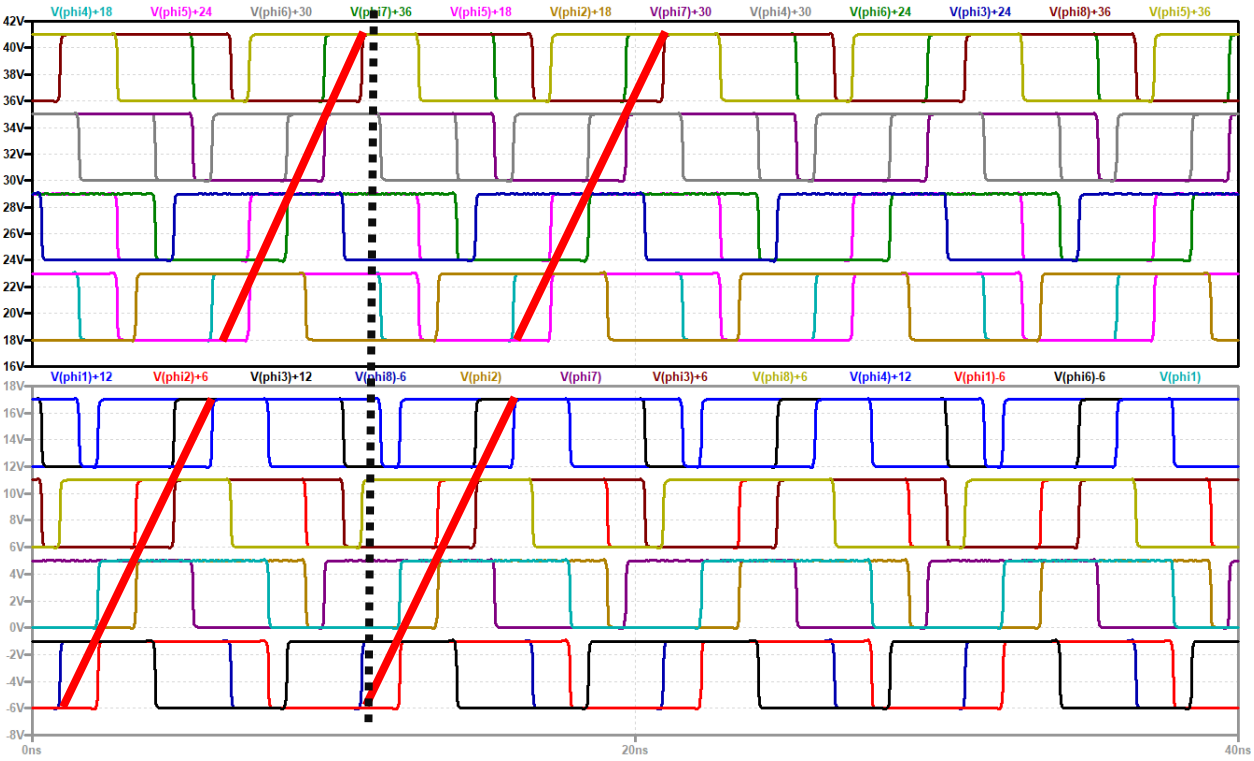

Figure 8: Clock Signal Timing Concerns When Controlling Feedback Signals

Figure 9 shows two feedback paths being clocked for *Vfb1, Vfb2* to be fed back to the integrator op-amp's minus terminal. Figure 10 shows a closer view of the clock signals, where *phi1* is clocking the comparator in the top feedback path and *phi2* is clocking the comparator in the bottom feedback path in figure 9.

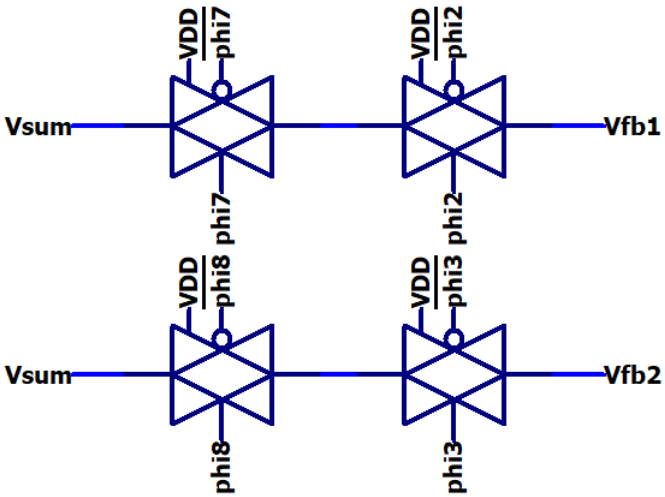

Figure 9: Transmission Gate Feedback Signal Control Paths

The window when all three of the clock signals (the comparator clock and the two transmission gates in any given feedback path) are high for a signal to be fed back is nearly 2 ns long, as can be seen from figure 10 below. During this time, the output of the comparator feeds through the two series-connected transmission gates and into the sum node (the minus terminal of the integrator's op-amp) which is common to all 8 feedback paths. However, note that in the figure, when *phi3* (pink trace) goes high, there are two feedback paths passing a signal through at the same time for around 0.7 ns. This is not good since the feedback could potentially (if both feedback signals are high or low) be too large, which damages the performance of the circuit. Ideally, we only one want one feedback path feeding back any signal at any given time to yield an effective sampling frequency of $K*f_s$ or in this case 8 times larger than the sampling frequency.

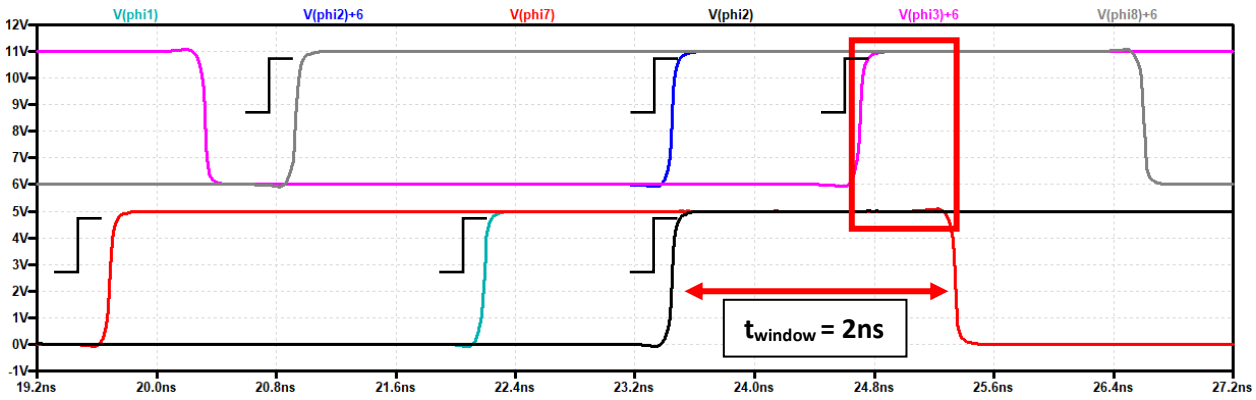

Figure 10: Timing Window Overlap Between Two Feedback Paths Using Clocked TGs

The problem itself arises as a result of the waveforms generated by the clock generator circuit having duty cycles greater than 50%. If the signals had 50% duty cycle, we would see no window overlap whatsoever, and the rising edge of the start of the next path feeding back would coincide in time with the falling edge of the end of the previous path feeding back. Attempts were made to modify the clock generator circuit to generate clock signals with 50% duty cycle, but to no avail. Adding logic, more inversions, and changing transistor widths in the inverters, the NAND gates, and the current starved inverters modified the delay stage delay time, but did not change the duty cycle of the signals significantly in any case.

If the clock generator were to work ideally, the first four clock signals generated and the last four clock signals generated would be complements of each other in the following manner: *phi1* is the complement of *phi5*, *phi2* is the complement of *phi6*, etc. This is not the case since the duty cycles of the signals are not 50%. However, the complements of *phi1, phi2, … phi8* can be generated using inverters. This way, instead of clocking a comparator/feedback path with *phi1*, *phi2, phi7,* the path can be clocked with *phi1, phi2, phi3's complement* to achieve no overlap, as can be seen in figure 11 below.

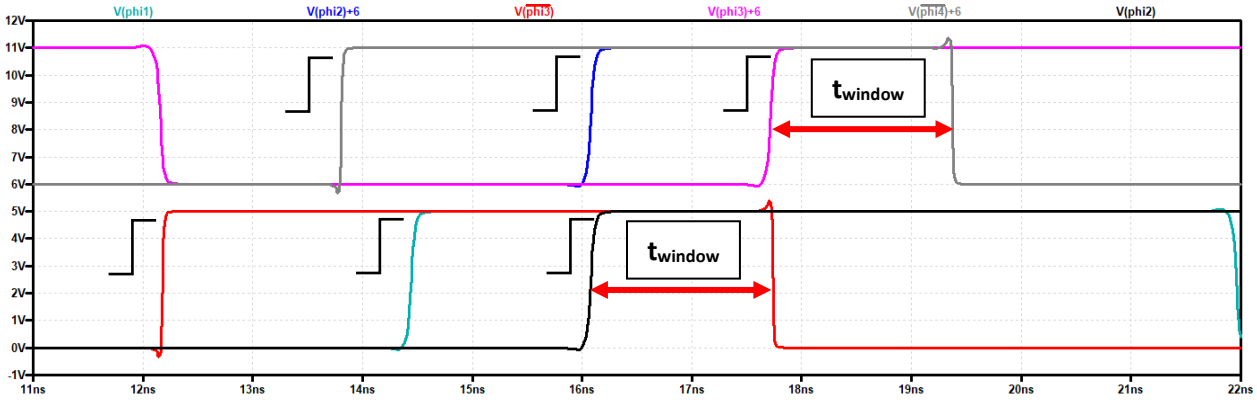

Figure 11: Timing Window Overlap Eliminated by Improved Clocking Scheme

III. Comparator

Two different comparator topologies were tested in the design of the KD1S modulator, shown in figures 12 and 13 below. For a better view of the comparator topology, the clock buffer transistors and SR latch were omitted from the figures, but each comparator is clocked by a buffered clock signal and connected out to an SR latch (latch inputs labeled on schematics: S, R).

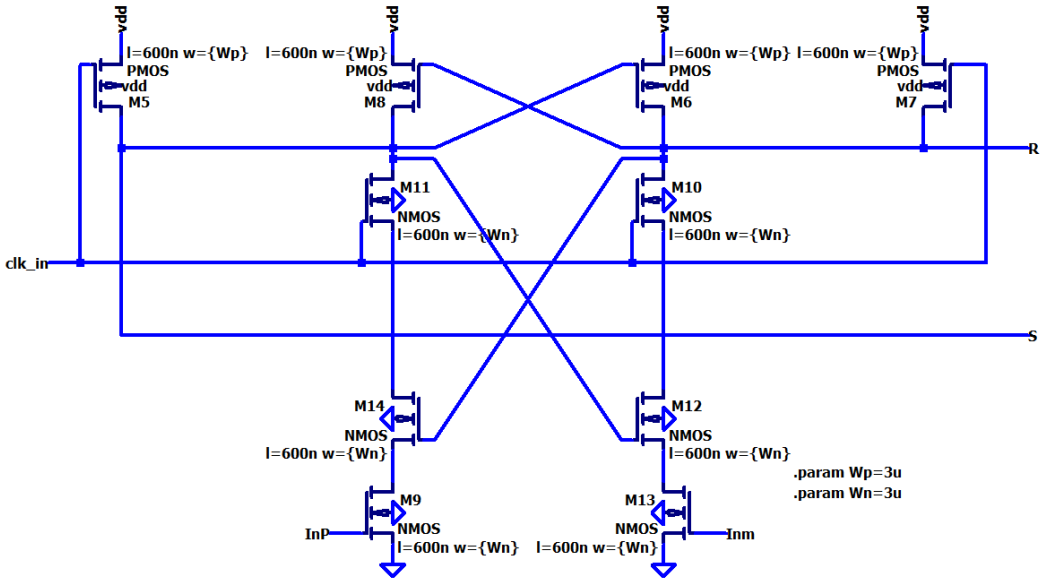

Figure 12: Low Power, Memoryless Clocked Comparator for Reduced Kickback Noise

The comparator in figure 12 above has both benefits and drawbacks compared to a simple sense amplifier topology. Since the clock signal pulls nodes R and S up through devices M7 and M5 when clock is low, the circuit has no memory and refreshes on every clock cycle. This is important for the comparator to consistently make correct decisions at high speeds. The outputs of the comparator are also isolated from clock, so feedthrough and kickback noise are minimized.

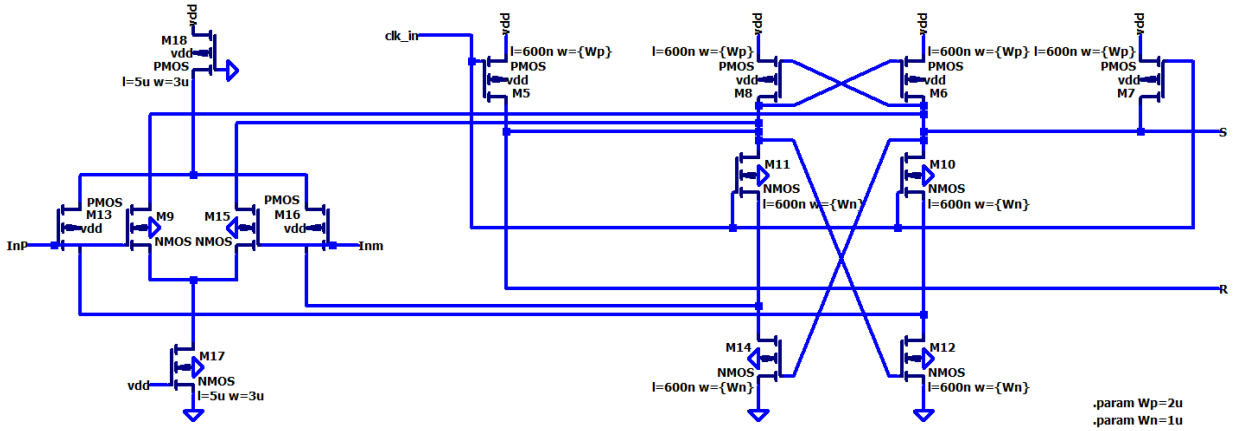

Figure 13: An Alternative Clocked Comparator Topology with Wide Input Range and High Sensitivity

An alternative clocked comparator topology was also explored for the comparator used in the K feedback paths. Figure 13 above shows a clocked comparator topology with wider input swing since the input devices are isolated from the power supply rails by at least once device drain-to-source voltage. The previous topology has lower input range since the input nodes are only one VGS above ground. This means that if the input to the comparator goes below the NMOS threshold voltage the device will shut off and the comparator will not likely make the correct decision. Simulations proved to show that the wide-swing comparator of figure 13 is also much more sensitive to small changes in voltage than the first comparator. For this reason, it is better suited for the application of sensing the difference between the integrator output node (which only swings slightly) and the common-mode reference voltage. The SR latch connected to the output of the comparators is shown in figure 14 below.

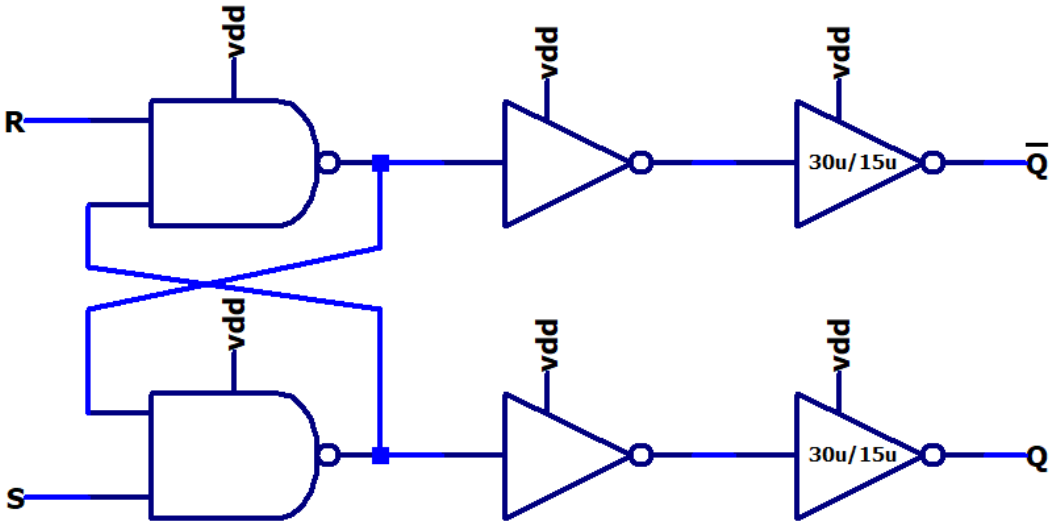

Figure 14: Cross-Coupled NAND SR Latch and Driver Logic on Comparator Output

IV. Amplifier

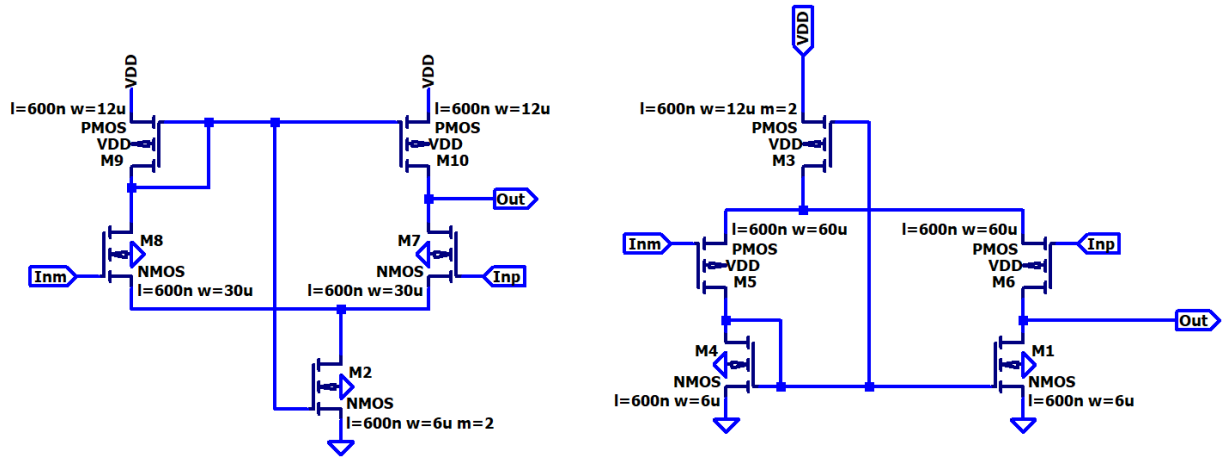

Figure 15: Wide-Swing Self-Biased Differential Amplifier used in Integrator

The amplifier used in the integrator is a wide-swing self-biased differential amplifier topology shown in figure 15 above. The gain of the amplifier as the plus input is swept from 0 to VDD and the minus input is kept constant at VDD/2 is plotted in the figure below. We can see that the gain of the amplifier is 25 at its peak from the black trace, the derivative of the output (flipped since the amplifier is inverting). Assuming that the integrator's summing node is regulated properly, the amplifier will operate with a gain of 25.

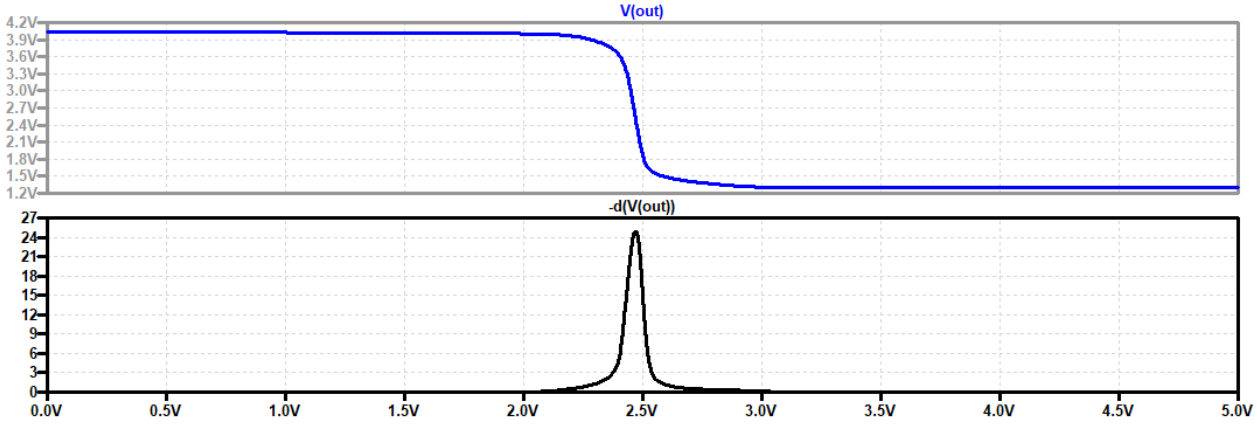

Figure 16: Simulation Results Showing Gain of Amplifier Used in Integrator

The integrator was designed with a self-biased amplifier so that less hardware could be used in the integrator's layout. An externally biased diff-amp was determined to be unnecessary, since the self-biased diff-amp provides sufficient gain to make the gain error term small. The gain error term is given by

$$\varepsilon_{gain} = G_I \cdot \frac{1}{AOL(f)}$$

where G_I is the integrator gain and *AOL(f)* is the open-loop gain of the amplifier, in this case 25. Since the gain error and the amplifier open-loop gain are inversely proportional, assuming the selected R,C values for the integrator are chosen to be sufficient, the gain error is minimized by the amplifier's gain, and an amplifier with higher gain will only slightly improve the gain error term. It is therefore sufficient to use a simple amplifier with limited hardware such as the amplifier in figure 15 used in this design.

Analysis of Design and Performance of a ΔΣ Modulator

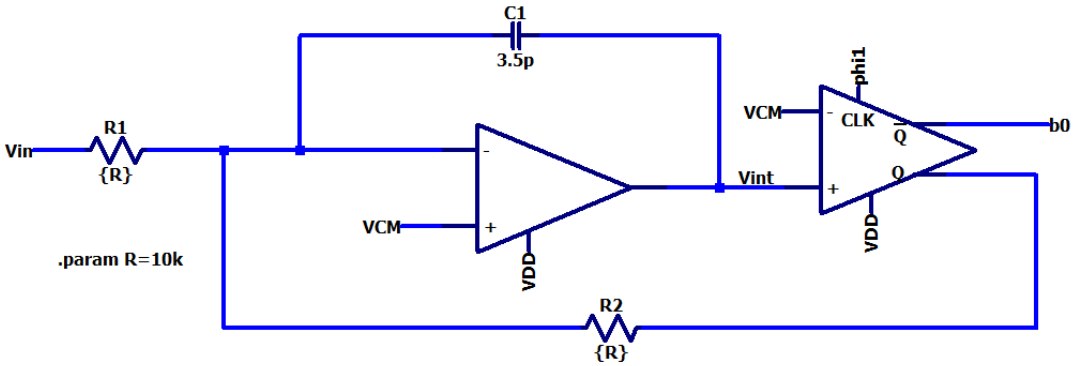

Figure 17: Schematic of First-Order Delta-Sigma Noise Shaping (NS) Modulator

Figure 17 shows the schematic implementation of the first-order delta-sigma noise shaping modulator used as the base design for building up to the final design, which uses $K_{path} = 8$. The design above uses the amplifier, clock generator, and comparator designs discussed previously in detail. Understanding the operation of the single-path delta-sigma modulator is integral to the understanding of the KD1S modulator designed for improved SNR and increased sampling rate. The discussion to follow details the operation of the circuit of figure 17 above.

The input signal is fed through the integrator's input resistor R1. As the input signal increases, it injects charge into the minus input of the integrator's op-amp. This charge injection forces the voltage across the capacitor C1 to increase. Since the op-amp wants to hold its minus input at the same potential as its plus input, the voltage on the integrator output will go down. The opposite happens when the input signal decreases (integrator output goes up). The integrator output is compared against the common mode voltage of VDD/2 (in the C5 process, 2.5V) and the result of this comparison is either a logic 1 (5V) or a logic 0 (0V). If the input signal is rising or above VCM, the signal fed back will be a logic 0. If the input signal is falling or below VCM, the signal fed back will be a logic 1. This regulation and feedback operation is what drives the sense operation carried out by the modulator. Figure 18 on the page to follow shows the transient simulation results of the single-path modulator.

Note that the signal plotted in the figure V(b0) is the complement of the signal that is fed back. This is because if charge is being injected into the minus terminal of the amplifier, we want to feed back a signal that will steal charge from that node (or feed back a logic 0), but we also want to plot the output signal which best represents the input signal. For this reason, V(b0) is plotted, but the complement of V(b0) is fed back.

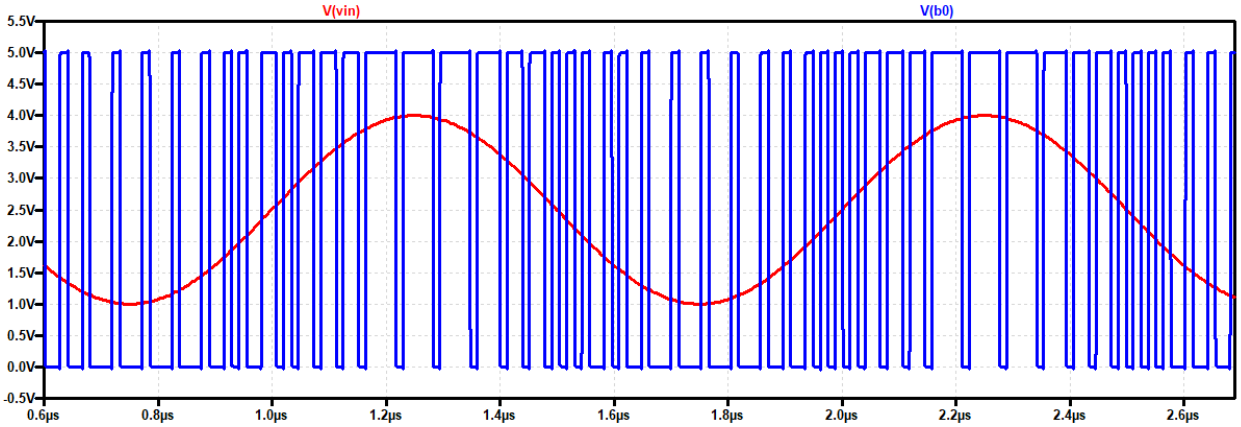

Figure 18: Transient Simulation Results of 1st-Order Delta-Sigma NS Modulator

From the plot above, we can see that the delta-sigma modulator is working as expected. Note that when the input signal is high, the comparator outputs are high most of the time. When the output signal is low, the comparator outputs are low most of the time. When the input signal is near the common-mode voltage, the comparator output is swinging back and forth from rail to rail trying to average to the common-mode voltage. This is proper delta-sigma action and the system SNR and SNDR can be obtained from MATLAB. In the MATLAB simulation results to follow, as specified by the legend, the green will represent the input signal tone. **The red points will specify noise in the desired bandwidth, and the blue will represent noise outside the bandwidth.** The data to follow was obtained using f_s=77MHz, BW=3.22MHz.

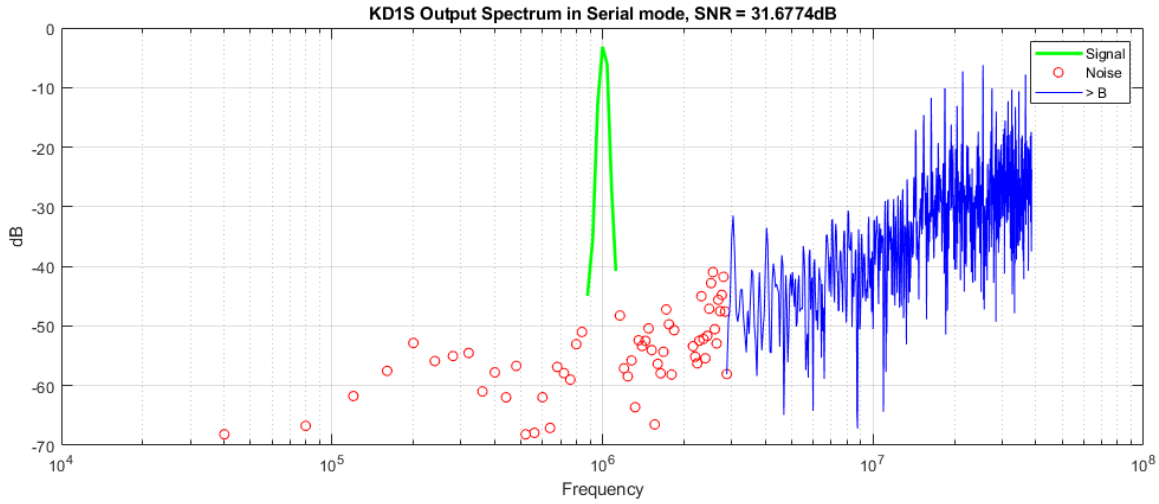

Figure 19: Single-Path KD1S Output Spectrum in Serial (and Parallel) Mode, Measuring SNR

Final Design Performance and Simulation Results

I. Four-Path 2nd-Order KD1S Modulator

Kpath	Order	F,osc (fs,new=K*F,osc)	Bandwidth	Serial SNR	Serial Neff	Parallel SNR	Parallel Neff	Serial SNDR	Parallel SNDR
4	2	71MHz	4.46MHz	37.0dB	5.86	30.4dB	4.75	32.4dB	29.3dB
4	2	71MHz	2.23MHz	47.3dB	7.56	42.9dB	6.82	43.8dB	40.7dB
4-Path 2nd-Order CT KD1S Average Power Consumption							48.5mW		

The first topology analyzed in this section will be the 2nd-order four-path feedback controlled KD1S modulator whose schematic is seen below. The clock circuitry here is omitted for a better view of the modulator circuitry.

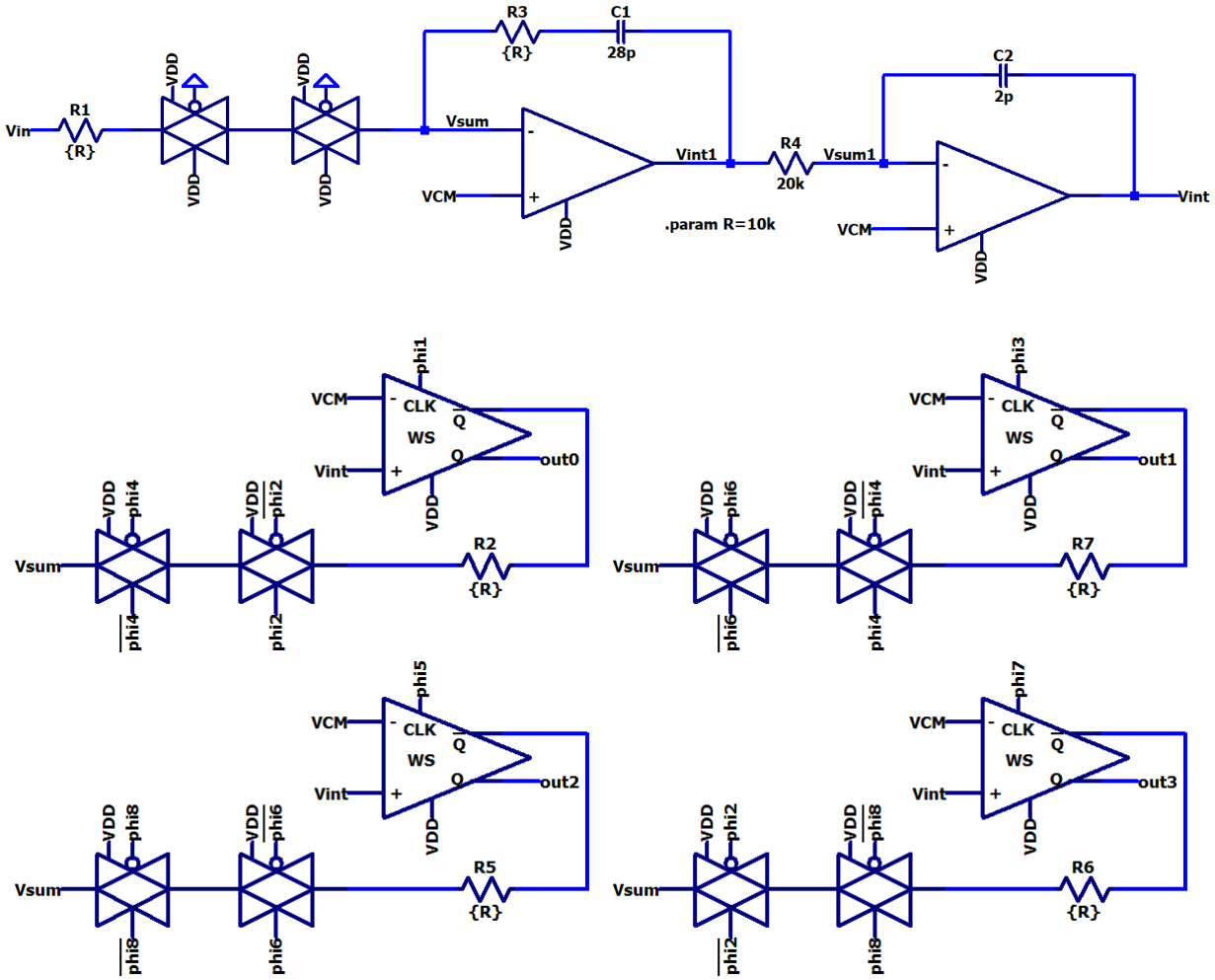

Figure 20: Schematic of K=4 2nd-Order KD1S Modulator, Clock Generation Circuitry Omitted

The ideal SNR for a second-order noise-shaping modulator is given by

$$SNR_{ideal} = 6.02N + 1.76 - 12.9 + 50logK$$

where $K = K_{avg} * K_{path}$ = OSR. Simulations were run for bandwidths of 4.46MHz and 2.23MHz corresponding to a K_{path} of 4 and an oscillator frequency of 71MHz. Since N=1 for our modulators, we can rewrite the equation as

$$SNR_{ideal} = 50logK - 5.12$$

For an OSR of 64, our expected SNR is then

$$\boxed{SNR_{ideal} = 50\log(64) - 5.12 = 85.2dB}$$

and for OSR of 32, our expected SNR is

$$\boxed{SNR_{ideal} = 50\log(32) - 5.12 = 70.1dB}$$

The ideal effective number of bits can then be calculated by

$$N_{eff} = \frac{SNR_{ideal} - 1.76}{6.02}$$

For OSR of 64,

$$\boxed{N_{eff} = \frac{85.2 - 1.76}{6.02} = 13.9\ bits}$$

For OSR of 32,

$$\boxed{N_{eff} = \frac{70.1 - 1.76}{6.02} = 11.4\ bits}$$

Using MATLAB, the actual data was obtained and can be compared against the hand-calculated ideal or expected data. We can see from the plots that our ideal SNR and Neff calculations do not match the simulated values obtained from MATLAB. This is because there are artifacts and other effects acting to decrease the SNR which are not taken into account in the ideal SNR equation. The MATLAB plots were obtained by extracting data from LTspice after running a transient simulation for 25 complete cycles. This large number of cycles assures that the data obtained is accurate and allows MATLAB to average a large number of points.

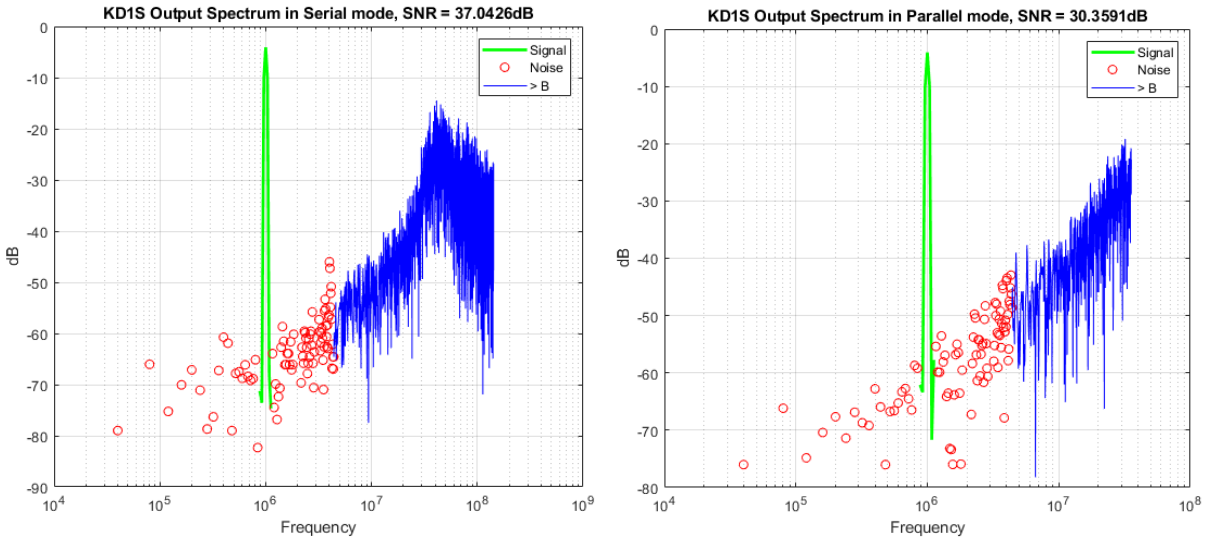

Figure 21: SNR in Serial and Parallel Mode for 4-Path 2nd-Order Modulator, OSR = 32

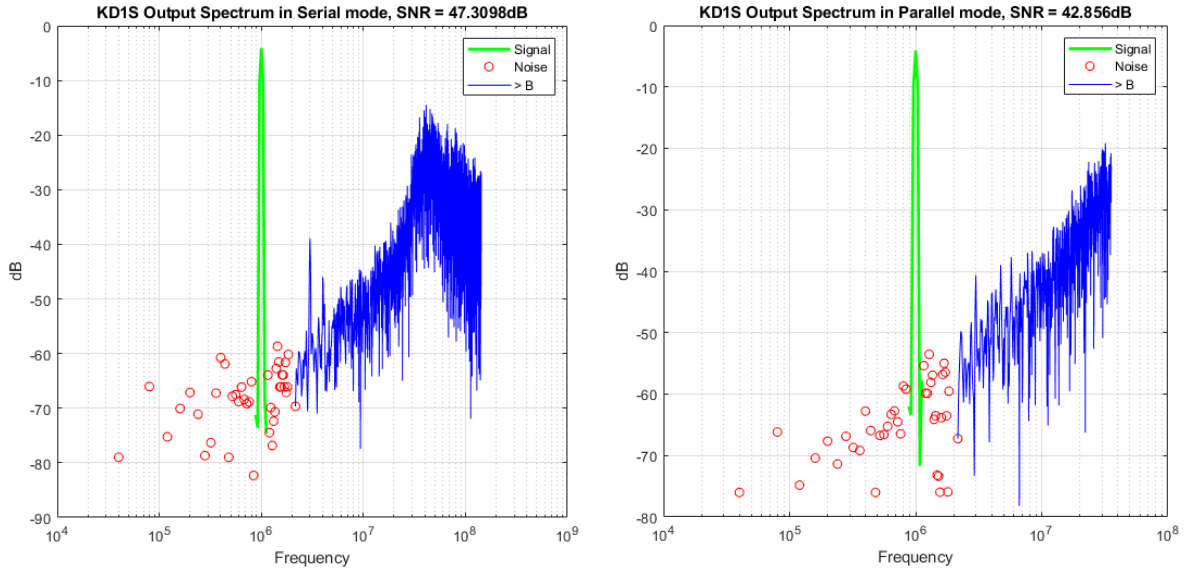

Figure 22: SNR in Serial and Parallel Mode for 4-Path 2nd-Order Modulator, OSR = 64

Below are transient simulations for the 4-path 2nd-order modulator whose effective sampling frequency is 284MHz. These plots were obtained in LTspice and their data was extracted by MATLAB to produce the figures above for SNR calculations. We can see from the plots that the output tracks the input. There are five possible states for the output: no comparators are high, all comparators are high, one, two, or three of the comparators are high. The modulator acts to output whichever state best corresponds to the input on every rising edge of clock.

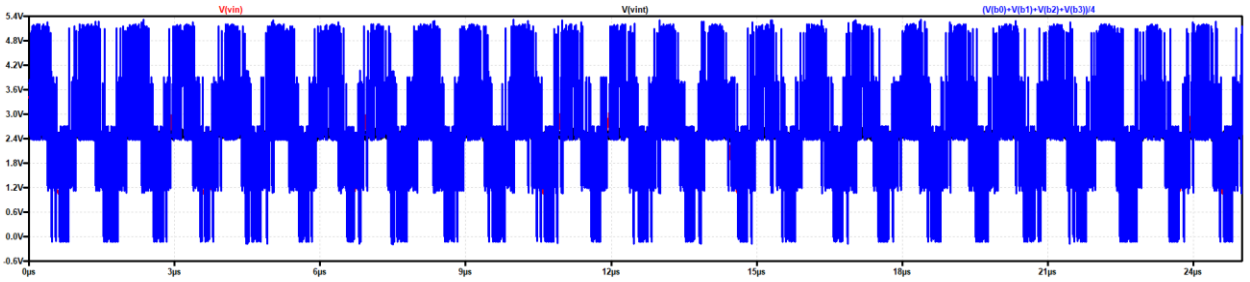

Figure 23: Transient Simulation of 4-Path 2nd-Order Modulator, Running for 25 Cycles

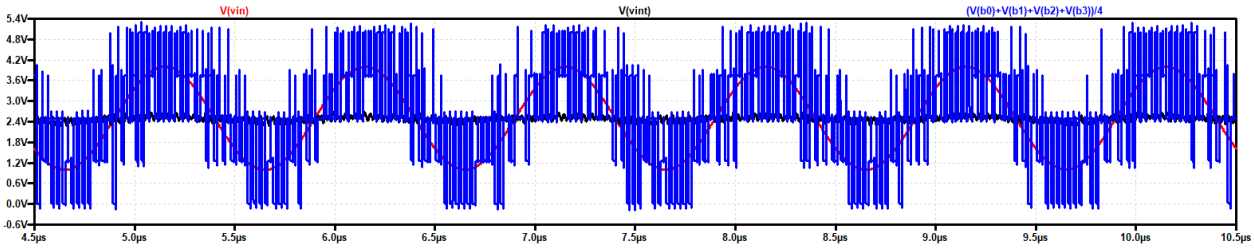

Figure 24: Transient Simulation of 4-Path 2nd-Order Modulator Zoomed-in on 6 Cycles

Figure 25 was generated to test for dead zones. There are high frequency spikes on many of the output pulses which are making it difficult to see the dead zones, but there are dead zones in the design. Since this design is second order, is far less likely that the feedback current into Vsum will be equal to the input current into Vsum, so there are less dead zones in this design than there are in the 8-path 1st-order design.

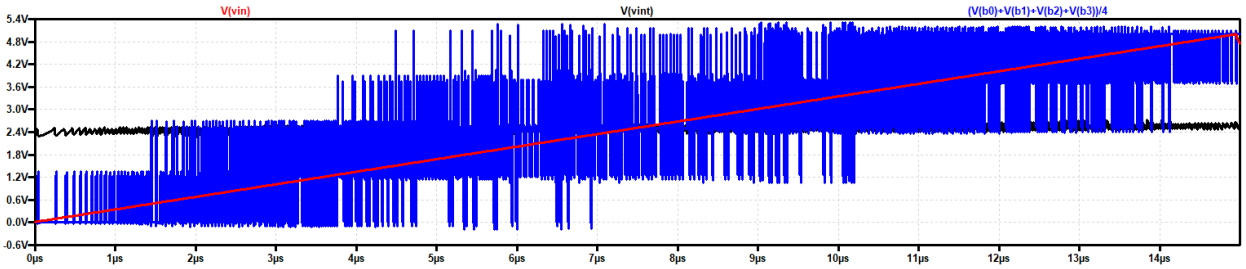

Figure 25: Transient Simulation of 4-Path 2nd-Order Modulator, Ramp Input

II. Eight-Path 1st-Order KD1S Modulator

Kpath	Order	F,osc (fs,new=K*F,osc)	Bandwidth	Serial SNR	Serial Neff	Parallel SNR	Parallel Neff	Serial SNDR	Parallel SNDR
8	1	71MHz	4.46MHz	40.1dB	6.49	30.2dB	4.72	38.0dB	29.0dB
8	1	71MHz	2.23MHz	44.5dB	7.10	44.5dB	7.10	41.9dB	39.5dB
8-Path 1st-Order CT KD1S Average Power Consumption							35.4mW		

The second topology analyzed in this section will be the 1st-order eight-path feedback controlled KD1S modulator whose schematic is seen below. Again, the clock circuitry here is omitted for a better view of the modulator circuitry.

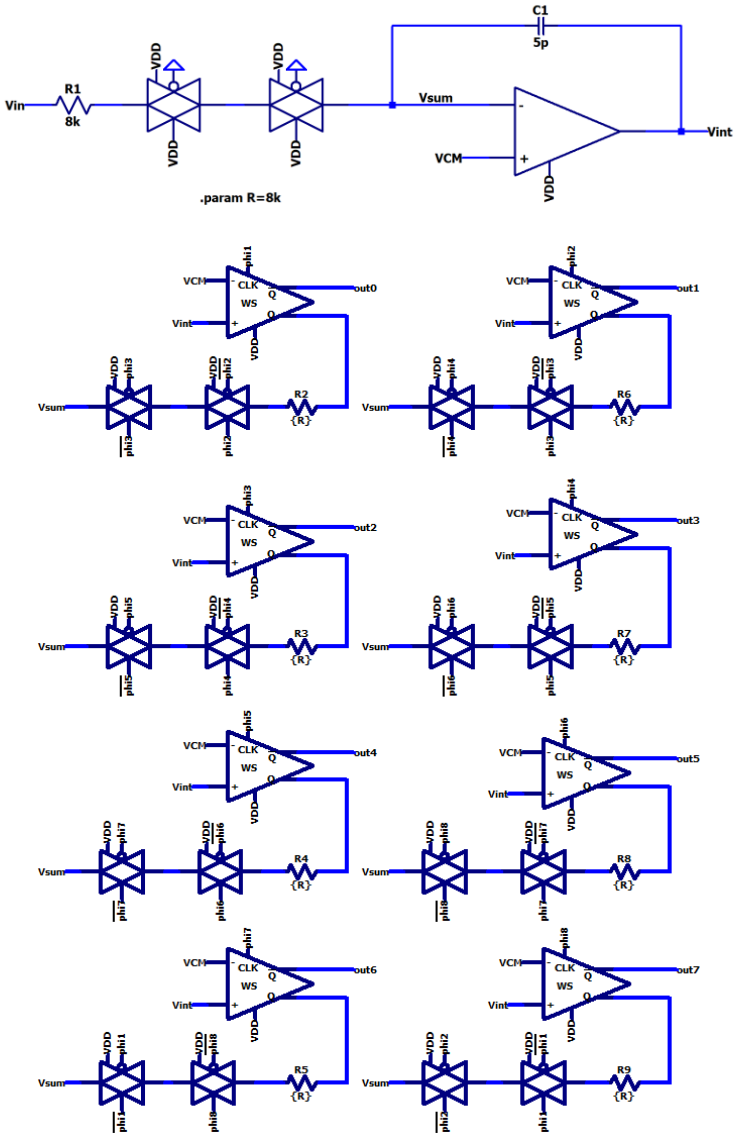

Figure 26: Schematic of K=8 1st-Order KD1S Modulator, Clock Generation Circuitry Omitted

The ideal SNR for a first-order noise-shaping modulator is given by

$$SNR_{ideal} = 6.02N + 1.76 - 5.17 + 30logK$$

where $K = K_{avg} * K_{path}$ = OSR. Simulations were run for bandwidths of 4.46MHz and 2.23MHz corresponding to a K_{path} of 8 and an oscillator frequency of 71MHz. Since N=1 for our modulators, we can rewrite the equation as

$$SNR_{ideal} = 30logK + 2.61$$

For an OSR of 128, our expected SNR is then

$$\boxed{SNR_{ideal} = 30\log(128) + 2.61 = 65.8dB}$$

and for OSR of 64, our expected SNR is

$$\boxed{SNR_{ideal} = 30\log(64) + 2.61 = 56.8dB}$$

The ideal effective number of bits can then be calculated by

$$N_{eff} = \frac{SNR_{ideal} - 1.76}{6.02}$$

For OSR of 128,

$$\boxed{N_{eff} = \frac{65.8 - 1.76}{6.02} = 10.6\ bits}$$

For OSR of 64,

$$\boxed{N_{eff} = \frac{56.8 - 1.76}{6.02} = 9.1\ bits}$$

Again using MATLAB, the actual data was obtained and can be compared against the hand-calculated ideal or expected data. Here again, we can see from the plots that our ideal SNR and Neff calculations do not match the simulated values obtained from MATLAB. These MATLAB plots were also obtained by extracting data from LTspice after running a transient simulation for 25 complete cycles.

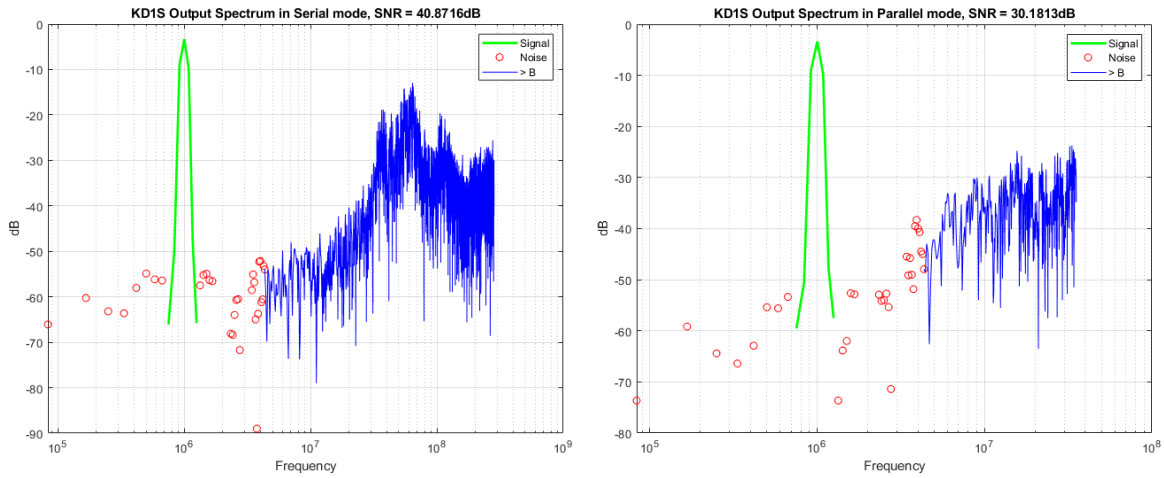

Figure 27: SNR in Serial and Parallel Mode for 8-Path 1st-Order Modulator, OSR = 64

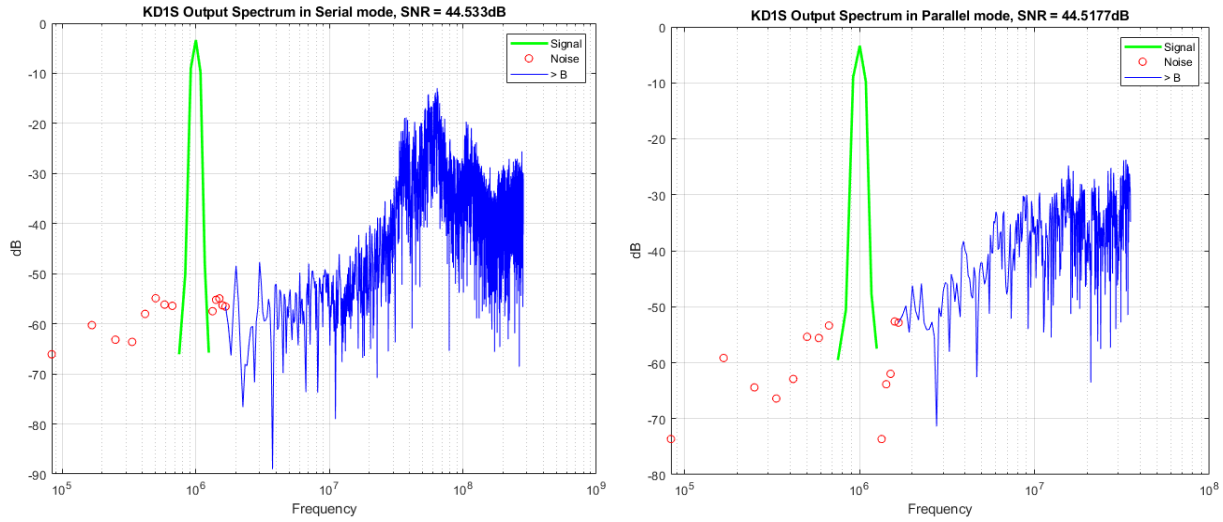

Figure 28: SNR in Serial and Parallel Mode for 8-Path 1st-Order Modulator, OSR = 128

Below are transient simulations for the 8-path 1st-order modulator whose effective sampling frequency is 568MHz. These plots were obtained in LTspice and their data was extracted by MATLAB to produce the figures above for SNR calculations. We can see again from the plots that the output tracks the input. There are 9 possible states for the output: no comparators are high, all comparators are high, one, two, three, four, five, six, or seven of the comparators are high.

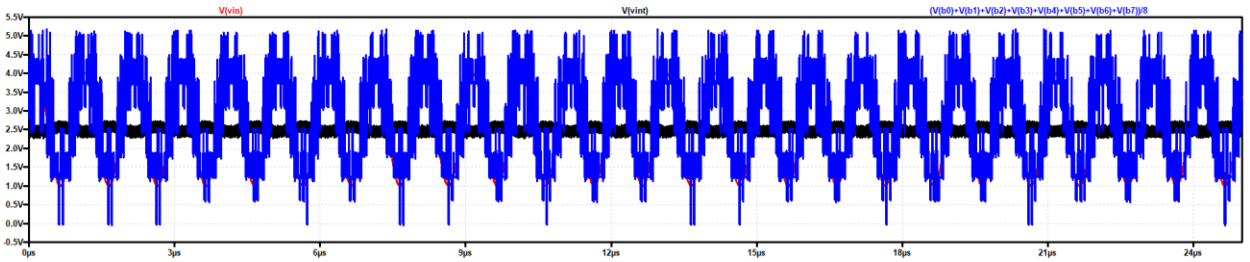

Figure 29: Transient Simulation of 8-Path 1st-Order Modulator, Running for 25 Cycles

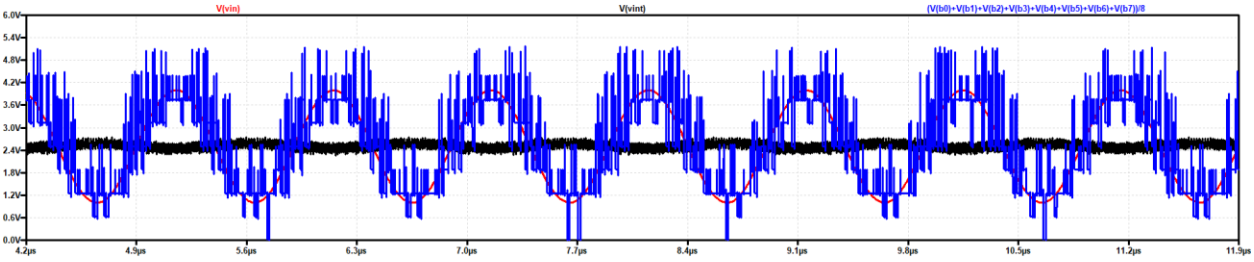

Figure 30: Transient Simulation of 8-Path 1st-Order Modulator Zoomed-in on 6 Cycles

The 1st-order topology is more susceptible to dead zones, especially when the input voltage is at a level which is around VDD/Kpath. This is because the input signal and the feedback signal are nearly equal in magnitude, causing the output code to be repeated and the modulator to stop modulating until the circuit works itself out of the dead zone. The 2nd-order topology which was seen previously is less susceptible to this issue.

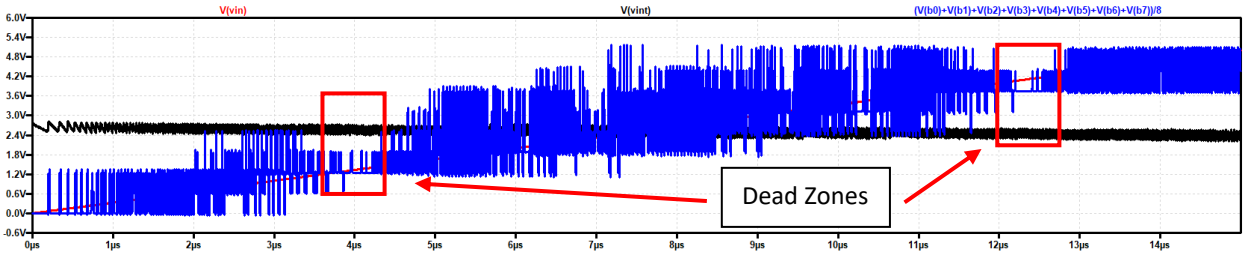

Figure 31: Transient Simulation of 8-Path 1st-Order Modulator, Ramp Input

Power Consumption

Perhaps one of the most important metrics by which the design should be compared to other designs is in the category of power consumption. The plots below show the two continuous time designs' average power consumption. Since it is quite constant as the modulator operates, the average value can be taken after only a small number of cycles. The average power consumed by the continuous time 4-path 2nd-order design is 48.5mW, and the average power consumed by the 8-path 1st-order design is 35.4mW. The most power-hungry portion of either design is the amplifier, which is why the increase in order increases the power by over 30%. The addition of a second integrator increases SNR, but also increases power consumption.

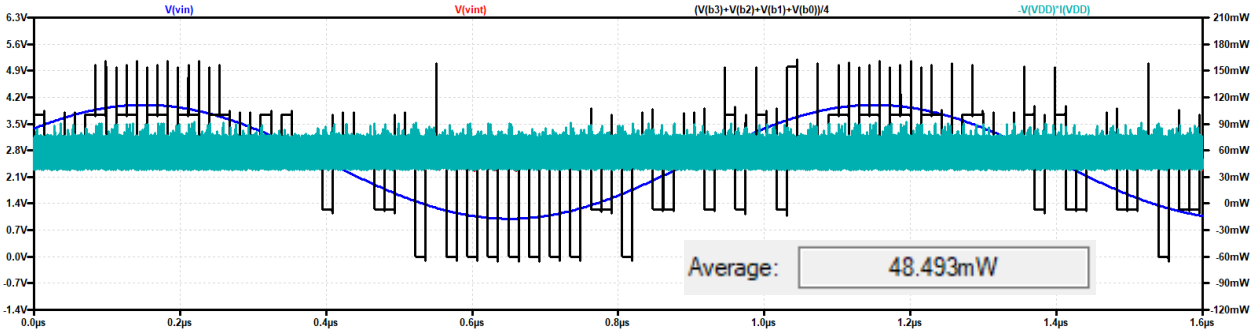

Figure 32: 4-Path 2nd-Order KD1S Power Consumption Over One Cycle

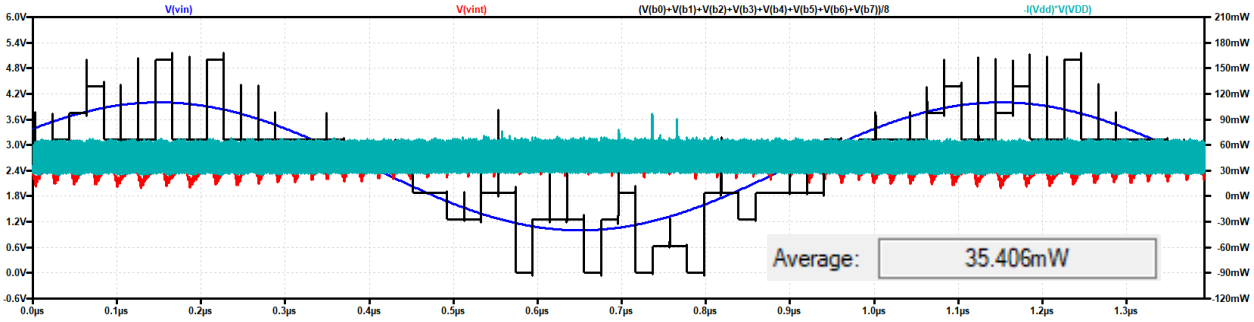

Figure 33: 8-Path 1st-Order KD1S Power Consumption Over One Cycle

Compared against the discrete time 8-path 1st-order modulator, the two continuous time designs consume less power, but do not have as high of an SNR or SNDR. The discrete time topology uses a 200MHz clock generator, and the power burned up in the switched capacitors likely accounts for the difference in power between the continuous time and discrete time topologies.

Summary

The 4-path 2nd-order KD1S modulator design outperformed the 8-path 1st-order modulator design. The second order modulator pushes more noise to higher frequencies leaving less noise behind in the bandwidth of interest, resulting in better SNR. The design can be characterized by the following metrics:

4-Path 2nd-Order KD1S Modulator

- Sampled at 284MHz (71MHz * 4 Paths)
- OSR = 32
    - SNR
        - Serial = 37.0dB, Neff = 5.86
        - Parallel = 30.4dB, Neff = 4.75
    - SNDR
        - Serial = 32.4dB
        - Parallel = 29.3dB
- OSR = 64
    - SNR
        - Serial = 47.3dB, Neff = 7.56
        - Parallel = 42.9dB, Neff = 6.82
    - SNDR
        - Serial = 43.8dB
        - Parallel = 40.7dB
- Power Consumption
    - Average power consumed by design = 48.5mW

Having four paths with more time to feed signal back and less dead zones due to the second integration, on top of more noise being pushed to higher frequencies, are the overall reasons why this topology outperformed the 8-path 1st-order topology. The design consists of a wide-swing differential amplifier used for an op-amp in the integrators, wide-swing comparators with high-sensitivity and high-speed, a ring-oscillator driven clock generator circuit with voltage controlled oscillation frequency, and other logic, transmission gates, and inverters used to control the feedback timing and amount of signal fed back.

The eight-path topology would seem to yield higher SNR due to the higher sampling frequency, but the second-order noise shaping is a powerful tool to boost SNR, so the second-order design clocked at a slower sampling frequency outperforms the converter whose sampling frequency is twice as fast. The 8-path design can be characterized by the following metrics:

8-Path 1st-Order KD1S Modulator

- Sampled at 568MHz (71MHz * 8 Paths)
- OSR = 64
    - SNR
        - Serial = 40.1dB, Neff = 6.49
        - Parallel = 30.2dB, Neff = 4.72
    - SNDR
        - Serial = 38.0dB
        - Parallel = 29.0dB
- OSR = 128
    - SNR
        - Serial = 44.5dB, Neff = 7.10
        - Parallel = 44.5dB, Neff = 7.10
    - SNDR
        - Serial = 41.9dB
        - Parallel = 39.5dB
- Power Consumption
    - Average power consumed by design = 35.4mW

Future Work and Improvements

There are several areas where the design of the ADC detailed in this report can be improved. ADCs in modern CMOS process using the same KD1S topology have achieved SNRs above 70dB corresponding to a resolution of 12 bits, so there is plenty of room for improvement. The key areas where improvements can be made are in power consumption, clock generator duty cycle, and optimization of the design in terms of R and C values.

- **Power Consumption:** Many of the inverters in the design were made with wide W devices to ensure that they would sink the required current at any given time and have no issues driving any capacitive loads. However, the design could likely be optimized such that these inverters would be made small enough that their device drain currents would significantly decrease but the circuits would still work properly. The integrator's amplifier could also be improved to consume less power, but at the cost of speed. The benefit of the topology used in these designs was the speed of the amplifier, which we would lose if we went for an amplifier with less power consumption.
- **Clock Generator Duty Cycle:** In order for the design to work properly, a high-performing clock generator circuit is certainly of the essence. As was seen in the section above regarding the clock generator, a clever clocking scheme was required

in order to produce the best results. This scheme also required one inverter for each clock signal, which adds 16 more devices to the clock generator and increases layout size and power consumption. The ideal clock generator would generate clock signals with 50% duty cycle so that the clever clocking scheme is not necessary and the inverse of phi1 is phi5, the inverse of phi2 is phi6, and so on. There would be no need to further invert any of these signals because their complements are also being generated as other clock signals. The reduction in power and layout space would be minimal, but a clock generator with a 50% duty cycle could be expanded to perhaps use 16 paths and achieve an even higher SNR and a higher effective number of bits.

- **RC Value Optimization:** RC values were chosen initially based on the sampling frequency of the given topology. For example, if the clock frequency had a period of T_{clk} for a given topology, the RC values were chosen to be at least 5 times the period. For the four-path topology, RC is 5*4**fosc*, and for the eight-path topology, RC is 5*8**fosc*. These RC values were tested but noted to not be suited for optimal performance. The R value was left fixed, but the C value was varied based on observation of what was happening at the integrator output. If the integrator output was swinging too much, the capacitance value was increased. If the integrator output was not swinging enough, the capacitance value was decreased. Once satisfying results were obtained, the RC values were left alone. It is certainly possible that continuing with this method would result in even better results.