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ECG 720: Advanced Analog IC Design

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High-Speed Transimpedance Amplifier (TIA) Design

The Analog Front-End discussed in this report was designed to convert current from an APD (Avalanche Photodiode) into an output voltage. Below is a summary of the performance of the TIA.

Summary of TIA Performance

Low Frequency Gain (in dB)	110.14 dB	**Low Frequency Gain (in Ω)**	321.5 kΩ

APD Capacitance	**None**	**100fF**	**200fF**	**300fF**	**400fF**	**500fF**
Bandwidth, 1pF Load	275 MHz	244 MHz	222 MHz	193 MHz	176 MHz	157 MHz
Input Referred Noise (Maximum)	$1.1pA/Hz^{1/2}$	$1.9pA/Hz^{1/2}$	$2.7pA/Hz^{1/2}$	$3.4pA/Hz^{1/2}$	$4.0pA/Hz^{1/2}$	$4.6pA/Hz^{1/2}$

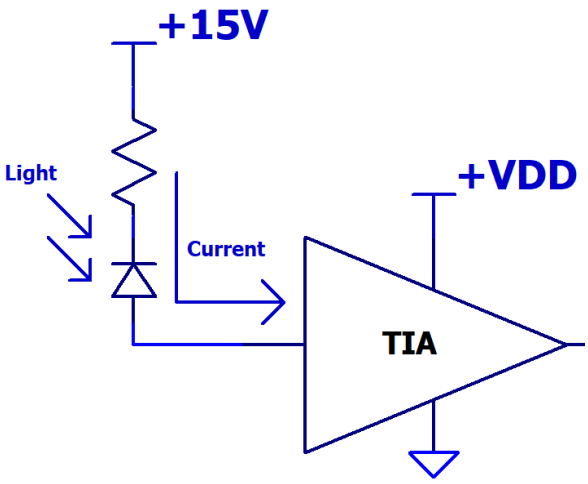
Input Current Pulse Amplitude (Pulse Frequency = 100MHz)	**1µA**	**2µA**	**3µA**	**4µA**	**5µA**
Output Slew Rate (1pF Load)	227mV/ns	551mV/ns	755mV/ns	834mV/ns	938mV/ns
Output Slew Rate (No Load)	288mV/ns	641mV/ns	877mV/ns	959mV/ns	1.05V/ns
Power Consumption (1pF Load)	24.1mW	25.7mW	27.2mW	28.6mW	29.9mW
Power Consumption (No Load)	22.9mW	23.0mW	23.1mW	23.1mW	23.2mW

Input Current Pulse Amplitude (Pulse Frequency = 100MHz)	1µA	2µA	3µA	4µA	5µA
Current Consumption (1pF Load)	4.22mA	4.5mA	4.8mA	5.0mA	5.2mA
Current Consumption (No Load)	4.0mA	4.01mA	4.02mA	4.03mA	4.04mA

APD input capacitance defaults to 100fF when not specified in the table above.
Input current defaults to 5µA when not specified in the table above.

The Off-Chip APD (Avalanche Photodiode)

An avalanche photodiode (APD) is a semiconductor electronic device which emits electrons and other free carriers when exposed to light, thereby converting light energy into electricity. APDs have a wide range of applications, including laser range-finding, long-range fiber-optic telecommunication, and particle physics. In order for APDs to be used in these applications, however, their output current must be converted to a respectable voltage using a transimpedance amplifier (TIA), an amplifier characterized by a current input, and a voltage output.



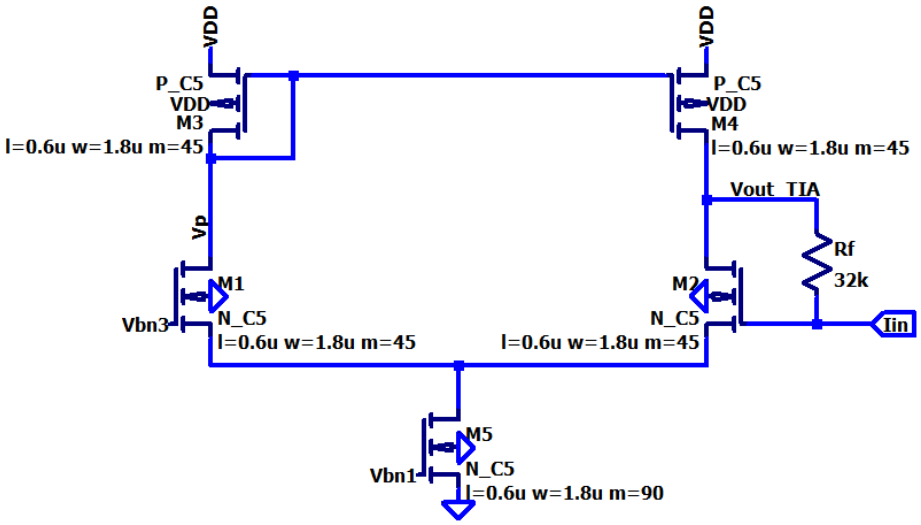
The APD is connected to the TIA as shown in the figure. In the C5 process, APDs break down between 13V and 14V, so a 15V supply is enough to cause the APD to break down. When light hits the APD, current is generated and flows into the TIA. Note that there is a resistor connected between the 15V supply and the cathode of the APD. If the APD breaks down at 13.5V, the excess 1.5V will be dropped across the resistor. If this resistor were to be removed, the anode of the APD (connected to the TIA input) would get pulled up and the biasing and overall performance of the TIA would be effected.

APD Connection Diagram to TIA

Aside from removing excess voltage, this resistor also contributes noise to the circuit. With this resistor in place, a noise current will be added to the APD current, and the sum of the noise current and APD current will flow into the TIA. This is a necessary tradeoff, however. If we were to omit the resistor, the biasing and performance issues could not be ignored. The resistor allows us to DC connect the diode's bias current to the input without the need of an AC coupling capacitor. Since a differential amplifier topology is used, the inputs are constantly fighting to try and remain at the same potential, so the value of this resistor need only be large enough that it is not comparable to the size of Rf. If the resistor was comparable in size to Rf, which in this case, is our input resistance, the gain of the amplifier would drop and performance would be damaged.

Designing the Analog Front-End (AFE)

Stage 1: NMOS Differential Amplifier TIA, Gain of 30kΩ



First Stage of Analog Front-End Design, TIA with Gain = 30kΩ

The differential amplifier topology was used to construct a TIA for the first stage of the analog front-end, with a gain of 30kΩ. The 32kΩ feedback resistor mainly controls the gain. Note that large multipliers were used on the devices, allowing them to source/sink more current. Though this first stage consumes a lot of current, and therefore consumes a lot of power, it is a necessary tradeoff to minimize the noise in the first stage of the front-end.

The open loop gain of the first stage can be calculated by

$$A_{OL} = \frac{v_{out,TIA}}{i_{in}} = g_{mn,M2} * Rf(r_{op,M4}//r_{on,M2}//Rf)$$

We can use the spice error log to obtain individual device transconductance and output resistance. Running the TIA alone with the biasing circuit connected, a fixed input current and a .op simulation, we can obtain the values necessary to compute the open loop and closed loop theoretical gains. Error log values can be found on the next page.

Name:	m4	m2
Model:	p_c5	n_c5
Id:	-9.72e-04	9.72e-04
Vgs:	-1.58e+00	1.40e+00
Vds:	-3.17e+00	1.40e+00
Vbs:	0.00e+00	-4.35e-01
Vth:	-9.20e-01	9.71e-01
Vdsat:	-5.05e-01	2.87e-01
Gm:	2.37e-03	4.10e-03
Gds:	7.62e-05	9.70e-05

Plugging in values from the spice error log, we obtain the following:

$$A_{OL} = 4.1mA/V * 32k\Omega(\frac{1}{76.2\mu} // \frac{1}{97.0\mu} // 32k\Omega)$$

$$A_{OL} = 4.1mA/V * 32k\Omega(4.891k\Omega)$$

$$\boxed{A_{OL} = 641.7k\Omega}$$

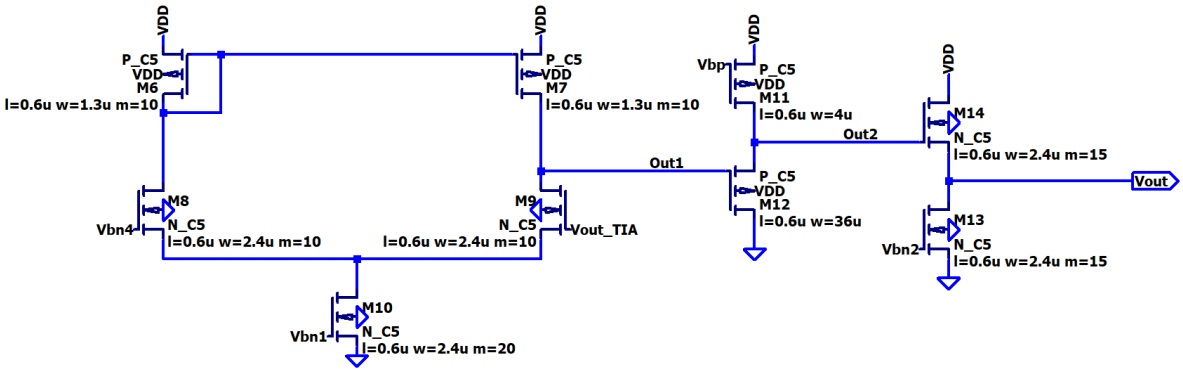
The closed loop gain can be calculated using the open loop gain and the feedback factor, β by

$$A_{CL} = \frac{A_{OL}}{1 + \beta A_{OL}}, \beta = \frac{1}{34k\Omega}$$

$$A_{CL} = \frac{641.7k\Omega}{1 + \frac{641.7k\Omega}{34k\Omega}}$$

$$\boxed{A_{CL} = 30.48k\Omega}$$

Stage 2: NMOS Differential Amplifier, PMOS/NMOS Follower Output Buffer



Second Stage of Analog Front-End Design, Voltage Amplifier with Output Buffer

A differential amplifier topology was used for the second stage as well. The second stage is a voltage amplifier with a gain of around 10.7 V/V. The differential amplifier in this stage has a gain of 14.6 V/V, but the combination of the PMOS and NMOS source followers on the output, which each have a gain less than 1, attenuate the output of the voltage amplifier, resulting in a final gain of 10.7 V/V.

The gain of the second stage can be calculated by

$$\frac{v_{out1}}{v_{out,TIA}} = g_{mn,M9} * (r_{op,M7} // r_{on,M9})$$

Again, we can use the spice error log to obtain individual device transconductance and output resistance.

Name:	m7	m9
Model:	p_c5	n_c5
Id:	-4.17e-04	4.17e-04
Vgs:	-2.32e+00	1.39e+00
Vds:	-3.70e+00	8.57e-01
Vbs:	0.00e+00	-4.39e-01
Vth:	-9.51e-01	8.84e-01
Vdsat:	-9.10e-01	3.28e-01
Gm:	4.68e-04	1.37e-03
Gds:	2.03e-05	7.47e-05

Plugging in values from the spice error log, we obtain the following:

$$\frac{v_{out1}}{v_{out,TIA}} = 1.37mA/V * (\frac{1}{20.3\mu} // \frac{1}{74.7\mu})$$

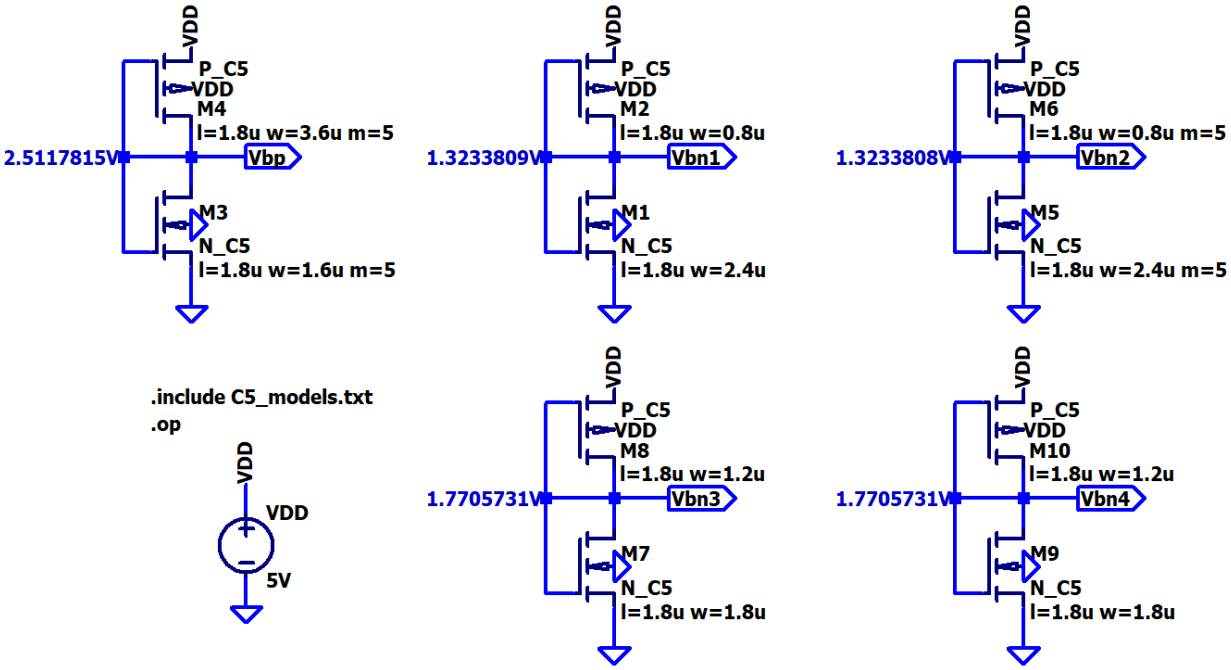
$$\boxed{\frac{v_{out1}}{v_{out,TIA}} = 14.33\ V/V}$$

Source followers were used on the output to drive high impedance loads. Prior to addition of the source followers on the output, with a load connected, the amplifier was very slow and unstable for input current pulses of 1µA or greater. The followers (particularly the NMOS source follower) are capable of sourcing/sinking large currents, and can easily drive capacitive loads (up to 1pF).

Design Tradeoffs

Category	Description of Tradeoff
MOSFET W/L Sizing	• With the exception of the biasing circuit, all MOSFETs were sized with minimum length. Widths were selected based on currents needed to provide gain in a particular stage. • **Pros:** Minimum L allows for high-speed operation. Wider W devices source/sink more current, are more tolerant to noise. • **Cons:** Minimum L limits gain.
Overdrive Voltage	• V_{ov} for NMOS devices was selected to be greater than 600mV (more than 10% of VDD). V_{ov} for source follower PMOS bias was selected to be 1.6V, turning the device on more, allowing it to sink more current. • **Pros:** Large overdrive voltage allows for high-speed operation. • **Cons:** Large overdrive voltage limits inherent device gain and overall gain of amplifier.
Diff-Amp Topology	• NMOS differential amplifier topology was used for TIA and for voltage amplifier stage. • **Pros:** Allows input voltages to move around so that biasing of the next stage is not affected. Can use large W devices in the diff amp to limit noise contributions, easy to manipulate gain. • **Cons:** Limited bandwidth in comparison to shunt-shunt feedback amplifier for TIA, series-shunt feedback amplifier for voltage amp.
Output Buffer	• Wide W output buffers capable of driving necessary loads. • **Pros:** Very fast slew rate in comparison with specification, very small difference in performance with varying loads. • **Cons:** Large layout size, giant increase in power consumption.
Large Multipliers in TIA	• Large multipliers were used to increase the widths of devices in the TIA, which is the first stage of the AFE. • **Pros:** Very low noise in first stage of amplifier results in low input-referred noise and reasonably low output noise voltage. • **Cons:** High current consumption in first stage, unable to meet current/power specification for current pulses of amplitudes greater than 4µA.

Generating Reference Voltages for Biasing



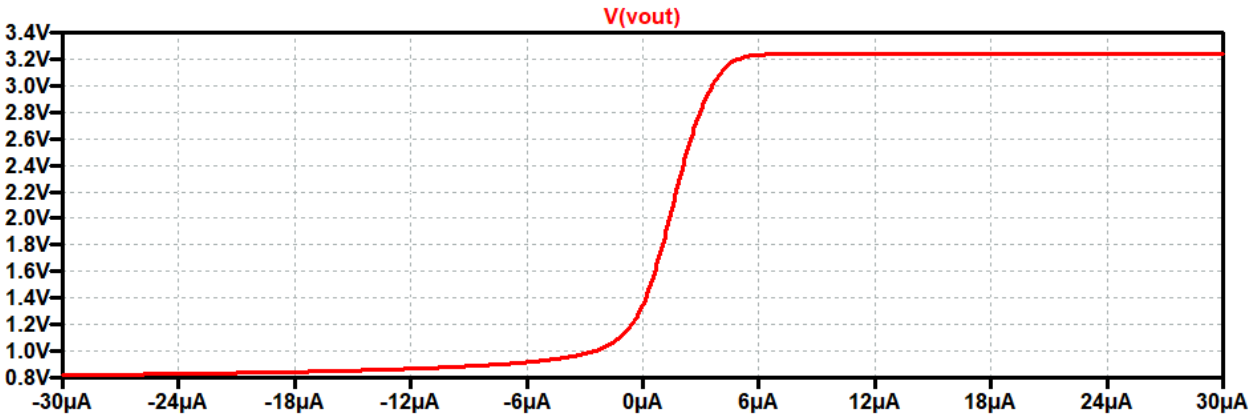
Circuit Designed to Generate Reference Voltages Used to Bias Transistors in TIA, Voltage Amp, Output Buffer

Simple voltage dividers were designed using MOSFETs to generate the reference voltages necessary to bias the TIA, voltage amplifier, and source followers. Longer L was used so that the devices could generate the necessary voltage while sourcing/sinking less current. Some of the dividers are used to bias large W devices in the TIA and in the voltage amplifier. Those dividers consist of wider devices which can source/sink more current, keeping the reference voltage stable as currents change in the circuit.

Analysis of Performance of Individual Stages

Range of Input Current, Output Voltage Swing

A couple of important parameters to consider are allowable range of input currents for amplification, and the maximum output swing on the output of the NMOS source follower. The amplifier will only amplify for a certain range of input currents. Sweeping the input current from a large negative current to a large positive current of the same magnitude yields the plot below, from which we can take away both the input current range and the output voltage swing.



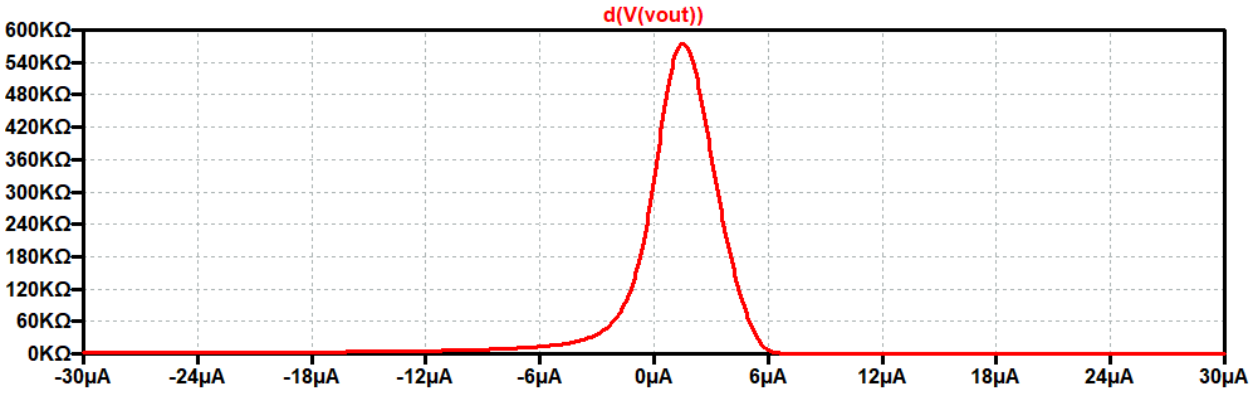
Sweeping Input Current from -30µA to 30µA, Plotting Vout to Obtain Output Swing

In the plot above, we can see that the minimum value of V_{out} is around 800mV and the maximum value of V_{out} is just above 3.2V, meaning our output voltage swing is

$$V_{out,swing} = V_{out,max} - V_{out,min}$$

$$V_{out,swing} = 3.2V - 0.8V = 2.4V$$

Our input current range can be estimated by taking the derivative of the plot above. The slope of the plot above gives us the gain of our amplifier, and we can see the range of input currents which are amplified.



Derivative of Vout from Current Sweep, Visual Analysis of Gain of Amplifier for Different Input Currents

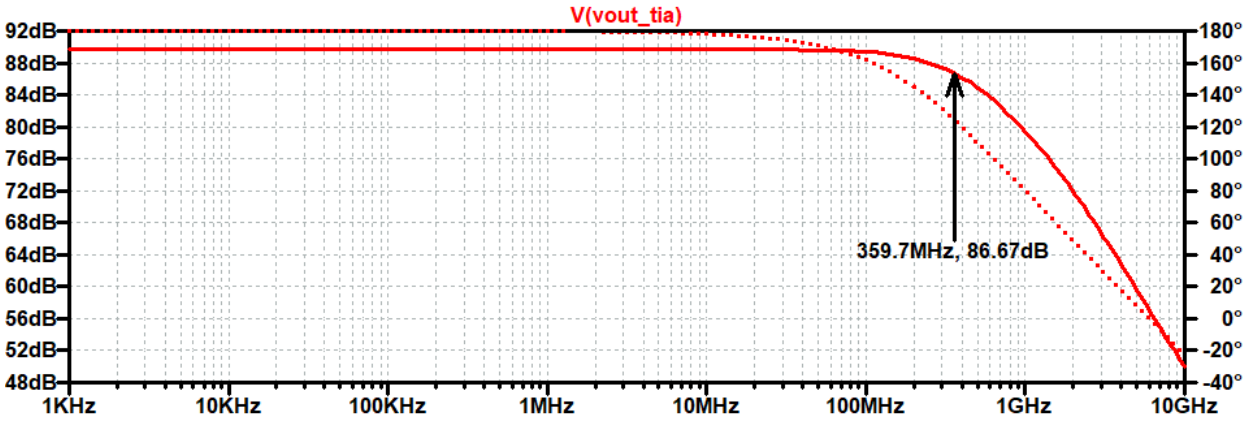
The specification for TIA gain is 30kΩ cascaded with a voltage amplifier whose gain is between 10 V/V and 20 V/V. By these standards, we can call the range of input currents the range of currents for which we have an overall gain of 300kΩ to 600kΩ. Therefore,

$$0 \leq I_{in} \leq 3.4\mu A$$

Transimpedance Amplifier Performance

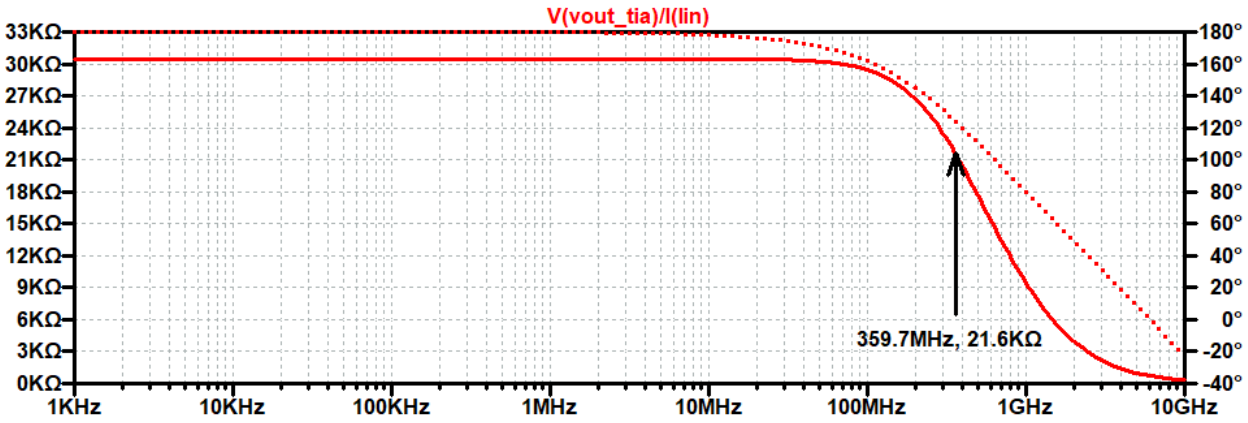
The first stage, the transimpedance amplifier, was designed to have a gain of 30kΩ for a bandwidth of at least 250MHz. Running an AC analysis of the first stage alone will yield gain and bandwidth of the TIA.

Below is the frequency response of the TIA in decibels.



Frequency Response of TIA with No Load, Measured in dB

Here we plot the same frequency response, but using linear measurement for the y-axis.



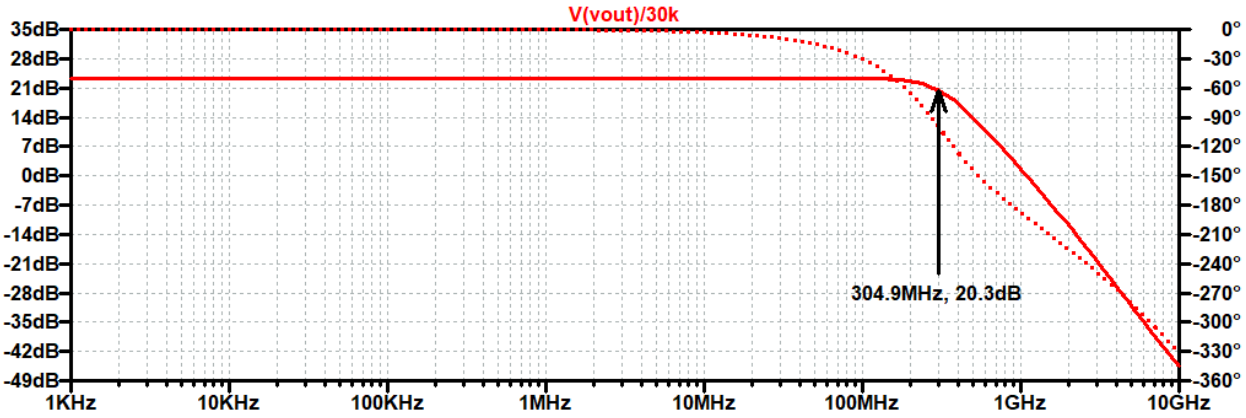
Frequency Response of TIA with No Load, Measured in kΩ

We can observe from the plots above that with no load, the TIA has a bandwidth of around 360MHz and a gain of just barely above 30kΩ. When connecting the second stage to the TIA, the bandwidth does not change at all. The simulations above are ran neglecting the input capacitance associated with using an off-chip APD. As was described in the summary of performance table previously, as APD input capacitance increases, the bandwidth begins to drop.

Voltage Amplifier Performance

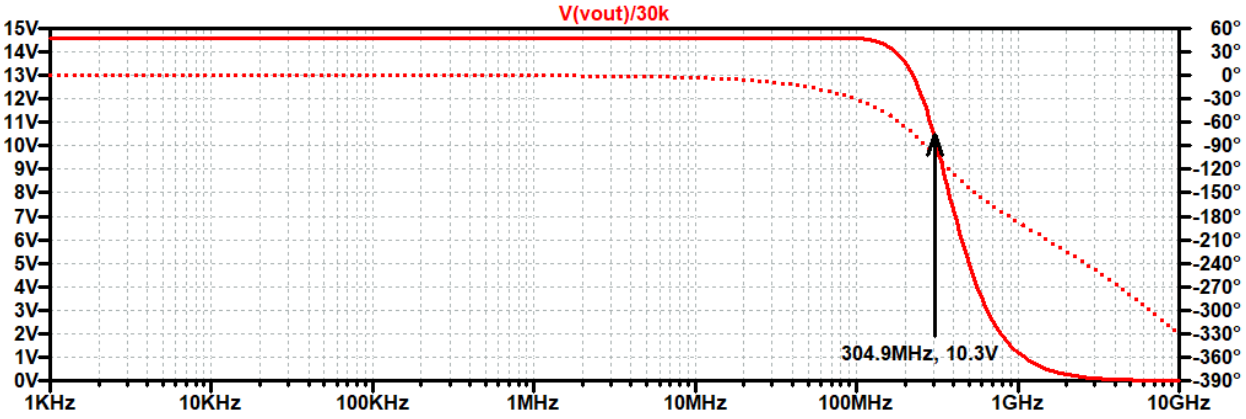
The second stage, the voltage amplifier, was designed to have a gain of 10-20 V/V for a bandwidth of at least 250MHz. Running an AC analysis of the first stage and second stage, and dividing out the gain of the TIA, we can obtain the frequency response of the voltage amplifier.

Below is the frequency response of the voltage amplifier in decibels.



Frequency Response of Voltage Amplifier with No Load, Measured in dB

Again, here we plot the same frequency response, but using linear measurement for the y-axis.



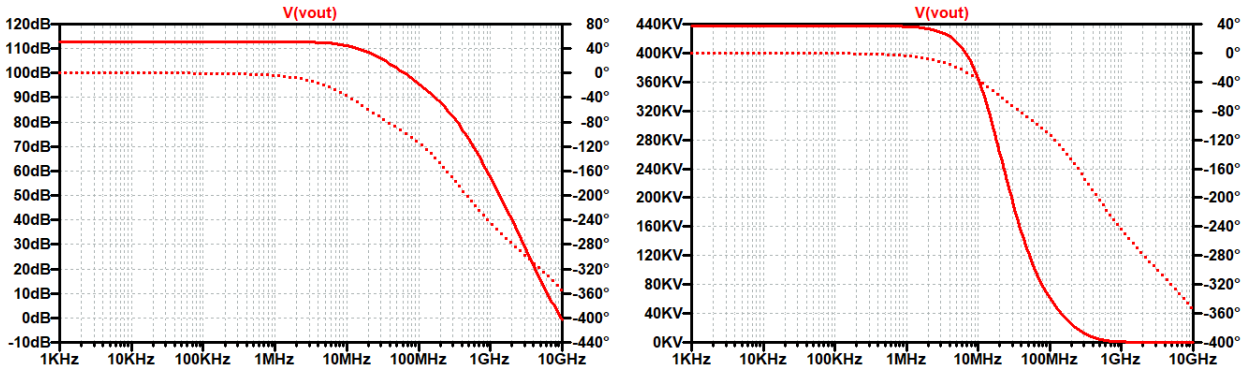
Frequency Response of Voltage Amplifier with No Load, Measured in V

Here we can observe that the low frequency gain of the voltage amplifier is around 14.5 V/V, and that the bandwidth of the amplifier is over 300MHz. However, connecting a 1pF load to the output of the voltage amplifier directly causes a drastic decrease in bandwidth. Since we want the analog front-end to maintain a bandwidth of 250MHz while driving high impedance loads, such as a 1pF capacitor, it was necessary to burn up some current/power in a wide W, high current output stage with load-driving capability. Thus, the PMOS source follower/NMOS source follower output buffer stage was designed to drive the necessary loads.

Output Stage Performance

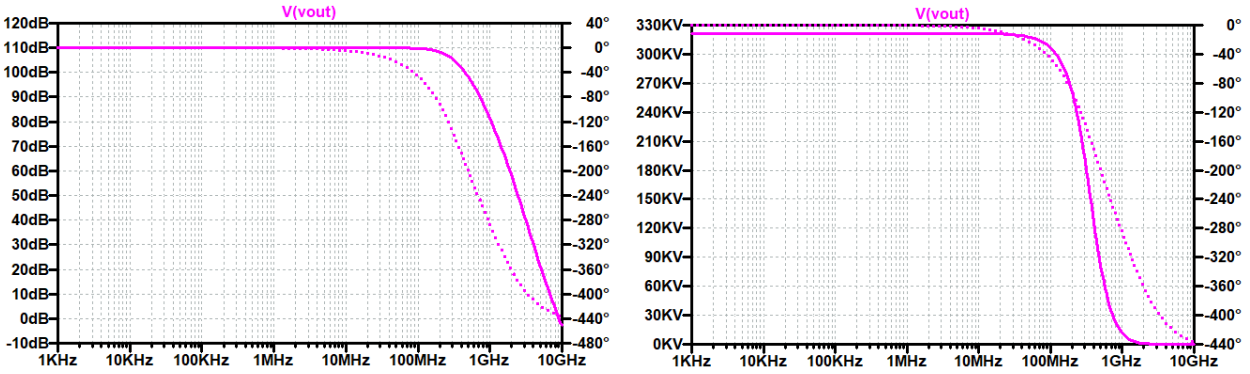
It is important to analyze the need for the output stage, since it consumes much of the current flowing in the entire circuit. The simulations below show why it is necessary to burn up a large amount of power in the output stage.

Below, we see simulations of the output of the voltage amplifier with a 1pF load connected. The bandwidth has dramatically decreased in comparison to the simulations ran previously with no load. While our bandwidth with no load was over 300MHz, our new bandwidth, driving a 1pF load, is under 50MHz.



Simulations Showing Performance of Amplifier with 1pF Load, No Output Stage

Here, we see simulation results after the addition of the output stage. Between the PMOS source follower and the NMOS source follower, around 1mA of current flows. Regardless, the bandwidth is back to where it needs to be, while driving a 1pF load. We should also note that the gain has dropped from 440kV/V to around 320kV/V (more than 25% decrease). This is because the gain of each source follower is less than 1, causing them to attenuate our output signal.

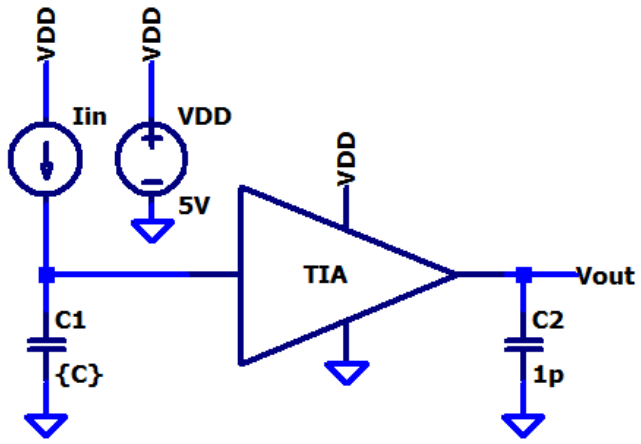


Simulations Showing Performance of Amplifier with 1pF Load, Output Stage Connected

The output stage did not come without a price. The circuit is now capable of driving capacitive loads up to 1pF, but our overall power consumption is much higher, and our gain is much lower, but still meets the specification for between 300kΩ to 600kΩ.

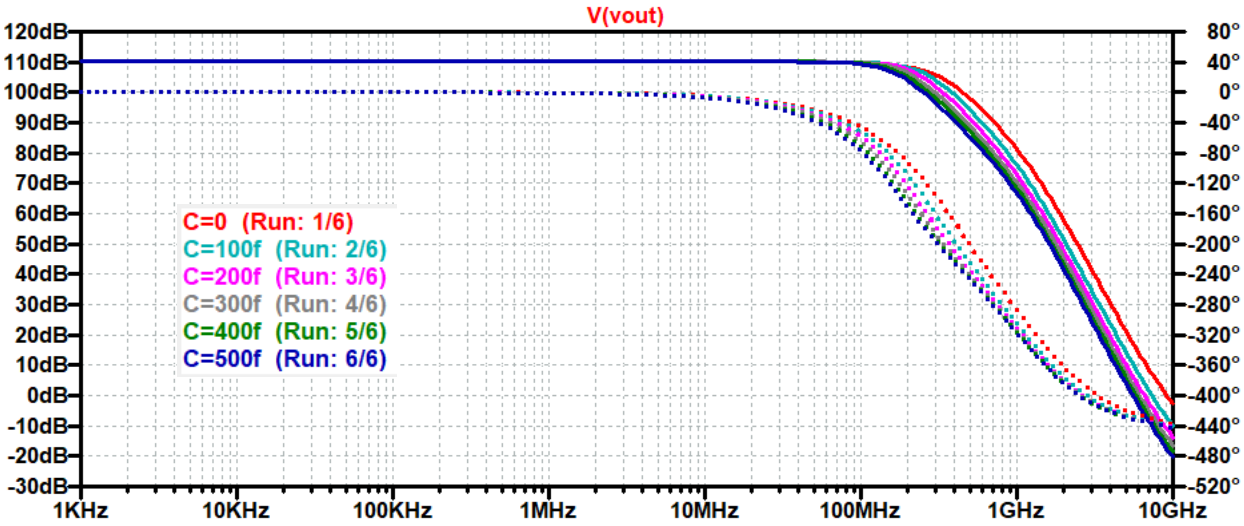
Overall Performance

A symbol was created for the final circuit, consisting of the biasing circuit, the transimpedance amplifier, the voltage amplifier, and the output stage.



Schematic Drafted for Simulations/Analysis using TIA Symbol

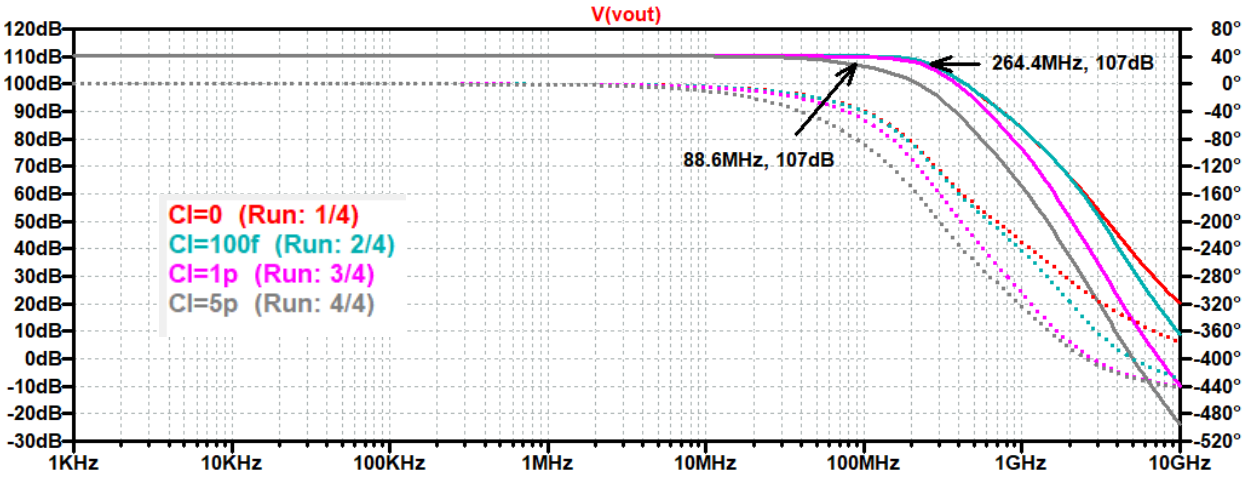
AC Analysis with Varying Off-Chip APD Capacitance, 1pF Load



Frequency Response of Amplifier with Varying APD Capacitance, Driving 1pF Load

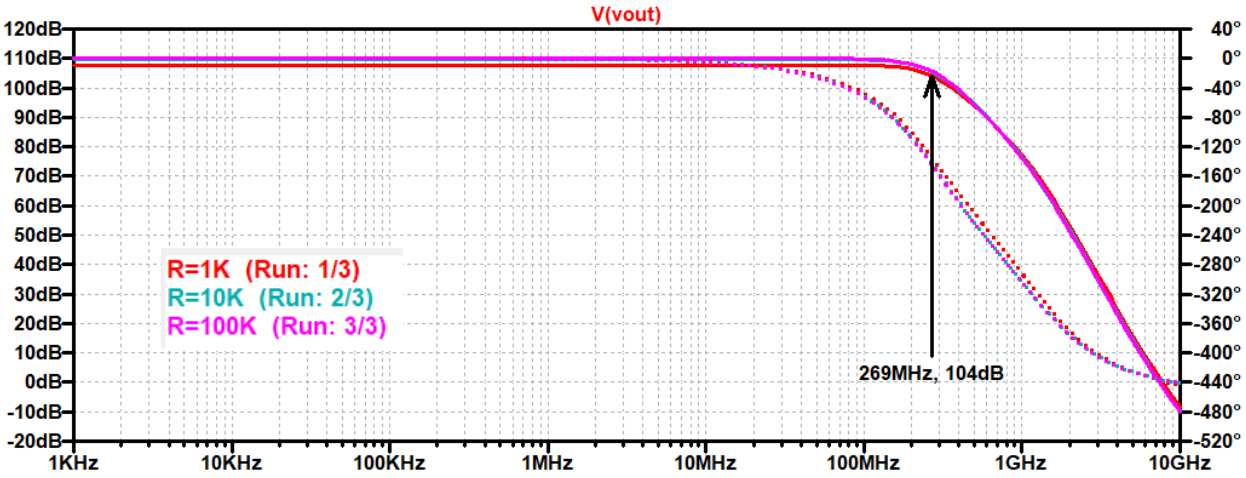
Above, we observe the frequency response of the amplifier while driving a 1pF load, as the modeled off-chip APD capacitance increases from 0 (negligible) to 500fF. Taking a look at the step legend, we see that when we neglect the off-chip APD capacitance, we get our maximum bandwidth. As the modeled capacitance increases, the bandwidth steadily decreases.

AC Analysis with Varying Loads



Frequency Response of Amplifier with Fixed 100fF Input Capacitance, Varying Capacitive Loads

In the simulation above, the input capacitance resulting from using an off-chip APD is fixed at 100fF and the load capacitance is varied. Taking a look at the step legend, we can see that for loads up to 1pF, the bandwidth remains pretty steady, right around 264MHz. Once we increase the load capacitance to a value above 1pF (here 5pF) the bandwidth decreases by almost 200MHz.

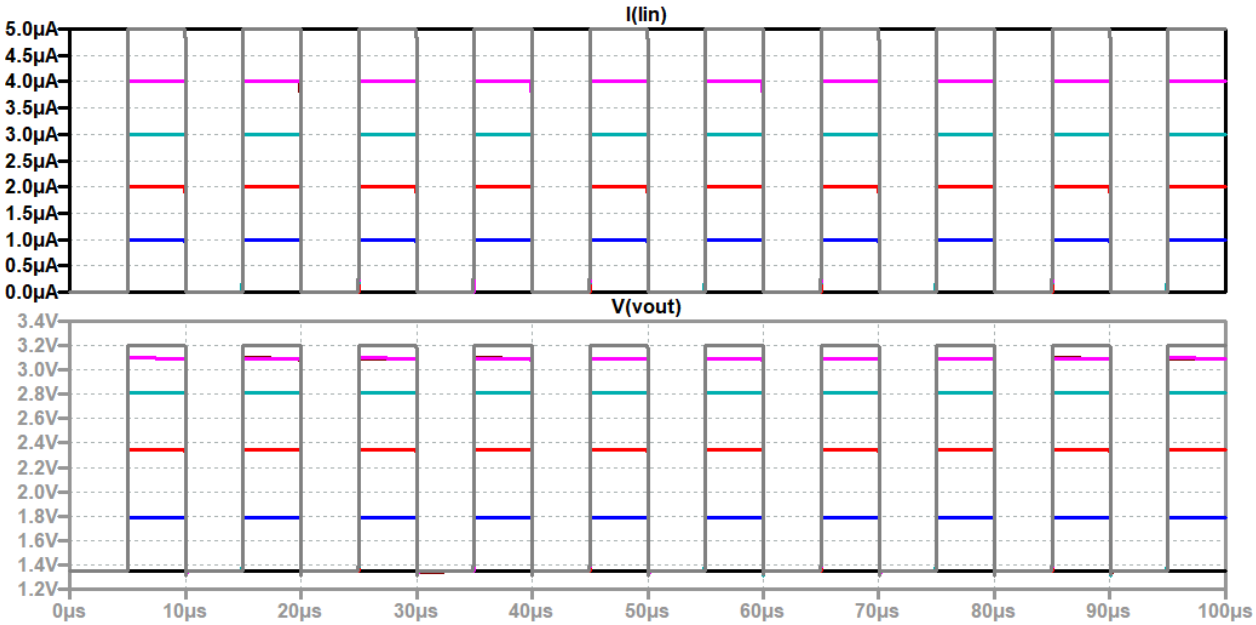


Frequency Response with Fixed 100fF Input Capacitance, Fixed 1pF Load Shunt with Varying Resistive Load

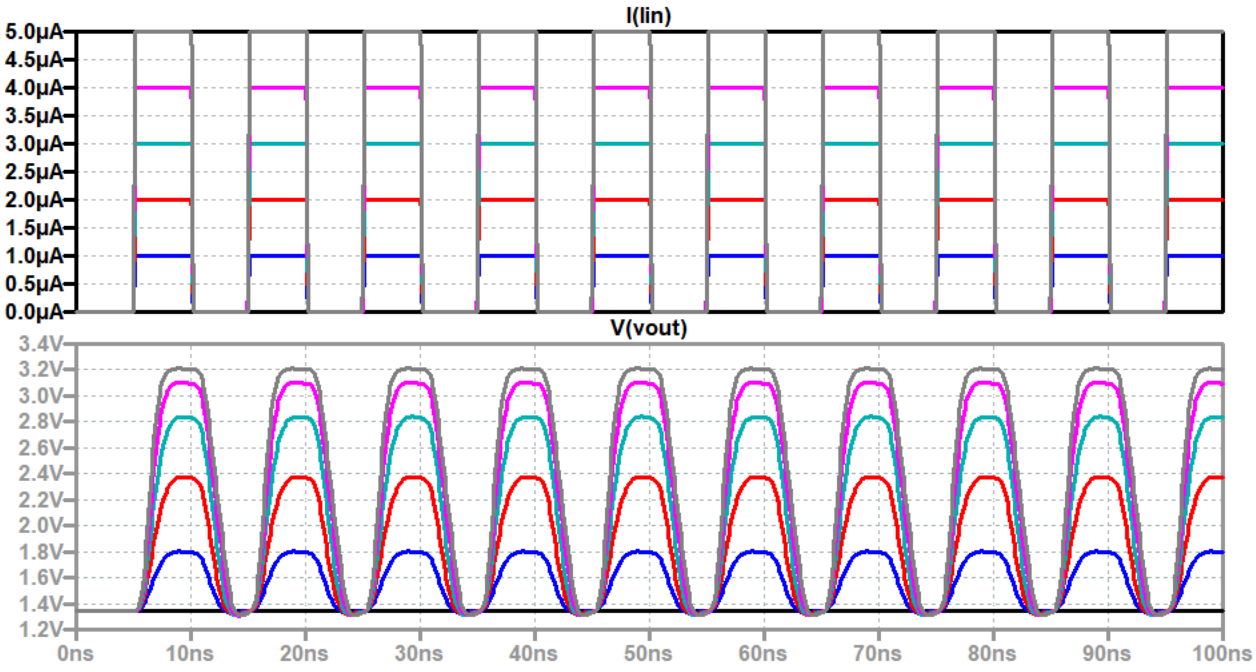
The simulation above shows the frequency response when the load is a 1pF capacitor shunt with a varying resistance. From values of R=100k down to R=1k, we see little to no change in bandwidth, but a small change (around 3dB) in gain.

Transient Response (Driving 1pF Load)

Below are transient analyses of the circuit at f=100kHz and f=100MHz for input current pulses varying in amplitude from 1µA to 5µA, driving a 1pF load.



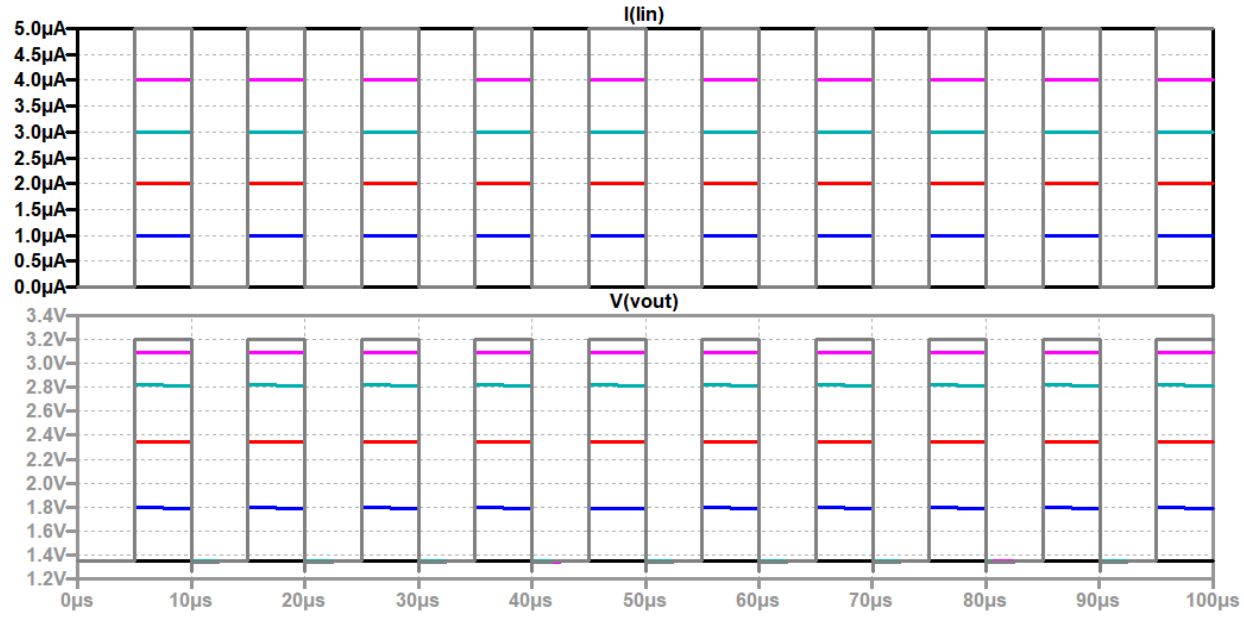
Transient Analysis over 100µs with Current Pulse Frequency of 100kHz, Driving 1pF Load



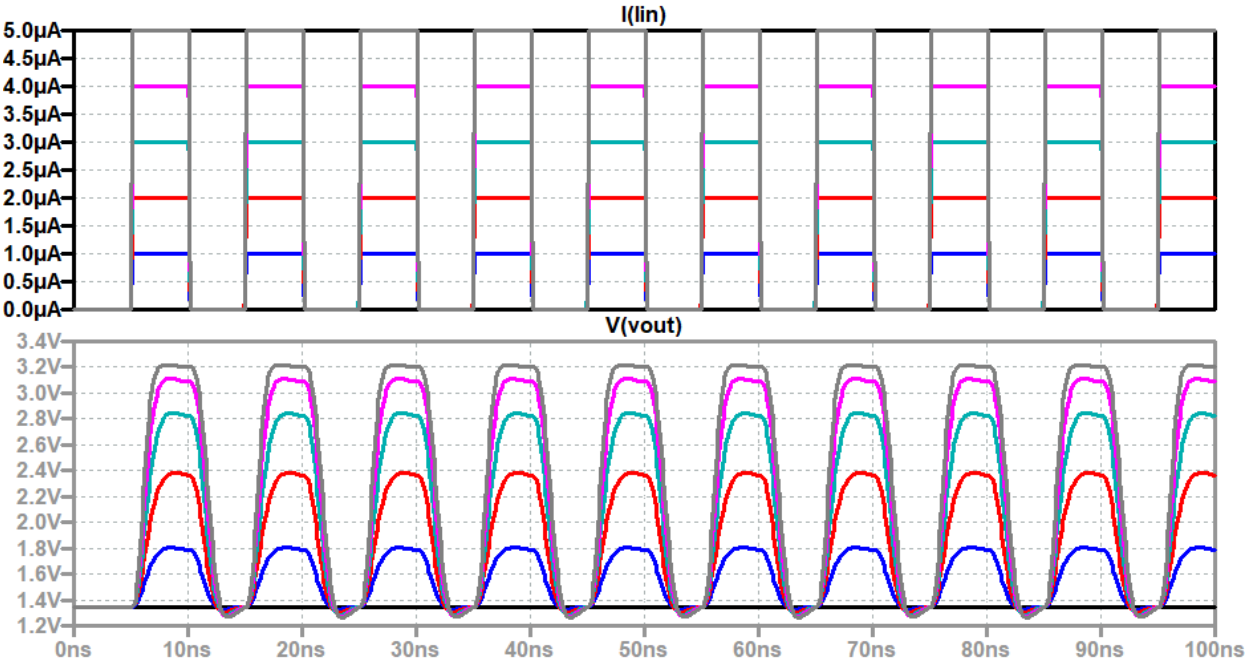
Transient Analysis over 100ns with Current Pulse Frequency of 100MHz, Driving 1pF Load

Transient Response (No Load)

Below are transient analyses of the circuit at f=100kHz and f=100MHz for input current pulses varying in amplitude from 1µA to 5µA, with no load connected. The output waveforms look similar to those above. This means the load does not effect our output much.



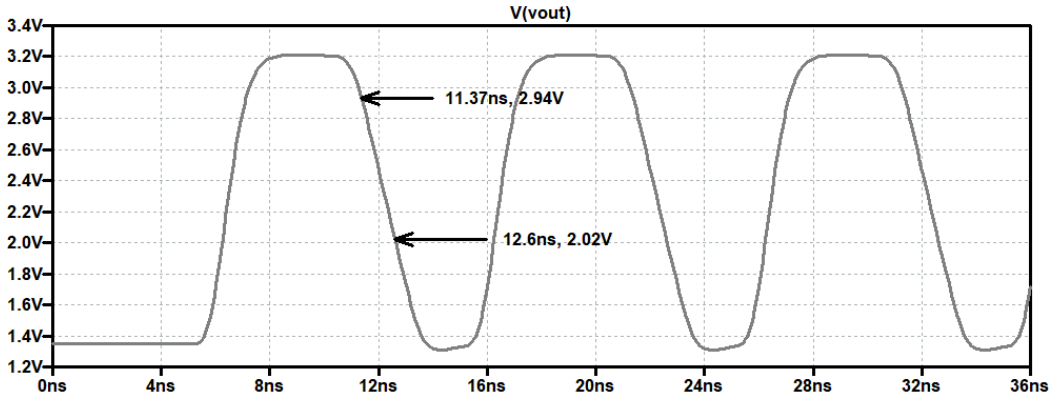
Transient Analysis over 100µs with Current Pulse Frequency of 100kHz, No Load



Transient Analysis over 100ns with Current Pulse Frequency of 100MHz, No Load

Slew-Rate with Maximum Load (1pF Capacitive)

The slew-rate is a measure of how fast the output voltage can rise or fall while driving a load. In other words, it is the maximum rate of change, or slope, of the output signal. Below, we analyze the slew-rate of the amplifier while driving a 1pF load, for varying input currents.

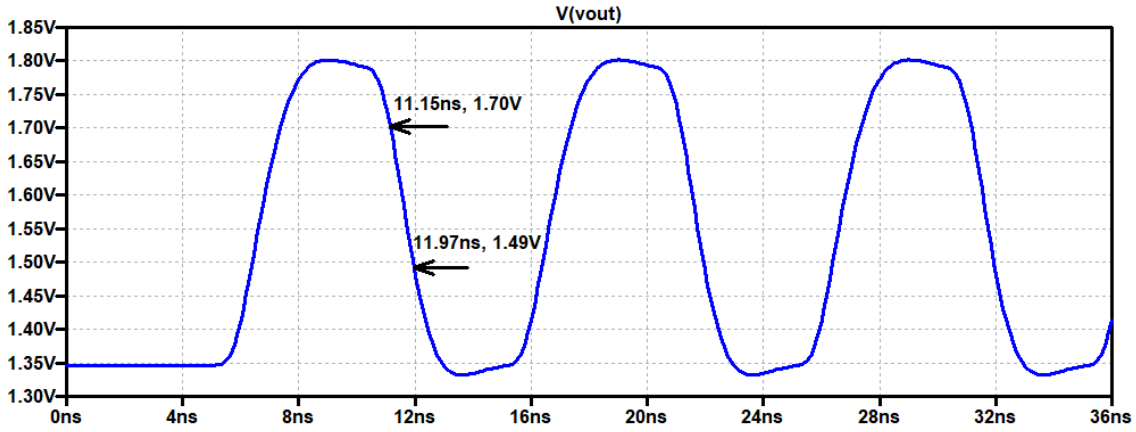


Determining Slew-Rate for Input Current Pulse of 5µA, Driving 1pF Load

The slew-rate can be calculated as the slope between the two points from the simulation, or

$$SR = \frac{\Delta V}{\Delta t} = \frac{2.94V - 2.02V}{12.6ns - 11.37ns}$$

$$SR = \frac{920mV}{1.23ns} = 747mV/ns$$

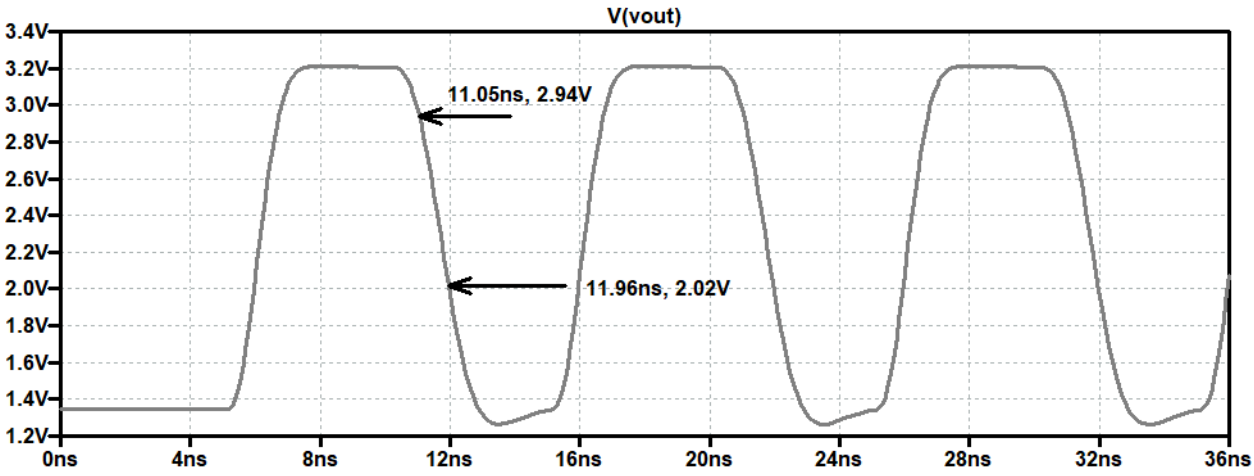


Determining Slew-Rate for Input Current Pulse of 1µA, Driving 1pF Load

$$SR = \frac{\Delta V}{\Delta t} = \frac{1.70V - 1.49V}{11.97ns - 11.15ns}$$

$$SR = \frac{210mV}{0.82ns} = 256mV/ns$$

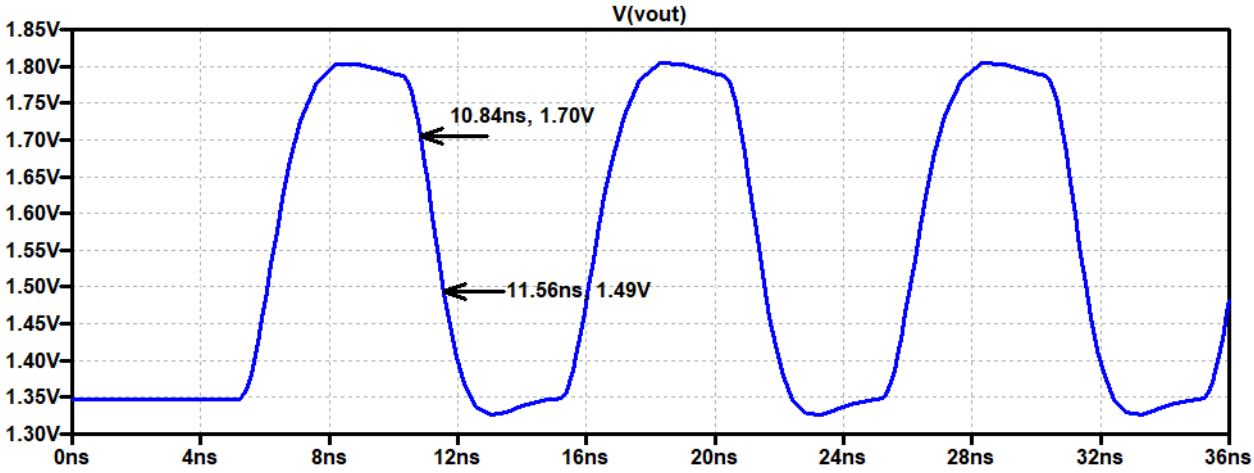
Slew-Rate with No Load



Determining Slew-Rate for Input Current Pulse of 5µA, No Load

$$SR = \frac{\Delta V}{\Delta t} = \frac{2.94V - 2.02V}{11.96ns - 11.05ns}$$

$$SR = \frac{920mV}{0.91ns} = 1.01V/ns$$



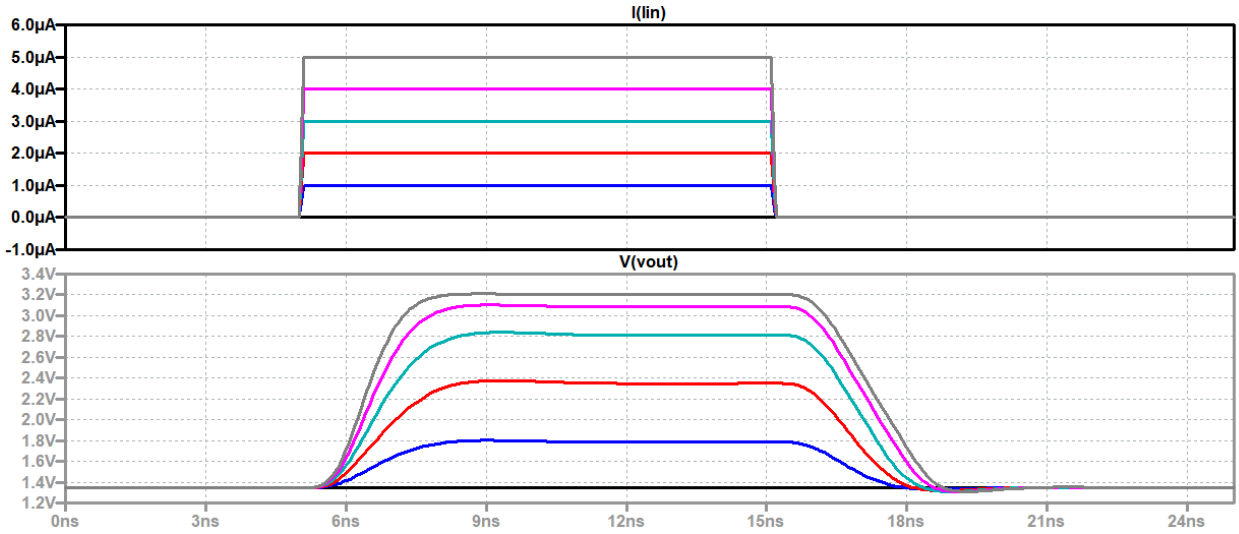
Determining Slew-Rate for Input Current Pulse of 1µA, No Load

$$SR = \frac{\Delta V}{\Delta t} = \frac{1.70V - 1.49V}{11.56ns - 10.84ns}$$

$$SR = \frac{210mV}{0.72ns} = 292mV/ns$$

Step Response (1pF Load)

In the simulation below, the input current is pulsed high at 5ns and pulsed low at 15ns. We can observe the rise time, fall time, and settling time of the circuit as it drives a 1pF load and for different input current pulse amplitudes, ranging from 1µA to 5µA.

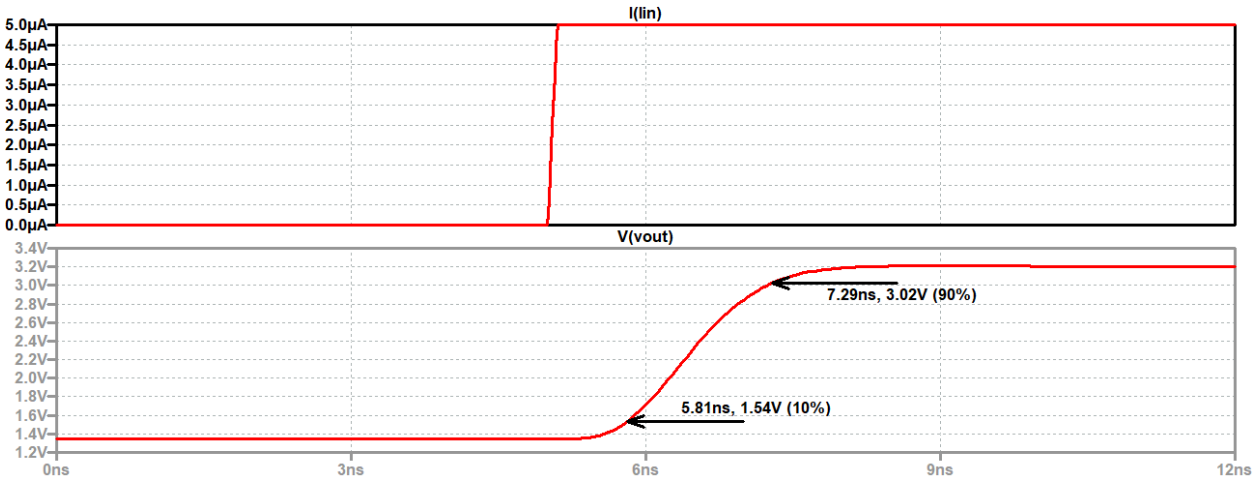


Step Response of the AFE Driving 1pF Load for Varying Input Current Pulse Amplitudes

From the plot above, we can observe some slight overshoot on the rising edge, and even more overshoot on the falling edge. It is important to analyze these edges individually and determine the rise time, fall time, and the settling time (for rising and falling edge) of the response.

Rise Time

The rise time can be determined by subtracting the time at which the output is at 10% of its final value from the time at which the output is at 90% of its final value, for the signal's rising edge.



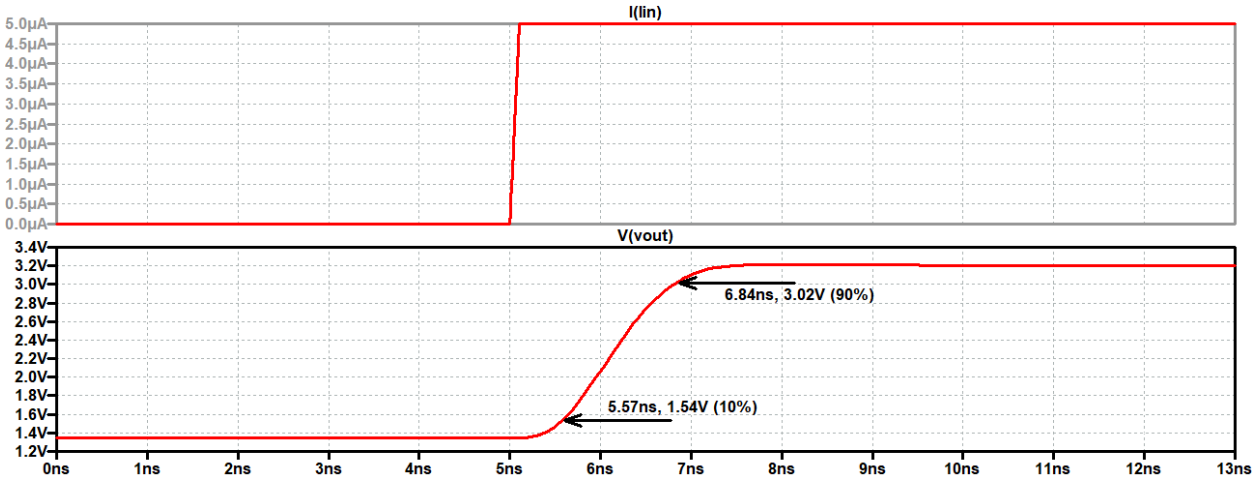
Measuring Rise Time with 5µA Input Current Pulse Driving 1pF Load

From the plot, the rise time while driving a 1pF load can be calculated by

$$t_{rise} = t_{90\%} - t_{10\%}$$

$$t_{rise} = 7.29ns - 5.81ns = 1.48ns$$

Here, we plot the rising edge of the signal with no load connected.



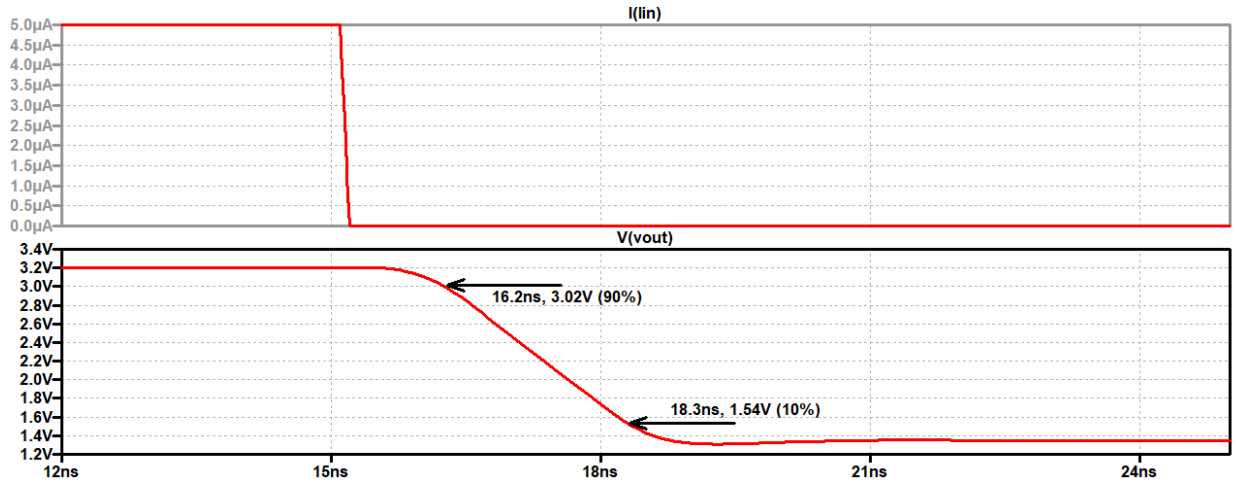
Measuring Rise Time with 5µA Input Current Pulse with No Load

We can calculate the rise time of the output signal with no load by

$$t_{rise} = 6.84ns - 5.57ns = 1.27ns$$

Fall Time

The fall time can be determined by subtracting the time at which the output is at 90% of its final value from the time at which the output is at 10% of its final value, for the signal's falling edge.



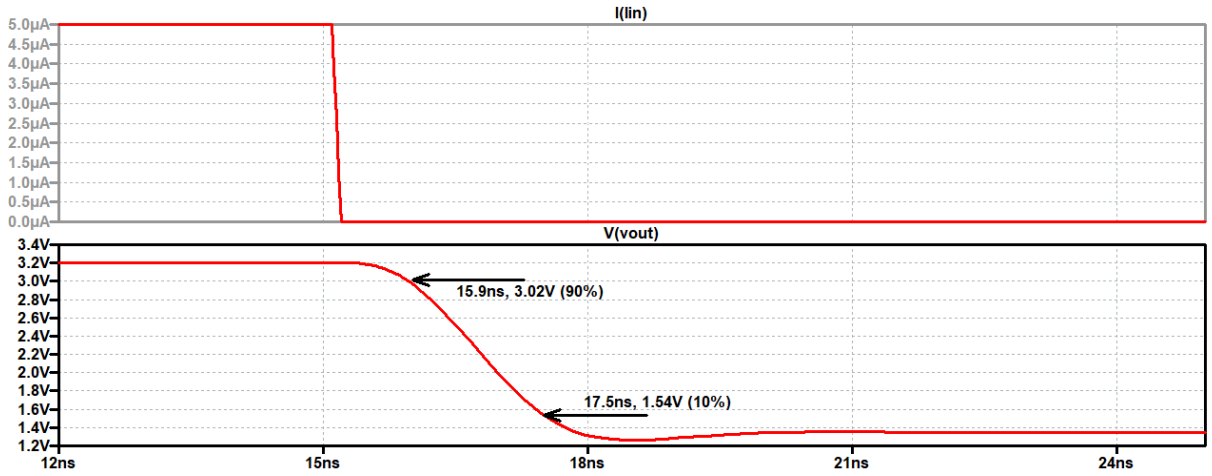
Measuring Fall Time with 5µA Input Current Pulse Driving 1pF Load

From the plot, the fall time while driving a 1pF load can be calculated by

$$t_{fall} = t_{10\%} - t_{90\%}$$

$$t_{fall} = 18.3ns - 16.2ns = 2.1ns$$

Here, we plot the falling edge of the signal with no load.



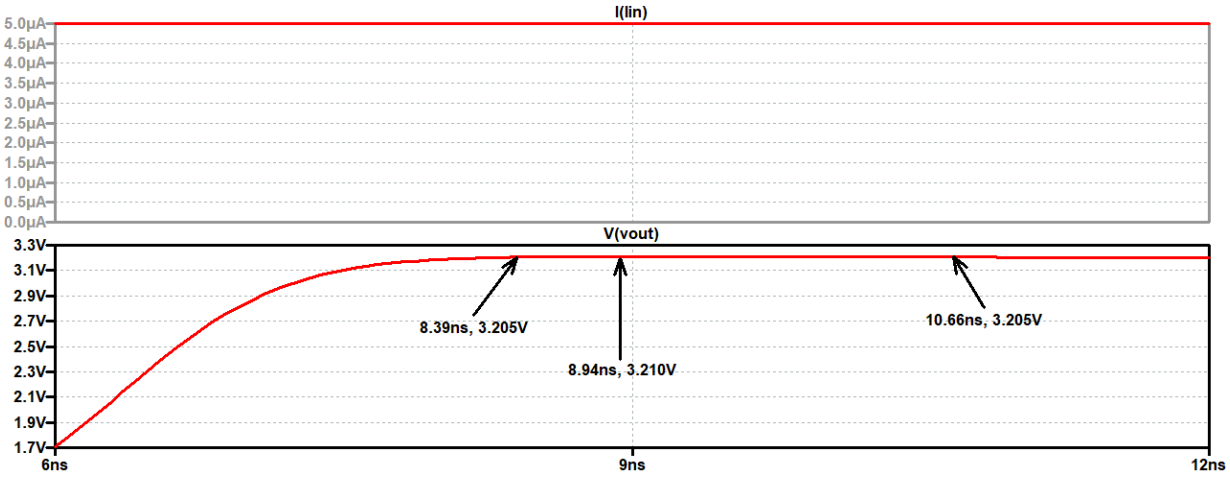
Measuring Fall Time with 5µA Input Current Pulse with No Load

We can calculate the fall time of the output signal with no load by

$$t_{fall} = 17.5ns - 15.9ns = 1.6ns$$

Settling Time

Signals with no overshoot (critically damped) have a settling time of 0. For signals with overshoot, the settling time is the amount of time elapsed from the first time the output over/undershoots past its final value to the next time the output hits its final value.

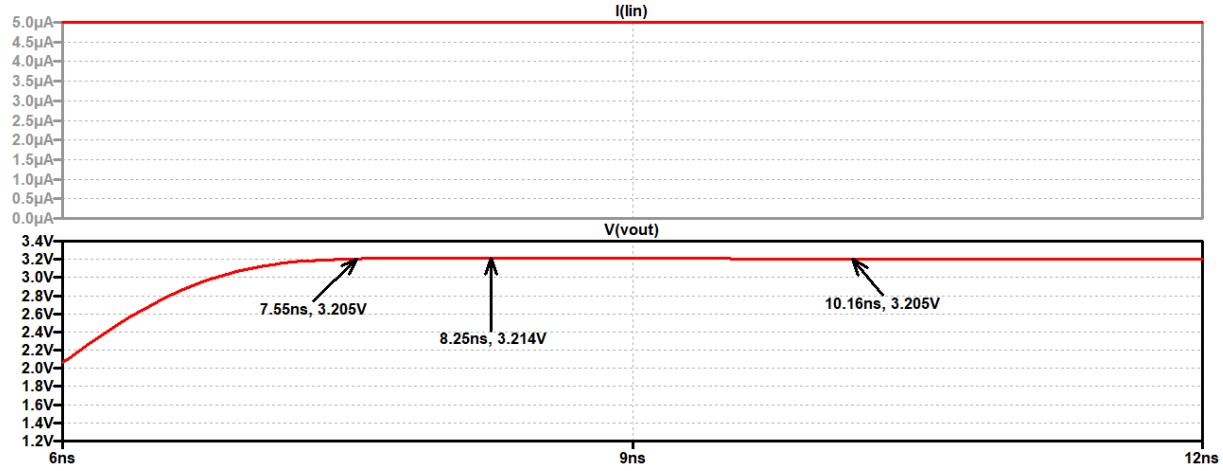


Measuring Settling Time of Rising Edge Driving 1pF Load

The settling time for the rising edge driving a 1pF load can be calculated by

$$t_{settle} = t_{Vfinal,2} - t_{Vfinal,1}$$

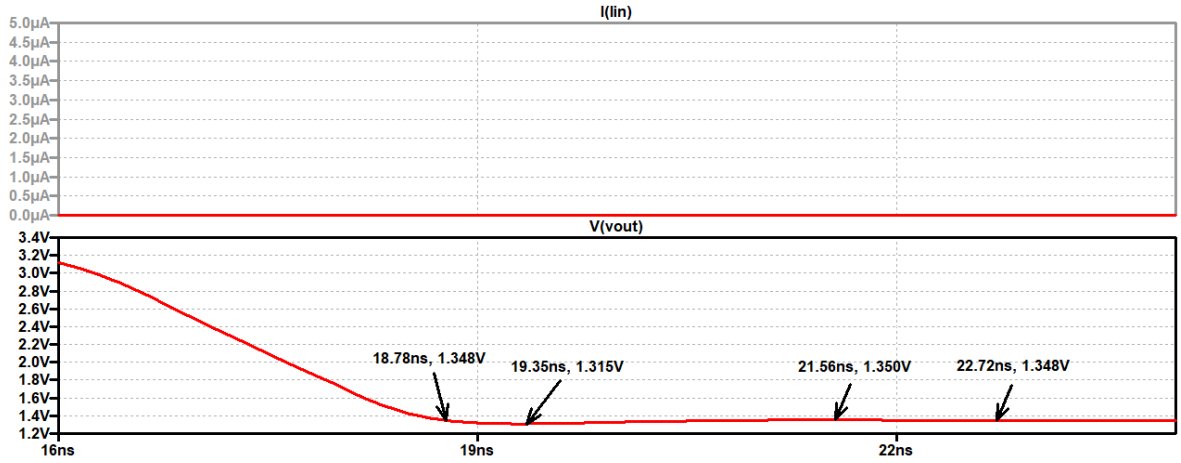
$$t_{settle} = 10.66ns - 8.39ns = 2.27ns$$



Measuring Settling Time of Rising Edge with No Load

The settling time for the rising edge with no load can be calculated by

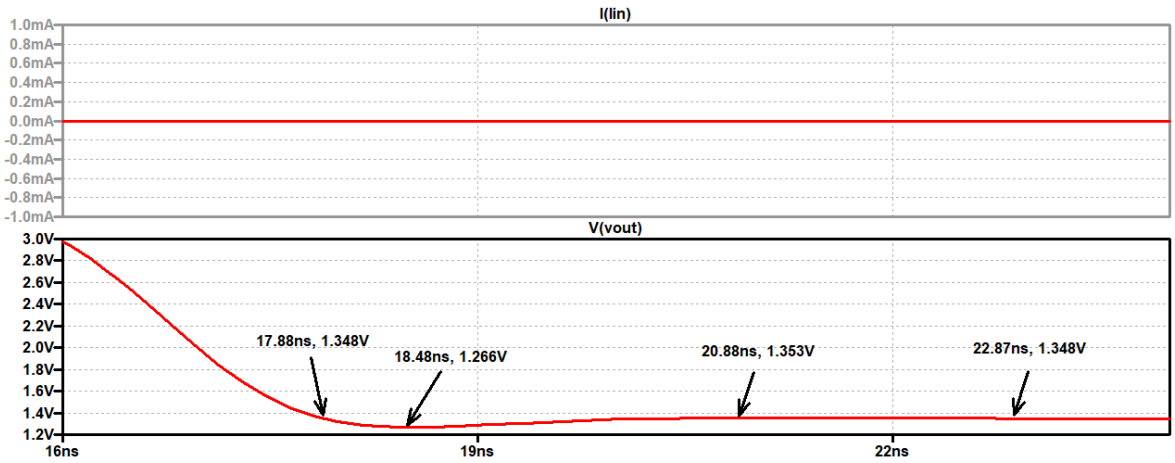
$$t_{settle} = 10.16ns - 7.55ns = 2.61ns$$



Measuring Settling Time of Falling Edge Driving 1pF Load

The settling time for the falling edge driving a 1pF load can be calculated by

$$t_{settle} = 22.72ns - 18.78ns = 3.94ns$$



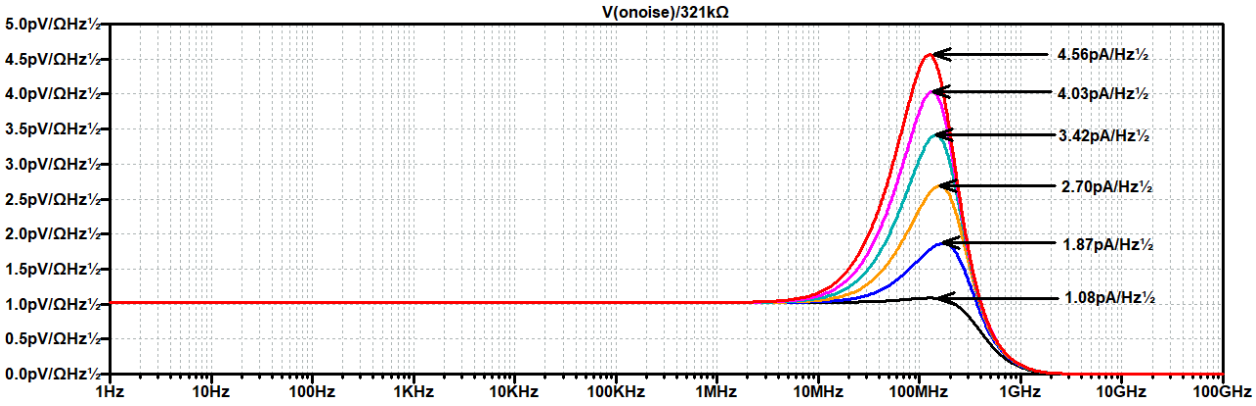
Measuring Settling Time of Falling Edge with No Load

The settling time for the falling edge with no load can be calculated by

$$t_{settle} = 22.87ns - 17.88ns = 4.99ns$$

Analysis of Noise, Off-Chip APD Capacitance Effects

Here, we analyze the output and input-referred noise spectra while varying the modeled APD input capacitance. The plot below shows input-referred noise in A/Hz$^{1/2}$, obtained by dividing the output noise voltage by the gain of the AFE.



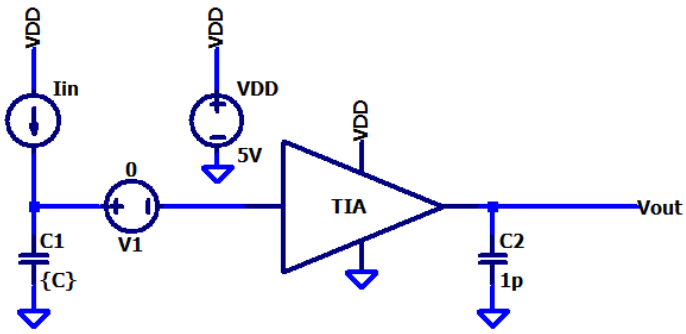
Input Referred Noise Current Spectrum as APD Capacitance Increases from 0 to 500fF

By inspection, we can conclude that at high frequencies, the APD input capacitance has a large effect on the peak noise current contribution of the off-chip APD. If we neglect the capacitance completely, the noise peak is minimal (less than 0.1 pA/Hz$^{1/2}$). However, as this capacitance increases, we see a significant increase in the noise current peak value. Even with 500fF of APD capacitance, the noise current never gets higher than 4.56pA/Hz$^{1/2}$.

Summary of Noise Analysis						
APD Capacitance	**None**	**100fF**	**200fF**	**300fF**	**400fF**	**500fF**
Output Noise	0.35µV/Hz$^{1/2}$	0.60µV/Hz$^{1/2}$	0.87µV/Hz$^{1/2}$	1.1µV/Hz$^{1/2}$	1.3µV/Hz$^{1/2}$	1.45µV/Hz$^{1/2}$
Input-Referred Noise	1.1pA/Hz$^{1/2}$	1.9pA/Hz$^{1/2}$	2.7pA/Hz$^{1/2}$	3.4pA/Hz$^{1/2}$	4.0pA/Hz$^{1/2}$	4.6pA/Hz$^{1/2}$

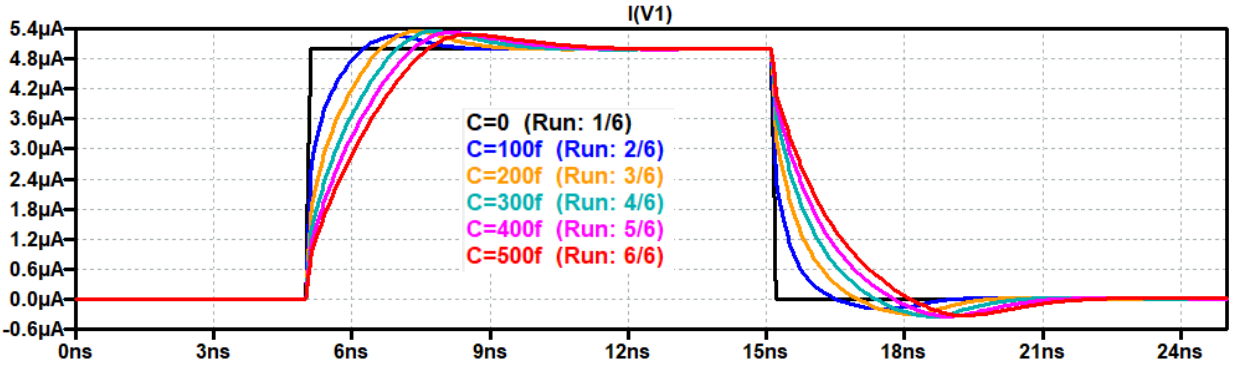
Table Containing Maximum Values of Output Noise and Input-Referred Noise

We can see from both the output noise and input-referred noise rows of the table, and similarly from the plot, that increases in the modeled APD capacitance increase the noise present in the circuit.



Schematic Drafted to Test APD Capacitance Effects

In order to further analyze the impact of the APD input capacitance on the performance of the circuit, a 0V voltage source was placed between the input to the TIA and the current source, with the APD capacitance shunting the current source. The 0V voltage source will allow us to measure the current that actually flows into the TIA in comparison with what the current source outputs.

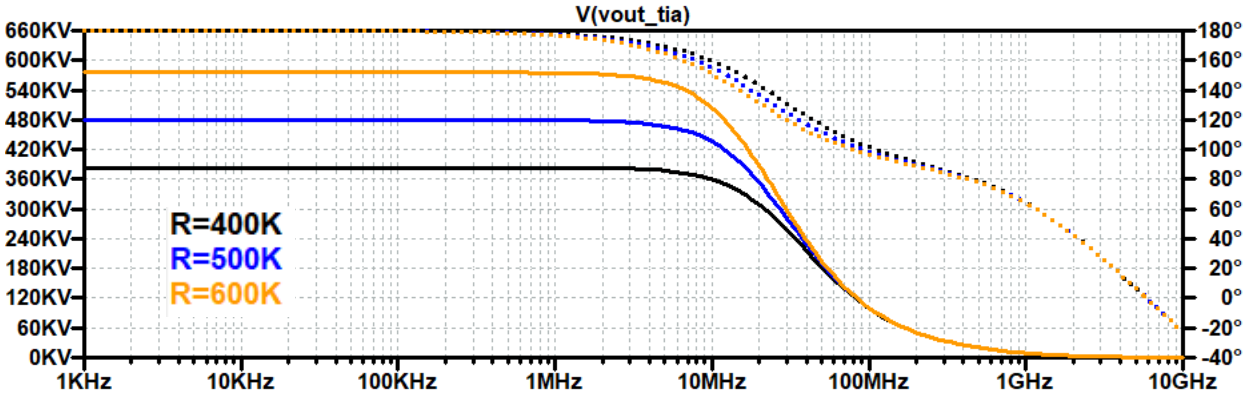


Simulation Results Testing APD Capacitance Effects, Varying Input Capacitance from 0 to 500fF, Iin=5µA

From the transient simulation above, taking a look at the step legend, when C=0 (black trace), we are neglecting the input capacitance completely, and a nice, clean, fast rectangular pulse of current flows directly into the TIA. As the input capacitance increases, the rise time and fall time of the current pulse that actually flows into the TIA get slower and slower. Since our output voltage is dependent upon our input current, the decrease in speed of the input results directly in a decrease in speed of the output as input capacitance increases. It is important to take this into account, since this capacitance is not likely to be negligible when using an off-chip APD.

Need for the Inclusion of a Second Stage

Many, if not all, specifications for the design could be met using only a single stage with an output buffer connected enabling the first stage to drive the necessary loads. For example, modifying the first stage so that Rf varies from 400kΩ to 600kΩ in 100kΩ steps, we can observe the following frequency response with a 1pF load connected.



Frequency Response Plot Varying the Feedback Resistance in the First Stage to Obtain Required Gain

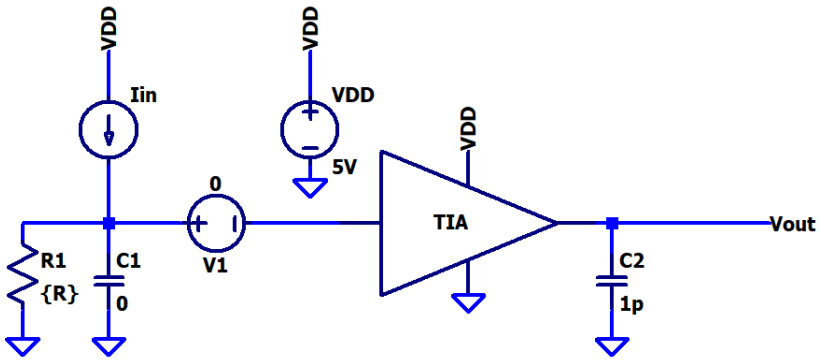
Since Rf mainly controls the gain of the first stage, simply increasing Rf to the value of gain desired gives us the gain required by both stages in the first stage alone. We notice that the bandwidth takes a large hit, due to the increase in gain without modifying the circuit further. Other design modifications, such as increase in overdrive voltage, adjustment of device sizes, and the addition of an output stage would allow us to meet the bandwidth requirement as well using only one stage. The need for the inclusion of a second stage lies in efficiency and practicality.

Practically, when laying out resistors on chip, there is an associated propagation delay or RC delay through the resistor if it is laid out using n-well. As one would imagine, the larger the resistor, the longer the delay through the resistor. This delay would cause practical speed problems that would not show up in simulation. A large resistor (400-600kΩ) would also occupy a large layout space; much larger than that of a 30kΩ resistor. Finally, a much larger resistor would have a much larger thermal noise contribution to the circuit, which can be avoided by

using two stages and minimizing the size of the resistor used in the first stage, while not using any resistor at all in the second stage. Since the first stage of any amplifier should have the lowest noise possible, adding a giant resistor to the first stage is not practically a good idea. It is more efficient, in terms of both speed and noise performance, to design a second stage to amplify the voltage further without contributing significant noise and without decreasing bandwidth.

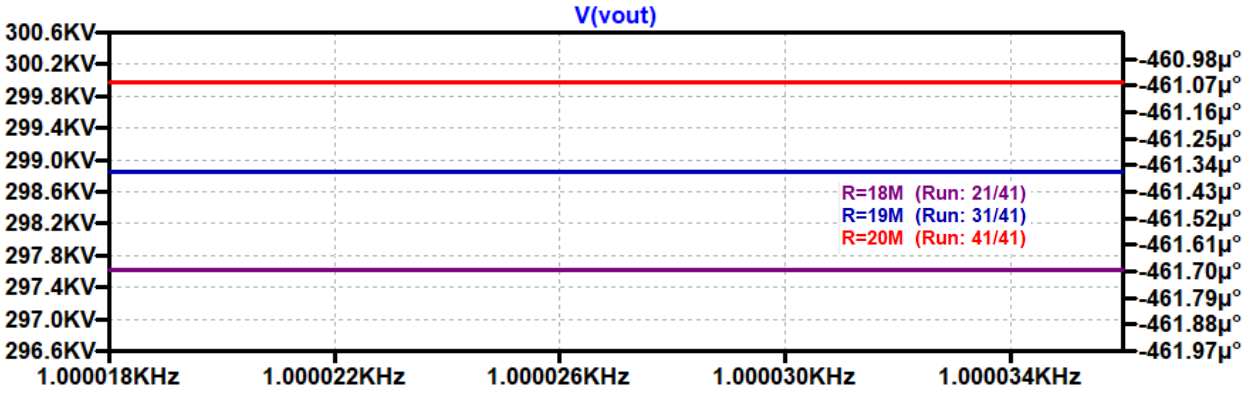
Further Discussion of APD Connection to TIA

In the C5 process, one possible configuration connects the APD's anode to ground through a resistor. As was mentioned previously, the value of this resistor is significant. If the resistor is too small (and therefore is comparable to the size of the feedback resistor) the gain and biasing of the differential amplifier will be effected, and the circuit will not perform as expected. To determine the value of this resistor, we can connect a resistor from the input node to ground and simulate, to determine at which value the gain begins to drop.



Modeling Connection From APD Anode to Ground Through Resistor

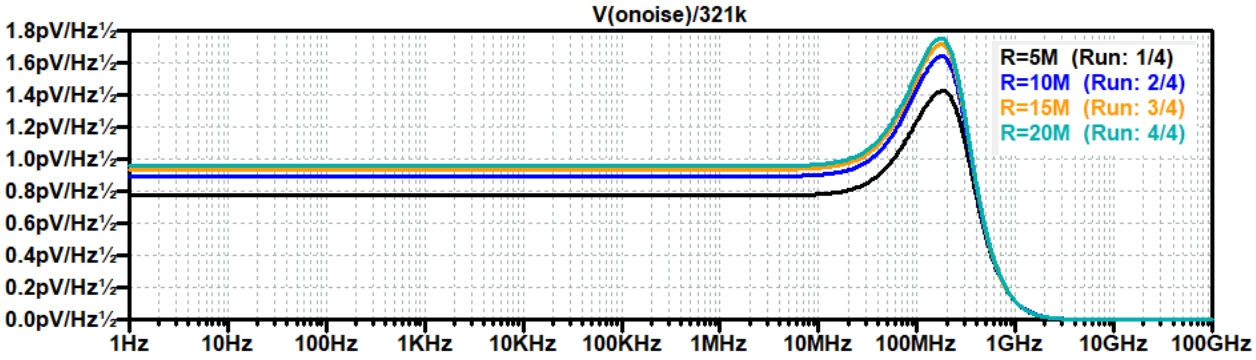
The resistance of R1 was swept from 20MΩ to 16MΩ and the results below were obtained.



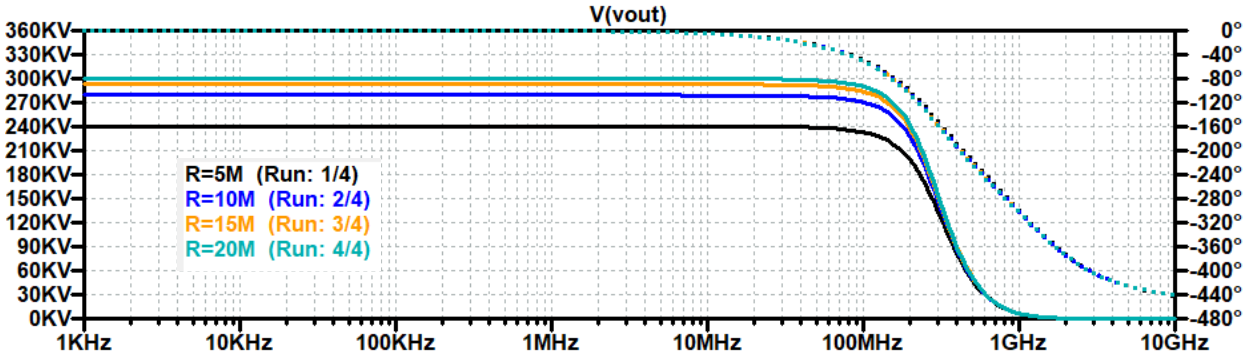
Simulation Results Used to Determine Minimum Size Allowable of Resistor

As we know, the required total gain for the AFE is 30kΩ * 10V/V or 300kΩ. From the plot, we see that the gain drops below 300kΩ for values of resistor less than or equal to 20MΩ. From this, we can conclude that the resistor connected from the anode of the APD to ground must exceed a value of 20MΩ in order for the circuit to maintain the desired gain and avoid biasing issues.

It is also important to analyze the SNR with the resistor connected in comparison to when it is not connected for practical purposes.



Noise Simulation to Analyze Circuit Noise with Different Values of Resistor Connected



Frequency Response to Show Decrease in Gain for Decreasing Anode-to-Ground Resistor Sizes

We can draw a couple conclusions from the plots above. First, for decreasing resistor values, the input-referred noise (and as a result the output noise) of the circuit decreases. This is because the main noise contributors in the circuit are thermal noise generated by the resistor to ground and the feedback resistor. We see that the overall noise improves when we decrease the value of resistor. This is because the smaller values of resistor are more comparable to the value of the feedback resistor, making their equivalent parallel resistance smaller. Since the magnitude of thermal noise current and noise voltage are dependent upon the value of resistance, smaller values of R decrease the overall noise. Regardless, we cannot neglect the second plot, which clearly shows large decreases in low frequency gain for decreasing R values. For R values lower than 20MΩ, we see that the gain is less than 300kΩ. Therefore, for peak performance, we must use a value larger than 20MΩ as was mentioned previously. Since the signal is remaining the same and all that is changing is noise, the SNR improves with the added resistor to ground. We can compare the value of noise ($1.9pA/Hz^{1/2}$) with 100fF and no resistor modeled to the value in the plot above (less than $1.0pA/Hz^{1/2}$) to prove that SNR improves when we model this resistor.

Summary

The Analog Front-End design discussed in this report meets all of the project specifications. The low-frequency gain of the first stage (TIA) is just over 30kΩ, and the low-frequency gain of the second stage (voltage amplifier with output buffer) is around 10.7V/V, resulting in an overall AFE gain of 321kΩ. While driving the maximum load (a high impedance capacitive load of 1pF), the AFE bandwidth is 275MHz, with an output that can swing from 800mV up to 3.2V, for a total swing of 2.4V. At the DC operating point, the AFE consumes 23.3mW of power, and consumes 4.66mA of current. For pulses up to 3µA in amplitude, total current consumption remains less than 5mA. For pulses 4µA in amplitude and greater, the current consumption ranges from 5mA to 5.2mA.

The AFE is capable of driving a 1pF load with a slew rate of 747mV/ns when current input pulse amplitude is 5µA, and a slew rate of 256mV/ns when current input pulse amplitude is 1µA. For a step current input with amplitude of 5µA driving a 1pF load:

- the rise time of the output signal is 1.48ns.
- the fall time of the output signal is 2.10ns.
- the settling time of the rising edge is 2.27ns.
- the settling time of the falling edge is 3.94ns.

With no load, the output slew rate is over 1V/ns when current input pulse amplitude is 5µA, and the output slew rate is 292mV/ns when current input pulse amplitude is 1µA. For a step current input with amplitude of 5µA and no load:

- the rise time of the output signal is 1.27ns.
- the fall time of the output signal is 1.60ns.
- the settling time of the rising edge is 2.61ns.
- the settling time of the falling edge is 4.99ns.

Key design decisions, packaged with significant tradeoffs, were made regarding MOSFET width/length, overdrive voltage, output stage device width and topology, and TIA topology.

  - **MOSFET Width/Length:** MOSFET widths were originally selected so that for the correct bias voltage, drain currents would be 10µA for easy calculation while scaling widths. MOSFET length for all devices outside of the biasing circuit was selected to be minimum length possible for the C5 process, 600nm. Using a length of 600nm allows for the highest possible speed of operation for the entire circuit. A significant tradeoff for selecting minimum length for all devices is that the inherent gain of the individual devices goes down as length goes down. Regardless, it was decided that the gain could be obtained while still using minimum length devices. Large multipliers were used in the TIA devices to improve the noise of the first stage. However, this results in much larger layout size and much higher current consumption.

- **Overdrive Voltage:** Overdrive voltage was selected to be greater than 10% of VDD for high-speed operation. Again, it was decided that the gain could be obtained despite the high overdrive voltage, and that the increase in overdrive voltage was necessary to obtain the desired bandwidth while driving high impedance loads.
- **Output Stage Device Width, Topology Used:** The output stage was designed to source/sink a large amount of current very fast so that a 1pF load could be driven without a decrease in speed. The final stage, the NMOS source follower, uses devices with large width multipliers to meet the needs of the amplifier. Since this stage uses such wide devices, it consumes a significant percentage of the total current consumed by the AFE. Using an NMOS source follower on the output allows us to output a signal that is proportional to our input scaled by the gain of the AFE. However, this topology limits our output swing to 2.4V. A class AB output amplifier could be used to improve output voltage swing, while still outputting a signal that is proportional by the gain to our input signal.
- **TIA Topology:** The differential amplifier topology was selected for the TIA since the TIA input is connected directly to the anode of the APD. The differential amplifier has two input terminals, which the diff-amp is constantly trying to force to the same potential. For this reason, we can DC connect the APD's current directly to the front-end's input without the need for AC coupling. Using a diff-amp for the TIA, which is the first stage, also makes connecting a second stage for a voltage amplifier very simple, since the inputs to the second stage can be pulled directly off of the first stage and it will bias the second stage correctly without much effort.

Future Work and Improvement

Although the analog front-end meets the specifications for this application, there are certainly areas where the design can be improved. The key areas where improvements can be made are range of input currents, output voltage swing, biasing circuit efficiency, step response overshoot, and power consumption.

- **Range of Input Currents:** Designing the circuit so that more current is flowing through the devices would improve the allowable range of input currents. However, the circuit operates right on the brink of the power consumption specification. Any more current consumption will break the specification, so more improvement would need to be done to limit power consumption before range of input currents can be improved at all.
- **Output Voltage Swing:** The output voltage swing is limited by the NMOS source follower, in place to drive high impedance loads. In order to improve the output

voltage swing, a different type of output buffer would need to be designed. For example, a class AB output buffer could be designed using an NMOS and PMOS device, but greater control of currents would be required so that the output is proportional to the input by the gain and does not rail.

- **Biasing Circuit Efficiency:** Amongst the three main branches of circuitry (the TIA, the voltage amplifier, and the output stage) there are only five transistors that require bias voltages, and these five transistors only require three total voltages: Vbiasn1, which is 1.3V, Vbiasn2, which is 1.75V, and Vbiasp, which is 2.5V. Instead of designing five separate MOSFET voltage dividers, for efficiency, clarity, and practicality, only three separate MOSFET voltage dividers are necessary. Simply increasing the widths of the devices will allow only three dividers to bias the five transistors.
- **Step Response Overshoot:** Mainly on the falling edge of the step response, there is noticeable overshoot, both with and without a load. Further increasing the overdrive voltage, thereby increasing the amount of current flowing in the circuit, would speed up the falling edge and more critically damp the response so that overshoot is eliminated. This would also increase power consumption by increasing the total amount of current drawn by the AFE.
- **Power Consumption:** For current pulse amplitudes of 4μA and greater, the maximum current consumption requirement is not met. Several things can be done to improve power consumption. For starters, the widths of devices in the NMOS source follower can be decreased. However, this would decrease the slew rate while driving loads, along with the output rise time and fall time. Another option would be to decrease the widths of the devices used in the TIA stage. This would increase the input-referred noise and output noise of the AFE.