Switched-mode Power Supply

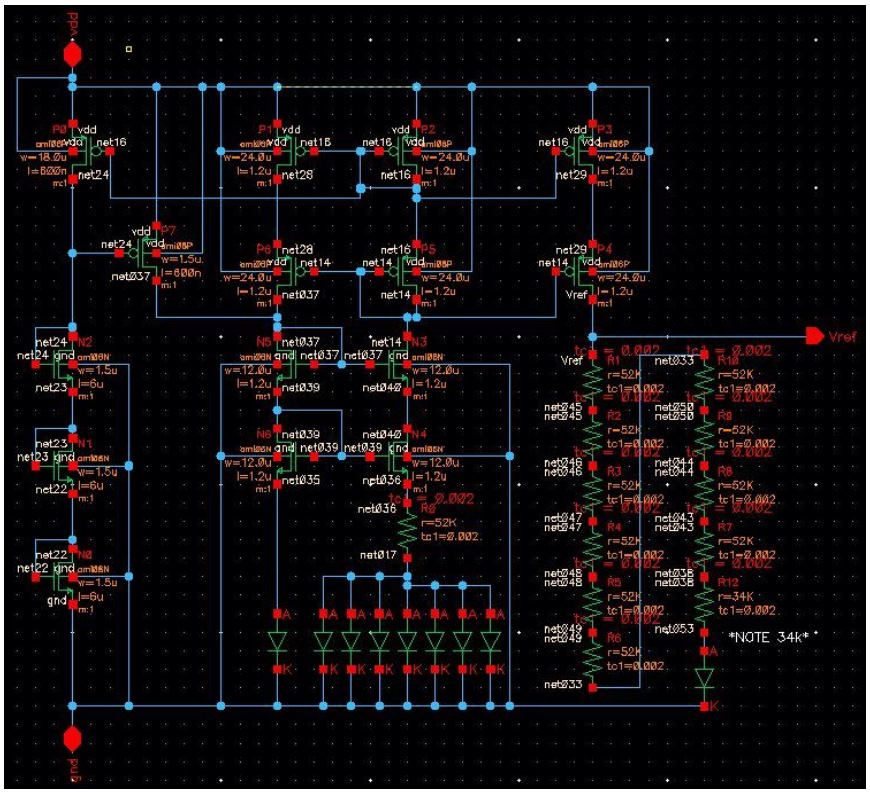
Using On Semiconductor's 500 nm process
EE 421 Digital Electronics and Digital IC Design (Fall 2017)
Course Project
By: Gonzalo Arteaga

Intro

This project involves designing a CMOS switching-mode power supply (Buck converter) with off-chip inductor and capacitor to generate a constant voltage of 3.75 volts. The circuit should operate at power supply voltages of 4 to 5.5 volts and for load currents of 0 to 100 milliamps.

Voltage Reference

The power supply's output voltage will be stabilized through the use of negative feedback. The output voltage will have to repeatedly be observed and compared to a voltage reference in order for the circuit to operate correctly. For this design a bandgap circuit was used for a voltage reference. This circuit generates a stable voltage reference of 1.25 volts that varies very little with changes in supply voltage and temperature. This is done by using a combination of PTAT and CTAT voltage references which when used together can create an almost invariable voltage. Using this voltage reference ensures that the output voltage of the power supply is compared to a constant voltage which will reduce the amount a variability in the output voltage.



Selecting Inductor and Capacitor

The output of the MOSFET switches will be connected to an LC low-pass filter. The equations used to determine the values of the inductor and capacitor are shown below.

$$V_L = L \frac{di}{dt}$$
$$L = \frac{V_L \Delta t}{\Delta i}$$
$$L = \frac{(VDD - V_o) D \cdot T_{CLK}}{\Delta i}$$

To select the value of the capacitor the following equations were used.

$$I_C = C \frac{dV}{dt}$$
$$C = \frac{I_C \cdot \Delta t}{\Delta V}$$
$$C = \frac{I_C \cdot (1 - D) \cdot T_{CLK}}{\Delta V}$$

Initially a nominal operating frequency was arbitrarily chosen so that the equations above could be used. For this design the operating frequency was chosen at 10 MHz. Using this value as well as the duty cycle (D) for a VDD of 5 volts resulted in the following,

$$L = \frac{(5 - 3.75)(0.75)}{(10\,MHz)(1\,mA)} = 93.8\,uH$$
$$C = \frac{(1\,mA) \cdot (0.25)}{(10\,MHz)(1\,mV)} = 25\,nF$$

The inductor value was rounded up to 100 uH and the capacitor was increased to 250 nF. After performing some simulations, these values were found to be too low as the operating frequency of the power supply was in the 100 kHz range.

The final components were selected through some trial and error with some intuition from analyzing the output as an RLC circuit. The final components chosen were a 4.7 uF capacitor and a 470 µH inductor.

Current Ripple		
	F = 100 kHz	F = 1MHz
VDD = 4 v	4.99 mA	499 µA
VDD = 5.5 v	25.4 mA	2.54 mA

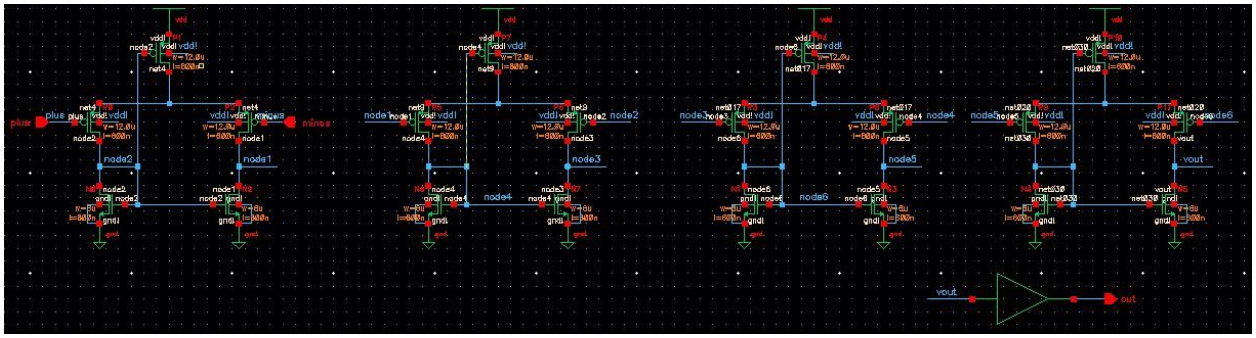
* assuming $I_C = 1\,mA$

Voltage Ripple		
	F = 100 kHz	F = 1MHz
VDD = 4 v	133 uV	13.3 uV

VDD = 5.5 v	677 uV	67.7 uV

Comparator Design

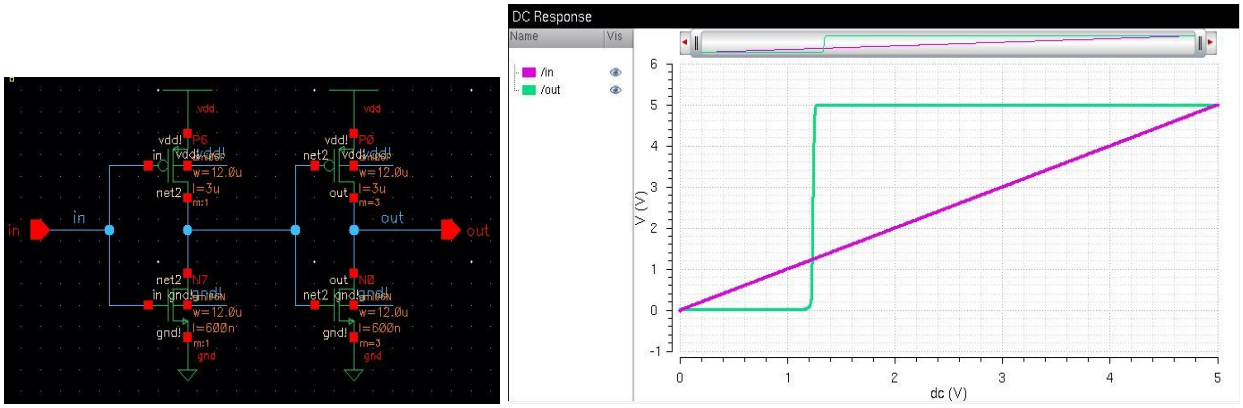
To determine the difference between the output voltage and the desired voltage, a comparator was used. Through the use of feedback, the output of the power supply is fed into the input of a comparator through a voltage divider with a gain of (⅓) producing a voltage of 1.25 volts. This voltage is compared to the bandgap voltage which is also 1.25 volts. Any difference between the inputs of the comparator will be amplified through the comparators. The comparator design used is shown below.



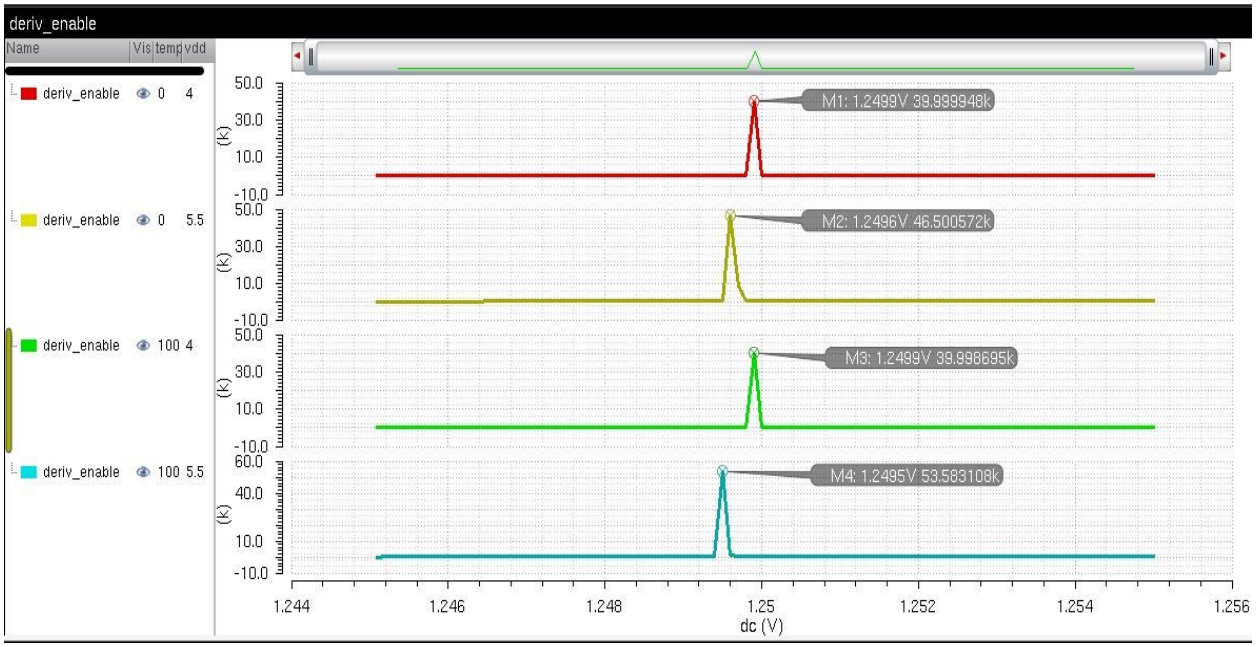
A self-biasing PMOS comparator was used for this design. The PMOS differential pair was chosen over the NMOS differential pair because its common-mode voltage range extends lower to ground which is appropriate when the input voltages to the comparator will be at 1.25 volts.

Because the gain of the individual comparator was roughly 20, four stages were cascaded to increase the overall gain. Increasing this gain means that the comparator will be able to detect smaller differences between the output and the voltage reference resulting in smaller ripple voltage. The drawback to using multiple stages is that there will be an increased amount of delay through the feedback loop. This could mean having an operating frequency that is lower than desired. To work around this, the device sizes were kept at minimum length for high speed operation.

Inverters were placed on the output of the comparator so that it would be able to switch the output MOSFET either ‘on’ or ‘off’. Since the output of the comparator swings closer to ground, the switching point of these inverters was lowered by increasing the strength of the NMOS and decreasing the strength of the PMOS. Also, a second inverter was implemented to sharpen the transition from low-to-high or high-to-low so that it can approximate an ideal inverter.



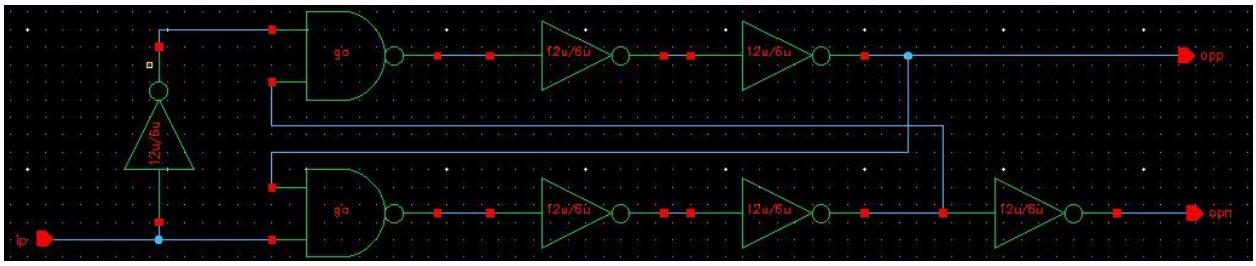
Pictured above is the output buffer of the comparator and a simulation showing its lowered switching point voltage of 1.2 volts and a steep transition from low-to-high.



The performance of the comparator with output buffer was simulated while varying the power supply voltage and temperature. From the results above, the gain increases with the power supply and the increases in temperature produce very small to no decreases in gain.

Lockout Circuit

During the switching of the NMOS and the PMOS, there is point where both devices are on. This causes a significant spike of unwanted contention current to flow through both devices. This causes power to be dissipated across the MOSFETs thus reducing the efficiency of the circuit. To solve this, a lockout circuit was designed which would ensure that the MOSFETs were never in the 'in between' state by turning off one device before turning on the other.
The schematic of the lockout circuit is shown below.



Sizing the PMOS and NMOS switches

When determining the size of the output MOSFETs, the switching resistance had to be considered. The transistors had to be capable of supplying up to 100 mA while maintaining a low voltage drop from drain to source (or source to drain). The following calculations were used to size the PMOS transistor.

$$R_P' = 40k \frac{L}{W}$$

For a VDD of 4.5 v, the voltage across the PMOS at full current load is approximately,

$$V_{sd} = 4.5 - 4.2 = 0.3\,v$$
$$R_P = \frac{V_{sd}}{I} = 0.3/0.1 = 3\,\Omega$$

Using the switching resistance of the PMOS one can then solve for the width of the device assuming minimum length.

$$W = \frac{40\,k}{3} = 13333$$
$$Actual\ Width = 13333(0.6\,um) = 8000\,um$$

Adjusting this width so that it is a multiple of 0.6 um and using 100 parallel devices, the final device width is,

$$W(actual) = 80.4\,um\ with\ M = 100$$

Since the switching resistance for the NMOS is half that of the PMOS, the device width of the NMOS was chosen to be,

$$W(actual) = 40.2\ um\ with\ M = 100$$

Transient Response

The transient response of the output voltage can be approximated as an RLC circuit where the resistance (R) is the switching resistance of the NMOS or PMOS.
The transfer function of this circuit is shown below,

$$\frac{V\,out}{V\,in} = \frac{(1/LC)}{s^2 + (R/L)\,s + (1/LC)} = \frac{\omega_n^2}{s^2 + 2\,\zeta\omega_{\,n} + \omega_n^2}$$

Equating the approximated transfer function to the 2nd Order transfer function equation we get,

$$\omega_{\,n} = 1/\sqrt{LC}$$
$$\zeta = \tfrac{1}{2}\sqrt{\tfrac{R^2C}{L}}$$

Using the device sizes above led to transient responses that had a very large overshoot. One effort made to reduce this was to obtain a ratio between the capacitor and the inductor that would yield a critically damped response (ζ=1). Using the switching resistances of the devices (3 Ω), and setting the damping ratio to one yielded a ratio of,

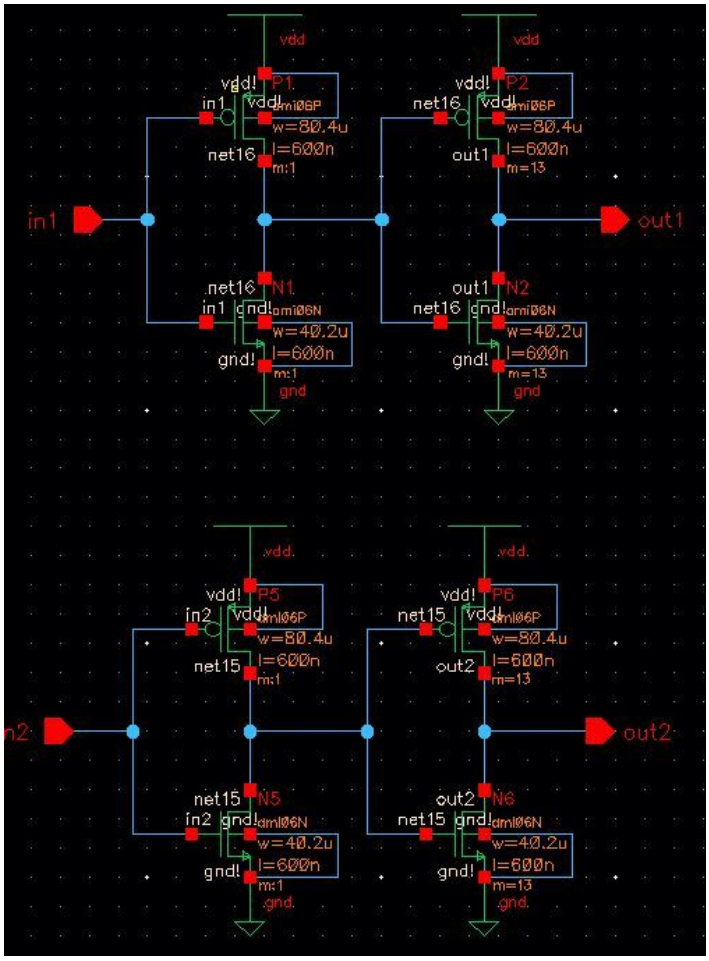
$$C = 0.444\,L$$

Although the final values selected for the inductor and capacitor don't adhere to the above ratio, the overshoot was still greatly reduced by trying component values near this ratio. This approach also helped further understand the transient response of the power supply.

Driving the switches

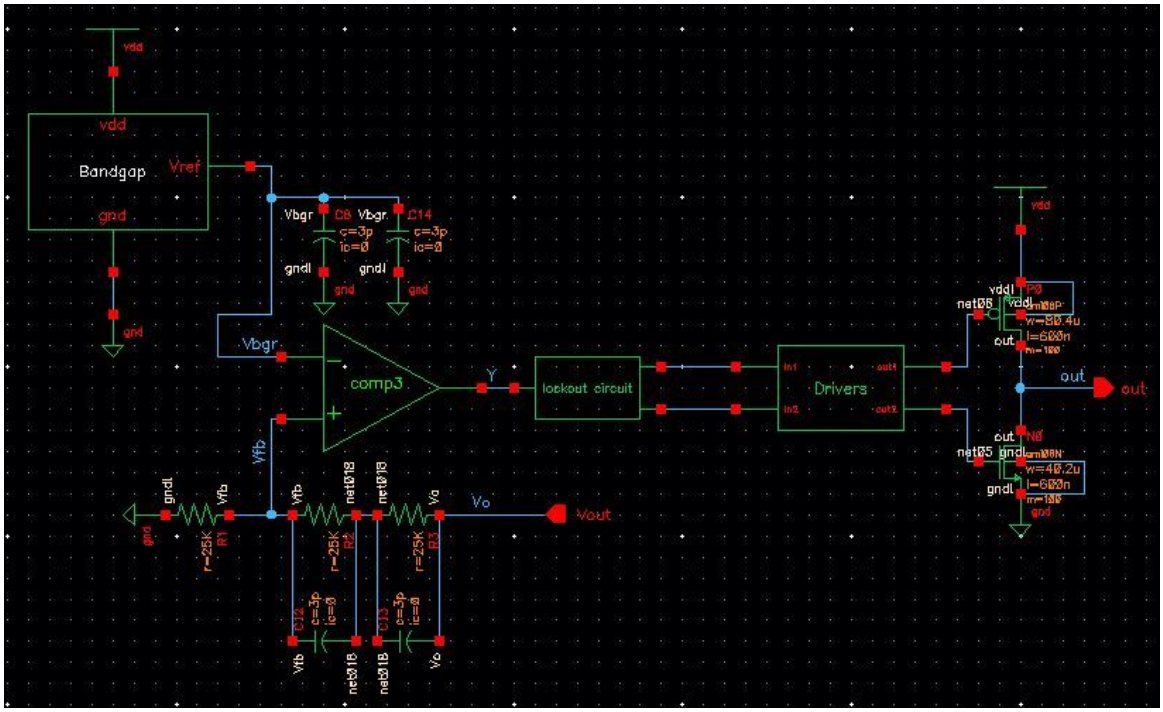
Increasing the sizes of the output MOSFETS means that their input capacitance has also increased. This input capacitance serves as a large load capacitance to the inverters in the lockout circuit. Simply connecting the lockout circuit directly into the gates of the devices won't be enough to switch the MOSFETs on and off. A set of buffers must be designed to go after the lockout circuit and before the output MOSFETs.
Starting from the sizes of the output MOSFETs, each previous stage's size was decreased by a factor of eight until the standard inverter size of 12u/6u was reached. A total of two inverters were added so that there wouldn't be any inversion between the lockout circuit and the gates of the MOSFETs.

The drivers schematic is shown below,


vdd
vdd!
P1
in1
nmi06P
w=80.4u
l=600n
net16
m:1
P2
net16
out1
m=13
in1
out1
N1
gnd!
nmi06N
w=40.2u
l=600n
gnd
N2
P5
in2
net15
P6
out2
N5
N6

Power Supply Circuit

The switch mode power supply was finally assembled with all the previous circuits as shown below.

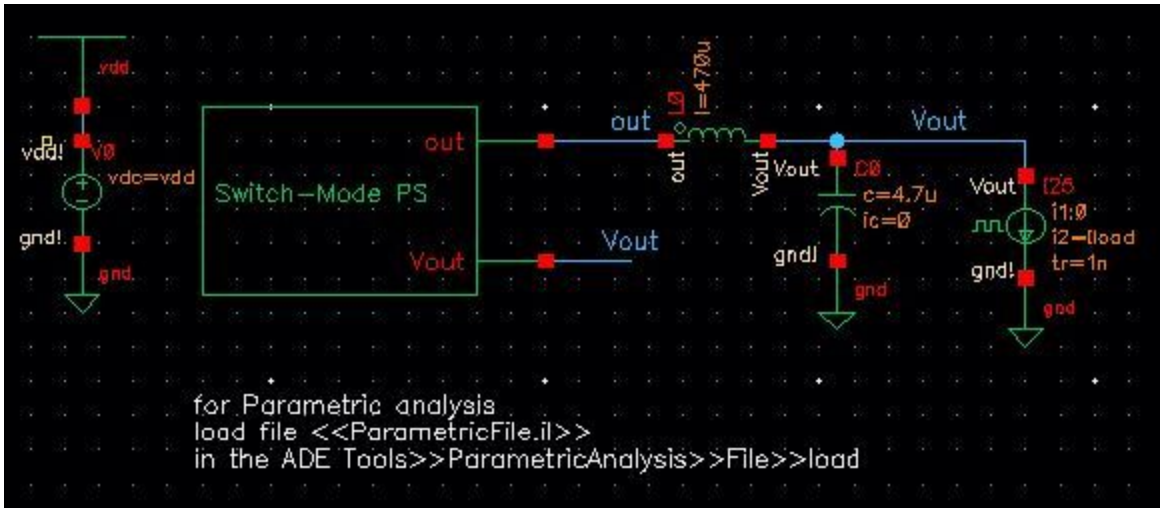


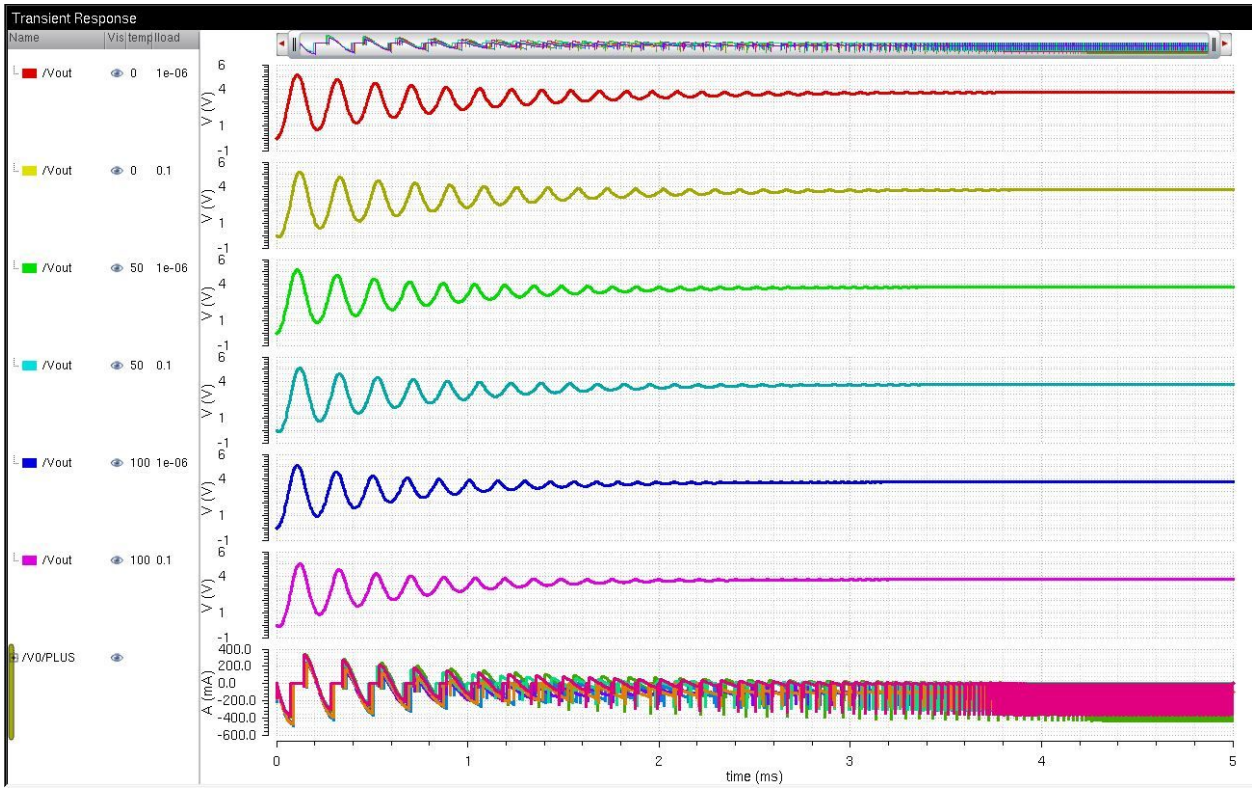
In the feedback loop, a voltage divider consisting of three 25kΩ resistors was used to generate the gain of ⅓ . The total resistance of 75 kΩ ensures that the amount of current drawn by the feedback loop is 50 µA. In addition, the value of these resistors also affects the delay since there is an RC delay from the parallel combination of the resistors and the input capacitance of the comparator. Selecting the resistors at 25 kΩ keeps the delay small while only drawing the maximum allowable current of 50 µA.

Capacitors (3 pF) were added across the resistors in the feedback loop to further reduce the delay across the loop. An additional 6 pF capacitor was placed from the output of the bandgap voltage reference to ground to reduce any ripple due to noise from the comparator. This improved the design by reducing the output voltage ripple.

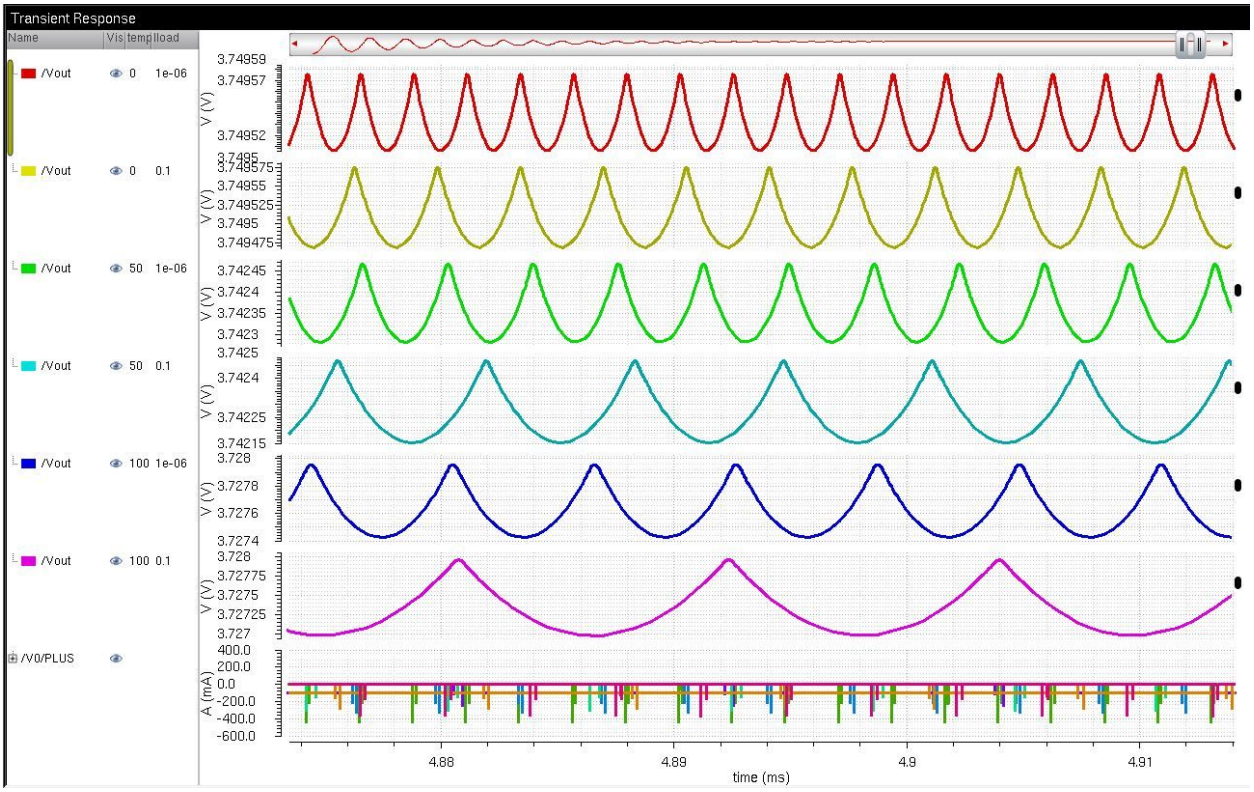
Simulations

The final design was simulated using the schematic shown below.





The above simulation shows a parametric analysis where the power supply voltage is held at 4 volts while varying the temperature and the load current. From this plot one can see the underdamped transient response at the start of the simulation. Because of this, the output voltage overshoots to 5 volts.

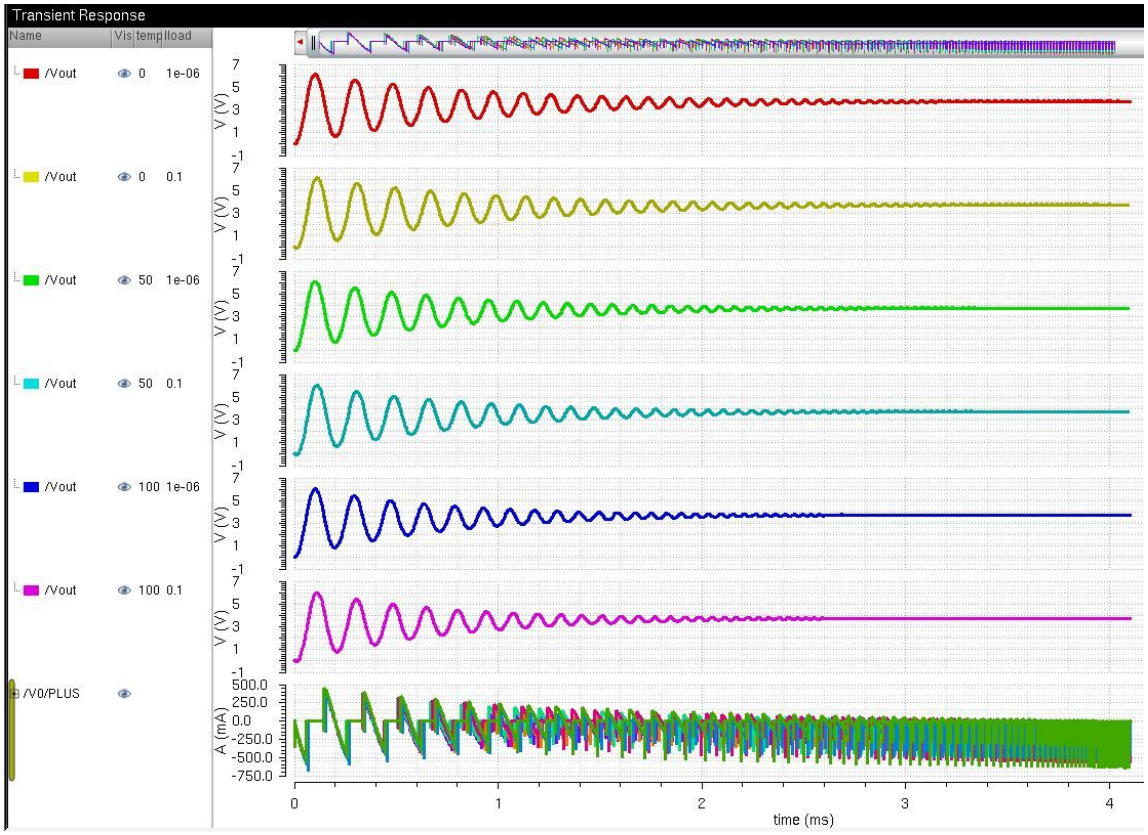


Shown above is the zoomed in view of the previous simulation for better clarity. Using this plot the following data was recorded.

vdd	Temp (celsius)	Load Current	Vavg	Voltage ripple (v)	Freq. (Hz)	T(s)
4	0	1uA	3.7495	68.8 µ	439 k	2.28µ
4	0	100mA	3.7495	105.4 µ	284 k	3.52µ
4	50	1uA	3.742	182.6 µ	273 k	3.66µ
4	50	100mA	3.742	313.2 µ	157 k	6.38µ
4	100	1uA	3.727	528.1µ	164 k	6.11µ
4	100	100mA	3.727	960.1µ	86.2 k	11.6µ

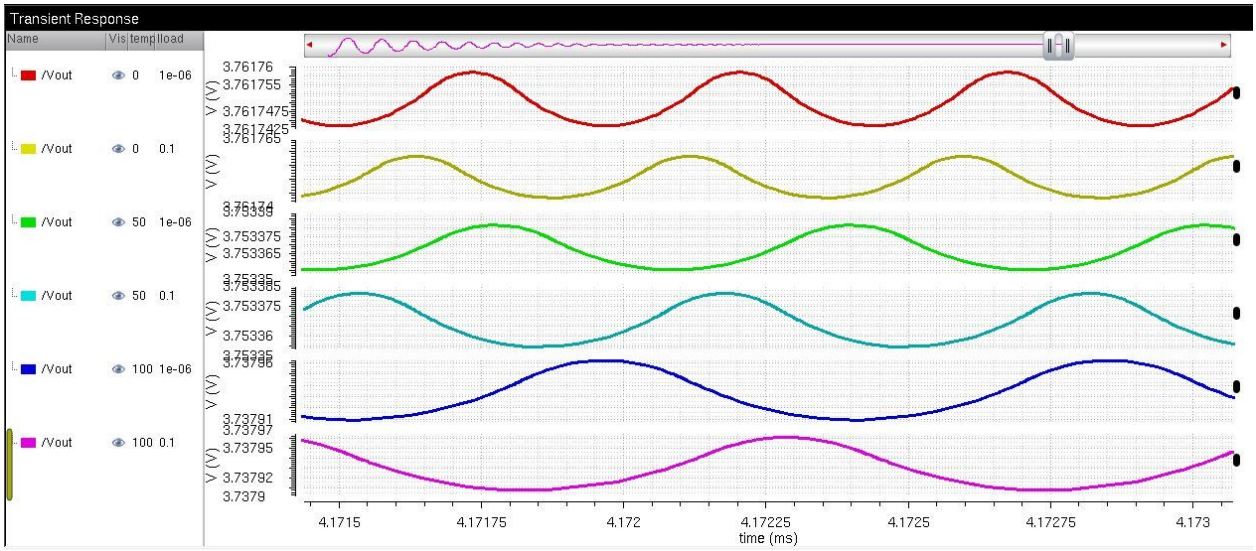
At a VDD = 4 v, the power supply generates a voltage of 3.74 volts with minimal voltage ripple. In the worst case the ripple voltage varies by just under 1 mV at full load and at 100 degrees celsius. The operating frequency also stays around 100 kHz which was on the low end of the desired frequency range.
Regarding temperature, the average output voltage seems to decrease with increases in temperature.

The same simulation was run again at the maximum power supply voltage of 5.5 volts.



This simulation again show the underdamped transient response at the start of the power supply. This time the output voltage overshoots to 6 volts.

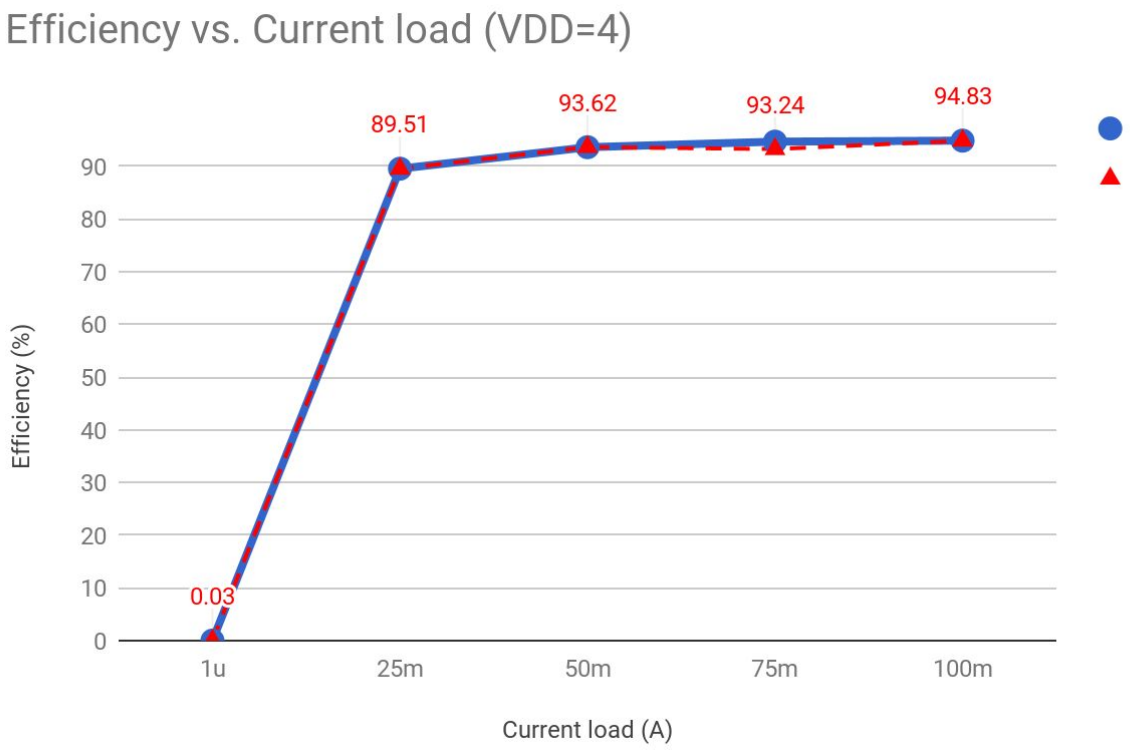
A zoomed in view of this simulation is shown below along with a table of data collected from the simulation.



Shown above is a zoomed in view of the simulation with VDD=5.5 v.

vdd	Temp (celsius)	Load Current	Vavg	Voltage ripple (v)	Freq. (Hz)	T(s)
5.5	0	1uA	3.762	15 µ	2.08 M	481n
5.5	0	100mA	3.762	15 µ	2.08 M	481n
5.5	50	1uA	3.7533	26.1µ	1.558 M	642n
5.5	50	100mA	3.7533	26.7µ	1.558 M	642n
5.5	100	1uA	3.7379	53.7µ	1.130 M	885n
5.5	100	100mA	3.7379	53.7µ	1.096 M	912 n

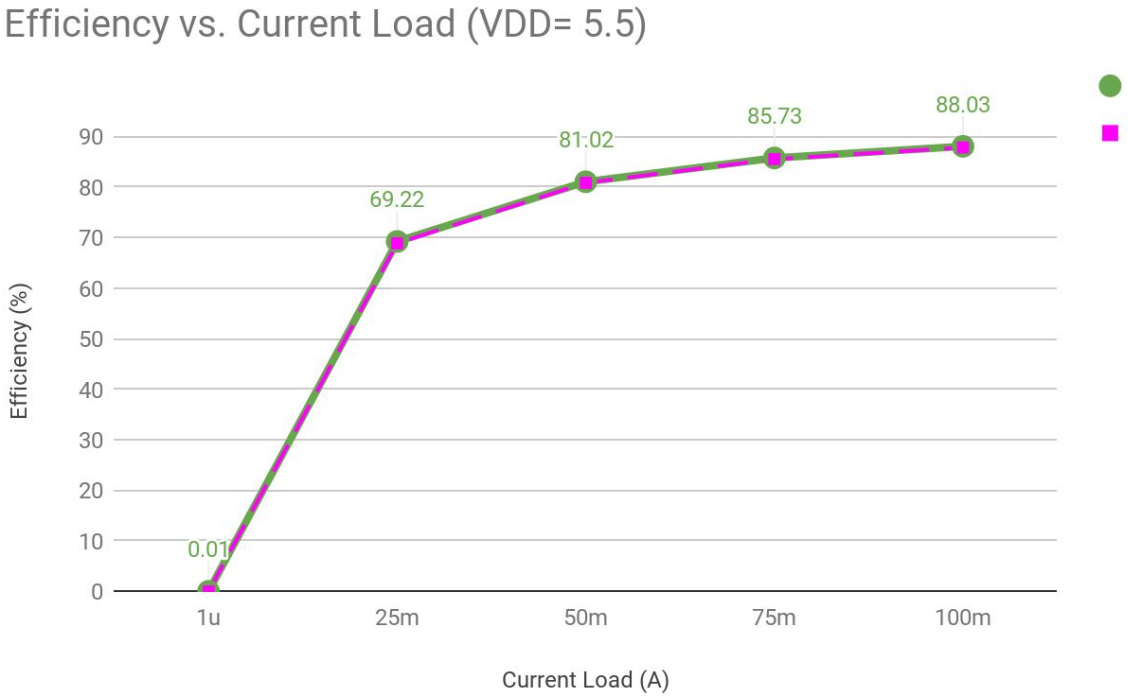
At a VDD of 5.5 volts the power supply generates a more stable output voltage with voltage ripples in the tens of microvolts. The operating frequency is also in the MHz range.
Once again, increases in the operating temperature caused the average output voltage to drop by tens of millivolts.



vdd=4	temp=0	temp=100
current load	efficiency	efficiency
1u	0.03	0.03
25m	89.52	89.51
50m	93.59	93.62
75m	94.65	93.24
100m	94.84	94.83

The chart above shows a plot of the power supply's efficiency with varying current loads at a VDD of 4 volts. From the data in the chart, we see that the efficiency is generally at or over 90% with loads that draw at least 25 mA. The best efficiency achieved was 94.83% at full load current.

The efficiency didn't change much with changes in temperature but higher temperatures yielded slightly less efficiencies.



vdd=5.5	temp=0	temp=100
current load	efficiency	efficiency
1u	0.01	0.01
25m	69.22	68.85
50m	81.02	80.81
75m	85.73	85.5
100m	88.03	87.79

The chart above plots the efficiency of the power supply with varying current load at a VDD of 5.5 volts. At this VDD, the efficiencies drop to around 70 to 80% with a peak efficiency of 88.04% at full load. In this chart we can see again that the efficiencies decreased slightly with increases in temperature.

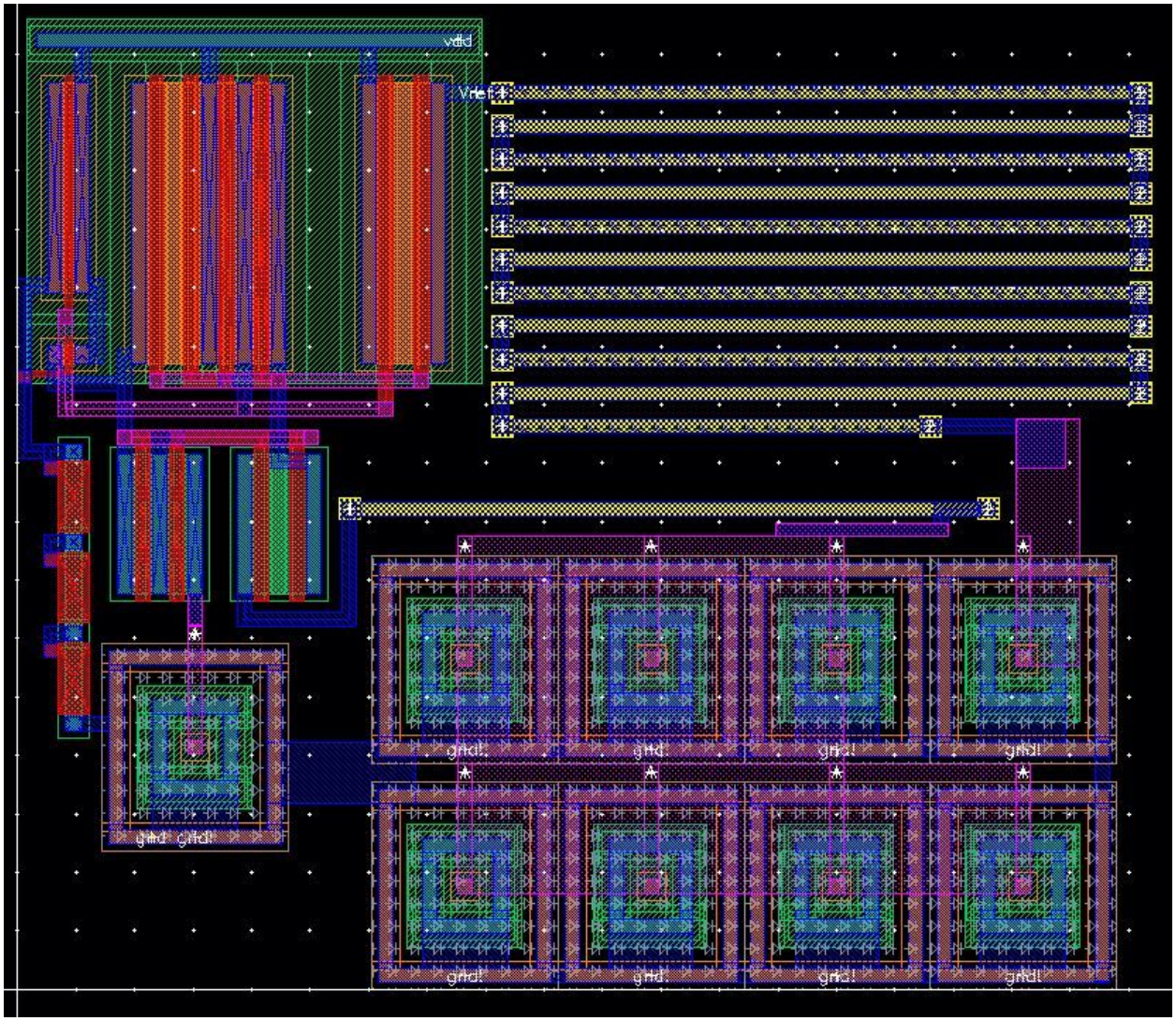
Conclusion

Regarding the performance of the design, the efficiency of the power supply at a VDD of 5.5 volts has some room for improvement. An optional addition that could help the efficiency is by implementing zero voltage switching. The operating frequency of the power supply might have also been improved by reducing the number of stages in the comparator and increasing the gain by using higher length devices for the current source.

Overall the project helped me learn a lot about how buck converters worked and it helped reinforced was I learned in the lecture class.

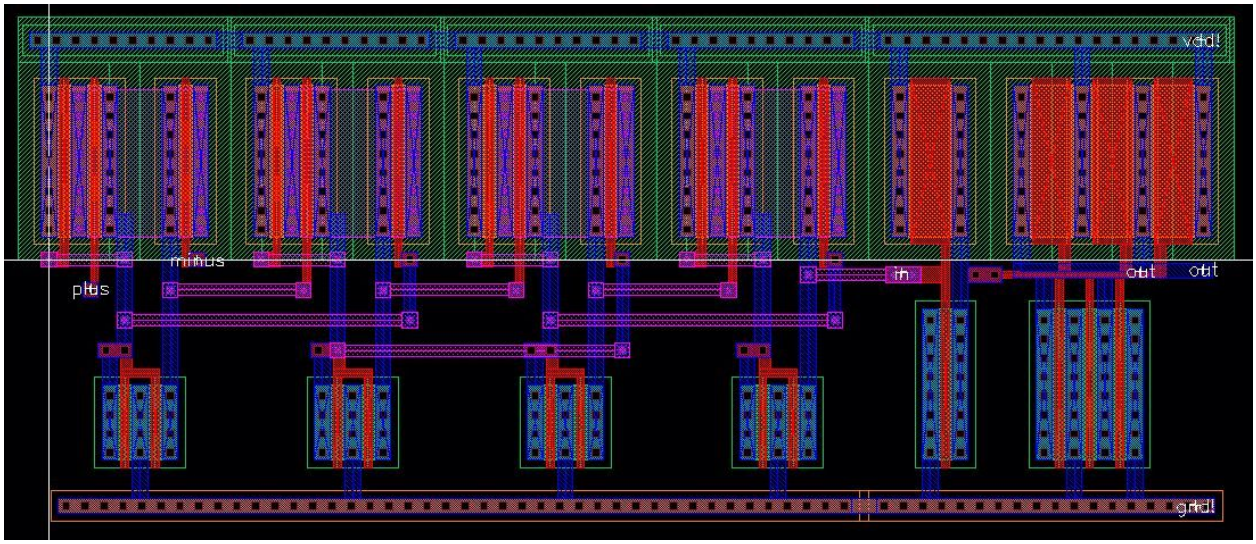
Layouts:

Bandgap Voltage Reference



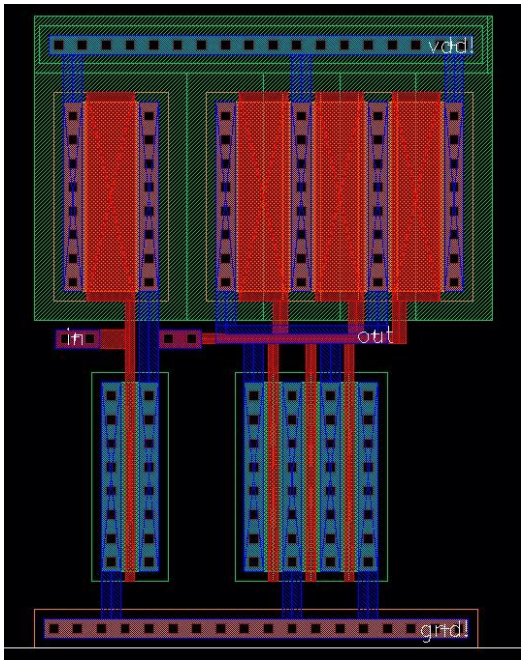
Pins	Location
vdd!	top ntap rail
gnd!	ptaps on the diodes
Vref	left side of top-most electrode resistor

Comparator with Output inverters



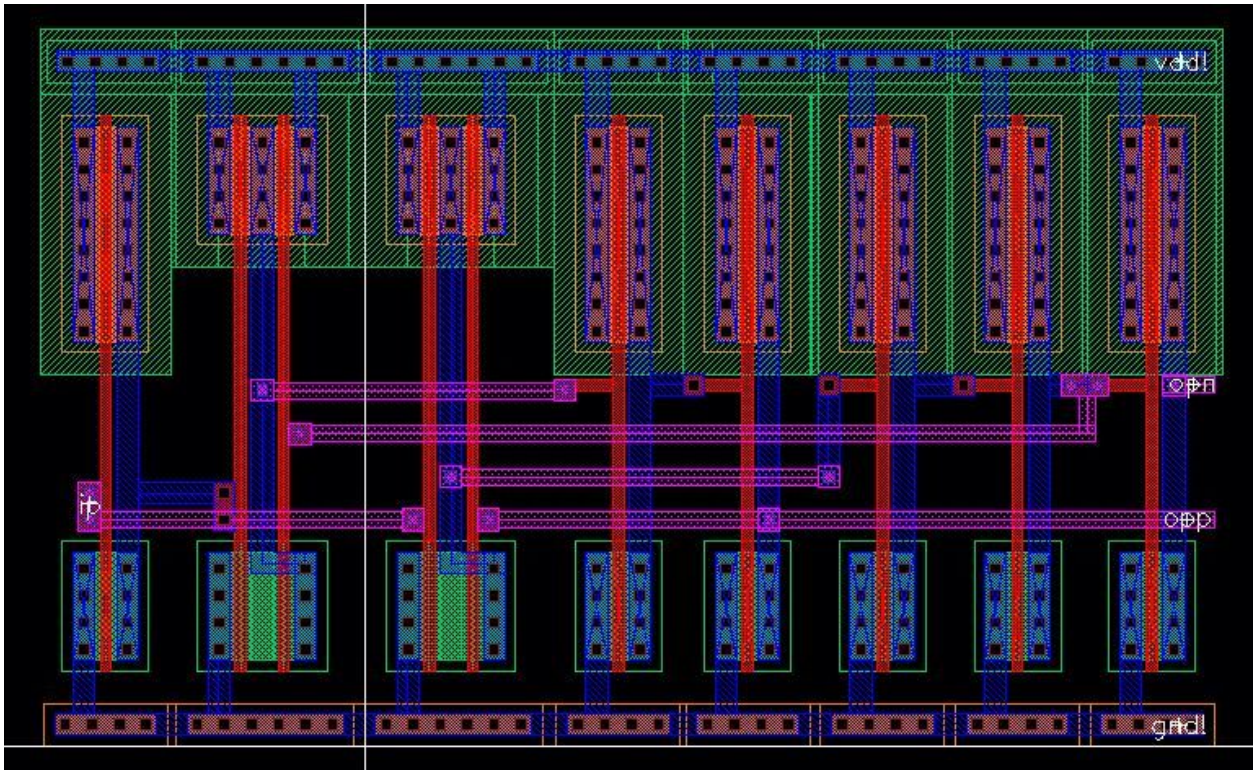
Pins	Location
vdd!	top ntap rail
gnd!	bottom ptap rail
plus	pmos gate m1_poly on the far left
minus	pmos gate m1_poly on the left
out	horizontal metal_1 wire on the right

Inverters on the output of the comparator



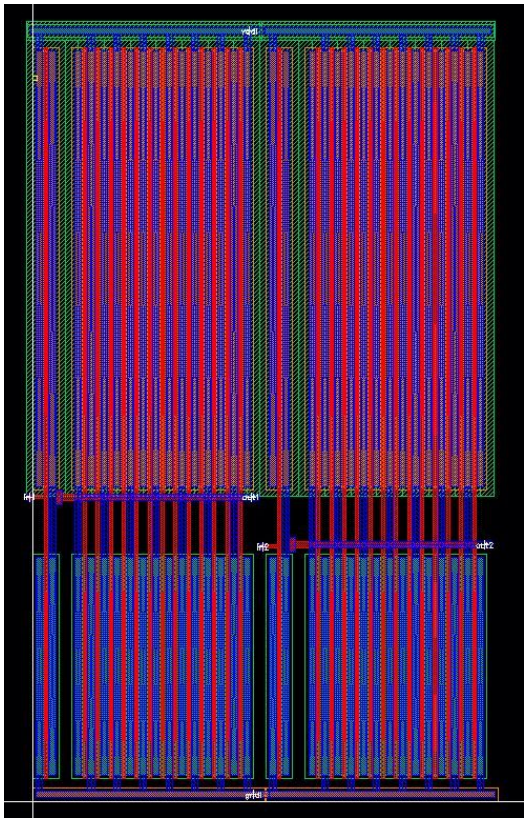
Pins	Location
vdd!	top ntap rail
gnd!	bottom ptap rail
in	left m1_poly connection
out	m1 wire joining the inverters on the right

Lockout Circuit



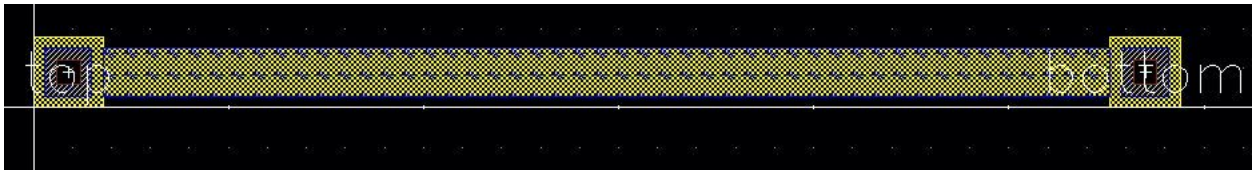
Pins	Location
vdd!	top ntap rail
gnd!	bottom ptap rail
ip	left m2_m1_poly connection on gate of first inverter
opn	right m2_m1 connection just under the nwell
opp	right m2 wire just above the NMOSs

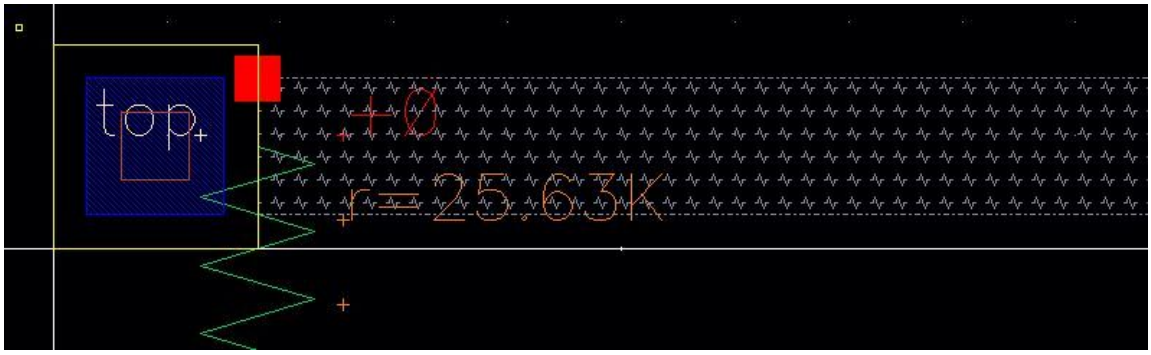
Drivers



Pins	Location
vdd!	top ntap rail
gnd!	bottom ptap rail
in1	left-most m1_poly on first inverter
out1	metal_1 joining the left side inverters together.
in2	middle of layout. Just above the middle NMOS.
out2	metal_1 joining the right side inverters together.

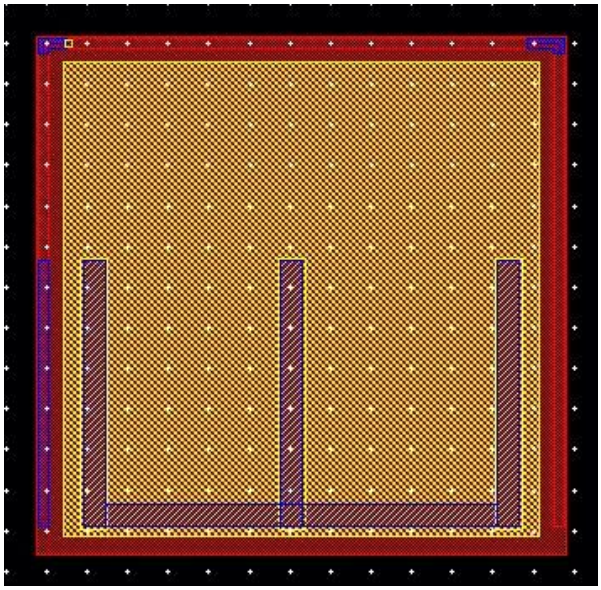
25KΩ Resistors





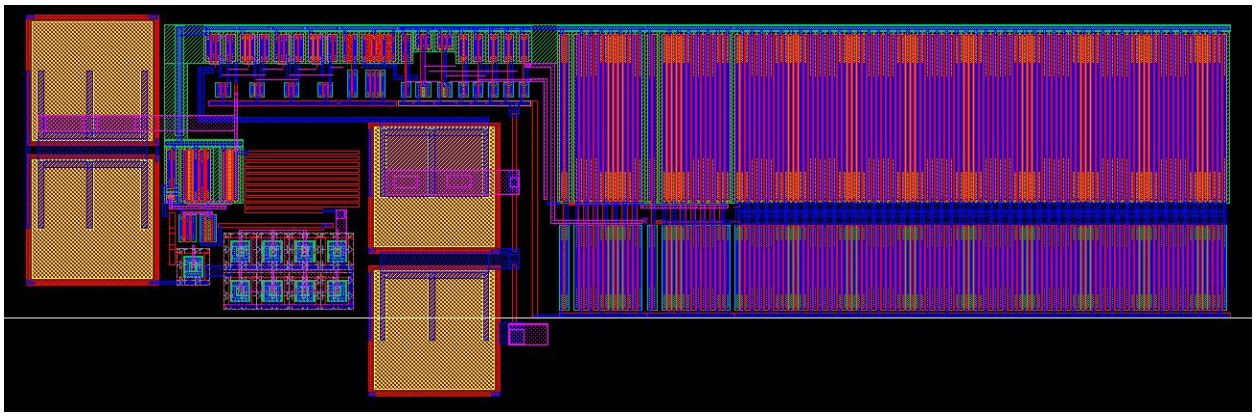
Dimensions/value of Resistor:
Width: 1.2 um
Length: 25.8 um
Extracted resistance: 25.63 k

3 pF Capacitor

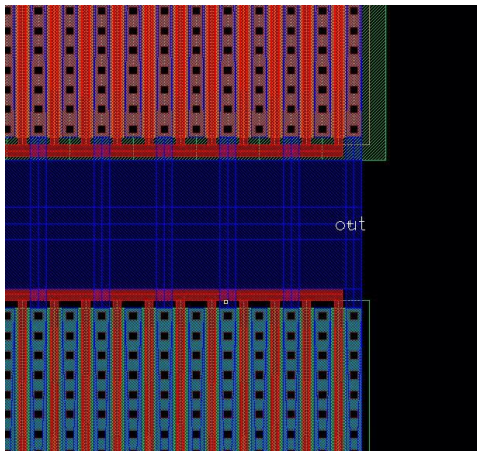


Dimensions/value of Capacitor:
Width: 58.8 um
Length: 58.35 um
Extracted capacitance: 2.738 pF

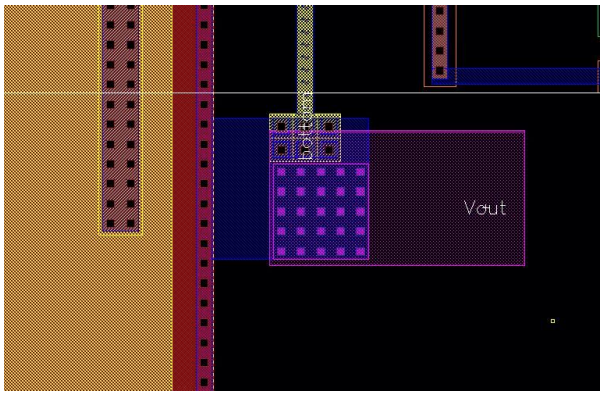
Switch-mode Power Supply



Pins	Location	info
vdd!	top ntap rail	
gnd!	bottom ptap rail under output NMOS	
	ptaps around diodes in bandgap	
out	horizontal metal_1 wire on right between the PMOS and NMOS	connects to inductor
Vout	metal_2 square on right side of bottom-most capacitor	connects to inductor and capacitor



Zoomed in view of pin “out”



Zoomed in view of pin “Vout”

DRC and LVS results for the final layout:

```
DRC started.......Sun Nov 26 20:17:50 2017
    completed ....Sun Nov 26 20:17:51 2017
    CPU TIME = 00:00:00  TOTAL TIME = 00:00:01
*********   Summary of rule violations for cell "smps layout"   *********
  Total errors found: 0
```

```
    Net-list summary for /home/arteag1/CMOSedu/LVS/schematic/
       count
         59              nets
         4               terminals
         15              res
         4               cap
         9               diode
         37              pmos
         32              nmos


    Terminal correspondence points
    N57       N8        Vout
    N55       N1        gnd!
    N58       N5        out
    N56       N0        vdd!

Devices in the netlist but not in the rules:
        res diode
Devices in the rules but not in the netlist:
        nfet pfet nmos4 pmos4

7 net-list ambiguities were resolved by random selection.

The net-lists match.
```