Low-Voltage Op-Amp Design

Using On Semiconductor's 500 nm process
EE 420 Engineering Electronics II and Analog IC Design (Spring, 2017)
Course Project
By: Gonzalo Arteaga

MOSFET Parameters for low-voltage, High gain design VDD = 2 V scale factor = **600nm**			
Parameter	**NMOS**	**PMOS**	**Comments**
Bias Current Id	10 uA	10 uA	
W/L	48/2	360/2	
Actual W/L	28.8u/1.2u	216u/1.2u	
Vds,sat Vsd,sat (overdrive voltage)	50 mV	50 mV	2.5% of VDD
Vgs Vsg	800 mV	950 mV	
Vthn Vthp	750 mV	900 mV	
KPn and KPp	333 uA/V^2	44.4 uA/V^2	
Cox'	2.4831 fF/um^2	2.4831 fF/um^2	
Coxn and Coxp	85.82 fF	644 fF	
Cgsn and Csgp	57.21 fF	430 fF	
Cgdn and Cdgp	5.76 fF	62.6 fF	
gmn and gmp	214 uA/V	217 uA/V	
ron and rop	400 k	725 k	@ 10 uA
gm ro	85.6	157.3	open circuit gain
lambda	0.25 V^{-1}	0.138 V^{-1}	
ftn ftp	210 MHz	46 MHz	

Summary of Results				
	No load (2 v VDD)		**1k load (5 v VDD)**	
DC Open Loop Gain	102 dB		80.3 dB	
Gain-Bandwidth Prod. (f_{un})	5 MHz		13 MHz	
	VDD=2v	VDD=3 v	VDD=4v	VDD=5v
CMRR (at 100 kHz)	78 dB	94 dB	83 dB	78 dB
PSRR+ (at 100 kHz)	51 dB (2 volts VDD)			
PSRR- (at 100 kHz)	28 dB (2 volts VDD)			
Max Slew Rate at Max Load	4 V/us			
Input CMR	CMRmax = VDD + 700 mV		CMRmin = - 850 mV	
Output Swing	For linear operation, operate within 50 mV of VDD and ground			
	For 2<VDD<3.2		**For VDD = 5**	
Power	600 uW to 960 uW		P = 5.1 mW	

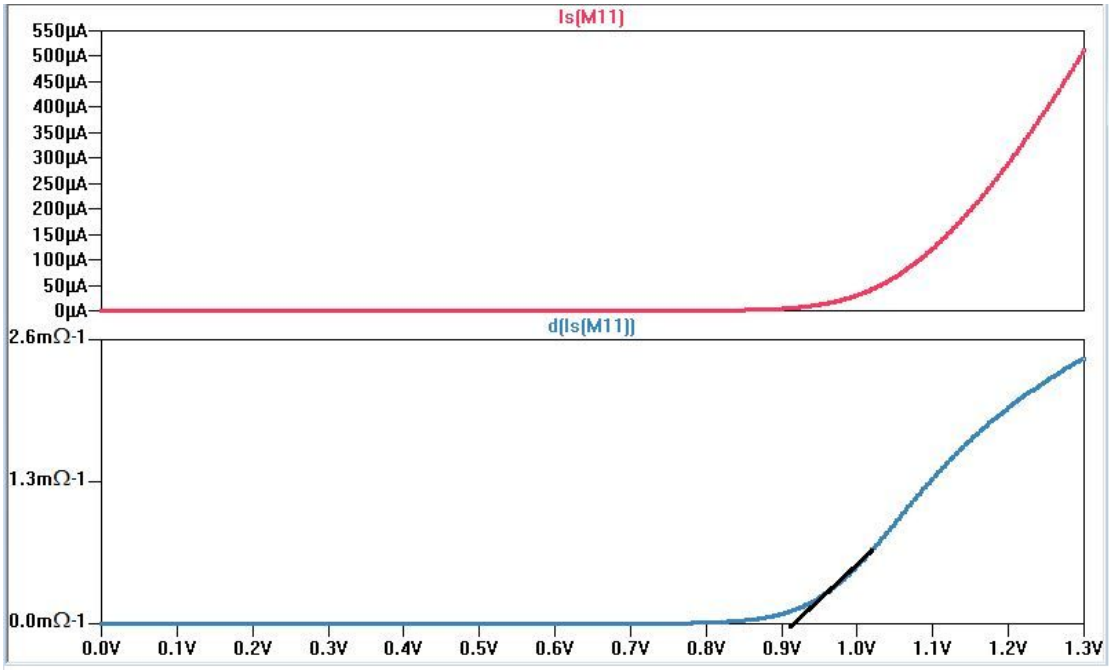
Selecting Device Parameters

The first step in designing the op-amp is to determine the appropriate device parameters for the application. Since this particular design calls for low-voltage and high gain, the device parameters should to reflect these specifications as opposed to a design where high speed is prioritized.

Threshold and Gate-Source Voltages

Before the gate-source or overdrive voltages are selected, the threshold voltages of the devices should be determined. In order to determine the threshold voltages of the NMOS and PMOS devices, we perform a DC sweep of the Vgs (or Vsg) and plot the drain current. Then one can take the derivative of the drain current with respect to Vgs and draw a line tangent to the curve towards the horizontal axis. The point where this tangent line intersects the axis is where the threshold voltage is determined.

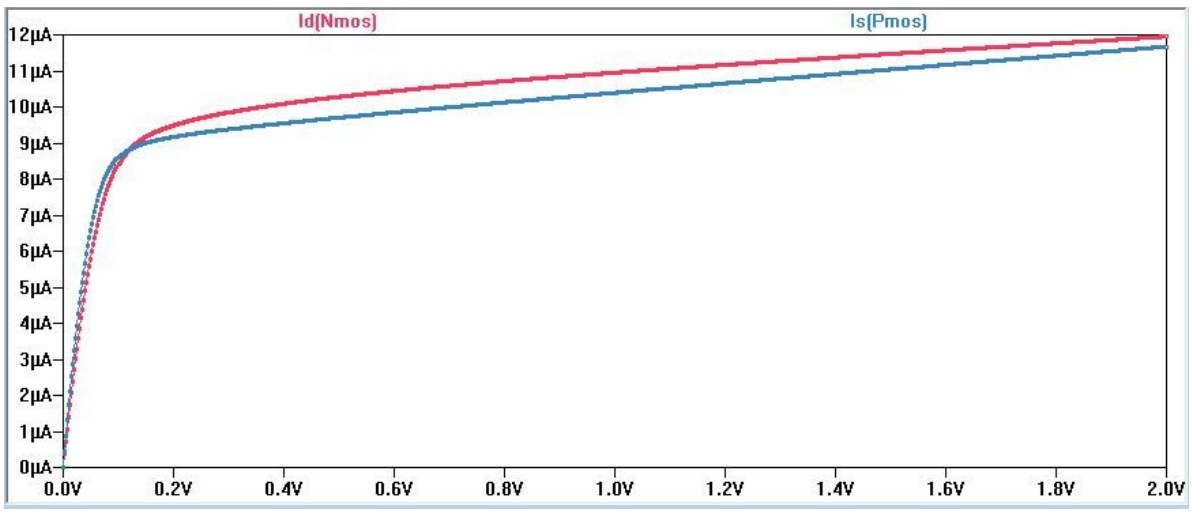
For the C5 process used in this design, the threshold voltages were 750 mV and 900 mV for the NMOS and PMOS devices respectively.



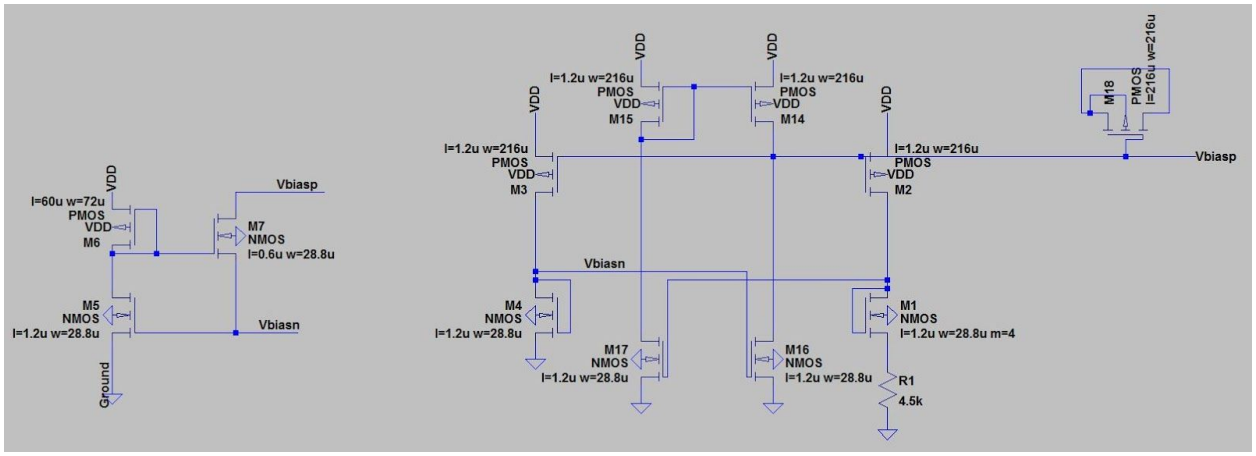
The next step in the design was in selecting the overdrive voltages. Knowing that for general design, an overdrive voltage of roughly 5% of VDD is used, the overdrive voltage would have to be a smaller percentage of the power supply in order to provide high gain and be low voltage. For this design the overdrive voltage chosen was 50 mV or 2.5% of the 2 volt power supply. Knowing the threshold voltages and the overdrive voltages, the gate-source voltages for the NMOS and the PMOS were set at 800 mV and 950 mV respectively.

Selecting device length (L)
For general design, the length is chosen to be between 2 to 5 times the minimum length. For this design, the length was chosen to be 2 times the minimum length of 600 nm. Using larger lengthed devices, while being beneficial for high gain purposes, would mean that the device widths would also have to increase in order to sink the same amount of bias current.

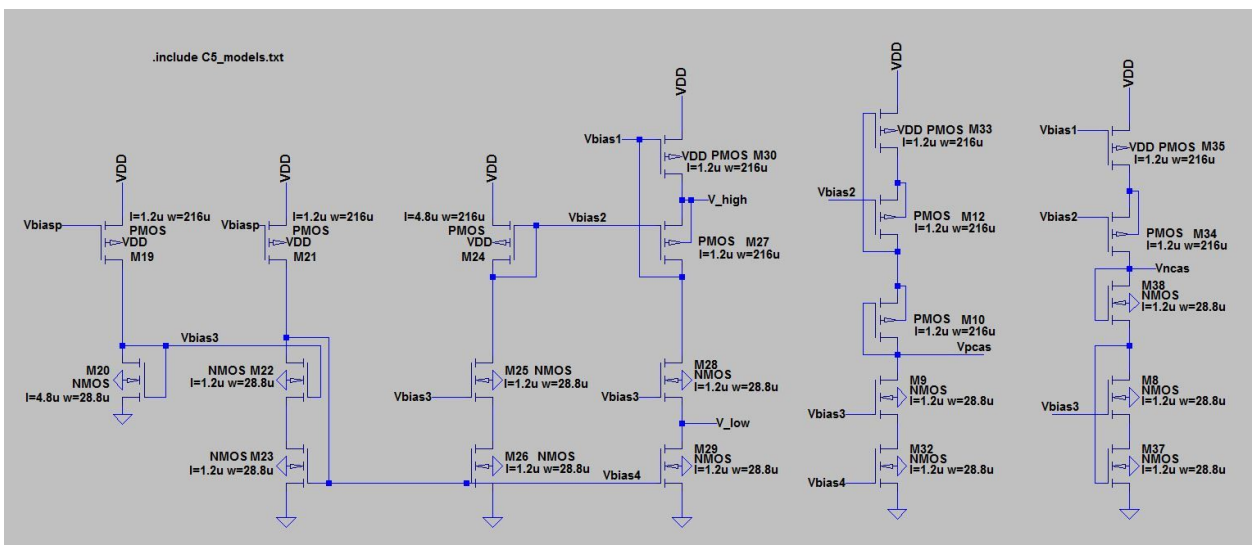
Selecting width (W)
Since the width does not influence the open circuit gain or speed, the width is determined by the amount of bias current necessary to achieve the slew rate specification. The design calls for a slew-rate greater than 1 volt per microsecond. To achieve this the bias current would have to be 10 uA. Using the gate-source voltages and the device lengths, the width was then sized until the devices produced approximately 10 uA of current.
Having these parameters, a table similar to table 9.1 in the textbook could be generated.

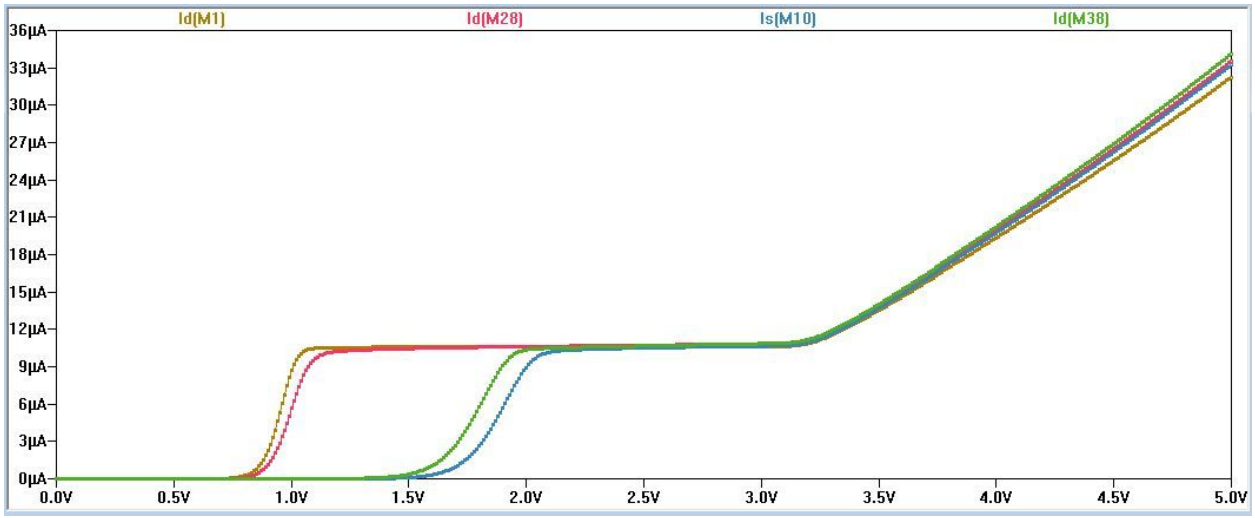


Building a Voltage Reference
Before the actual op amp is built, the biasing circuit must be built in order to provide voltage references for the rest of the circuit. The goal is to provide a biasing circuit to the op-amp where the voltages and currents won't vary with changes in power supply voltage. When using a beta-multiplier to create a stable current reference, the currents would vary quite a bit with changes in VDD since short-channel MOSFETs have small output resistances. In order to provide more stable currents that are less sensitive to the power supply voltages, a differential amplifier was added to the beta multiplier circuit.



From the beta-multiplier, a biasing circuit comprised of wide swing cascode current mirrors was used to make voltage references that would then bias the rest of the design. In order to generate voltages such as Vpcas, the bodies of all the PMOS devices were tied to their source. This would eliminate the body effect that would cause voltages such as Vpcas to take up the entire power supply voltage.

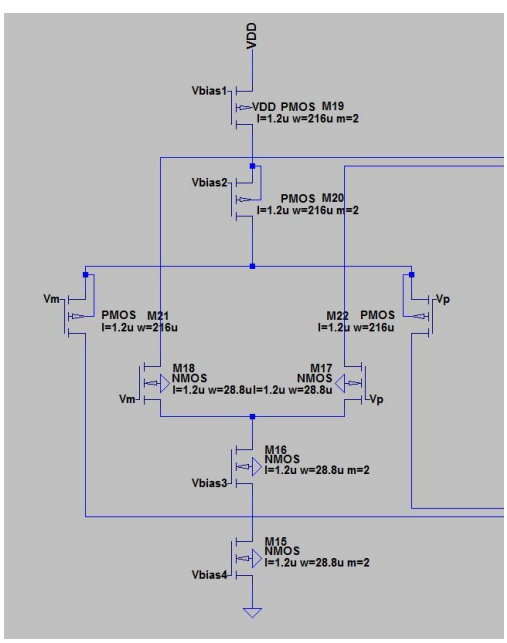




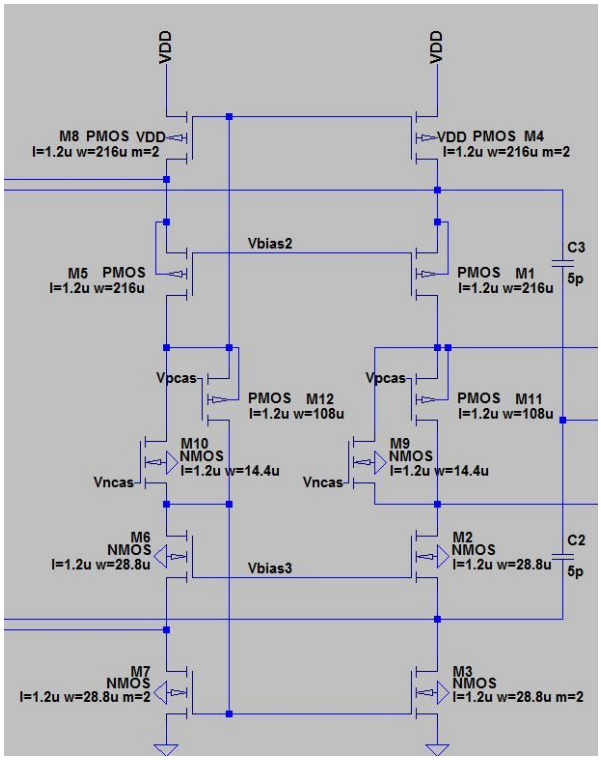
In the simulation above, as you sweep the power supply voltage, the bias current stays constant over voltages of 1 to 3.2 volts but since some branches of the biasing circuit require a minimum voltage of 2 volts to operate, the power supply voltage should stay within 2 and 3.2 volts for the bias current to remain constant.

Input of the Op-Amp

The input terminals of the op-amp consist of two differential amplifiers. An NMOS and PMOS diff amp are used in conjunction so that the op-amp could operate over a larger amount of input values. If the input voltages go up towards VDD, then the PMOS diff-amp would turn off but the NMOS diff-amp would still be on. If the inputs went towards ground, then the opposite would happen. Using them both would ensure that when one of them turns off, the other would still remain on.



In order to further increase the Common Mode Range of the op-amp, the diff-amps were connected to a folded cascode structure. With this design, the CMR of the op-amp can extend above VDD and below ground before the op-amp begins to function improperly.

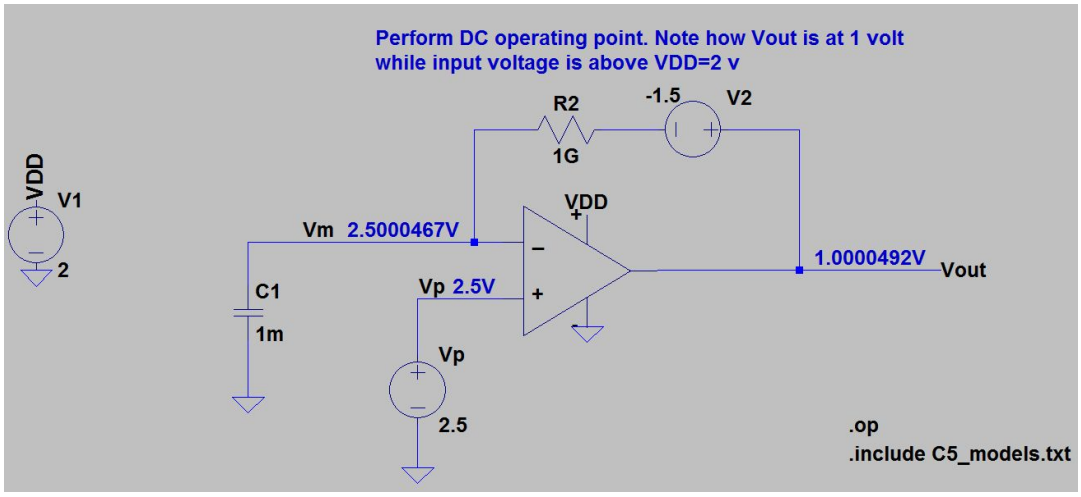


For NMOS device
Common Mode Range Max (CMRmax):

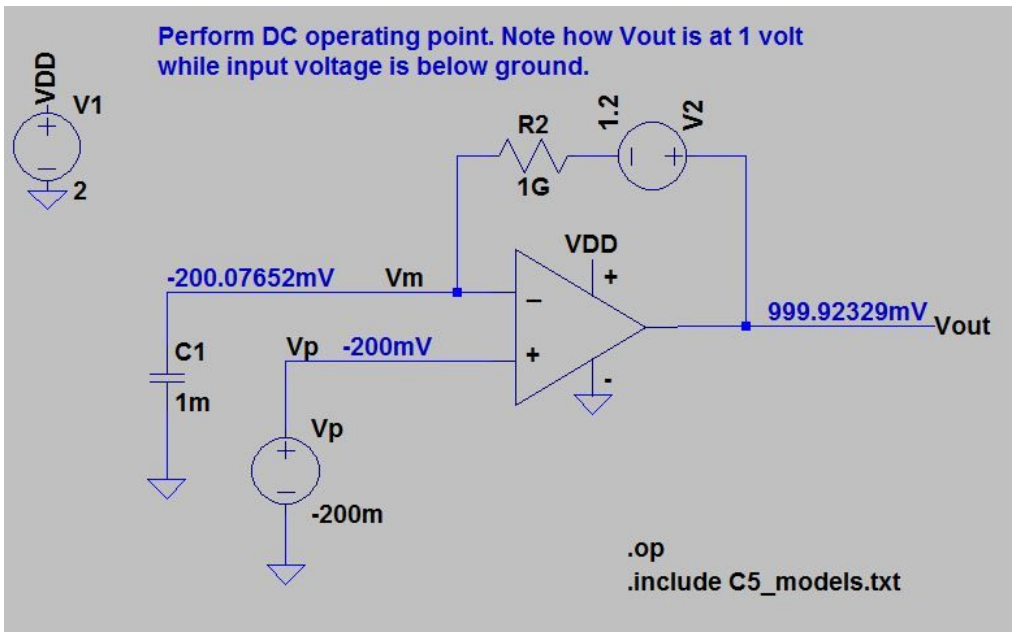
$$V_{DS} \geq V_{GS} - V_{THN}$$
$$V_D \geq V_G - V_{THN}$$
$$V_G \leq V_D + V_{THN}$$
$$V_G \leq V_{DD} - V_{SD,SAT} + V_{THN}$$
$$V_G \leq V_{DD} + 0.7\,v$$ (input can extend 700 mV above power supply)

For PMOS device
Common Mode Range Min (CMRmin)

$$V_{SD} \geq V_{SG} - V_{THP}$$
$$V_G \geq V_D - V_{THP}$$
$$V_G \geq V_{DS,SAT} - V_{THP}$$
$$V_G \geq -0.85\,v$$ (Input can extend 850 mV below ground)



** testing CMR with voltages above power supply



** testing CMR with negative input voltage

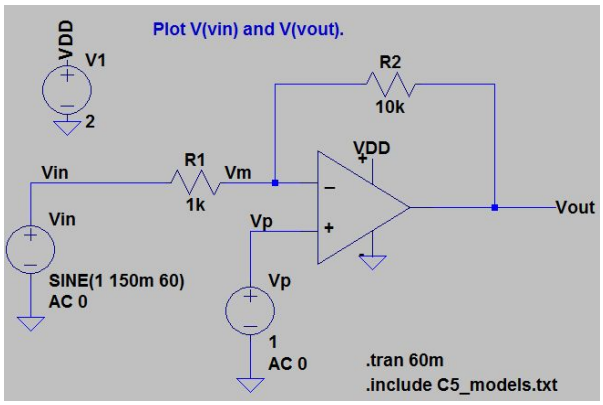
Output Stage of the Op-Amp

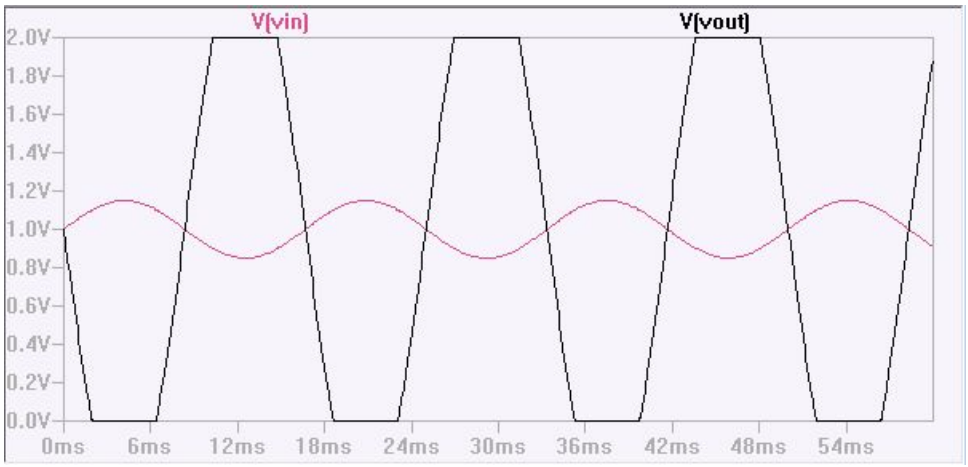
In order for the output voltage of the op-amp to have a voltage swing within 100 mV of both VDD and ground a push-pull amplifier was used as the output stage of the op-amp. The push-pull amplifier was biased using NMOS and PMOS floating current sources that were integrated into the folded cascode structure.

Since the minimum load the op-amp will drive is a 1 kohm resistor, the push pull amplifier will have to be capable of supplying enough current to ensure the gain of the op amp wont go below 80 dB. This is accomplished by increasing the widths of the output transistors. In this design, 14 transistors were connected in parallel.

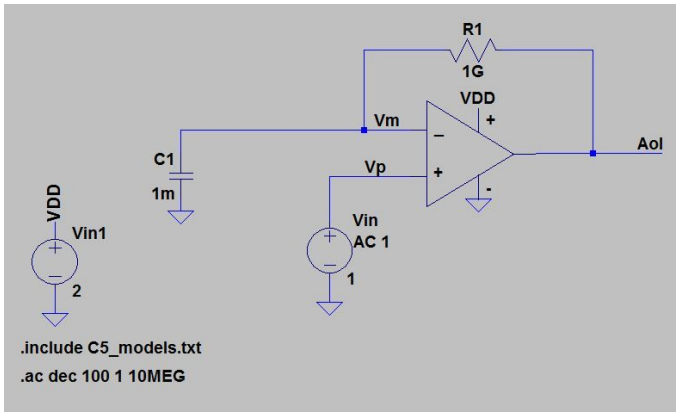
Output Swing

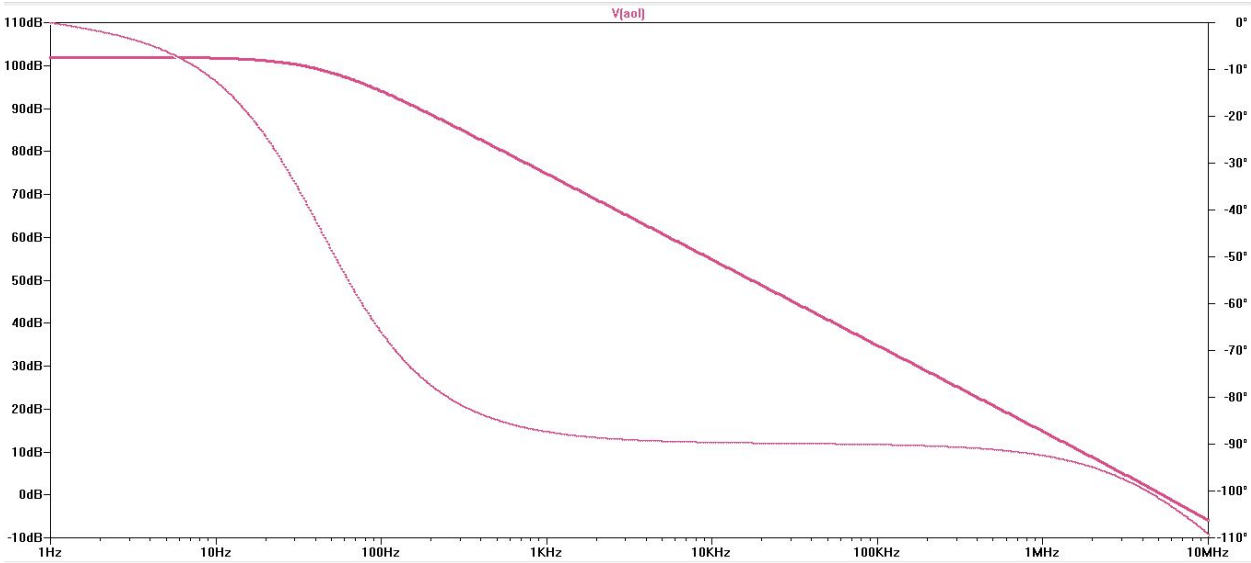
Due to the push-pull amplifier of the output stage, the output voltage of the op-amp must stay within a Vds,sat of both the power supply voltage and ground in order for it to operate within the linear region. For this design linear region of the output voltage is 50 millivolts below the power supply voltage and 50 millivolts above ground.
The simulation below shows the op-amp in an inverting op-amp configuration with an input signal large enough so that the output voltage will be clipped above VDD or below ground.
The output voltage in this simulation goes beyond the linear region and causes the output MOSFETs to enter the triode region when really close to VDD or ground.



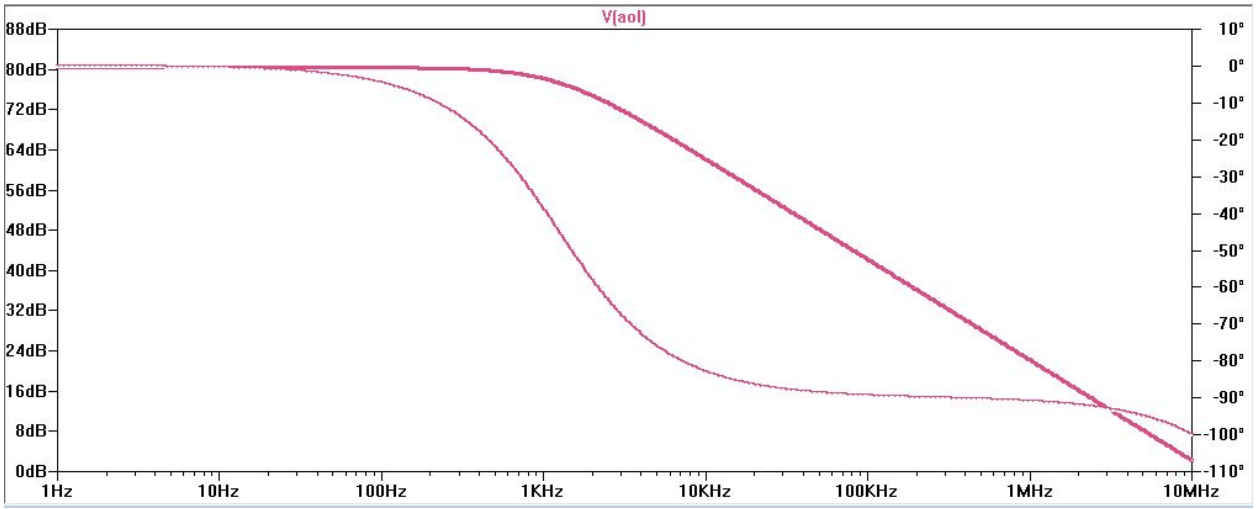


DC Open Loop gain
With no load attached to the output of the op-amp, the open loop gain is about 102 decibels, its unity gain frequency is 5 MHz and the phase at the unity gain frequency is -102 degrees.





When operating with a 5 volt power supply and a load consisting of a 1 kohm resistor and a 10 pF capacitor, the open loop gain is 80.3 decibels.



Gain bandwidth product

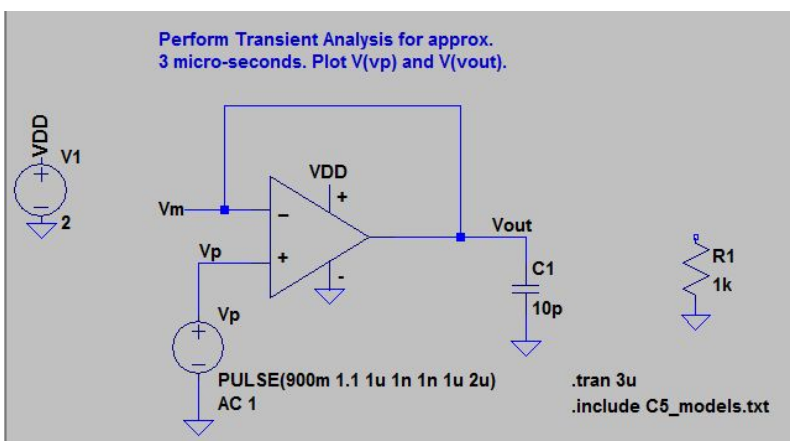
For the op amp, the gain bandwidth product is equal to the unity gain frequency. Using the pole splitting summary the unity gain frequency can be calculated using
$f_{un} = g_{m1} / 2\pi C_c$

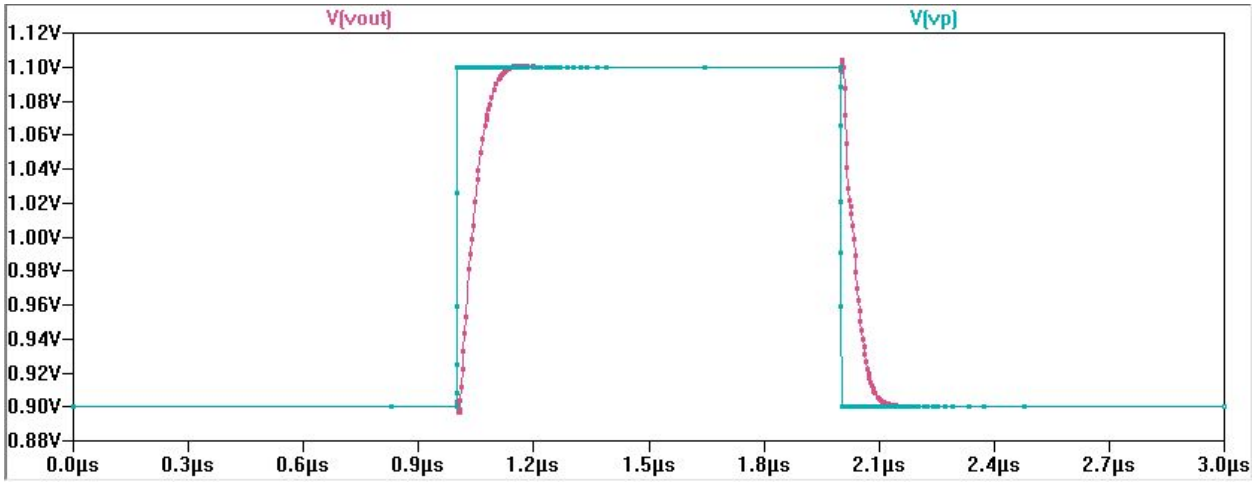
With both the PMOS and NMOS diff amps turned on the value of gm1 is equal to the sum of their transconductances.

$$g_{m1} = 214\ uA/v + 217\ uA/v \approx 430\ uA/v$$

Using this value and the values of the compensation capacitors the unity gain frequency and Gain Bandwidth Product are calculated as approximately 6.84 MHz. The simulations of the Gain Bandwidth Product are shown above.

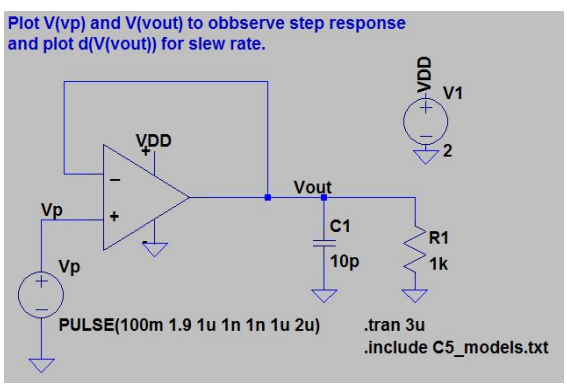
Compensation Capacitors and Step Response:
The compensation capacitors used in this design are both 5 picofarads. When simulating the open loop gain of the op-amp, the phase of the output would ideally be at -90 degrees in order for the step response of the op-amp to be a first-order response. Therefore the compensation capacitors were used to increase the phase margin of the op-amp closer to 90 degrees. In the simulation below a small step input of 200 mV is applied to the positive terminal of the op-amp. The output voltage shows a step response that has a negligible amount of overshoot.

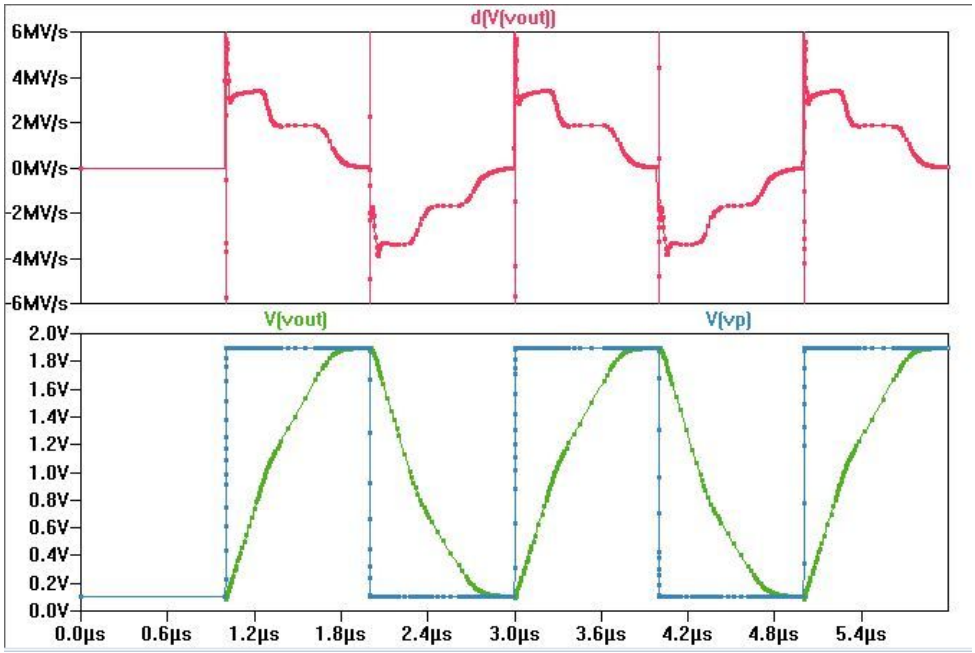




Slew Rate

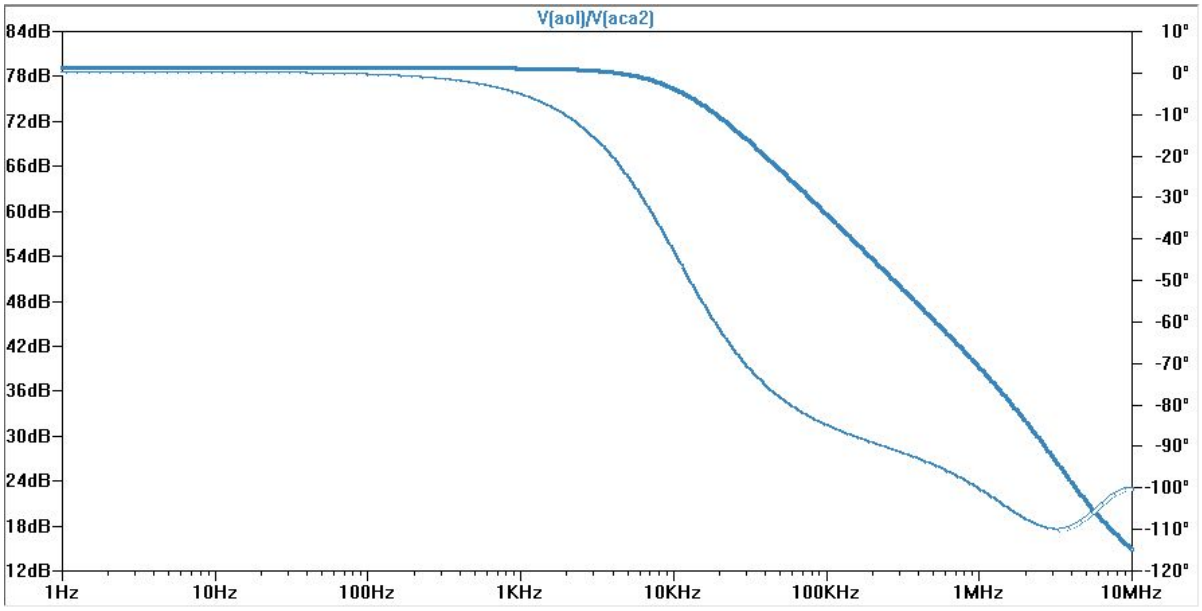
The simulation below shows the op-amp with a load of a 10 pF capacitor and a 1 kohm resistor. A step input voltage with a large change in amplitude that spans almost the entire output voltage range is used. Because of this large change in amplitude, the output voltage will be limited by the slew-rate of the op-amp. The step input goes from 100 mV to 1.9 V in 1 nanosecond. In the output, the maximum slew-rate shown is roughly 4 V/us.



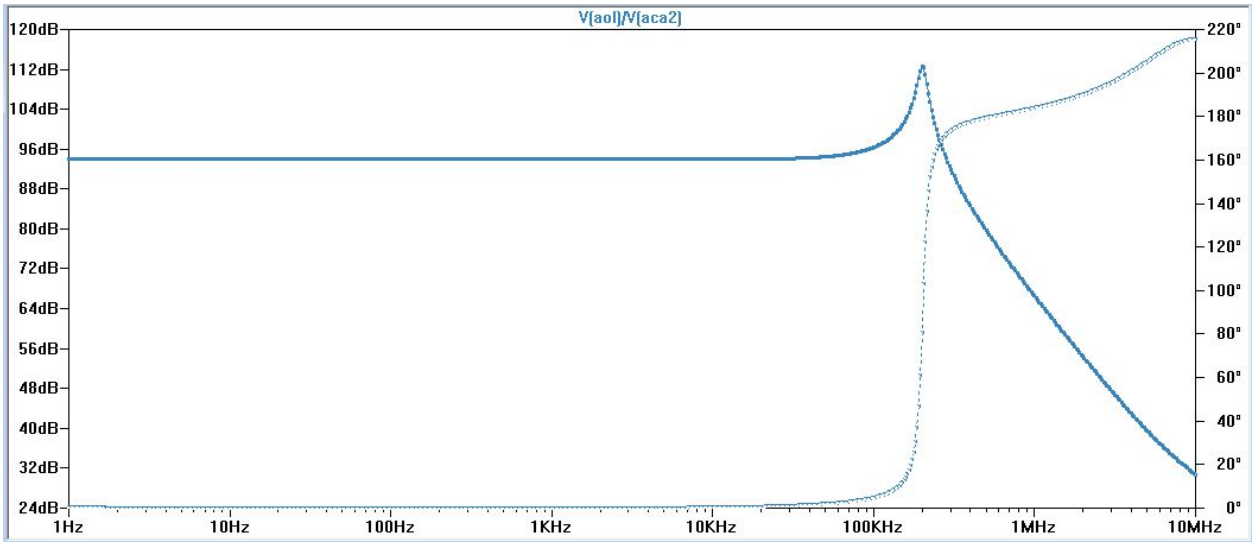


Common Mode Rejection Ratio (CMRR)

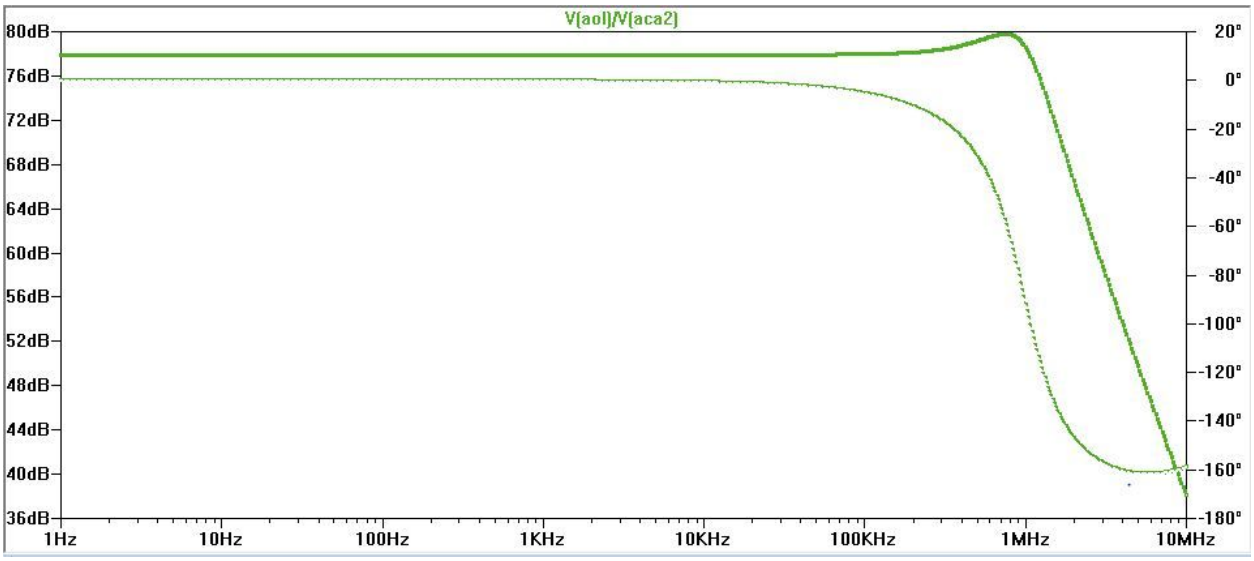
Shown below are the CMRR of the op-amp at power supply voltages of 2v, 3v, and 5v. When operating with a 2 volt power supply, the CMRR of the op-amp does not meet the required specification. The CMRR only reaches 78 dB and starts to drop at about 10 kHz frequency.
At a power supply voltage of 3 volts, the op-amp does meet the specification and has a CMRR of 94 db at 100 kHz and at 5 volts VDD the CMRR at 100 kHZ is 79 dB.



** CMRR of op-amp with 2 volt VDD



** CMRR of op-amp with 3 volt VDD

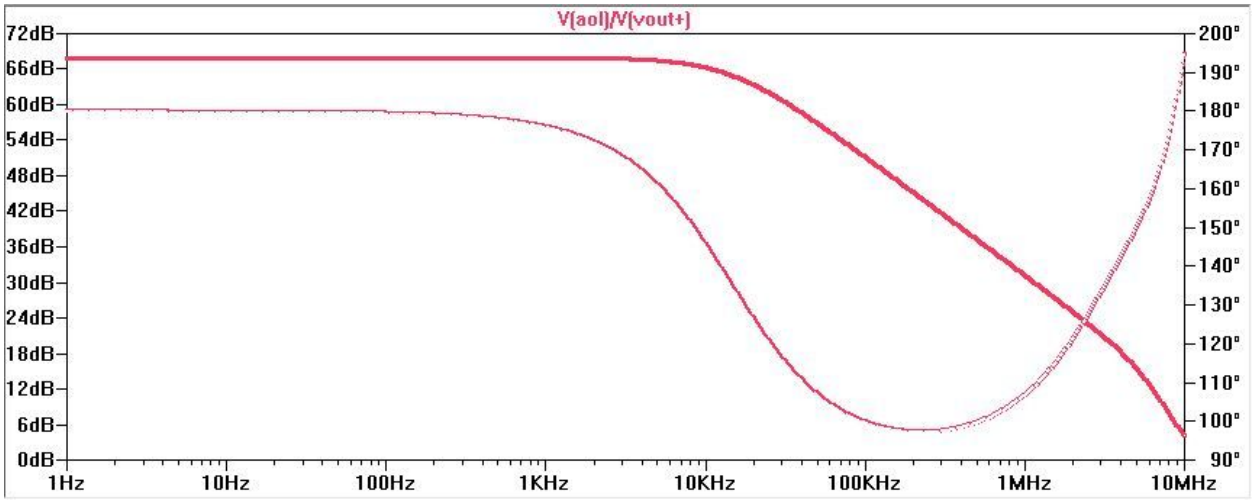


** CMRR of op-amp with 5 volt VDD

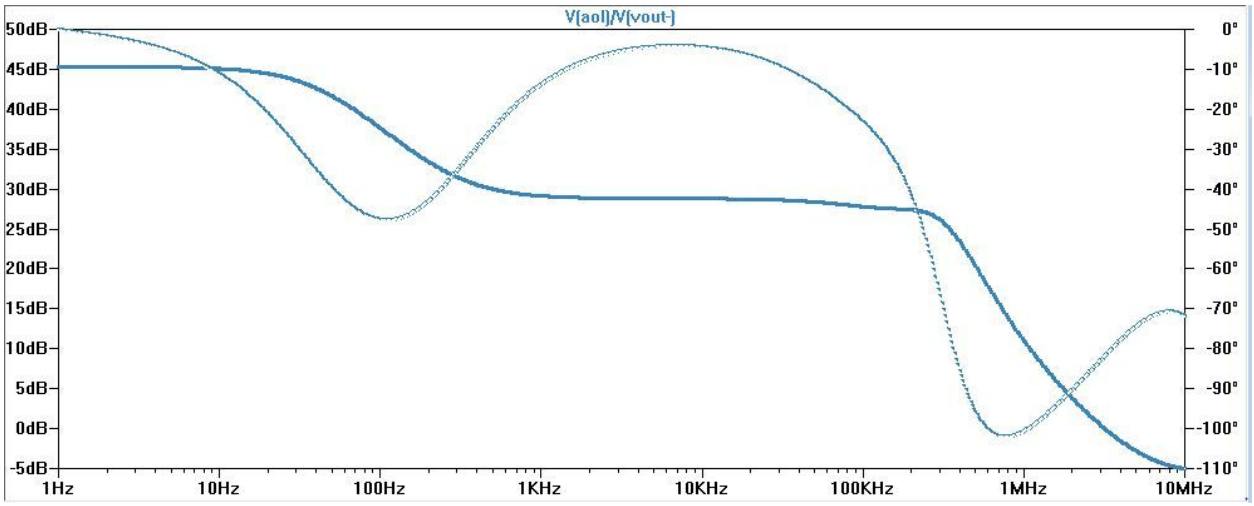
Power Supply Rejection Ratio (PSRR)

The PSRR describes how well the op-amp can reject noise in the power supply or ground busses. The designed op-amp does not perform as well as the specifications required. The positive PSRR only went up to 68 dB and it started decreasing at frequencies over 10 kHz. At 100 kHz the PSRR+ is 51 dB.

The negative PSRR at 100 kHz is 28 dB.



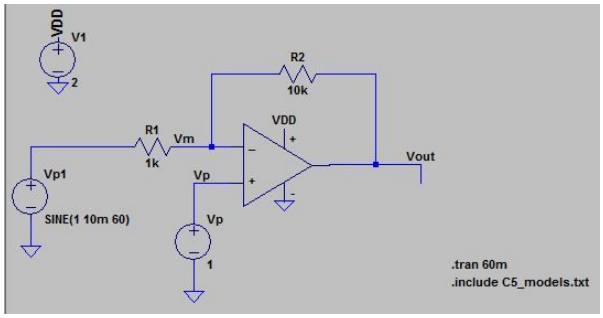
** PSRR+

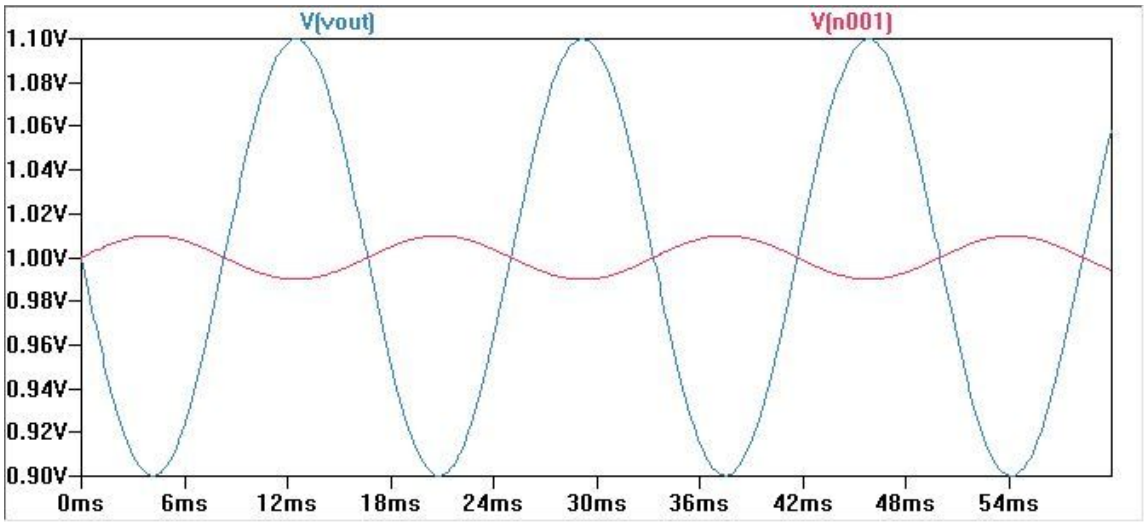


** PSRR-

Inverting Op-Amp Configuration

In the simulation below the op-amp is placed in an inverting op-amp configuration with a gain of -10. Both inputs are biased at 1 volt or VDD/2 and the input signal is 10 mV in amplitude. The output shown below is a sine wave with a DC bias at 1 volt with an amplitude of 100 mV.





Power Consumption

To calculate the power consumption of the op-amp, the total amount of current running through the circuit is multiplied by the power supply voltage. In the entire circuit there are a total of 30 branches of current that carry approximately 10 uA of current. If the op-amp runs with a 2 volt power supply, this yields a power dissipation of about 600 microwatts. Since the biasing circuit has a current of 10 uA for power supply voltage values between 2 and 3.2 volts, the power is estimated by P= VDD*(300 uA).