BiCMOS Op-Amp Design

Using AMS 0.35µm SiGe-BiCMOS process (S35)
Baker Research (Summer 2017)
Practice design
By: Gonzalo Arteaga

Summary of Results:

Parameter	Test conditions	Value	Unit
Supply voltage		3.2 - 5	V
DC open-loop gain	100 fF load; Vdd = 5 V;	90	dB
	1 kΩ load; Vdd = 5 V;	84.4	dB
Gain-Bandwidth Product	100 fF load; Vdd = 5 V;	204.2	MHz
	1 kΩ load; Vdd = 5 V;	13	MHz
Gain Margin	100 fF load; Vdd = 5 V;	-16.37	dB
Phase Margin	100 fF load; Vdd = 5 V;	92.1	deg
Input offset voltage	Vcm = 2.5 V	-1.3	mV
CMRR	Freq. = 100 kHz	110	dB
PSRR+	Freq. = 100 kHz	65	dB
PSRR-	Freq. = 100 kHz	100 - 113	dB
Slew rate	Vdd = 5; C(load) = 10 pF; Unity gain	82.17	V/µs
Common mode input range		1.61 to Vdd - 0.55	V
Output swing		660 to Vdd - 300	mV
Supply current	2 V < Vdd < 5 V	1.92	mA
Power consumption	Vdd = 3.2 V;	6.144	mW
	Vdd = 5 V;	9.60	mW

Device parameters			
MOSFET Parameters for biasing circuit VDD = 5 V scale factor = 350 nm ** widths of the devices of the op-amp are twice as wide as the devices in the biasing circuit.			
Parameter	**NMOS**	**PMOS**	**Comments**
Bias Current Id	120 uA	120 uA	
W/L	20 / 2	91 / 2	
Actual W/L	7 u / 0.7 u	32 u / 0.7 u	
Vds,sat Vsd,sat (overdrive voltage)	500 mV	500 mV	10% of VDD
Vgs Vsg	1.00 V	1.20 V	
Vthn Vthp	500 mV	700 mV	
HBT Parameters			
Model	npn132h5		
Device area	1.6		

Biasing Circuit

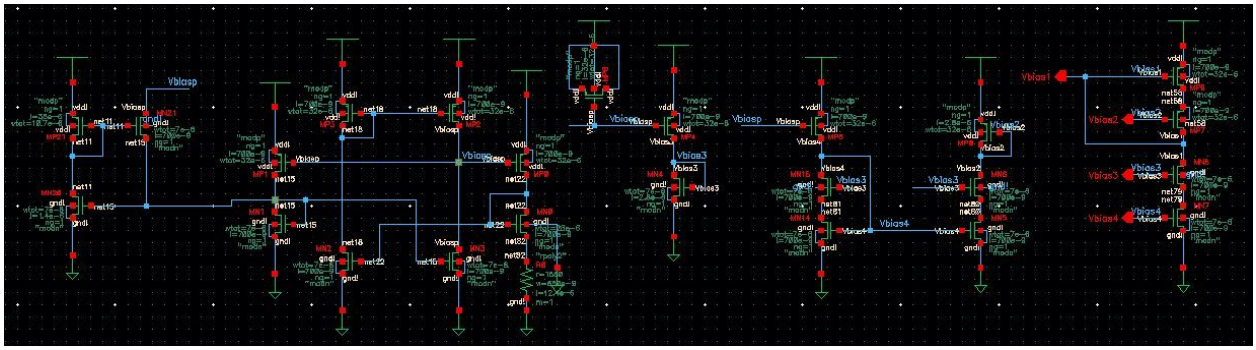

Figure 1: complete schematic of the biasing circuit.

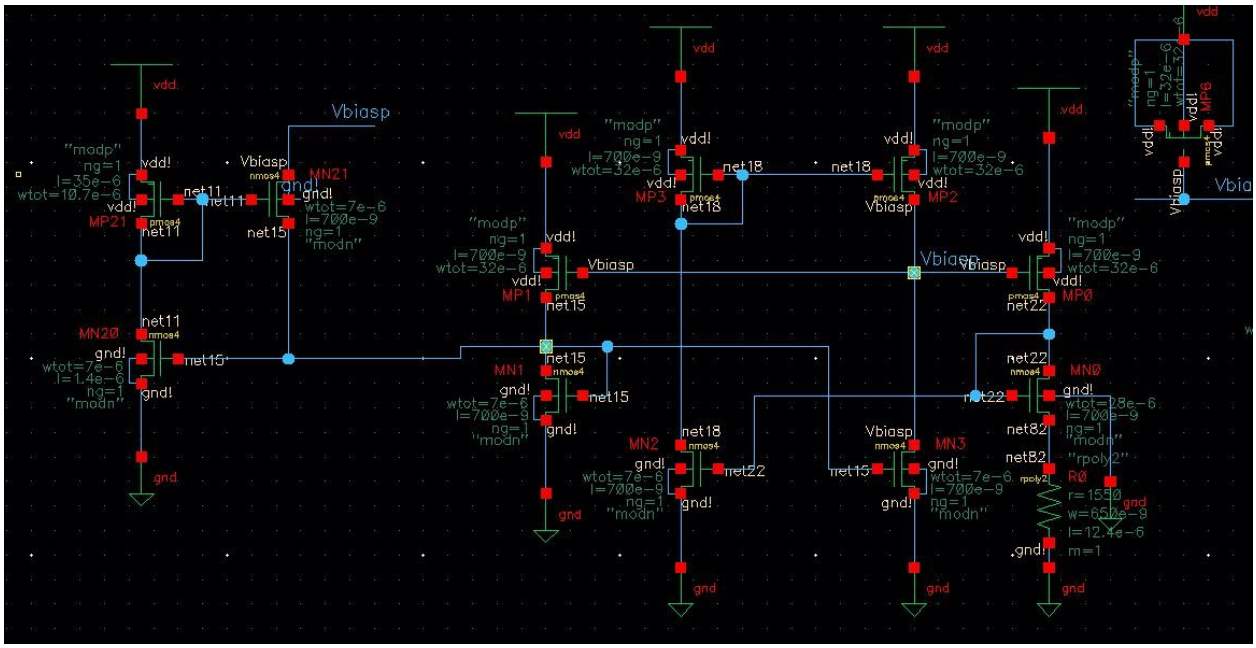

Figure 2: Close-up view of the start up circuit and beta-multiplier.

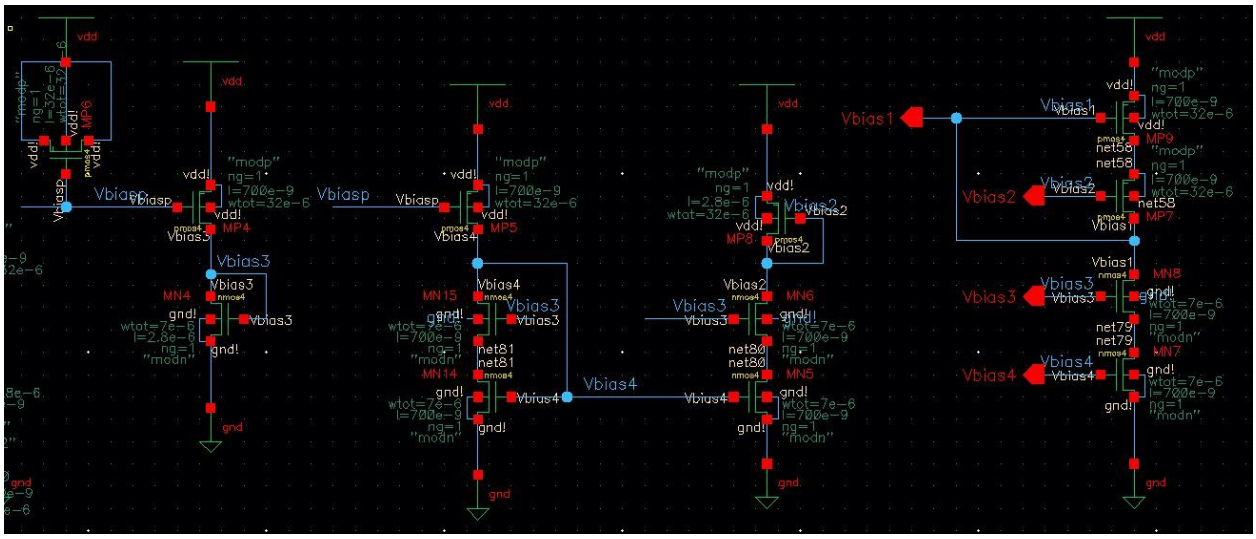

Figure 3: Close-up view of circuitry used to generate biasing voltages.

Biasing circuit layout

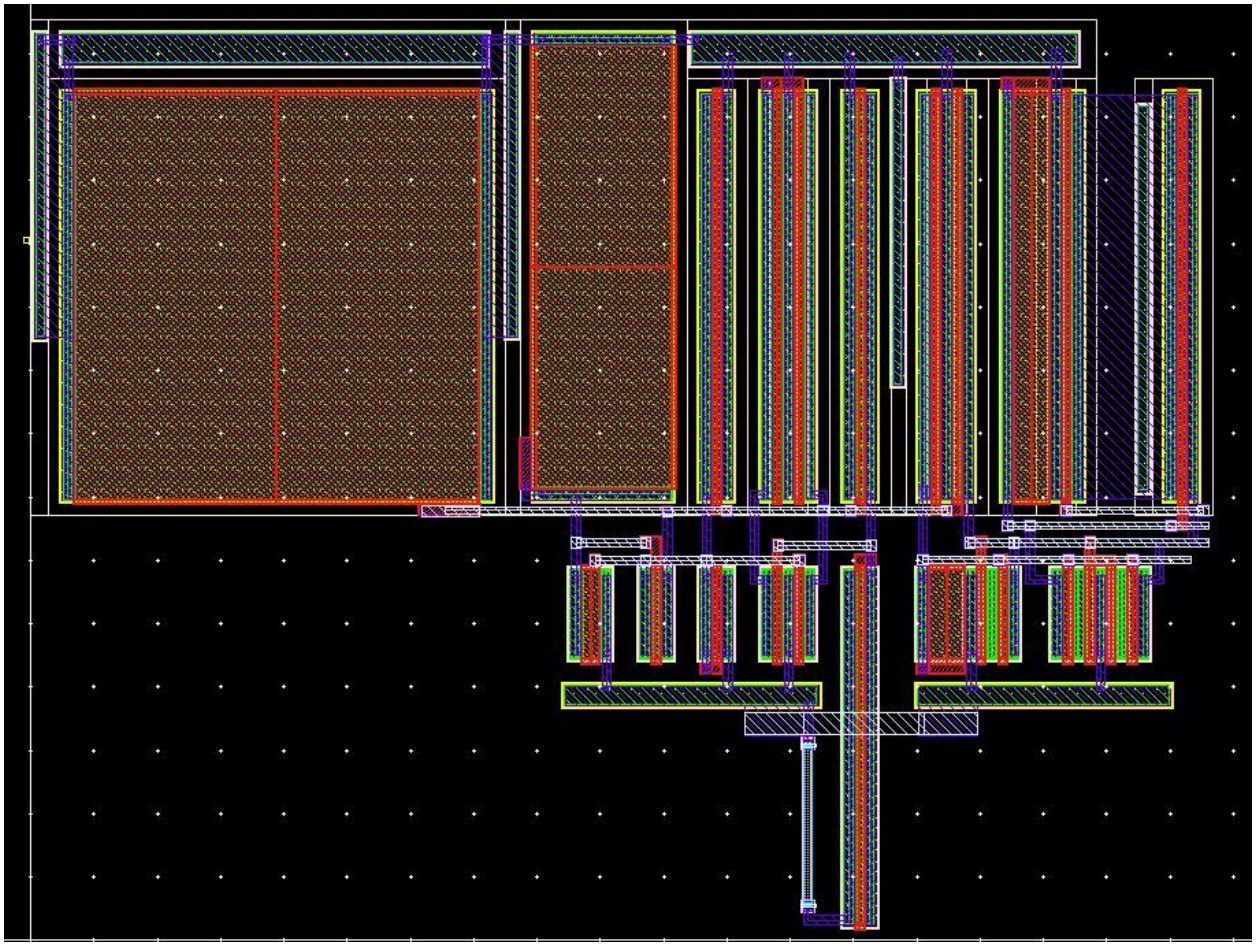

Figure 4: Layout view of the biasing circuit.

Biasing Circuit simulations

Bias voltages vs VDD

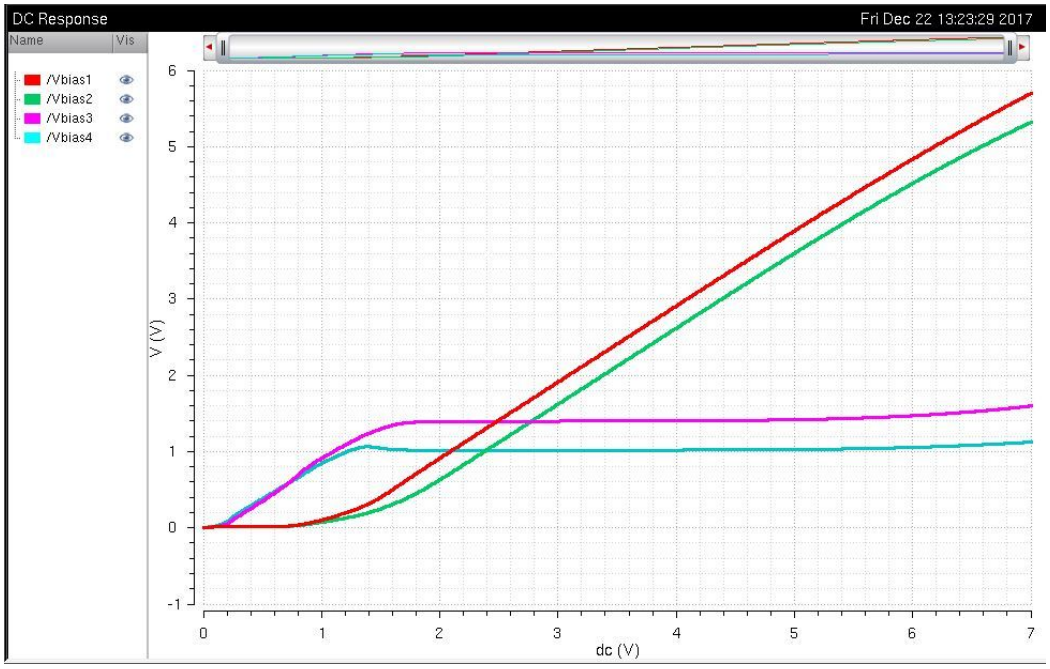

Figure 5: Simulation results of the biasing voltages when sweeping the power supply voltage from 0 to 7 volts. As shown, Vbias3&4 maintain a constant bias voltage between 2 and 5 V while Vbias1&2 maintain a bias voltage below the Vdd voltage.

Bias Current vs VDD

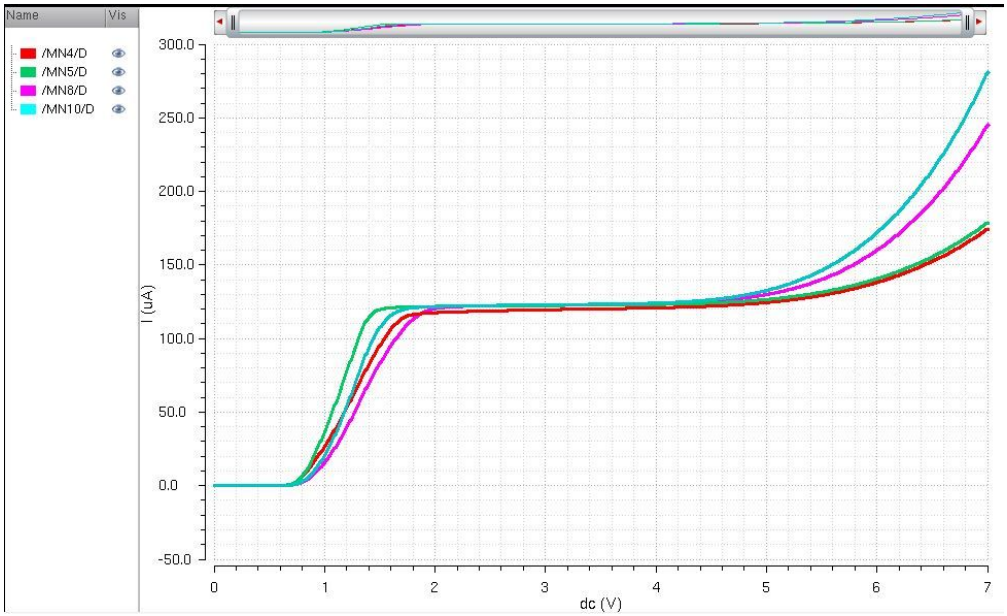

Figure 6: Simulation results of the bias current when sweeping the power supply voltage from 0 to 7 volts.

Op-amp

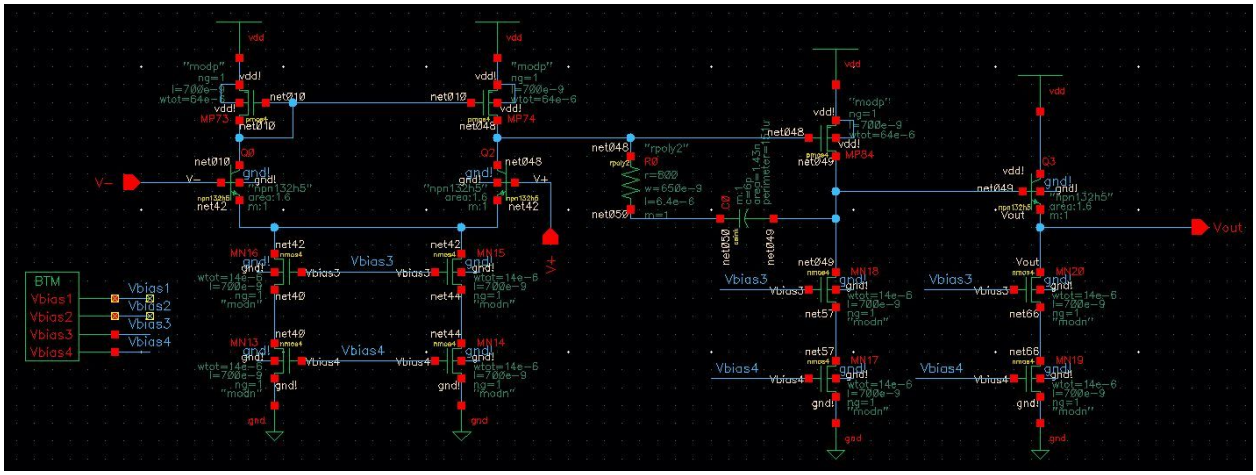

Figure 7: Complete circuit of the op-amp including (from left to right) the differential input stage, second voltage gain stage, and an output buffer. The compensation capacitor value is 6 pF and the series resistor has a value of 800 ohms.

Op-amp layout:

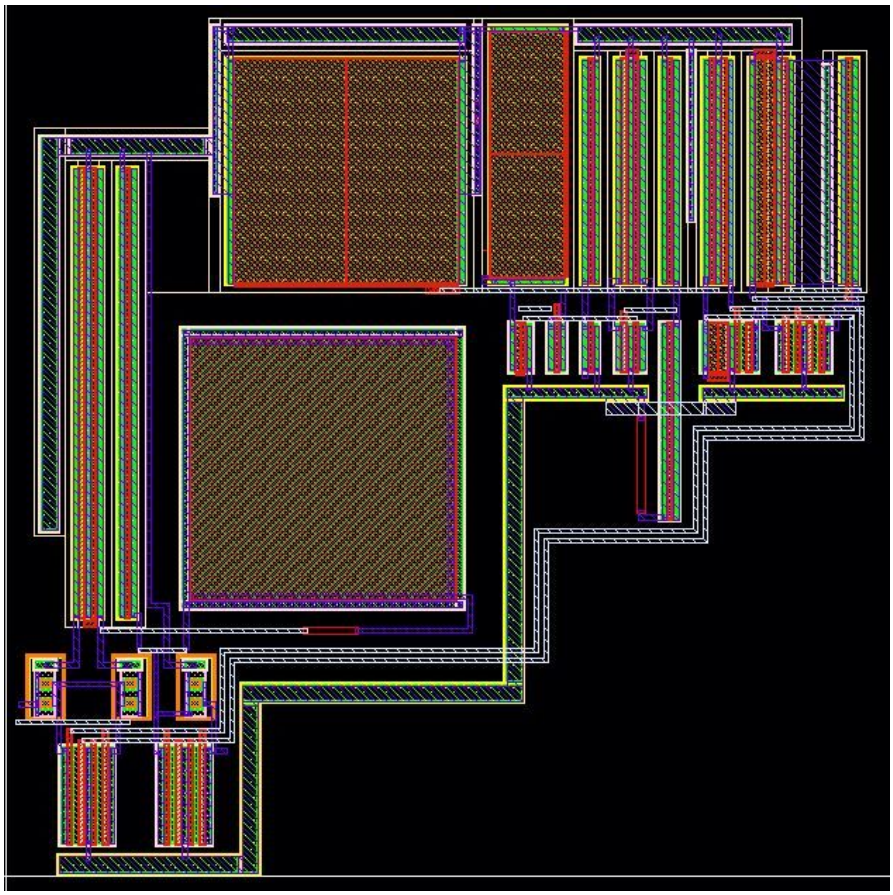

Figure 8: Layout of the op-amp and biasing circuit.

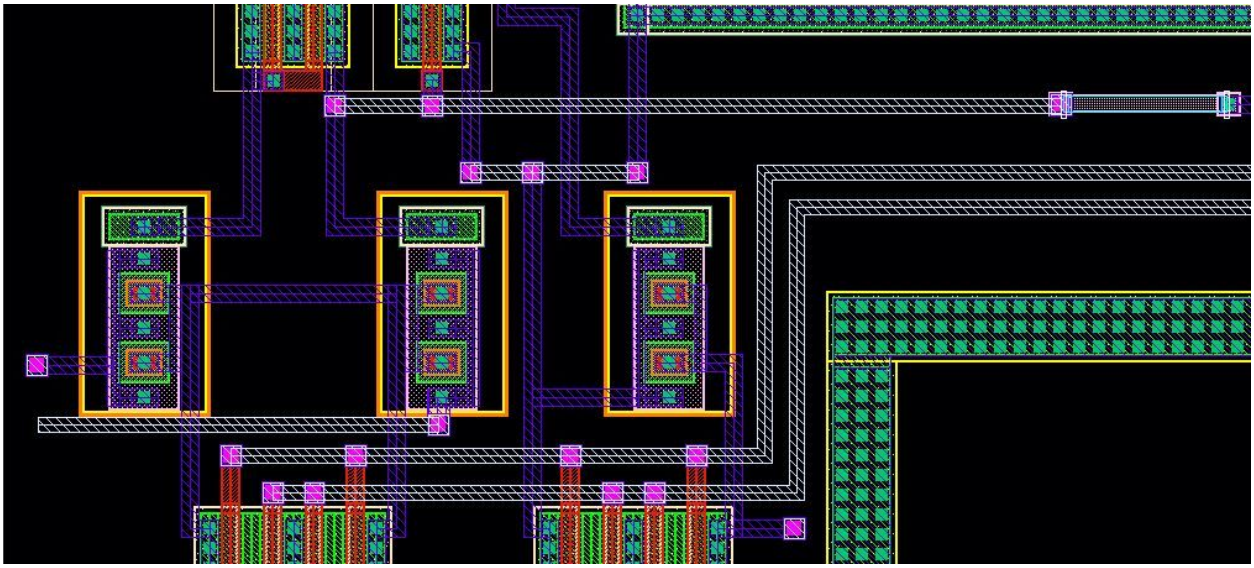

Figure 9: Close-up view of op-amp layout. Here the the Heterojunction Bipolar Transistors (HBT) are shown more clearly.

Op-amp simulations

Open-Loop gain

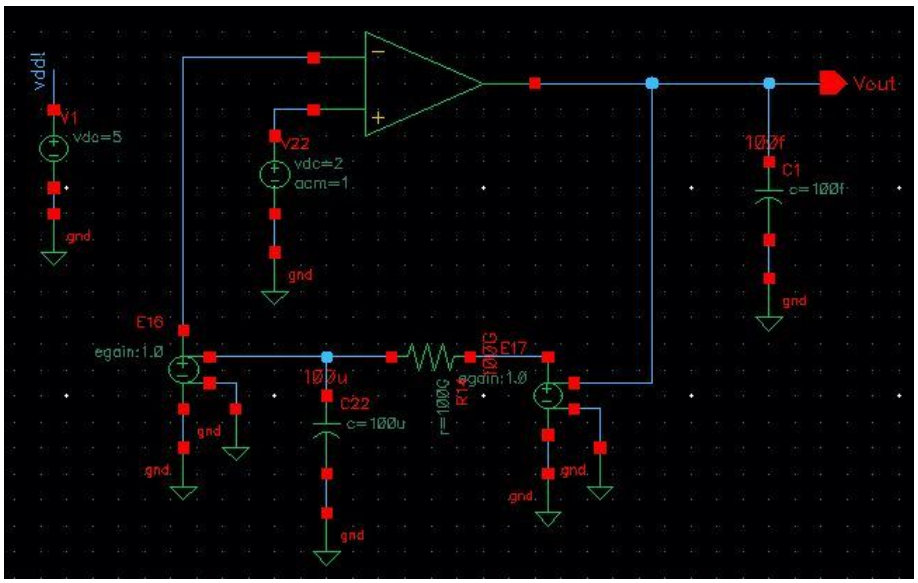

Figure 10: Schematic used to characterize the open loop gain of the op-amp. Since the input differential pair consists of bipolar transistors (smaller input impedance compared to MOSFETs), voltage-controlled voltage sources where used in the feedback loop to isolate the feedback.

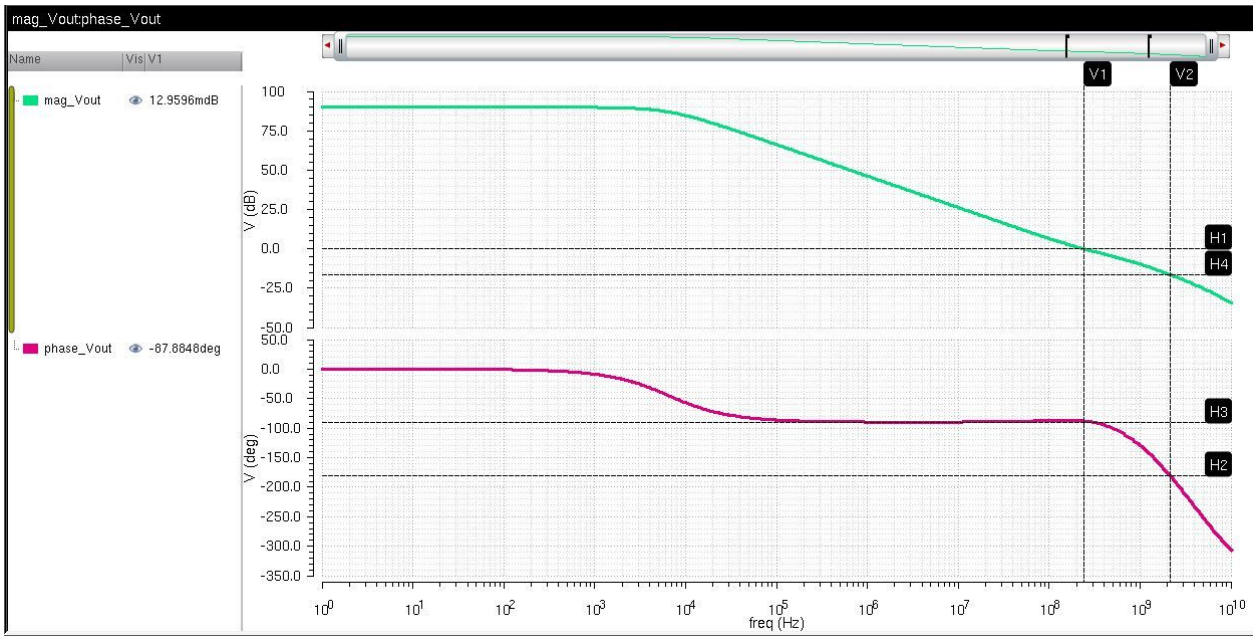

Figure 11: Simulation results of the open-loop gain.

Figure 12: Additional simulation results of the open-loop gain.

Step Response

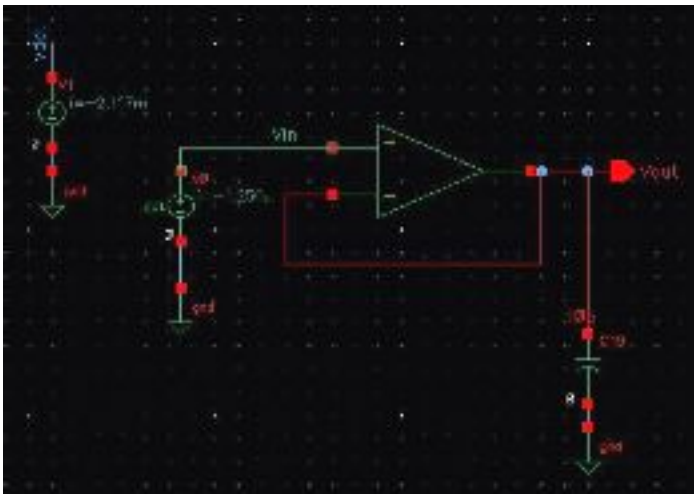

Figure 13: Schematic used to simulate the step response of the op-amp when driving a 10 pF load. The op-amp is placed in a unity gain configuration.

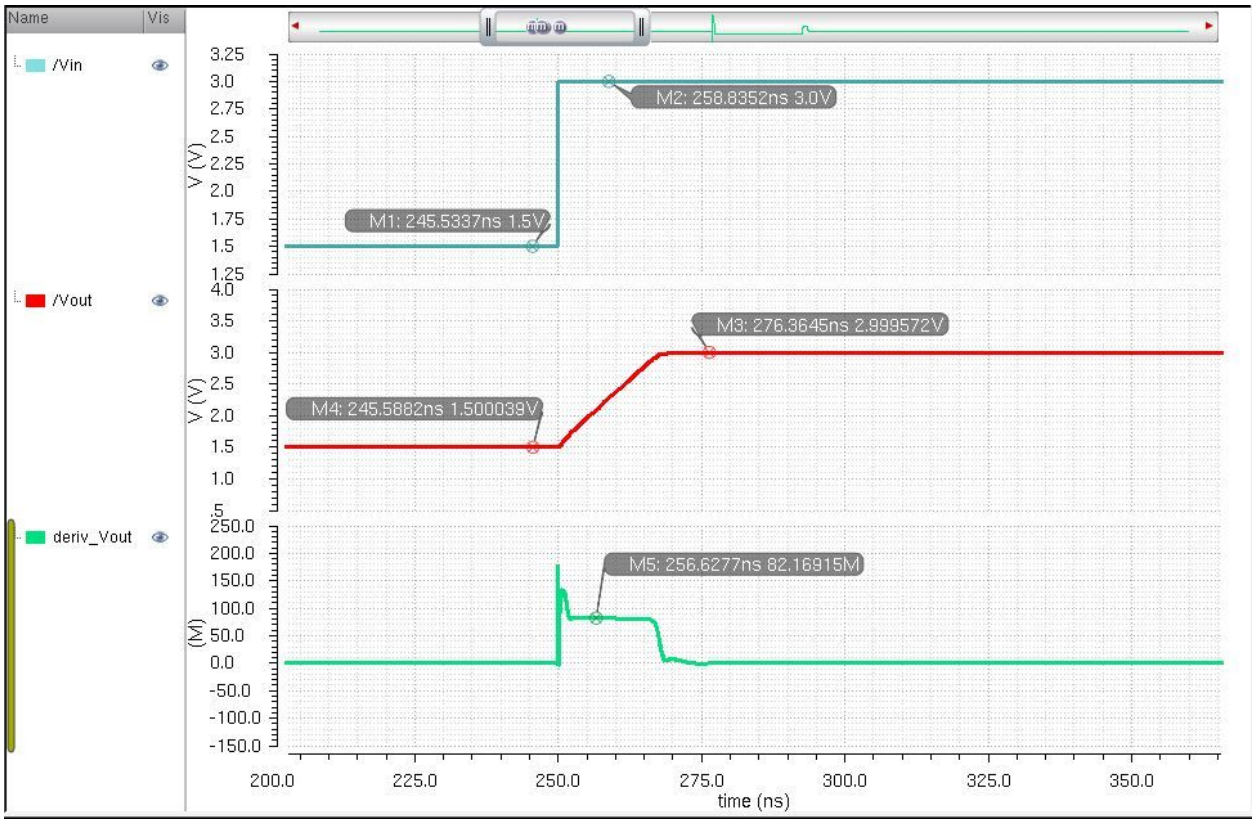

Figure 14: Close up view of rising edge of the output step response as well as the derivative of the output step response.

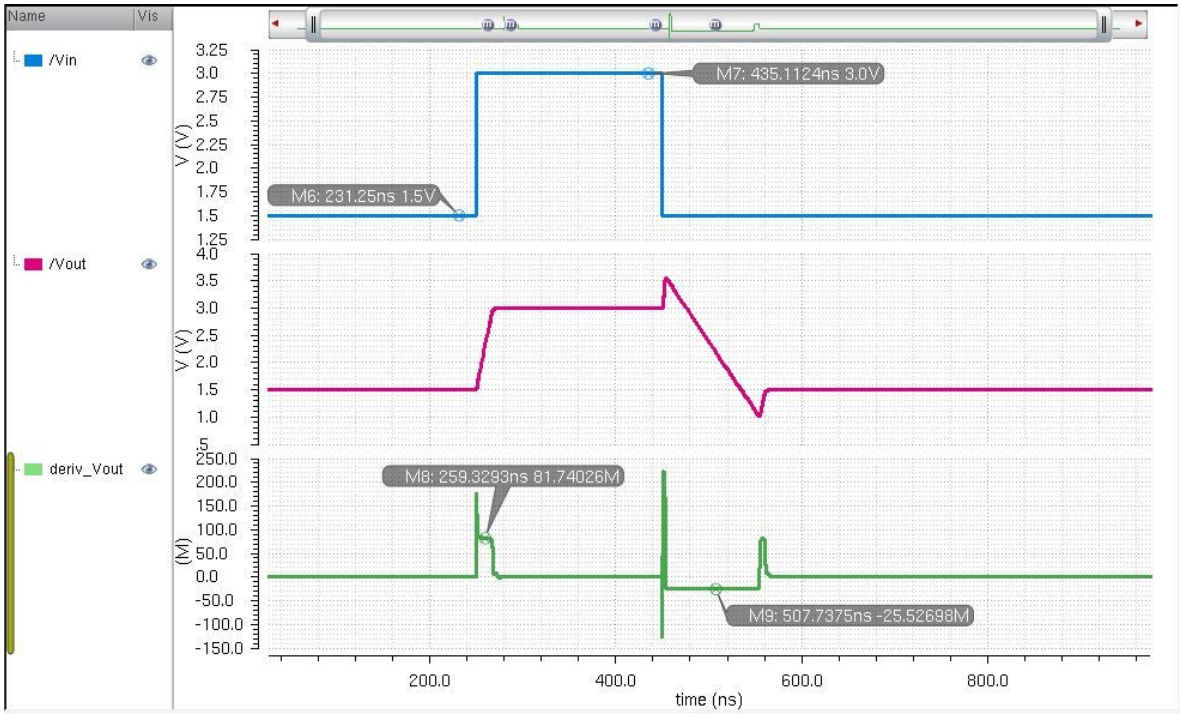

Figure 15: Another view of the step response of the op-amp.

Inverting and Non-inverting configurations

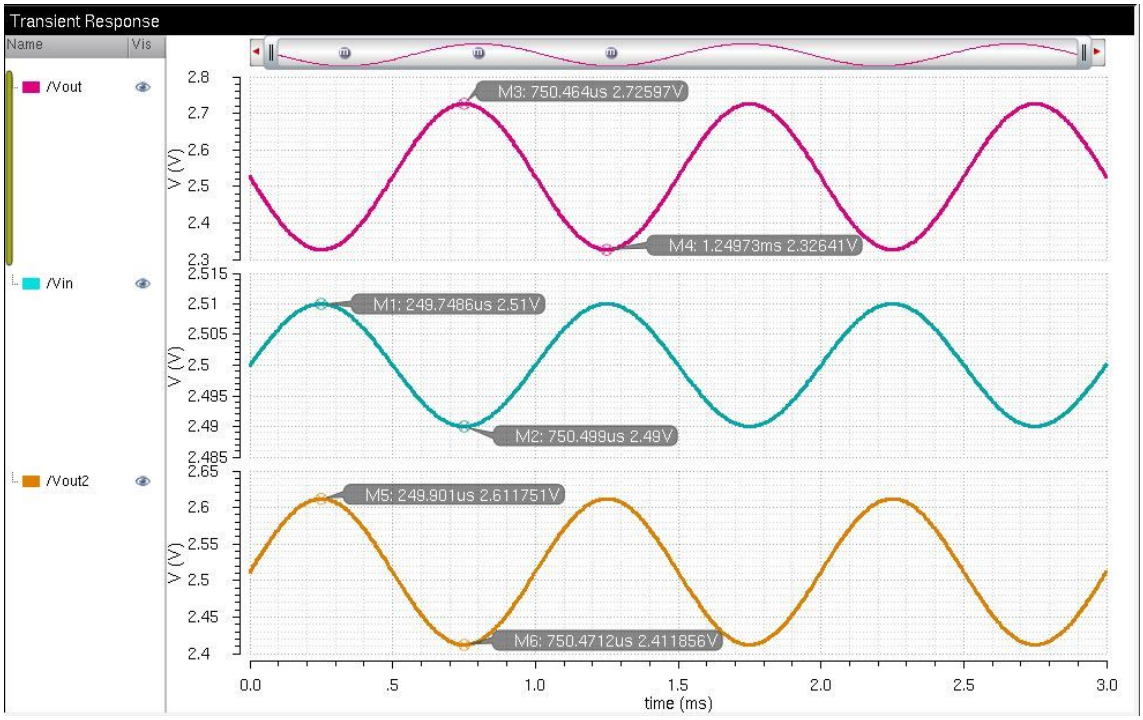

Figure 16: Shown above are the simulation results of two op-amp configurations. From top to bottom is the inverting output (purple trace) which had a gain of -20, input sine wave with 10 mV amplitude (blue trace), Non-inverting output (yellow trace) which had a gain of 10.

PSRR

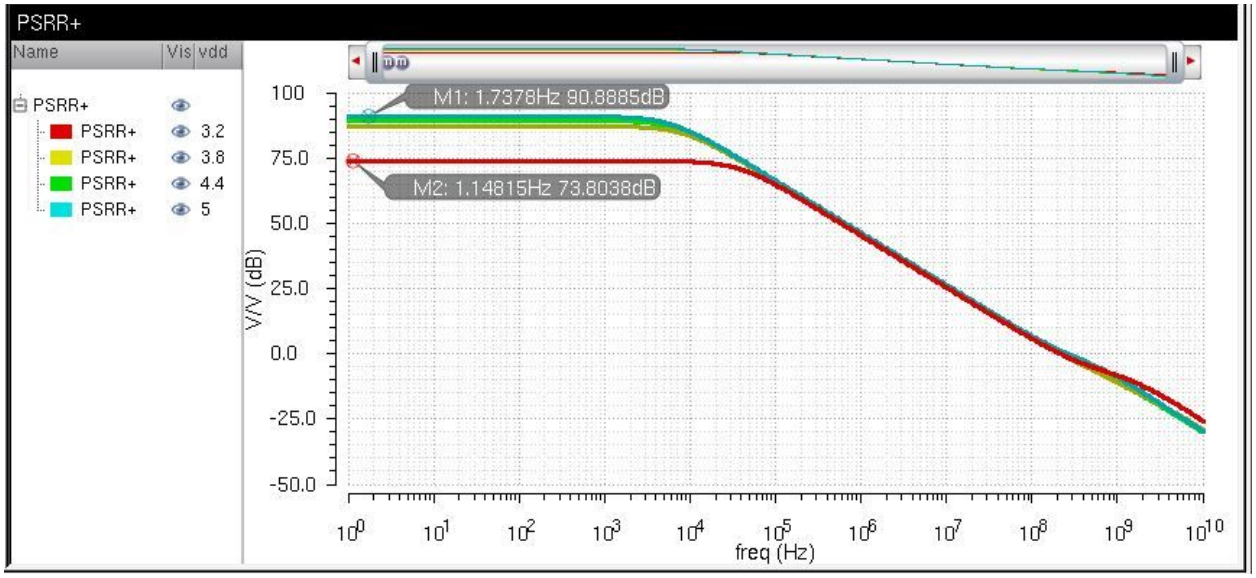

Figure 17: Simulation of the positive power supply rejection ratio with varying power supply voltages.

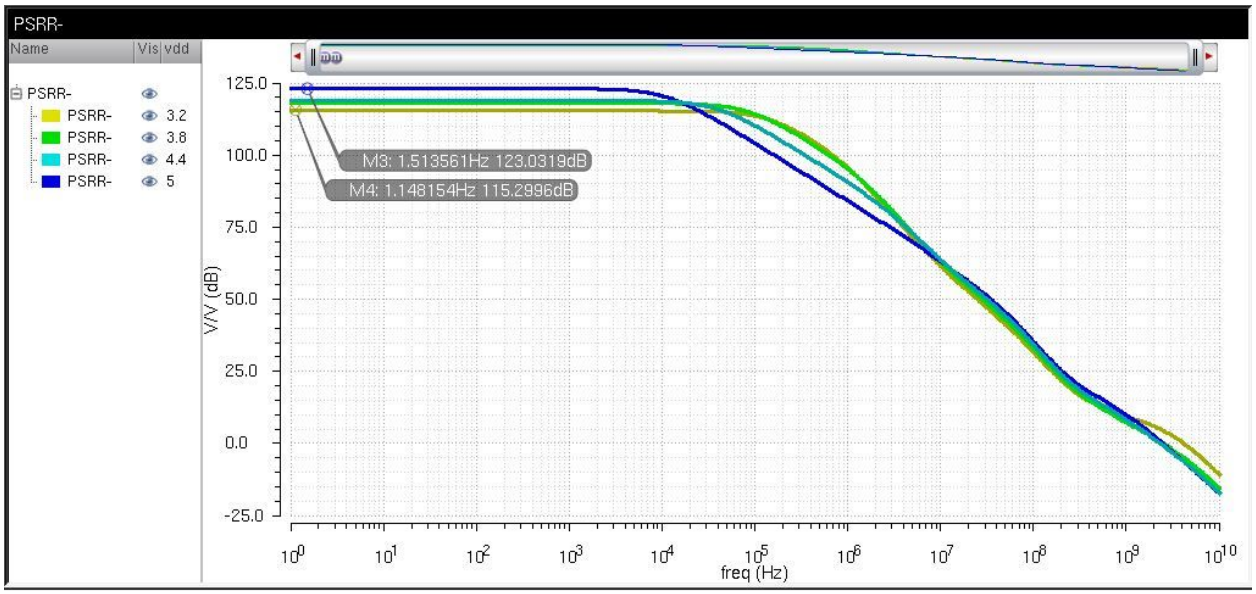

Figure 18: Simulation of the negative power supply rejection ratio with varying power supply voltages

CMRR

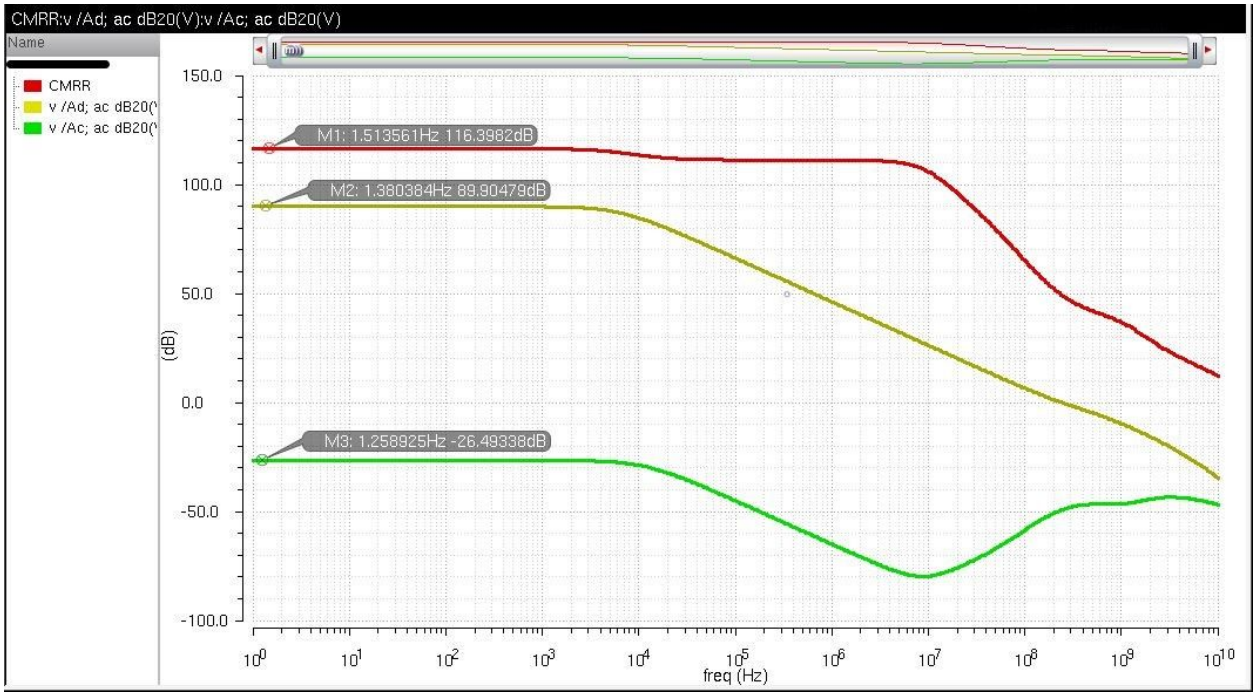

Figure 19: Shown above as the red trace is the common-mode rejection ratio, the differential open-loop gain in yellow, and the common-mode gain in green.

Conclusions

This practice design helped me understand more about the process of designing and compensating an op-amp for stability. It also helped with learning about the process within the Cadence tools. As far as the design goes, the op-amp suffers from a positive pulse and later an under shoot when a large step input is driven low. This is due to using direct compensation in the design. The layout also has room for improvement. Since the MOSFET devices has large widths, instead of placing the large device by itself a better option would have been to use multiple devices in parallel. This is especially the case for the wide NMOS in the beta-multiplier circuit.