Test Chip - PDC1+KD1S

Using AMS 0.35-µm SiGe-BiCMOS process (S35)
Baker Research (Summer 2018)
By: Gonzalo Arteaga

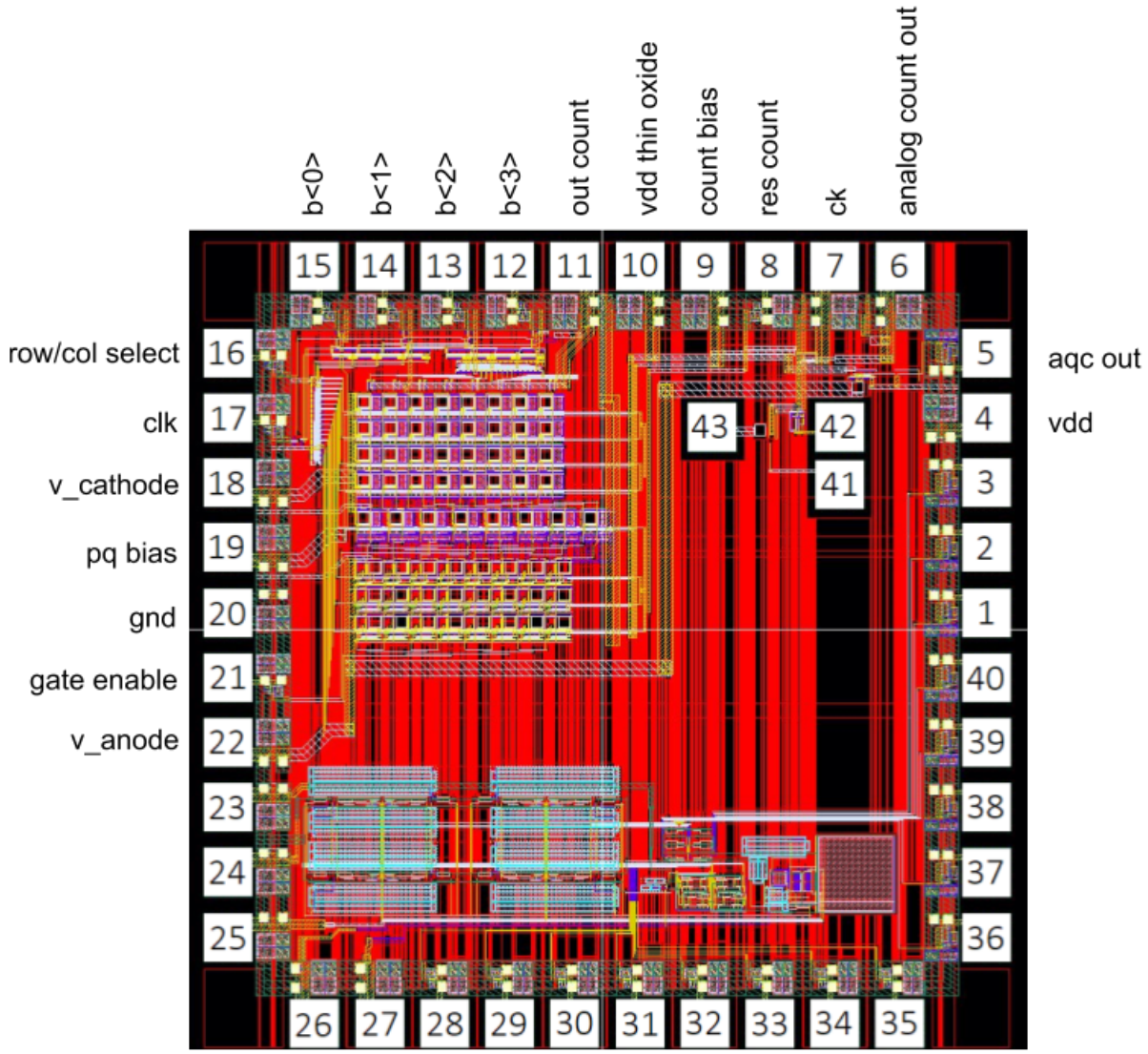
The following describes some of the contents of a test chip submitted in August 2018. Half of the chip was delegated to the design of a KD1S modulator ADC while the other half was delegated to a set of photon-counting circuits utilized with a geiger-mode avalanche photo-diode (APD). The contents of this latter half are documented below and includes circuits such as passive and active quenching circuits, monostable pulse generators, and analog counters. These circuits were used in conjunction with a 25-µm x 25-µm APD to construct four different pixel designs which were organized in an 8 x 8 grid. The circuits were implemented using a 0.35-µm SiGe BiCMOS process provided by AMS.

Parameter	Value	Unit	Additional information
Cox’	4.544	fF/µm^2	
tox	7.6	nm	From S35 process parameters
ε_r	3.9	—	For SiO2

Table 1: Table of parameters.

Pin Configuration

A layout image of the chip is shown in Figure 1 with labelled pads. The upper half of the chip contains the circuits relevant to this document while the lower half contains a KD1S modulator. The layout view shown below also contains dummy fill which is responsible for the red lines seen in the image.



inner bonding pads_
41: indv. pq bias
42: indv. pq out
43: indv. v_cathode

Figure 1: Image of chip with pads numbered and labelled. Only pins relevant to this report are labelled.

Pin Functions

Pin	Name	I/O	Brief description
4	vdd	---	+5 volts. supply voltage for digital logic.
5	aqc out	O (D)	output of individual active quenching circuit + APD
6	analog count out	O (A)	output voltage from an analog counter
7	ck	I (A)	negative clock pulse input to an analog counter
8	res count	I (D)	reset to the analog counter. active high.
9	count bias	I (A)	determines the step size (ΔV) of the analog counter.
10	vdd thin oxide	---	+3.3 volts. supply voltage for smaller devices.
11	out count	O (A)	output count from SPAD array.
12	b<3>	I (D)	bit 3 of 4x16 decoder
13	b<2>	I (D)	bit 2 of 4x16 decoder
14	b<1>	I (D)	bit 1 of 4x16 decoder
15	b<0>	I (D)	bit 0 of 4x16 decoder (LSB)
16	row/col select	I (D)	selects between writing to row/col flip flops
17	clk	I (D)	clock for row/col flip flops
18	v_cathode	I (A)	cathode voltage for the APDs in the passive quenching circuits.
19	pq bias	I (A)	gate of pull-down device in the passive quenching circuit array.
20	gnd	---	ground reference
21	gate enable	I (D)	enables quenching circuits. acts as a global shutter control.
22	v_anode	I (A)	anode voltage for the APDs in the active quenching circuits.
41	indv. pq bias	I (A)	gate of pull-down device in the individual passive quenching circuit.
42	indv. pq out	O (D)	output of the individual PQC + APD circuit.
43	indv. v_cathode	I (A)	cathode of APD in the individual PQC + APD circuit.
**D = digital, A = analog, PQC = passive quenching circuit			

Table 2: Description and list of pins.

Description of circuits

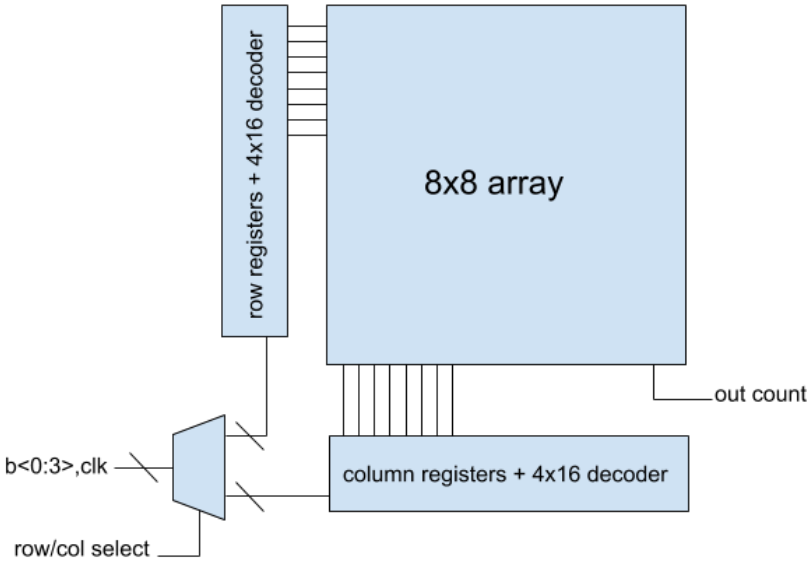


Figure 2: Basic block diagram of the array circuitry.

There are four designs of photon detection circuits within the 8x8 pixel array. The array size was settled on 8x8 despite having 4x16 decoders. Because of this, only rows 8-15 and columns 0-7 are needed to access every pixel within the array. Rows 12-15 consist of pixel design 1, row 11 consists of pixel design 2, row 10 consists of pixel design 3, and rows 8-9 consist of pixel design 4. These designs are elaborated on in the subsequent sections.

Net name	Pin(s)	I/O	Detailed function
row/col select	16	I (D)	Set to **0** for access to the row registers. Set to **1** for the column registers.
b<0:3>	15:12	I (D)	Input data pins for selecting a specific row/column. The registers will store the value of these bits on a rising edge on the ‘clk’ signal.
clk	17	I (D)	Clock signal for the row/column registers. This pin has an on-chip pull-down device to maintain a defined logic state at all times.
out count	11	O (A)	Output of the selected element within the array. If no element is selected this output will stay at zero volts.

Table 3: Detailed list of pins from Figure 2.

Design 1: PQC+Analog counter 1

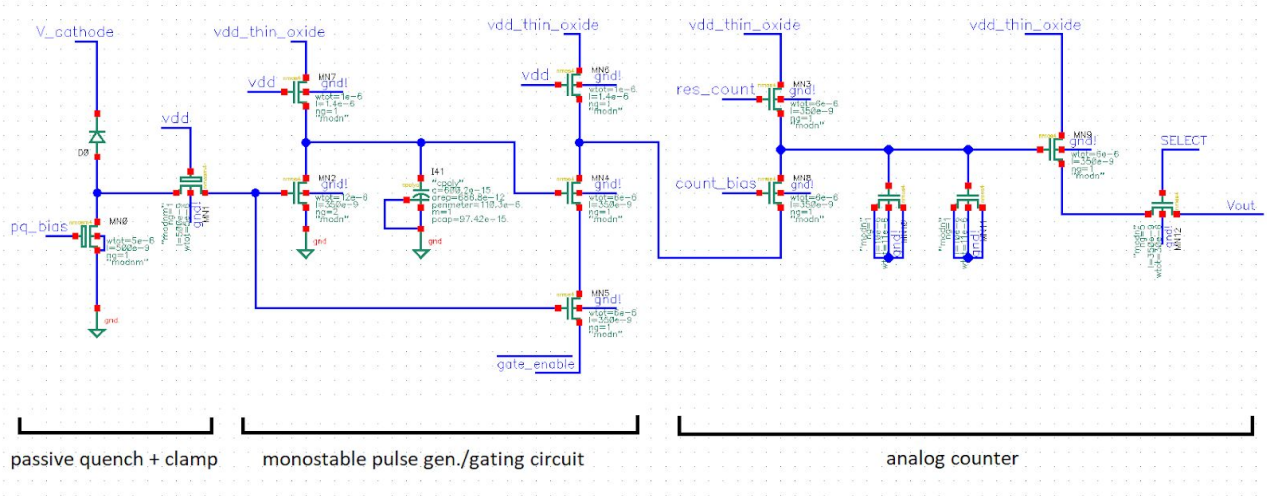


Figure 3: Schematic view of passive quenching pixel with analog counter that uses MOSCAPs.

The first design features a passive quenching circuit (PQC) with an NMOS load. The pulses coming from this circuit are clamped by an NMOS pass gate to allow operation with the following circuit section. After the pass gate, a monostable gating circuit generates a short negative pulse for each photon detected by the APD. These short pulses are then used by the analog counter to decrement the voltage across a capacitor which, after going through a source-follower, will indicate the number of breakdowns that the APD goes through within a certain window of time. Each circuit avoids the use of PMOS devices to avoid the use of N-wells and having a larger layout footprint.

This design incorporates the use of MOSCAPs within the analog counter. These were selected for a smaller layout area. Because of the output source-follower, the voltage across the MOSCAPs should be at least a threshold voltage above GND for proper operation. In this same operating range, the MOSCAP will maintain capacitor-like behavior. This design is included in rows 12 - 15 of the pixel array. The relevant pins relevant for the operation of this circuit are described in Table 4.

Design 2: PQC+Analog counter 2

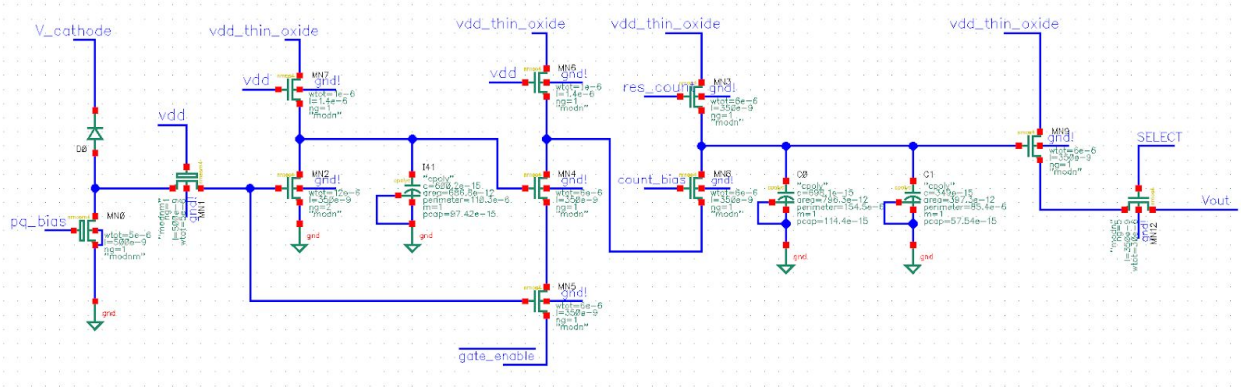


Figure 4: Schematic view of a passive quenching pixel plus analog counter with poly capacitors.

This design is largely the same as the previous design except for the use of polysilicon capacitors within the analog counter as opposed to MOSCAPS. This resulted in a larger layout area and consequently a reduction in the pixel's fill factor. This design is included in row 11 of the pixel array. For detailed descriptions of the relevant pins required to test this design see Table 4.

Net name	Pin(s)	I/O	Detailed function
v_cathode	18	I (A)	This pin gives access to the cathode of the APD. The node should be set to a high enough voltage such that the APD is operating in geiger mode.
pq bias	19	I (A)	This pin is used to bias the nmos transistor in the passive quenching circuit. A value of 1.2 volts was used in simulations assuming a breakdown current of 300 uA and an off current of 50 uA. The value of this voltage should be large enough to pull the anode of the APD down (quenching) but low enough to allow the APD to create a significant pulse when detecting a photon.
vdd	4	---	This pin connects to Vclamp in the schematic above. This voltage should be set to a value of +5 volts such that the APD pulse is clamped to a safe level for the subsequent devices and it also serves as a turn-on voltage for the pull-up nmos in the monostable gating circuit.
vdd thin oxide	10	---	This is the positive voltage supply of the smaller devices. Set this voltage to +3.3 volts.
gate enable	21	I (D)	Set to **0** to disable the gating circuitry. Set to **1** to enable the gating circuitry. When disabled the analog counters will not decrement and instead they will maintain their voltage level.
res count	8	I (D)	Set this pin to to reset the analog counter. Otherwise this pin should be set tied to ground.
count bias	9	I (A)	This pin is tied to the gate of the input NMOS device within the analog counter. Adjusting the voltage varies the step size of the analog counter. Larger bias voltage produces larger voltage decrements for the counter.

Table 4: Detailed list of pins relevant to Figures 3 and 4.

Design 3: AQC+Analog counter 1

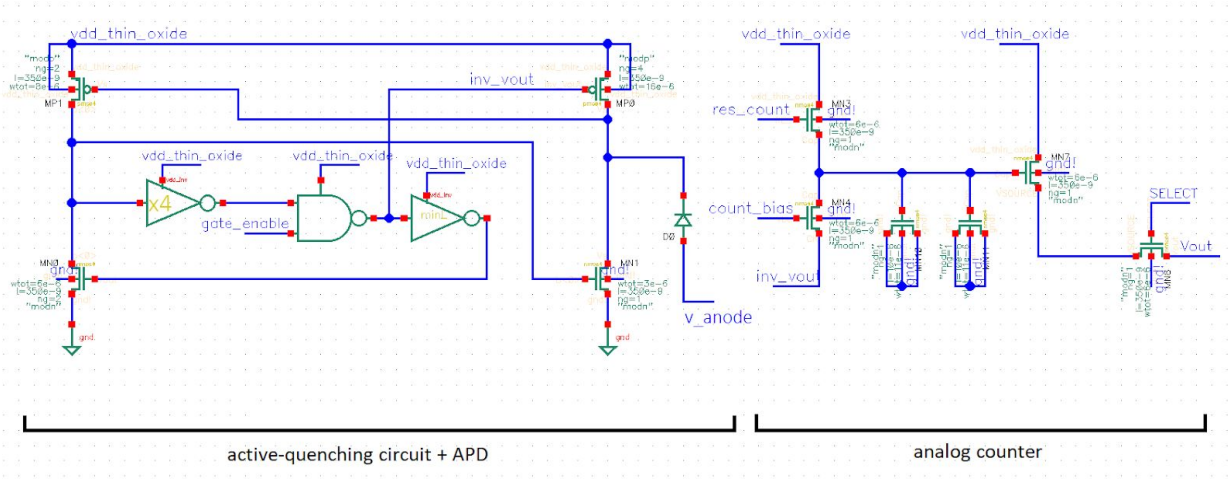


Figure 5: Schematic view of active quenching pixel #1 plus analog counter with MOSCAPs.

This circuit consists of an active quenching circuit (AQC) followed by an analog counter. Upon detecting a photon, the active quenching circuit lowers the voltage across the APD shutting off the avalanche current. Then the circuit will increase the voltage back to its original level so that the APD is again in geiger mode and can be ready to detect another photon. The time between shutting off the current and the resetting of the voltage across the APD is referred to as the hold-off time. This time is set by the series of inverters just before the NAND gate. The monostable pulsing circuit was omitted in this design because the pulse widths from the active quenching circuit are already quite narrow as will be seen in a later simulation plot. This circuit is featured in row 10 of the pixel array. The relevant pins for the operation of the circuit are described by Table 5.

Design 4: AQC 2+Analog counter 1

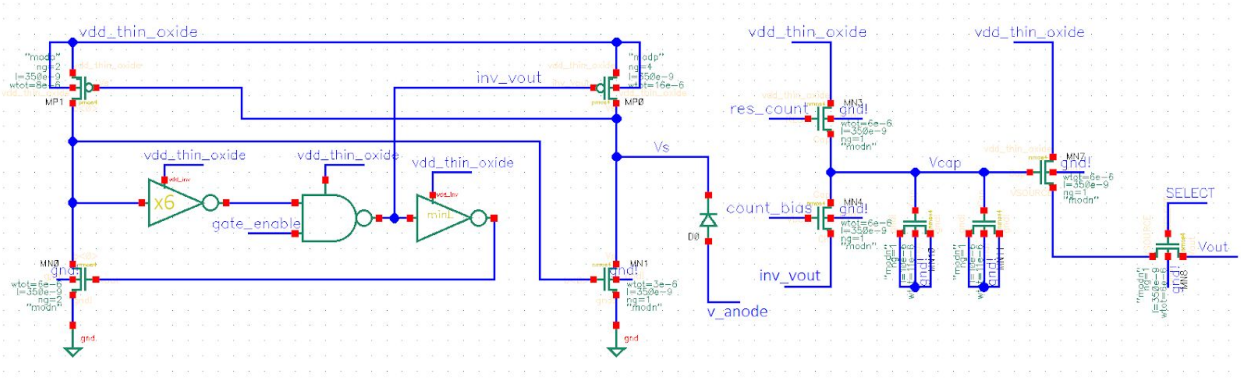


Figure 6: Schematic view of active quenching pixel #2 plus analog counter with MOSCAPs.

The second variation of the active-quenching pixel is shown in Figure 6. This variation only differs from the previous active-quenching pixel in that its hold-off time is made a bit longer to reduce the amount of after pulses while sacrificing the maximum count rate. This is done by increasing the number of inverters in the AQC just before the NAND gate. This circuit is featured within rows 8 - 9 of the pixel array. For detailed description of the relevant pins required to test this design see Table 5.

Net name	Pin(s)	I/O	Detailed function
vdd thin oxide	10	---	Positive voltage supply. Set this voltage to +3.3 volts.
v_anode	22	I (A)	This pin gives access to the anode of the APDs within the active quenching circuits. A negative voltage must be applied to ensure geiger mode operation.
gate enable	21	I (D)	Set to **0** to disable the gating circuitry. Set to **1** to enable the gating circuitry. When disabled the analog counters will not decrement.
res count	8	I (D)	Set this pin HIGH to reset the counter. Otherwise this pin should be LOW.
count bias	9	I (A)	This pin is tied to the gate of the input NMOS device within the analog counter. Adjusting the voltage varies the step size of the analog counter. Larger bias voltage produces larger voltage decrements for the counter.

Table 5: Detailed list of pins relevant to Figures 5 and 6.

Standalone Active quenching circuit

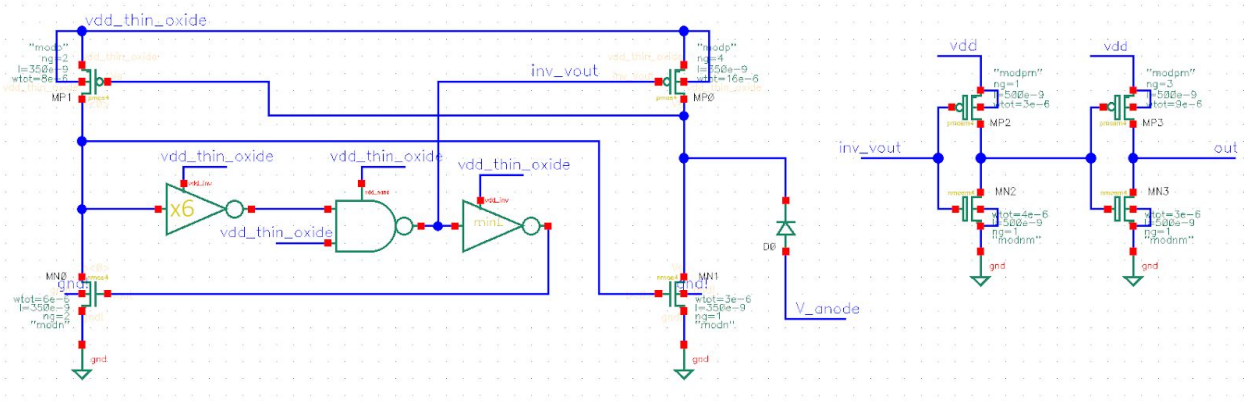


Figure 7: Schematic view of a standalone active quenching circuit #2.

An additional AQC is included for troubleshooting purposes. The standalone design includes the variation with the extra hold-time. To get the 3.3-V logic of the active quenching circuit to 5.5-V logic, the subsequent inverter after the AQC has its switching point lowered to about +1.6 volts. The output of the circuit is then transferred to a digital output pad. The relevant pins and their functions are described in Table 6.

Net name	Pin(s)	I/O	Detailed function
vdd thin oxide	10	---	Positive voltage supply. Set this voltage to +3.3 volts.
v_anode	22	I (A)	Anode of the APDs within the active quenching circuits. A negative voltage must be applied to ensure that the APD is operating in geiger mode.
aqc out	5	O (D)	Output of the individual active quenching circuit + APD.
vdd	4	---	Positive supply voltage for the two inverters after the AQC.

Table 6: Detailed list of pins relevant to Figure 7.

Standalone Analog Counter

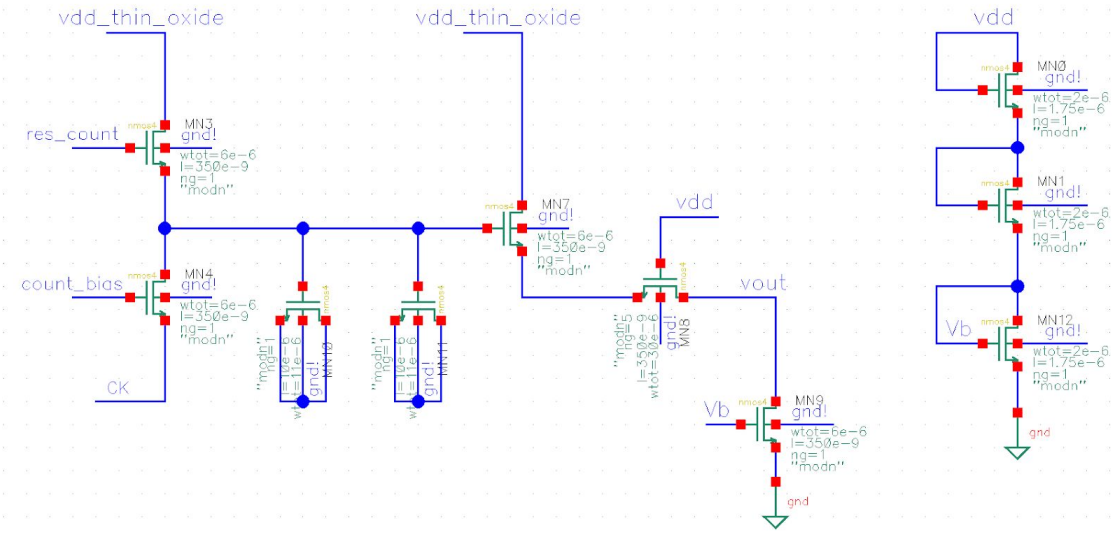


Figure 8: Schematic view of standalone analog counter with MOSCAPs.

An individual analog counter circuit is implemented into the chip for testing with a pulse generator. The relevant pins and their functions are included in Table 7.

Net name	Pin(s)	I/O	Detailed function
vdd thin oxide	10	---	Positive voltage supply of the smaller devices. Set this voltage to +3.3 volts.
vdd	4	---	This voltage should be set to a value of +5 volts. This pin is shared with other circuits including the pass gate in the PQC and the monostable gating circuit.
res count	8	I (D)	Set this pin to to reset the analog counter. Otherwise this pin should be set tied to ground.
count bias	9	I (A)	This pin is tied to the gate of the input NMOS device within the analog counter. Adjusting the voltage varies the step size of the analog counter. Larger bias voltage produces larger voltage decrements for the counter.
ck	7	I (A)	Input pin to the analog counter. Apply a short negative pulse to decrement the analog counter by a small amount set by the ‘count bias’ pin.
analog count out	6	O (A)	Output voltage of the analog counter.

Table 7: Detailed list of pins relevant to Figure 8.

Standalone Passive quenching circuit

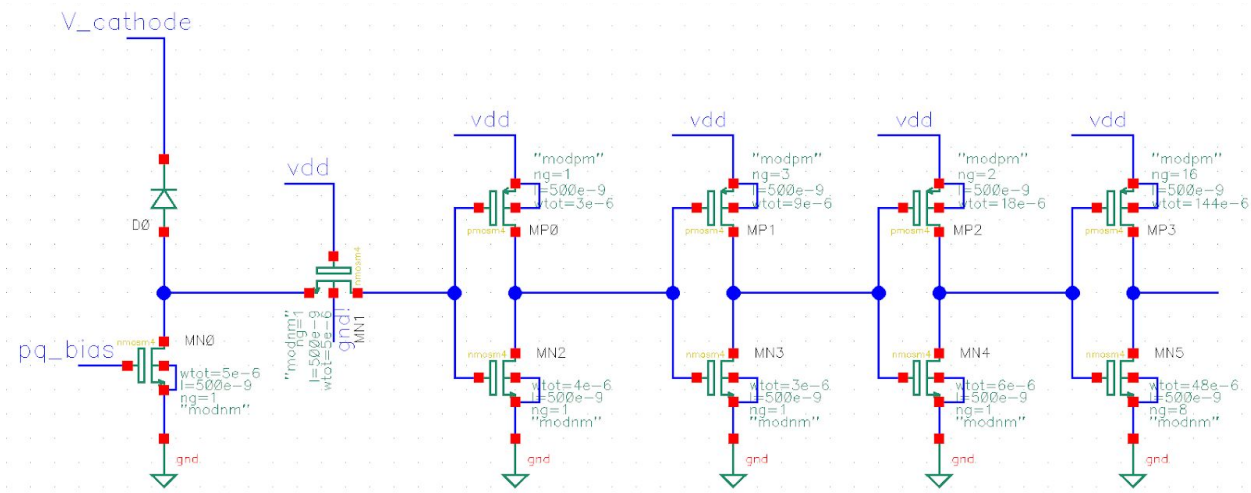


Figure 9: Schematic view of standalone passive quenching circuit.

An individual PQC was included for troubleshooting purposes. The passive quenching circuit was included in addition to the clamping NMOS pass gate. The first inverter has a lower switching point to account for the voltage limiting that occurs because of the pass gate. The subsequent chain of inverters serve to help drive a larger capacitive load. The last two inverters are usually included within the digital output pads but are instead shown here explicitly. The relevant pins and their functions are included in Table 8.

Net name	Pin(s)	I/O	Detailed function
vdd	4	---	This voltage should be set to a value of +5 volts. This pin is shared with other circuits including the pass gate in the PQC and the monostable gating circuit.
indv. v_cathode	43	I (A)	This pin gives access to the cathode of the APD within the individual passive quenching circuit. Set this pin to a high enough voltage to ensure geiger mode operation.
indv. pq bias	41	I (A)	This pin is used to bias the nmos transistor in the passive quenching circuit. A value of 1.2 volts was used in simulations assuming a breakdown current of 300 uA and an off current of 50 uA. The value of this voltage should be large enough to pull the anode of the APD
indv. pq out	42	O (D)	Output of the individual passive quenching circuit + APD.

Table 8: Detailed list of pins relevant to Figure 9.

Simulations

Simulating Design 1:

A simulation example of the first design is shown in Figure 10. The traces, from top to bottom, are the SPAD current (orange trace), SPADE anode voltage (red trace), output of the monostable pulse generator (green trace), analog counter reset (pink trace), gate enable (yellow trace), and the output of the analog counter (blue trace). For the following simulation the NMOS device which sets the amount of charge removed per photon detection had a gate voltage of 990-mV.

Figure 10: Simulation view for design 1.

Simulating Design 2:

A similar simulation is shown in Figure 11 for the second pixel design. From top to bottom traces are the anode voltage (red trace), the SPAD current (blue trace), output of monostable pulse generator (orange trace), gate enable (gold trace), reset (light green trace), and the output of the analog counter (green trace). As was done for the previous design the input NMOS device within the analog counter had its gate biased to 990-mV.

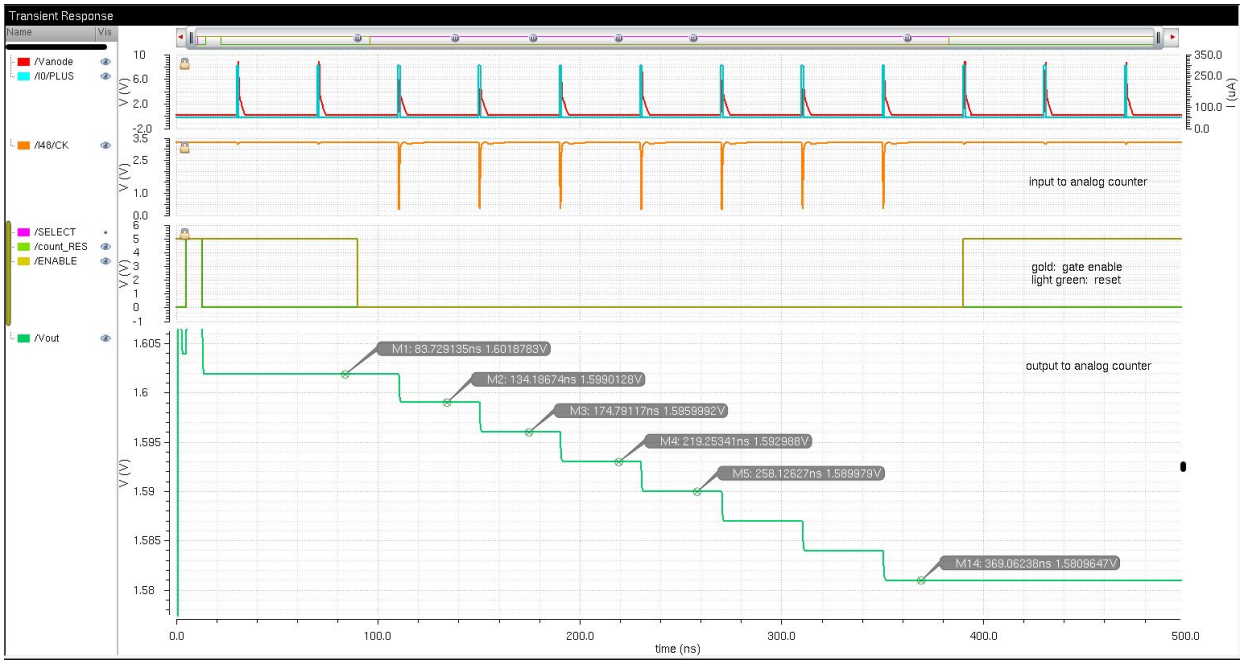


Figure 11: Simulation view for design 2.

Simulating Design 3:

A simulation of the performance of the third design is shown in Figure 12. From top to bottom the traces include the SPAD current (green trace), output of the active-quenching circuit (purple trace), reset to the analog counter (pink trace), gate enable (blue trace), output of the analog counter (red trace). The input NMOS device within the analog counter has its gate set to 530-mV to account for the wider pulse width from the lack of a monostable pulse generator.

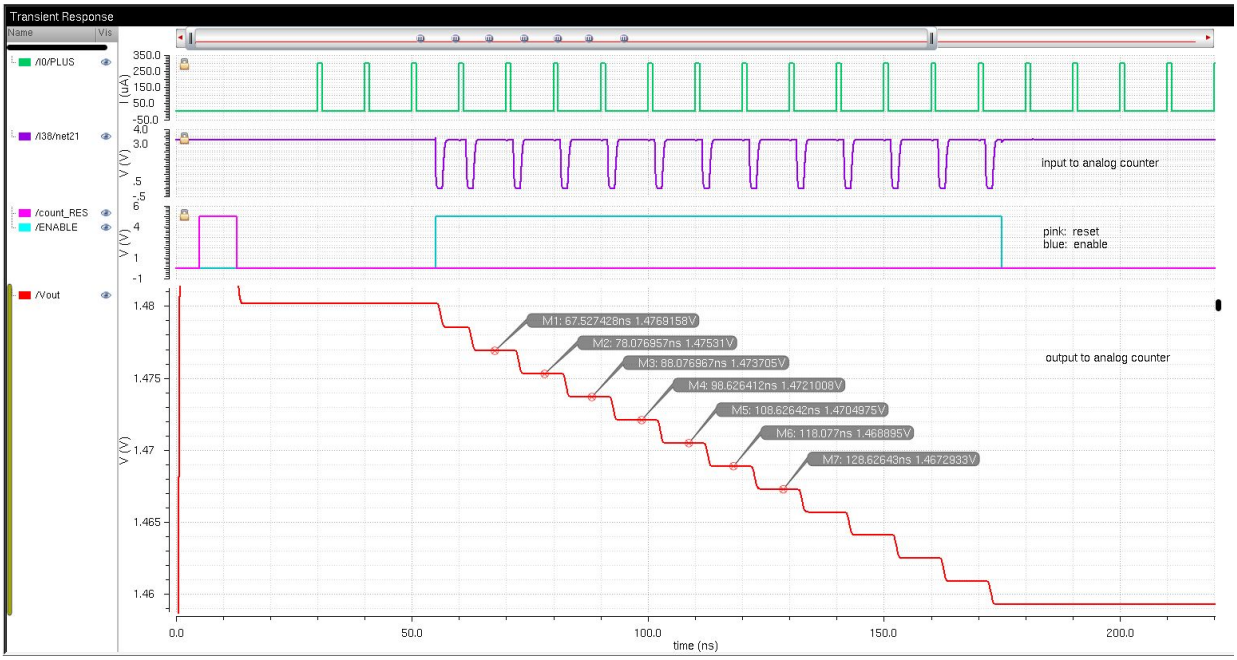


Figure 12: Simulation view for design 3.

Simulating Design 4:

A simulation of the fourth pixel design is shown in Figure 13. From top to bottom the traces include the SPAD current (green trace), reset to the analog counter (pink trace), gate enable (blue trace), and the output of the analog counter (red trace). The input NMOS device within the analog counter circuit has its gate biased to 480-mV in this simulation.

Figure 13: Simulation view of aqc with extra delay. The gate of the nmos in the analog counter was biased at 480 mV.

Simulating the individual passive quenching circuit:

A simulation of the standalone PQC is shown in Figure 14. The traces shown include the SPAD current (red trace), the anode voltage (green trace), the clamped voltage after the NMOS pass gate (blue trace), and the final output (pink trace). Note how the NMOS pass gate keeps the voltage from the quenching circuit from reaching too high of a value at the input of the 3.3-V devices.

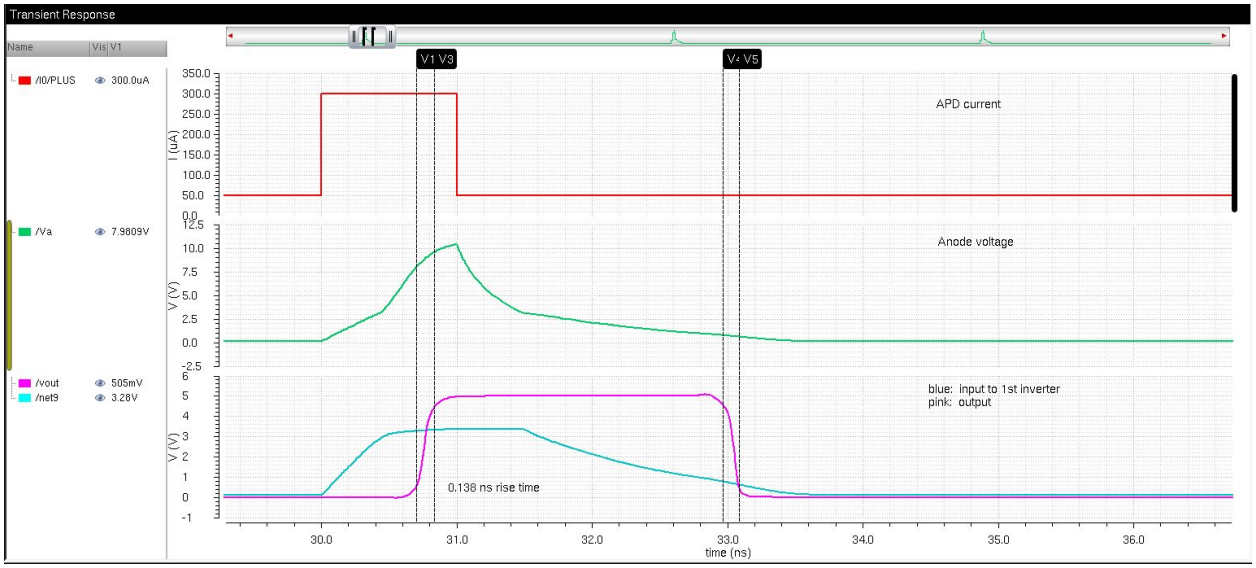


Figure 14: simulation of the individual passive quenching circuit.

Layout views

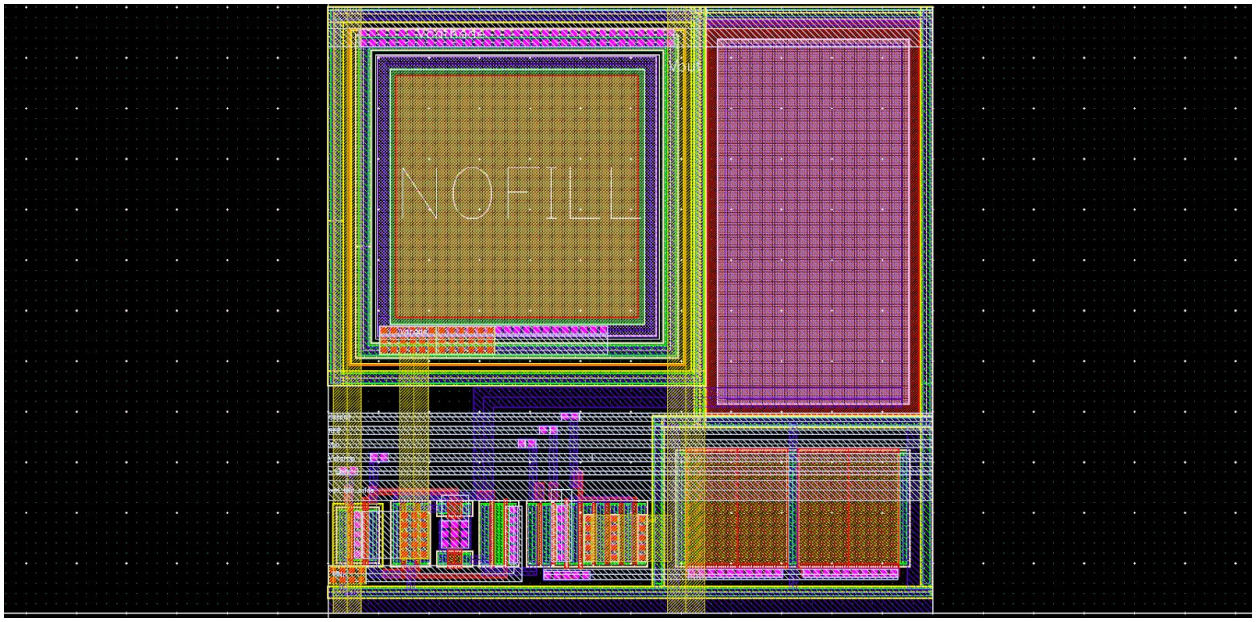


Figure 15: Layout view of pixel with design 1 + APD.

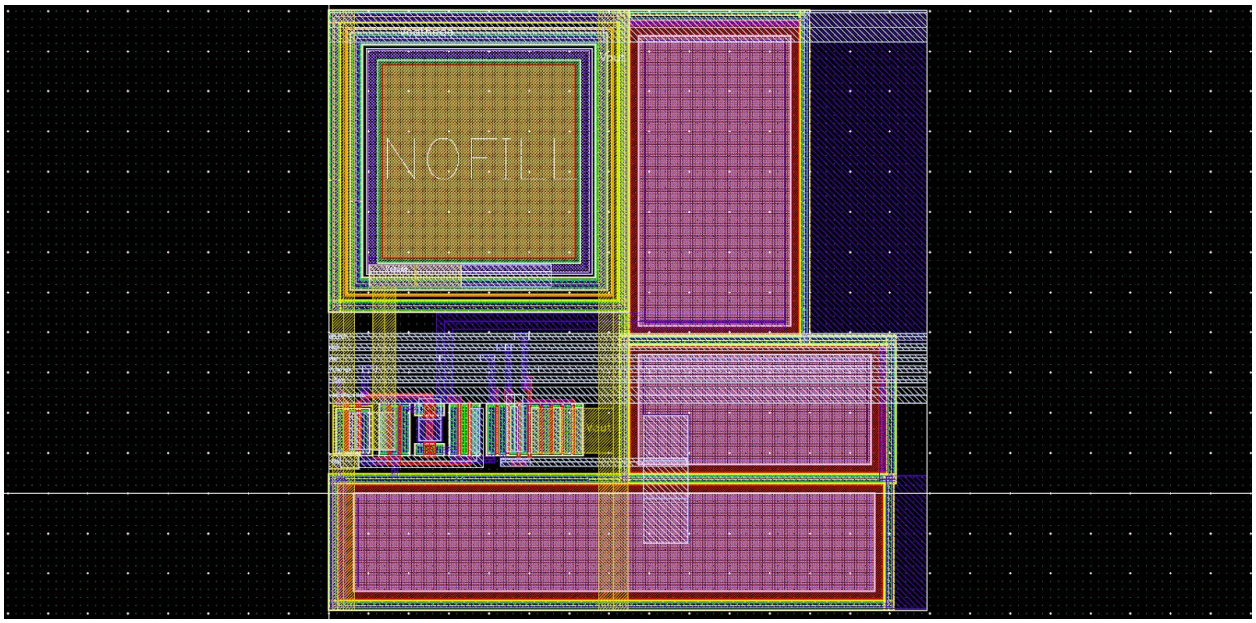


Figure 16: Layout view of pixel with design 2 + APD.

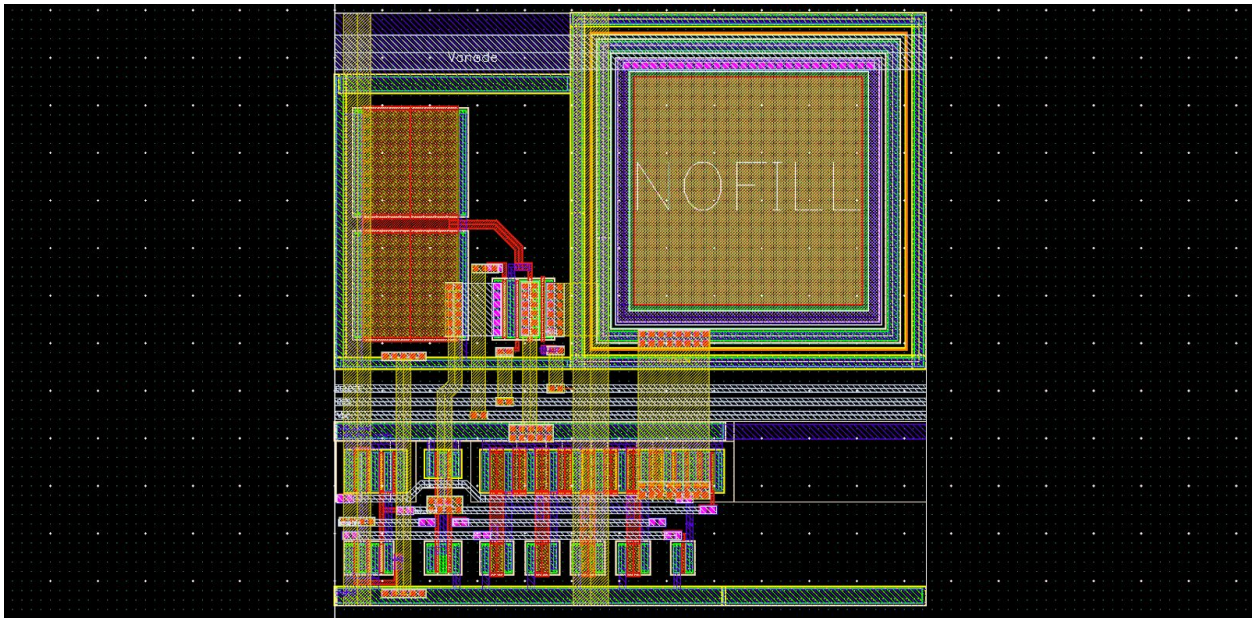


Figure 17: Layout view of pixel design #3.

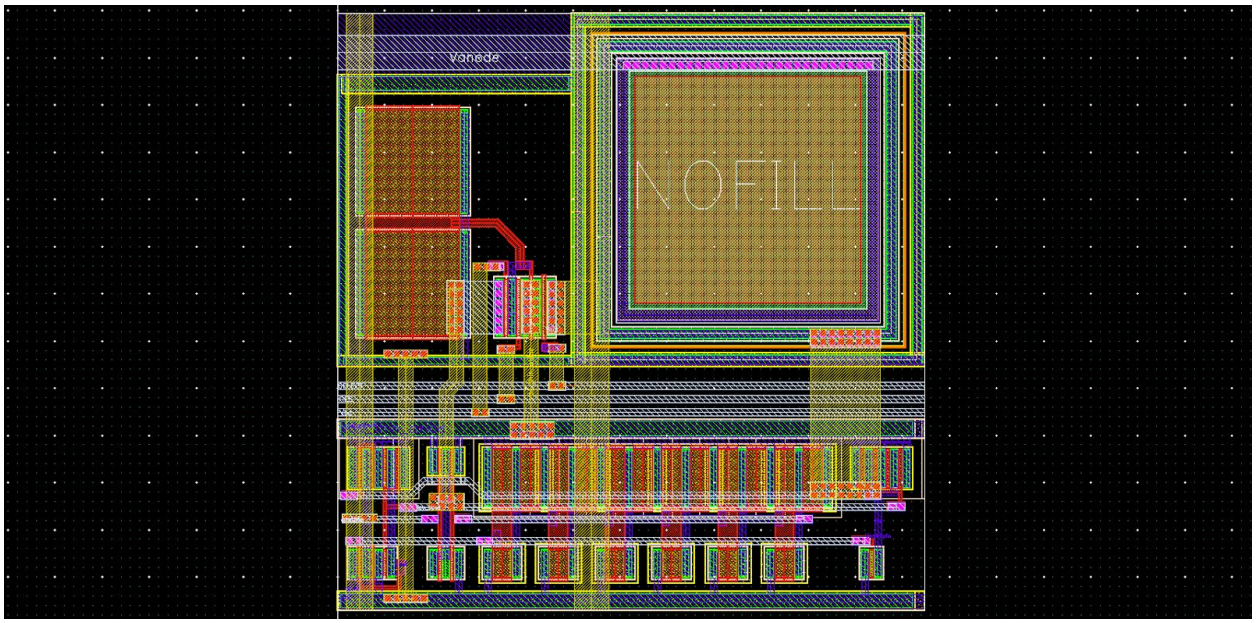


Figure 18: Layout view of pixel design #4.

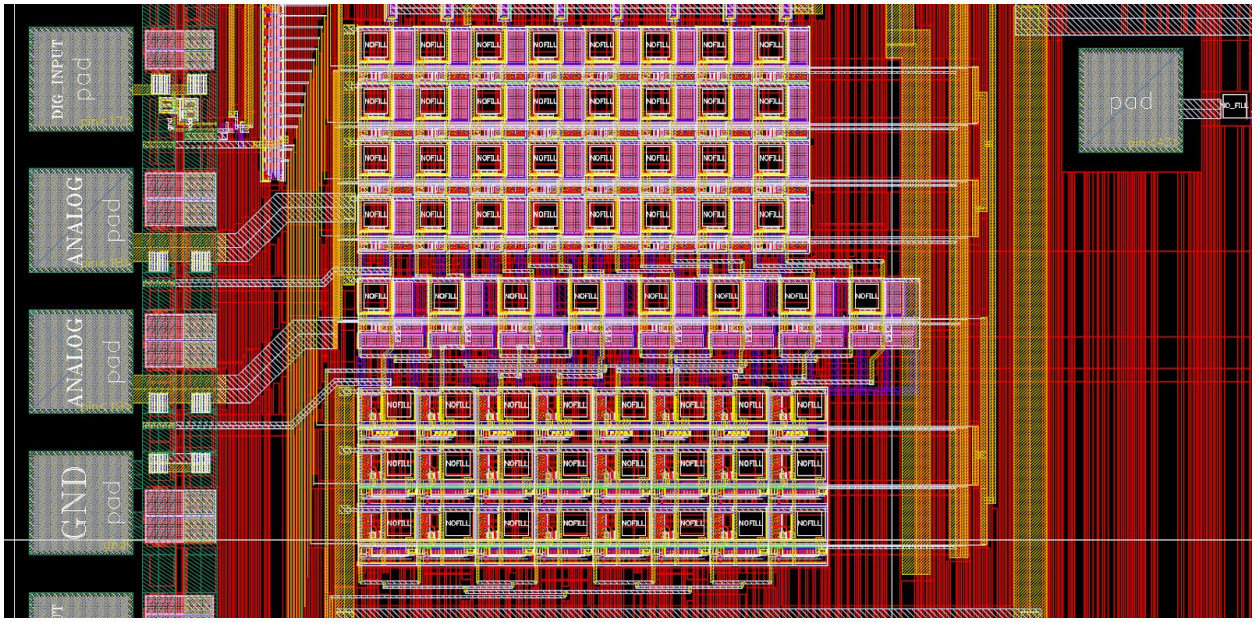


Figure 19: Layout view of the array which contains the various pixel designs.

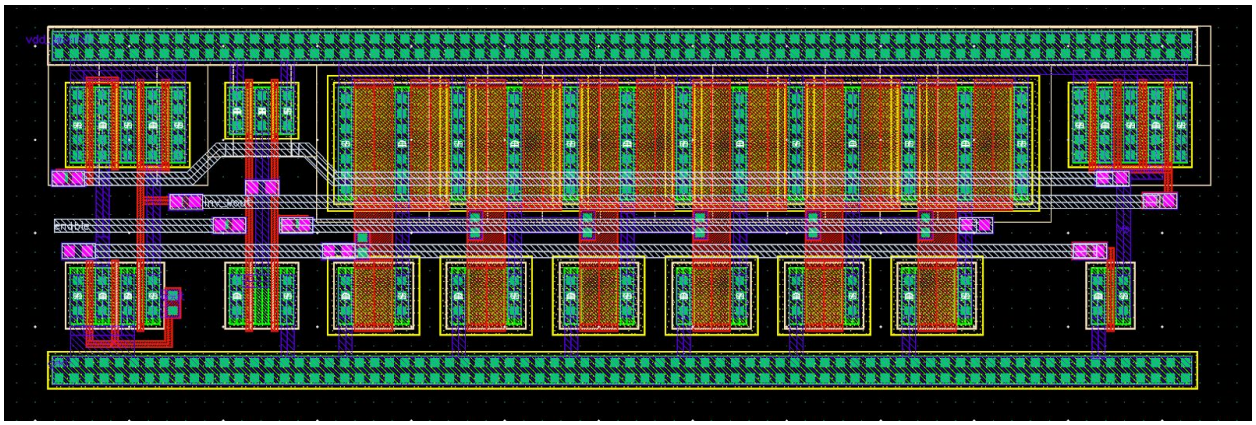


Figure 20: Layout view of AQC design 2 which features a larger hold-off time.

References

M. Perenzoni, “Single-photon avalanche diode-based detection and imaging,” *IEEE Solid-state circuits magazine*, vol. 10, no. 3, Summer 2018,

A. Eisele, R. Henderson, B. Schmidtke, T. Funk, L. Grant, J. Richardson, W. Freude, “185 MHz count rate, 149 dB Dynamic range single-photon avalanche diode with active quenching circuit in 130 nm CMOS technology,”

L. Pancheri, N. Massari, D. Stoppa, “SPAD image sensor with analog counting pixel for time-resolved fluorescence detection,” *IEEE Transactions on Electron devices*, vol. 60, no10, October 2013. pgs: 3442 - 3449.

A. Gallivanoni, I. Rech, M. Ghioni, “Progress in quenching circuits for single photon avalanche diodes,” *IEEE Transactions on Nuclear Science*, vol. 57, no. 6, December 2010.