Gonzalo Arteaga

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Education

M.S. in Electrical Engineering — *University of Nevada, Las Vegas* — GPA: 3.83 / 4.00 *Dec 2020*

B.S. in Electrical Engineering — *University of Nevada, Las Vegas* — GPA: 3.68 / 4.00 (*cum laude)* *Dec 2018*

Relevant Courses: Advanced Analog IC Design | Mixed-Signal IC Design | Memory Circuit Design

Experience

Research Assistant — UNLV Dept. of Electrical & Computer Engineering *May 2017 – Dec 2020*

- Designed integrated circuits including transimpedance amplifiers, SPAD quenching circuits, avalanche photodiodes (APD), and silicon photomultipliers for optical communication applications.
- Coordinated with a team of student research assistants to design, tape-out, and verify the designs of multiple test chips implemented in 350-nm and 180-nm SiGe BiCMOS processes.
- Designed a BiCMOS current-mode photon-counting circuit to interface with a photodetector in satellite-based LiDAR applications which could support count rates up to 1-GHz. The design featured a low static power consumption of 5-mW per channel and a small layout area. (Thesis)

Kiosk Assembler — AMW Precision LLC. — Las Vegas *Jan 2014 - Mar 2016*

- Assemble kiosks and their constituent parts as part of an assembly line. Trained new employees to assemble bill dispensers for cash-dispensing kiosks.

Skills

Software: Cadence Virtuoso, Assura Physical Verification, KiCad PCB design, Atmel Studio 7, LTspice, Spectre
Languages: MATLAB, C/C++, VHDL
Lab equipment: Power Supply, Oscilloscope, Function Generator, Multimeter, Soldering (through-hole & surface-mount)
Other: Fluent in Spanish (spoken/written)

Projects

Noise-shaping KD1S modulator ADC *Oct 2020 – Dec 2020*

- Designed a 1st and 2nd order multi-path delta-sigma modulator ADC with an ENOB of 7.4 and 8.9-bits respectively each with a conversion bandwidth of 3.25-MHz. Design included a differential ring oscillator for clock generation, single-stage op-amp, and clocked comparator.
- Implemented in LTspice using ON Semiconductor's 500-nm CMOS process and filtered using MATLAB.

Transimpedance amplifier *Oct 2019 – Dec 2019*

- Designed a TIA to interface with an avalanche photodiode with a total gain over 300-kΩ and a bandwidth of 140-MHz. Incorporated topologies which minimize influence of parasitic input capacitance.
- Implemented in LTspice using ON Semiconductor's 500-nm CMOS process.

SPAD photon-counting circuits *May 2018 – Aug 2018*

- Design four variants of geiger-mode APD sensors with passive or active-quenching circuits, a monostable pulse-shortening circuit, and an analog counter for in-pixel photon-counting.
- Designed with Cadence Virtuoso and fabricated using AMS 350-nm SiGe BiCMOS process.

Switch-mode power supply *Oct 2017 – Dec 2017*

- Designed a buck converter that outputs 3.75-V from a supply voltage ranging from 4 to 5.5-V with less than 1-mV ripple under loads that draw up to 100-mA. Used with an off-chip inductor and capacitor.
- Designed with Cadence Virtuoso and fabricated using ON Semiconductor's 500-nm CMOS process.

Low-voltage op-amp *Mar 2017 – May 2017*

- Designed an op-amp with an operating supply of 2 to 5-V, a DC open-loop gain of 78-dB, and a gain bandwidth product of 13-MHz. The circuit features a wide input voltage range that extends beyond the supply rails, a phase margin of 80-degrees, and a power consumption no more than 5.1-mW.
- Implemented in LTspice using ON Semiconductor's 500-nm CMOS process.