Design of K-delta-1-sigma modulator ADC

Using On Semiconductor's C5 process
ECG722 Mixed-Signal Circuit Design
Course project
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Abstract

A KD1S modulator is designed to replace the analog-to-digital (ADC) of Figure 9.32 using a continuous time topology. Two designs are proposed which include a 1st-order KD1S modulator with 8 feedback paths and a 2nd-order KD1S modulator with 4 feedback paths. The designs provide an effective sampling frequency of approximately 800-MHz and 400-MHz respectively and achieve a SNR greater than 34-dB with a bandwidth of 6.25-MHz.

Overview of KD1S design (first order)

A general continuous K-Delta-1-Sigma (KD1S) modulator schematic is shown in Figure 1. As the name implies, the circuit consists of a delta-sigma modulator with K paths and a single integrator. The circuit accomplishes better noise shaping by periodically updating the feedback signal K times for each sampling period. This causes the modulated noise to center around a much higher frequency of $(K \cdot f_s)\ /2$. Once filtered, a much larger resolution can be attained.

The feedback signals from the K paths are controlled with transmission gates which periodically open and close connecting the Kth path to the modulator. At any given time, only one path is connected to the modulator. As a result, the clock signals required for the circuit need to be carefully selected for best performance. In addition

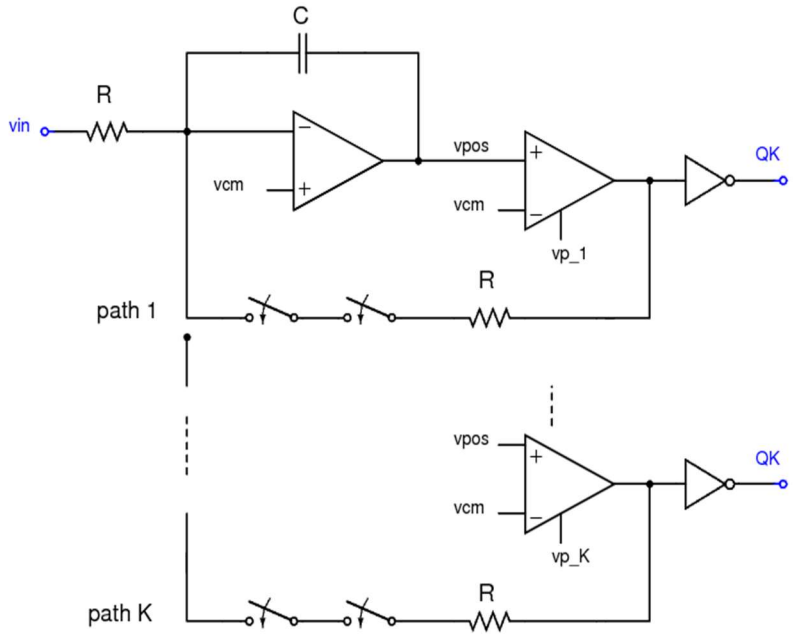

Figure 1: Schematic view of KD1S modulator

to that, a comparator which can resolve small differences in input voltages within a short decision time is important. Likewise, the amplifier within the integrator must be designed for high speed performance.

The designs of two KD1S modulators are presented. The first features a 1st-order modulator with 8 feedback paths while the second design features a 2nd-order modulator with 4 feedback paths. The design of the various components of this circuit are described below. This includes the design of the clock generator for both circuits, the timing of the clocks used in each path, the design of the operational amplifier within the integrator, and the clocked comparator. Following this, the proposed designs are presented along with simulated results which characterize their performance. Finally, the proposed designs are compared with the discrete-time KD1S modulator from Figure 9.32 in the course textbook and future work is suggested to improve on the presented designs.

Clock generation

The clock signals within the KD1S circuit are central to the function of the circuit. They oversee clocking the comparator as well as the transmission gates which control the feedback signals. A total of eight evenly spaced clock signals are required to fulfill the design requirements of an eight path KD1S modulator. To meet this goal a differential ring oscillator topology was adopted. A differential ring oscillator was chosen over a single-ended version because it could create oscillations with an even number of stages. A single-ended oscillator requires an odd number of stages which would not be able to produce an even number of equally spaced clocks. The unit cell for the ring oscillator is shown in Figure 2. The unit cell consists of a latch configuration of NAND and inverter gates which produce non-overlapping clock signals. The inverters on the right are increased five times in size to be able to drive larger capacitive loads. With the addition of the added driver inverters one can access to the clock signals within the oscillator with minimal impact on the internal oscillation frequency.

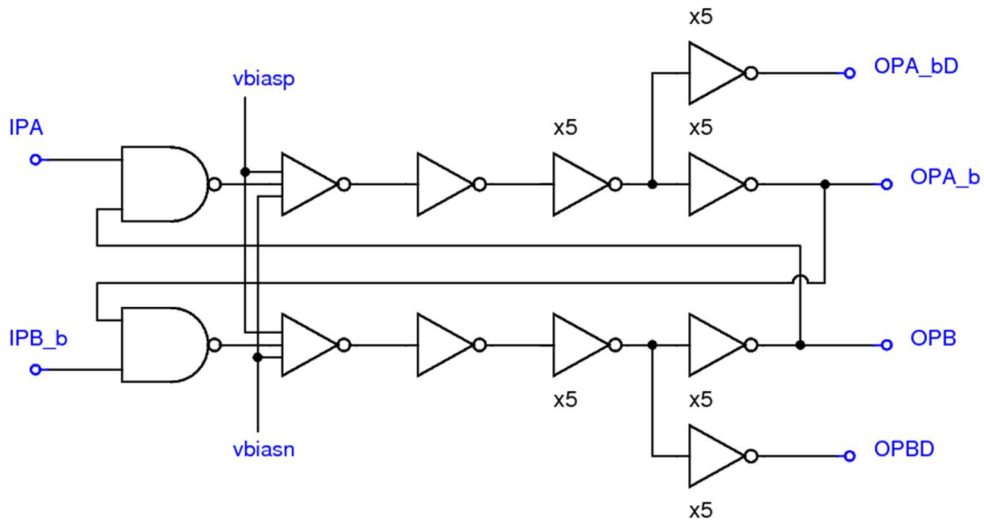

Figure 2: Oscillator unit cell

To produce variable oscillation frequencies, the first inverter in each path of the unit cell was replaced with the current-starved inverter shown in Figure 3 along with its corresponding biasing circuit. With this type of inverter, the charging and discharging current is set by the upper PMOS current source and lower NMOS current source. In this manner the time it takes to charge and discharge the input capacitance of the subsequent stage can be varied producing a variable oscillation. These currents are adjusted with a set of current mirrors which mirror

an input current set by the input voltage “vinvco” and resistor “R1”. Increases in the input voltage cause increases in bias current which result in smaller charge/discharge times and higher oscillation frequencies. Likewise, decreasing the input voltage results in lower oscillation frequencies.

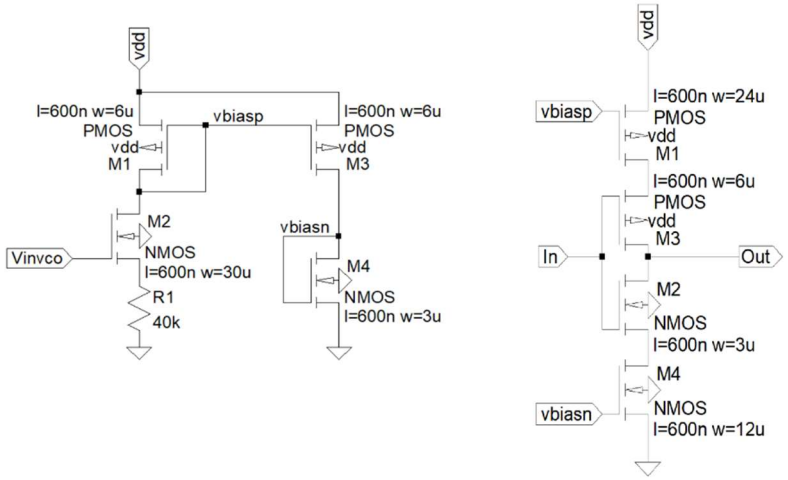

Figure 3: Current-starved inverter with biasing circuit

The complete schematic of the oscillator is shown in Figure 4. Here the unit cells are placed in series with one another and the final outputs of the last cell are switched and fed back to the first cell to create the imbalance necessary to create constant oscillation. In addition to the eight clock signals shown in blue (P<1:8>), the complements of these signals were also required throughout the modulator. To get the complements of each of the clock signals, additional inverters were used as shown in the figure.

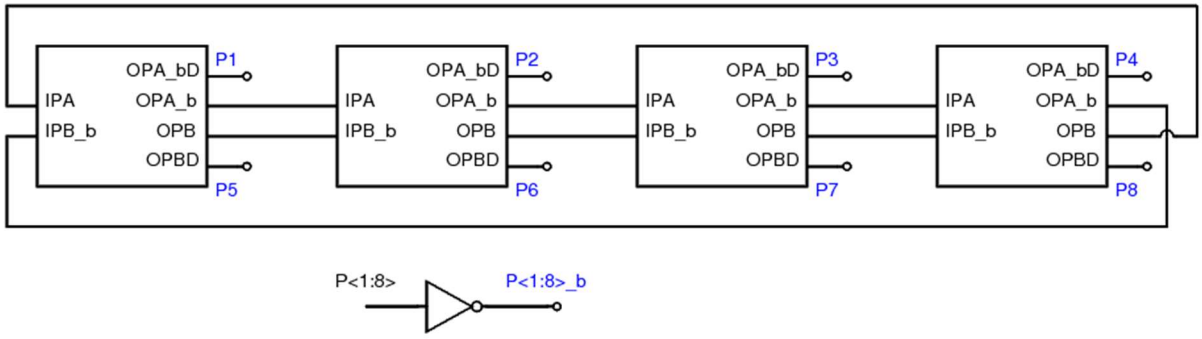

Figure 4: Complete schematic of the oscillator

A simulation of the clock signals from the oscillator is shown in Figure 5 when operating at its maximum frequency of 105-MHz. From this figure, one can see the eight equally spaced signals P1-P8. Although the resulting clock signals do not have a 50% duty cycle, only the rising edges are important to controlling the timing between the multiple feedback paths. An additional simulation is presented demonstrating the possible output frequencies of the clock generator given a certain input voltage. To get this plot, the oscillation frequency of the circuit was recorded after varying the input voltage in 500-mV steps from 1-V to 5-V. The resulting input voltage versus frequency plot is shown in Figure 6. The oscillator has an output frequency range of 50-MHz to 105-MHz.

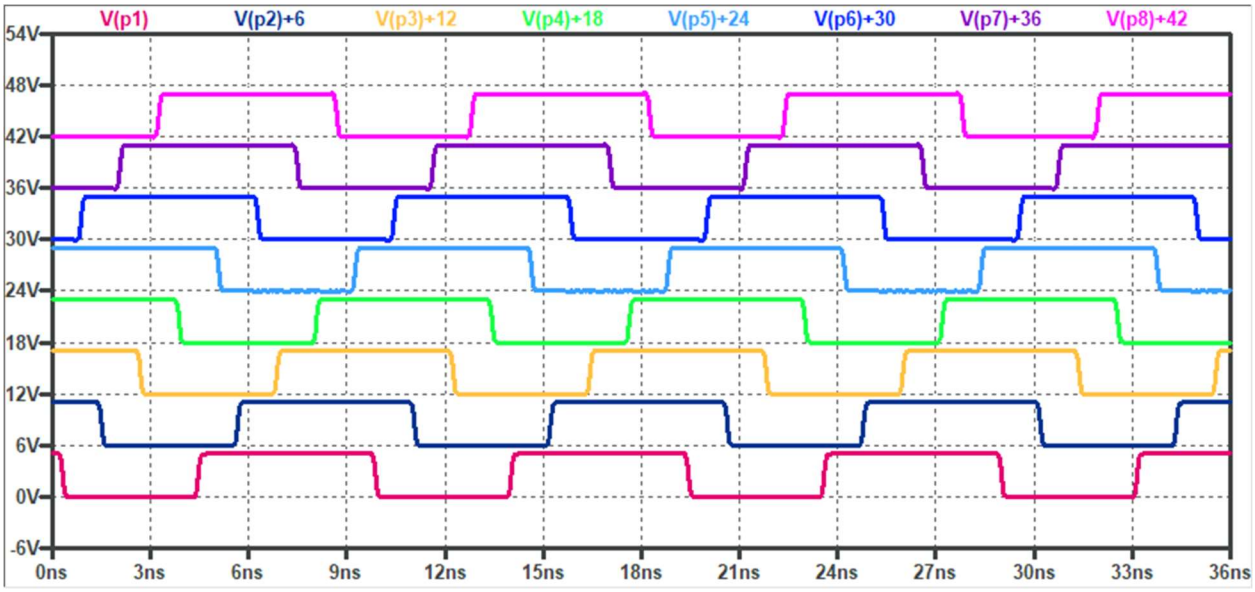

Figure 5: Clock signals from oscillator

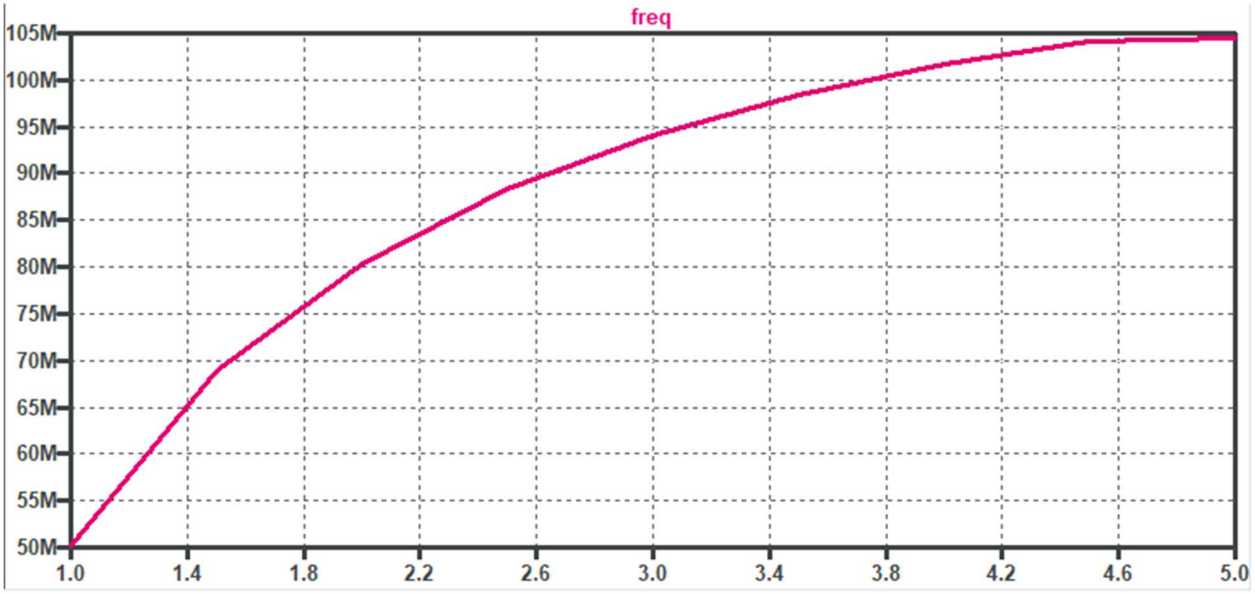

Figure 6: Input voltage versus output frequency plot

Description of clock timing

To describe the timing of the KD1S, the single path schematic from Figure 7 is considered. The clock timing signals associated with the first path are shown in Figure 8. As seen in Figure 8, the first signal to transition high is signal V(p3_b) (yellow trace) which is the complement of signal V(p3). This turns on the left transmission gate shown in Figure 7. Next, the comparator is clocked on the rising edge of signal V(p1) (red trace). A slight delay is allowed for the comparator to make a full decision before the signal V(p2) (blue trace) turns on the right transmission gate connecting the comparator output to the modulator through the feedback path. After one eighth of the sampling period, V(p3_b) shuts off the left transmission gate disconnecting the first feedback path. At the same time V(p3) will turn on the right transmission gate of the subsequent feedback path repeating the process.

As soon as the first feedback path is disconnected, the second feedback path is attached with minimal gap in between. The time windows showing when each feedback path connects to the KD1S modulator is shown in Figure 9. Here the corresponding signals of each feedback path are multiplied with each other to demonstrate where they overlap. Note how as soon as one window closes, the window of the subsequent feedback path is opened. At the maximum oscillating frequency of 105-MHz, the windows for each path have a width of 1.2-ns.0

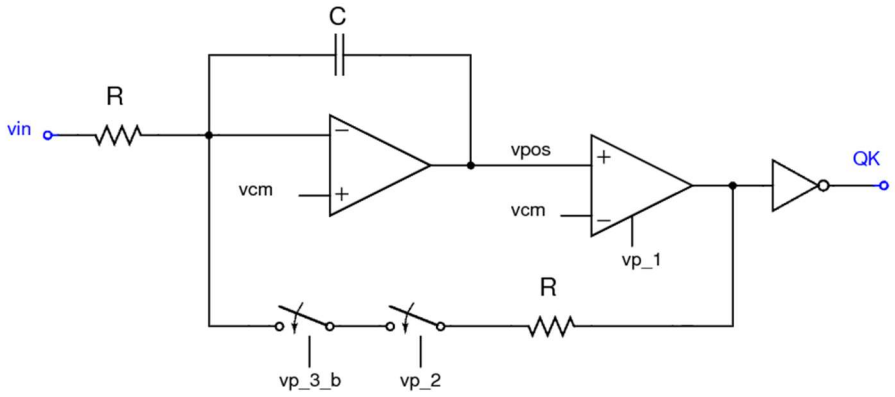

Figure 7: Single path view of KD1S

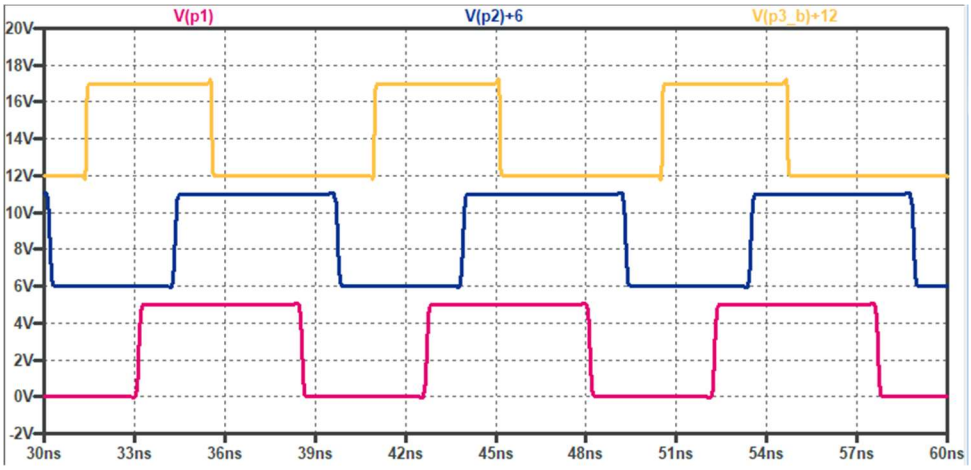

Figure 8: Clocks used in the first path of the 8-path KD1S design

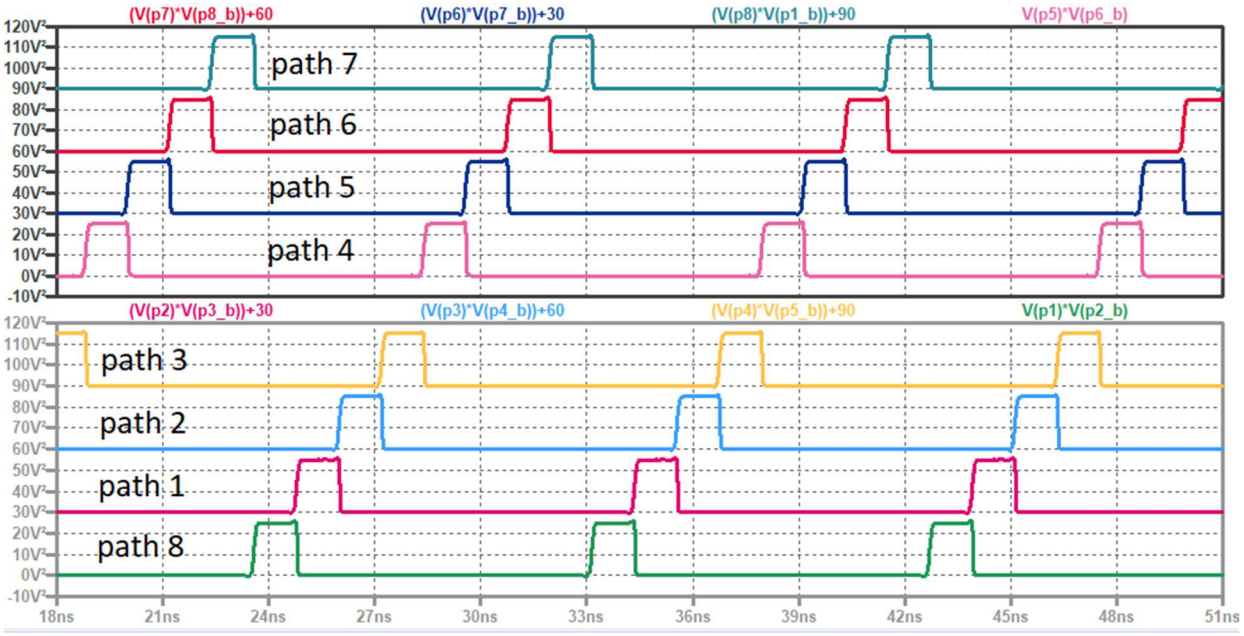

Figure 9: Clocking windows for the 8-path KD1S design

A similar setup is provided for the 4-path design. The same oscillator used in the 8-path design can be used for four paths with slight alterations in the choice of clock signals. With the four-path design, one must construct four windows where each path connects to the modulator again with minimal gaps in between. A plot of the clock signals associated with the first path of the 4-path design is shown in Figure 10. Using the same schematic from Figure 7, the first signal of interest is signal V(p4_b) (pink trace) which turns on the left transmission gate. Next, the comparator of the first path is clocked on the rising edge of V(p1) (blue trace). After a short time is granted to the comparator to decide, clock V(p2) (purple trace) turns on the right transmission gate connecting the first path to the modulator. Finally, V(p4_b) turns off severing the feedback path while the second feedback path starts to attach to the modulator.

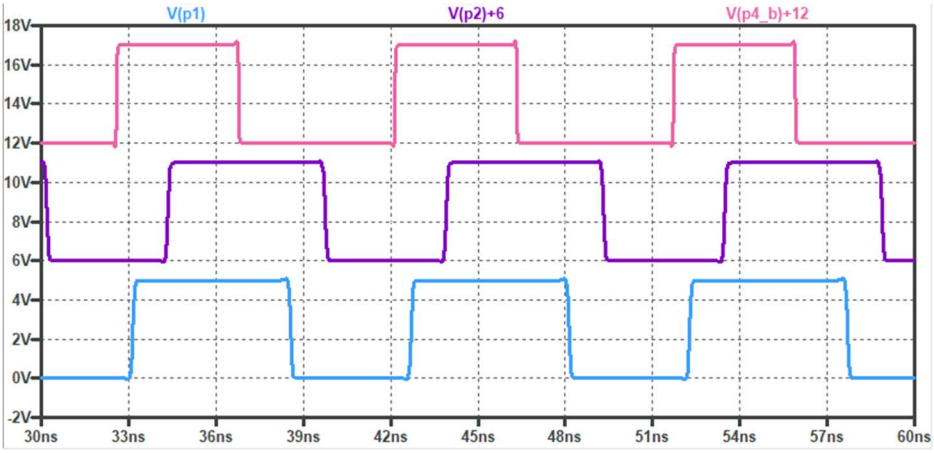

Figure 10: Clocks used in the first path of 4-path KD1S design

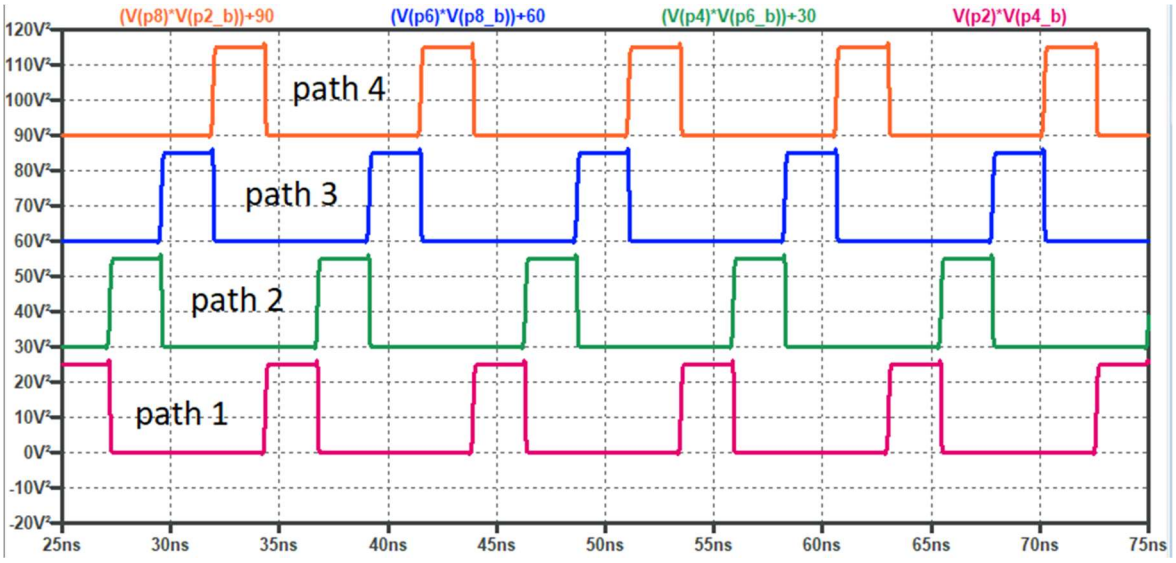

Figure 11: Clocking windows for the 4-path KD1S design

The four windows of the 4-path design are shown in Figure 11 with their corresponding paths labelled. Once again, the windows are kept equally spaced with minimal gap between subsequent windows. At the maximum frequency of 105-MHz, the windows have a width of approximately 2.3-ns.

Amplifier design

The amplifier used in the integrator is shown in Figure 12. The amplifier consists of a differential amplifier with a local common-mode feedback network formed by the two 10-KΩ resistors. This amplifier was chosen for its simple design and because both output nodes can swing up and down around a common voltage. A drawback to using this circuit is the need for a voltage to bias the tail PMOS devices. A simple PMOS current mirror with a biasing resistor can be used to provide a simple biasing circuit. The large current mirror ratio at the tail of the amplifier was selected to facilitate fast voltage swings even with the capacitive load of the gate of a comparator for example.

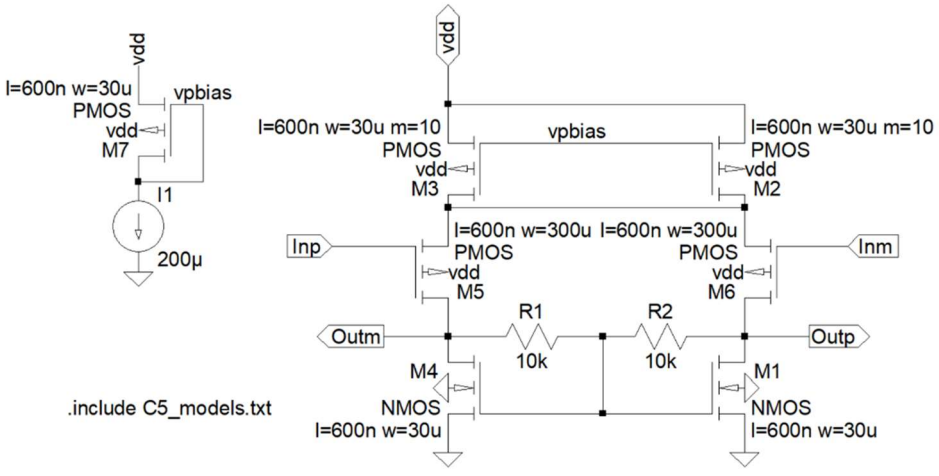

Figure 12: Schematic view of amplifier

A DC simulation of the amplifier is provided in Figure 13 to show the DC gain as well as the output voltage swing. Both outputs of the amplifier will be applied to the subsequent comparator. The lower pane of the figure shows a DC gain of approximately 19 which will suffice four our application.

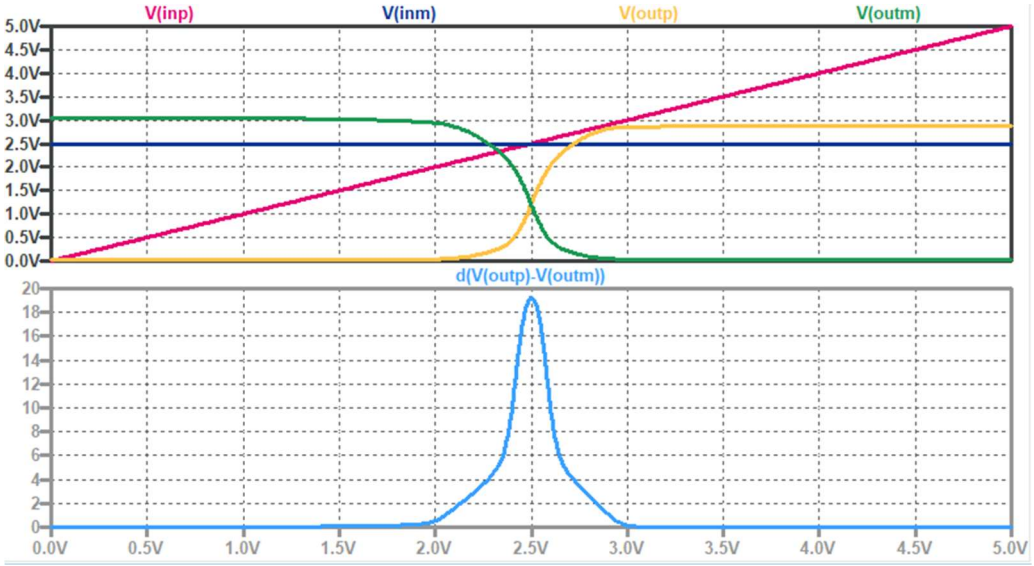

Figure 13: Simulation plot of DC sweep of the amplifier

Comparator design

The clocked comparator is used to periodically update the feedback signal within the KD1S modulator. As a result, we require a comparator which can quickly resolve the small differences between its two input voltages. To accomplish this, the circuit shown in Figure 14 was adopted. The circuit consists of a cross-coupled inverter latch which uses positive feedback to make fast decisions. This specific topology benefits from a reduced power consumption since there is no point in which contention current flows from the supply. Additionally with the use of the input stage in Figure 15, the comparator has a wide input voltage swing. Also shown in Figure 14, is a set of inverters to square the input clock signals as well a NAND gate latch on the output to prevent overlapping digital output signals. After the latch, a set of larger inverters are used to drive a larger output load.

A simulation showing the operation of the comparator is provided in Figure 16. The input signal consists of a ramped voltage while the negative input terminal is kept at a voltage of 1.2-V which is the voltage at which the output of the amplifier is centered. The output signal shows a slight offset on the comparator as seen by the early rising edge of the green trace.

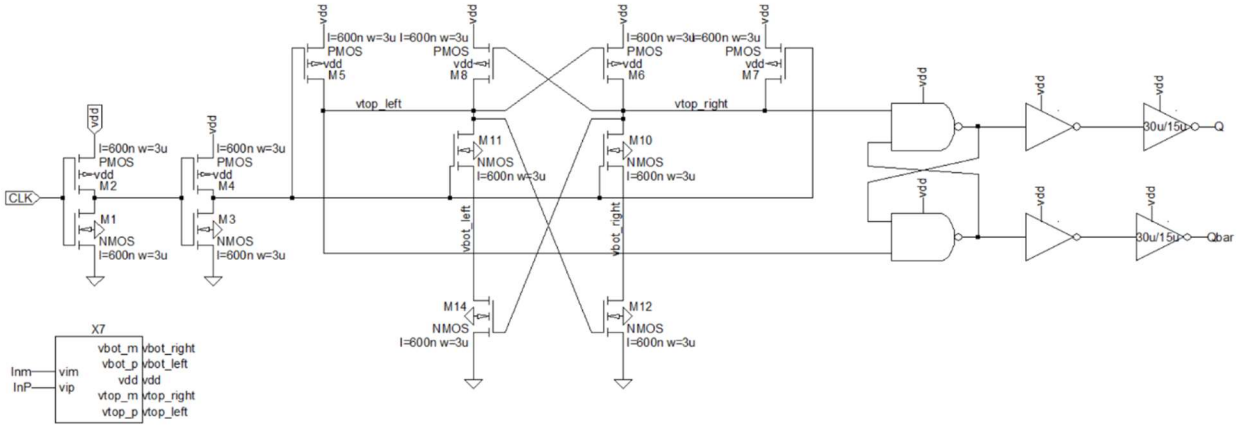

Figure 14: Schematic view of comparator

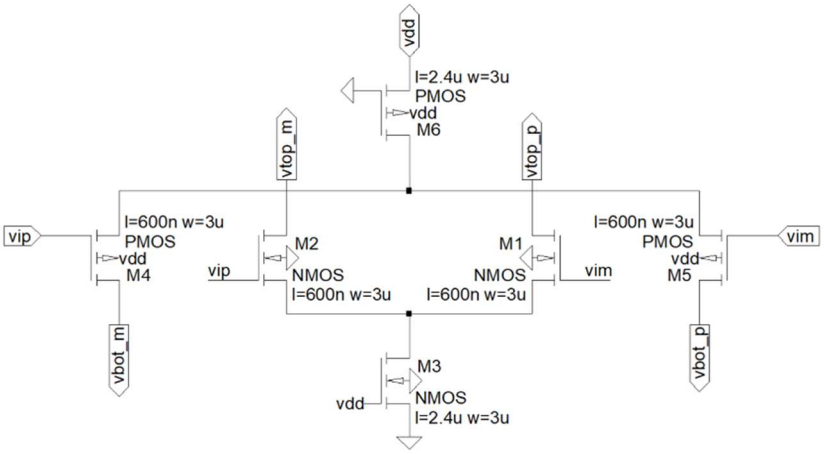

Figure 15: Schematic view of the input stage of the comparator

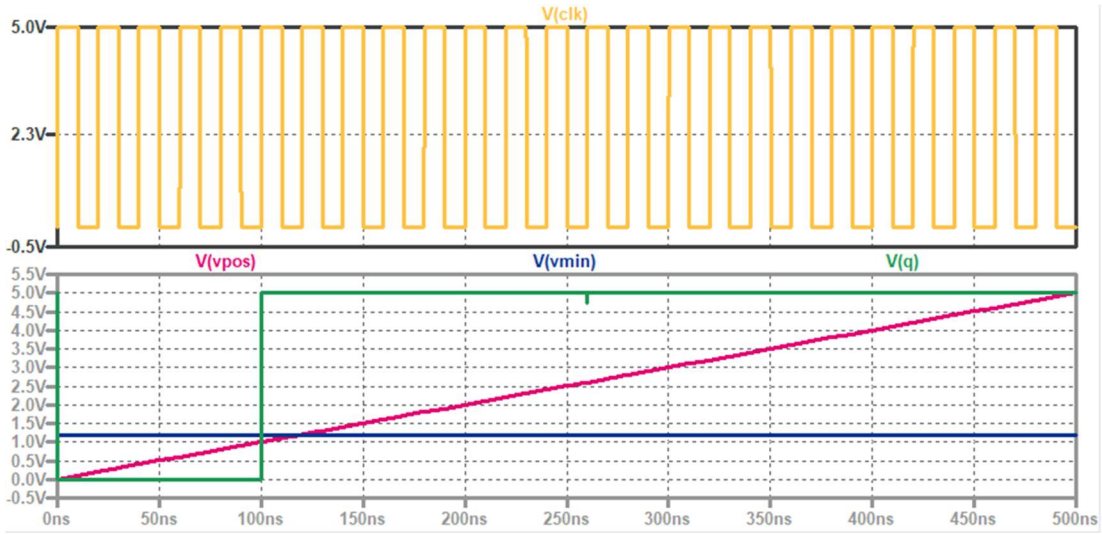

Figure 16: Transient simulation of comparator

Transmission gate design

The transmission gates used in the circuit consist of a parallel combination of a PMOS and NMOS pass gates. This combination allowed for the proper transmission of both HIGH and LOW voltage signals. Additionally, the devices were sized up to minimize the voltage drop that occurs when current flows through them. When it comes to laying out the circuit in a fabricated chip, a dummy transition gate is also placed in the forward path to improve matching between the forward and feedback paths. These specific transmission gates are always turned on. This can be seen in the schematic view shown in Figure 18.

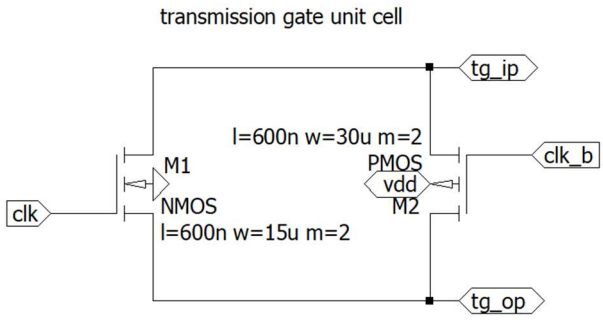

Figure 17: Schematic view of transmission gate

Design 1: First order KD1S modulator design

The first KD1S design consists of a first order modulator with eight feedback paths. A single path view of the design is shown in Figure 18. As seen in the schematic, the design assembles the components previously addressed in the prior sections. The appropriate clocking signals can be seen on the input of the transmission gates. Here the first path uses the clocking signals as shown in Figure 9. The full view of the eight paths are shown in Figure 19 along with its oscillator and output registers.

To analyze the operation of the single path we consider the case where a current is injected into the forward path of the modulator. As a current is injected into the forward path, the negative input terminal of the amplifier will start to increase in voltage. That causes the positive output terminal to move towards GND while the negative output terminal simultaneously moves towards VDD. This dual movement creates a wider output swing, which helps the comparator make much more accurate decisions. At this point the comparator will see that its negative input voltage is larger than its positive input. As soon as it is clocked, the comparator will output a LOW voltage which will sink current away from the negative input terminal of the amplifier countering the input signal and providing negative feedback.

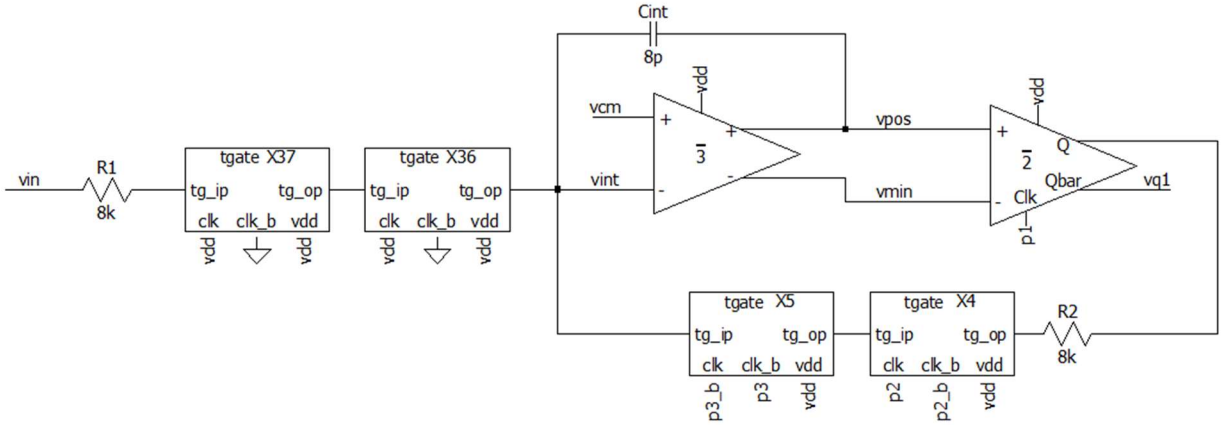

Figure 18: Single path view of the 1st-order, 8-path KD1S design

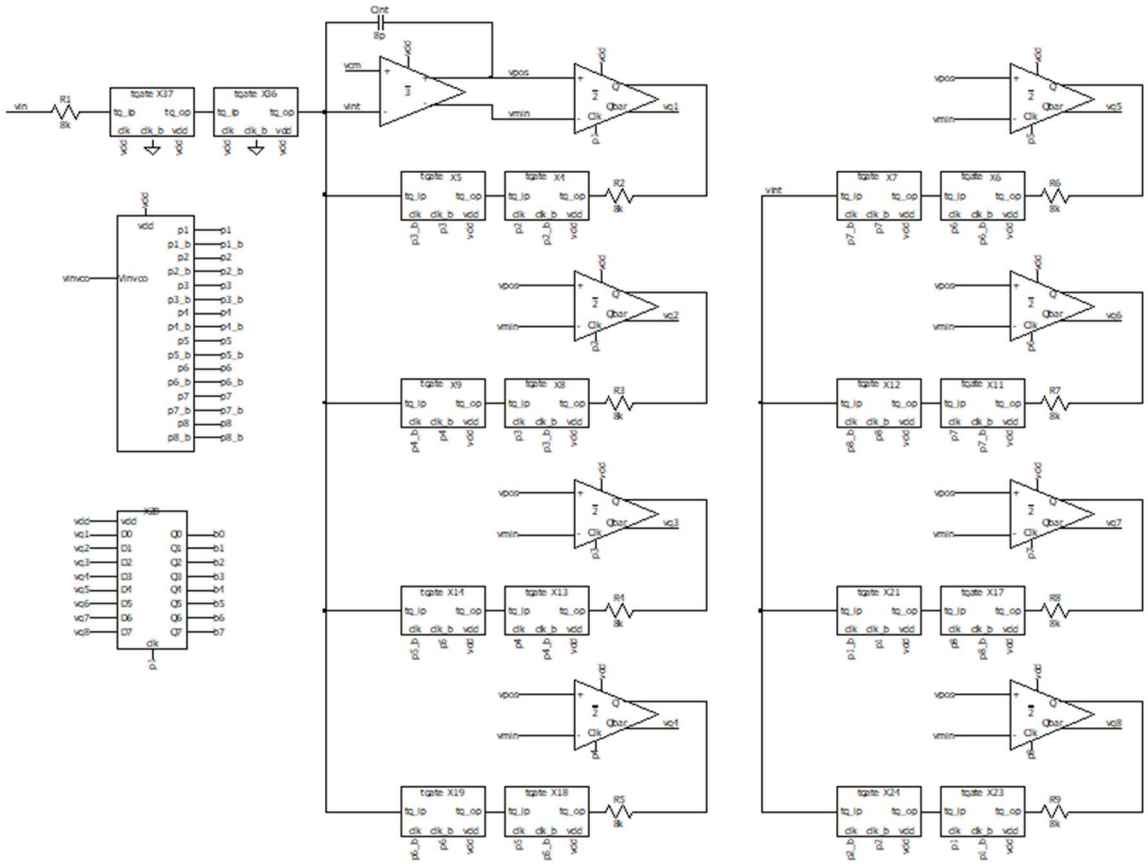

Figure 19: Schematic view of 1st-order, 8 path KD1S modulator

DC characterization: ramp simulation

To characterize the DC performance of the modulator, a slow ramp voltage signal is applied to the input of the modulator while plotting the average of the eight digital outputs. The results of the simulation are shown in Figure 20. As seen in the figure, the simulated output contains short transient spikes which get worse as the input voltage rises. There are a few dead zones within the plot however the major issue with this design is that the slope of the averaged output is shifted downwards slightly as seen by the fact that the output signal (green trace) never goes above 3.75-V.

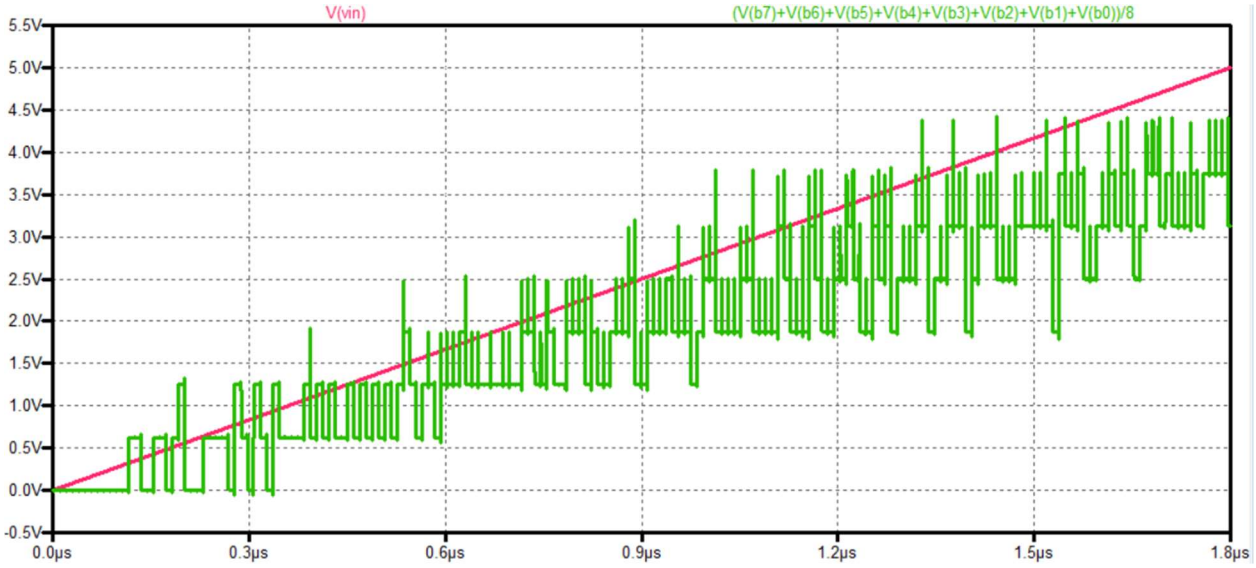

Figure 20: Simulation plot of ramp test for first KD1S design

Design 2: Second-order KD1S modulator design

An additional KD1S design was pursued that utilized only four feedback paths but with a second order modulator. The additional integrator helps shape the noise such that is much flatter within the bandwidth of interest. The complete schematic of the 2nd-order design is shown in Figure 21. The design is largely similar to that of the previous 1st-order design except for the additional integrator and different clock signals used to time everything as seen in Figure 11.

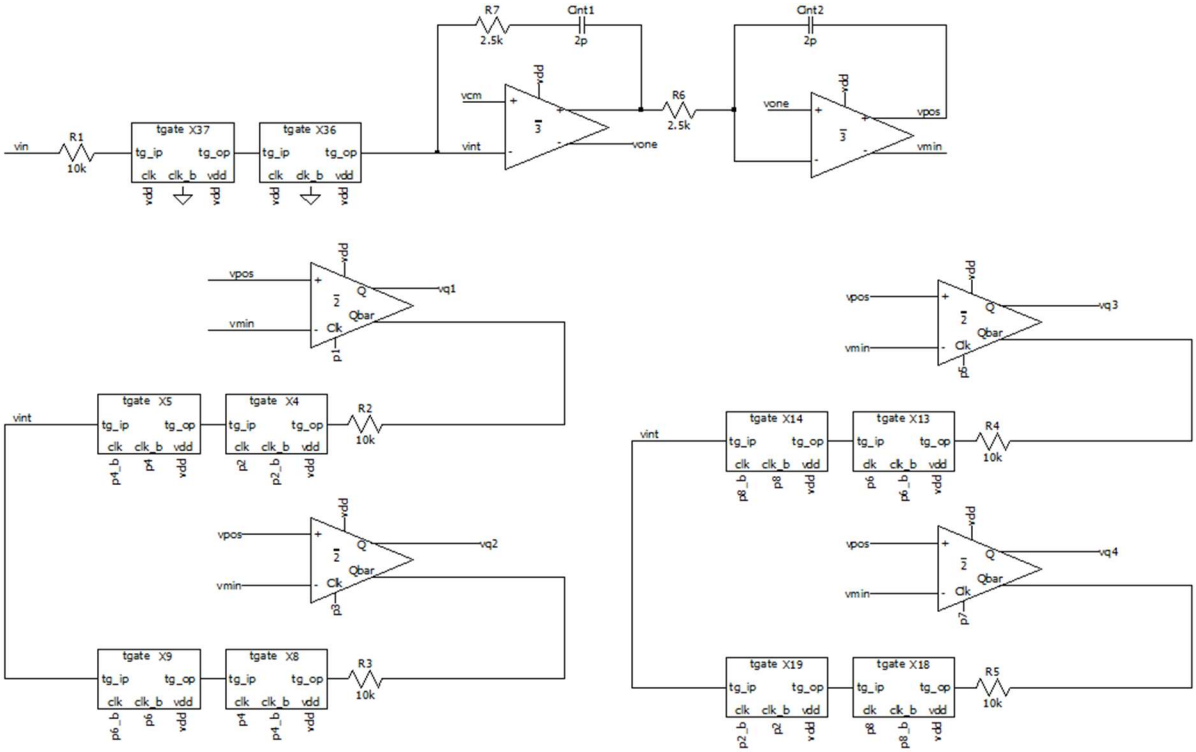

Figure 21: Schematic view of second order KD1S modulator with 4 paths

DC characterization: ramp simulation

A similar ramp test is applied to the input of the second design and is shown in Figure 22. Again, there are transient spikes that occur throughout the plot. There is a small dead zone that occurs when the input voltage is equal to approximately 3-V. Like the previous design the averaged output has a hard time reaching voltages above 4-V.

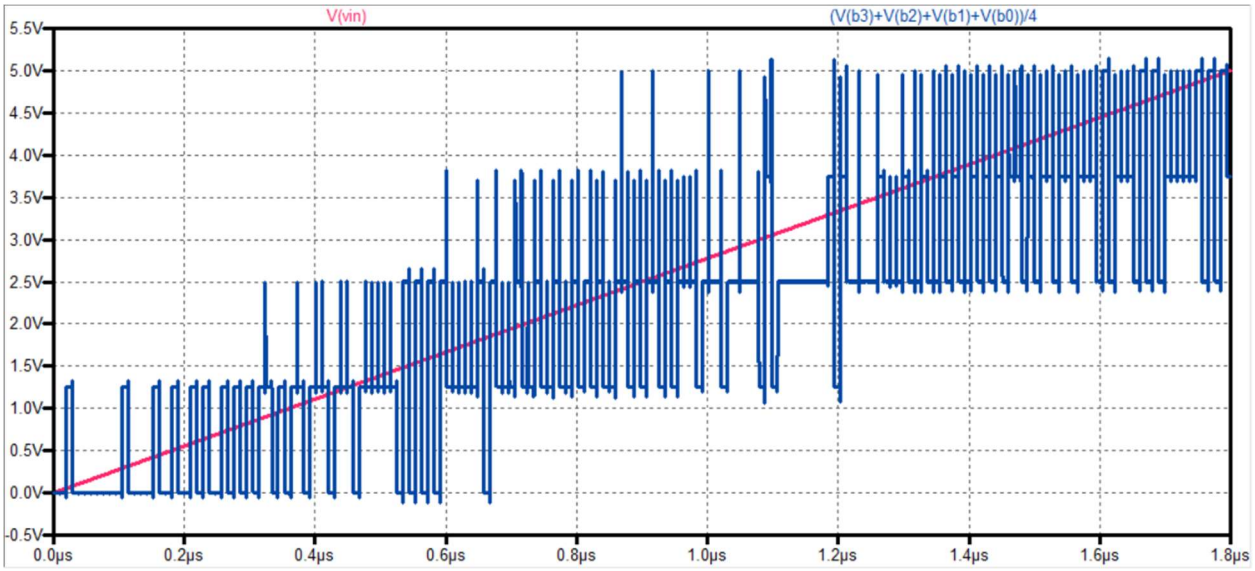

Figure 22: Simulation plot of the ramp test applied to the second order design

Noise-shaping characterization

To compare the designs with regards to how well they perform noise-shaping, digital filters are used with the help of MATLAB. The simulations are initially performed in LTspice by subjecting the designs to a sine wave input signal with an amplitude of 2-V, a DC offset of 2.5-V, and a frequency of 1-MHz. The outputs of these simulations are then digitally filtered, and a corresponding signal-to-noise ratio (SNR) is produced for comparison between the designs. Example simulations are shown for the first and second designs in Figure 23 and Figure 24 respectively. Note that these figures show only two periods of the simulation whereas the simulations used for MATLAB featured much longer run times.

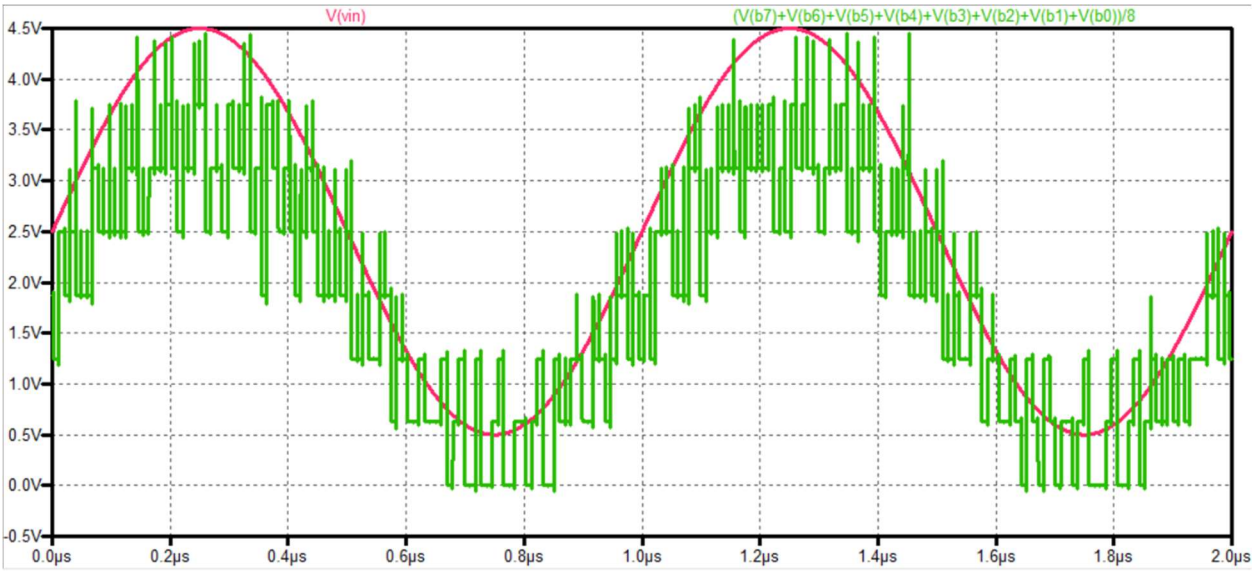

Figure 23: Simulation plot showing response to 1-MHz, 2-V amplitude input sine wave applied to the first order design

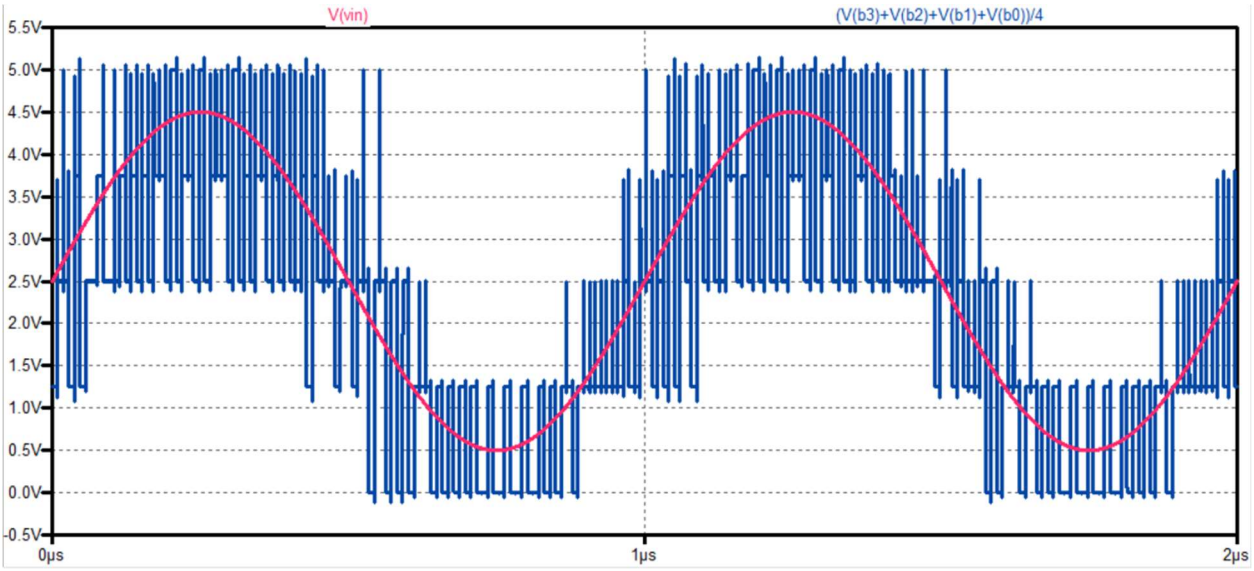

Figure 24: Simulation plot showing response to a 1-MHz, 2-V amplitude input sine wave applied to the second-order design

To filter the outputs of the modulators, the order of the digital filter (L) should be one more than the order of the modulator. Thus, for a 1st-order modulator we require a 2nd-order sinc filter and a 2nd-order modulator requires a 3rd-order sinc filter. For consistent comparison between the designs, two different bandwidths (B) of 6.25-MHz and 3.125-MHz were considered. In general, the bandwidth of the circuit is set by

$$B = \frac{f_s}{2 \cdot K_{avg}}$$

Since the oscillation frequency of the clock generator is approximately 100-MHz, K_{avg} is set to a value of 8 for a bandwidth of 6.25-MHz or a value of 16 for a bandwidth of 3.125-MHz. The variable K_{avg} corresponds to a sinc-shaped filter with the following transfer function,

$$|H(f)|^L = \left[\frac{1 - z^{-K_{avg}}}{1 - z^{-1}}\right]^L = [\,1 + z^{-1} + \cdots + z^{1-K_{avg}}\,]^L$$

Where the variable L stands for the order of the filter.

For the design featured in Figure 9.32, since the oscillation frequency is set to 220-MHz, the value of K_{avg} must approximately double to achieve the same bandwidths. Thus, a K_{avg} value of 16 yields a bandwidth of 6.25-MHz and a K_{avg} value of 32 yields a bandwidth of 3.125-MHz.

Ideal Signal-to-noise ratio

Before presenting the simulation results, an ideal value of the SNR is calculated to get a reference value for the simulated values of the SNR. The ideal signal-to-noise ratio can be calculated using the following equation

$$SNR_{ideal} = 6.02N + 1.76 - 5.17 + 30\log(OSR)$$

Since the modulator uses a one-bit ADC (the comparator), the value of N is equal to 1. The oversampling ratio is determined with the following expression

$$OSR = K_{path} \cdot K_{avg}$$

As seen by the equation above, the oversampling ratio is the product of the number of feedback paths and the number of samples that are being averaged. A table of the ideal SNR with varying oversampling ratios is provided in Table 1.

OSR	SNR_{ideal}	Units
32	47.8	dB
64	56.8	dB
128	65.8	dB
256	74.9	dB

Table 1: Ideal signal-to-noise ratios for various oversampling rates

Measured results

The results of the digital filtering are show for the two presented design in the following figures for both bandwidth specifications. Figure 25 shows the FFT view of the output of the modulator in both serial and parallel mode when the bandwidth of interest is 6.54-MHz. The green trace corresponds to the input sine wave at 1-MHz, the red circles correspond to the modulated noise within the bandwidth, and the blue trace corresponds to the modulated noise spectrum outside of the bandwidth of interest.

In serial mode the output of the modulator is taken as a steady 1-bit steam at the effective sampling frequency of approximately 840-MHz.

$$f_{eff} = K_{path} \cdot f_{sample}$$

In parallel mode the output of the modulator is taken as the sum of the individual outputs at the sampling frequency of 100-MHz. This additional addition introduces an additional filter which further attenuates the signal

using a smaller signal-to-noise ratio. The signal-to-noise ratio for this case is 37.8 dB for the serial mode and 34.1 dB for parallel mode.

A similar plot is shown in Figure 26 with the bandwidth reduced to 3.27-MHz. Because of the reduction in bandwidth, more of the modulated noise is filtered out producing a larger SNR. This time the SNR was 46.1 dB and 45.5 dB for serial and parallel mode respectively.

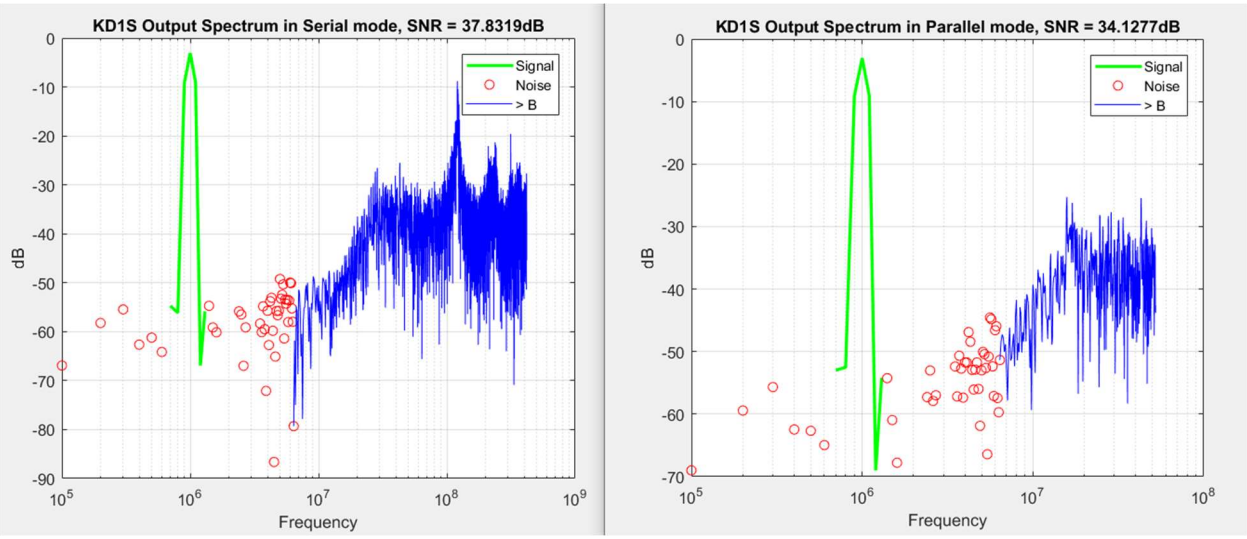

Figure 25: FFT plot of 1st-order, 8-path KD1S with bandwidth of 6.54-MHz

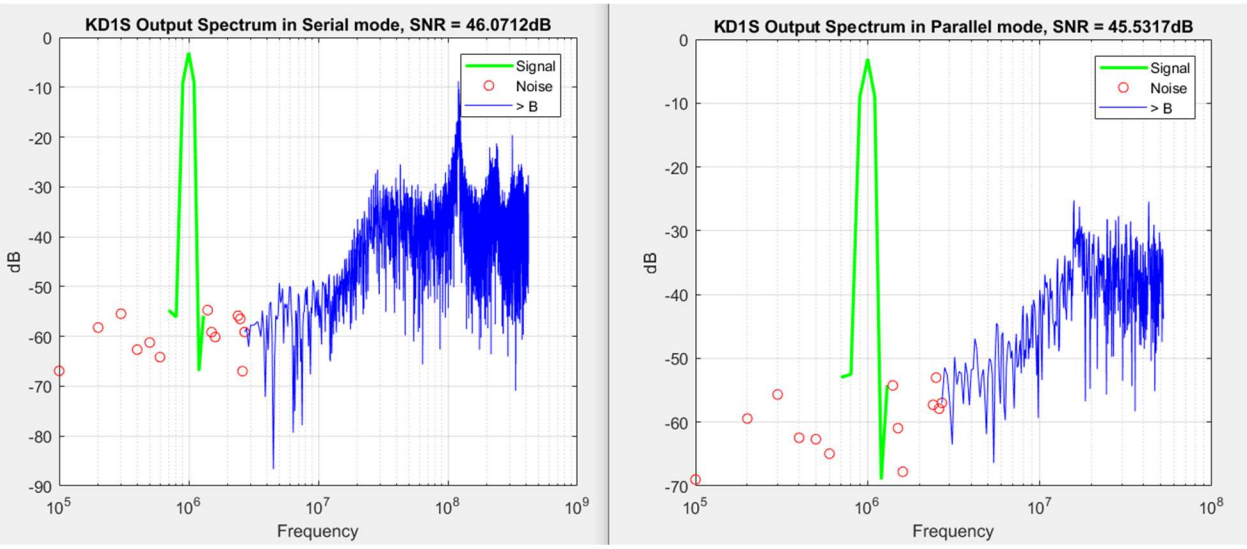

Figure 26: FFT plot of 1st-order, 8-path KD1S with bandwidth of 3.27-MHz

For the second design, since there is an additional integration that occurs, one should expect more noise-shaping to occur. The results of the simulation and digital filtering are shown in Figure 27. Once again, we have applied a 1-MHz sine wave with an amplitude of 2-V as seen by the green trace. The serial mode plot shows the

serial mode results with an effective sampling rate of 420-MHz and an SNR of 43-dB. This demonstrates how despite using a lower effective sampling rate the 2nd-order design with four paths performs better noise shaping than the 1st-order design with eight paths. In parallel mode the design still performs marginally better than the first design.

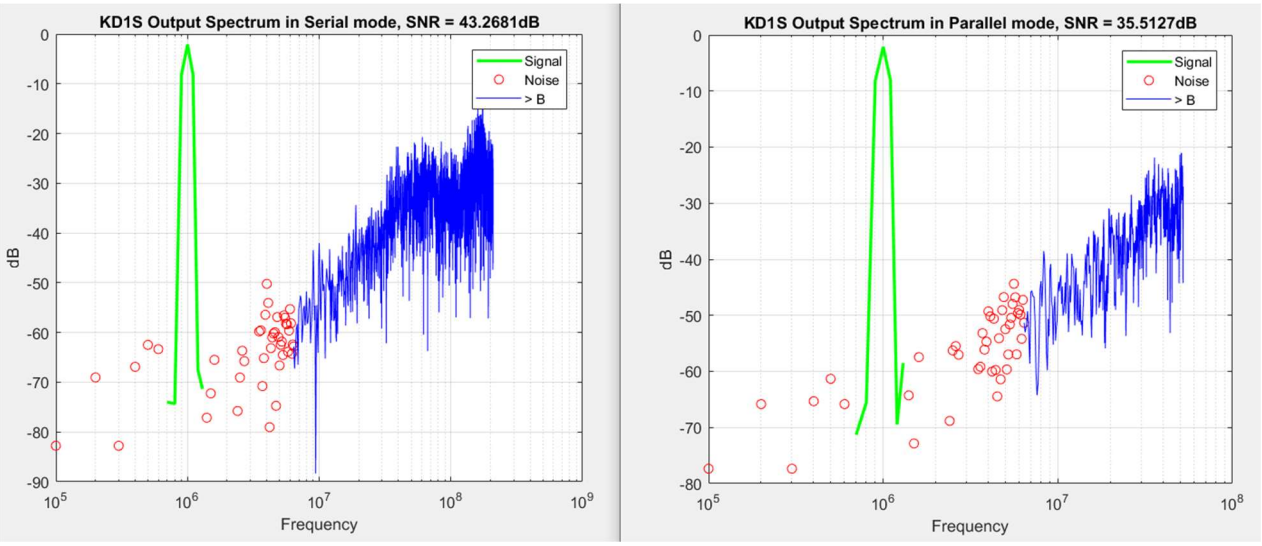

Figure 27: FFT plot of 2nd-order, 4-path KD1S with bandwidth of 6.54-MHz

When reducing the bandwidth to 3.27-MHz the second design again performs better than the first design as shown by the plots in Figure 28. In serial mode the 2nd-order design achieves an SNR of 55.5 dB at half the effective sampling rate of the 1st-order design. Likewise, in parallel mode the design achieves a higher SNR of 49.2 dB.

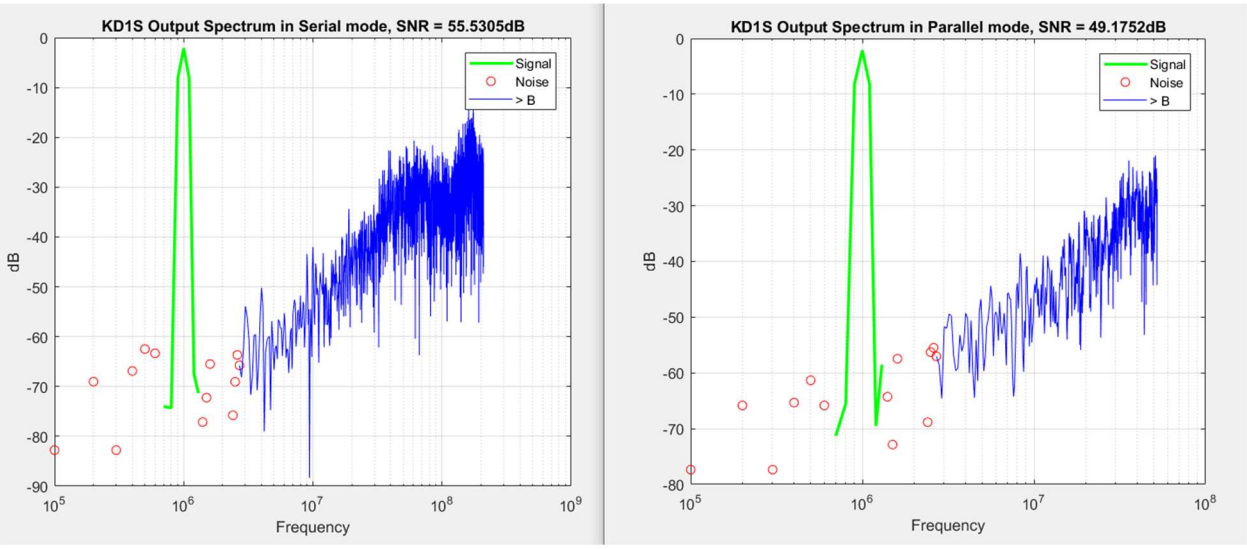

Figure 28: FFT plot of 2nd-order, 4-path KD1S with bandwidth of 3.27-MHz

1st-order, 8-path KD1S (K = 4, M = 2)					
	OSR = 64		OSR = 128		
Parameter	**Serial**	**Parallel**	**Serial**	**Parallel**	**Unit**
Fs,new	839	105	839	105	MHz
SNR	37.83	34.13	46.07	45.53	dB
Neff	5.99	5.37	7.36	7.27	Bits
BW	6.55	6.55	3.28	3.27	MHz
SNDR	36.65	33.17	41.62	40.18	dB
2nd-order, 4-path KD1S (K = 4, M = 2)					
	OSR = 32		OSR = 64		
Parameter	**Serial**	**Parallel**	**Serial**	**Parallel**	**Units**
Fs,new	419	105	419	105	MHz
SNR	43.27	35.51	55.53	49.18	dB
Neff	6.89	5.60	8.93	7.87	Bits
BW	6.55	6.54	3.27	3.27	MHz
SNDR	40.29	34.34	43.18	41.36	dB
1st-order, 8-path KD1S from Figure 9.32 (K = 8, M = 1)					
	OSR = 128		OSR = 256		
Parameter	**Serial**	**Parallel**	**Serial**	**Parallel**	**Units**
Fs,new	1830	228	1830	228	MHz
SNR	55.22	50.94	59.08	57.76	dB
Neff	8.88	8.17	9.52	9.30	Bits
BW	7.15	7.14	3.57	3.57	MHz
SNDR	41.8	41.28	59.08	57.76	dB

Table 2: Summary of results and comparison between designs

A summary of the results at the maximum sampling frequency is provided in Table 2. Additionally, the performance of the design featured in Figure 9.32 of the course textbook is provided for comparison. The design featured in Figure 9.32 exceeded the performance of both presented designs due to its significantly larger OSR.

Another comparison between the designs can be made with regards to average power consumption. This parameter is listed in Table 3 for the three designs of interest. Since the average dynamic power is a function of the operating frequency, the worst-case performances were listed which correspond to their highest operating frequency. As seen in the table, the first design presented in this report had the least amount of average power consumption. However, this topology also operated at about half the operating frequency of the design from Figure 9.32. The second proposed design had the largest power consumption as a result of the additional integrator needed for the 2nd-order modulation. Since the amplifier is the most power-hungry device, the impact of including one additional integrator has a significant impact on the power consumption.

Design	Average Dynamic Power (@f_{max})	Units
1st-order, 8-path KD1S	52.6 (@ 105-MHz)	mW
2nd-order, 4-path KD1S	69.7 (@ 105-MHz)	mW
Figure 9.32	65.6 (@ 220-MHz)	mW

Table 3: Comparison of average dynamic power consumption at maximum operating frequency

Conclusion

Two continuous-time KD1S modulator designs were proposed to replace a discrete time KD1S modulator from Figure 9.32. The designs had a much smaller sampling frequency than the design they were intended to replace. As a result, the bandwidths of the proposed designs were limited to 6.55-MHz or 3.27-MHz. When comparing the proposed designs to one another, the 2nd-order design performed much better noise shaping even with half the feedback paths and half the effective sampling frequency. This however came at the cost of additional power consumption. Future improvements to the designs include increasing the oscillation frequency of the clock generator to achieve larger bandwidths or to achieve larger SNR with the same bandwidths used in this report.