Overview on Analog phase-locked loop design

ECG721 Memory circuit design

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Outline

- What is a PLL?
- Applications
- Overview of APLL components
  - Phase detector
  - Loop filter
  - Voltage-controlled oscillator
- Closed-loop model of the PLL
- Design example

What is a phase-locked loop (PLL)?

- A PLL is a closed-loop feedback system that generates a periodic signal whose phase is synchronized to the phase of a periodic reference input.

  Some types of PLLs:

  All-digital PLL (ADPLL) - every component operates in digital domain

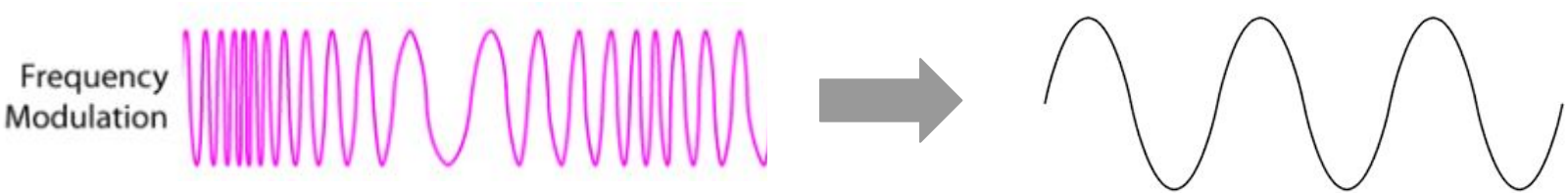
  Digital PLL (DPLL) - XOR or phase frequency detector used for phase detection. Clock divider may be used.

  Analog PLL (APLL) - Multiplier for phase detection, analog filter, analog VCO

Applications of PLLs

Applications include:

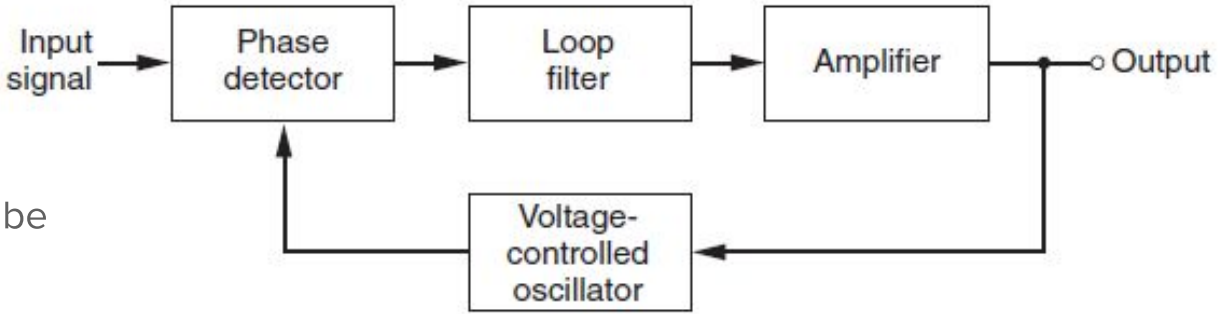
- FM signal demodulation
- Frequency synthesis
- Clock recovery
- Tone detection



Components of an PLL

The basic components of a PLL are:

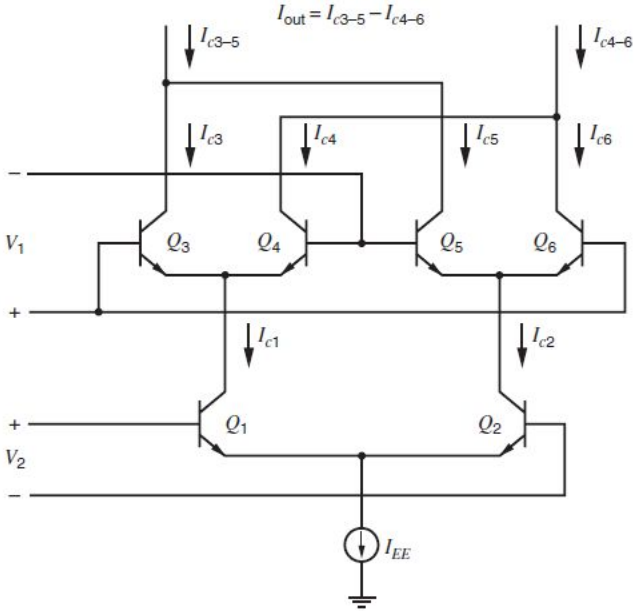
- Phase detector: outputs a voltage proportional to phase difference
- Loop filter: filters unwanted high frequency components
- Voltage controlled oscillator (VCO): outputs periodic signal proportional to input voltage
- Amplifier (optional)



** Depending on the application output may be the output of the VCO.

Phase detector: multiplier

- Output signal is proportional to the phase difference of its two periodic inputs
- Example: Gilbert multiplier cell or 4-quadrant multiplier



$$\Delta I = I_{c3-5} - I_{c4-6} = I_{c3} + I_{c5} - (I_{c6} + I_{c4})$$
$$= (I_{c3} - I_{c6}) - (I_{c4} - I_{c5})$$
$$= I_{EE}\left[\tanh\left(\frac{V_1}{2V_T}\right)\right]\left[\tanh\left(\frac{V_2}{2V_T}\right)\right]$$

- For small signal inputs (< 2Vt) linear multiplication of V1 and V2 is obtained
- For large signal voltages (> 2Vt) switch-like behavior occurs. The result is an **effective multiplication by a square wave**.

Phase detector: multiplier

Our interest is in operating with large-signal voltages.

Operating with small-signal inputs yields an output signal dependent on both the phase **and** amplitude of the inputs. (BAD!)

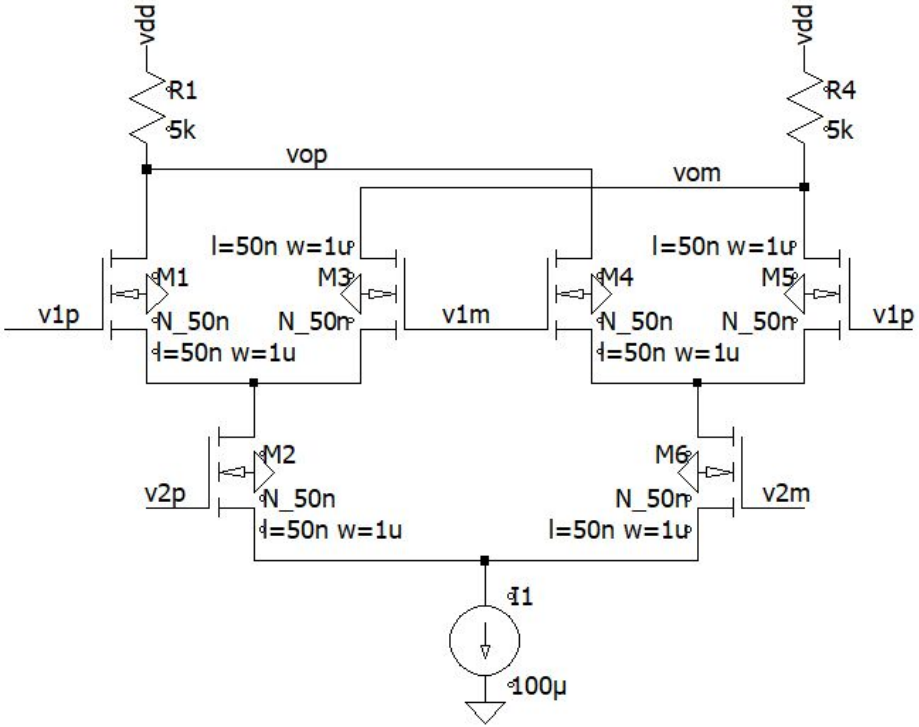
- An amplifier or limiter may remedy this by bringing the output signal to the rail voltages.

Phase detector: LTspice example

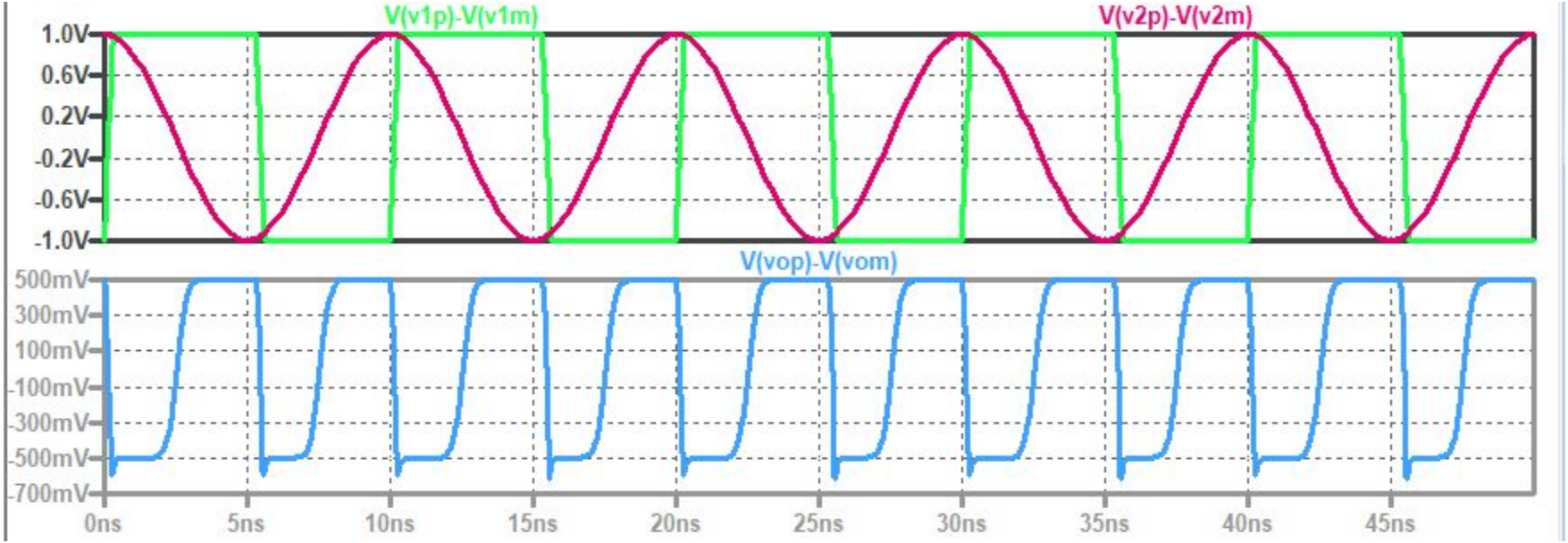
Multiplier circuit using NMOS devices

Inputs:
V1 = v1p - v1m
V2 = v2p - v1m

Output:
Vout = vop - vom

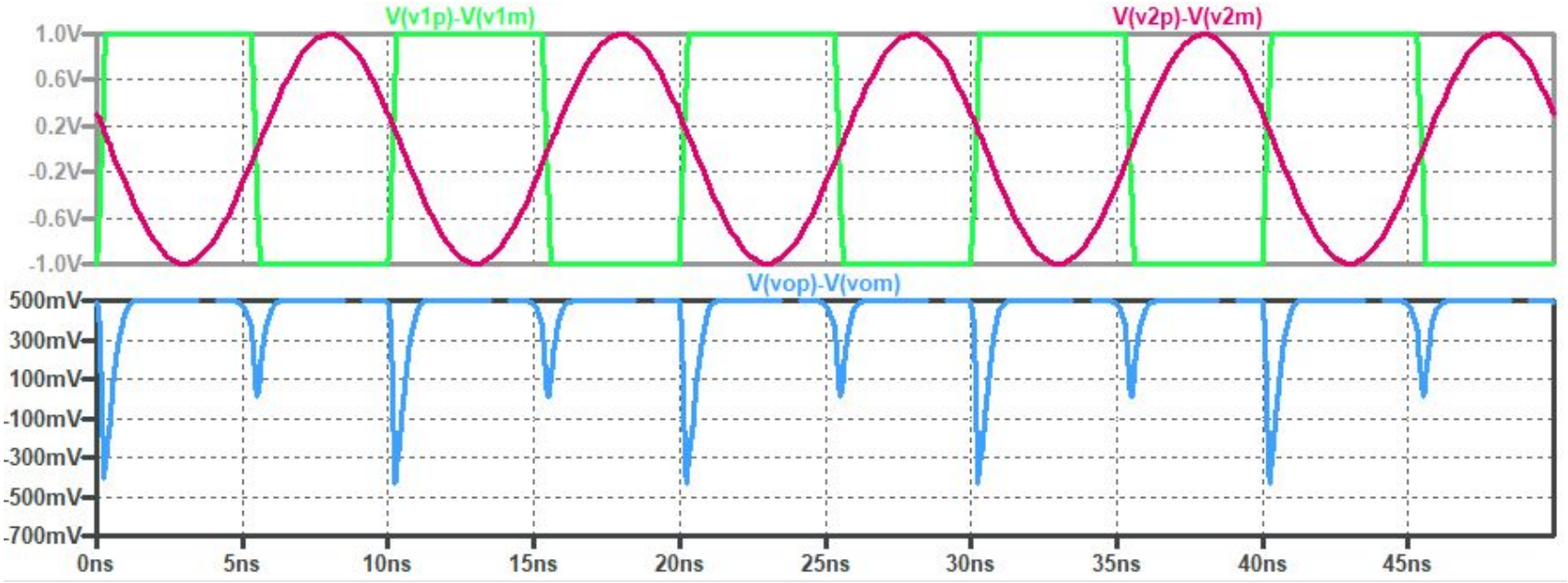


Phase detector example sim: φ = 0.5 π



Leading edge of sine wave is ahead in phase by 0.5 pi. The resulting output signal has a DC value of 0 V.

Phase detector example sim: φ = 0.9 π



Leading edge of sine wave is ahead in phase by 0.9 pi causing the output to have a positive DC value near 500 mV.

Phase detector example sim curve:

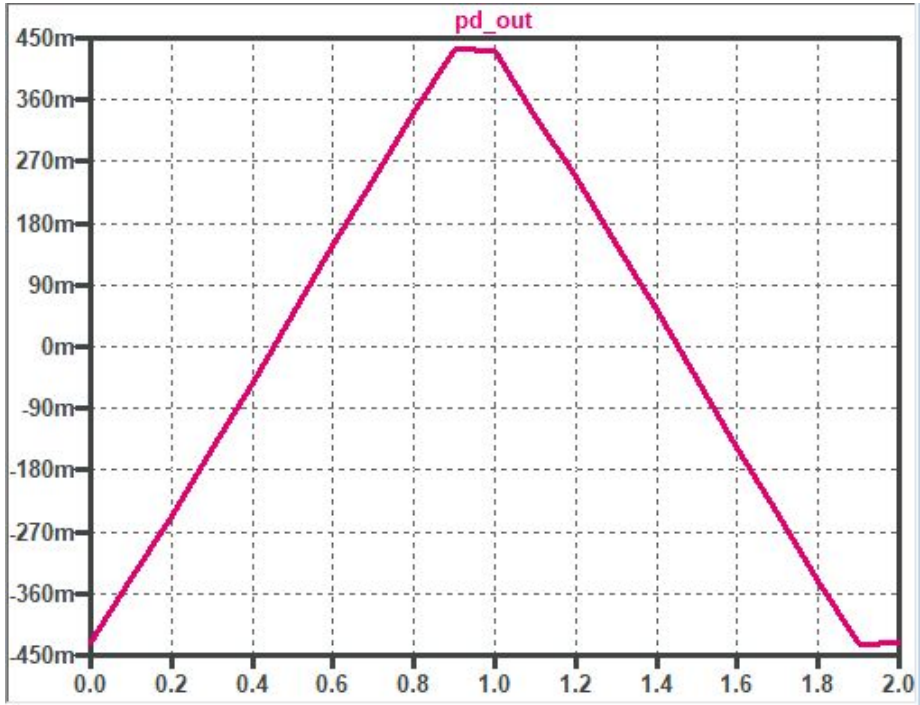
Characteristics curve of multiplier similar to the XOR gate used in a digital PLL

Max values set by the tail current and the load resistors

$$max(|V_{out,avg}|) = I_1 \cdot R_1 \approx 450\ mV$$

Gain of this phase detector:

$$K_D = \frac{0.45}{0.5\ \cdot \pi} = 0.29\ V/rad$$

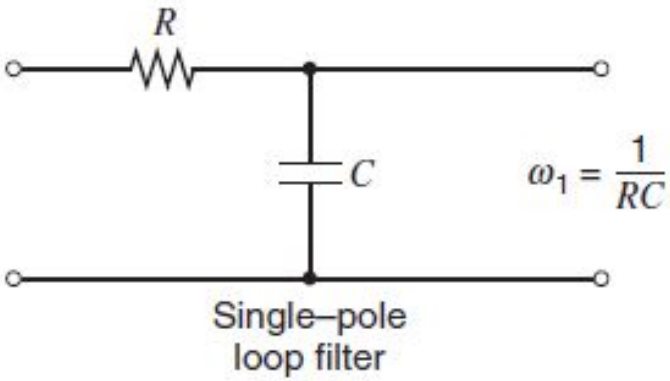


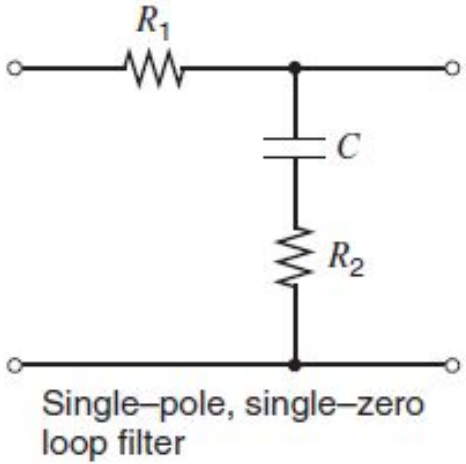
(x π radians)

Loop filter

- Filters out unwanted frequencies present at the output of the phase detector.
- Can provide memory in the case where the PLL unlocks for a moment.

Examples of loop filters:





What if the loop filter is omitted?

Multiple frequencies result from multiplication of time harmonic signals.

$$V_1 = A_1 cos(\omega_1 t) \qquad V_2 = A_2 cos(\omega_2 t + \phi)$$

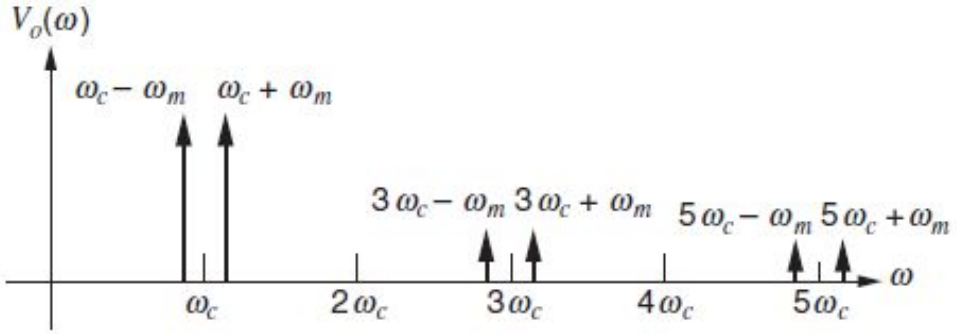
$$V_1 * V_2 = 0.5 A_1 A_2 \ [cos((\omega_1+\omega_2)t+\phi)+cos((\omega_2-\omega_1)t+\phi)]$$

** If the frequencies are the same,

$$V_1 * V_2 = 0.5\ A_1 A_2 \ [cos(2\,\omega\, t + \phi) + cos(\phi)]$$

Frequencies outside the bandwidth of interest appear on the VCO's input which may yield nonlinearities

What if the loop filter is omitted?



← Fourier series of a square wave carrier signal multiplied by an input message signal

- For square wave multiplication, additional frequency components are expected as described by the fourier series of a square wave.

Voltage-controlled oscillator

- Produces a periodic output with frequency proportional its input voltage.
- **Must remain oscillating when no input signal is applied.**
- Center frequency should be within bandwidth of interest
- VCO example on the right varies the delay between inverter stages by varying the current in each stage.

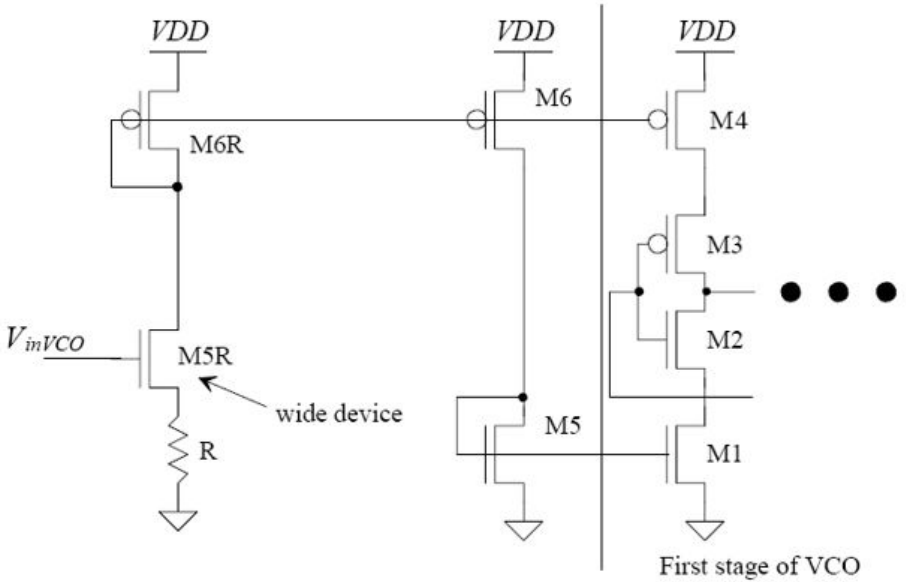


Figure 19.17 Linearizing the current in a current-starved VCO.

Voltage-controlled oscillator

- Other VCO topologies dissipate less power such as source-coupled multivibrators.

- Schmitt trigger based vibrator (right)

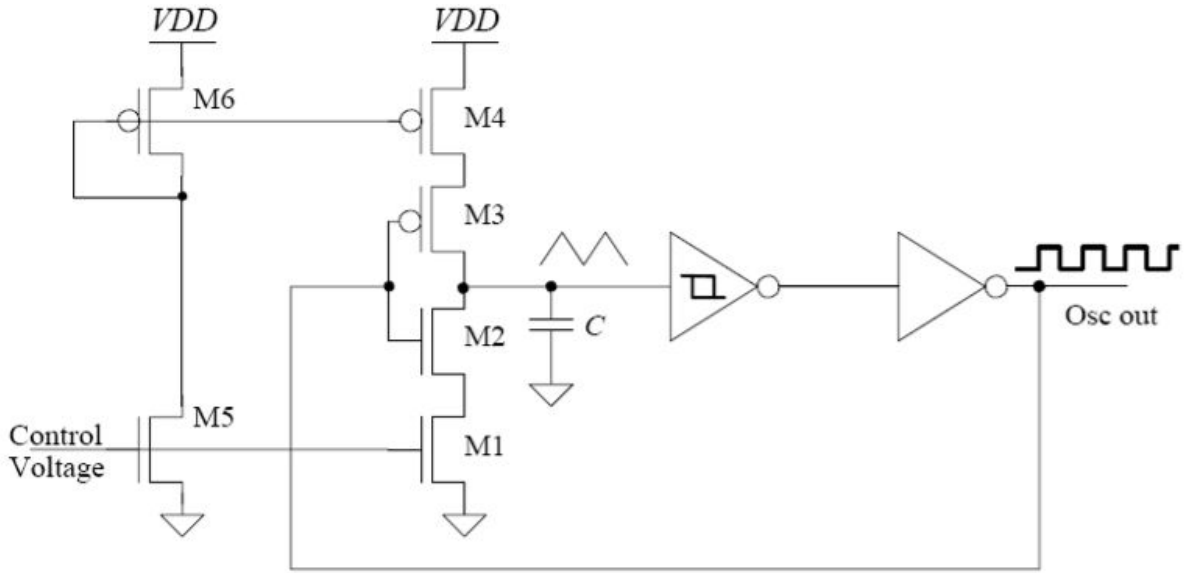
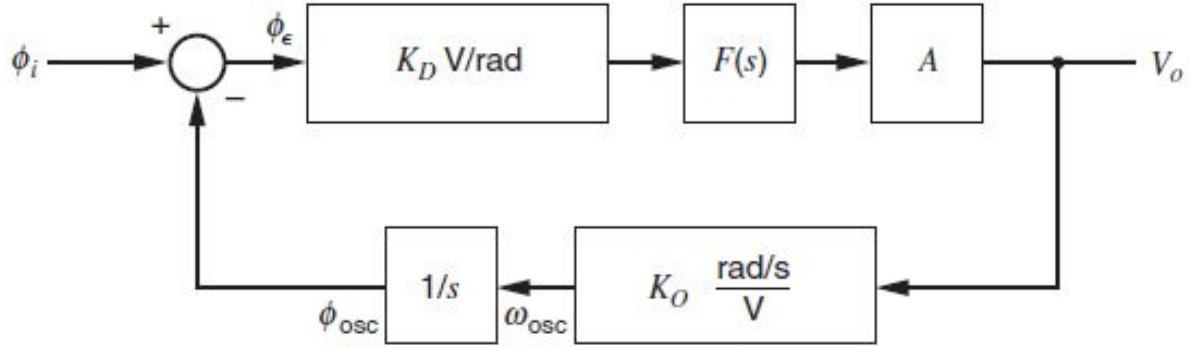


Figure 18.8 Voltage-controlled oscillator using Schmitt trigger and current sources. MOSFETs M2 and M3 are used as switches.

PLL block diagram model



- Kd is the gain of the phase detector
- F(s) is the transfer function of the loop filter
- A is the amplifier gain (optional)
- Ko is the gain of the oscillator
  ** note how the VCO frequency is integrated to get its phase. This is inherent to the PLL and not a physical component.

PLL - 1st order system (no loop filter)

The closed loop transfer function of the PLL is,

$$\frac{V_o}{\omega_i} = \frac{1}{s}\frac{V_o}{\phi_i} = \frac{K_D F(s) A}{s + K_D K_O A F(s)}$$ where $\omega_i(s) = s\,\phi_i(s)$

ωi: frequency modulating the input signal

If the loop filter is omitted (F(s) = 1), the PLL has a single pole response with bandwidth equal to the product of KD, K0, and A

$$\frac{V_0}{\omega_i} = \frac{1}{K_0}\;\frac{1}{1+s\,\frac{1}{K_D\,K_O\,A}}$$

$$K_V = K_D K_O A$$

** Kv: loop gain

PLL - 2nd order system

Including a simple RC low pass filter as the loop filter makes the PLL a second-order system

$$\frac{V_o}{\omega_i} = \frac{1}{s}\frac{V_o}{\phi_i} = \frac{K_D F(s) A}{s + K_D K_O A F(s)}$$

where $F(s) = \frac{1}{1+s\frac{1}{\omega_1}}$ Loop filter transfer function

$$\frac{V_o}{\omega_1}(s) = \frac{1}{K_O}\left(\frac{1}{1 + \frac{s}{K_v} + \frac{s^2}{\omega_1 K_v}}\right)$$

$$\omega_n = \sqrt{K_v \omega_1}$$

$$\zeta = \frac{1}{2}\sqrt{\frac{\omega_1}{K_v}}$$

Analyzing the PLL's open-loop response

Open-loop response of PLL can provide intuition into the stability of the closed-loop response

Phase margin: measured as the amount of phase shift away from 180 degrees when the gain is unity

- larger phase margins are safer from instability

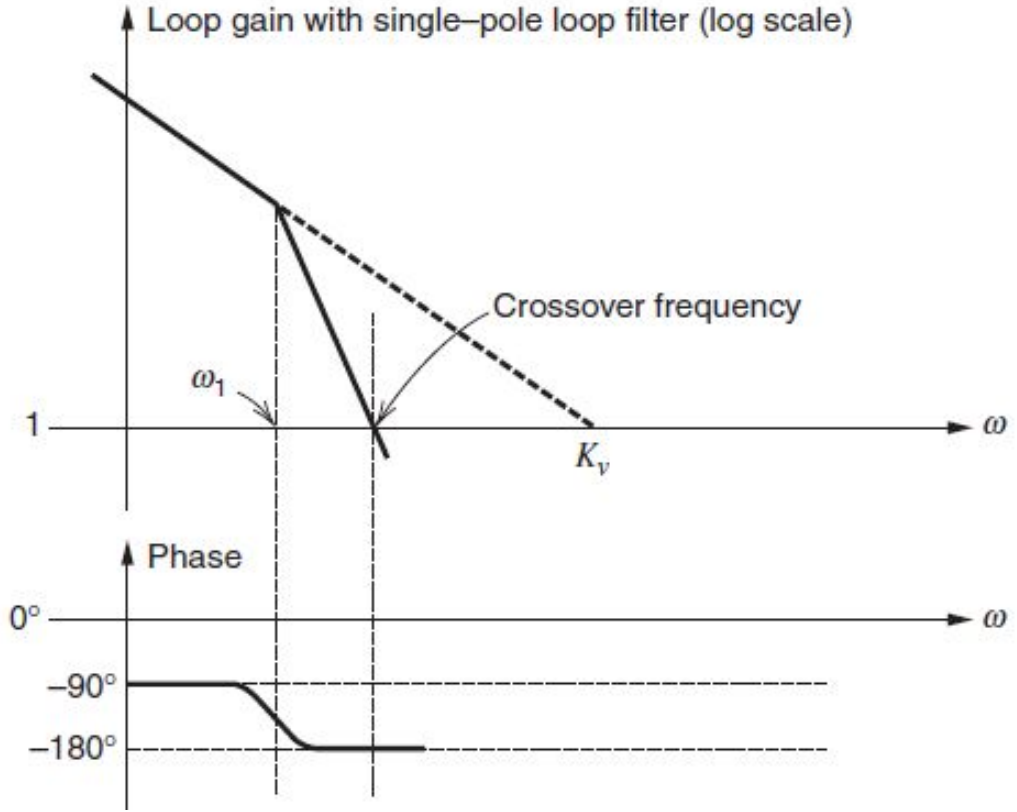
We consider the open-loop response with two types of loop filters

- Single-pole filter
- Single-pole single-zero filter

Open-loop response: single-pole filter

$$P_{OL}(s) = \frac{K_V}{s\,(1+\frac{s}{\omega_1})}$$

- Phase margin is near zero
- Causes peaks in the transient response (underdamped response)



Open-loop response: single-pole filter

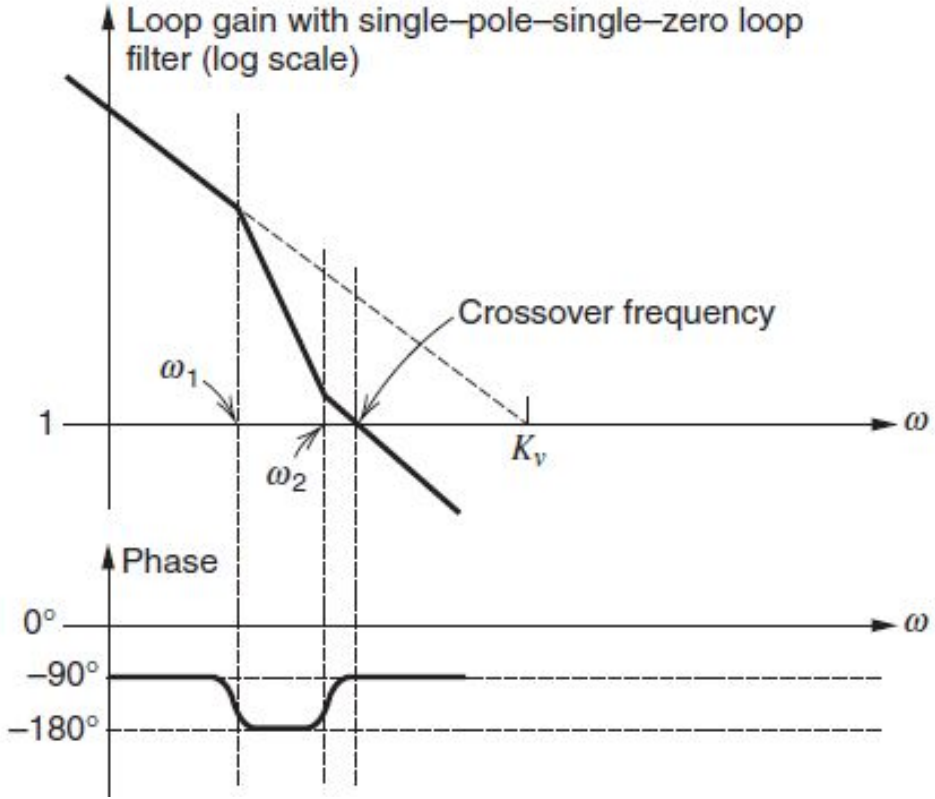
Drawbacks:

- If Loop filter bandwidth is increased (ω1 moves closer to Kv), more out-of-band signals are present at the input of the VCO.
- If loop gain is decreased (Kv), the frequency lock range is decreased. Greater demand on VCO design to have precise operating frequency range if VCO gain is decreased.

****Lock range:** range of frequencies with which the PLL will maintain lock

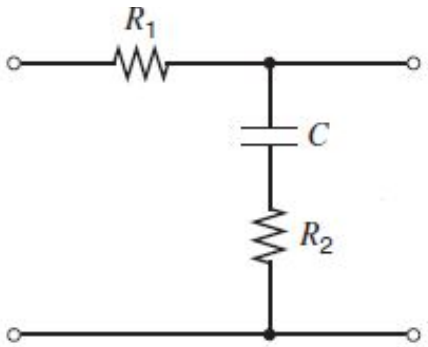
Open-loop response: single-pole single-zero filter

- Inclusion of zero improves phase margin
- More stable transient responses
- Bandwidth of loop filter (= unity gain frequency) reduced while maintaining similar loop gain Kv



Loop filter design equations

Single-pole single-zero

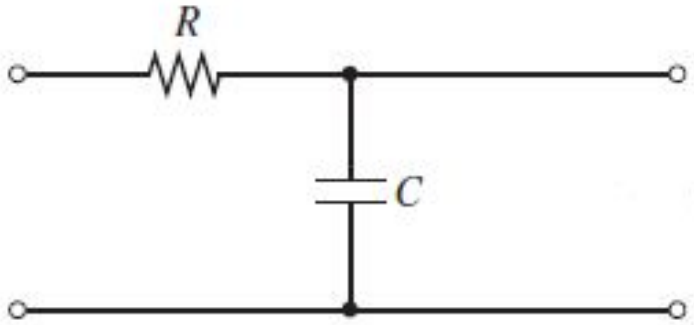


$$F(s) = \left(\frac{1 + \frac{s}{\omega_2}}{1 + \frac{s}{\omega_1}} \right)$$

$$\omega_2 = \frac{1}{CR_2}$$

$$\omega_1 = \frac{1}{C(R_1 + R_2)}$$

Single-pole



$$F(s) = \frac{1}{1 + \frac{s}{\omega_1}} \qquad \omega_1 = \frac{1}{RC}$$

Design example

A PLL is assembled using the multiplier phase detector, a single-pole single-zero loop filter, and a current-starved VCO (fig. 19.18 in the CMOS textbook) with center frequency at 100 MHz.

$$K_V = K_D K_O = (0.29\ V/rad)(1.57 \times 10^9\ rad/V \cdot s)$$ Loop gain

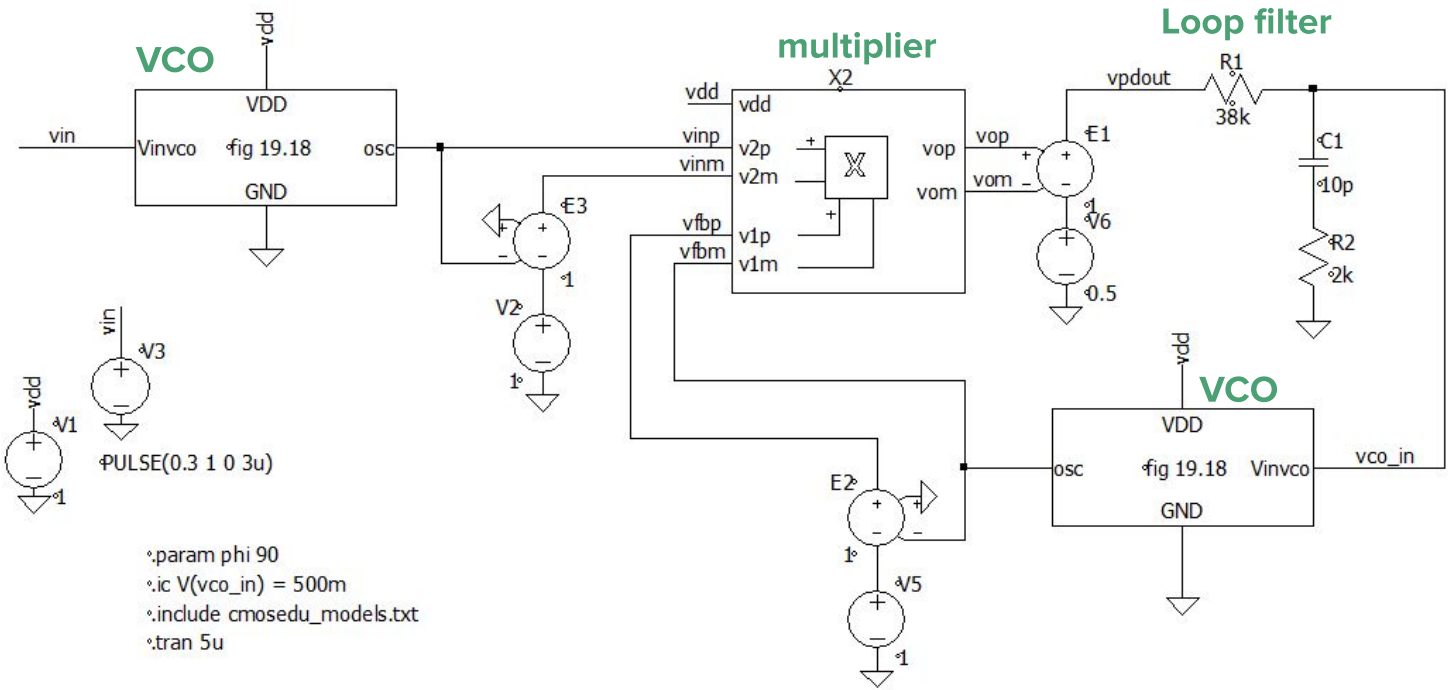
The pole and zero of the loop filter were chosen to be,

$$\omega_1 = \frac{1}{400\ ns} \qquad \omega_2 = \frac{1}{20\ ns}$$

Component values:

$$R_1 = 38k\Omega, \quad R_2 = 2k\omega, \quad C = 10pF$$

Design example: FM demodulator



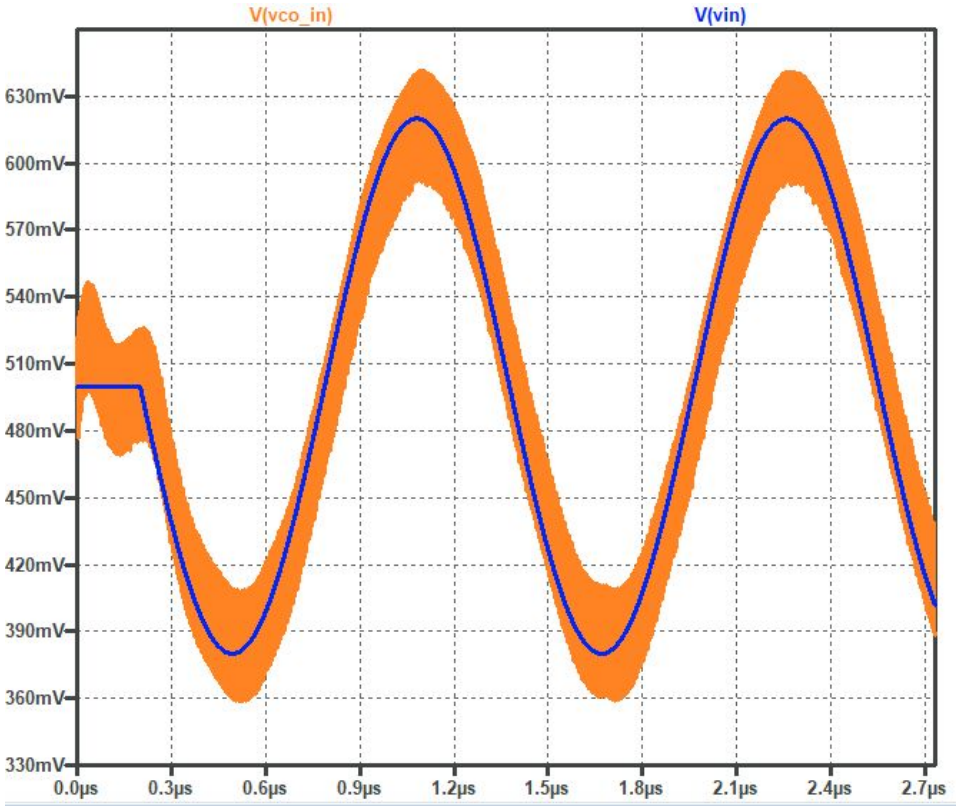
An FM signal with center frequency at 100 MHz is fed into the PLL. The PLL is expected to demodulate the FM signal and output its message signal at the loop filter output V(vco_in).

Design example: FM demodulator

V(vco_in): VCO control voltage. Shows the demodulated message signal. (orange trace)

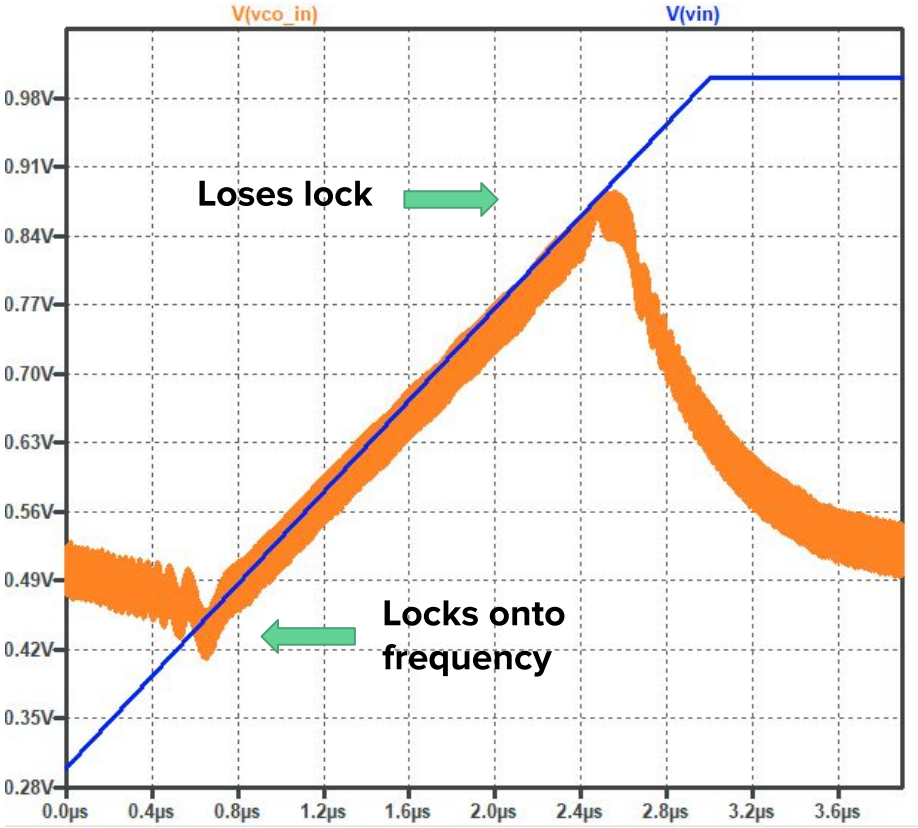
V(vin): original message signal. (blue trace)

PLL output accurately follows the message signal within the FM input signal.



Design example: capture range and lock range sim

- Frequency of input is ramped from 75 MHz to 150 MHz to demonstrate the PLL's capture and lock range
- Locks on at about 80 MHz and holds lock until 150 MHz.
- Lock range roughly spans the linear range of VCO operating frequencies



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