# APD Analog front-end

Using ON Semiconductor's C5 process
ECG 720 Advanced analog IC design (Fall 2019)
Course project
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Using the ON C5 process, two transimpedance amplifiers (TIA) front ends are designed to be used with an avalanche photodiode (APD) to process the APD's current signal and convert it into a voltage. The target specifications are summarized in Table 1. Design efforts and considerations taken in achieving these specs are detailed below as well as discussion on drawbacks and benefits of both designs.

| **Summary of results** | | | | |
|---|---|---|---|---|
| **Parameter** | **Target specifications** | **2-stage design** | **1-stage design** | **Units** |
| Supply voltage | 3 or 5 | 5 | 5 | V |
| Current draw | < 5 | 4.165 | 1.63 | mA |
| 1st stage gain | 30 (89.5) | 37.4 (91.46) | 316 (110) | kΩ (dB) |
| 2nd stage gain | 10 - 20 (20 - 26) | 14.96 (23.96) | na | V/V (dB) |
| Total gain | 300 - 600 (109.5 - 115.5) | 462 (113.3) ** | 316 (110) | kΩ (dB) |
| TIA bandwidth (1 pF load) | > 250 | 56.2 | 140 | MHz |
| Input-referred noise | < 5 | < 3.6 | 1.12 (with 100fF)<br>4.36 (with 400 fF) | pA/sqrt(Hz) |
| Output swing | 1.5 - 2 | 2 | 2 | V |
| Slew rate (1 pF load) | > 100 | 116 - 720 (charging)<br>111 - 400 (discharging) | 500 (charging)<br>800 (discharging) | V/µs |

Table 1: quick reference table summarizing results of designs.
** total gain includes two common-drain amplifiers used between the two stages.

**Note on device parameters**

Given the target bandwidth specification, device sizes and biasing were selected to facilitate high speed operation. This entailed using minimum length devices (L=600 nm) and high overdrive voltage (10% of supply voltage). Detailed estimates of device parameters are listed in Table 2 at the end of this document.

## TIA1 design

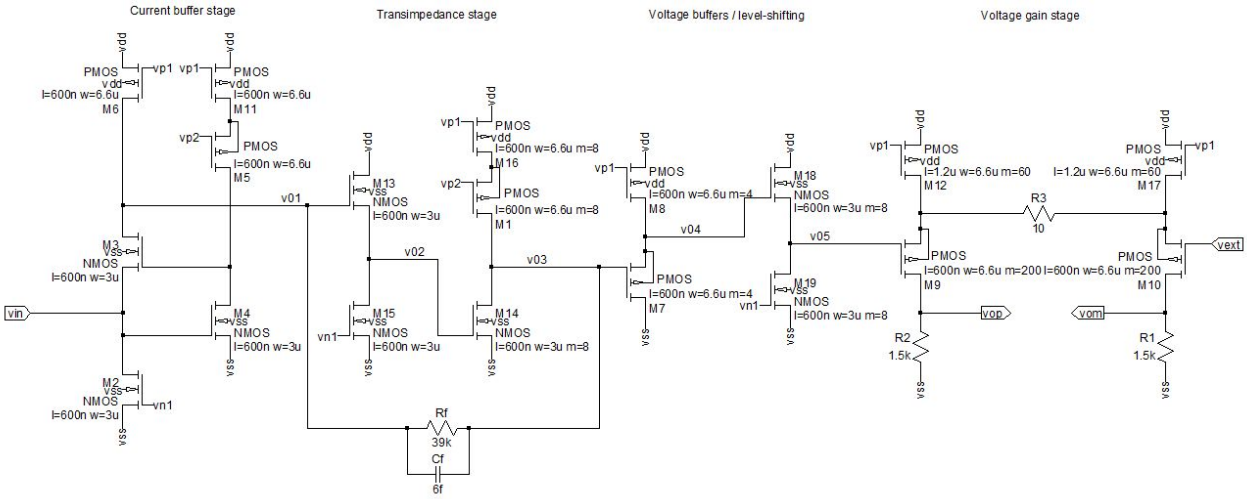


Figure 1: Schematic of first APD front end

Figure 1 shows the design of the first TIA. It consists of four subcircuits which include a current buffer, transimpedance stage, source-followers, and a final voltage gain stage. Since the bandwidth of the TIA that processes the APD's output current is dependent on the parasitic capacitance at the input of the amplifier, a regulated gate cascode (RGC) current buffer is used at the input to reduce the effects of the parasitic capacitance on the TIA. The RGC configuration allows for a substantial decrease in the input impedance seen by the APD. Figure 2 shows the standalone regulated cascode RGC topology used before the TIA stage.

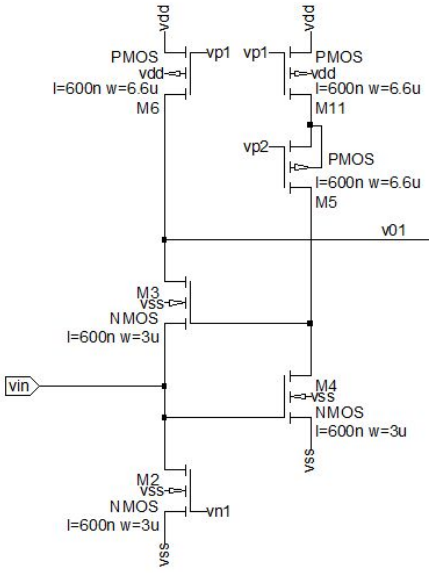


Figure 2: Regulated cascode (RGC) current buffer

Because of the local feedback within the RGC input stage, the transconductance of the input device is increased. This results in an input impedance that is the inverse of this new transconductance.

$$Z_{in} = 1 / [\, g_{mn3} (1 + g_{mn4} R_{ocasn}) \,]$$

Where $g_{mn3}$ is the transconductance of the input common-base device M3 and the product $g_{mn3} R_{ocasn}$ is the gain of the local common-source amplifier. Using the approximated values from table 2, the following is obtained,

$$Z_{in} \approx (\, 215e-06 \,)^{-1} (1 + [\, 215e-06 \,][\, 3.6e+06 \,])^{-1} = 6\ \Omega$$

To verify these calculations, an AC simulation is performed with the following schematic,

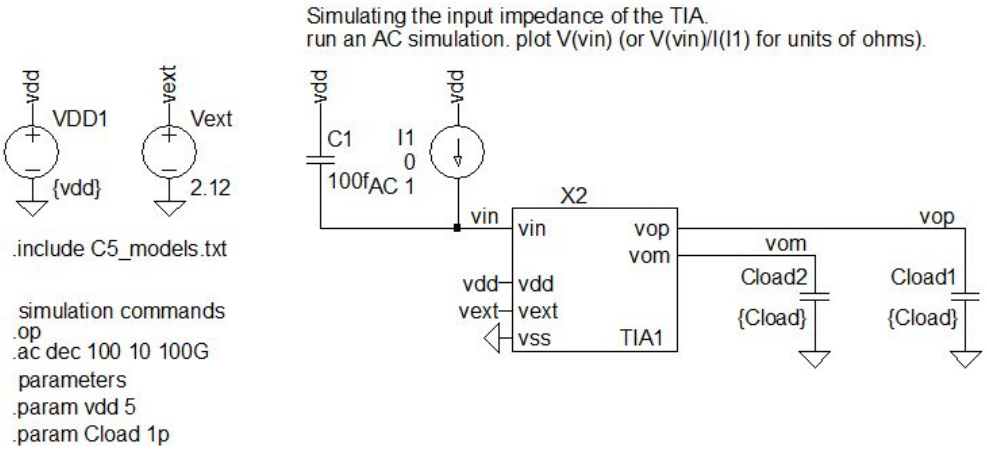


Figure 3: schematic used to simulate the input impedance of TIA1.

Simulating the input impedance of the amplifier yields the following plot,

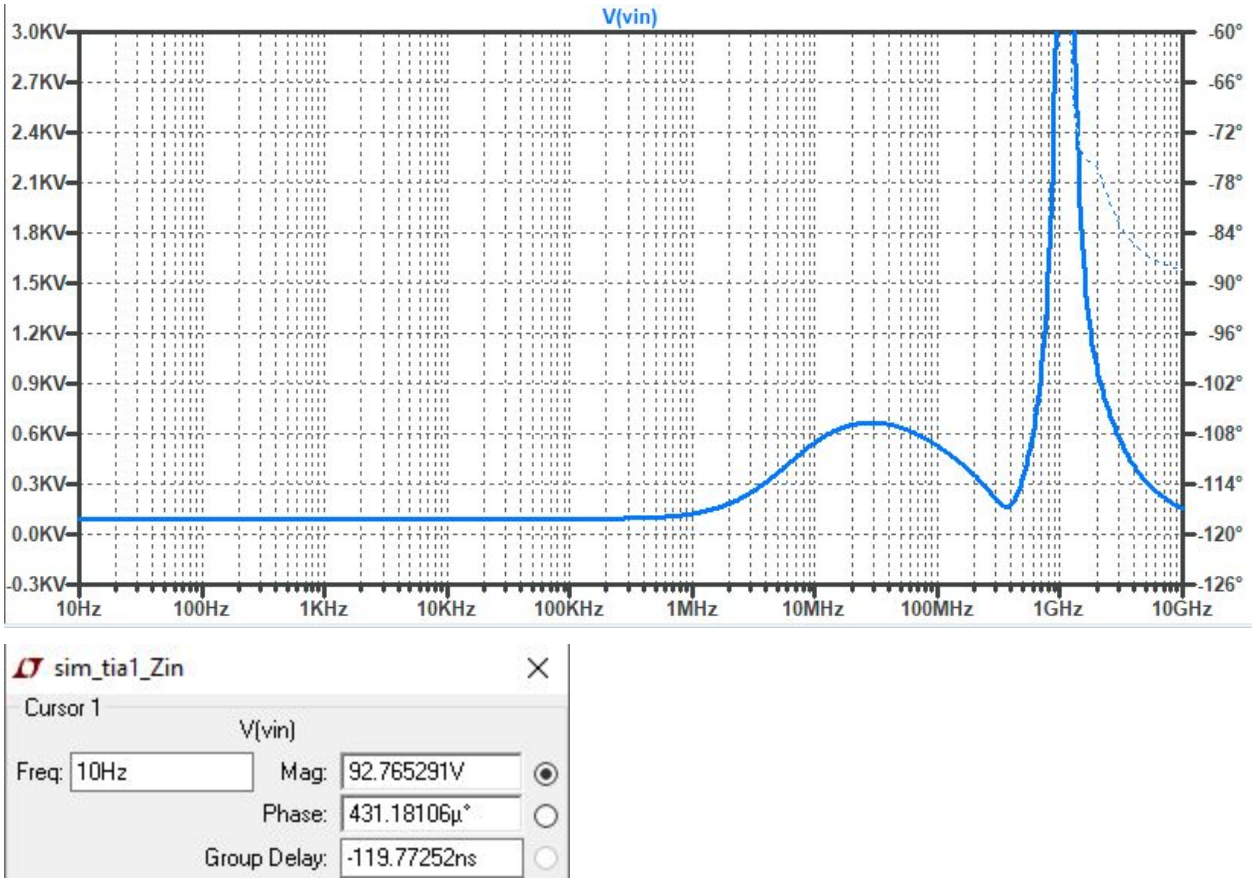


Figure 4: Simulation results of the input impedance of TIA design 1 and the cursor window showing the DC input impedance.

From Figure 4 above, the input impedance of the TIA with the RGC current buffer at DC is about 93 Ω. Within the 250 MHz bandwidth the input impedance never goes above about 670 Ω.

Following the current buffer is the first amplification stage shown below in Figure 5. This shunt-shunt transimpedance amplifier consists of a common-drain (CD) input stage followed by a common-source (CS) amplifying stage. The CD stage serves to step down the voltage from the previous stage so that the CS stage can be properly biased in the saturation region. To increase the open-loop gain of the TIA, cascode PMOS current sources are used to set the bias current and increase the output resistance. Additionally the transconductance is increased by using multiple devices in parallel.

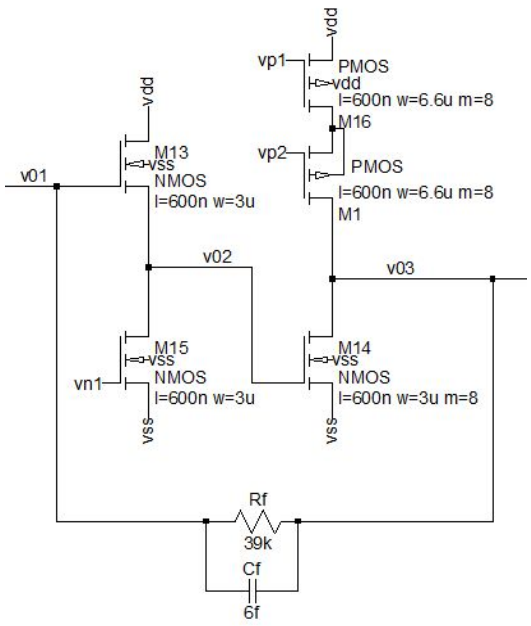


Figure 5: schematic of shunt-shunt transimpedance amplifier.

The open-loop gain of the transimpedance amplifier is given by the following,

$$A_{OL} = V_{out} / I_{in} = A_{CD} * A_{CS} \approx -g'_{mn}(R'_{ocasp} || R'_{on} || R_F)\, R_F = -g'_{mn}\,(R'_{on} R_F{}^2) / (R'_{on} + R_F)$$
$$A_{OL} = -g_{mn}\, R_{on}\, R_F{}^2 / (R'_{on} + R_F)$$

Where we assume the gain of the source-follower ($A_{CD}$) is one and the values $g'_{mn}$ and $R'_{on}$ are eight times greater and less than the values in the device parameter table respectively. The factor of eight is cancelled out in the numerator of the expression. Using the approximated values the open-loop gain is,

$$A_{OL} \approx -(40.85)(39K)^2 / (0.125 * [190K] + [39K]) = -990\ K\Omega$$

Using this the closed-loop gain is calculated as,

$$A_{CL} = -990K / (1 + (-1/39K)(-990K)) = 37.5\ K\Omega$$

Where the feedback resistor is selected to be 39 kΩ. The choice for such a gain comes from the fact that two source-follower stages follow the transimpedance stage. Since the source-followers will attenuate the gaina slightly larger gain is chosen for the TIA.

Performing an AC simulation of the TIA stage yields the following results,

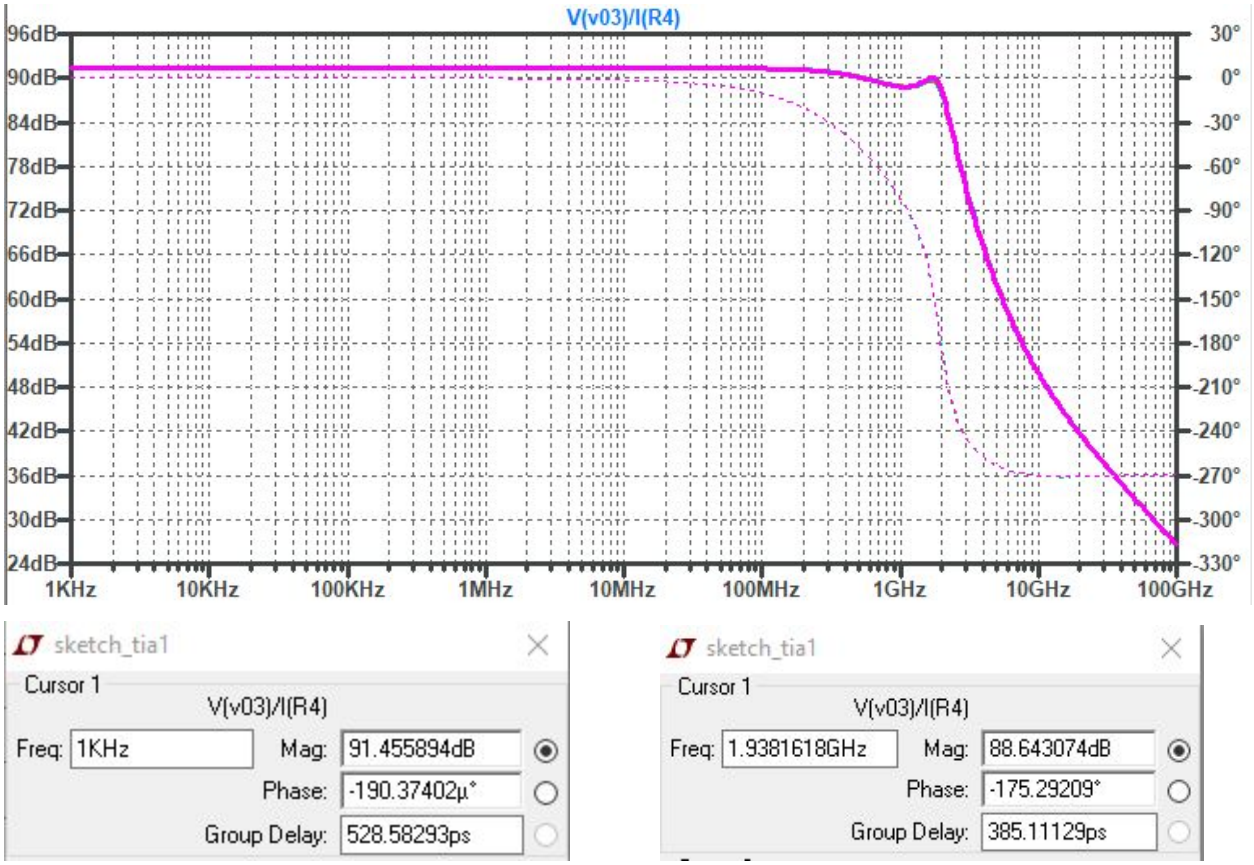


Figure 6: Simulation results of the gain of the TIA stage.

From Figure 6 we can see that the TIA stage has a DC gain of 91.46 dB which is equivalent to a gain of 37.4 KΩ. The -3 dB frequency is shown to be approximately 1.9 GHz. The peaking in the frequency response in this range of frequencies is responsible for the high -3 dB frequency.

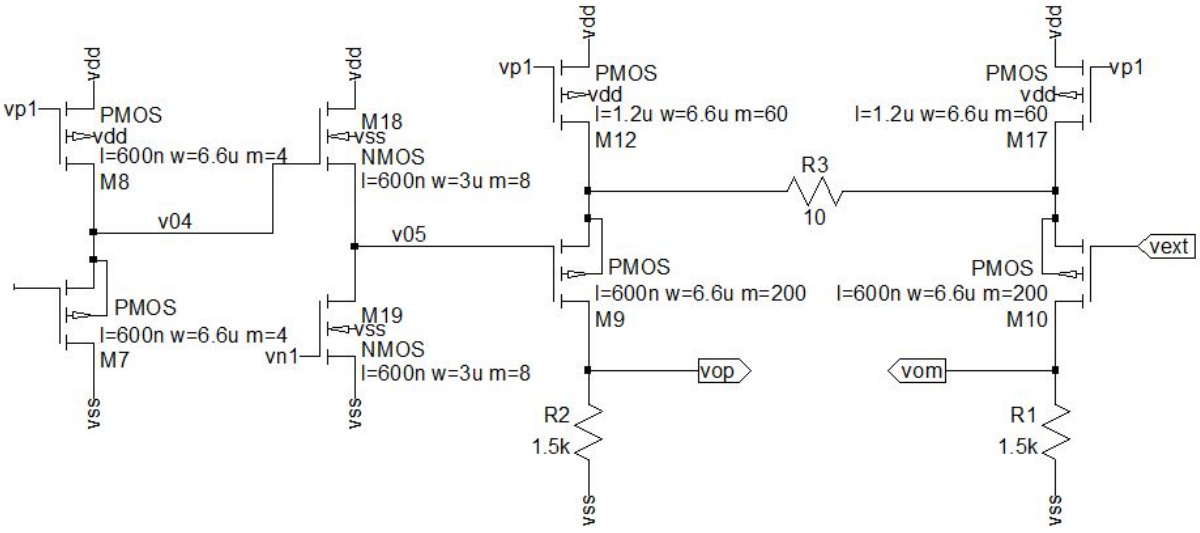


Figure 7: Two source-follower amplifiers followed by a differential amplifier with source degeneration.

As was previously mentioned, two source-followers are implemented after the TIA stage. These are shown in figure 7. They serve the function of driving the large input capacitance of the PMOS input device as well as level-shifting the output of the TIA twice so that it can remain within the input range of the differential amplifier.

Also shown in figure 7 is the second stage voltage amplifier. It consists of a differential amplifier with source degeneration. To avoid any reduction in output swing the two source resistors are combined and placed between the two PMOS current sources. Additionally, the output of the amplifier is taken differentially between the two outputs to allow for a larger output voltage swing. The goal of this stage was to design a final output stage amplifier that utilized negative feedback such that the gain could be set by a ratio of two resistors. The first concern regarding this design choice is that in order for the differential gain to be set by the two resistances, the transconductances of the differential pair must be significantly smaller than the source resistors as shown by the following equations,

$$|A_{DIFF}| = |(V_{op} - V_{on}) / (V_{ip} - V_{in})| = R_D / (R_S + 1/g_{mp})$$
$$|A_{DIFF}| = R_D / R_S \; ; for \; Rs >> 1/g_{mp}$$

The second concern is that in order for this amplifier to be the final stage, it has to be able to drive the 1 pF capacitive load at the target bandwidth. This means most of the allowable current consumption would be expended in this stage which means smaller drain and source resistors would have to be used. The smaller source resistors place a larger burden on the increase in transconductance of the PMOS diff-pair. Because of this, a large number of PMOS transistors are placed in parallel in an attempt to meet the requirement for a linear gain.

Using the gain equations and substituting the respective parameters the gain of the amplifier is roughly estimated to be,

$$A_{DIFF} \approx 1.5K / [\, 5 + (200 * 250 \; \mu A/V)^{-1} \,] = 1.5K / 25 = 60 \; V/V$$

The above equation over estimates the transconductances as will be shown by the following AC simulation results.

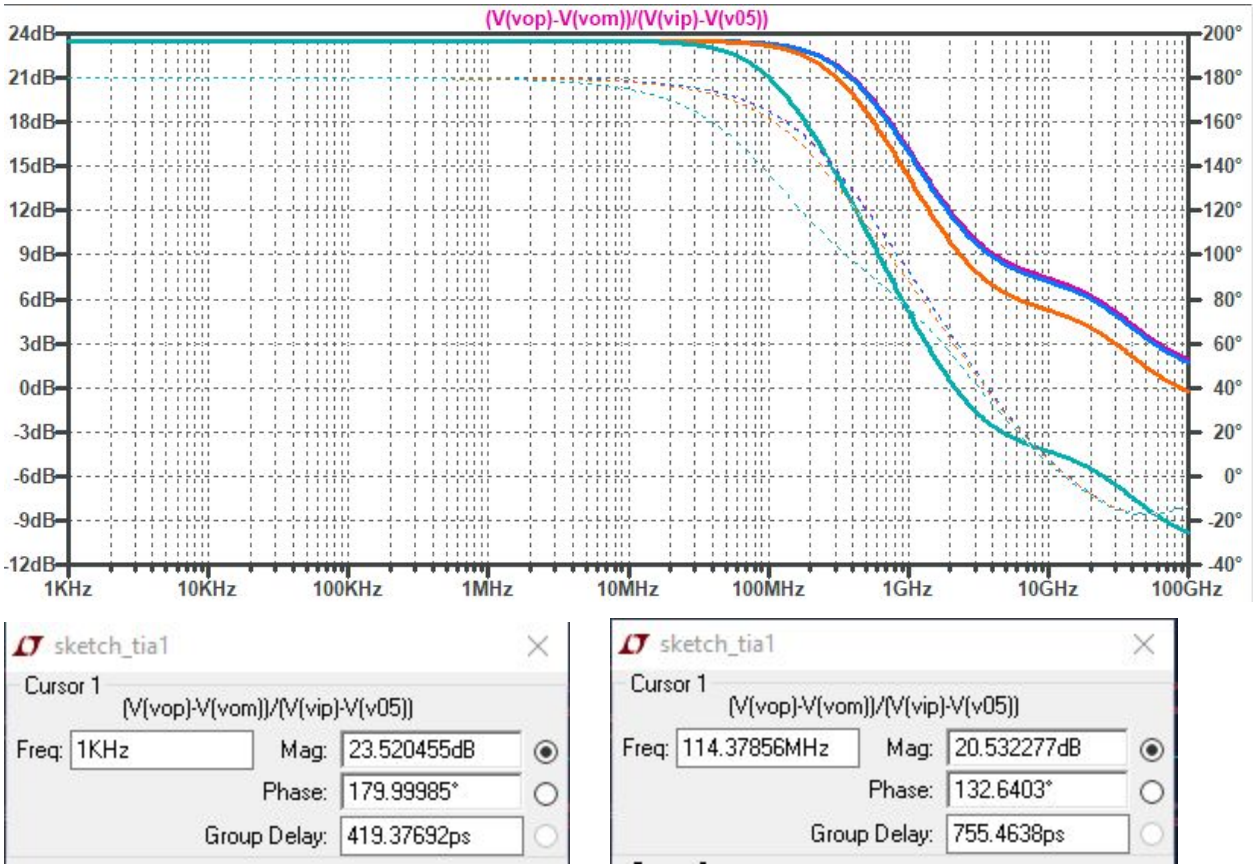


Figure 8: simulation results for the gain of only the differential amplifier with source-degeneration. Load capacitance is varied from 1 fF to 1 pF by 1 step per decade. The red trace corresponds to a load of 1 fF while the green trace corresponds to a load of 1 pF.

The plot in Figure 8 shows that the actual gain is closer to 23.5 dB (14.96 v/v). Also shown is the performance of the amplifier with varying load capacitance. With a -3 dB frequency of 114 MHz, the differential amplifier fails to meet the bandwidth specifications with a 1 pF load.

In order to utilize the amplifier, the second input terminal would have to be biased around the switching point by the user prior to detecting any light from an APD. This was seen as a more versatile option for a DC-coupled voltage amplifier as opposed to using a series-shunt amplifier where the input range would be limited to less than 500 mV or 250 mV depending on if the closed-loop gain is 10 or 20 V/V. In this case process variations and mismatches between devices during manufacturing could knock the input out of the ideal range of the voltage amplifier and reduce the output swing or in the worst case render the entire amplifier useless.

**Simulations:**

**Small signal response**

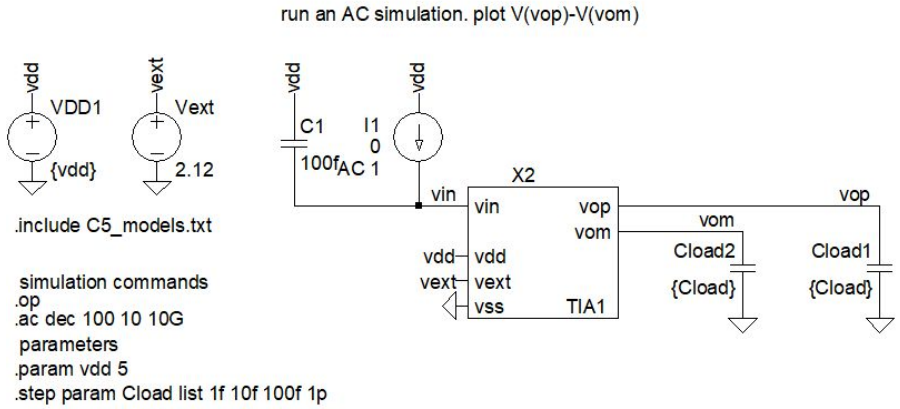


Figure 9: schematic used to generate the small signal response of TIA1. A 100 fF capacitance is added in parallel to the current source to model the APDs parasitic capacitance.

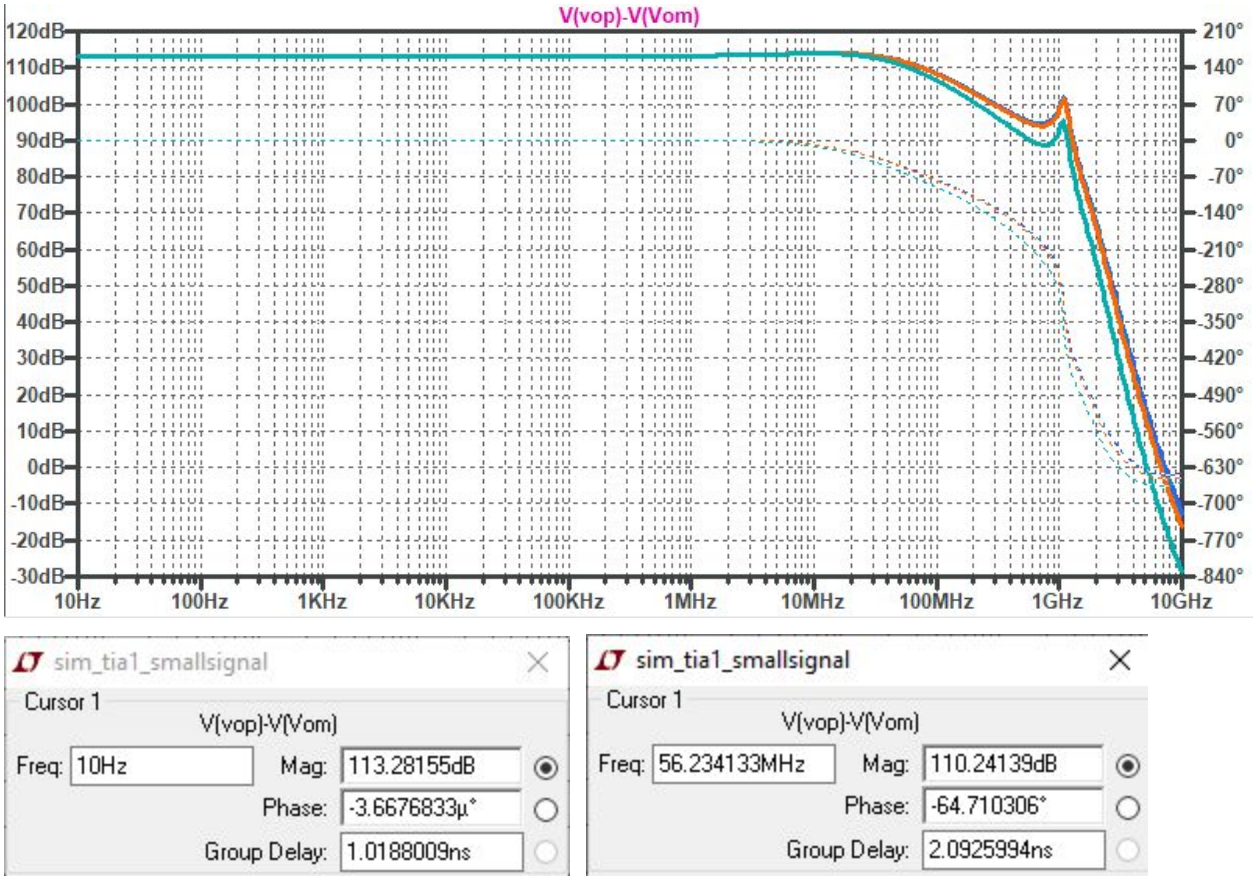


Figure 10: plot of AC simulation results of the TIA design 1. Load capacitance is varied from 1 fF to 1 pF by 1 step per decade. The pink trace corresponds to a 1 fF load while the green trace corresponds to the 1 pF load. The cursor boxes show a total DC gain of 113.3 dB and a -3 dB frequency of 56.2 MHz at a load of 1 pF. The design fails to reach the bandwidth requirement.

## Large signal response

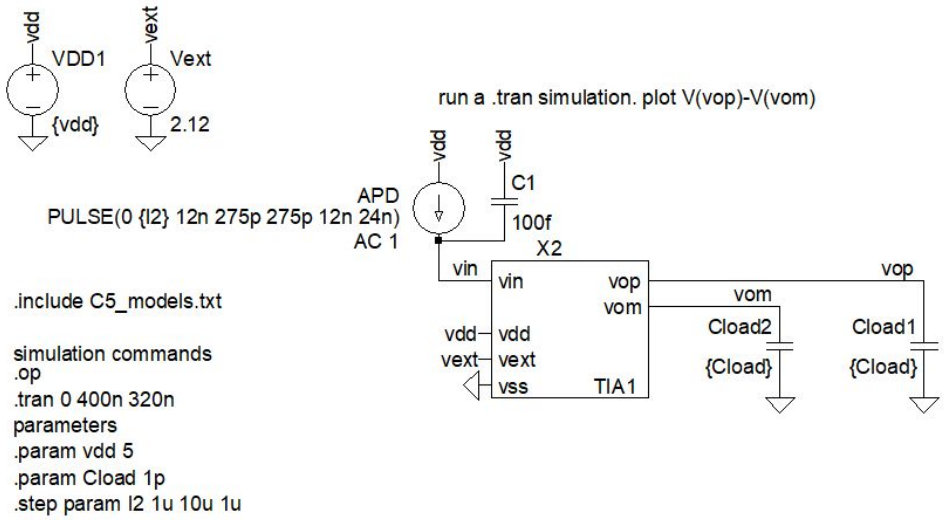


Figure 11: schematic used to simulate the large signal response and linearity of TIA1. A transient simulation is performed where the input current pulse is varied from 1 µA to 10 µA in increments of 1µA. A 1 pF load is assumed for both outputs.

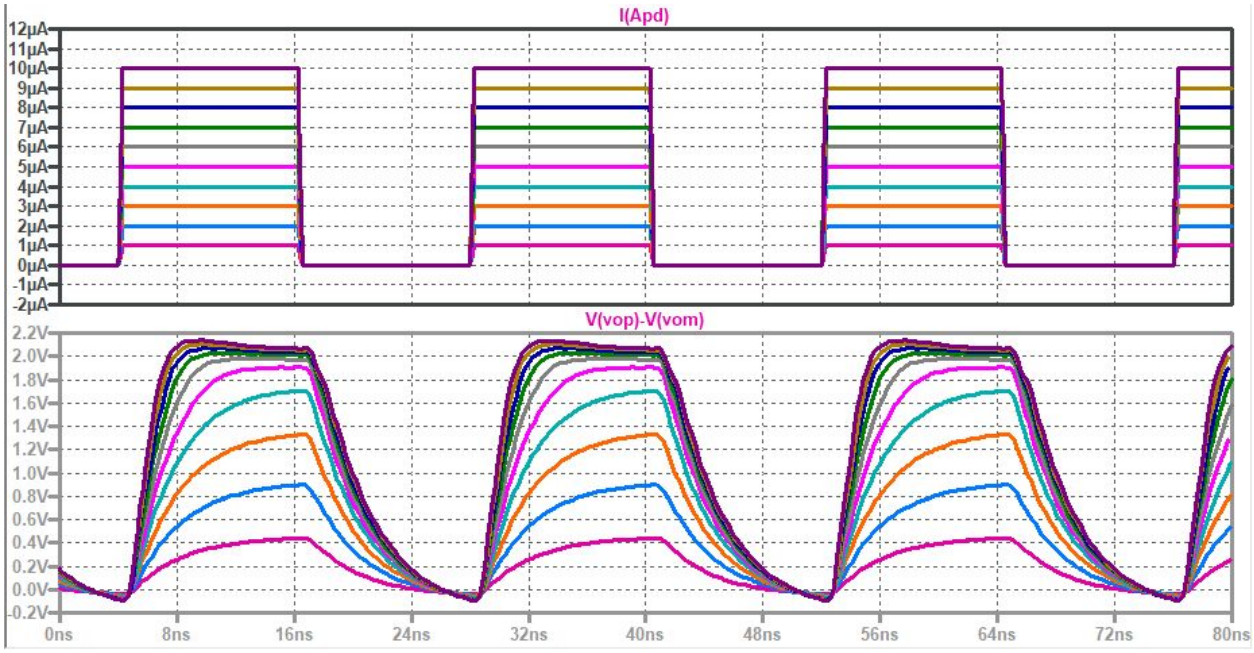


Figure 12: simulation results of the transient response of TIA1 to a 41.67 MHz square wave with 50% duty cycle. The plot shows the linearity of the TIA decreases for input currents above 5 µA. This shows how the input current pulses should be limited to no more than about 5 uA for this design. Also shown is the output swing which when taken differentially is about 2 volts.

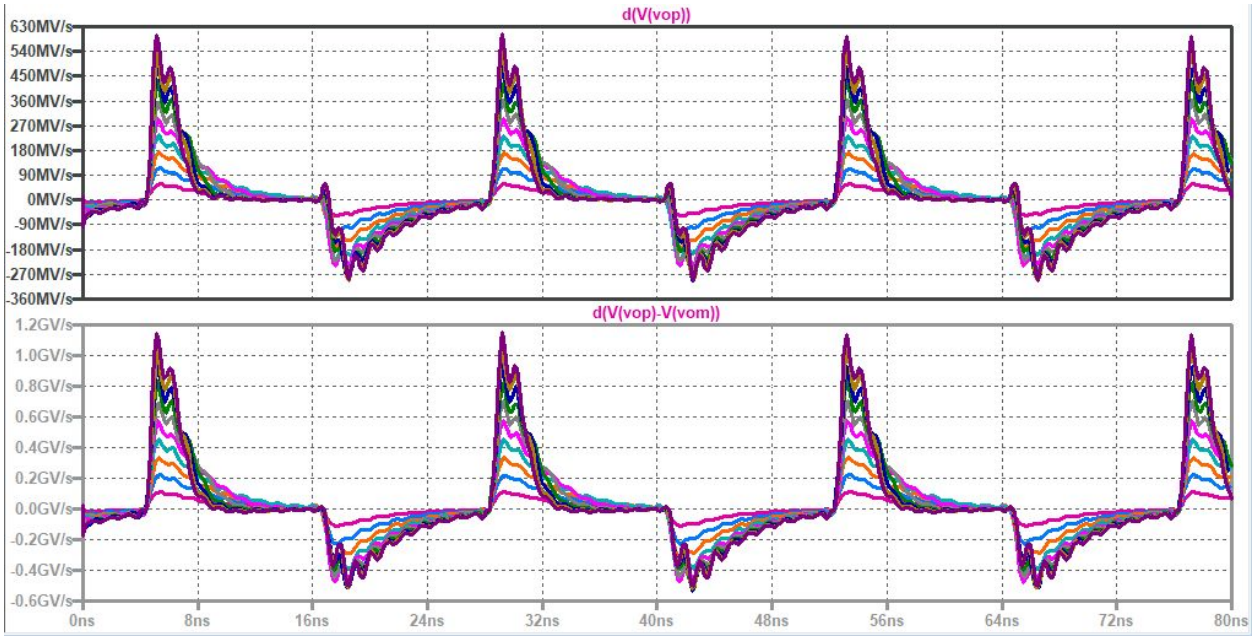


Figure 13: plot showing the slew rate of a single-ended output (top plane) and the slew rate of the differential signal (bottom plane) as a function of input current pulse. For large input currents of around 8 μA the single-ended slew rate reaches over 360 V/μs while for small input currents of 1 μA the single-ended slew rate only reaches 58 V/μs. Given that the differential slew-rate is double that of the single-ended, the design meets the minimum slew rate requirements.

### Noise simulation

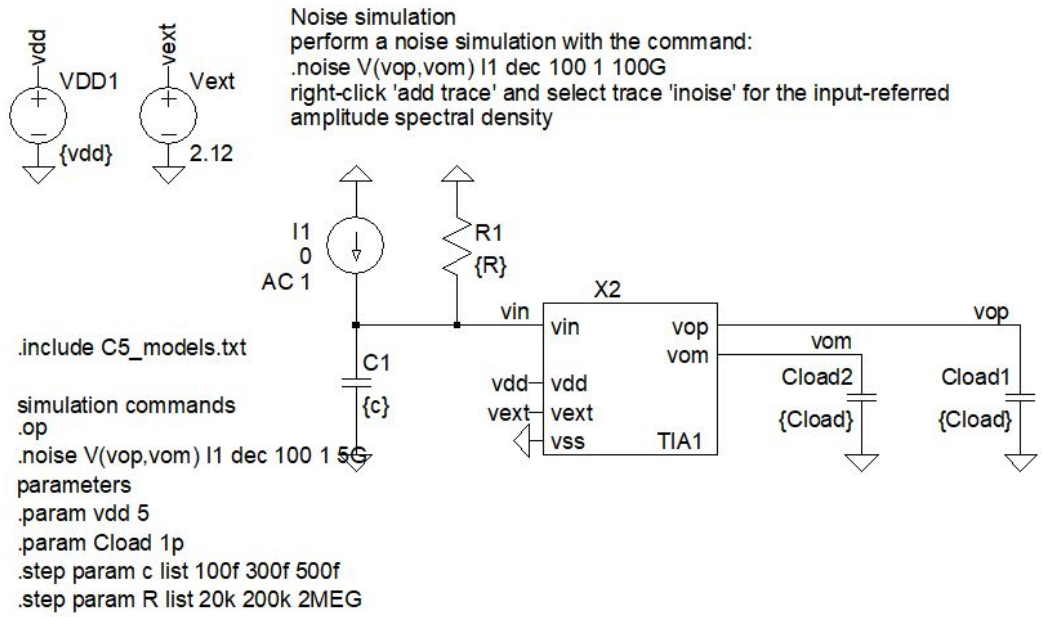


Figure 14: schematic used to simulate the input-referred noise of TIA1. Both resistor and capacitor values are varied to see their effect on the input-referred noise. The above configuration models the noise contributions when the APD is in series with a resistor and the anode is DC coupled to the input of the TIA input.

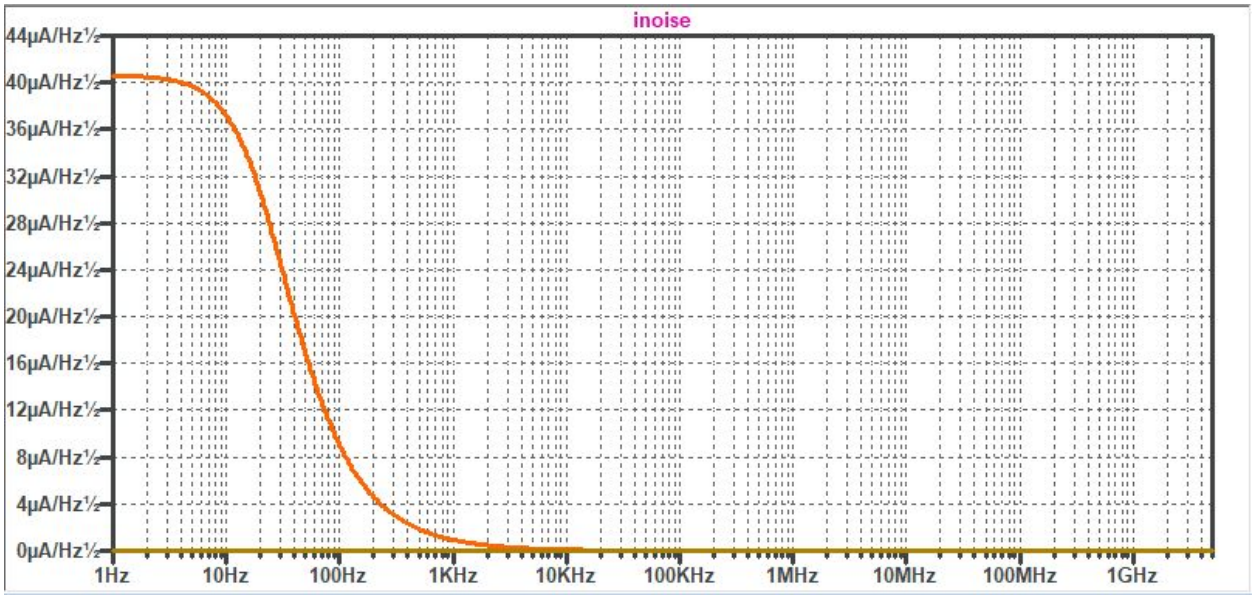


Figure 15: Noise simulation showing the effect of a small resistor (R = 20kΩ) on the input-referred noise. In order to meet the specifications a resistor on the order of at least 200 kΩ is required.

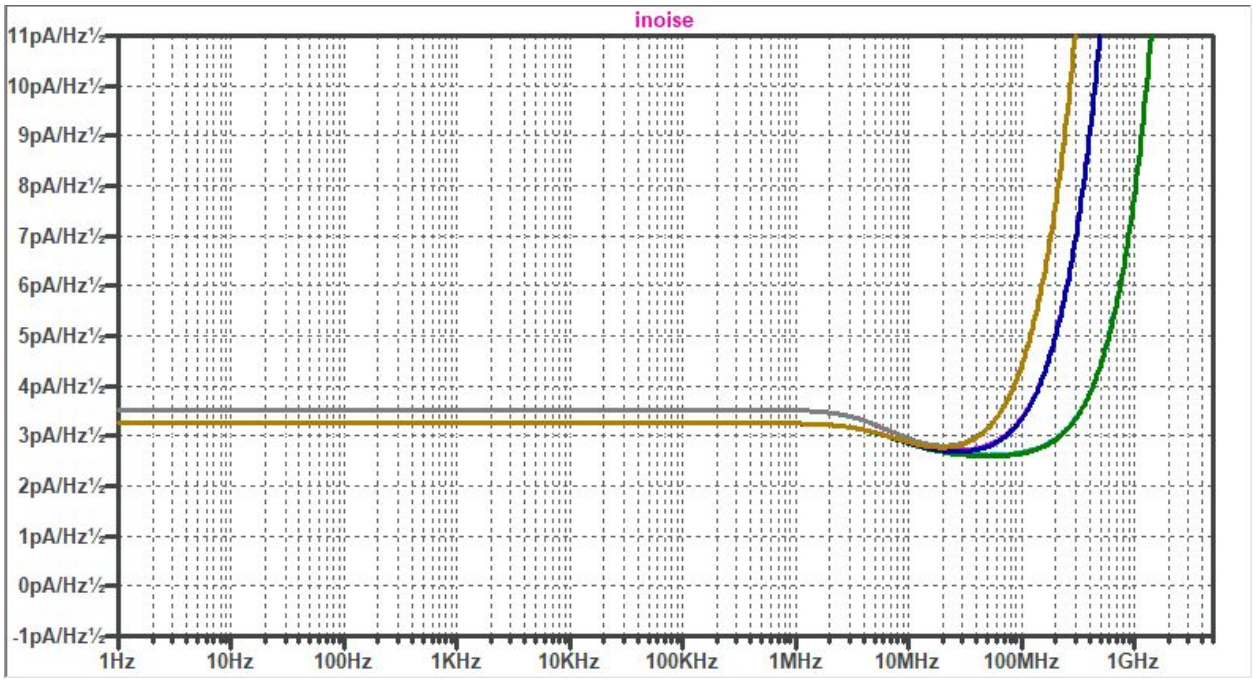


Figure 16: Noise simulation showing the effect on the input-referred noise that variations in resistance and capacitance on the input node have. The input-referred noise remains at a value below 3.6 pA/sqrt(Hz) within the bandwidth of 56.2 MHz.

**One-stage vs two-stage amplifier (TIA2 design)**

Given the difficulty in biasing a second stage amplifier following the transimpedance stage, one might go the route of using a single-stage amplifier with larger feedback resistor to set the gain.

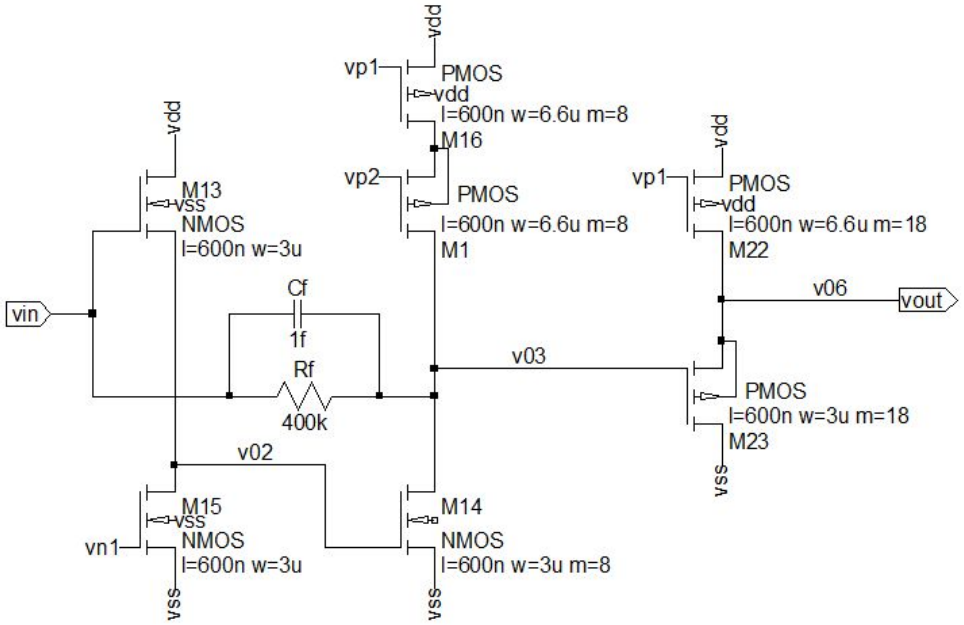


Figure 17: single stage transimpedance amplifier consisting of a common-drain input TIA followed by a source-follow amplifier. A 1 fF feedback capacitor is added to reduce the peaking in the frequency response. This may be implemented with several larger capacitors in placed in series.

Figure 17 shows an implementation of a single stage TIA followed by a simple source-follower used to drive the 1 pF load capacitor. Immediate advantages to the single stage TIA is, as already mentioned, that we avoid the trouble of biasing a second stage. Compared to the first design there is also a significantly less amount of current drawn from the supply and the layout area is vastly reduced.

A possible concern now that the feedback resistor is so large is that there may be a significant delay occurring between the two ends of the feedback resistor. Depending on the layout of the feedback resistor, parasitic capacitances along the resistor can accumulate to the point where the phase delay could cause stability issues at high frequencies. An alternative to using polysilicon or nwell resistors may be to use a MOSFET as the resistive device to generate the high resistance needed for the single stage amplifier. Other drawbacks include the higher input impedance and bandwidth sensitivity to parasitic input capacitance.

The following ac simulation shows how the performance of the single-stage TIA meets both total gain and bandwidth specifications when ignoring parasitic input capacitance.

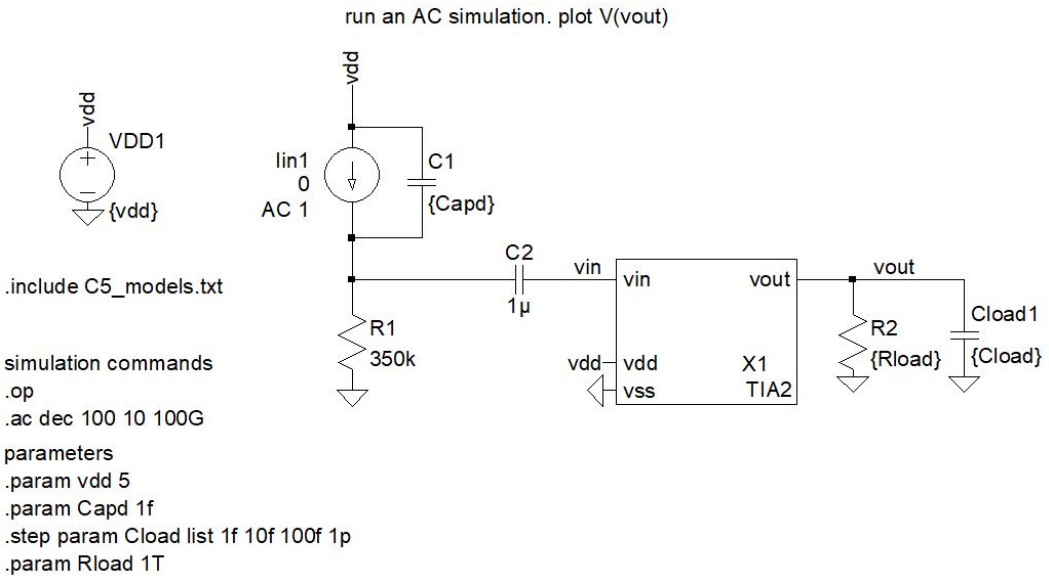


Figure 18: schematic used to generate the small signal response of TIA 2. The load capacitance is incremented from 1 fF to 1 pF by 1 step per decade. The simulation is run once with a small APD capacitance of 1 fF and then run again with a 100 fF capacitor.

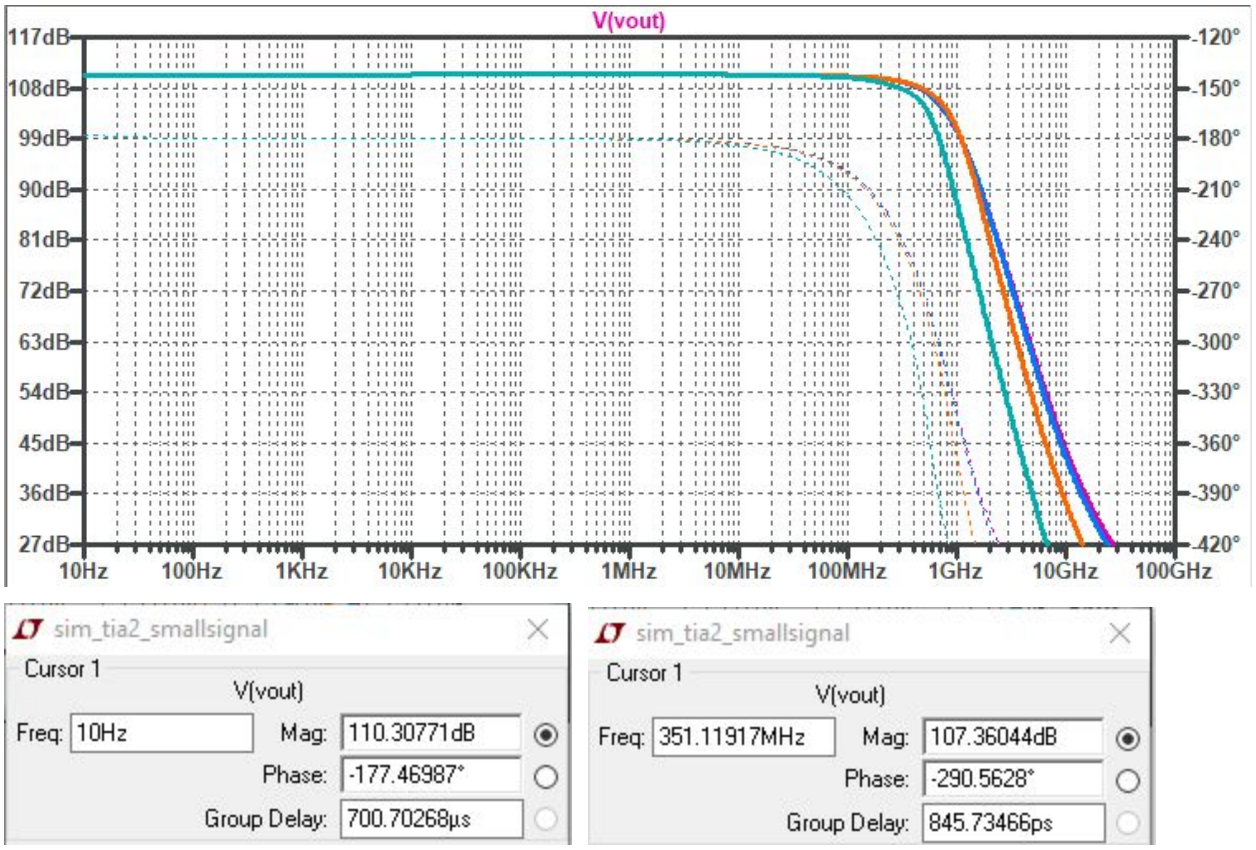


Figure 19: simulation results from the small signal analysis of TIA2 without the 100 fF APD parasitic capacitance. The pink trace corresponds to a load of 1 fF and the green trace corresponds to a load of 1 pF. The DC gain of TIA2 is 110 dB and the -3 dB frequency with a 1 pF load is about 350 MHz.

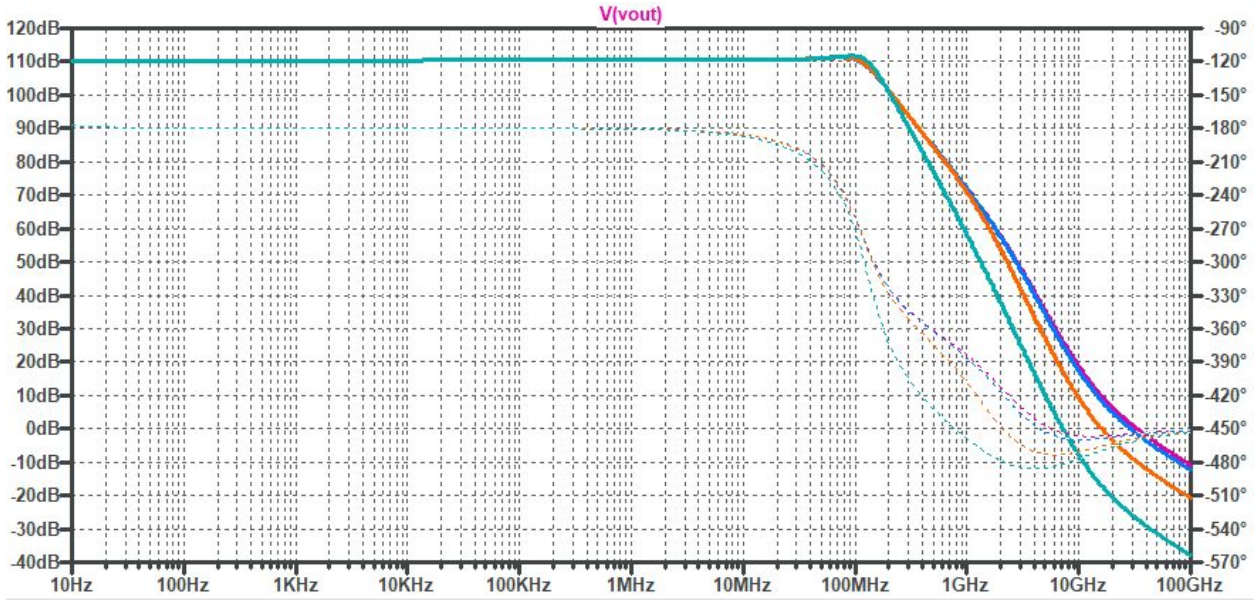


Figure 20: small signal response of TIA2 with a 100 fF parasitic capacitance on the input of the TIA. Note how the bandwidth has decreased to about 140 MHz below the target bandwidth.

**Conclusion**

The first design suffered from the inclusion of a second stage which was unable to achieve the required bandwidth. With further tweaking, the second stage could prove more promising than the attempt described in this report. Future improvements could include omitting one of the source followers used for level-shifting and instead use a complementary differential amplifier. This way level-shifting won't be as crucial considering the increase in the allowable input voltage range.

The second design was capable of meeting the bandwidth target until a parasitic capacitance was introduced and dropped the -3 dB frequency down to 140 MHz. The RGC input stage could help the design in terms of preserving bandwidth but DC coupling the TIA to the RGC input stage with such a high closed-loop gain causes a substantial DC current to flow through the feedback resistor. Because of the simplicity of design and reduced power consumption this design may prove to be the most promising for on-chip APDs which have smaller parasitic capacitances.

| MOSFET parameters for high speed design<br>VDD = 5 V<br>Scale factor = **600 nm** | | | |
|---|---|---|---|
| **Parameter** | **NMOS** | **PMOS** | **Comments** |
| Bias current | 60 uA | 60 uA | |
| W/L | 5/1 | 11/1 | |
| Actual W/L | 3 um / 600 nm | 6.6 um / 600 nm | |
| Vovd (Vds,sat and Vsd,sat) | 500 mV | 500 mV | 10% of VDD |
| Vgs and Vsg | 1.25 V | 1.4 V | |
| Vthn and Vthp | 750 mV | 900 mV | |
| C'ox | 2.48 fF/μm^2 | 2.48 fF/μm^2 | |
| Coxn and Coxp | 4.46 fF | 9.82 fF | |
| Cgsn and Csgp | 2.97 fF | 6.50 fF | 0.667 * Cox |
| Cgdn and Cdgp | 0.6 fF | 1.91 fF | CGDO * W |
| gmn and gmp | 215 uA/V | 250 uA/V | |
| Ron and Rop | 190 kΩ | 120 kΩ | |
| gmn * Ron and gmp * Rop | 40.85 V/V | 30 V/V | |
| Rocas,n and Rocas,p | 7.76 MΩ | 3.6 MΩ | |

Table 2: Device parameter reference table

**References**

[1] Park, Sung Min. Yoo, Hoi-Jun. "1.25-Gb/s Regulated Cascode CMOS Transimpedance Amplifier for Gigabit Ethernet Applications". IEEE Journal of solid state circuits. Vol. 39, No. 1, January 2004.