CMOS Switching Power Supply (SPS)
EE421 Digital Electronics and ECG 621 Digital Integrated Circuit Design
Course Project
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Introduction

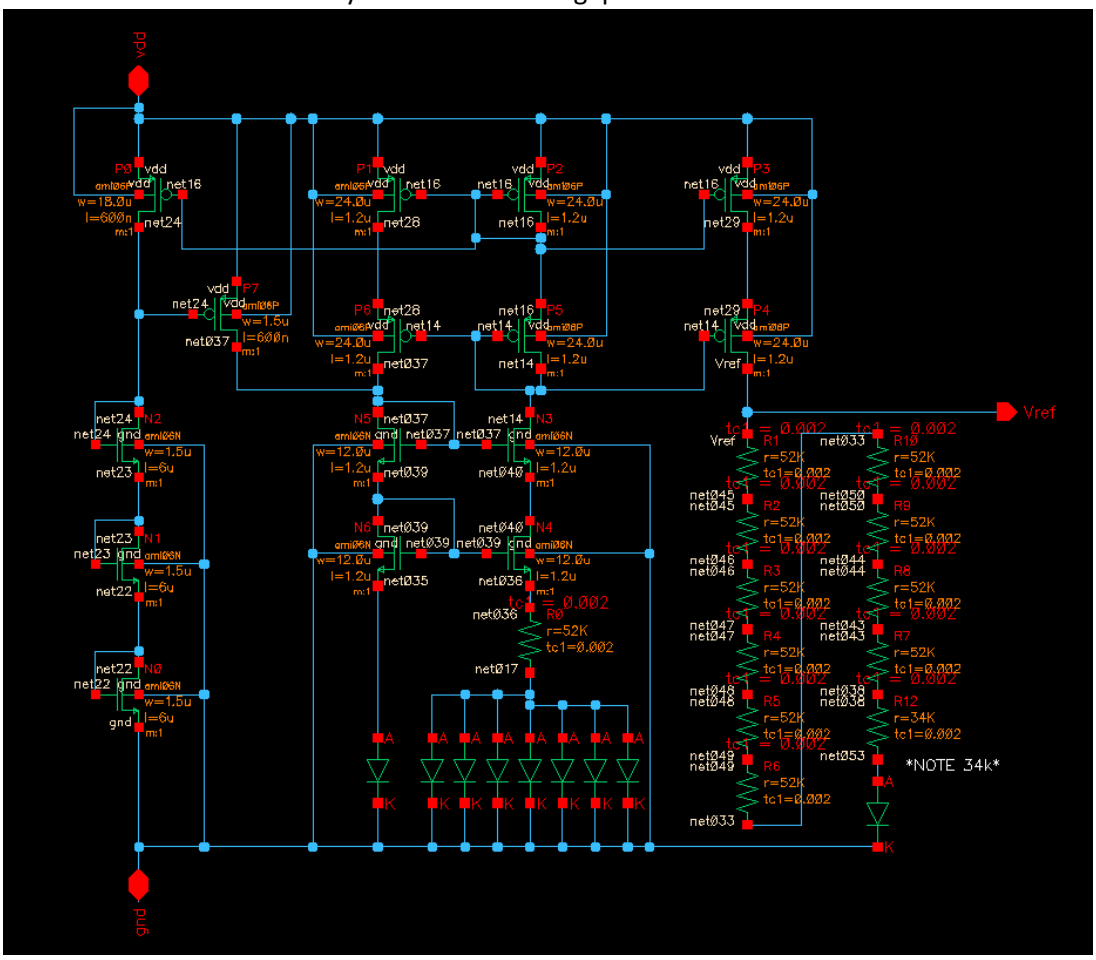
The course project is to design a CMOS switching power supply (SPS), Boost converter, that is powered with a VDD that can vary from 3.75 to 4.75V. This power supply uses an off-chip Schottky diode, inductor, and capacitor to generate a constant output voltage of 5V. The load current ranges from 0 to 20mA.

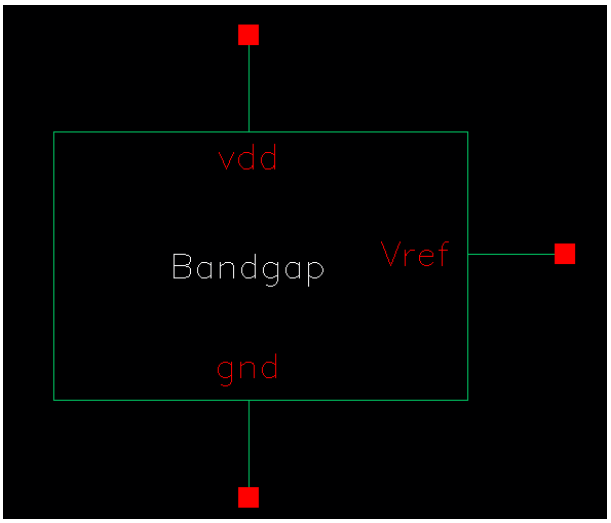
The project is broken down into a couple parts and several components. The components are the bandgap, the comparator, the ring oscillator, the boost, and a voltage divider with an input voltage coming from the boost output or feedback, having the output of the voltage divider going into the comparator. The boost part of the circuit is an inductor, Schottky diode, capacitor, and a resistor representing the load. The boost is the part of the circuit that will not be a layout design, but the rest of the circuit will be a layout using the C5 process (500nm).

First part of the project: Bandgap

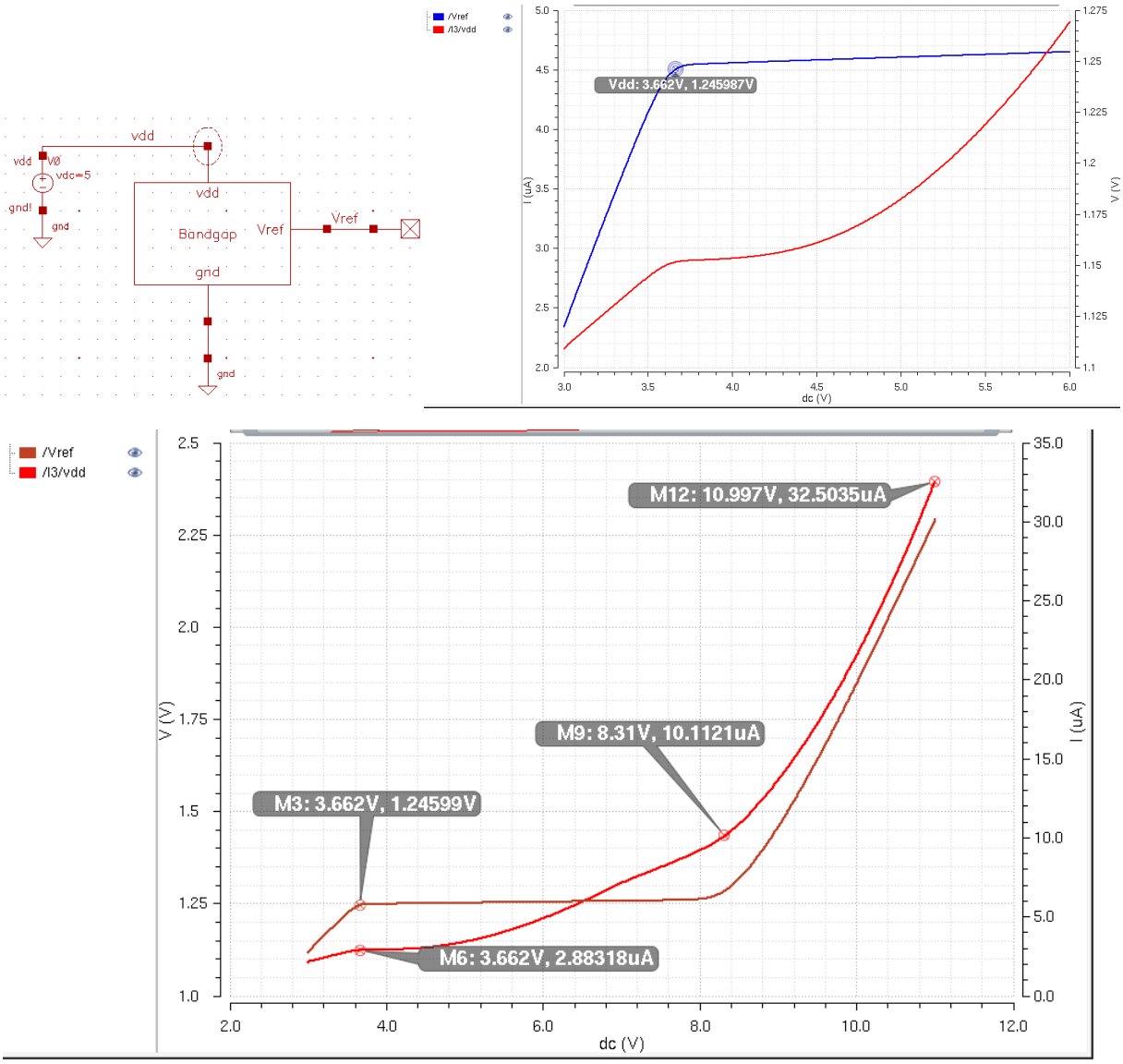
The first part of this project is to layout the bandgap. The bandgap is a circuit that generates a voltage that changes very little in respect to variations in temperatures, and/or VDD (power supply voltage). For this reason, this voltage can be use as a reference voltage. The output of the bandgap is 1.25V.

Below is the schematic and symbol for the bandgap





Simulation for the bandgap showing the change in output (Vref) as the power supply increases. If the power supply goes below 3.66V, then there is a dramatic change of rate in the Vref and the output voltage drops below, the value that we want. Also, the current increases semi linearly between 3.66V and about 8.4V at a rate of about 1.525uA per voltage.



Second Part:
The second part of the project is to design a circuit that senses the output voltage *Vout*. The design should use the bandgap from part 1. The output (called *Enable*) of the circuit is a logic 0 (gnd) when *Vout* is greater than 5 V and a logic 1 (vdd) when *Vout* is less than 5 V. The circuit's input is connected to *Vout* and should draw no more than 50 uA of current and no less than 10 uA of current. A practical design concern pops–up when *Vout* is near 5 V, which it will be in these projects.

The comparator
The comparator we are using is comparing the positive and negative inputs, and outputs high or low depending on which is higher. In this case the positive input is connected to the Bandgap output, which is being used as the reference voltage. The negative input is the output of a voltage divider circuit with and input coming from the feedback output of the system. The voltage divider has been set to output 1.25V for an input of 5V, which is the output of Boost SPS. Since the positive input of the comparator is connected to the bandgap, the reference voltage is 1.25V. The output of the Boost SPS is being compared to this reference voltage. Thus, when the output of the system is below 5V (below 1.25 after the voltage divider, then the output (enable) of the comparator goes high. And when the output of the Boost is higher than 5V, then the output (enable) goes low.

This output, which is called enable is being used to connect to a 2-input NAND gate, which has an output connected to the input of an oscillator. The output of the comparator controls the oscillator. When the output (enable) is high the oscillator runs its course. However, when the output goes low the oscillator stops oscillating because the output of the NAND gate is hold at 1 for that period.

This circuit is designed using three cascaded self-biased diff-amps and two inverters. Below in fig. 18.17 the circuit of a differential amplifier, which is a self-biased because no external references are used to set the current in the circuit. When Vinp is larger than Vinm, the current is M2 is larger the current in M1 because the Voltage between the gate and source of M2 becomes larger than the voltage between the gate and source of M1. M1 current's flows through M3, and is mirrored by M4, which causes diff-amp's output to go to ground. The information to describe this set up was taken from the CMOS Circuit, Design, Layout, and Simulation Third Edition book.
This topology is used for the comparator, but the Width and Length of M6 NMOS is sized to be 6u for both because this minimizes the current flowing through it, to create a higher gain.

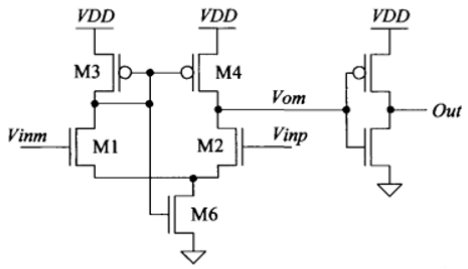
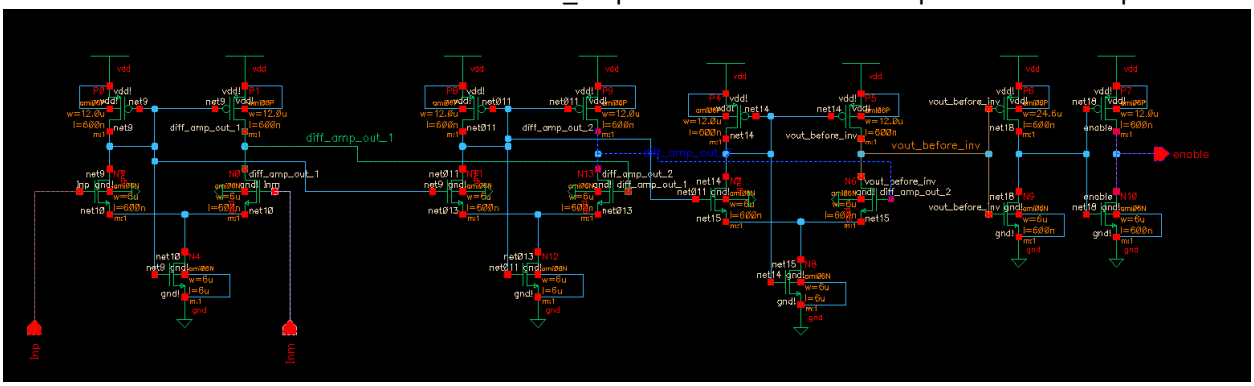
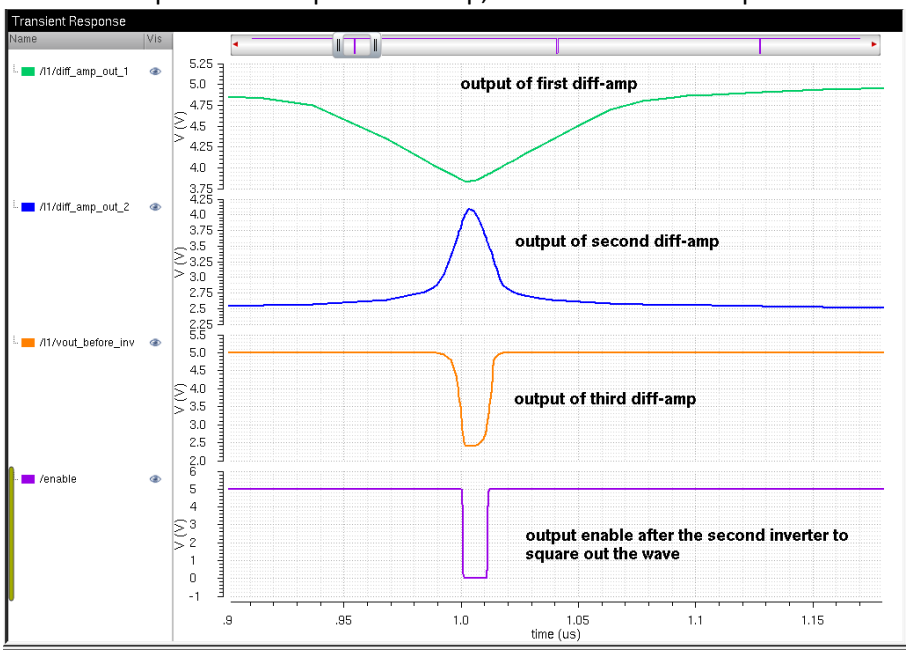


Figure 18.17

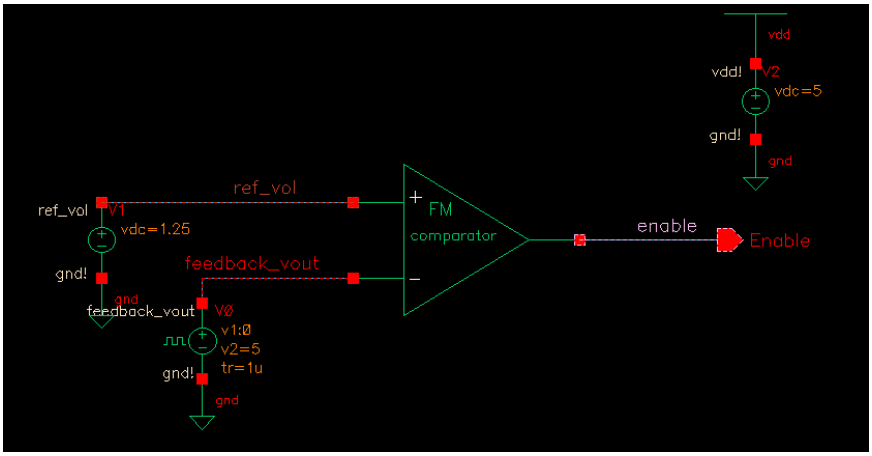
Below is are the three cascaded self-biased diff_amps and two inverters to square out the output wave.



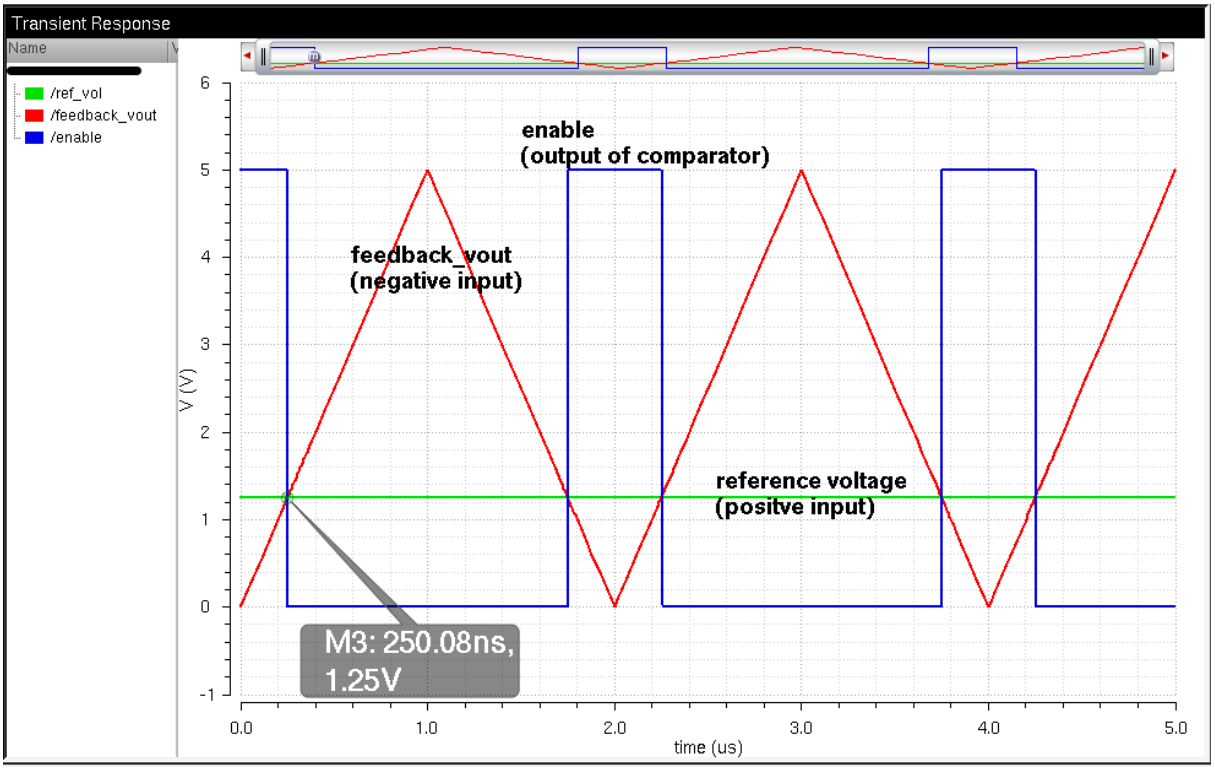
Below is the plot for a simple test set up, which shows the output of each diff-amp



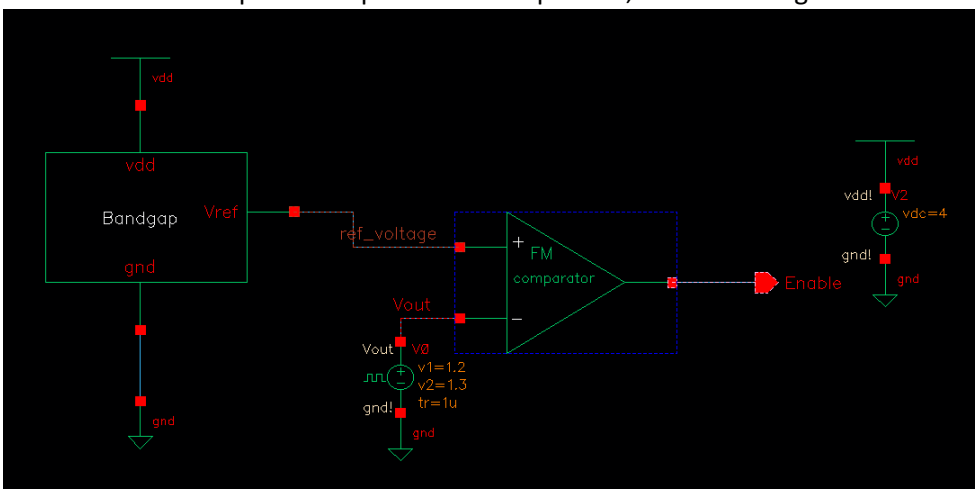
Below is the schematic used to simulate the test set up. This is also the same set up to which the plot above and below belongs to.



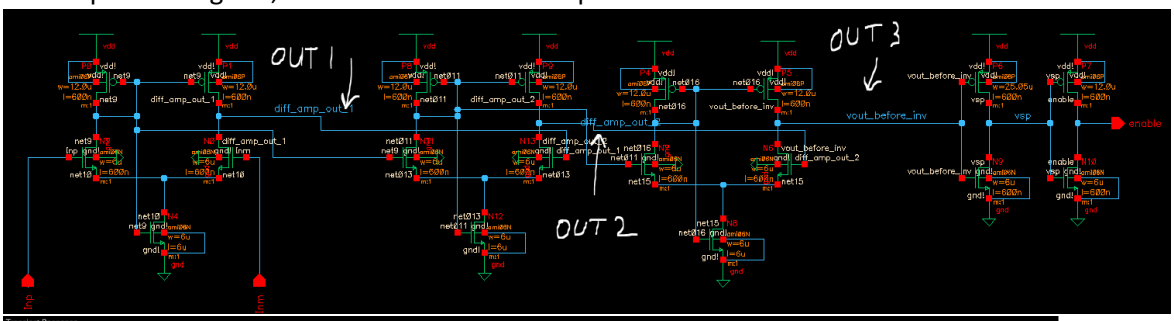
Here we can see that the comparator is working correctly with the simple set up shown above. When the negative input of the comparator is higher than 5V, the output (enable) goes low, and when the negative input goes below 5V the output goes high.

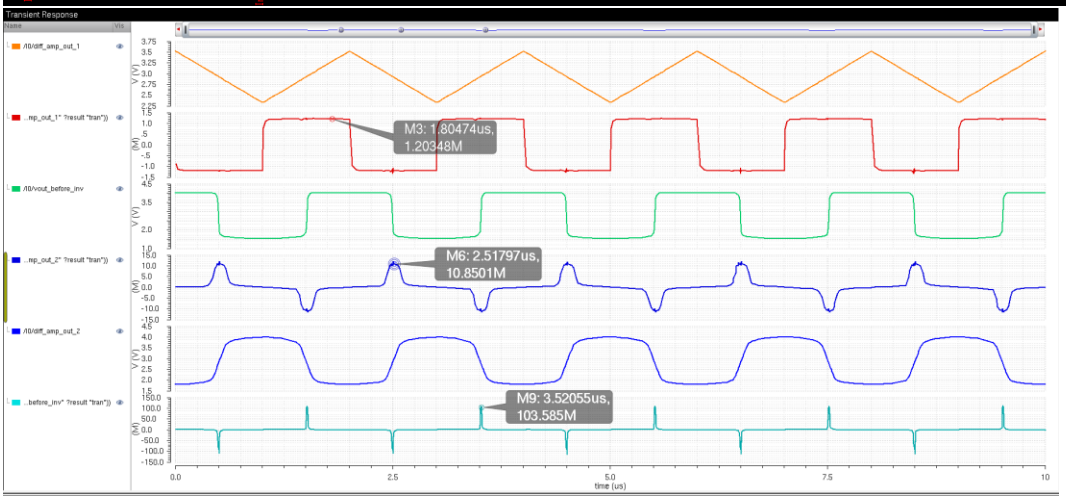


The schematic below is the set up to test the comparator with the Bandgap. The bandgap output (Vref) is connected to the positive input of the comparator, which is being used as the reference voltage.



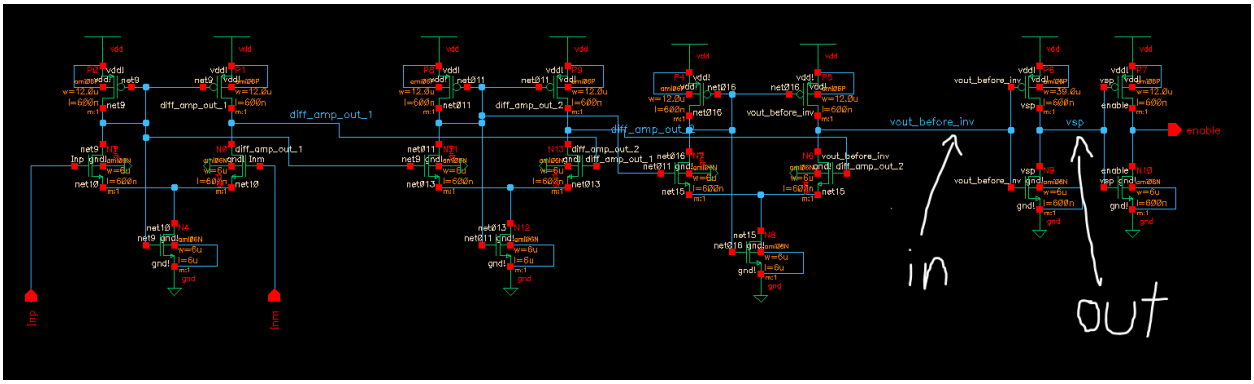
Here, the schematic shows the nodes that are being tested to show the output voltage swing of each diff-amp and the gains, which are shown on the plot below the schematic.

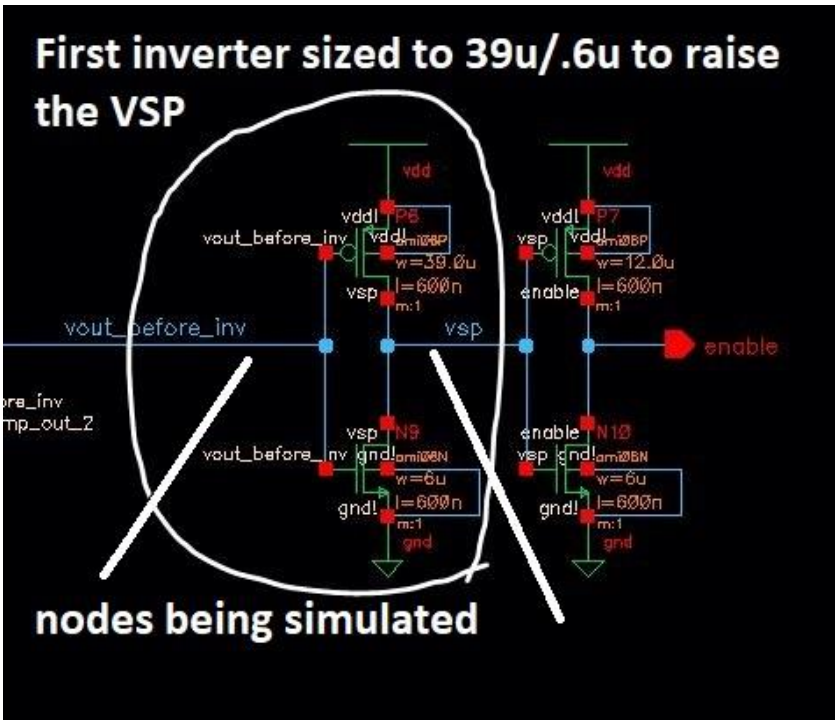




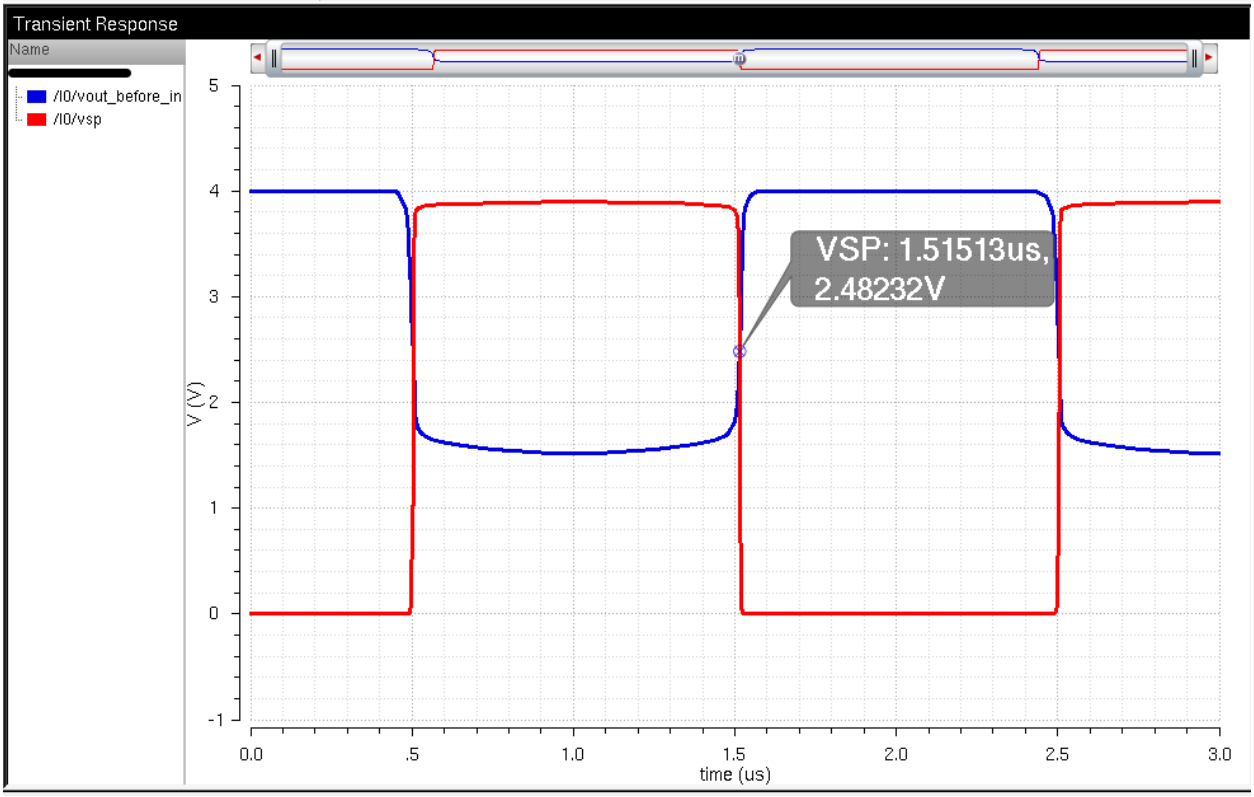
The schematic below shows the nodes that were tested to look at the switching point. Because the input voltage of the first inverter, which is the output of the third diff-amp was not swinging between VDD and ground, the switching point had to be brought higher in order to slice the input voltage.
To raise the switching point, the 50nm VSP topology was used, and then make small adjustments if needed. However, in this case, no other adjustments were necessary, since the VSP of the inverter was raised high enough. In this case since VDD = 4V and the voltage from the diff-amps are swinging between 4 and 1.521, then we want a VSP at half that, which is at about 2.76V

$$Vsp = VDD\frac{R_n}{R_n + R_p} \quad \Rightarrow 2.76 = VDD\frac{2k}{3k + R_p} \quad \Rightarrow R_p \simeq 620\Omega, \quad w = \frac{40k}{930\Omega} = 65, \quad 39um$$





The plot below shows the switching point at the nodes specified above. The PMOS' width of the first inverter was sized to 39um according to calculations above. Even though we calculated the VSP to be about 2.76V, we obtained an actual VSP of about 2.44V, which is close to what we were looking for.



Next, the resistors for the voltage divider connected to the negative input of the comparator were calculated. We know that this resistance should not draw no more than 50 uA of current and no less than 10 uA of current. So, we took the difference voltage coming from the Vout (output voltage of system), 5V, and 1.25V, which is the voltage divider output connected to the comparator. This output of the voltage divider is what is being compared to the reference voltage, 1.25V, coming from the Bandgap.

$$Vout_{divider} = vout\frac{R_1}{R_1 + R_2} \;\Rightarrow\; 1.25V = 5V\frac{R_1}{R_1 + R_2}$$

$$\frac{5V - 1.25V}{R_1} = 30uA \;\Rightarrow\; R1 = \frac{3.75V}{30uA} = 125k\Omega$$

$$R2 = \frac{1.25V}{30uA} = 41.67k\Omega$$

The Ring Oscillator

The oscillator is the system's clock that is controlled by the output of the comparator or the Enable. When the Enable is high the oscillator turns on and when the Enable is off, then the oscillator stops working or oscillating. The oscillator is made of 30 weak inverters (6u/6u for PMOS and NMOS) and a 2-input NAND gate. The NAND gate inputs are the Enable from the comparator and the output of the last inverter named osc_out. First, the delay of one inverter was calculated, then used that information to obtain the frequency between 1MHz and 5MHz. For 1MHz it was about 53 inverters but chose 30 inverters instead to minimize the layout space. Then a buffer was connected to the output of this oscillator in order to drive the switching NMOS that has the off-chip inductor and Schottky diode connected to the drain.

$$C_{oxn} = C'_{ox}WL = \frac{2.5fF}{um^2}(6u)(6u) = 90fF$$

$$C_{oxp} = C'_{ox}WL = \frac{2.5fF}{um^2}(6u)(6u) = 90fF$$

$$R_p = 40K\frac{L}{W} = 40K\frac{6u}{6u} = 40k \qquad R_n = 20K\frac{L}{W} = 20K\frac{6u}{6u} = 20k$$

$$C_{total} = C_{oxp} + C_{oxn} + \frac{3}{2}\left(C_{oxp} + C_{oxn}\right) = \frac{5}{2}\left(C_{oxp} + C_{oxn}\right) = \frac{5}{2}(90fF + 90fF) = 450fF$$

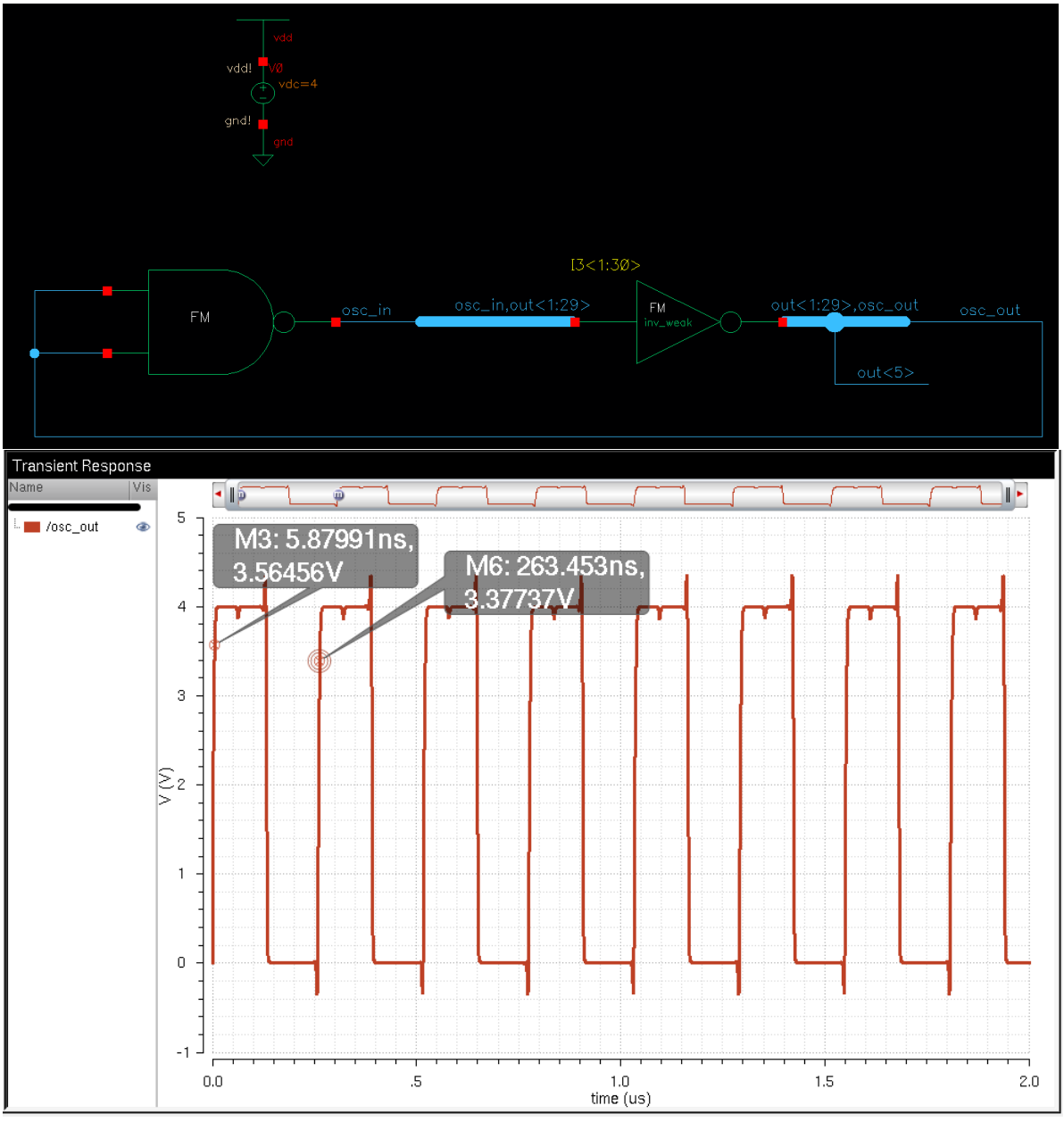
$$(t_{PLH} + t_{PHL}) = (0.7)(R_n + R_P)(C_{total}) \quad\Rightarrow\quad (0.7)(20k + 60k)(450fF) = 18.9ns$$

$$f = \frac{1}{n(t_{PLH} + t_{PHL})} \;\Rightarrow\; n = \frac{1}{f(t_{PLH} + t_{PHL})} \;\Rightarrow\; n = \frac{1}{1MHz(18.9ns)} = 52.9$$

By looking at the number of inverters needed for 1MHz, this will take much space in a layout, so the number is decreased to 30 inverters. Which comes to a frequency of about 1.76MHz. Here the delay of the NAND gate is being neglected because is very small compared to one inverter.

$$f = \frac{1}{30(18.9ns)} = 1.76MHz$$

However, after doing simulations the frequency came to be at about 3.85MHz and period of 260ns. Below is the schematic and simulation plot for the oscillator.



Before we start sizing up the inverters composing the buffer, we want to size the switching NMOS, which will give us the capacitance needed to calculate the widths of the cascading inverters. If we choose A(gain) to be 8 then we can calculate the number of inverters using the formula below.

$$N(lnA) = ln\frac{C_{load}}{C_{in}}$$

But first we want to size the switching NMOS. We want small Rn value, because we want it to handle the current and have a low voltage drop.

The Rn being chosen is about 4 Ohms. Now we want to solve for the W if we make L=0.6u

$$R_n = 20k\frac{L}{W} \quad \Rightarrow \quad 4\Omega = 20k\frac{1}{W} \quad \Rightarrow \quad W = \frac{20k}{4} = 5000, \qquad W = \ 5000 * 0.6u = 3000u$$

$$C_{oxn} = C'_{ox}WL = \frac{2.5fF}{um^2}(3000u)(0.6u) = 4.5pF$$

Now, using the formula above we can calculate the number of inverters needed using A(gain) of 8 and the Cox from the switching NMOS as the C_load. And Cin is the Coxn and Coxp from the first inverter being added together times 3/2.

$$C_{oxn} = C'_{ox}WL = \frac{2.5fF}{um^2}(12u)(0.6u) = 18fF$$

$$C_{oxn} = C'_{ox}WL = \frac{2.5fF}{um^2}(6u)(0.6u) = 9fF$$

$$C_{in} = \frac{3}{2}(18fF + 9fF) = 40.5fF$$

$$N(ln8) = ln\frac{C_{load}}{C_{in}} \quad \Rightarrow \quad N = \frac{1}{2}ln\frac{C_{load}}{C_{in}} \quad \Rightarrow \quad N = \frac{1}{2}\left(ln\frac{4.5pF}{40.5fF}\right) = 2.36\,, \qquad N = 3(odd\ number)$$

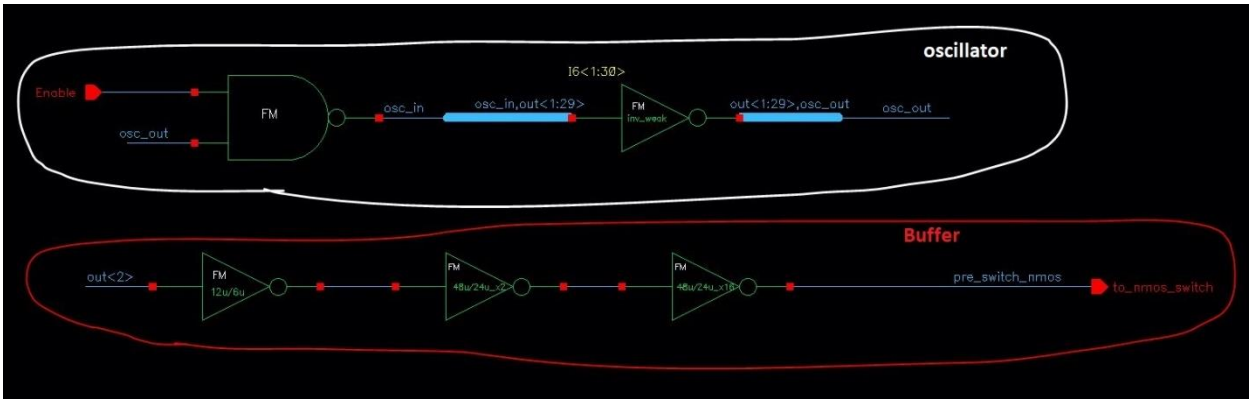
This means that we want 3 inverters each having an increase of 8 or gain = 8.

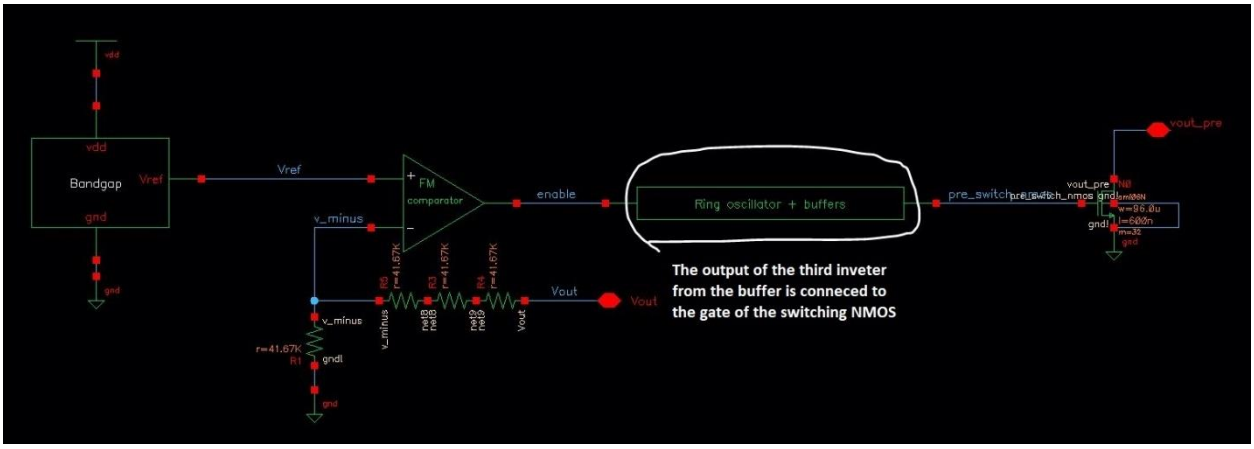
$$first\ inverter\ size = \frac{w_{PMOS}}{w_{nMOS}} = \frac{12u}{6u}$$

$$second\ inverter\ size = \frac{w_{PMOS}}{w_{nMOS}} = \left(\frac{12u}{6u}\right) * 8 = \frac{96u}{48u}$$

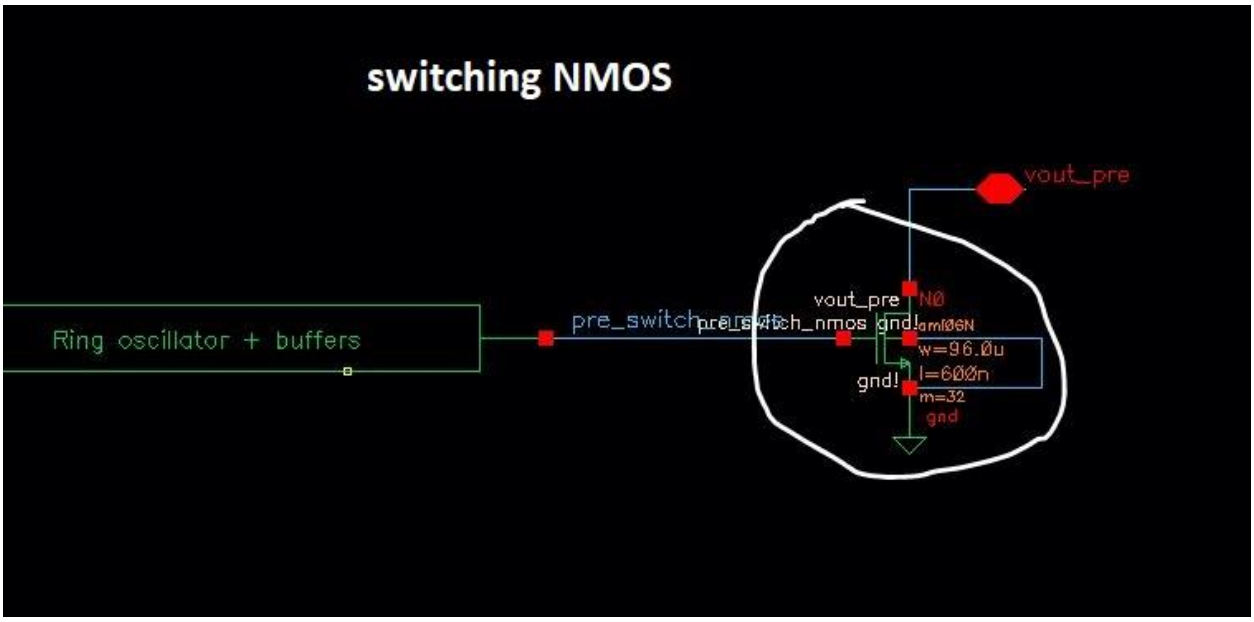
$$third\ inverter\ size = \frac{w_{PMOS}}{w_{nMOS}} = \left(\frac{96u}{48u}\right) * 8 = \frac{768u}{384u}$$

The output of the third inverter will be connected to the gate of the switching NMOS

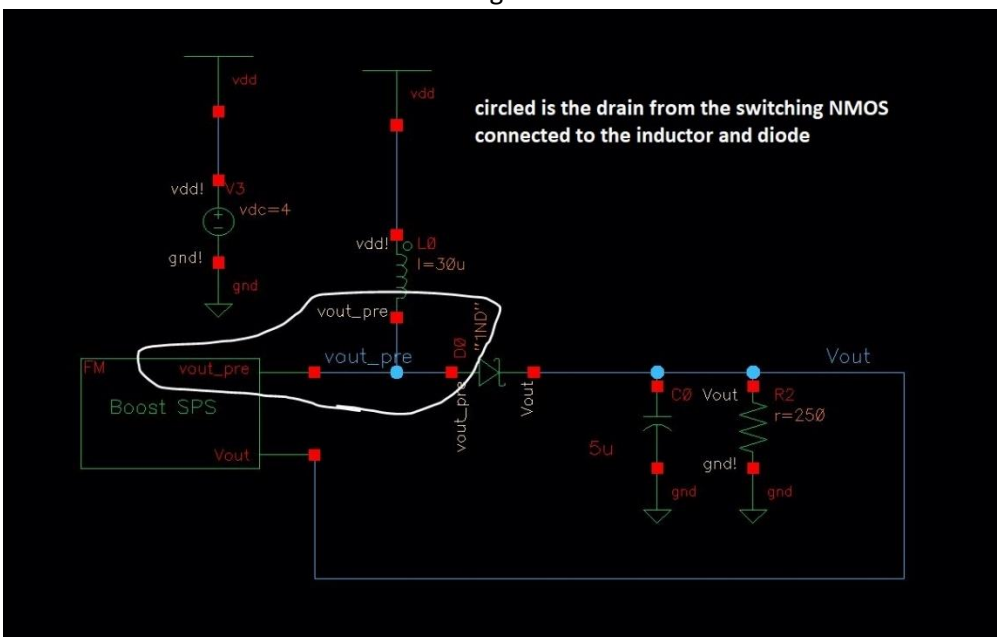




Below is a snip of the switching NMOS. The source is connected to ground and the drain is connected to the inductor and diode.



Below shows the drain from the switching NMOS connected to the inductor and to the schottky diode.



Above is the schematic for the top hierarchy. The inductor, schottky diode, capacitor, and the Load Resistor. Those components are the off-chip components, which will not be in the layout.

Now, we can calculate the values for the off-chip components.

$$I_R = 20mA \ , \quad R_{load} = \frac{5V}{20mA} = 250\Omega$$

$$Average\ I_L = \frac{I_R}{(1-D)} = \frac{20mA}{0.5} = 40mA$$

To calculate the inductor value the formula below was used. For Δ_{iL} we will be using 5% of the maximum average current, which is 2mA

$$L = \frac{(Vout)D(1-D)}{f(\Delta_{iL})} = \frac{5(0.5)(1-0.5)}{3.84MHz(2mA)} \simeq 162.76\ uH$$

And for the Capacitor, we are choosing for a small ripple voltage of 0.001.

$$C = \frac{D}{(R)f\left(\frac{\Delta Vout}{Vout}\right)} = \frac{0.5}{(250)(3.84MHz)(0.001)} \simeq 0.5208uF$$

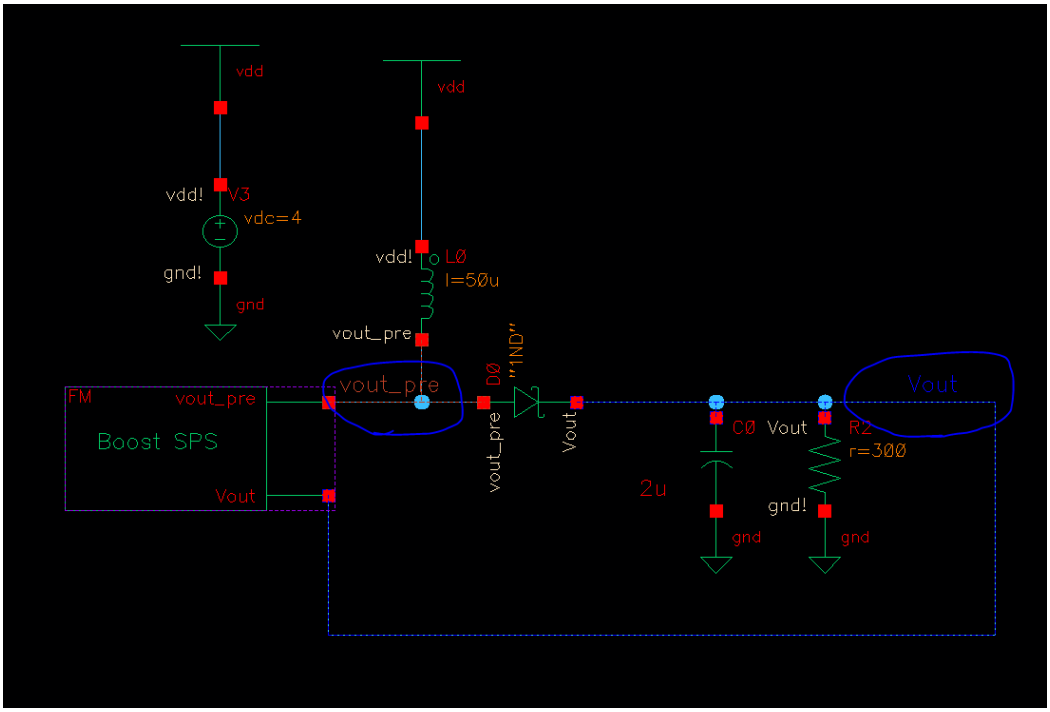
However, those values were giving results with a bigger ripple voltage than expected, So the capacitor and the inductor values were changed to 5uF and 30uH. Those numbers were chosen because the output was showing small ripple voltage.

Values for L and C used are 30uH and 5uF respectively.

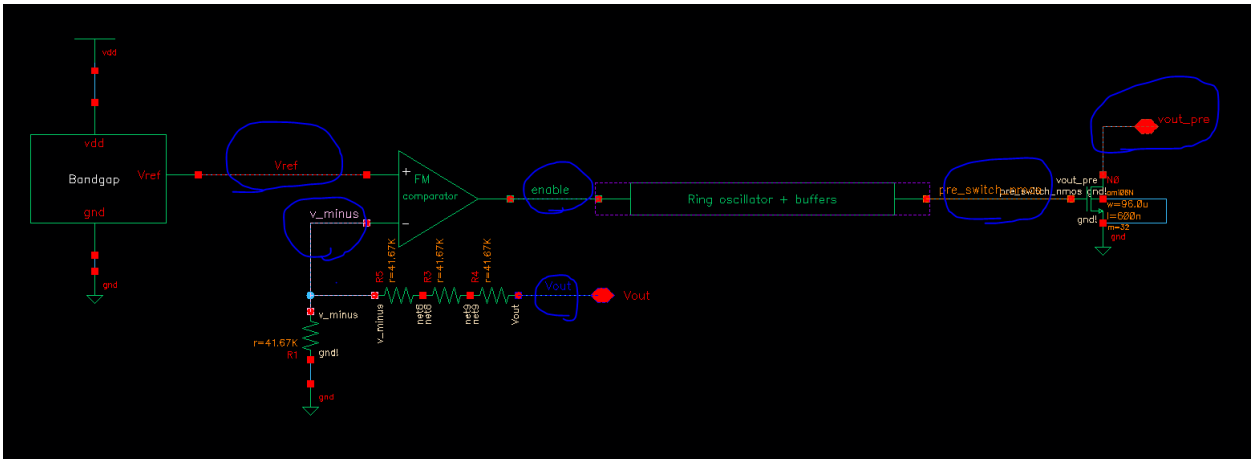
The schottky diode chosen was 1N5819 because it has a small parasitic resistance Rs=0.051. This diode has small voltage drop, because we want to match as close as possible the voltage on the drain of the Switching NMOS and the output (Vout) voltage. And to prevent the current from flowing back into the inductor node when the NMOS turns off.

Below is the schematic and plot showing the that the nodes being tested are working correctly after doing small adjustments or tweaking the circuit.

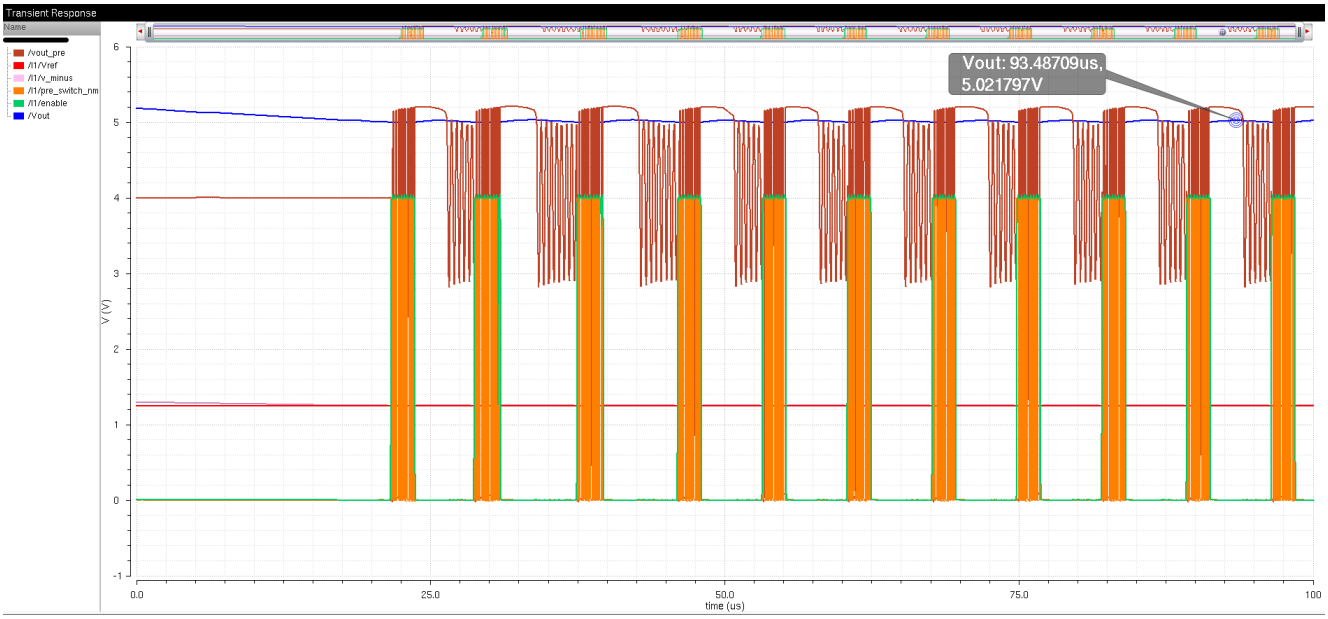
Upper hierarchy of the circuit. The nodes circled in blue are the nodes being tested.



Nodes being tested in the lower hierarchy

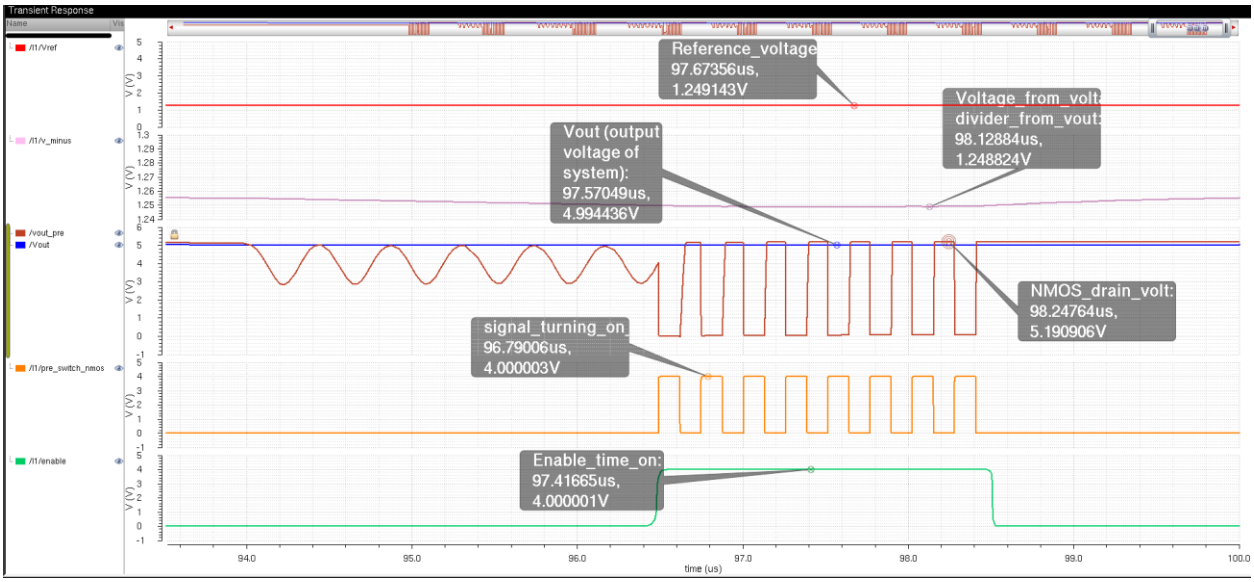


Here is a plot of all the nodes shown at once, but the Vout (output) is being marked to show is very close to 5V.

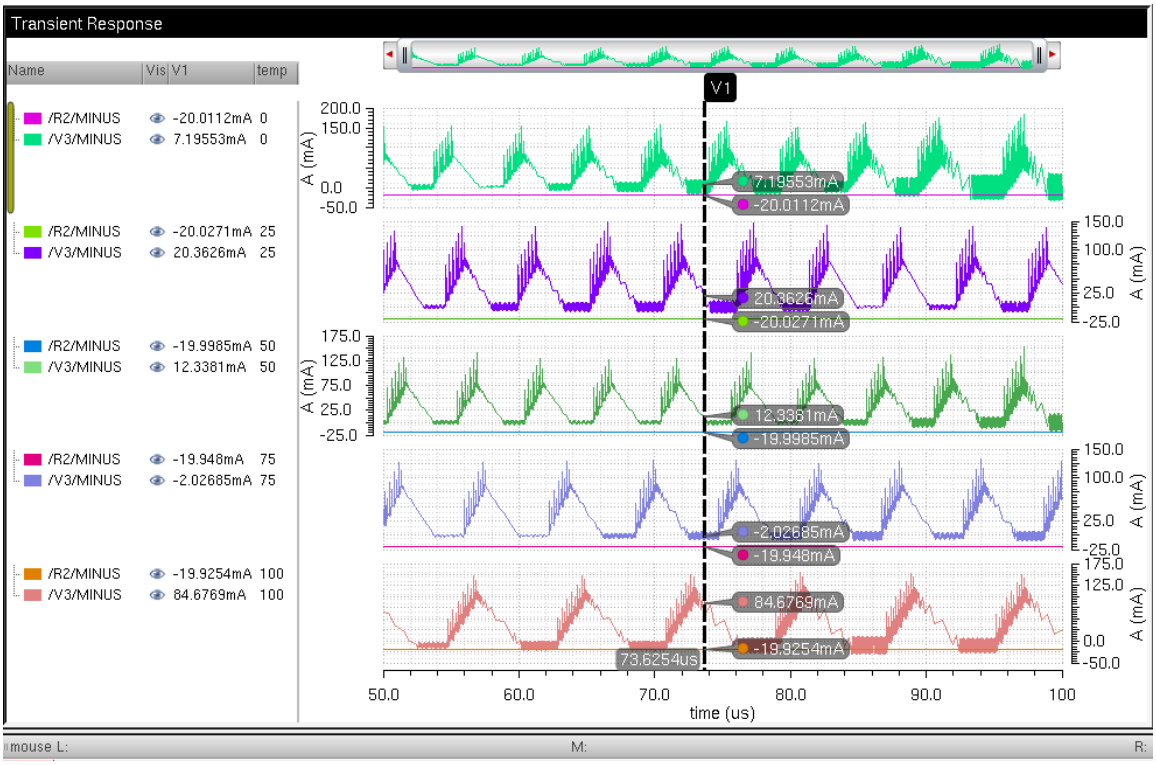


The plot below shows the same nodes at the plot above except with divided strips to show what each node is doing.

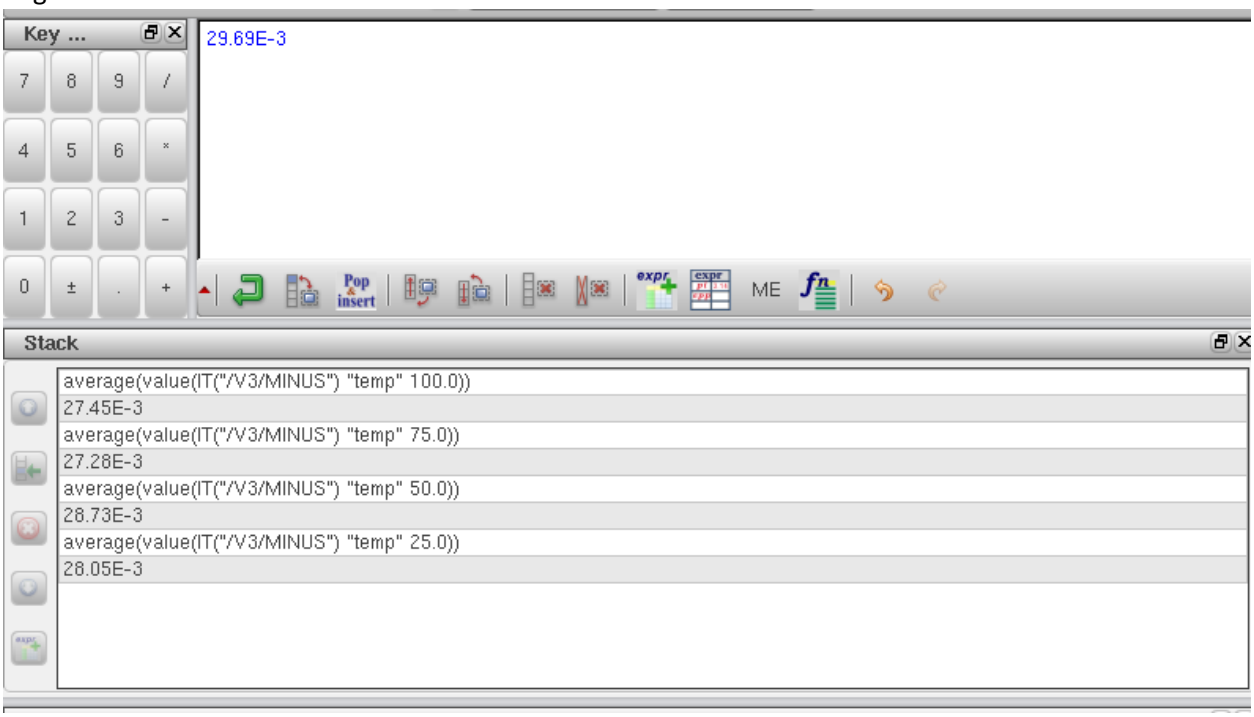
- The Vref is the Reference Voltage coming from the bandgap is being maintained at 1.25V as expected.
- V_minus is the output voltage from the voltage divider, which has the input coming from the feedback output.
- Vout_pre (red) and Vout (blue) show the output voltage which is at 5V and the voltage before the diode. Vout_pre is the voltage on the drain lead of the switching NMOS and is a little over 5 volts because of the charge from the diode capacitance.
- Pre_switch_nmos (yellow) is the on/off switching signal connected to the Gate of the NMOS, having a frequency same as the oscillator and coming from the set of buffers to minimize the delay (td) in order to drive the switching NMOS. This signal stays on while enable (green signal) is high and is off when enable is low.
- Enable (green) is the output signal from the comparator. Output is high when Vout (output voltage) is lower than 5V and is low when Vout is higher than 5V.



Below is the plot showing the current of the load and the current through the battery or power supply.



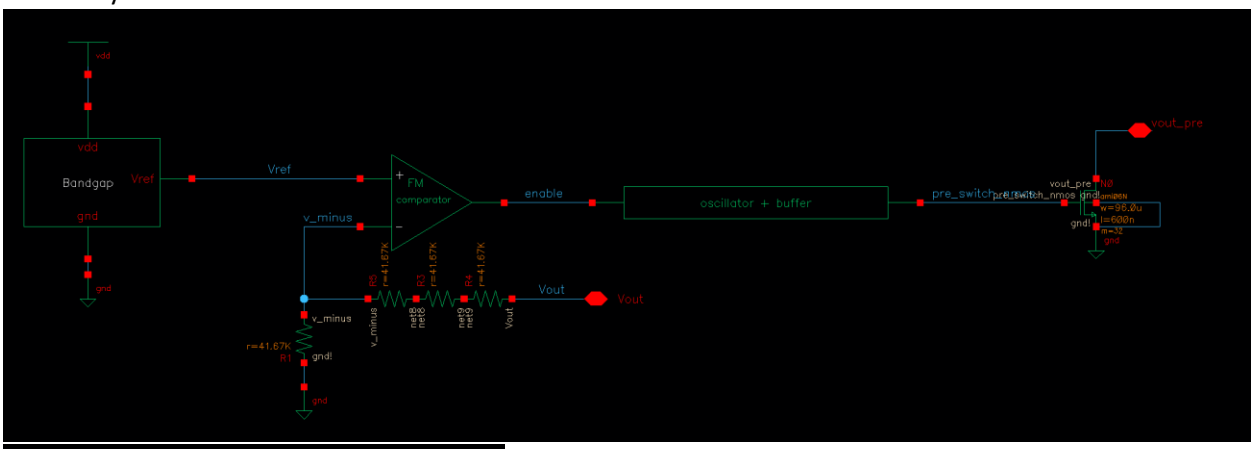
The values below are for the average current thorough VDD=4V and temperatures ranging from 0 to 100 degrees

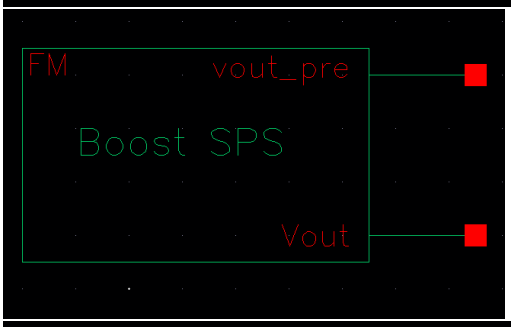


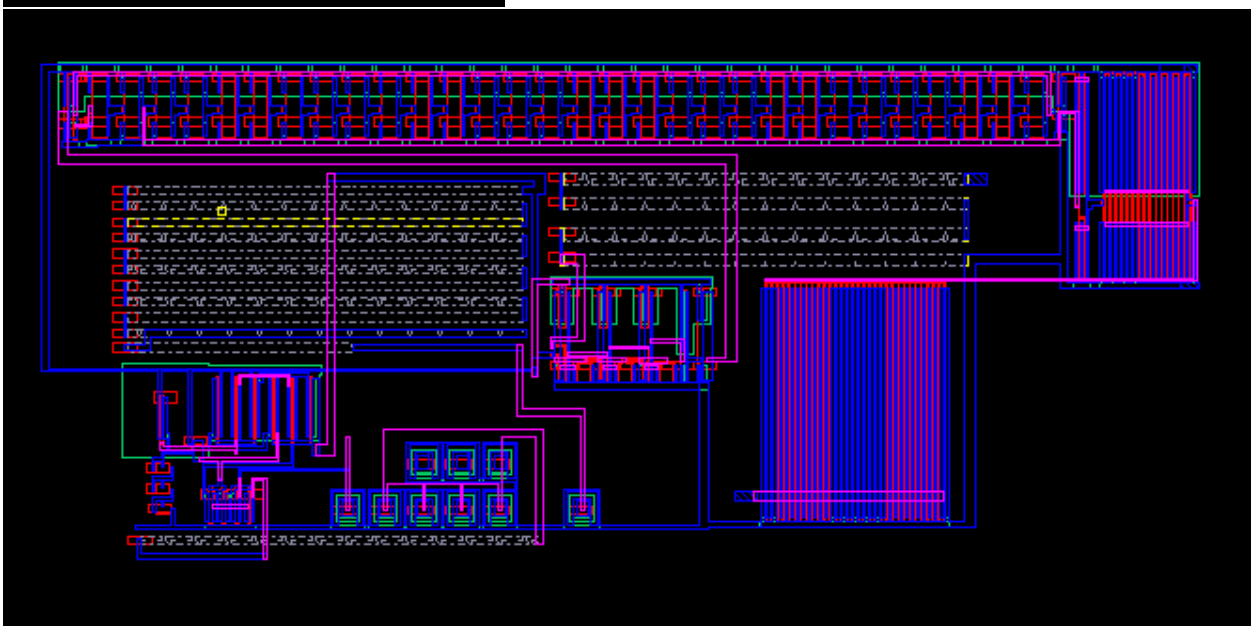
$$0\ de100\ degrees\ E\ = \frac{(Vout)(I_{Load})}{(VDD) * Avg(I(VDD))} = \frac{(5V)(50uA)}{(4V) * 497.3uA} = 0.125$$

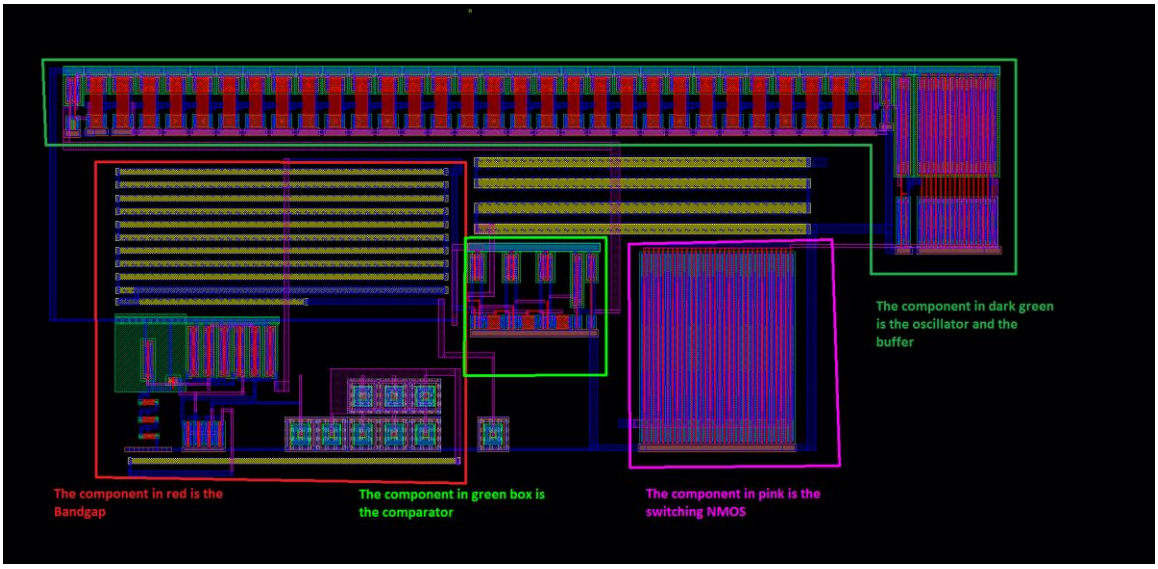
VDD=4V	Temp=0 C◦	Temp=25 C◦	Temp=50 C◦	Temp=75 C◦	Temp=100 C◦
Load current	Efficiency	Efficiency	Efficiency	Efficiency	Efficiency
$I_R = 50uA$	0.277	0.125	0.125	0.125	0.125
$I_R = 500uA$	0.277	0.269	0.324	0.305	0.277
$I_R = 1mA$	0.414	0.456	0.482	0.425	0.242
$I_R = 5mA$	0.747	0.768	0.781	0.764	0.612
$I_R = 20mA$	0.891	0.87	0.916	0.91	0.84

Below is the schematic and symbol along with the layout and the extracted view of the components that will be layout.



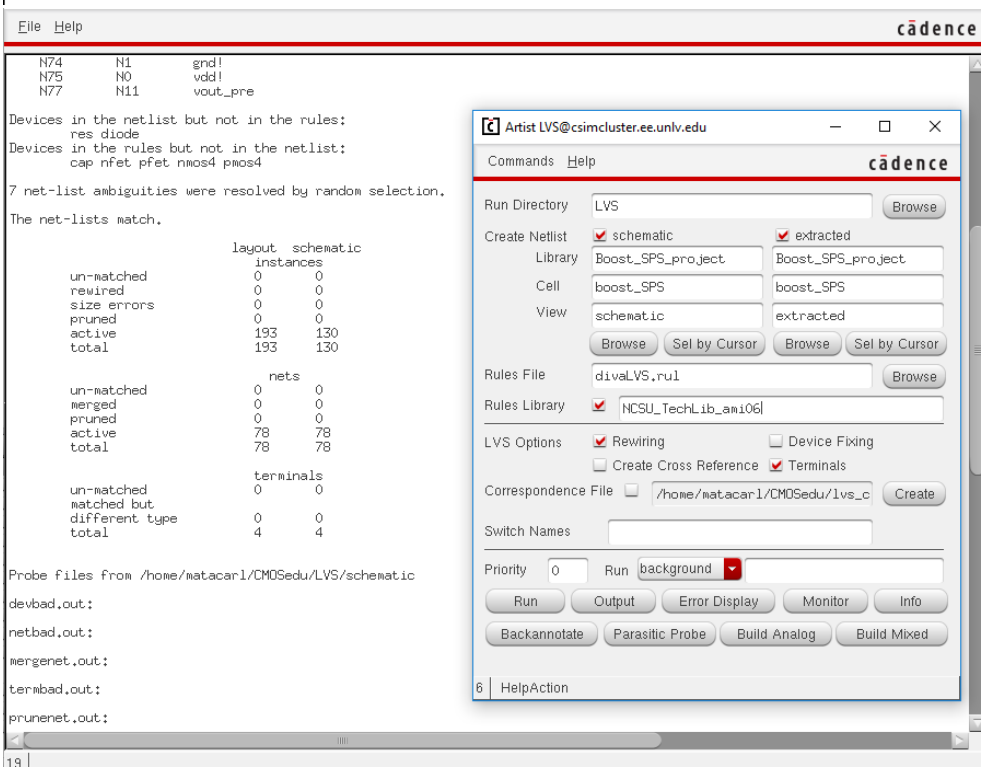




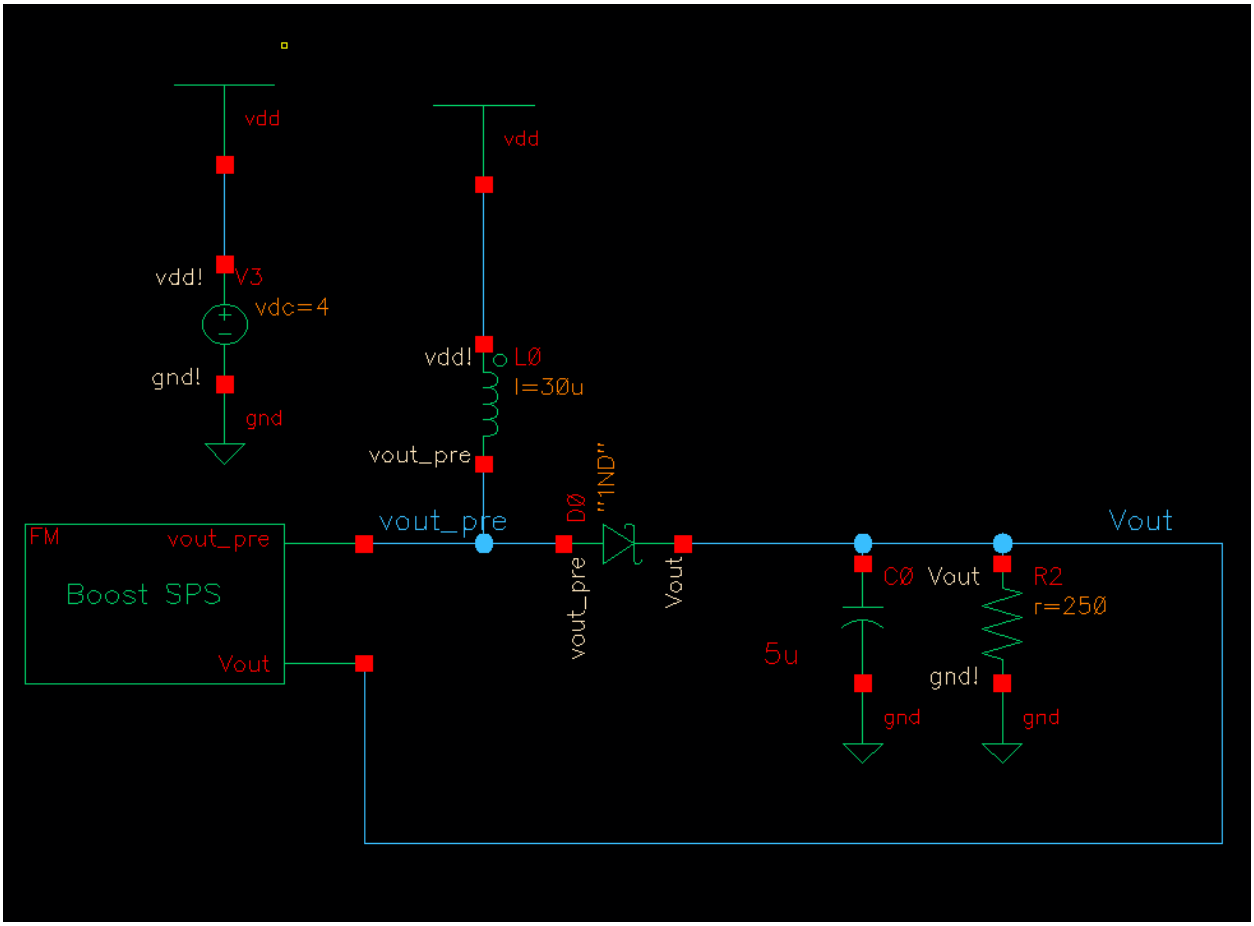


Below are the DRC and LVS for the Boost SPS

```
executing: drc(highresEdge elecHighresEdge (enc < (lambda * 2.0)) errMesg)
DRC started.......Fri Nov 30 15:03:54 2018
    completed ....Fri Nov 30 15:03:54 2018
    CPU TIME = 00:00:00  TOTAL TIME = 00:00:00
*********   Summary of rule violations for cell "boost_SPS layout"   *********
   Total errors found: 0
```



The full schematic is shown below. The symbol named Boost SPS is the on chip components and the inductor, capacitor, diode, and load resistor are off-chip components.



One of the most important trade off in this system is the sizing of the switching NMOS. We want small resistance (Rn) because of the desired small voltage drop, and the higher currents it can handle. However, the smaller the resistance, the larger the width of the NMOS becomes. This is an issue because, this means the layout of the NMOS will take a bigger area on a chip, minimizing the amount of components that can be fit on a chip. Also, if the Width of the NMOS becomes bigger, then its capacitance will also be large, which will cause for larger inverters or higher gains in the buffer, in order to drive the NMOS.

Another trade-off is the speed of the system. A certain number of inverters have to be used and sized to bring the frequency of the oscillator down. The higher the speed, the closer it will get to the component's delay. This can cause problems in the system.

Also, when it comes to loads and efficiency, the higher the current the higher the efficiency. Which means sizing up the right conductor for small loads, and capacitor for heavy loads, is important due to changes in the load and power dissipation.