EE 420 Engineering Electronics II and ECG 620 Analog IC Design
Op-Amp Design Project
Spring 2019
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MOSFET Parameters (VDD=2V), scale = 0.6μm			
Parameters	NMAS	PMOS	Comments
Bias Current, ID	11μA	11μA	
W/L	200/2	405/2	
Actual W/L	120μ/1.2 μA	243μA/1.2 μA	
VDS, sat and VSD, sat	50mV	50mV	
Vthn and Vthp	670mV	920mV	
VGS and VSG	720mV	970mV	
KPn and KPp	24 μA/V^2	5.8 μ/V^2	
$C'_{ox} = \varepsilon_{ox}/t_{ox}$	2.53 fF/μm^2	2.53 fF/μm^2	
C_{oxn} and C_{oxp}	364.3fF	737.7fF	
C_{gsn} and C_{sgp}	242.6fF	491.3fF	
C_{gdn} and C_{gdp}	23.9fF	70.3fF	
g_{mn} and g_{mp}	230(μA/V)	227(μA/V)	At ID= 11μA
r_{on} and r_{op}	9.1 MΩ	8.34 MΩ	
$g_{mn}r_{on}$ and $g_{mp}r_{op}$	2.093kV/V	1.893kV/V	
λ_n and λ_p	0.01V^-1	0.0109V^-1	

Result Summary				
	VDD = 2V		VDD = 5V	
	No Load	Load	No Load	Load
DC open loop gain	94.16 dB	79.2 dB	90.87 dB	78.8 dB
Gain-Bandwidth Product	1.76 MHz	2.22MHz	1.76MHz	2.15MHz
VDD	2V	3V	4V	5V
CMRR - 100kHz	102 dB	110 dB	111 dB	111 dB
PSRR, positive – 1kHz	82dB	80dB	79.8dB	79.9dB
PSRR, negative – 1KHz	61.7dB	60dB	58.7dB	57.5dB
Power Consumption	276μW	450μW	626μW	817μW

Device selection

The device width and length were chosen in respect to the threshold voltage and overdrive voltage. Looking at the C5 MOSFET text file we can see a threshold voltage that we can use with a chosen overdrive to come up with a VGS/VSG parameter. An overdrive voltage of 50mV was chosen for both the PMOS and the NMOS. A general way to start a design is to begin with an overdrive within 5% of VDD. Since we need to use a VDD that goes down to 2V, we can set this as the VDS, sat and VSD, sat, if we want the circuit to stay in saturation. The Threshold voltage for NMOS and PMOS are about 0.669V and 0.921V respectively. Adding the threshold and overdrive values, results in the VGS and VSG parameters. Those two values come to be about 0.7196V (VGS) for the NMOS and 0.9714 (VSG) for the PMOS. The length for both devices is 2 times bigger than the minimum length (0.6um), so the length is 1.2um. A test set up was used to find the width, which is shown below in figure 1.

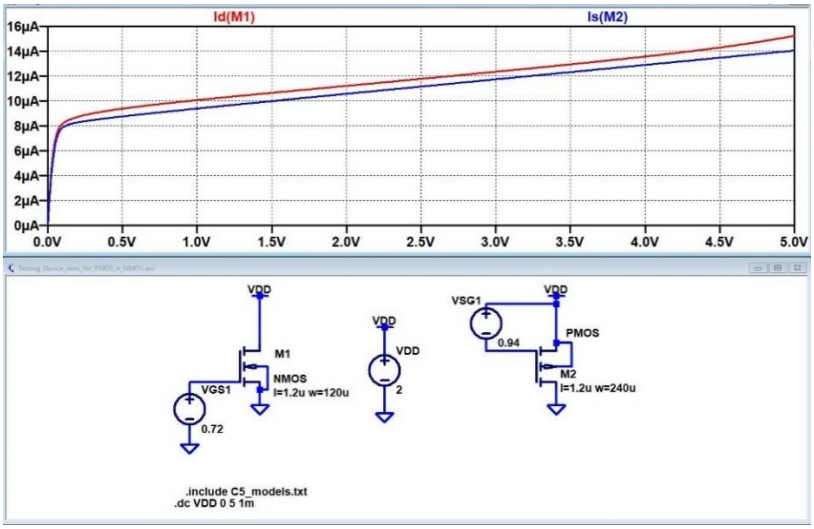


Figure 1

Creating the basing circuit

The first step to create the bias circuit is to design a beta-multiplier. For this case a diff-amp is being used to add resistance and to keep the Vbias node and V_r node at the same potential in order sink and source the same current and keep it constant after saturation. Since the multiplier for the BMR is 4, we can use a resistor that is equal to 1/gm but the resistor value used is lower because the results seemed to be better. A PMOS was used as capacitor from Vbiasp to VDD in order to add stability. Since the PMOS have larger width and are in parallel with the capacitor, which add more stability, it would be wise to use the Vbiasp to bias the current mirrors for the rest of the reference voltages. The schematics below show the start-up circuit, BMR with diff-amp, and the reference voltages.

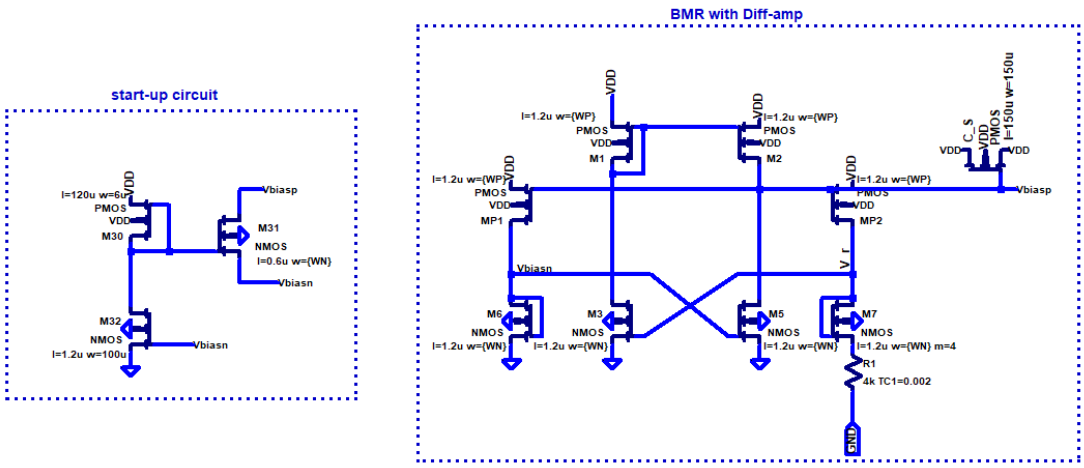


Figure 2

Figure below shows that the currents flowing through M4, M7, MP1, and MP2 are the same which should be expected.

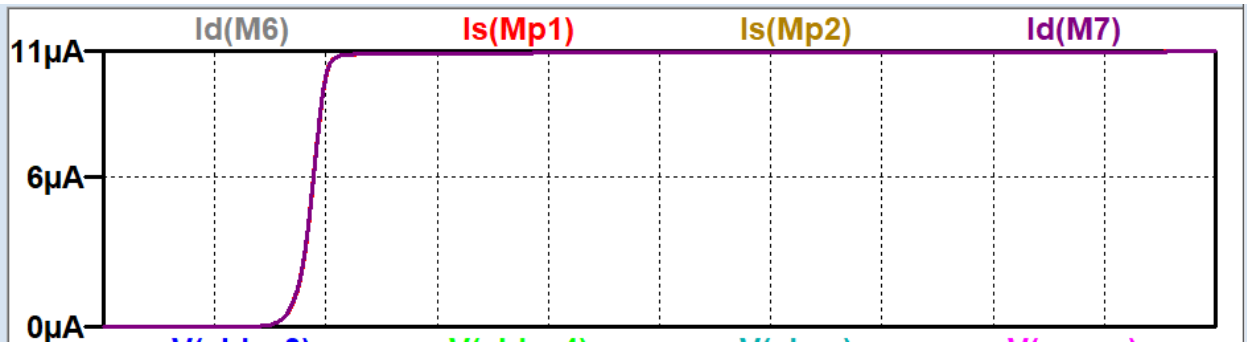


Figure 3

Calculations: VDD=2V

$Vbiasp = VDD - VSG = 2 - .97 \simeq 1.03V$

$Vbias1 = VDD - VSG = 2 - .97 \simeq 1.03$

$Vbias2 = VDD - VSG - VSD, sat = 2 - .97 - 0.050 \simeq 0.980V$

$Vbias3 = VDS, sat + VGS = \ .050 + .71 \simeq 0.770V$

$Vbias4 = VGS = 0.72V$

$Vpcas = VDD - 2VSG = 2 - 2(0.97) \simeq .060V$

$Vhigh = VDD - VSD, sat = 2 - .050 \simeq 1.95V$

$Vncas = 2(VGS) = 2(.72) \simeq 1.44V$

$Vlow = VDS, sat \simeq \ .05V$

$Vbiasn = VSG \simeq .72V$

The figures below show the schematic and the simulation plot of the voltages, which are to be used as the bias/reference voltages and are mirroring the beta-multiplier

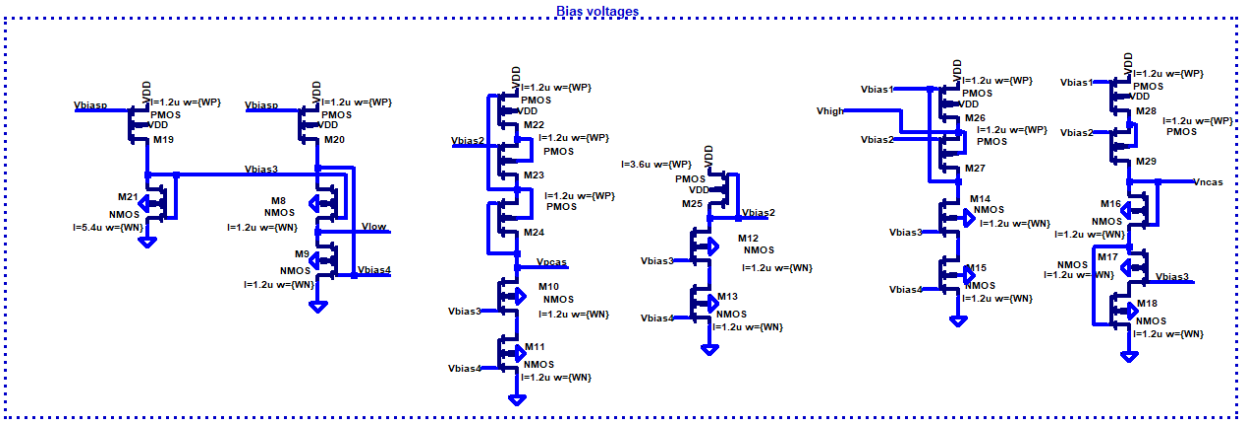


Figure 4

The figure below shows the current being mirrored through each branch of the bias circuit, which is about 11.25uA.

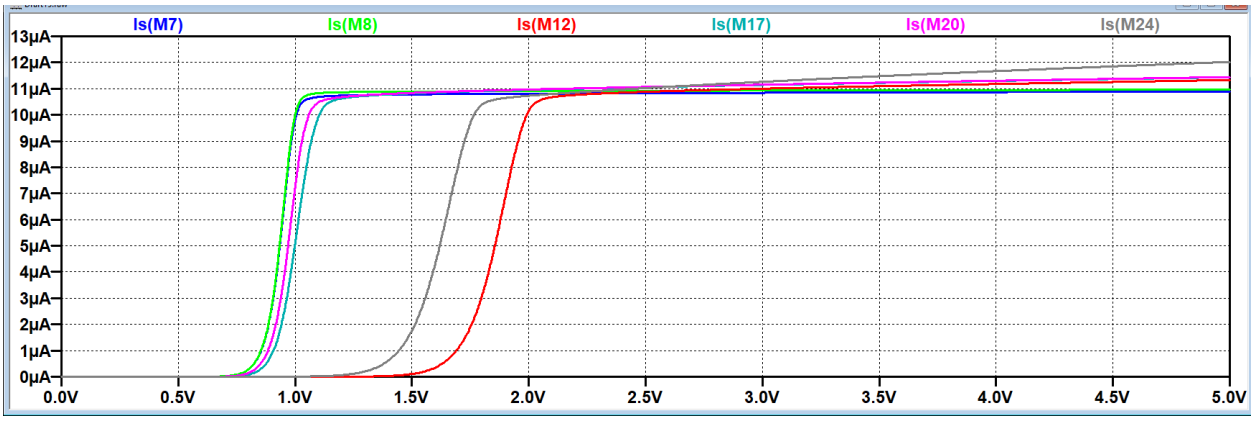


Figure 5

Op-amp topology

The op-amp topology used for this project is the folded-cascode with class AB output buffer. This op-amp is based from the Operational Transconductance Amplifier (OTA). A simple OTA can be represented as a differential amplifier with a current mirror. From this base topology the rest of the circuit get developed. This circuit has been folded-cascoded for several reasons. By making the OTA a cascoded current mirror the output resistance increases, which also increments the low frequency gain. Now, if we applied the folded-cascoded stack topology along with an AB output buffer, the input common-mode voltage range and output swings get enhanced. The class AB buffer helps the circuit to improve its speed by turning on and off the MOSFETs depending on the amount of current being pulled. Either-one can be on at a single time or both; this part of the circuit is also called the push-pull stage.

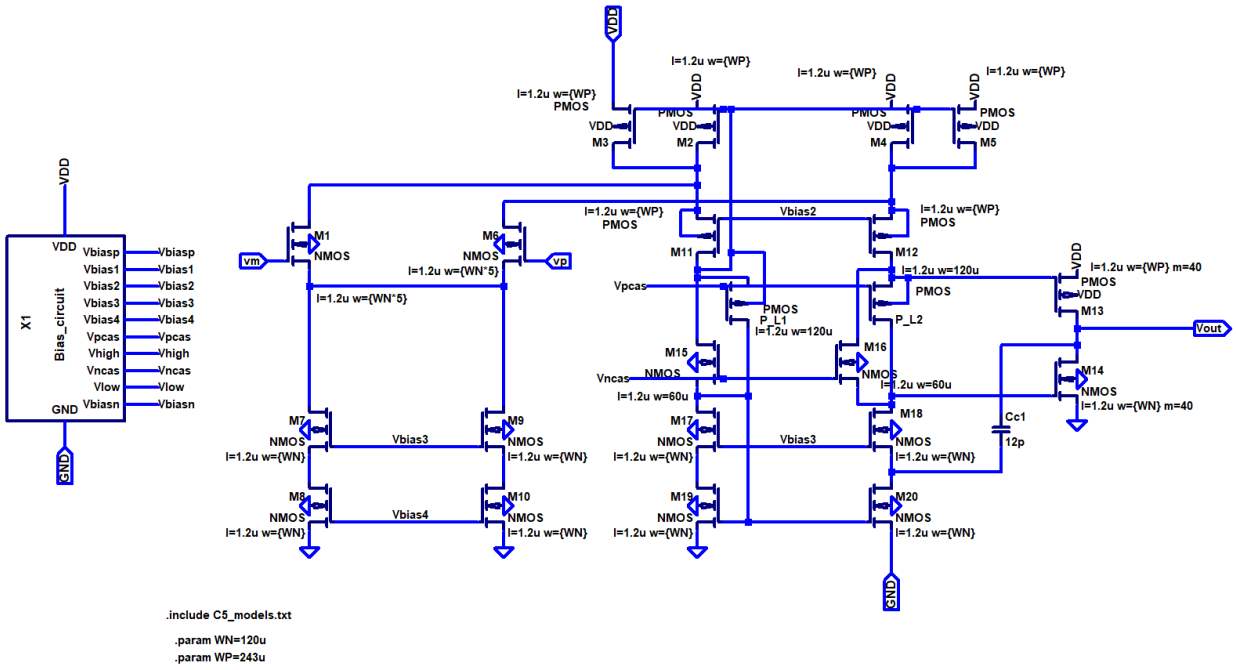


Figure 6

Because we have a cascaded OTA and an AB buffer stage, the low frequency gain is the multiplication of the differential amplifier gain and the push-pull stage.

Low frequency open loop gain of this op-amp topology:

$$A_{OLDC} = gm_n * (R_{ocasn} || R_{ocasp}) * (gm_n + gm_p) * (r_p || r_n)$$
$$= between\ 90dB\ to\ 95dB, for\ VDD\ ranging\ from\ 2V\ to\ 5V$$

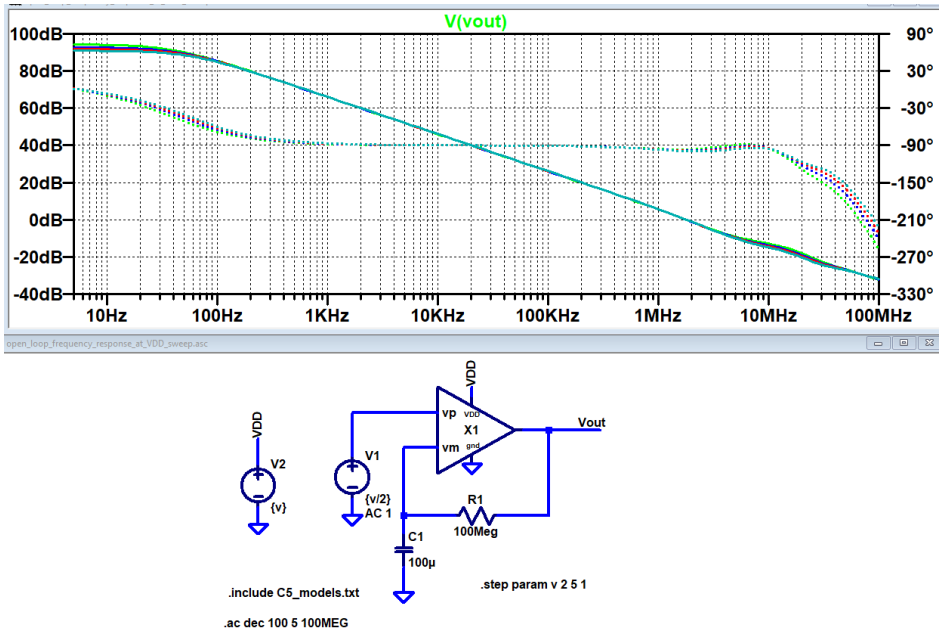


Figure 7

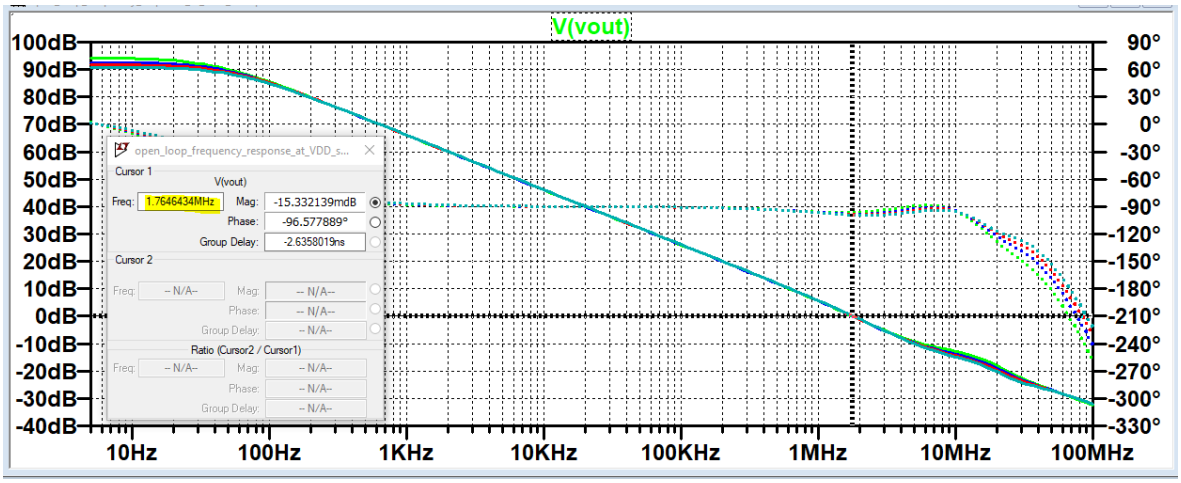


Figure 8

Input Common-Mode Range

$V_{CMMIN} = 2(VDS, sat) + VGS \simeq 0.914V$

$V_{CMMAX} = VDS \geq VGS - V_{thn}$

$VD \geq VG - V_{thn}$

$VD = Vbias2 + VSG \simeq 1.908V$

$VD \geq VG - V_{thn}$

$VD + V_{thn} \geq VG$

$1.908 + V_{thn} \geq VG$

$2.6V \geq VG$

DC open-loop gain with 1kΩ and 100pF load

VDD voltage range: 2V < VDD < 5V

Under all load, the open-loop gain is above 66dB with the varying VDD specified above.

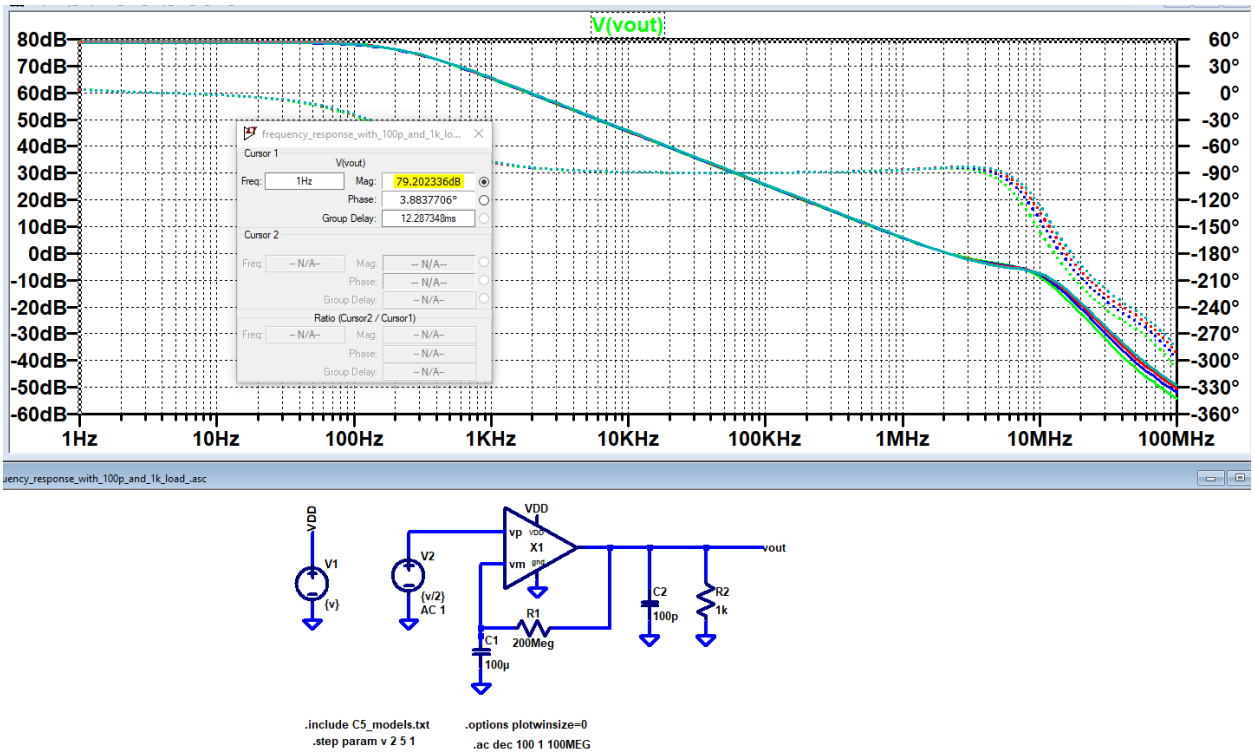


Figure 9

Unity Gain Frequency

$$f_{un} = \frac{gm_2}{2\pi * C_c} = \frac{227u}{2\pi * 12pF} \simeq 3.0MHz$$

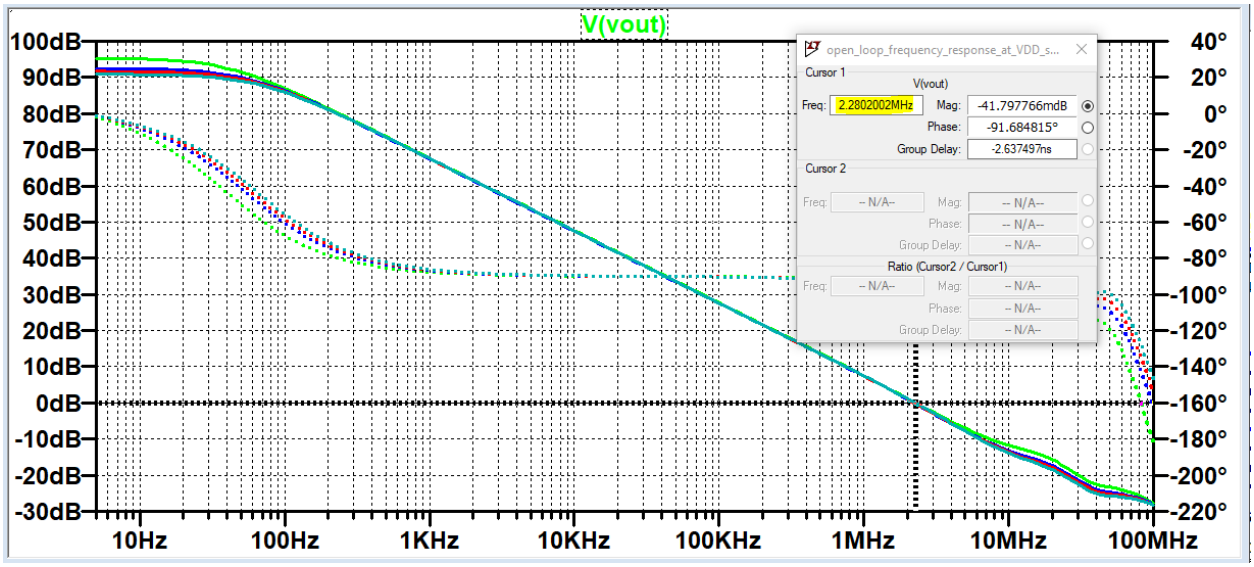


Figure 10

The Gain-bandwidth product meets the requirements given.

Testing the output of the op-amp using the inverting and non-inverting topology

Because we have a class AB buffer (push-pull) on the output stage, the output can swing from VDD to ground. The reason for this is because the output stage mirrors the floating currents and multiplies itself times its width. The first plot below shows the loads being tested using the inverted topology with a gain of 20, which means the input signal of 100mV is being increased to 2V. Because the common node is at 1V, and VDD is at 2V the output rails at 2V and 0V (VDD and ground).

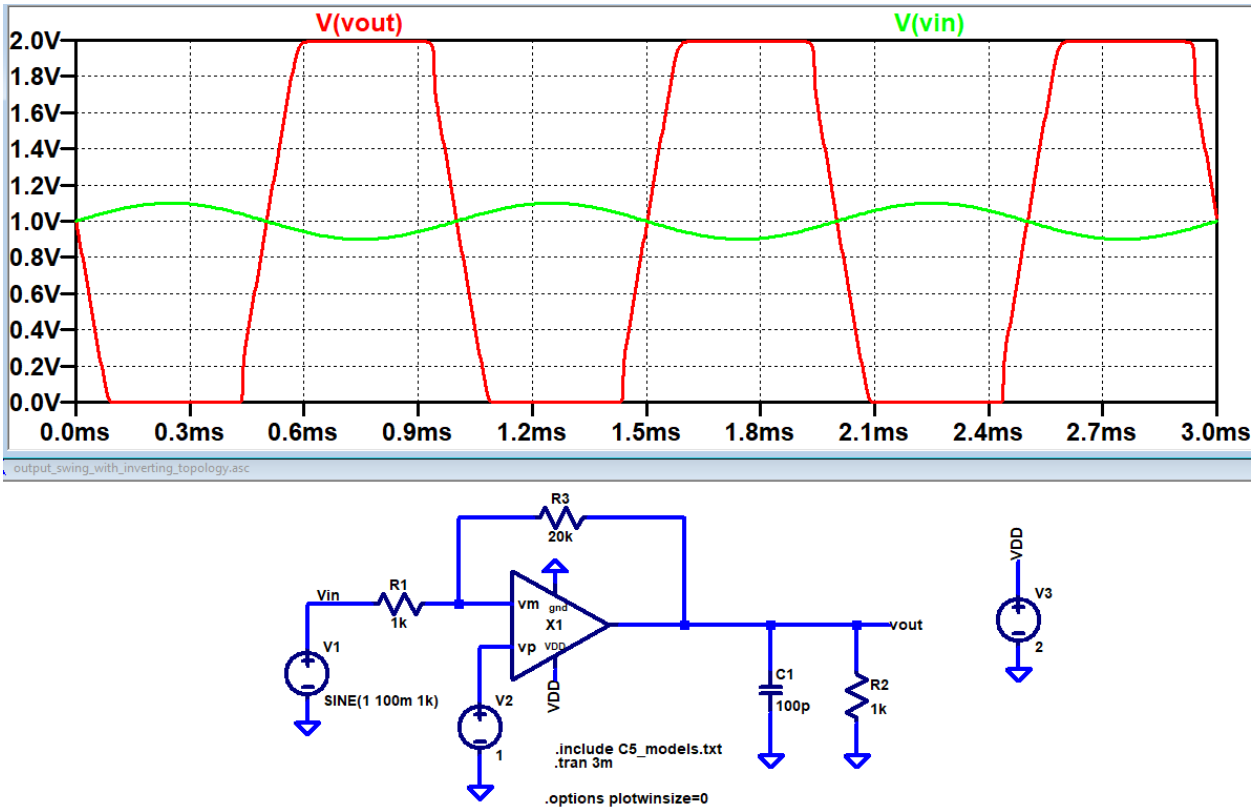


Figure 11

The next plot below shows the circuit being tested using the non-inverting input. For this test the input has been minimalize in order to see the gain of the output without railing. As we can see, the gain of the input is close to 20 since the Rf is 19k and Ri is 1k, and by using the non-inverting formula we should be seeing an output swing of about 200mV. Thus, the output is in phase with the input and is about 20 times larger than the input.

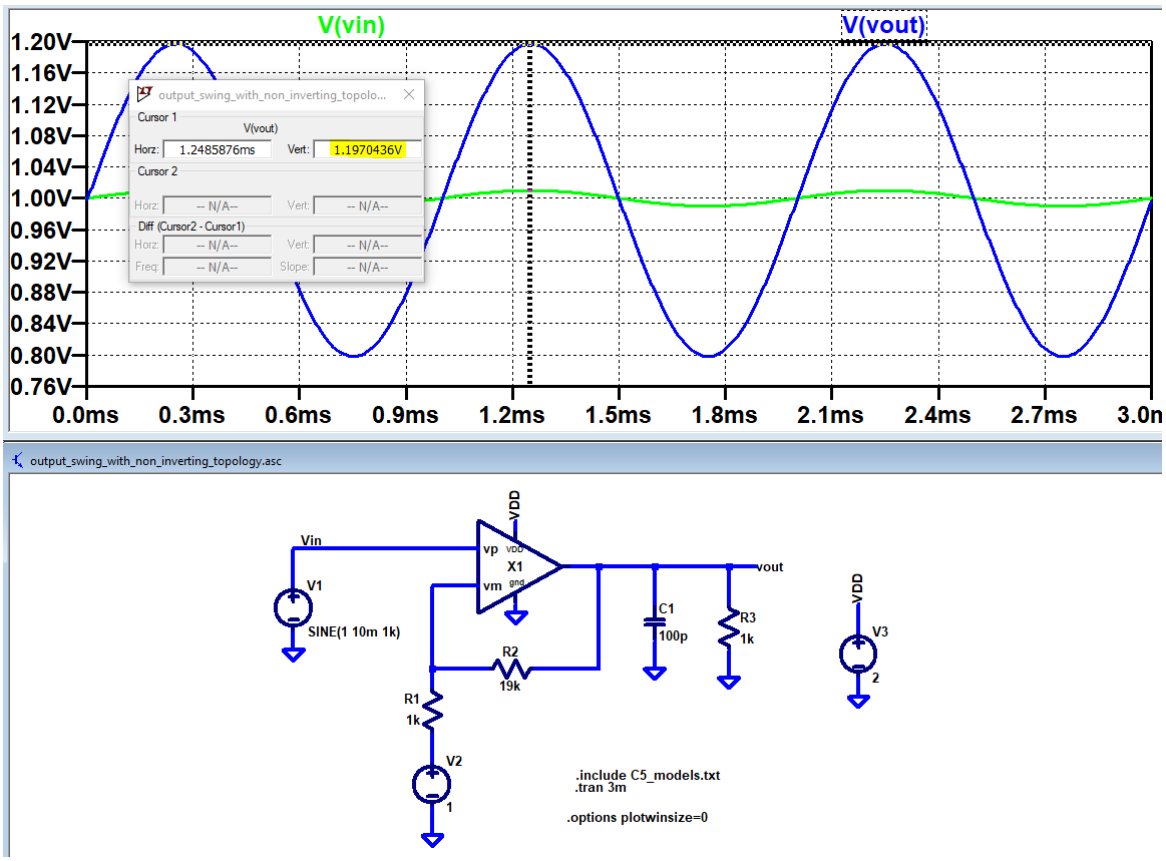


Figure 12

Testing for Slew Rate

Below are two figures showing different slew rates. The first one is with a 12p Cc capacitor, which is the value I have been using to test all the other plots. This plot does not meet the minimum requirement of 1V/us. The second plot meets the requirement, but the compensation capacitor had to be decreased. If we want to improve the slew rate and the ringing then we need to decrease the value of the Cc capacitor even more and move the phase towards 90 degrees, so it behaves as an first order RC circuit.

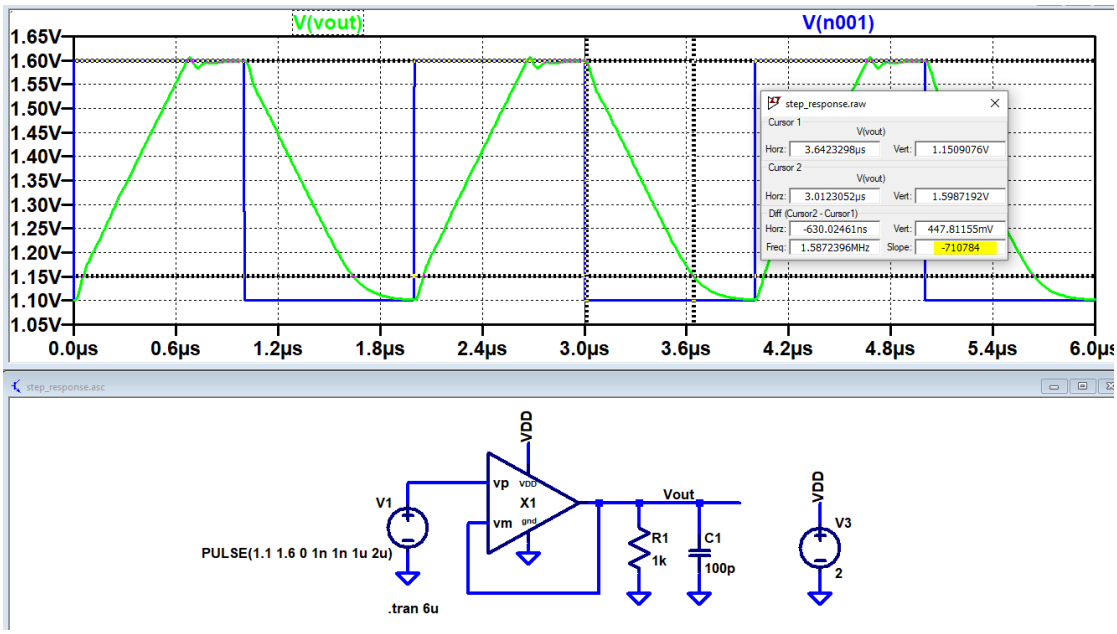


Figure 13

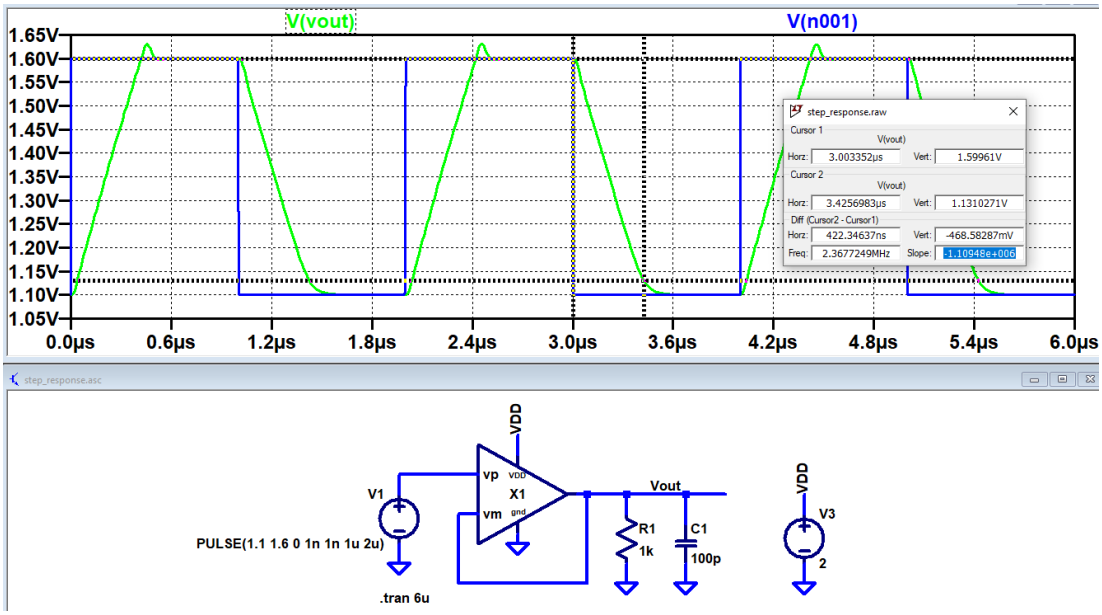


Figure 14

Common-Mode Rejection Ratio (CMRR)

Below we can see that at 100kHz the CMRR ratio is higher than 90dB, so this circuit meets the requirement. The power supply is being swept 1V per step and we can see from the plot below that from 2V to 5V the requirement has been met.

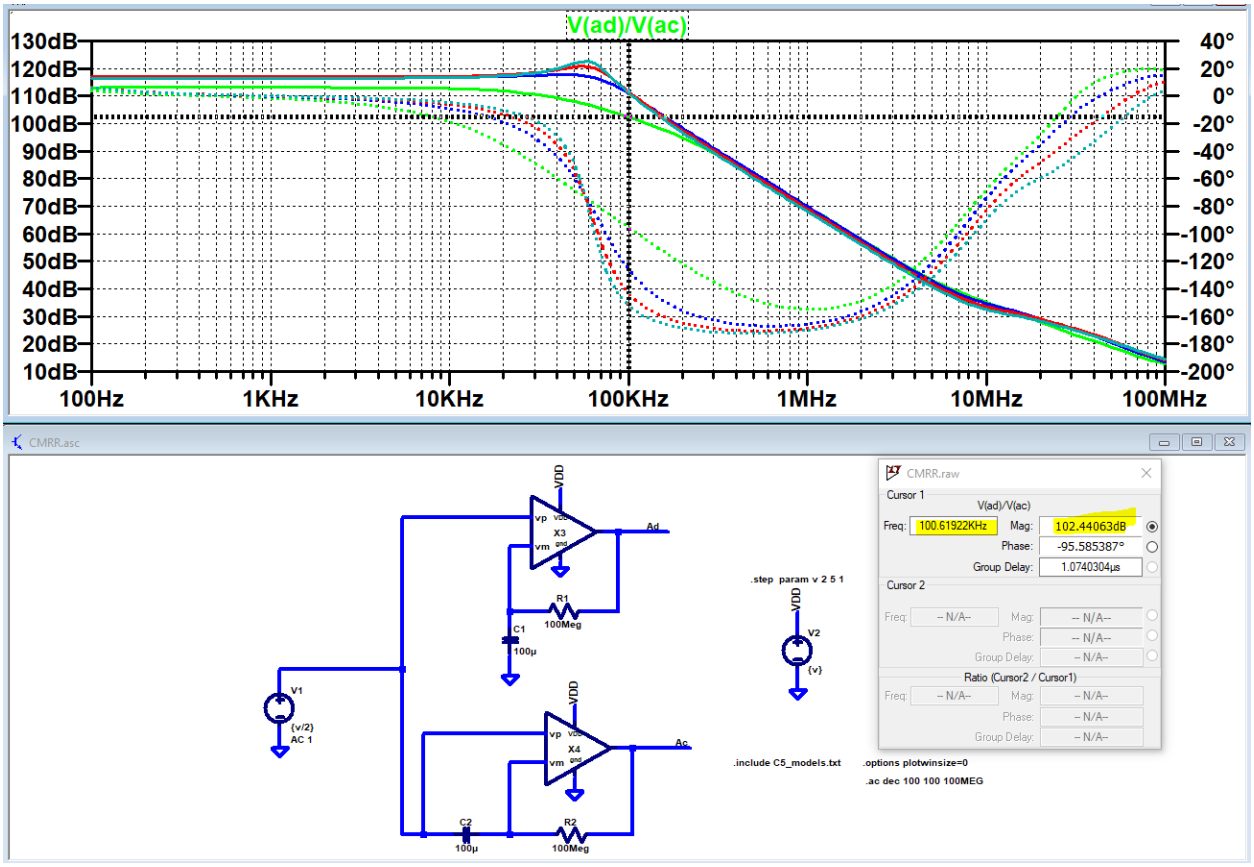


Figure 15

Power Supply Rejection Ratio (PSRR)

A rejection ratio greater than 60dB at 1kHz must be met to satisfy this requirement.

Two tests are being set for this ratio, one the positive PSRR and the negative PSRR. Testing for the positive ratio a small signal is sent through VDD, and the output is divided by the same circuit without the small signal.

The plot below shows positive PSRR ratio gain.

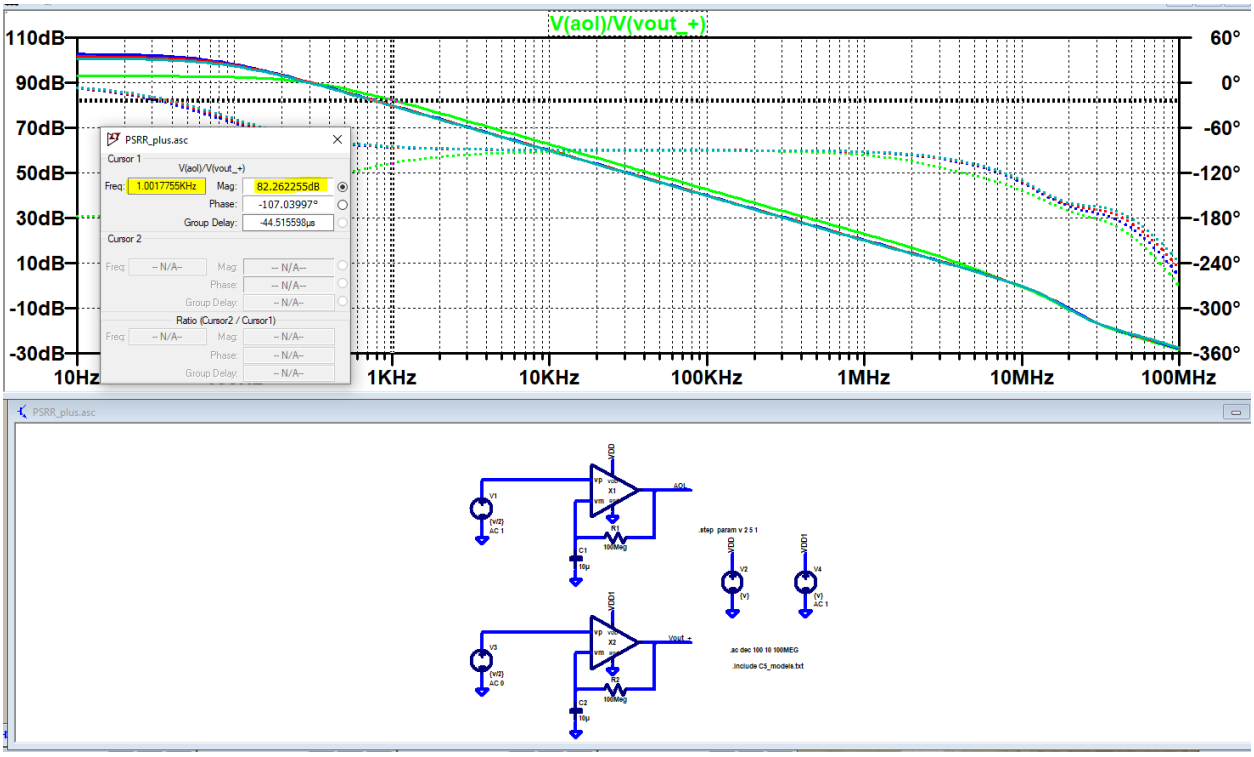


Figure 16

The plot below shows the negative PSRR with a ratio of about 61dB

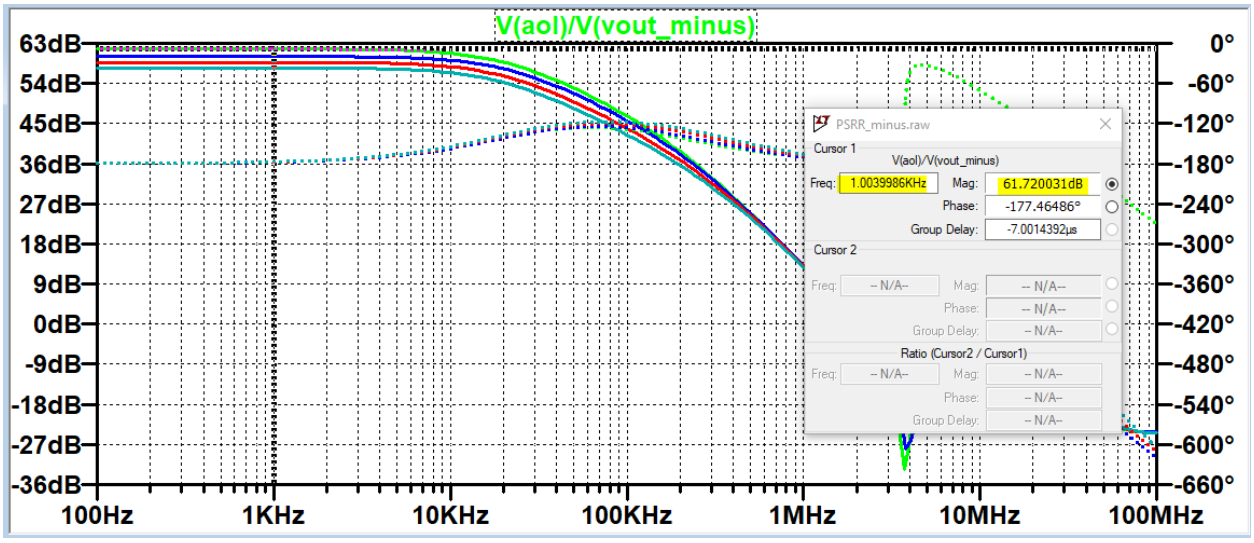
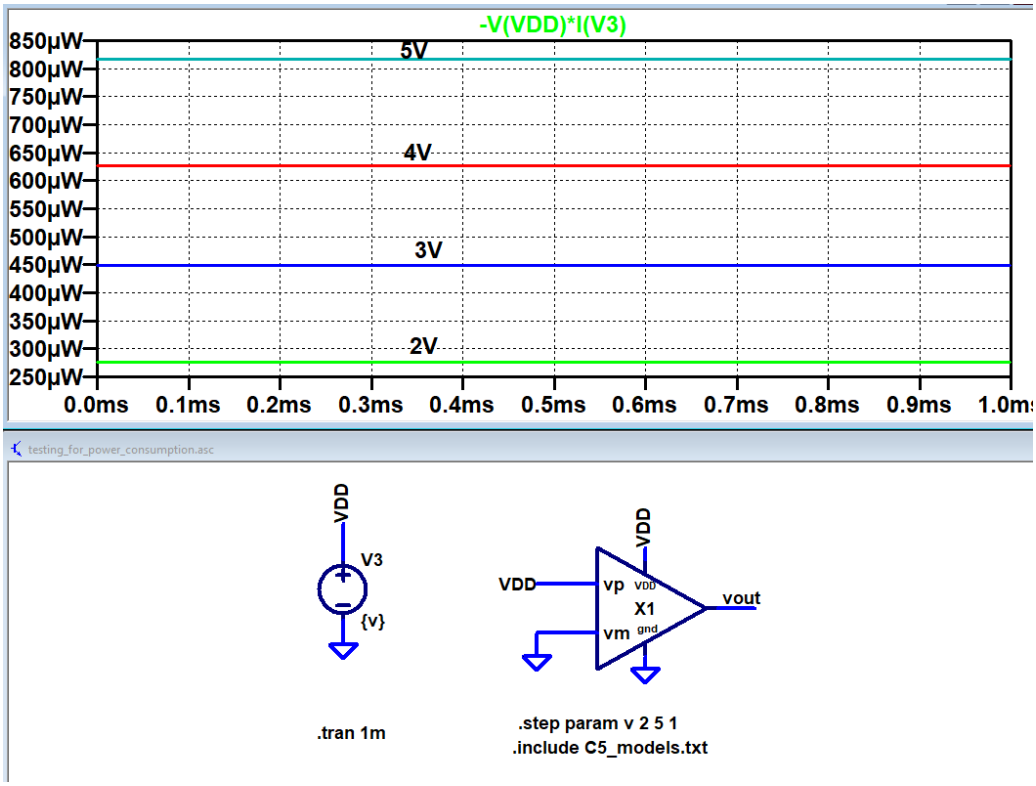


Figure 17

Power Consumption

The power supply is being varied with 1V steps, from 2V to 5V.



Encountered problems

One major problem I encountered was my design going from working and passing most requirement one day to failing all of them the next day. Then the next few days I spent trying to make it work, and when it started working properly, LTspice crashed and when I reopened my files, again the circuit did not work. Finally, at the last minute I was able to put something together that pass some of the requirements. But it could be better.

Future improvement

Make changes to the compensation capacitor and indirect feedback to make the system more stable. Decrease sizes to save space on a chip. Understand pole splitting better to make changes to f1 and unity frequency. Make improvements to the floating currents and understand how to properly apply gain-enhancement techniques. Make enough time to run and understand temperature behavior of the circuit.

Summary

The results for the DC open-loop gain were all satisfactory. The gain response is for VDD varying from 2V to 5V is above 66dB, with load and without load. The gain-bandwidth product stays over 1MHz with load and without load. CMRR also meets the requirement of 90dB at 100KHz for 2V<VDD>5V. Positive PSRR stays above 60dB but negative PSRR comes short at 1KHz. The slew-rate of the circuit does not meet the requirement of 1V/μs. The power consumption stays below 1mA under quiescent conditions.