MAY 3, 2016

COURSE PROJECT: VOLTAGE FOLLOWER

EE 420 ENGINEERING ELECTRONICS II

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1. Course Design Project : Voltage Follower

The course design project for EE 420 Electronics Engineering II requires the design of a voltage follower using an operational amplifier. The voltage follower is important for buffering or isolating low impedance loads from voltage sources. This topology allows a power source to avoid being loaded down by a resistance. The goal of the project is to design a voltage follower with marginal internal impedance and thus low current usage, yet able to output the full voltage input. This strategy allows the voltage follower to act as an ideal voltage source. Detailed design considerations will be presented in the following sections of this report. To begin, the design parameters are presented below:

Using On's C5 process (process information can be found at On's website, minimum L is 600 nm, SPICE models are found in C5_models.txt) design a voltage follower using an op-amp (input voltage connected to the noninverting, "+," input of the op-amp and output voltage connected back to the inverting, "-," input of the op-amp) that can operate with a VDD between 3 and 5 V while driving a 10 pF (max) and 1k (min) load.

Other requirements are:

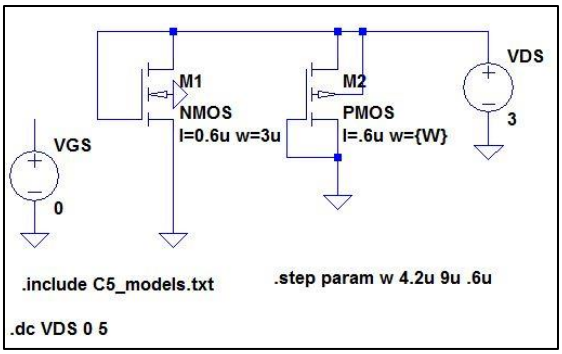
- The error (difference) between the input signal and output signal should be < 0.1%
- Bandwidth of the follower should be > 100 MHz
- Slew-rate with maximum load > 100V/microsecond
- Current draw from VDD should be less than 10 mA under full load conditions
- Output swing should be 80% of VDD (e.g. 0.5 V to 4.5 V when VDD = 5 V or 0.12 V to 2.88 V when VDD = 3 V. The output swing doesn't have to be centered as these examples are, that is, 0.25 to 4.25 V when VDD = 5 V is fine too).

2. Design Process

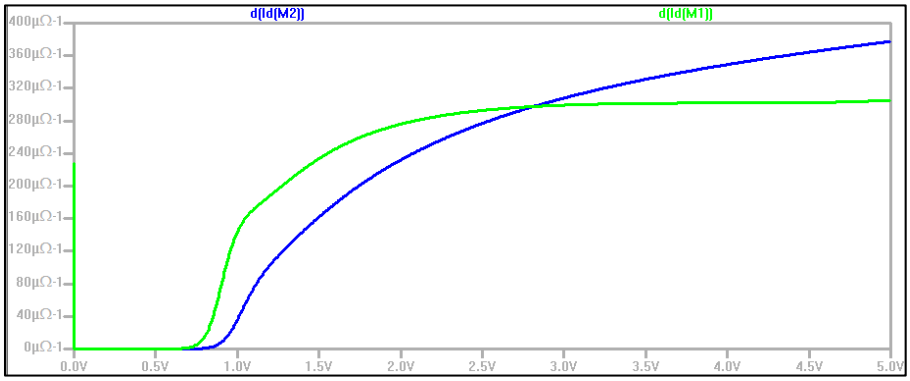
A. Selection of Lengths and Widths

The design strategy decided upon for this project utilizes a two stage operational amplifier consisting of two wide-swing folded cascode differential amplifiers for stage one with a push-pull amplifier for stage two. The operational amplifier stages will be biased via a Beta-Multiplier Reference (BMR) circuit.

The first step in the process was characterizing the On C5 models to select a biasing current, length and width. The minimum length of 600nm was selected, ideally to allow for a large enough transition frequency to meet the minimum bandwidth requirements when driving a load. The initial length was selected at 3um, a ratio of 5, with the understanding that the width can be scaled later if necessary. To select a PMOS width, a sweep of I_D versus V_{DS} and V_{SD} was performed on the same plot while also sweeping the width of the PMOS. Taking the derivative of the drain currents allowed a comparison of the transconductances, g_m , of both devices to attempt to match the g_m. Based on this method of iteration, the width of the PMOS was selected at 4.8um with length 600nm, a ratio of 8. This was not the recommended method for determining the width of the PMOS, where this would normally be 2-3 times the width of the NMOS, but seemed like a valid method for attempting to match the devices. The circuit and simulation are seen below. The related file is in titled IDvVDS_GM_Sweep.



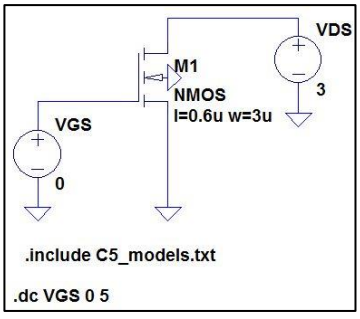
I_D vs V_{DS} and I_D vs V_{SD}



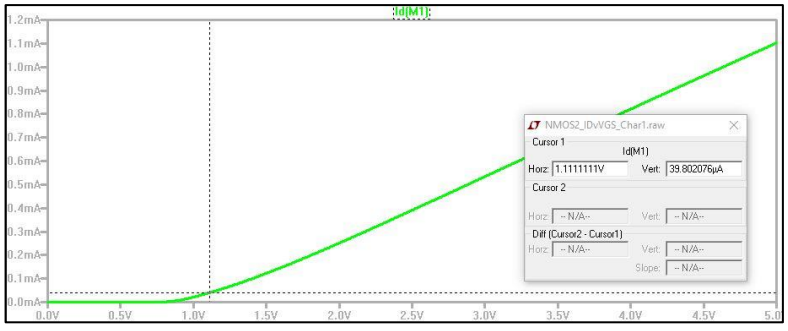
The image above displays the closest match of the transconductances, g_{mn} and g_{mp} , as well as a range for each based on VDD. All the values for both devices will be included in tables at the end of each device characterization.

B. NMOS Characterization

To begin the NMOS characterization, an I_D versus V_{GS} sweep was performed to select a bias current. The selected bias current was 40uA at V_{GS} = 1.11V and V_{THN} = 750mV. The goal is to keep the BMR bias current low to reduce current draw from VDD. The circuit schematic and waveform are displayed below. The related file is titled NMOS2_IDvVGS_Char1.

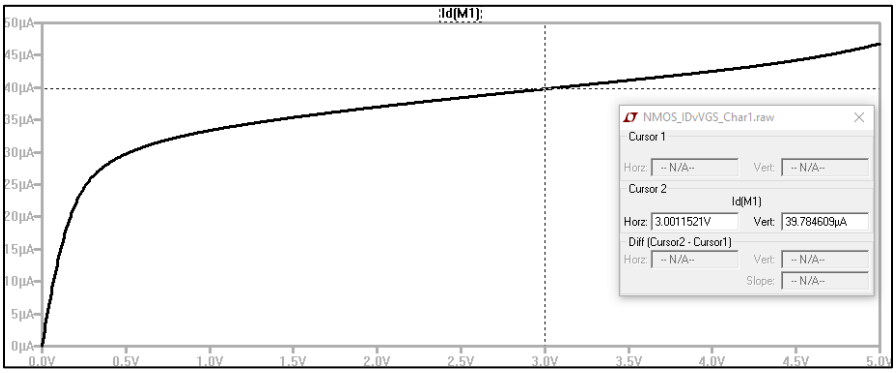


I_D vs V_{GS}



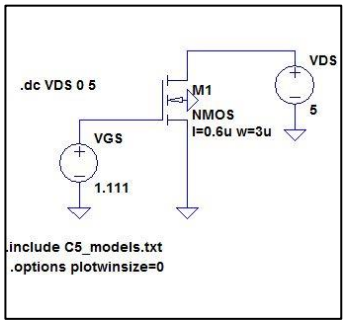
Bias current selected at 40uA with V_{GS} at 1.11V

The waveform below displays the I_D vs V_{DS} sweep demonstrating the device is in saturation at the selected bias current for VDD ranging from 3V to 5V. The related file is titled NMOS2_IDvVDS_Char1.

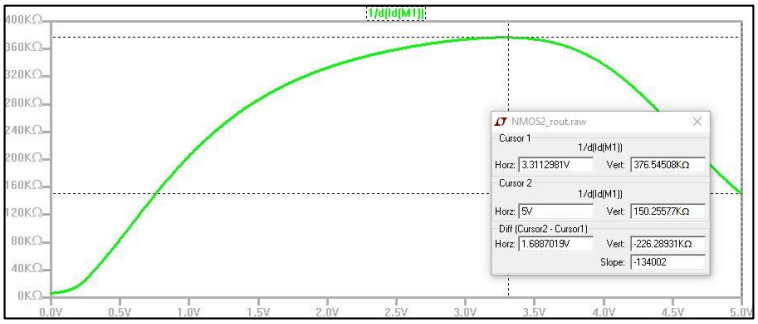


At I_D = 40uA NMOS is in saturation at VDD ≥ 3V

The next parameters determined were the output resistance, r_{on}, and $V_{DS,SAT}$. These were determined via the following schematic and waveform. The relate file is titled NMOS2_rout. A table containing the range of values for r_{on} will be included at the end of this section.



Schematic



Waveform displaying values of r_{on} and $V_{DS,SAT}$

$V_{DS,SAT}$ can be estimated as the point where the output resistance begins to enter saturation on the above waveform. An operating point simulation was performed to record a range of values for $V_{DS,sat}$ and g_{ds} over 1V increments from 0V to 5V. An estimate of 270uA/V will be used as an average value for $V_{DS,SAT}$. The operating point simulations included the added feature of recording a range of values for g_{mn}. The low and high range of these values are displayed below with a full set of values included at the end of this section. An average value of 180uA/V will be used to approximate g_{mn}.

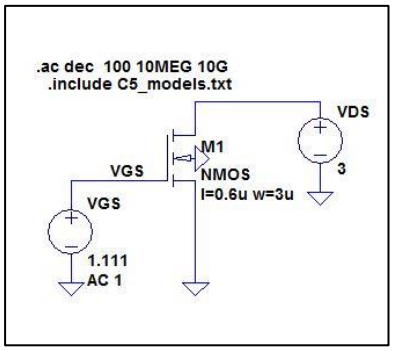
Name:	m1
Model:	nmos
Id:	3.39e-05
Vgs:	1.11e+00
Vds:	1.11e+00
Vbs:	0.00e+00
Vth:	7.22e-01
Vdsat:	2.56e-01
Gm:	1.69e-04
Gds:	4.42e-06
Gmb	4.41e-05
Cbd:	0.00e+00
Cbs:	0.00e+00
Cgsov:	5.01e-16
Cgdov:	5.01e-16
Cgbov:	5.28e-16
dQgdVgb:	4.24e-15
dQgdVdb:	-4.81e-16

Low range of $V_{DS,SAT}$

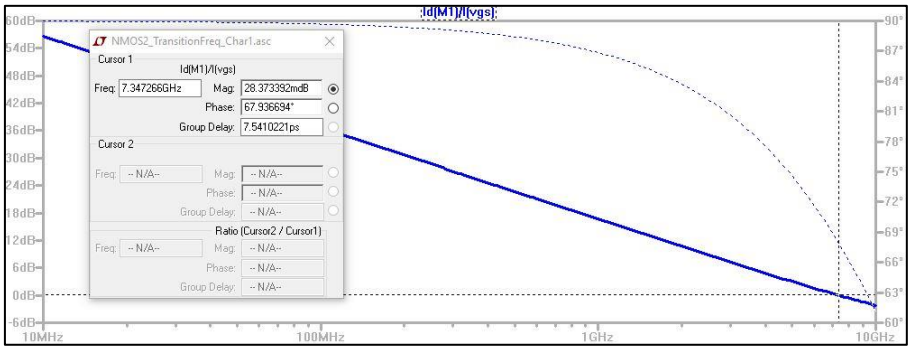
Name:	m1
Model:	nmos
Id:	4.68e-05
Vgs:	1.11e+00
Vds:	5.00e+00
Vbs:	0.00e+00
Vth:	6.74e-01
Vdsat:	2.81e-01
Gm:	1.94e-04
Gds:	6.67e-06
Gmb	5.00e-05
Cbd:	0.00e+00
Cbs:	0.00e+00
Cgsov:	5.01e-16
Cgdov:	5.01e-16
Cgbov:	5.28e-16
dQgdVgb:	4.24e-15
dQgdVdb:	-4.80e-16

High range of $V_{DS,SAT}$

The final parameter characterized for the NMOS was the transition frequency. The design needs to have enough bandwidth to meet the minimum requirement of 100MHz while driving a 10pF maximum and 1kΩ minimum load. Selecting the minimum length of the device should allow for enough bandwidth once this load is added to the amplifier. As a result of the device sizing selected, the transition frequency, f_T, of the NMOS is approximately 7.3GHz, as seen in the waveform below. The related file is titled NMOS2_TransitionFreq_Char1.



Transition Frequency Test Circuit



NMOS Transition Frequency at 3um/600nm

The following tables contain a summary of the NMOS values obtained for this design project.

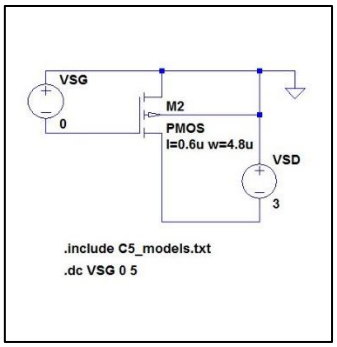
NMOS Characteristics	
W/L = 3um/600nm	Ratio = 5
I_{bias} = 40uA	
V_{thn} =0.750V	
V_{GS} = 1.11V	
V_{OVN} = 1.11-0.750 = 0.360V	
$V_{DS,sat}$ = 270mV approx	

VDD (V)	r_{on} (Ω)	g_{ds} (A/V)	g_{mn} (A/V)
0.00	6.11k	164u	0.00
1.00	205k	4.87u	167u
2.00	332k	3.01	177u
3.00	373k	2.68u	182u
4.00	337k	2.96u	186u
5.00	150k	6.68u	194u

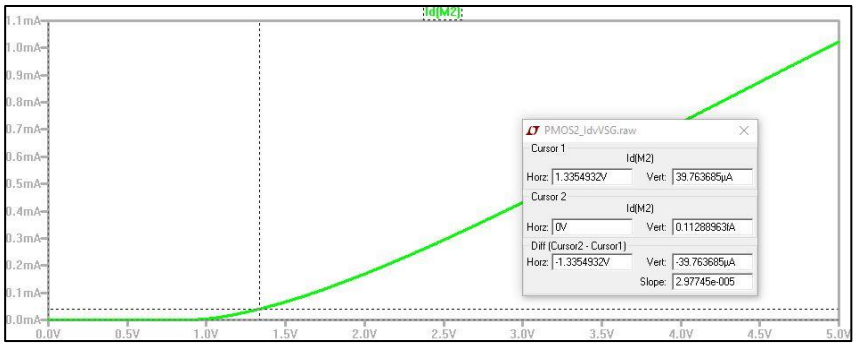
Sample values of interest from NMOS simulations

B. PMOS Characterization

The same process outlined above was followed for the PMOS. Recall, the initial width/length was set to 4.8um/600nm. The results of the PMOS characterization are detailed in the waveforms and tables below.

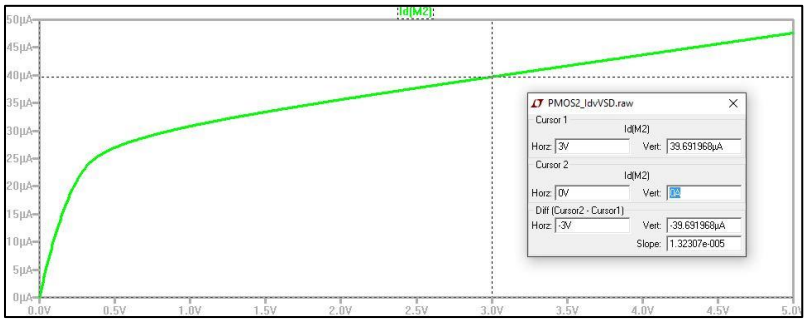


PMOS Circuit



I_d vs V_{SG} Curve

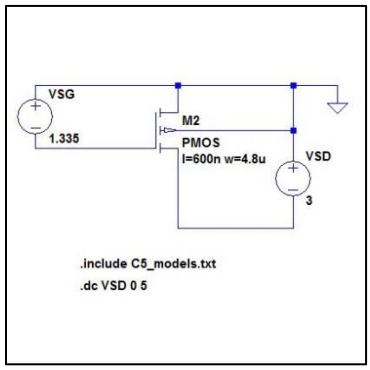
The waveform above displays the selected bias current, 40uA, and the corresponding value of V_{SG}, 1.335V. This will serve as V_{bias1} in the design. The threshold voltage was also measured at 840mV from this simulation. The related file is titled PMOS2_IdvVSG.



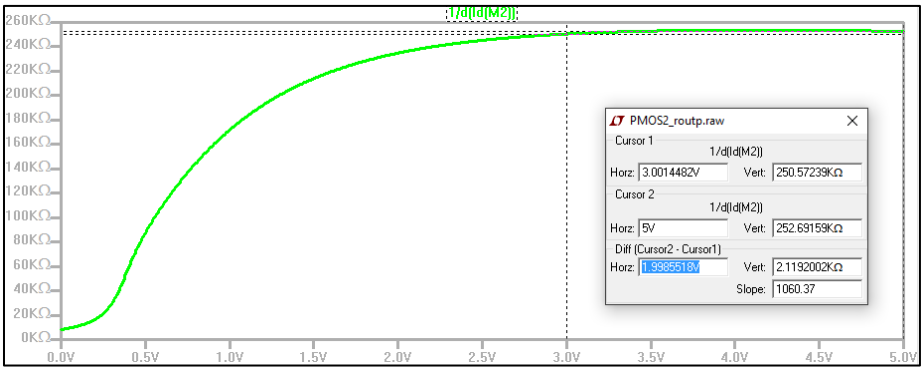
I_d vs V_{SD} Curve

As with the NMOS, the waveform above displays the PMOS operating in saturation between 3VDD and 5VDD at the selected bias current. The related file is titled PMOS2_IdvVSD. The results will be summarized in a table at the end of this section.

The next parameters determined were the output resistance, r_{op}, and $V_{SD,SAT}$. These were determined via the following schematic and waveform. A table containing the range of values for r_{op} will be included at the end of this section. The related file is titled PMOS2_routp.



PMOS Schematic



Waveform displaying values of r_{op} and $V_{SD,SAT}$

A visual approximation for $V_{SD,SAT}$ can be made around 300mV, but operating point simulations provide a better range of values. The low and high values of this range, along with the transconductance, g_{mp} , can be seen in the figures below. An estimate of 370mV will be used as an average value for $V_{SD,SAT}$ and 145uA/V for $g_{mp.}$ Measured values will be included in a table at the end of this section.

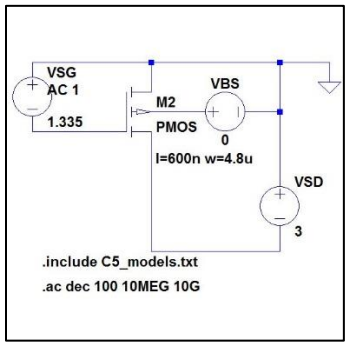
Name:	m2
Model:	pmos
Id:	3.08e-05
Vgs:	-3.35e-01
Vds:	1.00e+00
Vbs:	1.00e+00
Vth:	-8.96e-01
Vdsat:	-3.65e-01
Gm:	1.20e-04
Gds:	5.83e-06
Gmb	3.02e-05
Cbd:	0.00e+00
Cbs:	0.00e+00
Cgsov:	1.23e-15
Cgdov:	1.23e-15
Cgbov:	4.89e-16
dQgdVgb:	7.07e-15
dQgdVdb:	-1.21e-15

Low range of $V_{SD,SAT}$

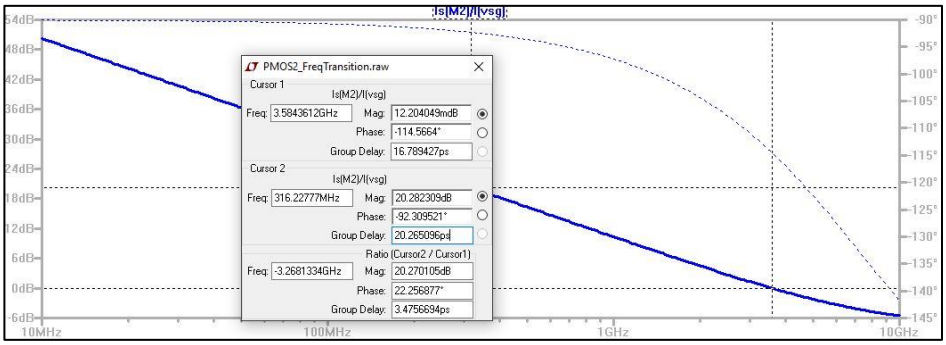
Name:	m2
Model:	pmos
Id:	4.76e-05
Vgs:	3.67e+00
Vds:	5.00e+00
Vbs:	5.00e+00
Vth:	-8.76e-01
Vdsat:	-3.78e-01
Gm:	1.62e-04
Gds:	3.96e-06
Gmb	3.95e-05
Cbd:	0.00e+00
Cbs:	0.00e+00
Cgsov:	1.23e-15
Cgdov:	1.23e-15
Cgbov:	4.89e-16
dQgdVgb:	7.07e-15
dQgdVdb:	-1.21e-15

High range of $V_{SD,SAT}$

The transition frequency of the PMOS was determined to be 3.58GHz. The circuit and waveform are displayed in the figures below. The related file is titled PMOS2_FreqTransition.



Transition Frequency Circuit



PMOS Transition Frequency, f_T

The following tables contain a summary of the PMOS values obtained for this design project.

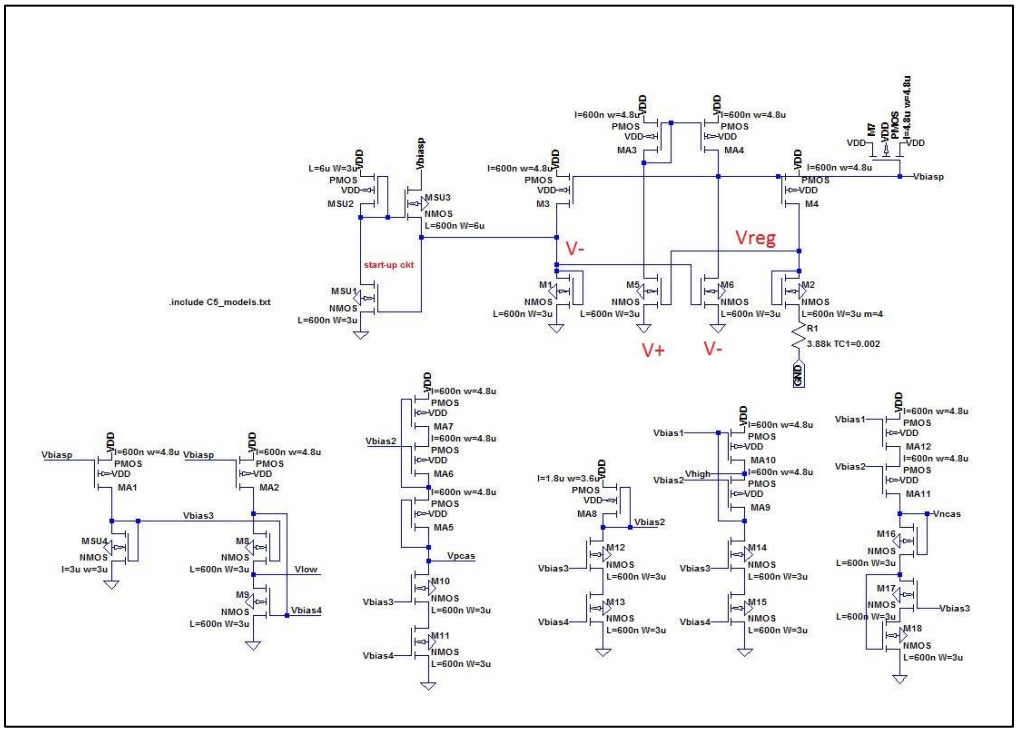
PMOS Characteristics	
W/L = 4.8um/600nm	Ratio = 8
I_{bias} = 40uA	
V_{thp} =0.840V	
V_{SG} = 1.335V ≈ 1.34V	
V_{OVP} = 1.34 - 0.840V = 0.810V	
$V_{SD,sat}$ = 370mV approx	

VDD (V)	r_{op} (Ω)	g_{sd} (A/V)	g_{mp} (A/V)
0.00	8.30k	129u	0.00
1.00	171k	5.85u	120u
2.00	235k	4.25u	136u
3.00	250k	4.00u	145u
4.00	254k	3.94u	154u
5.00	253k	3.95u	162u

Sample values of interest from PMOS simulations

C. Beta-Multiplier Reference Design

The BMR design was selected to reduce the sensitivity of the short-channel design process to changes in VDD that result from the low output resistances involved with the short-channel process. To this end, a general biasing circuit for short channel design was selected for the project. The schematic is seen below.



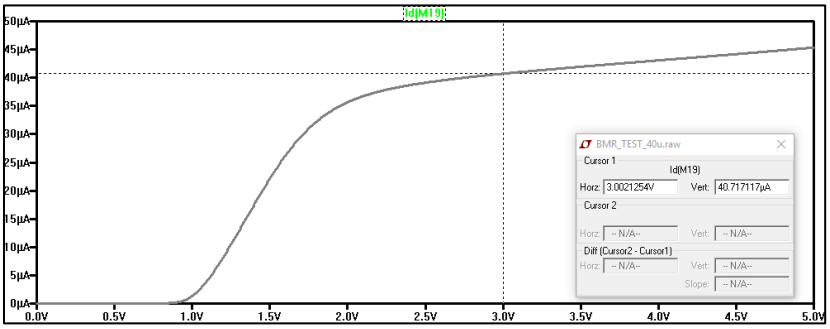
BMR Circuit

The point of this design is to use negative feedback to make the differential inputs, V_+ and V_-, equal, thus making V_{GS} equal on both sides of the amplifier. This works due to a comparatively larger output resistance on the side of the amplifier with the beta multiplier. The output of the differential amplifier is tied to the PMOS gates. This causes the PMOS devices to turn on equally, but the current on the right side of the circuit increases quicker due to the larger width. To address this issue, a negative feedback is added to the positive terminal of the differential amplifier to subtract and stabilize V_{GS} . This works by equalizing the drains of M1 (V_-) and M5 (V_{reg}). The feedback works systematically to increase V_{reg} if it is less than V_-, or decrease V_{reg} if it is larger than V_-. For example, if V_{reg} is less than V_-, the current through M5 decreases, the gate of MA3 increases, and the output of the amplifier decreases. In turn, this drives the gate of M4 down allowing it to source more current, ultimately driving V_{reg} up until it is equal to V_- .

The BMR startup circuit allows a small amount of current to trickle in through a transistor functioning as a switch, MSU3 in the schematic above. This current is generated via the voltage ranging from VDD to VDD - V_{thn} at the gate of MSU2. MSU3 functions as a switch by turning on and leaking current into the gates of the NMOS M1 and M6. Eventually, the circuit snaps and turns on. Simultaneously, MSU3 is pulled to ground by the current mirror MSU1. At this point, the BMR is operational and the start-up circuit no longer impacts the BMR's behavior.

Testing the BMR proved to be challenging. The main issue was selecting the resistor to be used for the beta-multiplied NMOS. This was solved for iteratively in simulations by stepping the resistor from 1kΩ to 10kΩ and then repeating until a resistor value resulting in the appropriate range for the selected bias current was determined. The end result was a resistor value of 3.88kΩ. Using this value gave the best fit for the desired bias current of 40uA between 3VDD and 5VDD. This is not the most practical method, but the most effective due to

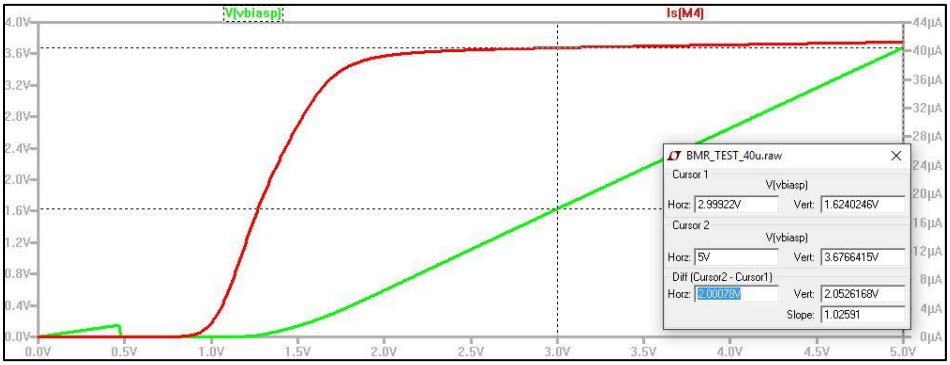
the lack of a transconductance parameter in solving for the resistor, as done in the long-channel process. The test file is titled BMR_TEST_40u_3VDD.



I_{bias} 40uA with R =3.88kΩ

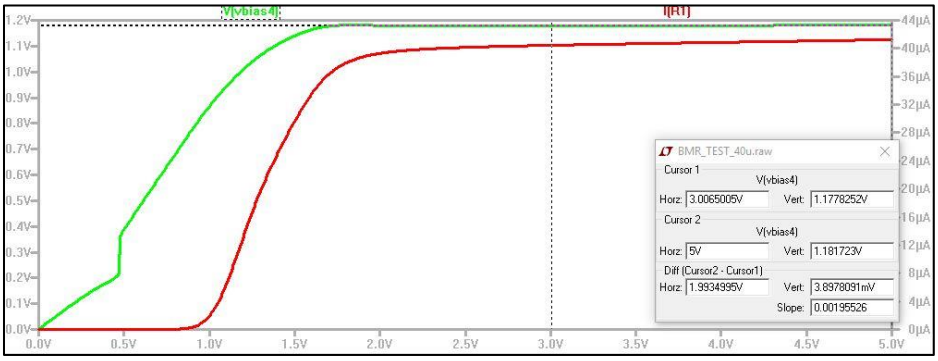
Checking the bias voltages versus the calculated voltages was performed using the values determined in the NMOS and PMOS characterization process. The first value compared to the theoretical value was V_{biasp}, seen below the theoretically calculated value. The simulated values closely mirror the theoretical values calculated using the values obtained via characterization of the devices.

$$V_{biasp} = VDD - V_{SG}$$
$$V_{biasp} = 5 - 1.34 = 3.66$$
$$V_{biasp} = 3 - 1.34 = 1.66$$



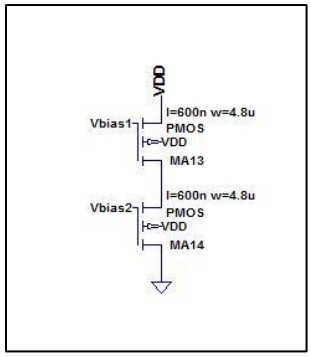
Values of V_{biasp} at 3VDD and 5VDD

Similarly, the theoretical value of V_{bias4} closely matches the simulated value for V_{GS} , but this should match considering V_{bias4} equals V_{GS} . The value for V_{GS} at the bias current 40uA was determined to be 1.11V. As seen in the figure below, V_{bias4} remains relatively constant at 3VDD and 5VDD, approximately 1.17V. This suggests the biasing circuit is functioning properly.

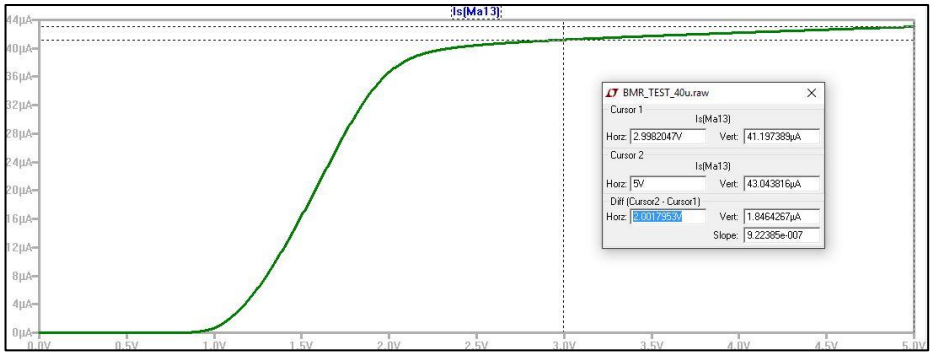


Values of V_{biasp} at 3VDD and 5VDD

V_{bias1} and V_{bias2} were tested using cascoded current mirrors to ensure these were also biasing properly. The current is a close approximation to the 40uA bias current. The results are displayed below.

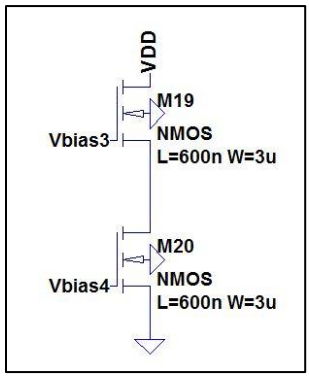


PMOS Cascode Mirror

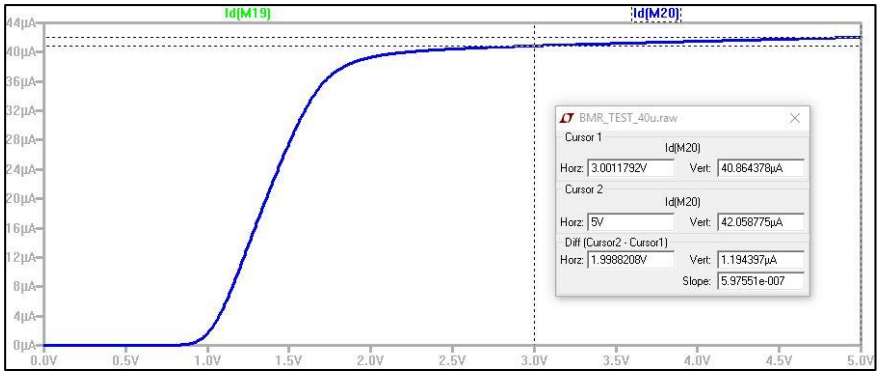


V_{bias1} and V_{bias2}

Similarly, V_{bias3} and V_{bias4} were tested to verify proper biasing with similar results displayed below. These results indicate the BMR is biasing properly.

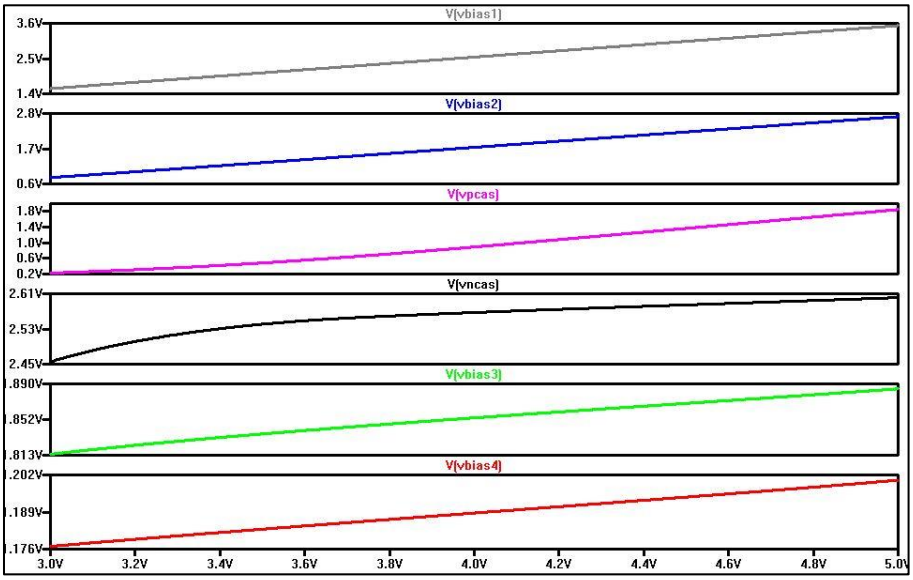


NMOS Cascode Mirror



V_{bias1} and V_{bias2}

The BMR bias voltages are displayed below between 3VDD and 5VDD.



Note V_{bias1} increases linearly with VDD and V_{bias4} approximates the 1.11V determined for V_{SG} via the NMOS characterization.

Voltage	3VDD Range (V)	5VDD Range (V)
V_{bias1}	1.55	3.57
V_{bias2}	0.747	2.71
V_{pcas}	0.224	1.88
V_{ncas}	2.45	2.59
V_{bias3}	1.81	1.88
V_{bias4}	1.17	1.20

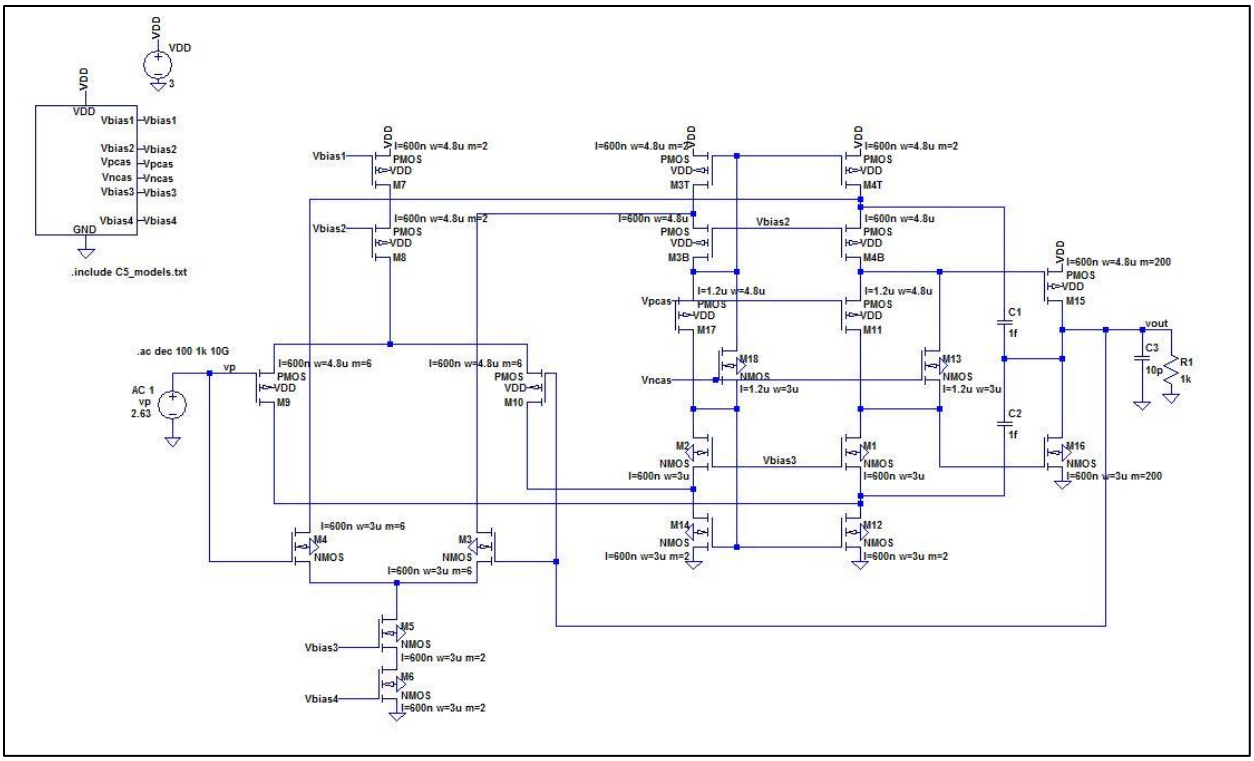
Bias Voltages for 3VDD to 5VDD

D. Operational Amplifier

The operational amplifier design selected for this project is a two stage design consisting of a folded-cascode op-amp with a push-pull output buffer. This was the final design selected after several earlier designs were altered due to limitations that would have been obvious with more design experience. Specifically, the initial design was a three stage op-amp consisting of a differential amplifier, a common source amplifier and a source follower output stage. The limitations faced with this circuit were mainly based on the output swing. The initial concept may have been able to meet the required specs, but the common mode range (CMR) seemed to be an issue. Specifically, the design would likely fall short of the required 80% output swing. Another issue faced was the initial bias current. The first BMR designed was set with a bias current of 160uA that resulted in too much current drawn from VDD. This simple design seemed like a bad idea after starting initial calculations.

This led to trying a folded-cascode operational transconductance amplifier as a first stage with a push-pull output buffer for the second stage. The first stage of the op-amp would be a PMOS driven OTA. This stage was selected to limit the op-amp to two stages and to take advantage of the OTA's characteristics. Specifically, the OTA can drive high impedance loads because it has a high output impedance and a large gain. This would allow the op-amp to drive the maximum 10pF capacitive load alone, but the push-pull output buffer is needed to lower the output resistance so driving the minimum 1kΩ load would not kill the gain. This design tested close to project specifications, but fell short of the required bandwidth and would not meet the required error difference of less than 0.1%. Despite numerous attempts to calculate a compensation capacitor, C_c, value and attempting to find a value via sweeping C_c , the compensation never worked properly. Thus, testing and designing for this topology was abandoned.

The final design was decided upon after reviewing wide-swing op-amp topologies. The final schematic is shown in the figure below.



Final Voltage Follower Design

This design incorporates two differential amplifiers with two folded cascodes together as a first stage with a push pull output buffer as a second stage. The first stage of this design uses a PMOS differential amplifier to bias an NMOS folded cascode and an NMOS differential amplifier to bias a PMOS folded cascode. The major benefits of this topology are a large gain and a common mode input range that extends beyond the rails. This can be seen by examining the CMR maximum and minimum input values.

$CMR_{max} = VDD - V_{SD,sat} + V_{THN} \geq V_G \; also \; > VDD$

$5VDD: V_{CMRmax} < 5V - 370mV + 0.750V = 5.38V$

$3VDD: V_{CMRmax} < 3V - 370mV + 0.750V = 3.38V$

$V_{CMRmin} = V_G \geq V_D - V_{THP} = V_{DS,sat} - V_{THP}$

$V_{CMRmin} > 270mV - 840mV = -570mV$

The gain of this stage is as follows:

$$\frac{v_{out}}{v_{in}} = g_{mp}(R_{o,cascn} || R_{o,cascp}) = g_{mp}(R_{o,cascn} || R_{o,cascp}) = g_{mp}(g_{mn} r_{on}^2 || g_{mp} r_{op}^2)$$

$$\frac{v_{out}}{v_{in}} \approx 145uA/V[(\frac{180uA}{V})(370k\Omega^2) || (\frac{145uA}{V})(250k\Omega^2)] \approx 6.6MV/V$$

Clearly, this is a large gain, but the drawback is this stage also has a large output resistance, meaning a small 1kΩ load will kill the gain of the amplifier. This is the reason the inverting push-pull amplifier stage is added for stage two. This stage has a low output impedance that will allow the op-amp to drive a small load and also allows for a large CMR.

The design is such that when the common mode voltage moves toward ground the NMOS diff amp shuts off and when it moves toward VDD the PMOS diff amp shuts off. This changes the current versus when both differential amplifiers are operating somewhere in the middle of the common mode range. For example, the overall gain of the op amp in the middle of the CMR is as follows:

$$\frac{vout}{vin} = (g_{mn} + g_{mp}) * (r_{on}||r_{op}) = (145uA + 180uA) * (150k\Omega||253k\Omega) \approx 30V/V$$

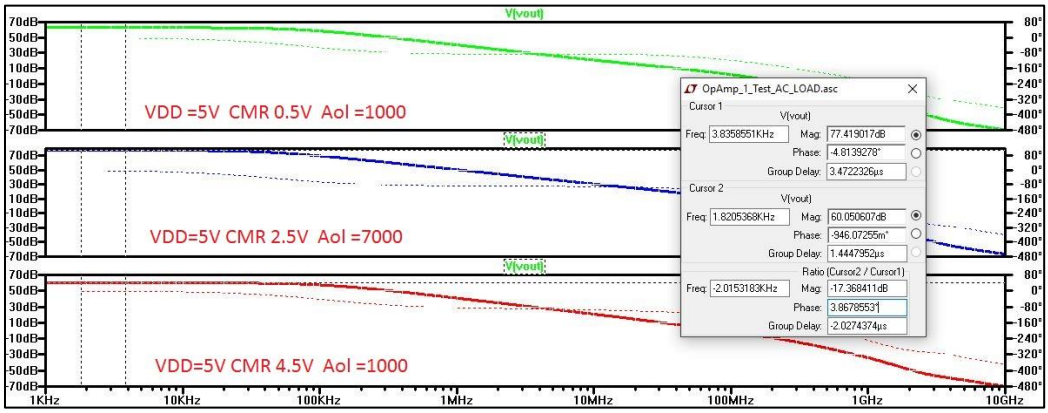
or, near VDD

$$\frac{vout}{vin} = g_{mn} * (r_{on}||r_{op}) = 180uA * (150k\Omega||253k\Omega) \approx 16V/V$$

or, near ground

$$\frac{vout}{vin} = g_{mp} * (r_{on}||r_{op}) \approx 13.65V/V$$

However, when one of the diff amps is off, that transconductance goes to zero and the gain decreases. This is demonstrated via an AC simulation showing the gains when the DC bias is near ground, in the middle and near VDD. The simulation results below show the gain increasing in the middle plot when the common mode input is 2.5V and both inputs are on. The gain decreases when the CMR approaches VDD or ground.



Gain Variations with changes in CMR

Performing an operating point simulation for 5VDD revealed the DC biasing for the circuit. The results below demonstrate the BMR circuit is biasing the op-amp properly. The related files are titled DCBias_3VDD and DCBias_5VDD.

--- Operating Point ---

V(vdd):	5	voltage	
V(n002):	4.21413	voltage	
V(n001):	3.6001	voltage	
V(n003):	4.21679	voltage	
V(vp):	2.5	voltage	
V(n005):	3.56126	voltage	
V(vbias2):	2.70106	voltage	vs 2.71V sim
V(n004):	4.33974	voltage	
V(vbias1):	3.52821	voltage	vs 3.57V sim
V(n006):	3.8193	voltage	
V(n008):	0.635261	voltage	
V(n007):	0.637048	voltage	
V(vout):	2.49987	voltage	
V(vgs12):	1.15013	voltage	
V(vgs16):	1.12335	voltage	
V(vbias3):	1.8846	voltage	vs 1.88V sim
V(n009):	1.32767	voltage	
V(n010):	0.572998	voltage	
V(vbias4):	1.20016	voltage	vs 1.20V sim
V(vpcas):	1.84664	voltage	vs 1.88V sim
V(vncas):	2.60119	voltage	vs 2.59V sim

DC Bias at 5VDD

--- Operating Point ---

V(vdd):	3	voltage	
V(n002):	2.22739	voltage	
V(n001):	1.65475	voltage	
V(n003):	2.22697	voltage	
V(vp):	2.5	voltage	
V(n005):	1.66181	voltage	
V(vbias2):	0.796872	voltage	vs 0.747V sim
V(n004):	3	voltage	
V(vbias1):	1.56092	voltage	vs 1.55V sim
V(n006):	3	voltage	
V(n008):	0.618621	voltage	
V(n007):	0.618431	voltage	
V(vout):	2.50002	voltage	
V(vgs12):	0.965019	voltage	
V(vgs16):	0.967165	voltage	
V(vbias3):	1.81407	voltage	vs 1.81V sim
V(n009):	1.30754	voltage	
V(n010):	0.535496	voltage	
V(vbias4):	1.17694	voltage	vs 1.17V sim
V(vpcas):	0.223202	voltage	vs 0.224V sim
V(vncas):	2.45513	voltage	vs 2.45V sim

DC Bias at 3VDD

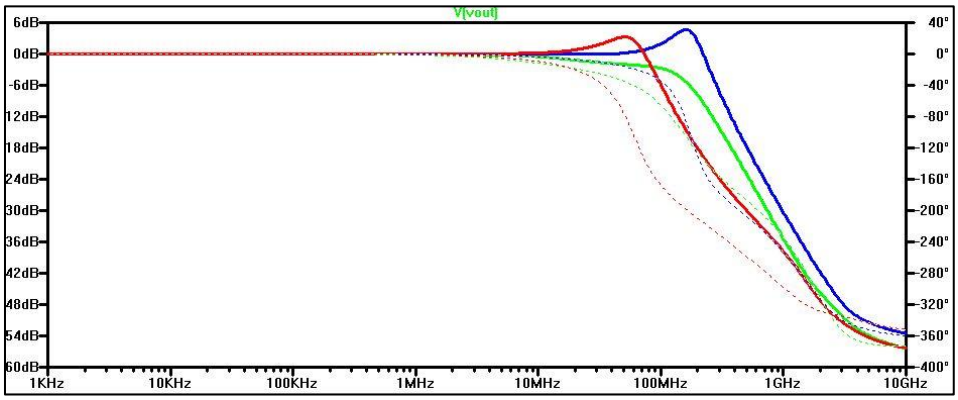
The labeled values in the image above display the operating point values for the two stage operational amplifier versus the bias voltages determined in the independent BMR testing. These results demonstrate the circuit is

biasing almost perfectly with the only noticeable difference V_{bias2} is almost 50mV less than the value determined from testing the BMR independently.

The largest issue faced in designing this circuit was determining the value of the compensation capacitor. This was determined iteratively via simulations when the calculated value did not work. The calculated value was determined as follows:

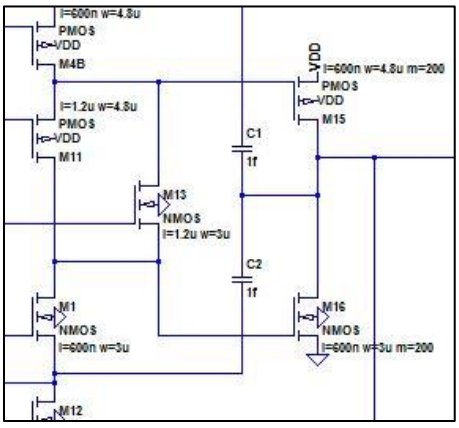
$$C_c = \frac{g_{mp} + g_{mn}}{2\pi * f_{un}} = \frac{145u + 180u}{2\pi * 100MHz} \approx 517fF$$

However, this capacitor placed between the two folded cascode PMOS devices resulted in the following waveform for 3VDD at steps of 0.23V, 1.43V, and 2.63V. The peaking was an issue that was difficult to correct.



Poor Compensation

This was ultimately solved by splitting the capacitor between the NMOS and PMOS folded cascode devices and setting the value to 1fF, as seen below. This was the most difficult portion of the design to correct. The output with this compensation can be seen in the following Results section of this report.



Proper Compensation

Another challenge in meeting the required specifications was modeling the load at the output of the amplifier. This was attempted by modeling the output stage as a capacitance in an effort to ensure enough current would be available to drive the loads.

First, the push-pull load was modeled as a capacitance as follows;

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} = \frac{3.9 * (\frac{8.86x10^{-12}F}{m})}{13.9x10^{-9}m} = 2.48x10^{-3}F/m^2$$

Given a slew rate minimum of 100V/us as a specification, the current necessary to drive the required load is

$$I_{out} = C_{Load}\frac{dV_{out}}{dt} = 10pF * \frac{100V}{us} = 1mA$$

The number of parallel devices, m, needed to drive 1mA is solved for as follows:

$$m = \frac{I_{out}}{I_{bias}} = \frac{1mA}{40uA} = 25$$

Initially, an additional 20% was added to this number to account for approximation errors. This made the initial total m =30. However, during simulations the poor decision to choose the PMOS width using the method outlined in Section 2 finally became an issue. The PMOS was not able to source enough current at the selected width with to drive the necessary load and still meet the bandwidth specification necessary for the project.

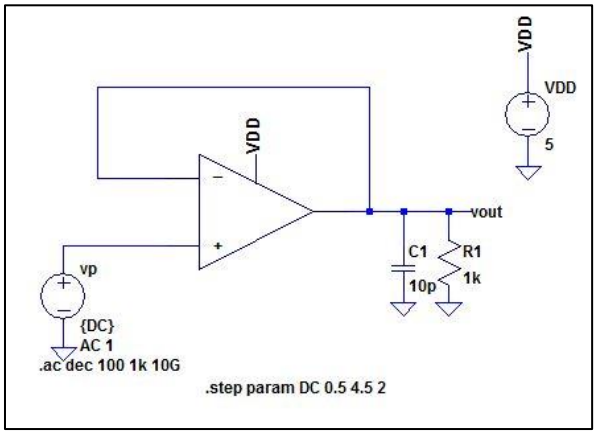
This began a process of experimenting with different values of m to attempt to reach the specifications. Increasing the number of parallel devices in the NMOS and PMOS differential amplifiers from 1 to 6 pushed the gain out far enough to meet the bandwidth requirement and increasing m on the PMOS and NMOS output to 200 allowed the design to meet all the necessary specs except one.

At 5VDD, the total current drawn from the design was 10.006mA, slightly over the 10mA maximum specification. The first attempt to correct this was to reduce the number of parallel devices at the output from m=200 to m=190. While this reduced the current draw enough to meet the requirement, this meant performing all the simulations again to ensure this change did not impact anything else previously determined. Thankfully, the reduction in current had a negligible impact on the circuit.

3. Results

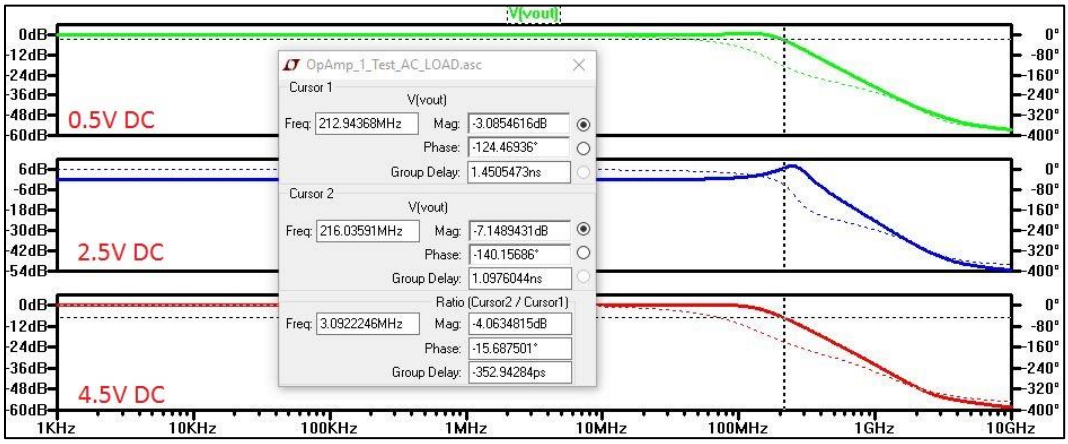
A. GAIN

The first project specification tested is the ability of the op-amp to operate between 3VDD and 5VDD while driving a 10pF maximum and 1kΩ minimum load. The ability of the voltage follower to operate under the above specifications and maintain the minimum bandwidth of 100MHz is demonstrated below. The voltage follower has a gain of one, thus the unity gain frequency is equivalent to the 3dB frequency. These results are included in the tables below.



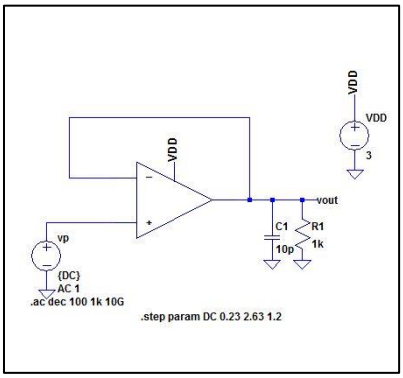
Voltage Follower Circuit 5VDD

Performing an AC sweep using file GAIN_BW_5VDD.asc with DC values set at intervals of 0.5V, 2.5V and 4.5V resulted in the following output. A table of results is included in section four of this report.

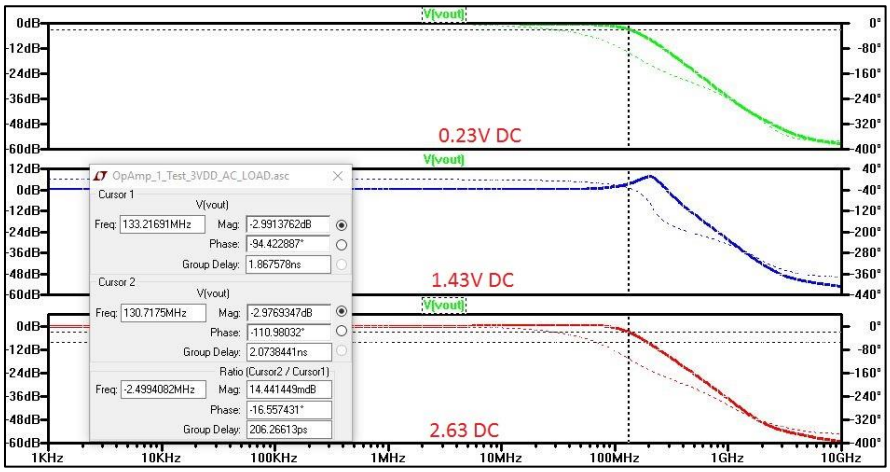


Gain 5VDD

Performing the same sweep for 3VDD using file GAIN_BW_3VDD.asc at DC intervals of 0.23V, 1.43V and 2.63V resulted in the following output.



Voltage Follower Circuit 3VDD



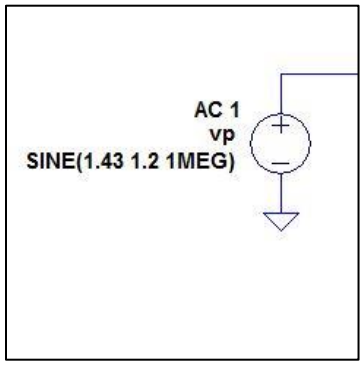
Gain 3VDD

VDD	DC 0.23V f_{un} (Hz)	DC 1.43V f_{un} (Hz)	DC 2.63V f_{un} (Hz)
3V No Load	48M	724M	813M
3V Full Load	134M	320M	131M

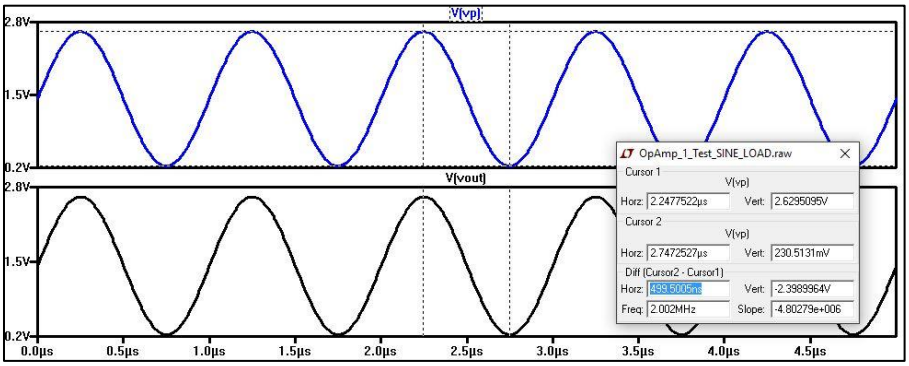
The full load conditions for both 3VDD and 5VDD meet the project specifications for minimum bandwidth of 100MHz when driving a 10pF and 1kΩ load.

B. Output Swing

Next, the output swing needs to be 80% of VDD to meet project specifications. This is the point where the limitations placed on the circuit by the common mode range are important. If the CMR is too small, the output swing will not meet the specifications. Using file OutputSwing_3VDD, the signal input for 3VDD and the resulting schematic are displayed below. The output at a DC offset of 1.43V swings from 230mV to 2.63V for a pk-pk swing of 2.4V, or equivalently 80% of 3VDD. These results are at full load.

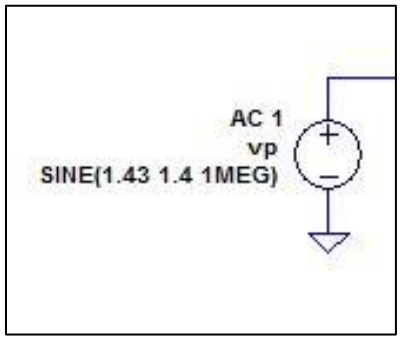


Input Signal at 80% of 3VDD

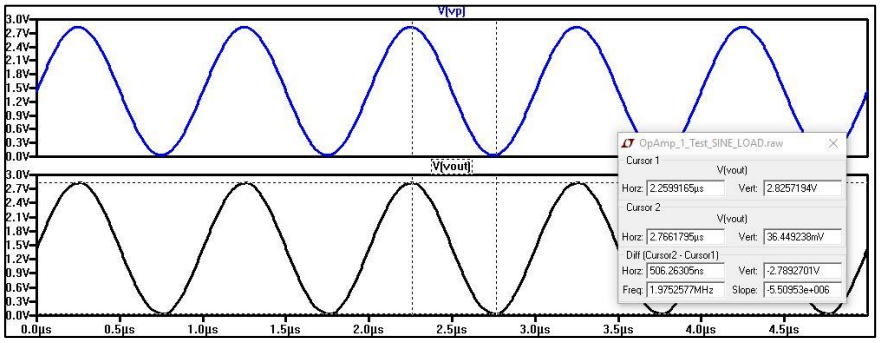


Output Swing at 80%

The extra swing from this circuit design can be shown by increasing the amplitude of the input signal. Changing the amplitude to 1.4V results in a swing of 2.8V, or 93.3% of 3VDD. This can be seen in the figures below.

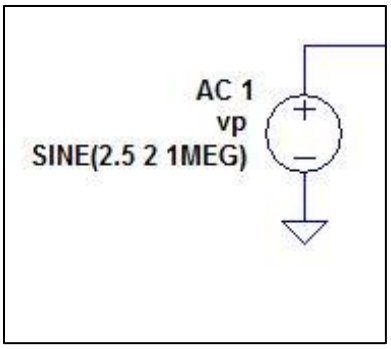


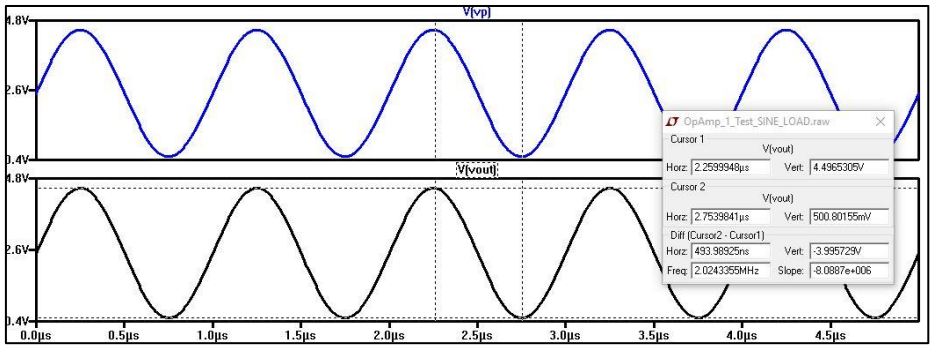
Input Signal at 93.3% of 3VDD



Output Swing at 93.3%

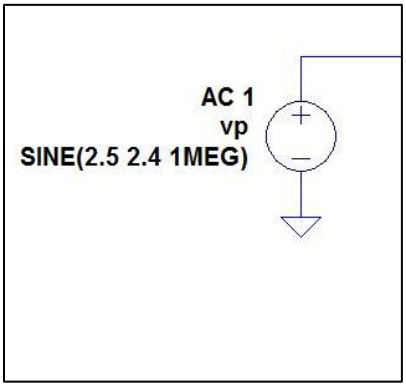
Similarly for 5VDD, using file OutputSwing_5VDD, at a DC offset of 2.5V the output swings from 0.5V to 4.5V, or 80% of 5VDD. The input signal and resulting waveform are displayed in the figures below.

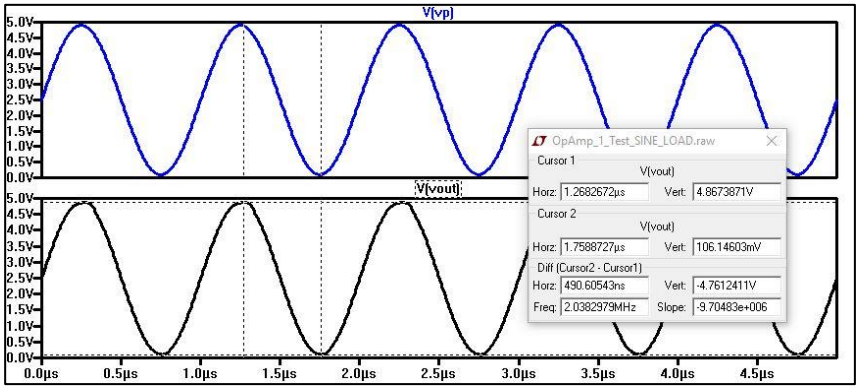




Input Signal at 5VDD Output Swing at 80%

Again, the output swing can easily exceed the 80% required as demonstrated via the same technique of increasing the amplitude. Using an amplitude of 2.4V swinging around 2.5V results in an output signal swinging at 96% of 5VDD.

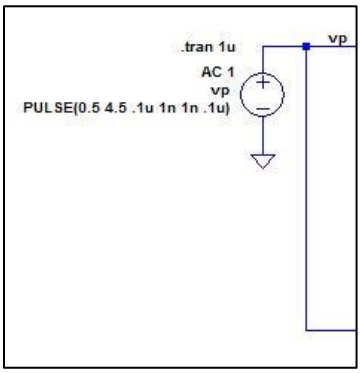


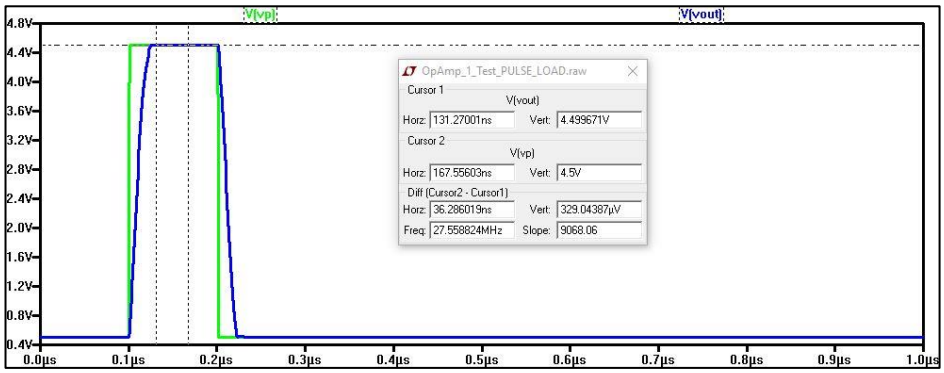


Input Signal at 96% of 5VDD Output Swing at 96%

C. Percent Error

The next requirement to be tested is the error difference between the input signal and output signal. This needs to be less than 0.1% for the project. The error was determined via a pulse input, using file StepInput_5VDD, at 80% of VDD. The results are displayed below.



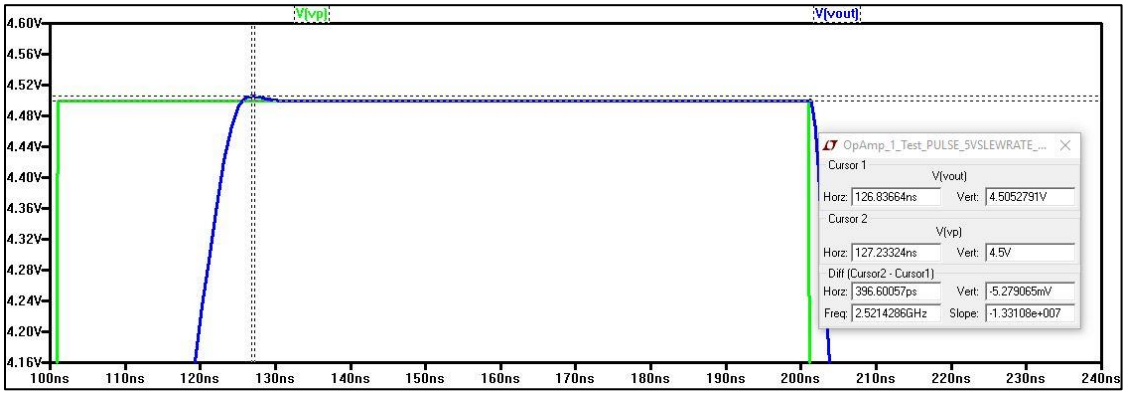


Step Input for 5VDD at 80% Percent Error 0.0073%

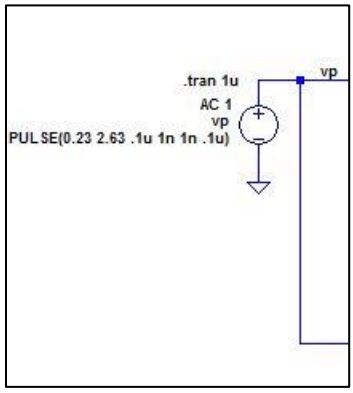
The percent error is calculated as follows:

$$Percent\ Error = \frac{4.5V - 4.499671}{4.5V} x100\% = 0.0073\%$$

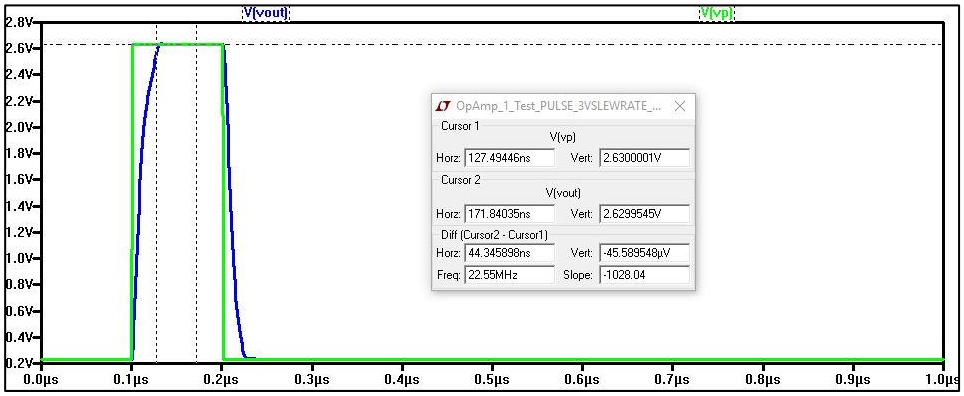
A small overshoot can be seen in the output signal when examined closely.



The percent error for 3VDD, using file StepInput_3VDD, is displayed in the figure below.



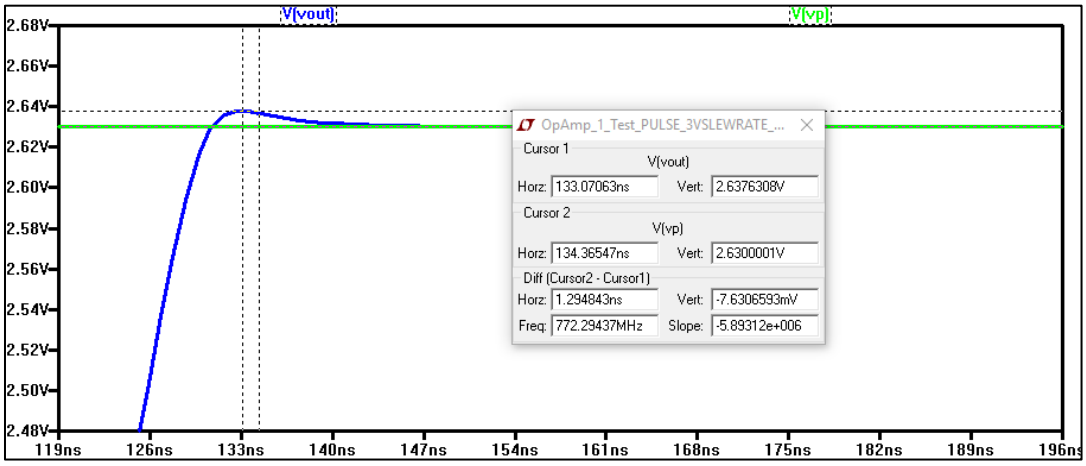
Step Input for 3VDD at 80%



Percent Error 0.0017%

$$Percent\ Error = \frac{2.63V - 2.6299545}{2.63V} x100\% = 0.0017\%$$

Again, there is a small overshoot visible in the output signal before flattening out.

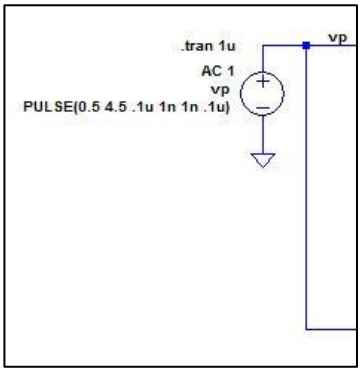


D. Slew Rate

The minimum slew rate required for the project is 100V/us where slew rate is determined as follows:

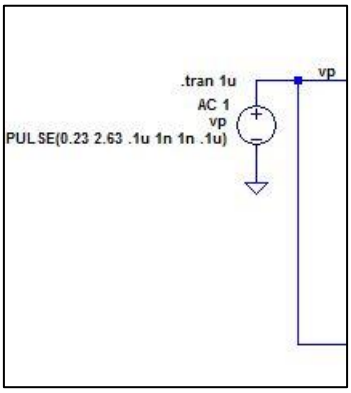
$$Slew\ Rate = \frac{dV_{out}}{dt}$$

The design easily surpasses the minimum specification as seen in the figure below. This was determined with a step function set to 80% of VDD and taking the derivative of the output. The related file name is SlewRate_3VDD.

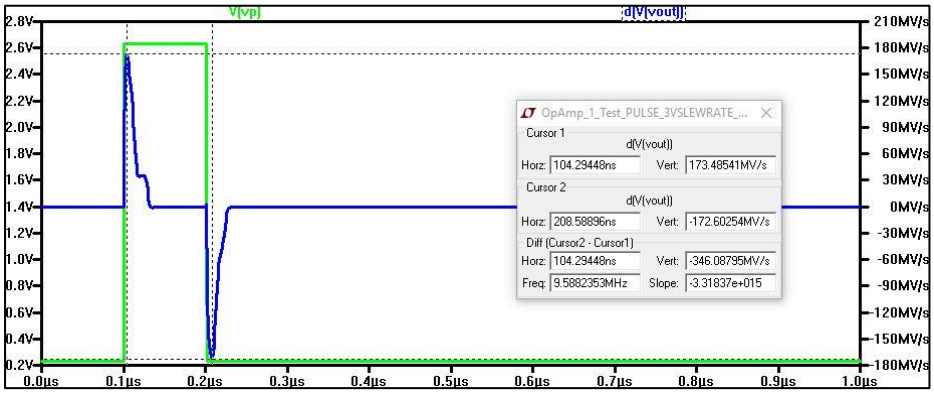


Step Input at 80% of 5VDD

Slew Rate of 246V/us at 5VDD



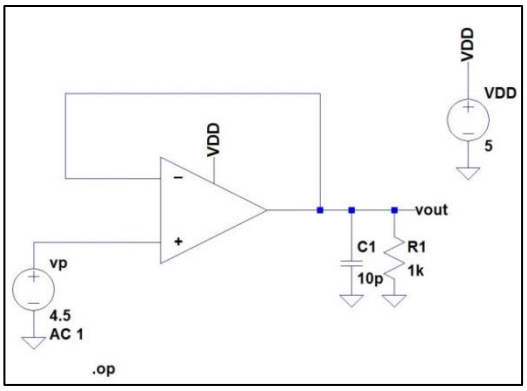
Step Input at 80% of 3VDD



Slew Rate of 173V/us at 3VDD

E. Current Draw from VDD

The simplest method to determine the current draw from VDD was an operating point simulation. The results for these simulations at 3VDD and 5VDD are seen below. The related files are titled CurrentDraw_3VDD and CurrentDraw_5VDD.

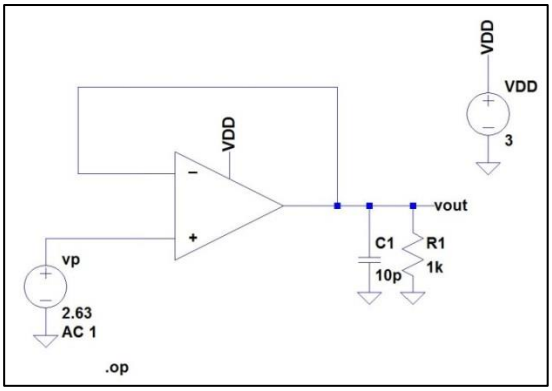


Operating Point Simulation Circuit

```
        --- Operating Point ---

V(vdd):         5               voltage
V(n001):        4.5             voltage
V(vout):        4.49959         voltage
I(C1):          4.49959e-023    device_current
I(R1):          0.00449959      device_current
I(Vdd):         -0.00973404     device_current
I(Vp):          0               device_current
Ix(x1:VDD):     0.00973404      subckt_current
Ix(x1:VOUT):    -0.0022498      subckt_current
Ix(x1:VP):      0               subckt_current
Ix(x1:VOUT):    -0.0022498      subckt_current
```

5VDD .op Results

The results above show the total current drawn from VDD at 5VDD, I(Vdd), is 9.73mA, just below the project specification of 10mA. This results in power dissipation at 5VDD of approximately 48.7uW.



Operating Point Simulation Circuit

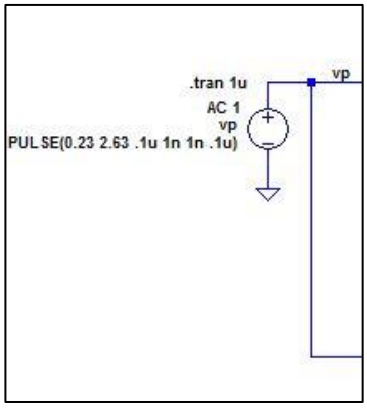
```
        --- Operating Point ---

V(vdd):         3               voltage
V(n001):        2.63            voltage
V(vout):        2.62994         voltage
I(C1):          2.62994e-023    device_current
I(R1):          0.00262994      device_current
I(Vdd):         -0.00579927     device_current
I(Vp):          0               device_current
Ix(x1:VDD):     0.00579927      subckt_current
Ix(x1:VOUT):    -0.00131497     subckt_current
Ix(x1:VP):      0               subckt_current
Ix(x1:VOUT):    -0.00131497     subckt_current
```

3VDD .op Results

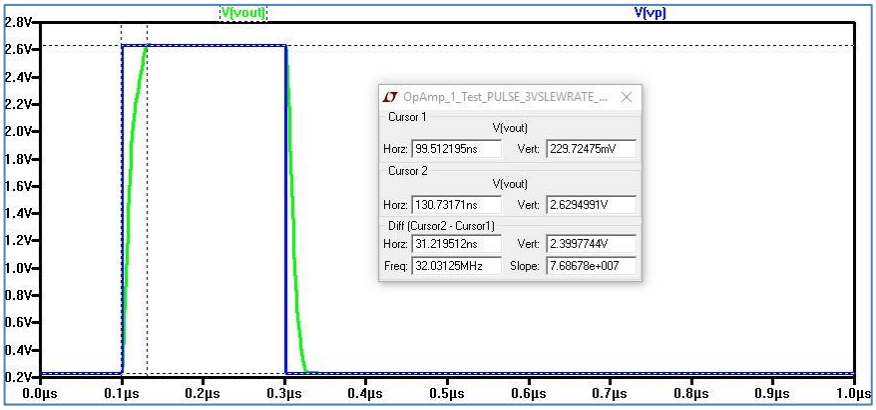
The results above show the total current drawn from VDD at 3VDD, I(Vdd), is 5.79mA, well below the project specification of 10mA. The power dissipation at 3VDD is approximately 17.4uW.

F. Settling Time and Rise and Time Delay

The settling time was determined using the file StepInput_3VDD and under full load. The low-to-high transition for 3VDD is seen below at 31.2ns. The related files for these simulations are titles StepInput_3VDD and StepInput_5VDD.

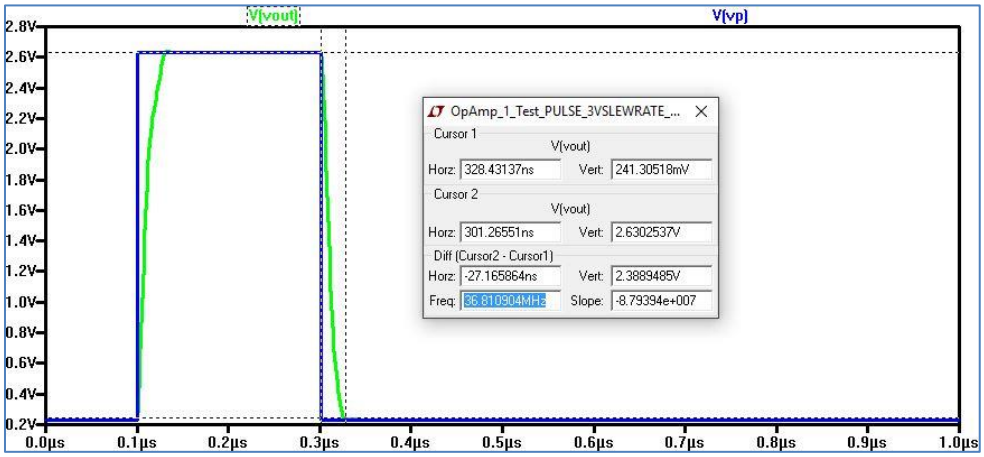


3VDD Input Signal



3VDD Settling Time Low-to-High Transition

The settling time high-to-low transition at 3VDD is displayed below at 27.1ns

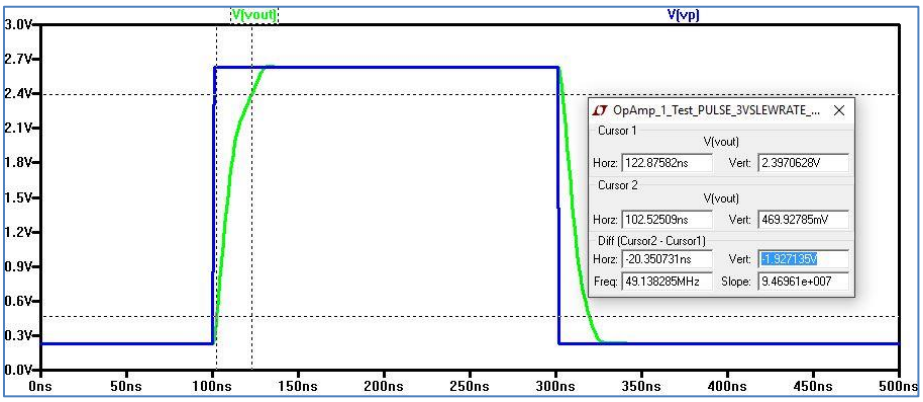


3VDD Settling Time High-to-Low Transition

The rise time is determined via the following calculation:

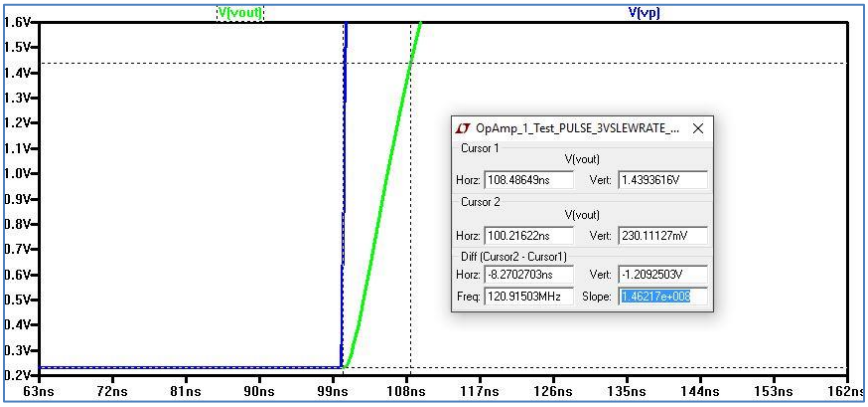
$$t_r = t_{90\%} - t_{10\%} = 122.8ns - 102.5ns \approx 20.35ns$$

where 90% of the 2.4V amplitude pulse from 0.23V to 2.63V is 2.39V and 10% is 0.47V.



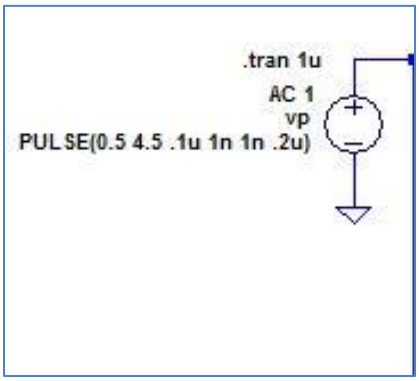
Rise Time at 3VDD

The time delay, t_d is determined as the time the pulse takes to rise to $0.5V_{pulse}$, or 1.43V for this signal. The resulting time delay is seen below at 8.27ns.

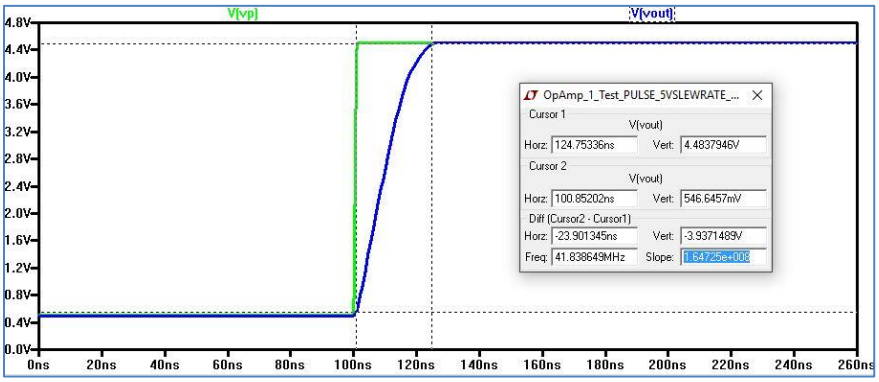


Time Delay at 3VDD

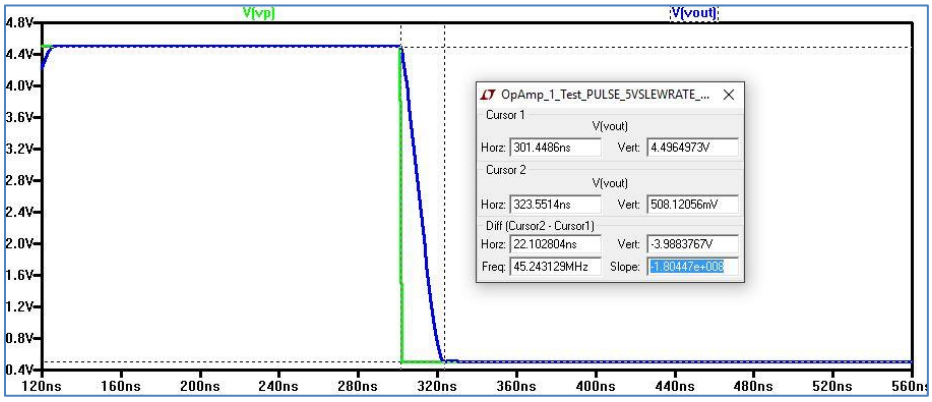
Repeating the same simulations for 5VDD, using the file StepInput_5VDD, resulted in a low-to high transition of 23.9ns and a high-to-low transition of 22.1ns.



5VDD Input Signal



5VDD Settling Time Low-to-High Transition

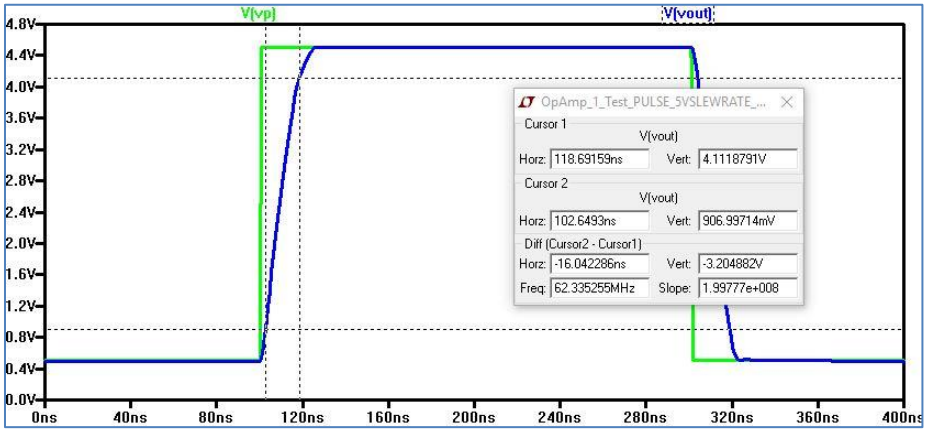


5VDD Settling Time High-to-Low Transition

The rise time at 5VDD is displayed below at 16.04ns.

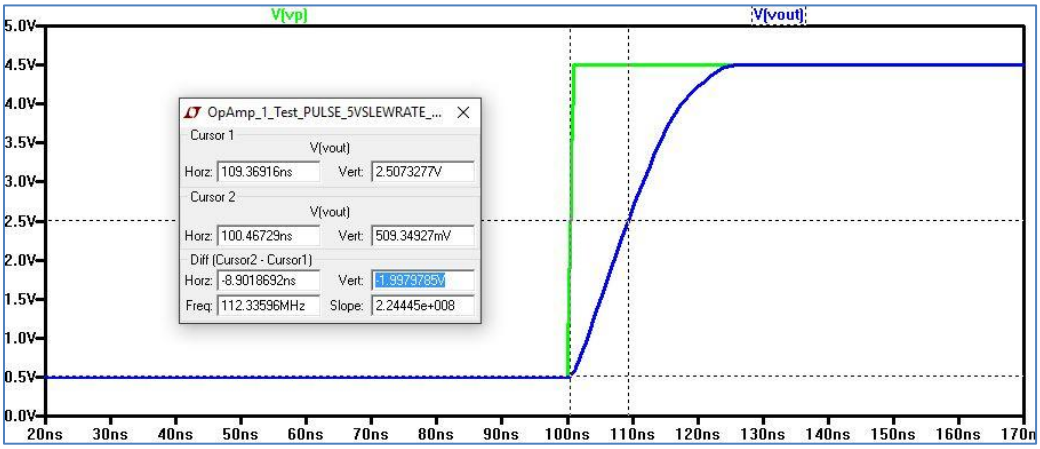
$$t_r = t_{90\%} - t_{10\%} = 118.6ns - 102.6ns \approx 16.04ns$$

where 90% of the 4V amplitude signal is 4.1V and 10% is 0.9V.



Rise Time at 5VDD

Lastly, the time delay at 5VDD is displayed below at 8.9ns.



Time Delay at 5VDD

4. Summary of Results

The following tables present a summary of the results determined via the design process outlined above.

Common Mode Range	3VDD	5VDD
$V_{CMR,min}$	-570mV	-570mV
$V_{CMR,max}$	3.38V	5.38V

Unity-Gain Frequency	DC 0.5V f_{un}(Hz)	DC 2.5V f_{un} (Hz)	DC 4.5V f_{un} (Hz)
5V No Load	183M	812M	164M
5V Full Load	210M	389M	157M

Unity-Gain Frequency	DC 0.23V f_{un} (Hz)	DC 1.43V f_{un} (Hz)	DC 2.63V f_{un} (Hz)
3V No Load	48M	724M	813M
3V Full Load	134M	320M	131M

Power Dissipation	Current Drawn from VDD (A)	Power (W)
3VDD	5.79u	17.4u
5VDD	9.73m	48.7u

Slew Rate	Slew Rate (V/us)
3VDD	173
5VDD	246

Output Swing	Percentage
3VDD	93%
5VDD	96%

Settling/Slewing	Low-to-High (s)	High-to-Low (s)	Rise Time (s)	Time Delay (s)
3VDD	31.2n	27.1n	20.4n	8.27n
5VDD	23.9n	22.1n	16.0n	8.90n

Percent Error	
3VDD	0.0017%
5VDD	0.0073%

5. Conclusion

The voltage follower design was initially a seemingly difficult project that required the correlation of topics covered during the duration of the course. There were numerous failures throughout the design process that assisted in learning and creating a functioning design, but these came at the expense of much lost time. The project also provided an opportunity to analyze my strengths and weaknesses as a designer and to learn from the mistakes made during the design process. Despite these mistakes and failures, a successfully functioning voltage follower that meets the required specifications as outlined in the project parameters was designed and is presented for evaluation.