APRIL 30, 2018

COURSE PROJECT:
K-DELTA-1-SIGMA MODULATOR

ECG 722 MIXED-SIGNAL CIRCUIT DESIGN

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1.Introduction: K-DELTA-1-SIGMA MODULATOR

This report details the design and characterization of a continuous time K-Delta Sigma noise shaping analog-to-digital converter (ADC) using On Semiconductor's C5 process. The proposed ADC is intended to replace the ADC seen in Figure 9.33 of the course textbook, *CMOS Mixed-Signal Circuit Design*, and displayed in Figure 1 below and demonstrate comparable results. Additional constraints of the design include the requirement of replacing the switched-capacitors in the circuit below with resistors and the exclusion of non-overlapping clock signals for switching. To this end, three different topologies have been designed for consideration as follows: first order with 8 K-paths, first order with 16 K-paths, and second order with 8 K-paths.

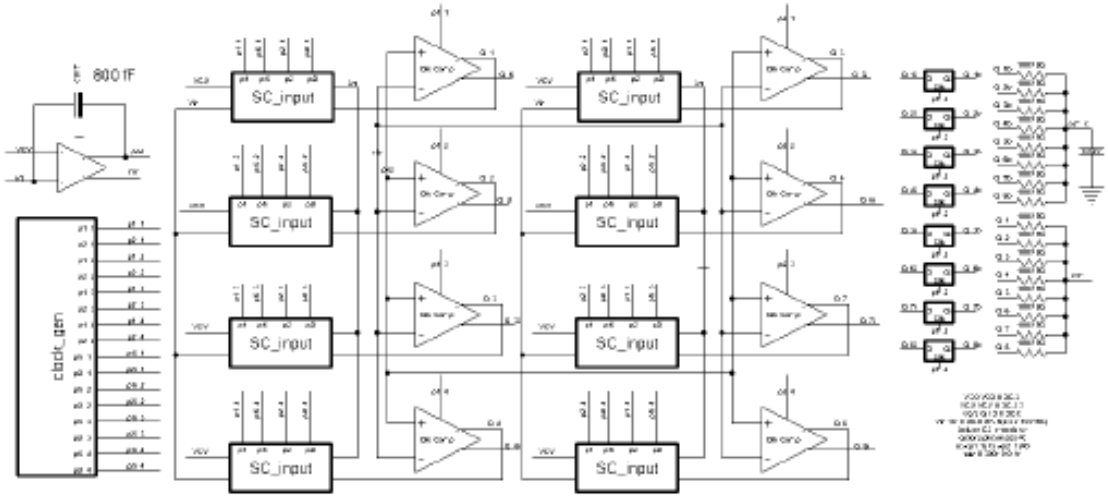

Figure 1

2. Project Design Specifications

The project specifications include the following:

- Ring oscillator design to generate eight equally spaced edges
- Comparator
- Amplifier to use in the integrator
- Feedback signal control and logic
- No non-overlapping clocks
- Replace switched capacitors with resistors

3. Design Results

Tables 1 and 2 below characterize the performance criteria the new ADC designs will attempt to meet or exceed. Note, the ADC results below are for a 1st order design based upon Figure 1 and simulated for 10 full cycles using an input sinusoid with a 2.5V DC offset, 2V amplitude and a 1MHz input frequency.

Fig 9.33 1st	Serial 64	Parallel 64	Serial 128	Parallel128	Serial256	Parallel256
$f_{s,new}$ (MHz)	1828	228	1828	228	1828	228
SNR (dB)	38.08	34.58	41.09	39.51	52.99	51.66
N_{eff} (bits)	6.03	5.45	6.53	6.27	8.51	8.29
Bandwidth (MHz)	14.29	14.28	7.14	7.14	3.57	3.57

Table 1: Fig.9.33 First Order Results with 1MHz input

Fig 9.332nd	Serial 64	Parallel 64	Serial 128	Parallel128	Serial256	Parallel256
$f_{s,new}$ (MHz)	1709	213	1709	213	1709	213
SNR (dB)	35.26	34.76	37.23	36.15	64.39	61.95
N_{eff} (bits)	5.56	5.31	5.89	5.71	10.40	9.99
Bandwidth (MHz)	13.35	13.34	6.67	6.67	3.34	3.34

Table 2: Fig. 9.33 2nd Order Results with 1MHz input

Tables 3-5 below display the results for each of the three design topologies using an input sinusoid with a 2.5V DC offset, 2V amplitude and a 1MHz input frequency.

1st order K=8	Serial 64	Parallel 64	Serial 128	Parallel128	Serial256	Parallel256
$f_{s,new}$ (MHz)	846	106	846	106	846	106
SNR (dB)	35.26	34.16	53.05	49.02	55.97	55.32
N_{eff} (bits)	5.56	5.38	8.52	7.85	9.00	8.89
Bandwidth (MHz)	6.61	6.61	3.31	3.31	1.65	1.65

Table 3: First Order 8 K-paths with 1MHz input

2nd order K=8	Serial 64	Parallel 64	Serial 128	Parallel128	Serial256	Parallel256
$f_{s,new}$ (MHz)	846	106	846	106	846	106
SNR (dB)	43.81	37.32	54.70	46.94	57.86	57.67
N_{eff} (bits)	6.98	5.90	8.79	7.50	9.32	9.28
Bandwidth (MHz)	6.61	6.61	3.31	3.30	1.65	1.65

Table 4: Second Order 8 K-Paths with 1MHz input

1st order K=16	Serial 64	Parallel 64	Serial 128	Parallel128	Serial256	Parallel256
$f_{s,new}$ (MHz)	813	51	813	51	813	51
SNR (dB)	43.63	30.95	54.92	43.26	58.35	53.38
N_{eff} (bits)	6.95	4.85	8.83	6.89	9.40	8.57
Bandwidth (MHz)	6.35	6.34	3.18	3.17	1.59	1.58

Table 5: First Order 16 K-Paths with 1MHz input

Table 6 displays power consumption results for each topology.

Power Consumption I_{RMS}*VDD	
Fig 9.33 1st order	67mW
Fig 9.33 2nd order	97mW
KD1S 1st order 8-path	114mW
KD1S 1st order 16-path	129mW
KD1s 2nd order 8-path	128mW

Table 6: Power Consumption

3. Design Considerations

This section details the considerations for each of the project components and provides an overview of the general methodology behind the delta-sigma noise shaping modulator design. The individual topologies explored for this project will be detailed in Section 4.

3.1 Noise Shaping

The proposed designs all use noise shaping (NS) along with oversampling to achieve high resolution. Simple oversampling allows for increased resolution by decreasing the amplitude of the quantization noise spectrum and bandlimiting the spectrum with a filter, but to provide a substantial increase a high oversampling ratio is required. Noise shaping techniques employ the use of filters to push quantization noise outside the signal bandwidth of interest.

In the proposed designs, the output of a comparator will feedback to the summing node of an integrator where quantization noise added by the comparator is differentiated. The result gives us the noise transfer function (NTF). In an oversampled system, the quantization has a flat spectrum that repeats. By differentiating, the noise shifts to higher frequencies while conserving the energy in the Power Spectral Density (PSD). Figure 2 below shows a general case PSD for a first-order and second-order noise shaping modulator's modulation noise. It is clearly shown that at lower frequencies, bandlimiting a signal has the effect of filtering out a large amount of noise from the spectrum.

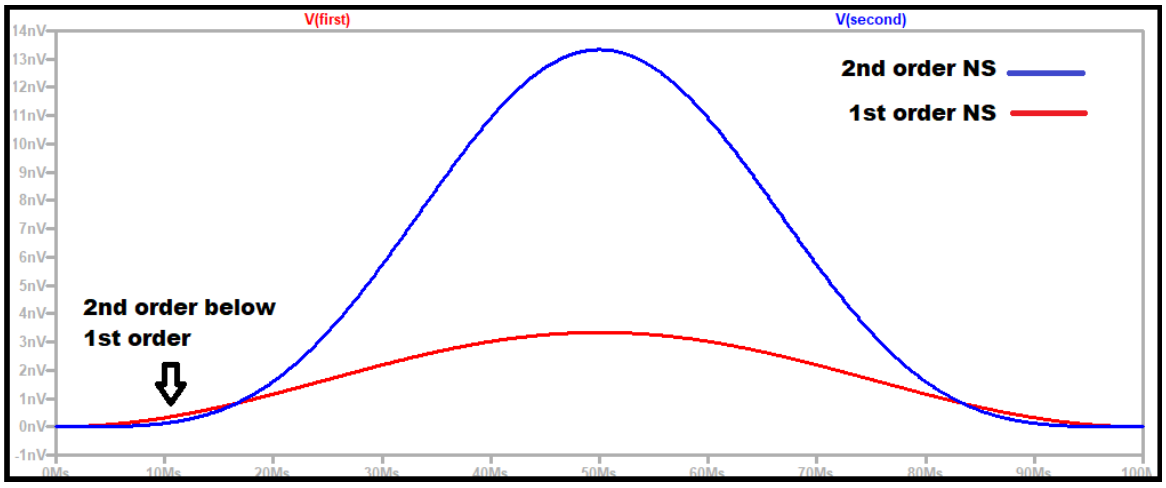

Figure 2 First- and second-order NS modulator's modulation noise

Limiting the input signal bandwidth and increasing the sampling frequency, f_s, without using noise shaping results in an increase in ADC resolution of 0.5-bits for every doubling of the sampling frequency. By combining noise shaping and oversampling, the resolution increases by an ideal 1.5-bits for every doubling in a first order topology and 2.5-bits in a second-order topology. This is given as follows

$$SNR_{ideal,1-NS} = 6.02N + 1.76 - 5.17 + 30\log(K) \approx 74.8dB$$

$$SNR_{ideal,2-NS} = 6.02N + 1.76 - 12.9 + 50\log K \approx 115.2dB$$

where K in the above represents the oversampling ratio (OSR) and N is the number of bits. Note, this equation is dependent on the RC time constant set in the design, thus these values will be approximations.

The oversampling ratio is given by

$$K = \frac{f_s}{2 * B}$$

where B is bandwidth. In this project, the oversampling is performed using Matlab at OSR values of 64, 128, and 256.

3.2 K-Paths

One of the issues involving simple oversampling is the difficulty in clocking at very high frequencies due to negative effects that result, such as electromagnetic interference. A method to achieve high sampling frequencies while avoiding the difficulties of high speed clocking is to use 'K' number of paths on the feedback that are clocked at evenly spaced clock phases over the course of a sampling period. This effectively increases the sampling frequency by a factor of 'K' or

$$f_{s,new} = K_{path} * f_s$$

The two proposed 8-path topologies use f_s equal to 100MHz resulting in an $f_{s,new}$ of 800MHz. The 16-path topology uses f_s equal to 50MHz again resulting in an $f_{s,new}$ of 800MHz. Each path also contains two transmission gate switches acting as controls to either connect a path to the integrator summing node or disconnect the path while a different 'K' path connects. The transmission gate switches will be detailed later.

3.3 Comparator

The comparator is arguably the most critical component of the delta-sigma modulator. In simple terms, the comparator needs to be able to make fast decisions wherein the output snaps high or low quickly and decisively. This is due to using 8(16) K-paths and thus 8(16) comparators. The clocks used for each comparator will be 8(16) times faster than the sampling frequency. The nature of sigma-delta topology averaging reduces glitches that may occur due to a slow comparator, but a fast comparator will further limit these glitches and increase resolution. The clocked comparator designed and found in the file ***clk_comparator_v2*** is used in all three topologies and displayed below in Figure 3.

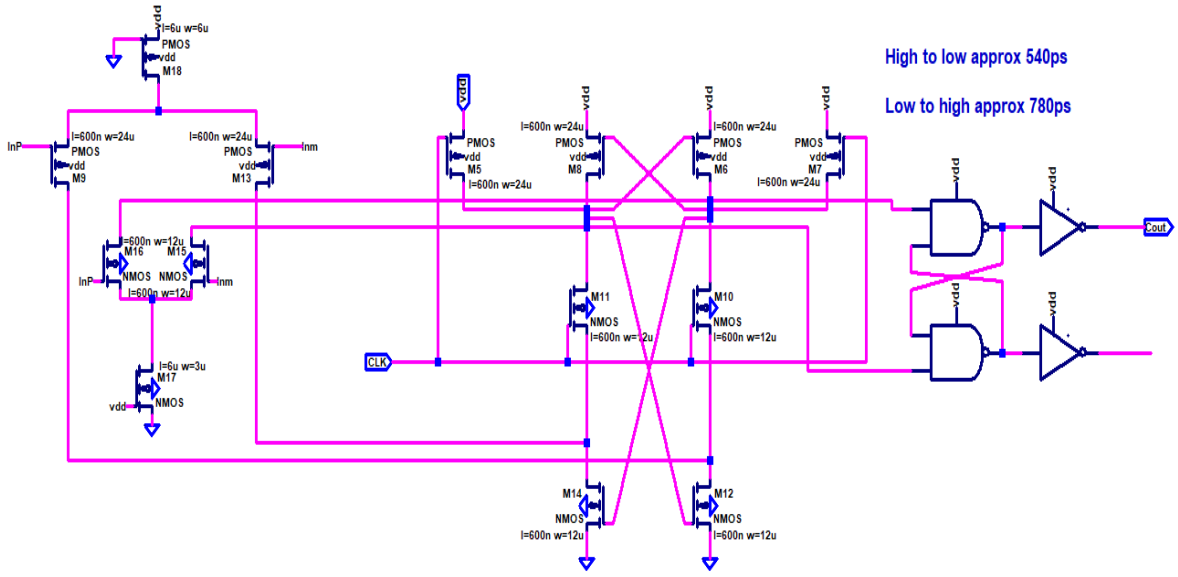

Figure 3: SR Delay stage

The initial topology given in the design files had a delay of approximately 1.2ns and appeared to be limiting initial design results. This topology uses the basic concept of a sense amplifier to snap the comparator outputs to the rails and provides high sensitivity and wide output swing. An additional benefit to this topology is that only one differ-amp is required to create the imbalance required for fast decision making. Simulation results found in the file ***clk_comparator_test*** are displayed below in Figure 4. In the top plot we see the positive terminal going high just before the comparator is clocked as seen in the middle plot. The results show the comparator swings from 5V to 0V in approximately 500ps and from 0V to 5V in approximately 700ps.

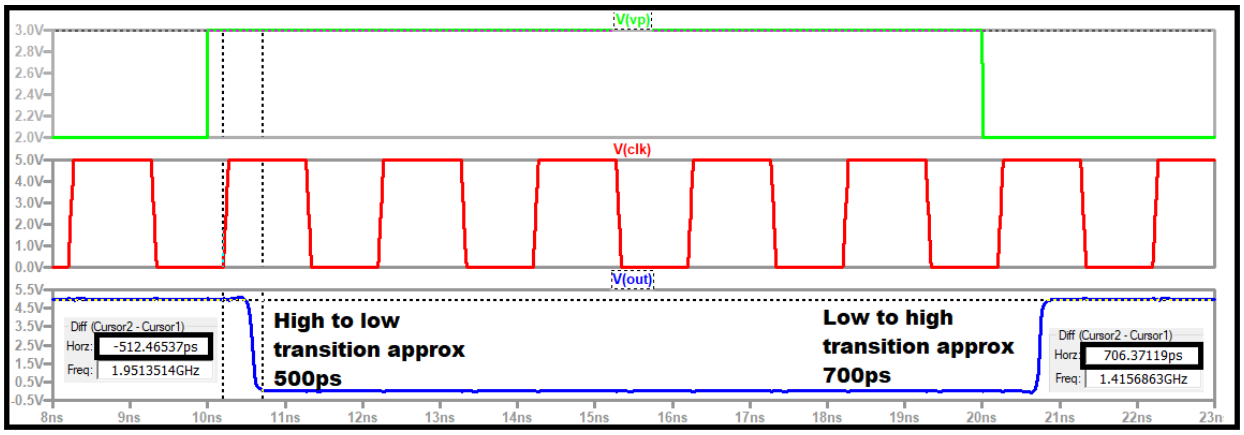

Figure 4: Comparator swing and transition times

3.4 Clock Edges

The K-path topologies all require designing clock edges with 'K' evenly spaced phases over the interval of one cycle of the sampling frequency. For example, the 8-path topologies require eight evenly spaced, 1.25ns clock edges over a 10ns, or 100MHz, sampling interval. These clocks are ultimately used on eight clocked comparators with an ideal 50% duty ratio to give precise switching in the feedback path. This is relevant as it allows only a single feedpack path to be differentiated at a given time. The methodology for designing both the 50MHz and 100MHz clocks is identical, thus only the 100MHz clock will be discussed.

A ring-oscillator was designed to create eight evenly spaced clock edges, seen below in Figure 5, over a single period to implement a at a maximum f_s of approximately 100MHz. The simulation results below can be found in the file ***clock_gen_x8_test.***

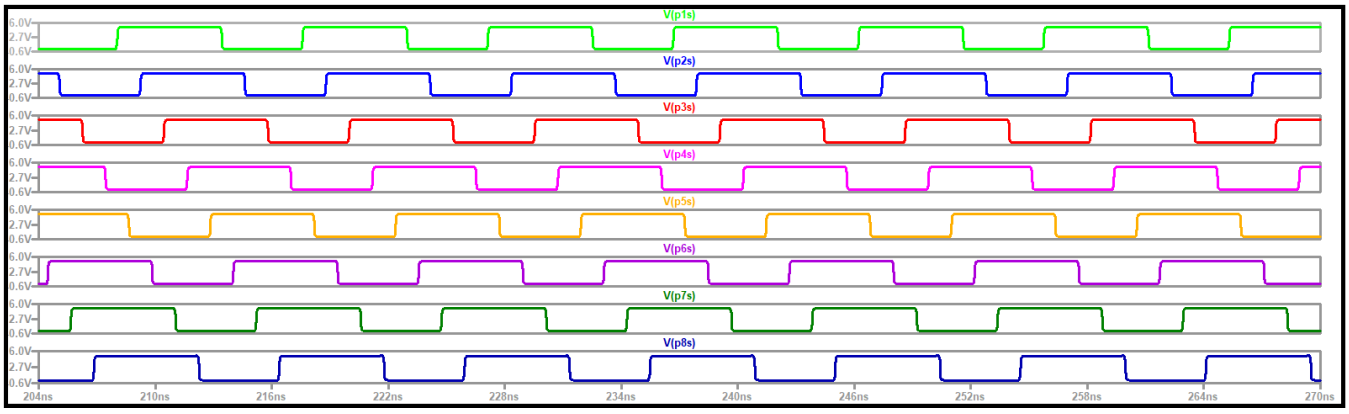

Figure 5: 100MHz clock with 8 edges spaced by approximately 1.23ns

To achieve a 50% duty cycle, the separation between edges needed to be 1.25ns. The designed oscillator does not meet this ideal constraint with a duty cycle of approximately 53%. This was the limiting factor in an abandoned attempt to implement a topology using both the rising and falling clock edges of four clocks, similar to DDR, to reduce the number of components. Additionally, this gave a

non-ideal overlapping of capture windows in the feedback path that resulted in small periods where two sequential paths were on at the same time.

The ring oscillator design uses four SR delay stages and a bias generator, both seen below in Figure 6. Each delay uses additional, oversized inverters to keep the clock independent of the load and thus allow the middle outputs to propagate to the next delay stage.

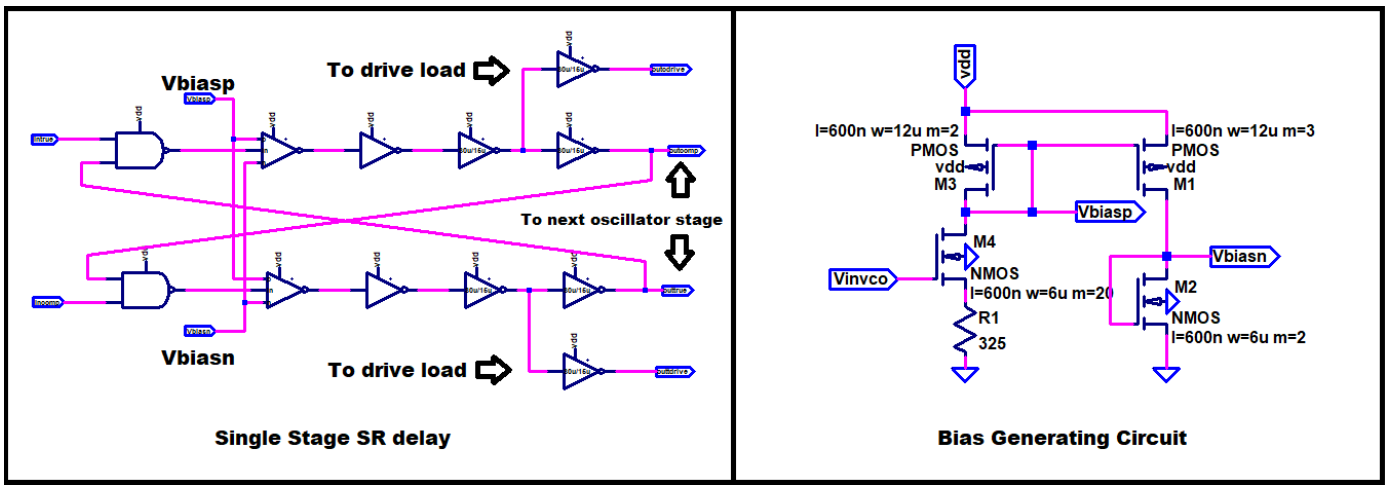

Figure 6: Single stage SR delay (left) and bias generation circuit (right)

Note, the first inverter in the delay stage uses a current-starved topology, seen below in Figure 7.

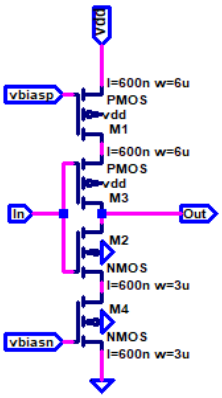

Figure 7: Current starved inverter topology

This inverter is controlled by the bias voltages, Vbiasp and Vbiasn, that are set by the bias generating circuit input voltage, Vinvco. The goal of the bias generation circuit was to create biasing with a linear adjustment range as seen below in Figure 8. The simulation results found in the file ***BiasGen_test*** show the linear region varies from approximately 700mV to 2.3V.

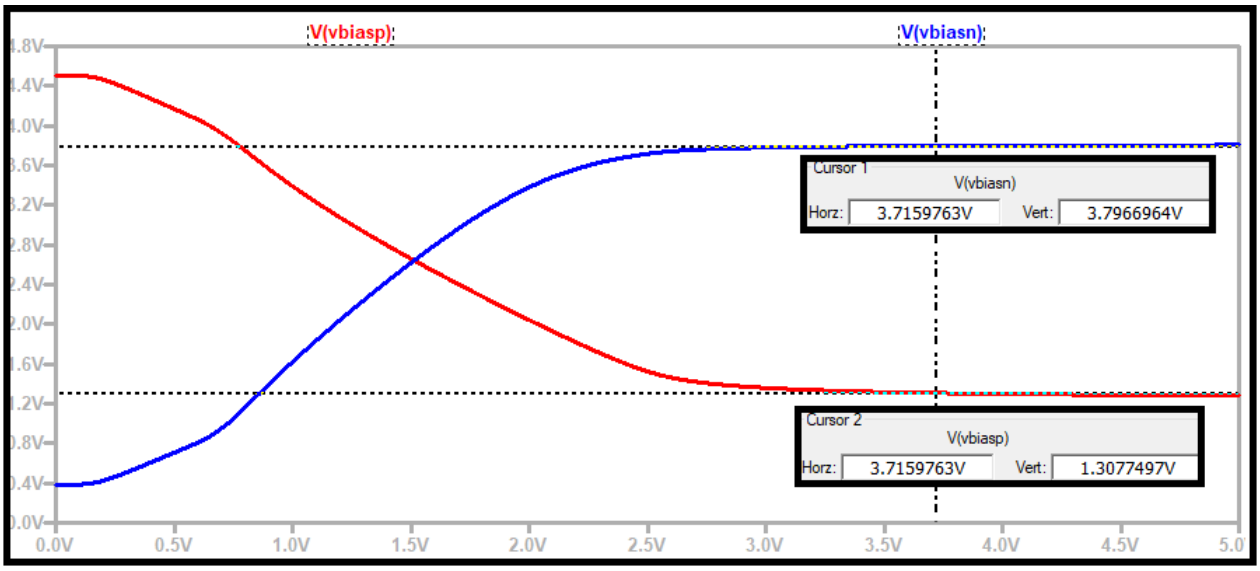

Figure 8 Vbiasn and Vbiasp

Varying Vinvco allows the frequency of the clock to be adjusted over a wide range by choking off or opening a path for current to flow in the inverter. Simulation results found in the file ***clock_gen_x8_sweepVinvco*** for steps of 0.75V, 1V and 5V show a frequency range of approximately 18MHz to 107MHz, as seen in Figure 9 below.

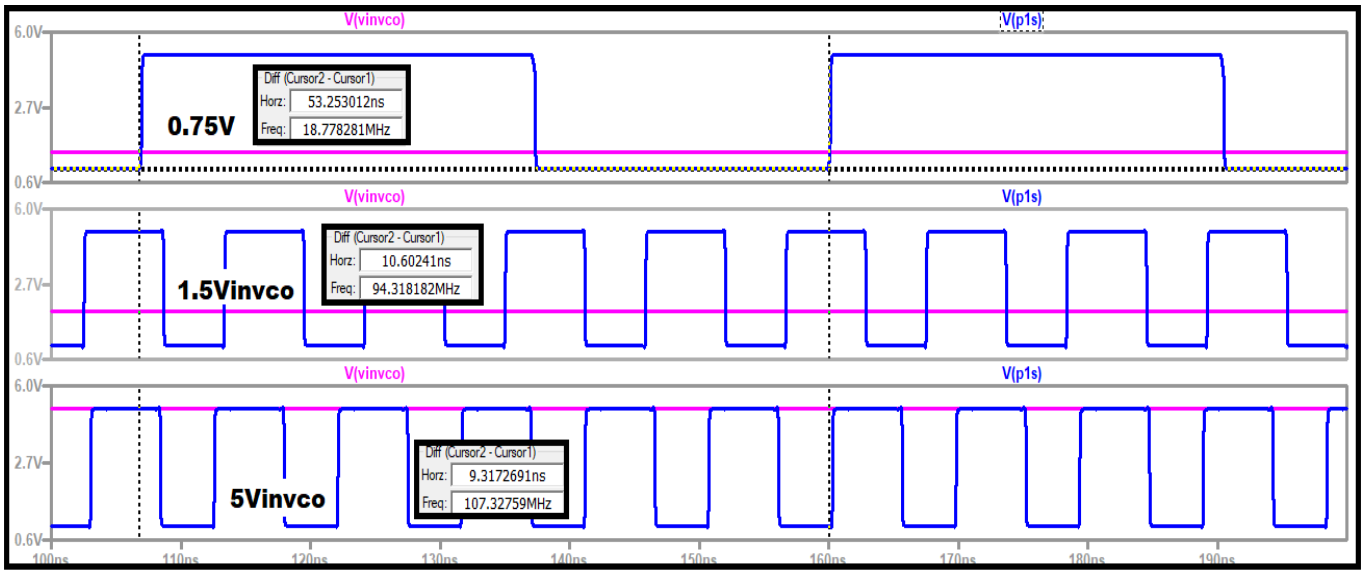

Figure 9: Frequency range of ring oscillator

The same methodology was used to design a ring oscillator with 16 equally spaced edges over a clock period, however the sampling period frequency was reduced to approximately 50MHz such that the new sampling frequency was not too fast for the integrator. Figure 10 below displays the 16 clock edges to validate a working design. The related simulation file is ***clock_gen_x16_test***. Figure 11 below shows the duty cycle for the 16 phase clock.

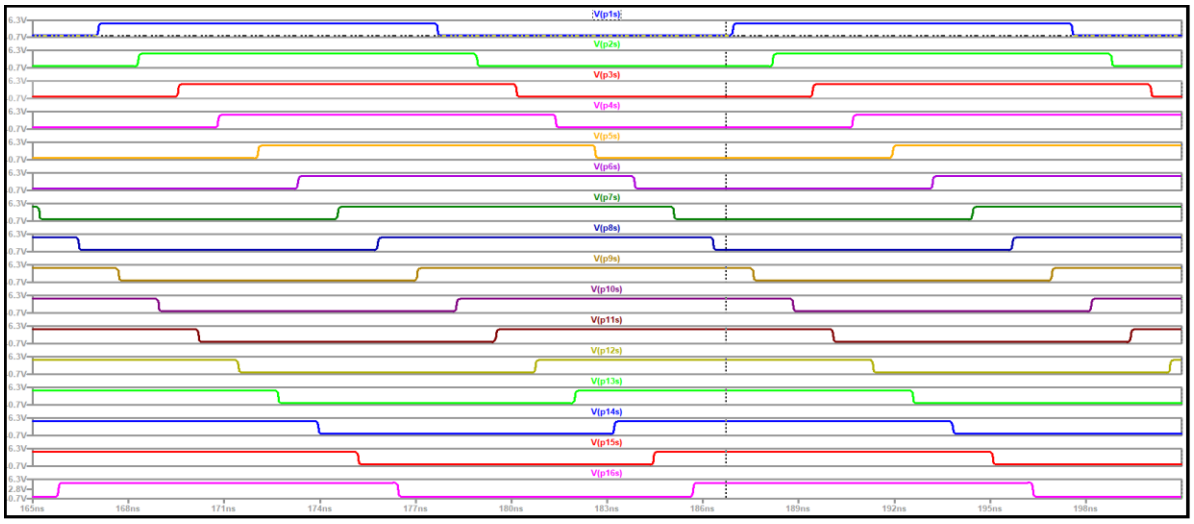

Figure 10: 16-path ring oscillator edges

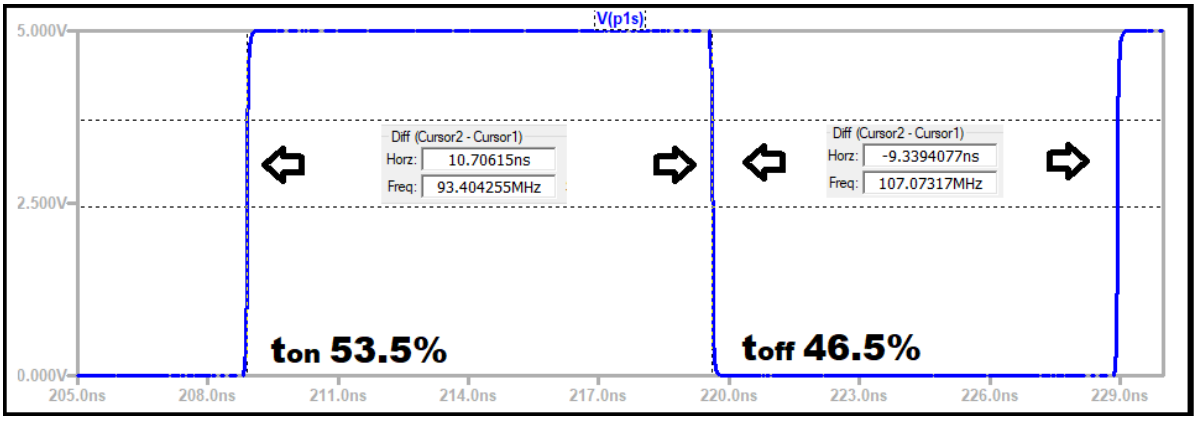

Figure 11: Duty cycle of 16 phase ring oscillator

3.5 Transmission Gate Switches

As discussed earlier, simple transmission gate (TG) switches, seen in Figure 12, control the feedback path and connect or disconnect a given K-path from the integrator summing junction.

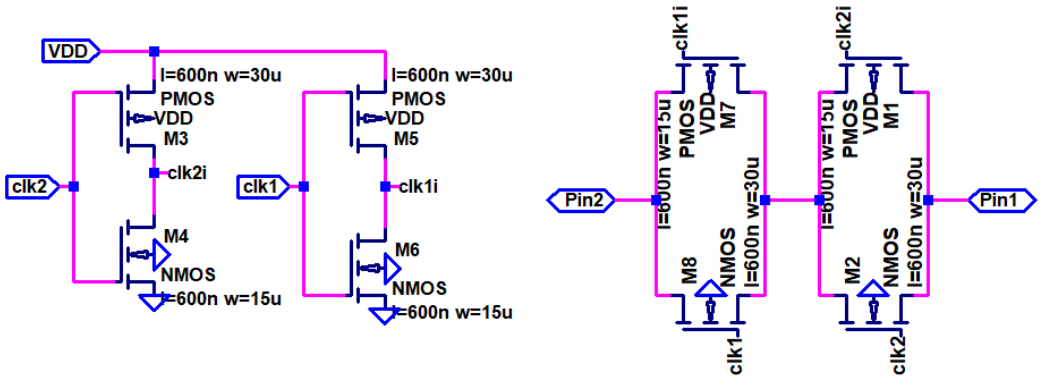

Figure 12: TG switching circuit

The TG switches were simulated in a basic resistive divider circuit to give an estimate of what type of resistance to expect due to TG's providing nonlinear resistance. The basic relationship for the resistive divider is as follows

$$R_{switch} \approx \frac{V_{out} * R_2}{V_{in} - V_{out}} \approx \frac{V_{out} * 500\Omega}{5 - V_{out}}$$

Two different switches, switch_x2.asc and switch_x2_v2.asc, were used and are seen in the Figure 13 below along with simulation results.

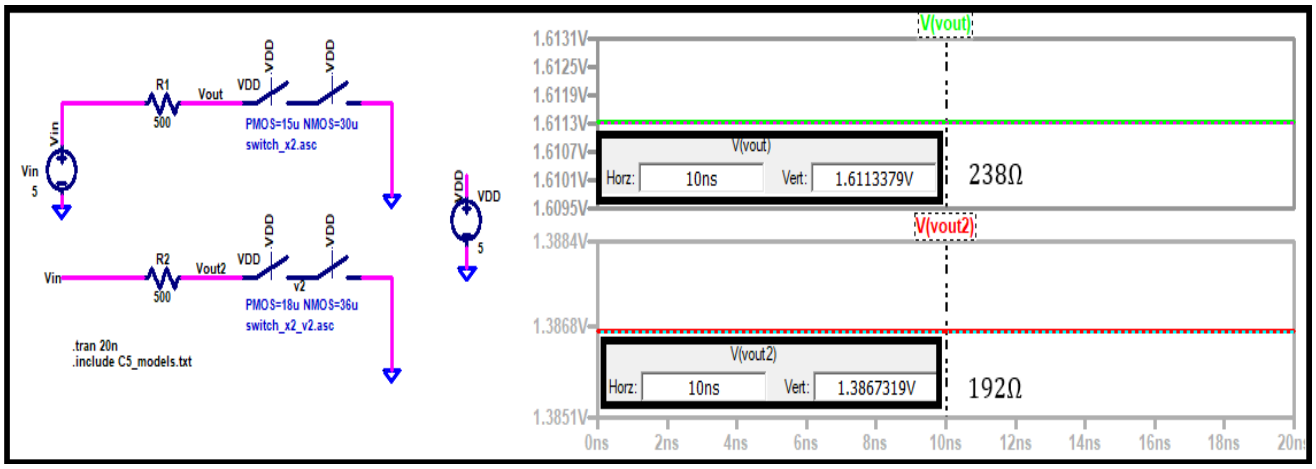

Figure 13: TG resistance simulation results

The simulation results show the first switch resistance, *switch_x2*, is approximately 238Ω, and the second switch, *switch_x2_v2*, is approximately 192Ω. To mitigate the effect of this resistance on the input and feedback signals, a TG switch was also placed in the input signal path with both switches tied high. Additionally, a larger resistor relative to the TG switch resistance was placed in each path. This ideally helps to equate the path resistances by giving each path a larger resistance that dominates the path.

3.6 Feedback Control

The TG switches are controlled in sequence with the clocks and are connected such that each K-path has a clocked comparator feeding back to the resistor and TG switches discussed in Section 3.5 and eventually back to the summing node of the integrator. Two separate K-paths are seen below in Figure 14.

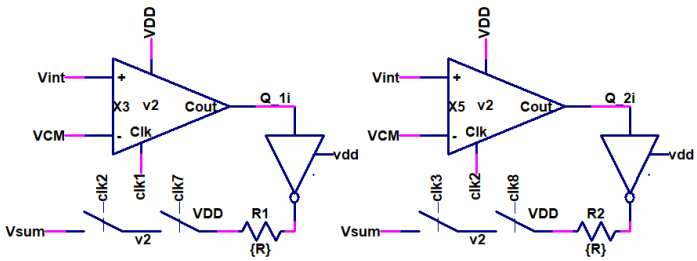

Figure 14: Two separate K-paths

The clocking sequence for the above paths is seen below in Figure 15, using file ***clock_gen_x8_capture***, with the top and bottom panels representing the logic for the left and right circuits, respectively, in Fig. 14. The comparators are clocked as discussed earlier, but the feedback path is not enabled until the time when both switches are on, as indicated by the 'X' in Fig. 15. In Fig. 14, the K-path on the left first sees clk 7 switch on, and next the comparator is clocked. However, the feedback is not energized until clock 2 goes high and both TG switches are on at the same time. When clk 7 goes low, the feedback path is disconnected. However, we see in Fig. 15 the next stage has both switches on and the second path is now connected. The process iterates over K-paths, in this case 8, and repeats iteratively as seen below in Figure 15.

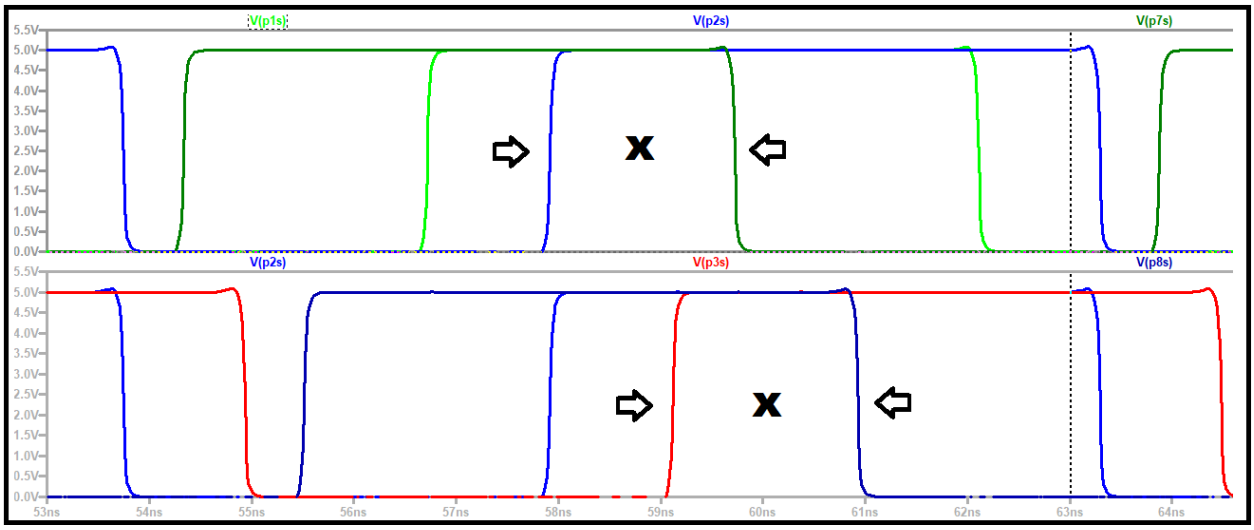

Figure 15: Feedback control logic

Figure 16 below shows the process for all K-paths. Note, there is overlap of the clock signals due to the duty cycle not being precisely 50%. Although the report only details the capture windows and logic control for the 8 K-path topologies, the same logic is used for the 16-path topology.

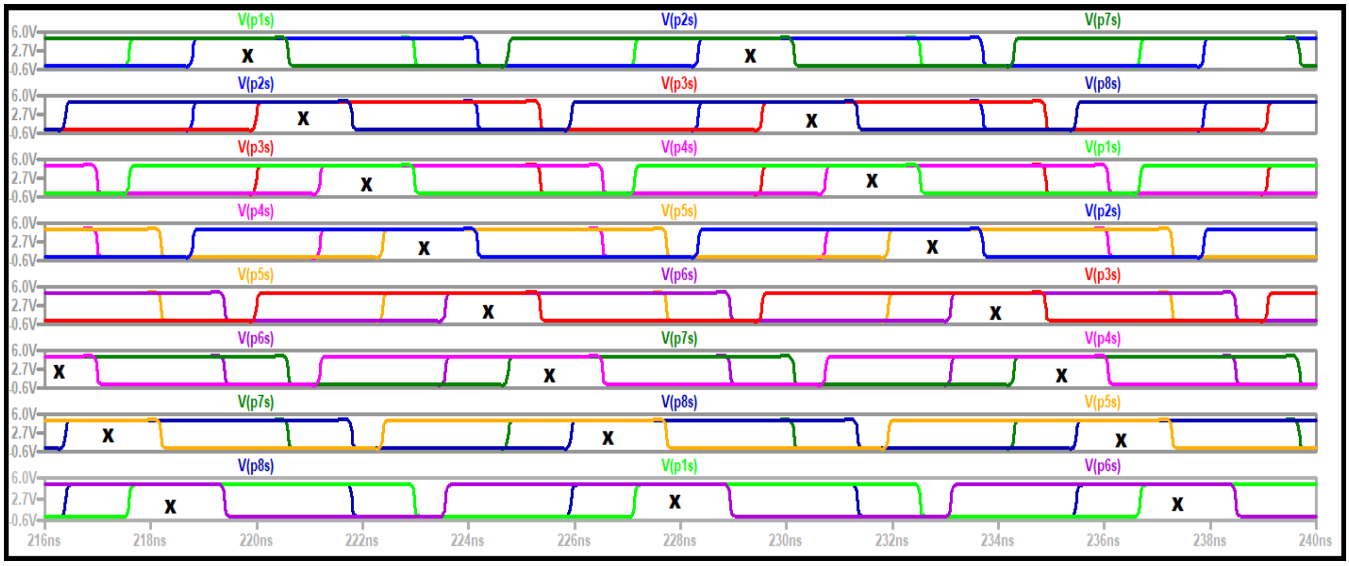

Figure 16: Feedback control iterative clocking sequence

3.7 Operational Amplifier

The operational amplifier in the delta-sigma ADC acts as an active integrator to perform the integration required for the averaging. One of the advantages of using a delta-sigma topology is the ability to use less accurate analog components in the forward path. This is due to the feedback path being able to desensitize component mismatches and any nonlinearities present in the forward path. The ideal signal transfer function in the forward path of a noise-shaping modulator is unity, thus the op-amp can have low gain. Due to these relaxed specifications, the simple self-biasing differential amplifier seen below in Figure 17 was selected for the topologies, although the gain was lowered for each design.

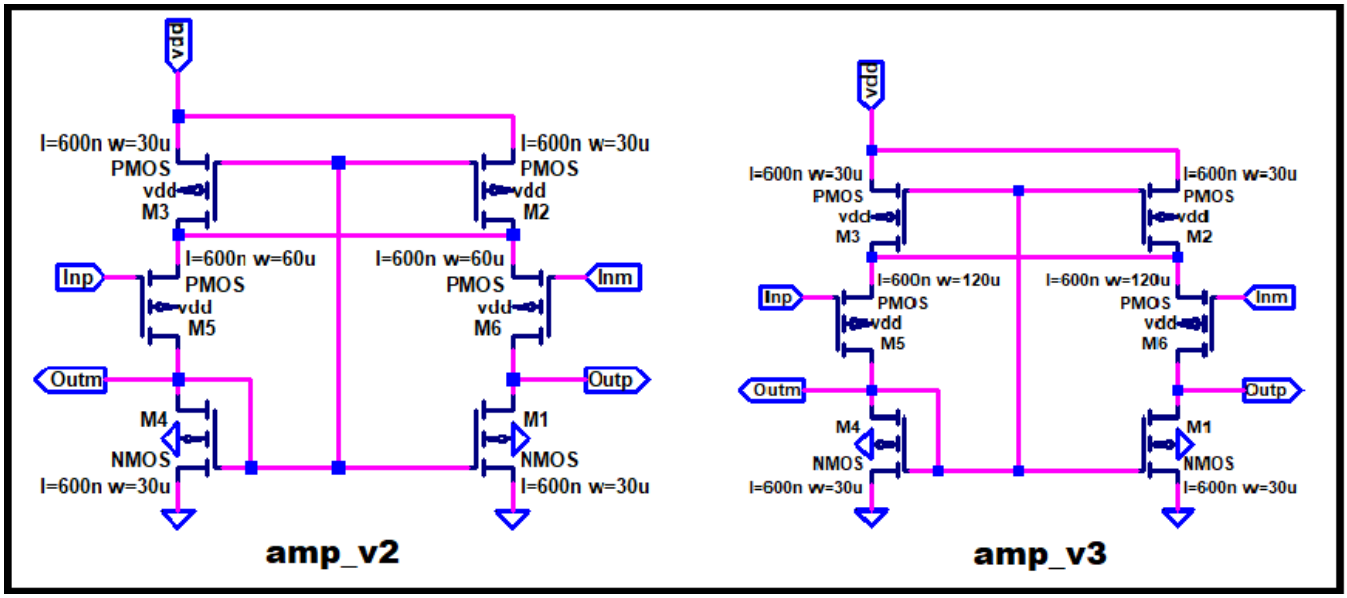

Figure 17 Self-biasing op-amps

Table 6 contains basic figures of merit for the op-amp design. The minimum unity gain frequency is governed by the following

$$f_{un} = K * B = f_s/2$$

such that for this design the gain-bandwidth product needs to be at least 50MHz for f_s equal to 100MHz and 25MHz for f_s equal to 50MHz. The AC open loop response simulation found in the file ***op_amp_AC_open_loop*** and seen in Figure 18 below show this op-amp easily meets the design specifications.

KD1S	1st order 8-path	1st order 16-path	2nd order 8-path
op amp file	amp_v3	amp_v3	amp_v2
f_{un}	735MHz	735MHz	447MHz
AoI_{DC}	16.3	16.3	13.0
Settling time	1.1ns	800ps	800ps

Table 7: Op Amp Characteristics

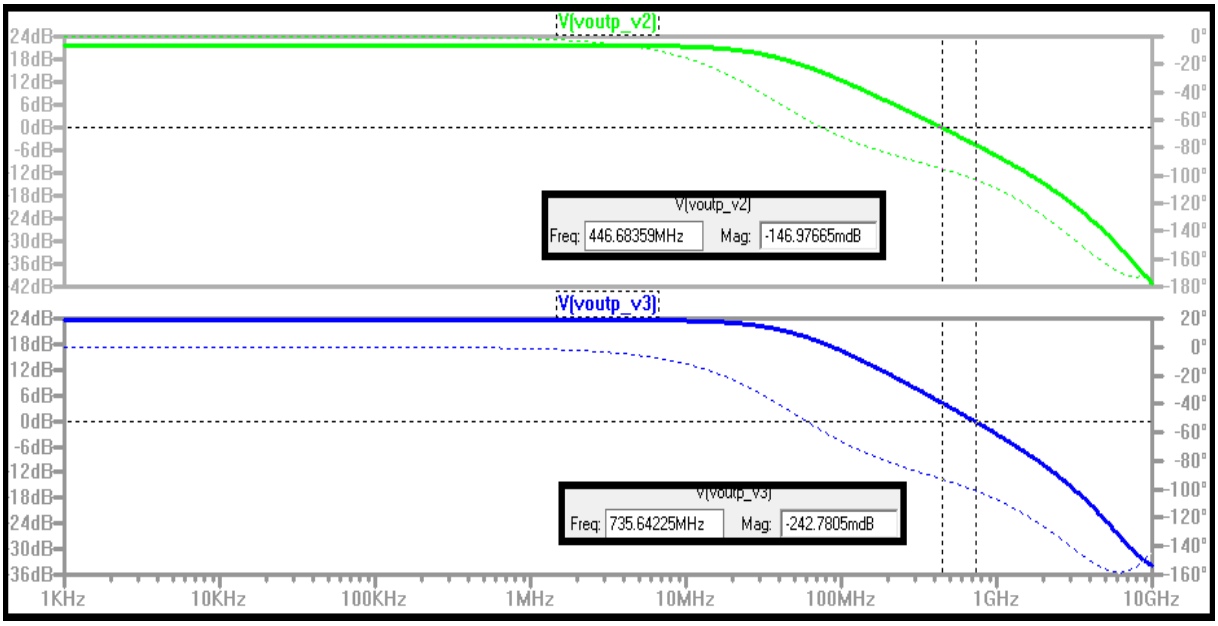

Figure 18: Op-amp open loop frequency response

Figure 19 below was generated using the schematic ***amp_test*** and displays the DC open loop gain of the op amps.

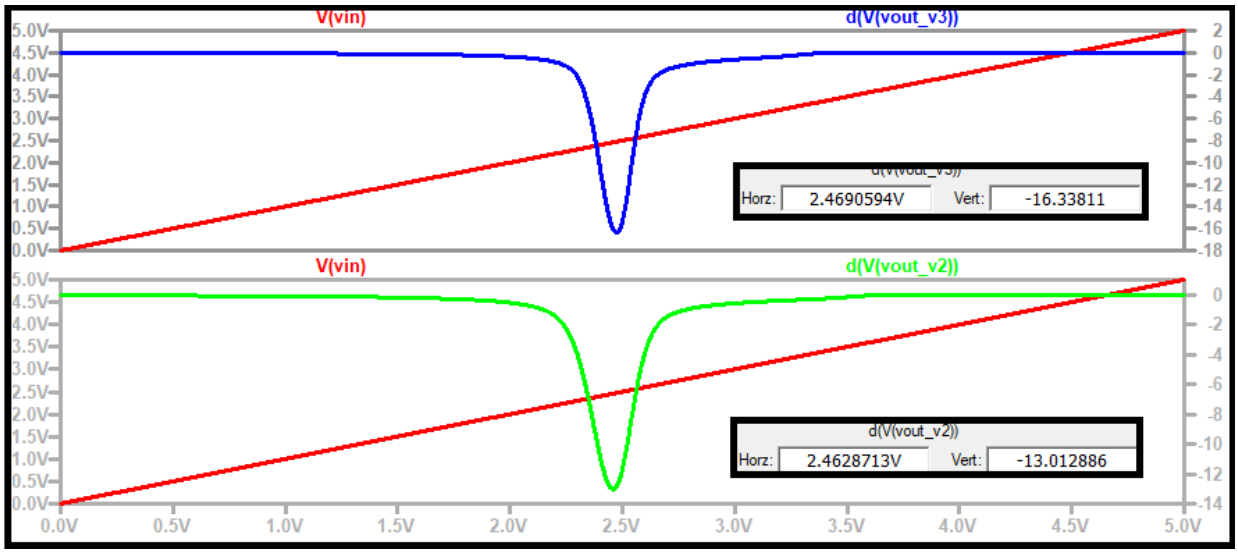

Figure 19: Op-amp $AolDC$

The last specification of interest is settling time. A fast settling time is important such that the output reaches the ideal final value and to avoid incomplete setting. To avoid this, f_{un} needs to be much larger than f_s. This represents one of the fundamental oversights made during the design process. The op-amp gain was reduced during simulations without performing settling time simulations to determine the overall impact on the design. This oversight led to slower than expected settling time, as seen in Figure 20 and found in file ***amp_tran***. Despite this the ADC designs still performed relatively well, but missing the opportunity to increase performance is disappointing. Future iterations of these designs will take this into consideration as a starting point for improvement.

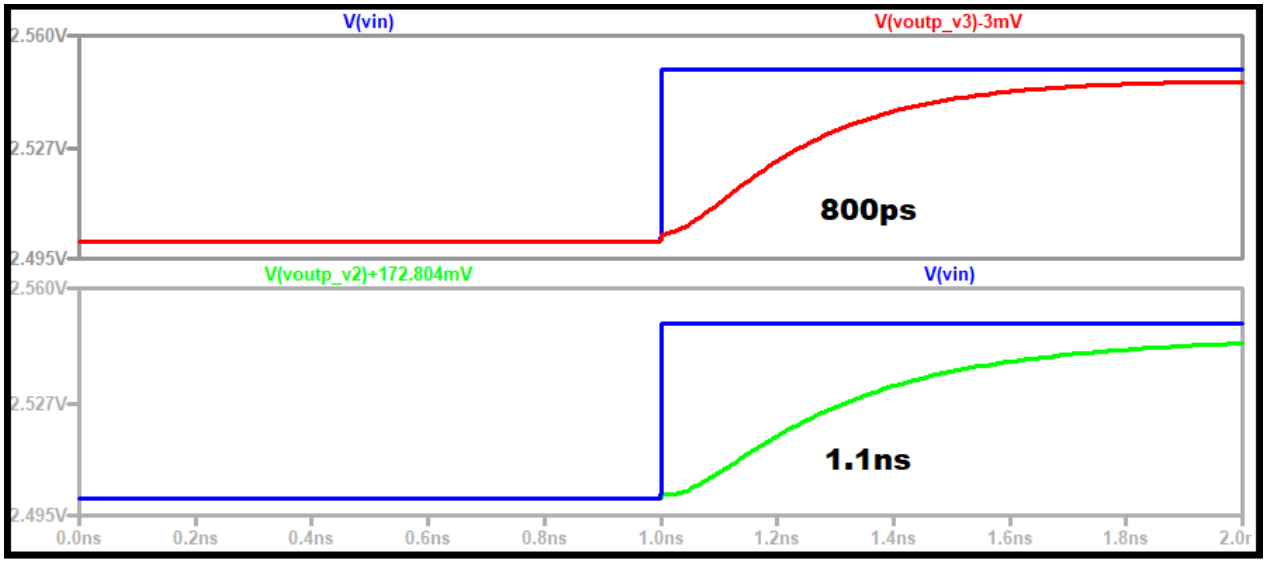

Figure 20: Settling Time

4. ADC Design Topologies

4.1 1st order 8-path NS ADC

The first topology designed was a 1st-order NS modulator due to the added complexity regarding the stability of higher order NS modulators and as a matter of practical experimentation. Designing the first order topology to match the theoretical foundation presented in the course allowed for a simpler learning curve. The schematic for the 8-path first order topology is displayed below in Figure 21 and found in file ***ADC_MONAHAN_CT_8D1S_1st_order_1MHz***.

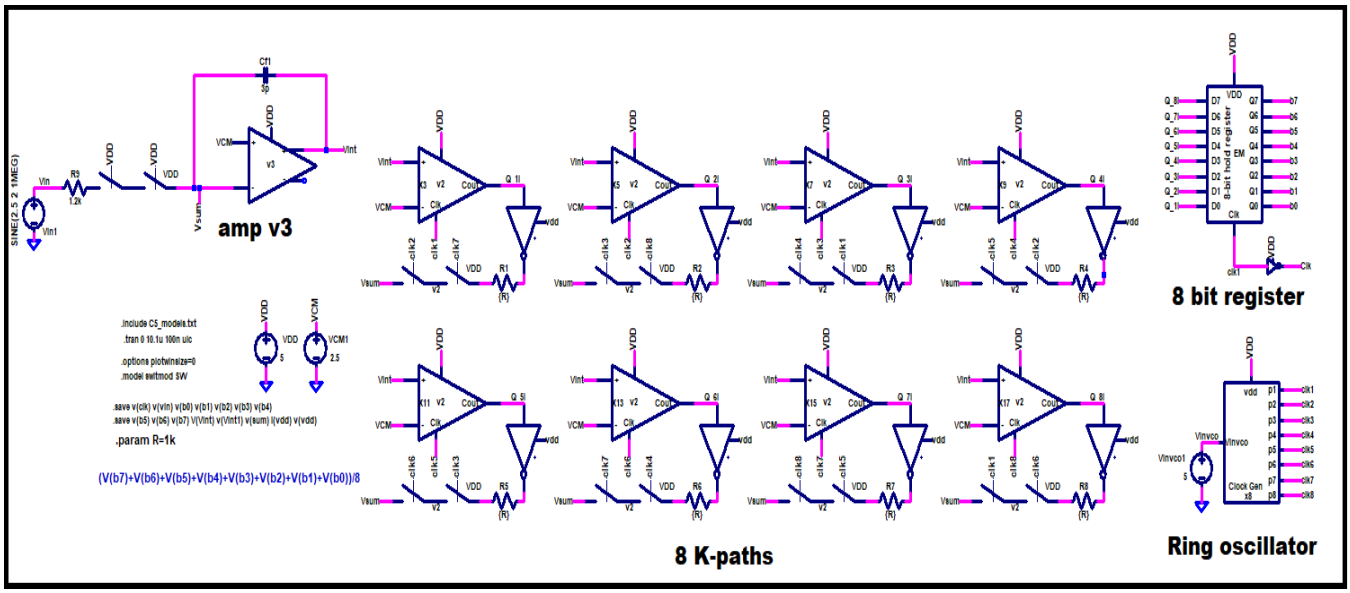

Figure 21: 1st

The clocked comparator was changed for higher speed along with the op-amp. The op-amp gain was reduced from approximately 24 to 16 to attempt to conserve power and to keep the integrator capacitor and feedback resistance smaller. During simulations this resulted in better performance, however in hindsight the tradeoff for op-amp speed was not worth the lower gain.

4.1.1 1st order 8-path NS ADC Simulation Results

The LTSpice transient simulation results are displayed in Figure 22 below. The red trace shows the input to the comparator is not saturating. In the bottom panel, the converted output can be seen to be closely following the input signal. Similar results will be demonstrated for each of the next two topologies. The top panel is simply included to measure power consumption.

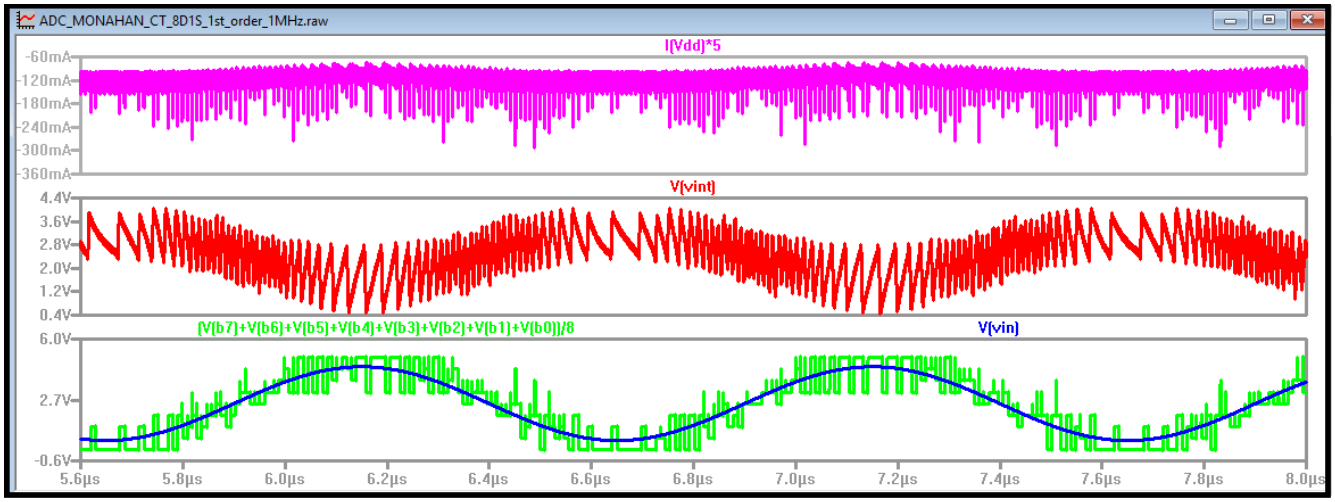

Figure 22: 1st order 8D1C NS Modulator transient simulation results

Next, a slow input ramp was simulated for DC characterization. Figure 23 below shows the ramp demonstrates no real dead zones or marginal gain error. The ramp simulation is found in the file ***ADC_MONAHAN_CT_8D1S_1st_order_1MHz_RAMP*.**

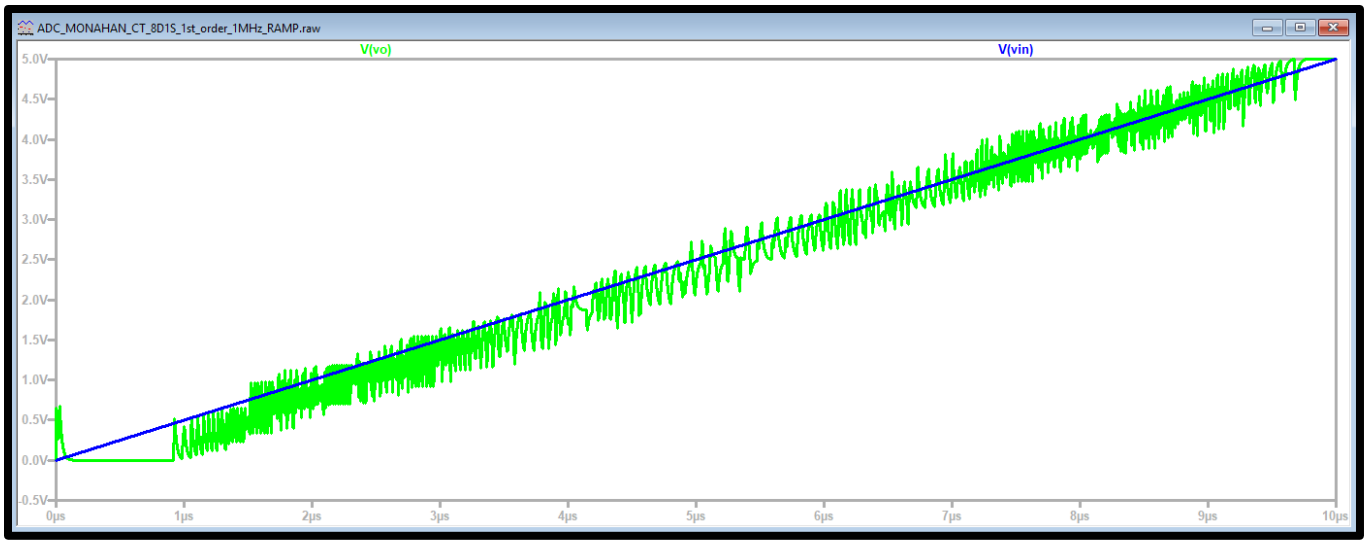

Figure 23: DC Characterization 1st order 8-path NS ADC

The results for this topology are documented in Table 3, but the results for OSR equal to 256 are included again here for quick reference.

KD1S	Serial256	Parallel256
$f_{s,new}$ (MHz)	846	106
SNR (dB)	55.97	55.32
N_{eff} (bits)	9.00	8.89
Bandwidth (MHz)	1.65	1.65

Table 8: 1st order K=8 OSR 256

MATLAB was used for digital filtering of all three modulator topologies to reconstruct the output signal for comparison to the input signal. The following MATLAB plots generate results for comparison to Figure 9.33 as seen in Figure 24 below.

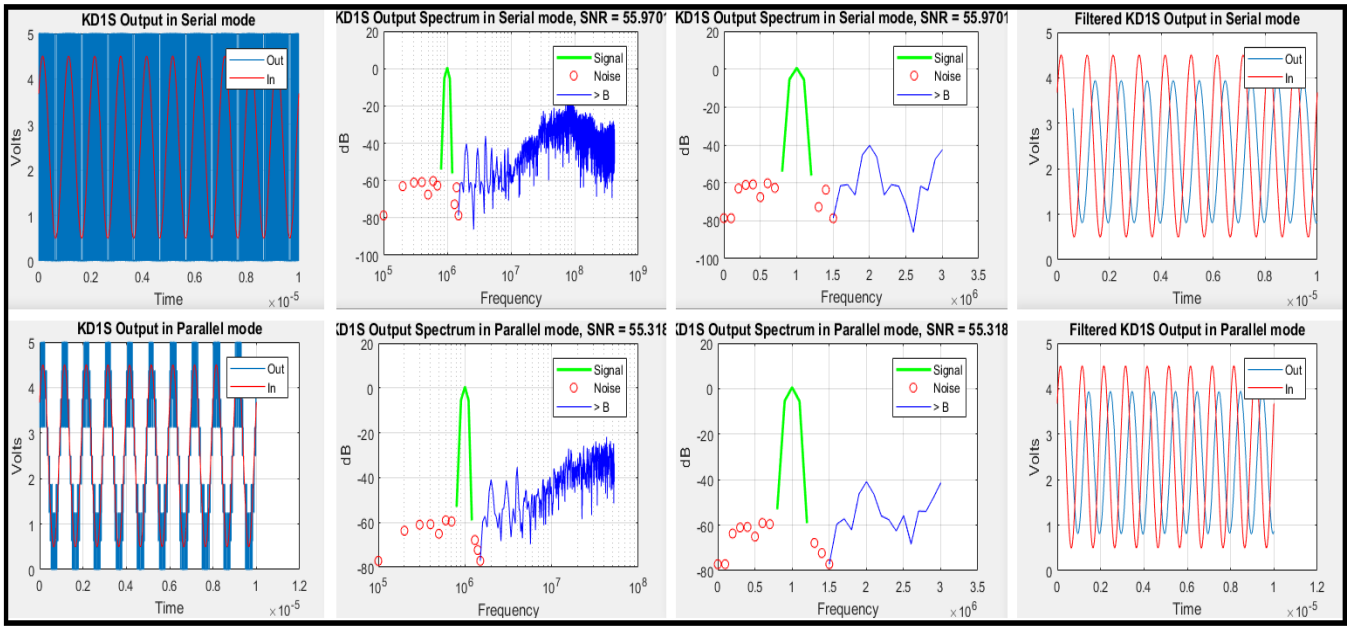

Figure 24: 8D1S 1st-order NS Modulator MATLAB RESULTS for OSR =256 at 1MHz

The plots above were generated using ***ADC_MONAHAN_CT_8D1S_1st_order_1MHz.m***. The results demonstrate the noise shaping capability of the modulator. We can see the noise has been pushed out to higher frequencies as designed. Additionally, it is visible in the transient results that at a higher OSR the input signal is attenuated.

4.2 2nd order 8-path NS ADC

The second design, seen in Figure 25, attempted to implement the design discussed above as a second-order variation to see if the performance could be increased. Theoretically, a second-order topology should outperform a first order topology. Adding a second integrator to the forward path and adjusting the gain ideally allows the comparator gain to increase by keeping the comparator input node as small as possible. An additional change was lowering the gain of the op-amps, in this case to thirteen using ***amp_v2***. Using the first amplifier was resulting in quite a bit of saturation. Increasing the capacitor helped, but the performance seemed to stabilize once the gain was reduced. The schematic and simulation results are found in file ***ADC_MONAHAN_CT_8D1S_2nd_order_1MHz.***

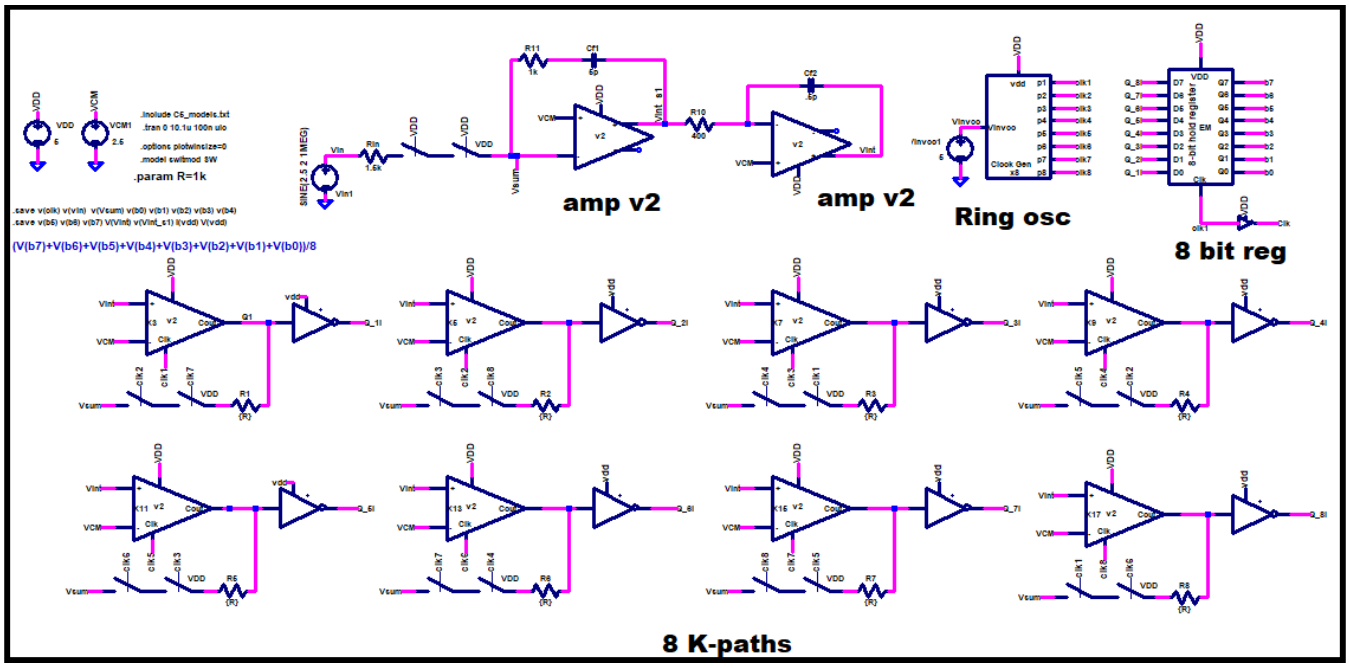

Figure 25: 2nd-order 8D1S Modulator

4.2.1 2nd order 8 path NS ADC Simulation Results

The LTSpice transient simulation results are displayed in Figure 26 below. There is evidence of some slight saturation in the integration node, but this was not addressed due to time constraints related to the desire to attempt another topology. However, the performance is still good.

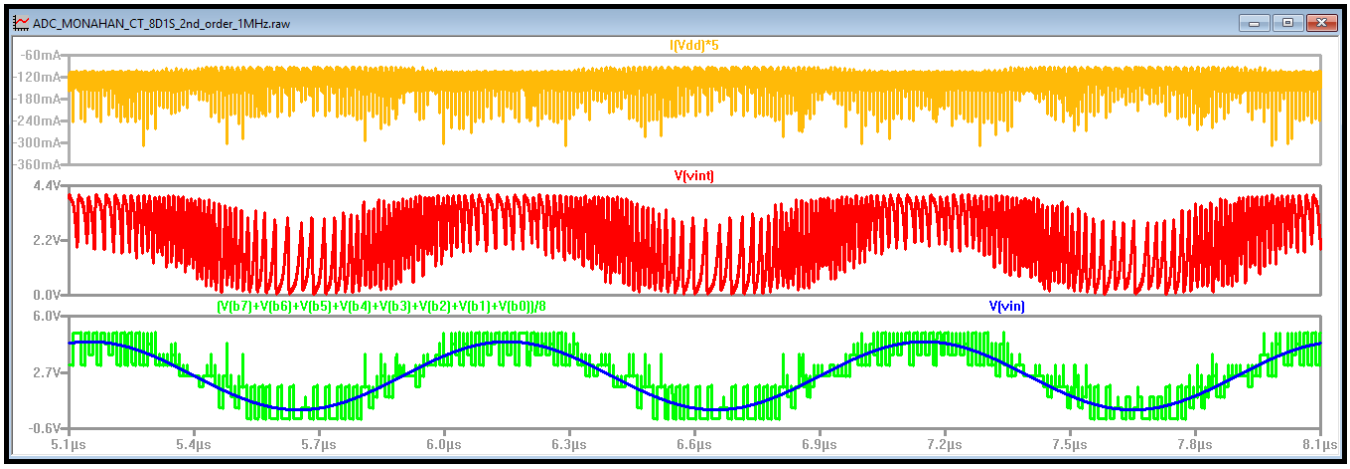

Figure 26 : 2nd order 8D1C NS Modulator transient simulation results

The DC characteristics for this design, seen in Figure 27 below, again demonstrate no bad dead zones and a slight gain error, but overall the performance is good. The simulation file is ***ADC_MONAHAN_CT_8D1S_2nd_order_1MHz_RAMP.***

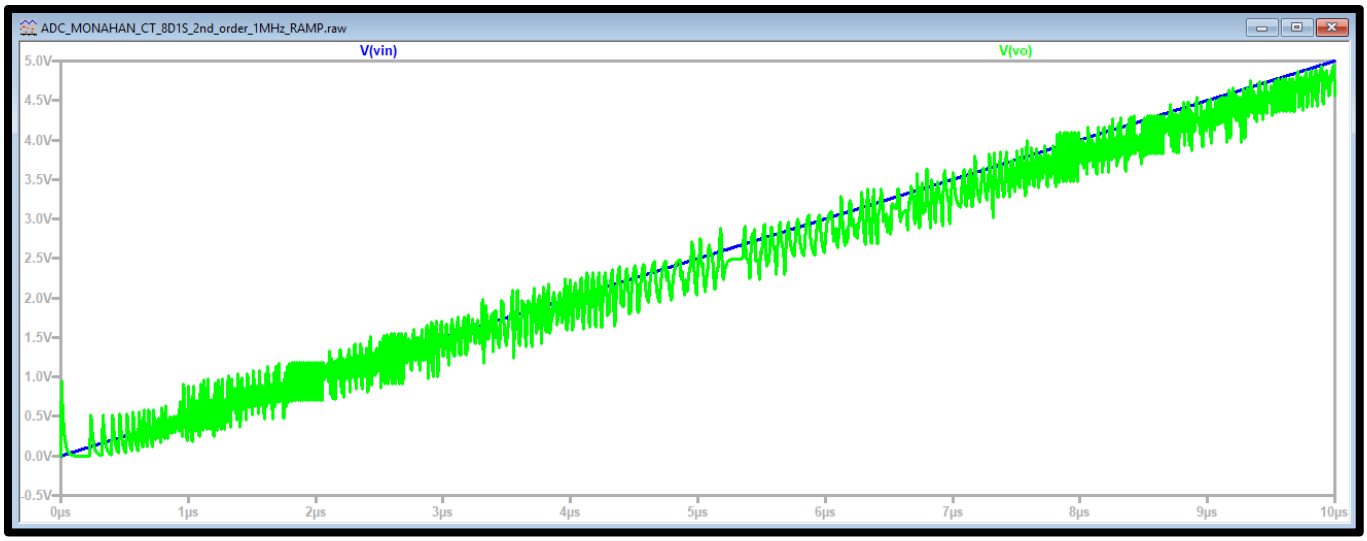

Figure 27: DC Characterization 2nd order 8-path NS AD C

The results for this design are documented in Table 4, but the results for an OSR equal to 256 are included again here for quick reference.

KD1S	Serial256	Parallel256
$f_{s,new}$ (MHz)	846	106
SNR (dB)	57.86	57.67
N_{eff} (bits)	9.32	9.28
Bandwidth (MHz)	1.65	1.65

Table 9: 2nd order K=8 OSR 256

The following MATLAB plots were generated using ***ADC_MONAHAN_CT_8D1S_16path_1st_1MHz.m***.

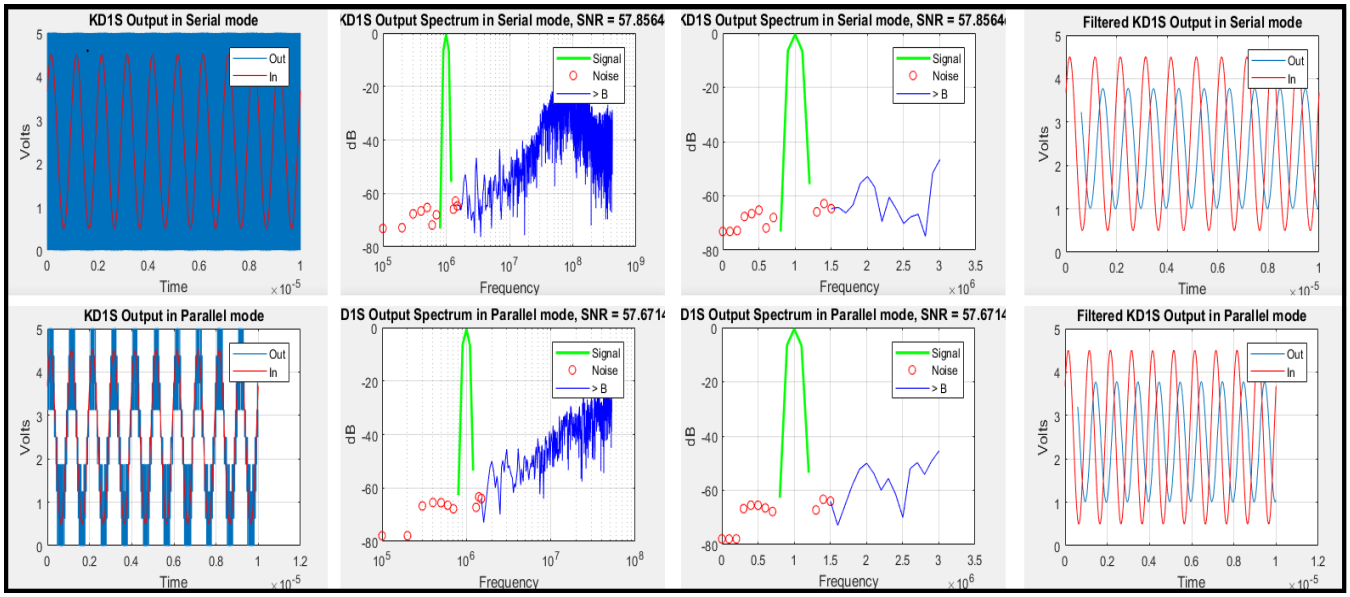

Figure 28: 8D1S 2nd-order NS Modulator MATLAB RESULTS for OSR =256 at 1MHz

Figure 28 shows the performance of this topology is better than the first-order performance. In hindsight, the better strategy would have been to attempt to increase the performance of this design, rather than moving on to attempting a third design. However, the simulation results favorably compare to Fig. 9.33.

4.2.1 2nd order 8 path NS ADC Simulation Results

4.3 1st order 16-path NS ADC

The final design attempted is a 16 K-path first order topology seen in Figure 29 below. This is the same fundamental topology as detailed in Section 4.1 with the addition of a 16-bit register, a new ring oscillator designed for 16-paths, and a larger integrating capacitor. The interest in this design stemmed from a desire to see how more paths would impact performance, as well as wanting to attempt to create a larger scale design. The overlap in the capture window between sequential paths of this design was a little worse than the 8-path version. The schematic and simulation can be found in the file ***ADC_MONAHAN_CT_8D1S_16path_1st_1MHz.***

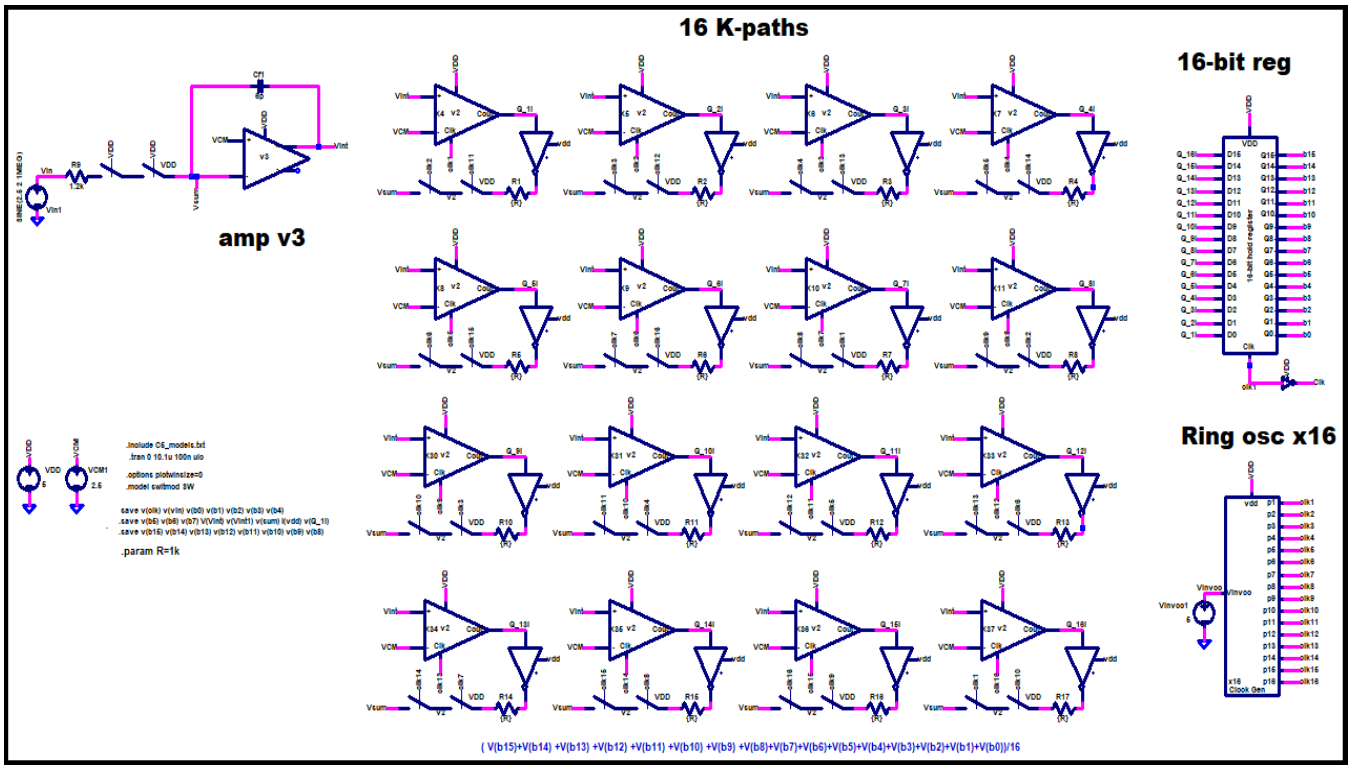

Figure 29: 1st-order 16D1S Modulator

4.3.1 1st order 16-path NS ADC Simulation Results

The LTSpice transient simulation results are displayed in Figure 30 below. The results seem comparable to earlier designs.

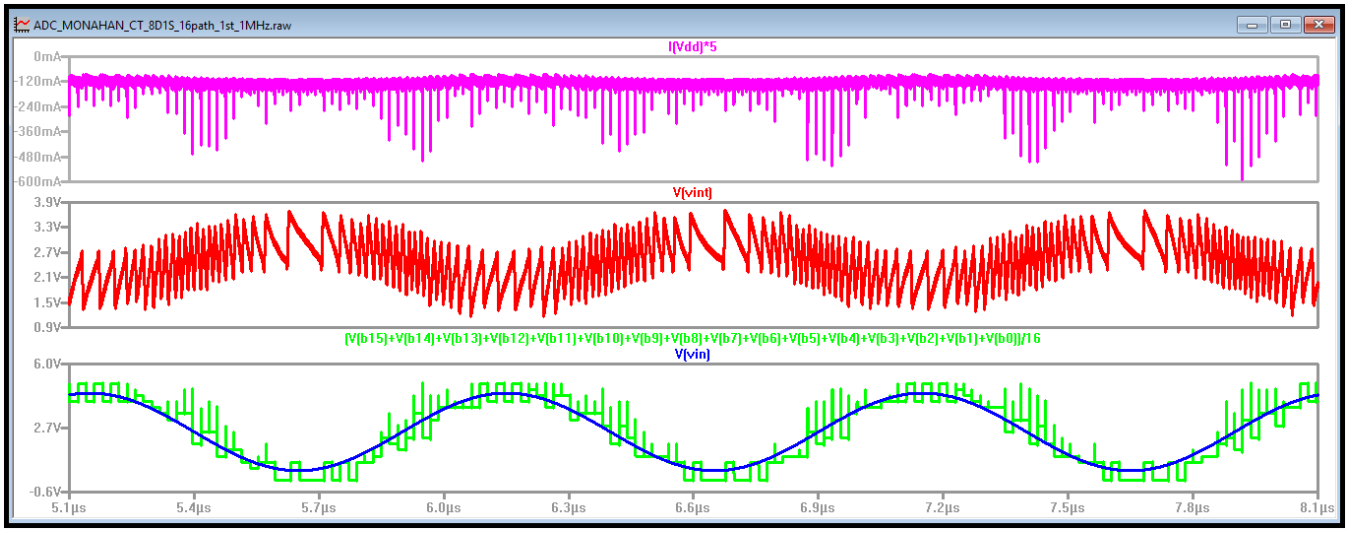

Figure 30: 1st order 16D1C NS Modulator transient simulation results

The DC characteristics of this design, seen in Figure 31 below, show the performance drops off a little with multiple dead zones and some gain error, although the output code does follow the ramp fairly well. Time permitting, this flaw would have been addressed with the belief it could have been corrected and resulted in the overall best performance. The simulation file is ***ADC_MONAHAN_CT_8D1S_1st_order_1MHz_RAMP.***

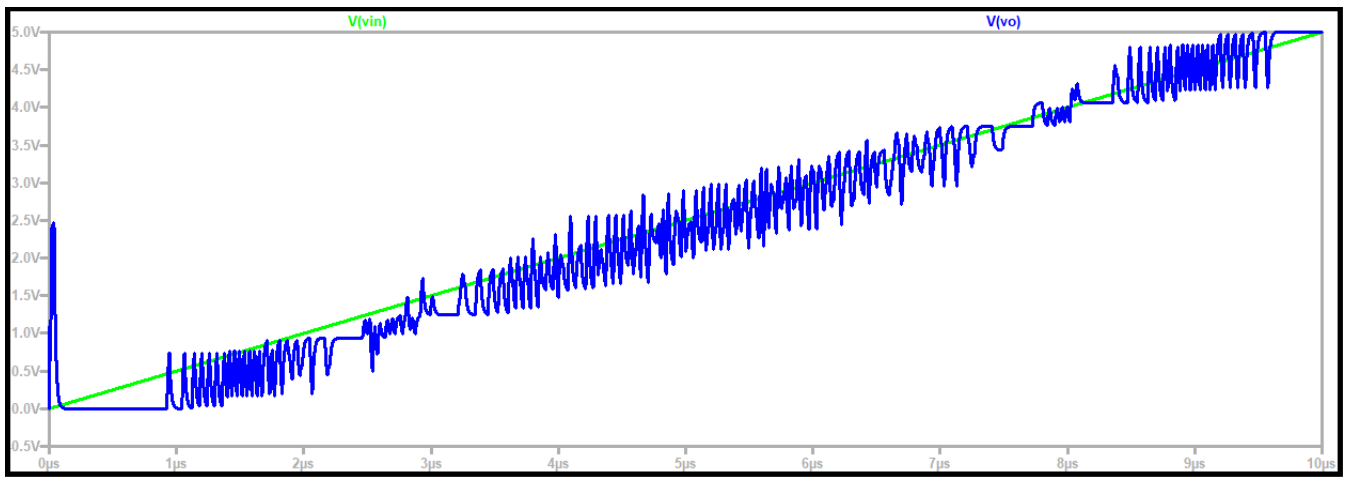

Figure 31: DC Characterization 1st order 16-path NS ADC

The results for this design are documented in Table 5, however the results for OSR equal to 256 are included again here for quick reference.

KD1S	Serial256	Parallel256
$f_{s,new}$ (MHz)	813	51
SNR (dB)	58.35	53.38
N_{eff} (bits)	9.40	8.57
Bandwidth (MHz)	1.59	1.58

Table 10: 1st order K=16 OSR 256

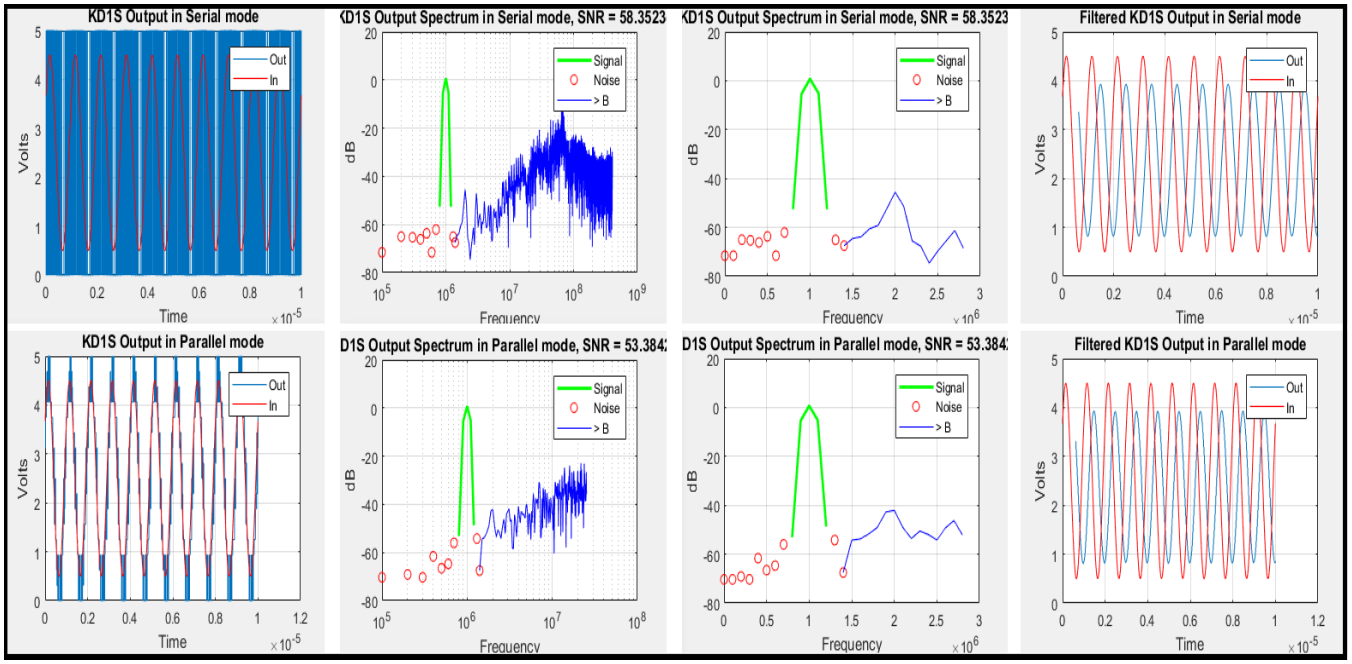

Figure 31: 16D1S 1st-order NS Modulator MATLAB RESULTS for OSR =256 at 1MHz

Figure 31 above uses file *ADC_MONAHAN_CT_8D1S_16path_1st_1MHz.m*. The digitally filtered results demonstrate the performance of this design gives respectable overall specifications, but the dead zones in the DC ramp simulation are of concern and need to be addressed in future iterations of this design.

5. Final Design and Result Synopsis

The second-order 8D1S NS modulator is the design selected for submission. The performance slightly exceeds the single-order 8D1S, however the belief is the design has better overall characteristics. This includes increased randomization of noise in the feedback path to limit patterning in the output spectrum. Note, the $SNR_{ideal,}$ calculated in Section 3.1, does not match the simulated values seen below. A side by side comparison of all three designs and Figure 33 for an OSR of 256 is include in Table 11 below.

Specification	Fig 9.33 1st	Fig 9.33 2nd	1st order 8-path	2nd order	1st-order 16-path
Serial					
$f_{s,new}$ (MHz)	1828	1709	846	846	813
SNR (dB)	52.99	64.39	55.97	57.86	58.35
Serial N_{eff} (bits)	8.51	10.40	9.00	9.32	9.40
Bandwidth (MHz)	3.57	3.34	1.65	1.65	1.59
Parallel					
$f_{s,new}$ (MHz)	228	213	106	106	51

SNR (dB)	51.66	61.95	55.32	57.67	53.38
Serial N_{eff} (bits)	8.29	9.99	8.89	9.28	8.57
Bandwidth (MHz)	3.57	3.34	1.65	1.65	1.58

Table 11: Final Comparisons for OSR 256

As seen above, the 2nd-order topology had the best overall performance of the three designs, although the other designs did perform well.

6. Conclusion

The ECG 722 course design project, designing a KD1S NS Modulator, was a difficult project that required the correlation of topics covered during the duration of the course. There were numerous challenges throughout the design process that assisted in learning and enabled the creation of a functioning design. The project also provided an opportunity to analyze design process strengths and weaknesses and to learn from mistakes, while simultaneously increasing experience designing for real world mixed-signal applications. As an end result, a successfully functioning KD1S NS Modulator that favorably compares to all required specifications as outlined in the project parameters was designed and is presented for evaluation.

LTspice Simulation File Index

ADC_MONAHAN_CT_8D1S_1st_order_1MHz: 1st order 8-path 8D1S topology
ADC_MONAHAN_CT_8D1S_1st_order_1MHz_RAMP: 1st order 8-path slow ramp
ADC_MONAHAN_CT_8D1S_1st_order_1MHz.m: file used to interface LTSpice and MATLAB

ADC_MONAHAN_CT_8D1S_2nd_order_1MHz: 2nd order 8-path 8D1s topology
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ADC_MONAHAN_CT_8D1S_16path_1st_1MHz.m: file used to interface LTSpice and MATLAB

amp_test: AoI_{DC} of op amps v2 and v3
amp_tran: step response of amp v2 and v3

BiasGen_test: displays bias range of bias generation circuits for x8 and x16 ring oscillatos

clock_gen_x8_test: test file for 8-path ring oscillator
clock_gen_x8_capture: simulation results aligning capture windows of 8 K-paths

clock_gen_x16_test: test file for 16-path ring oscillator

clk_comparator_test: simulates comparator switching times and output swing

op_amp_AC_open_loop: op amp AC response, f_{un}

switch_x2_test: basic resistive divider to test TG switch resistance