NOVEMBER 29, 2017

COURSE PROJECT:
CMOS TRANSIMPEDANCE AMPLIFIER
ECG 720 ADVANCED ANALOG IC DESIGN

ERIC MONAHAN

1.Introduction: CMOS Transimpedance Amplifier

Avalanche photodiodes (APDs) are highly sensitive, high speed semiconductors that effectively convert light to electricity via the emission of free carriers when exposed to light. APD's have a wide range of applications including measuring distances, range finding, and as receivers in optical fiber communications where data is transmitted via pulses of light through an optical fiber. These applications include the need for transimpedance amplifiers to convert the current generated by the APD into a voltage. To this end, the course design project for ECG 720 Advanced Analog IC Design is to design an analog front end (AFE) that converts current from an APD into an output voltage using a transimpedance amplifier (TIA).

2. Project Design Specifications

The course project is to design and simulate an AFE using On's C5 process models and LTspice to meet the following minimum design criteria:

- Total gain: First Stage – 30kΩ (Transimpedance amplifier, TIA) and Second Stage 10–20x V/V
- TIA Bandwidth minimum of 250 MHz
- Input referred noise: < 5 pA/√Hz but preferrably 1.5 pA/√Hz
- 1.5 – 2 V output swing
- 3.3 or 5 V power supply operation with less than 5 mA current consumption
- Amplifier output signal is designed to drive high impedance loads (use 1 pF)
- Slew–rate with maximum load > 100V/microsecond = 100 mV/nanosecond

The gain range required for the two stages is defined by the following:

$$A_{total} = A_{TIA} * A_{VoltageAmp} = 30k * (10\ to\ 20) = 300k\ to\ 600k$$

To meet the minimum required output swing of 1.5V, the total amplifier design needs to satisfy the following relationship for the current range

$$I_{in,range} = \frac{1.5V}{300k} = 5\mu A$$

at a minimum. As gain increases, the range of currents decreases proportionally. This is summarized in Table 1 below:

Gain	$I_{in,range}$ (uA)
300k	5.00
350k	4.28
400k	3.75
450k	3.33
500k	3.00
550k	2.73
600k	2.50

Table 1

3. Design Process

3.1 TIA Topology

The topology selected for the TIA was a PMOS differential pair to simplify DC biasing and due to the large bandwidth the differential pair is able to achieve. A PMOS differential amplifier was selected since the range the output voltage needs to swing around was not set to a specific value. The initial goal was to center around 2.5V for a 5V power supply, so using either an NMOS or PMOS first stage was equally appropriate for a differential topology. The completed TIA is displayed below in Figure 1 and includes two biasing circuits acting as voltage dividers designed with small widths to keep DC biasing relatively constant with variations in VDD. The tail current is set to 888uA by Vbias1. This high current enabled the final amplifier to meet the design specifications after the second stage was added.
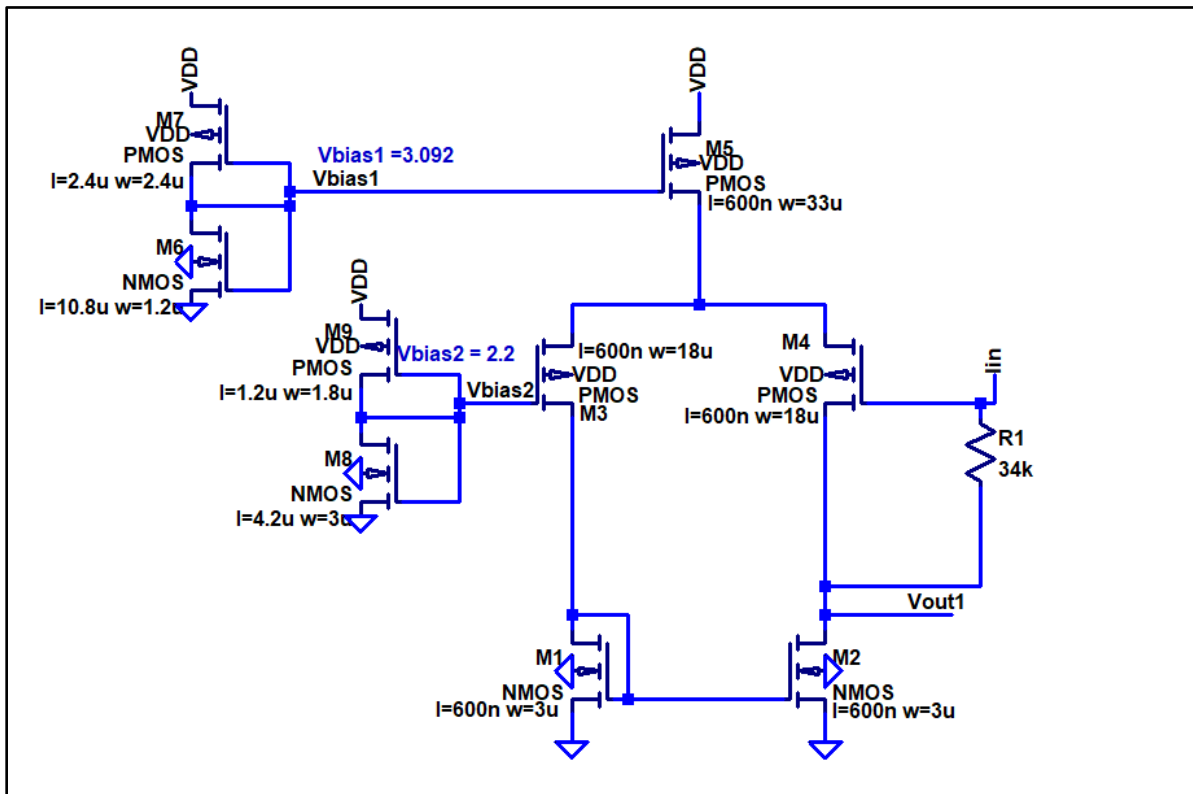

Figure 1 Transimpedance Amplifier Design

Simple characterization of the C5 model transconductance, g_m, and the output resistance, r_o, was performed for different sizes to provide approximate values as a starting point for designing with a short channel process. The simulations all use the C5 process minimum length of 600nm in an effort to design for high speed. Table 2 below only includes results for relevant sizes used in the final design. These results are included in the files *NMOS_smallsignal_gm, PMOS_smallsignal_gm, NMOS_smallsignal_ro,* and *PMOS_smallsignal_ro.*

NMOS	g_m (A/V)	r_o (Ω)
3u/600n	0.29µ	72.7k
24u/600n	2.79m	7.8k
36u/600n	4.23m	5.2k
72u/600n	8.54m	2.6k
PMOS	g_m (A/V)	r_o (Ω)
18u/600n	1.38m	7.6k
21u/600n	1.62m	6.5k
33u/600n	2.56m	4.1k

Table 2. NMOS and PMOS Transconductance and Output Resistance

3.2 TIA Simulation Results

The initial starting point included deriving the open loop gain, A_{ol}, and using this to derive the closed loop gain, A_{CL}. The open loop gain for the topology selected is the following:

$$A_{OL} = \frac{v_{out1}}{i_{in}} = g_{m4} * R_F(r_{op,4}||r_{on,2}||R_F)$$

Using operating point simulations located in the file *TIA_op* to determine the transconductance and output resistances for the selected device sizes led to the following:

$$A_{OL} = \frac{v_{out1}}{i_{in}} = 8.05x10^{-4} * 34k * (\frac{1}{44.3\mu}||\frac{1}{16.3\mu}) \approx 304k\Omega$$

```
Name:        m4         m2
Model:      pmos       nmos
Id:        4.41e-04   4.41e-04
Vgs:       1.33e-15   2.71e+00
Vds:       1.92e+00   2.24e+00
Vbs:       2.76e+00   0.00e+00
Vth:      -1.05e+00   7.08e-01
Vdsat:    -6.79e-01   8.01e-01
Gm:        8.05e-04   2.80e-04
Gds:       4.43e-05   1.63e-05
```

Figure 2 TIA operating point values for g_m and r_o

The open loop simulation, included in the file *TIA_AOL,* resulted in a simulated value of 287kΩ as seen below in Figure 3.
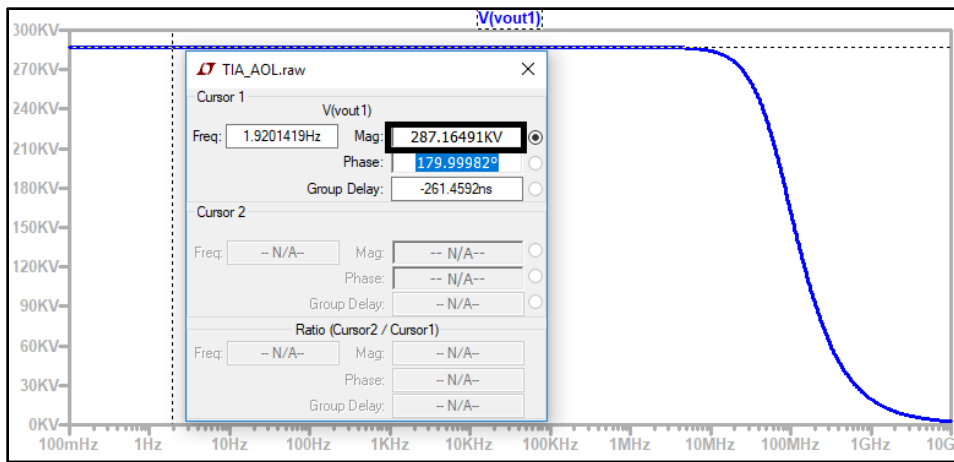
Figure 3 TIA open loop gain

Using the following relationship led to the derivation of the closed loop gain:

$$A_{CL} = \frac{A_{OL}}{1 + \beta A_{OL}} = \frac{304k}{1 + \frac{1}{34k} * 304k} \approx 30.5k\Omega, \qquad where \; \beta = \frac{1}{R_F} = \frac{1}{34k}$$

The TIA frequency response is displayed below in Figure 4 and is located in the file titled *TIA_ACanalysis*. The gain with no load is 89.6dB, or approximately 30.3kΩ, with a bandwidth of 730MHz. This closely approximates the hand calculations. The gain with a 30kΩ feedback resistor was slightly less than 30k due to the output resistances of the MOSFETs in parallel with the feedback resistor. Increasing the feedback resistor to 34kΩ resulted in a sufficient gain increase to meet the 30kΩ goal.
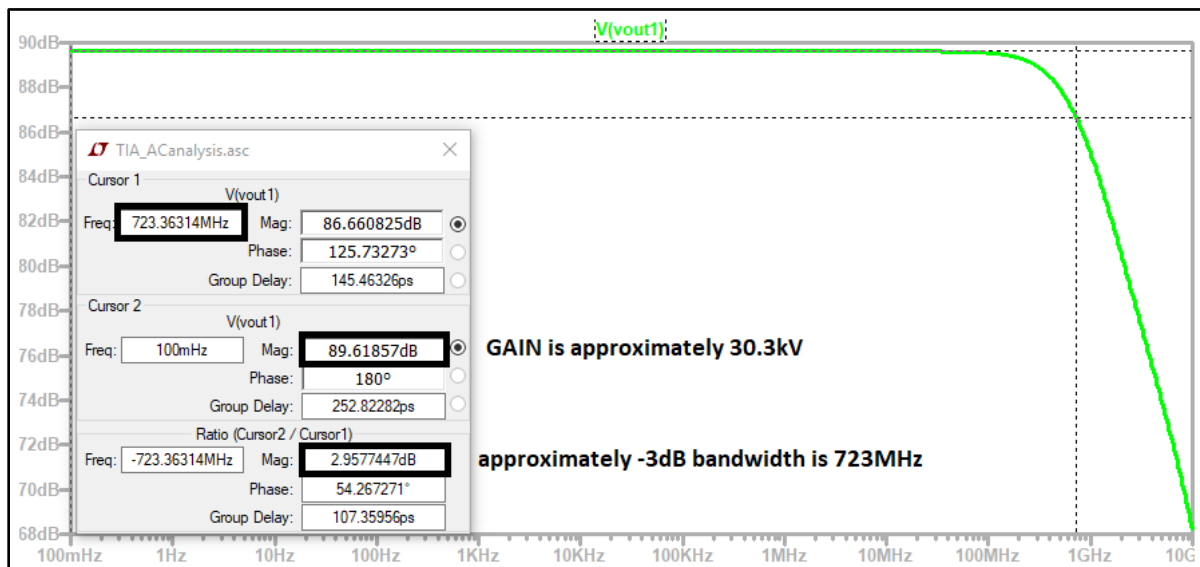

Figure 4 TIA Frequency Response

To meet the minimum output swing required for a 300k gain requires the TIA to have an output swing of 0.15V as defined by the expected minimum gain of 10V/V for the second stage amplifier. This figure is determined by the following:

$$V_{swing,TIA} = \frac{1.5}{10} = 0.15$$

The transient analysis results performed using the file *TIA_transient* are displayed below in Figure 5. The simulation results verify the TIA meets the minimum criteria for the first stage output swing using a 5uA input current with a resulting 0.151V output swing. Another point to note is the topology of the TIA is inverting, thus as the input current increases the output voltage decreases.
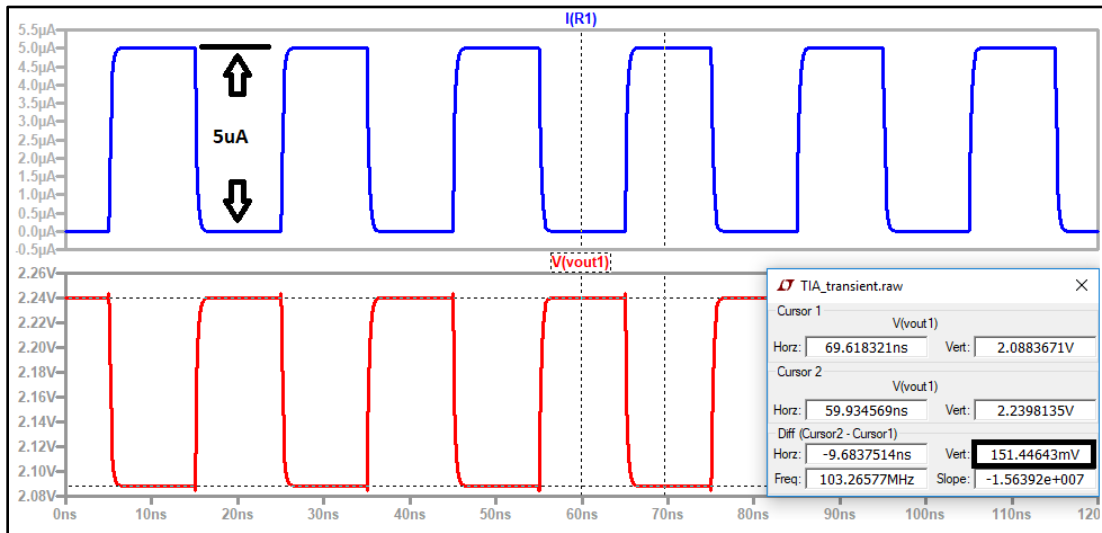

Figure 5 TIA transient analysis input current with output voltage

The TIA noise analysis provides a critical assessment of determining if the overall design will meet the minimum criteria for input referred noise less than 5pA/√Hz since the first stage noise will receive amplification of 30k. The area of interest in the noise simulation will be 250MHz since this represents the minimum bandwidth for the overall amplifier design. A capacitance was added on the input with values swept from 0fF to 500fF to determine the range of input capacitances the TIA is able to withstand before exceeding the minimum noise specification. The simulation results displayed below in Figure 6 are located in the file *TIA_noise*.
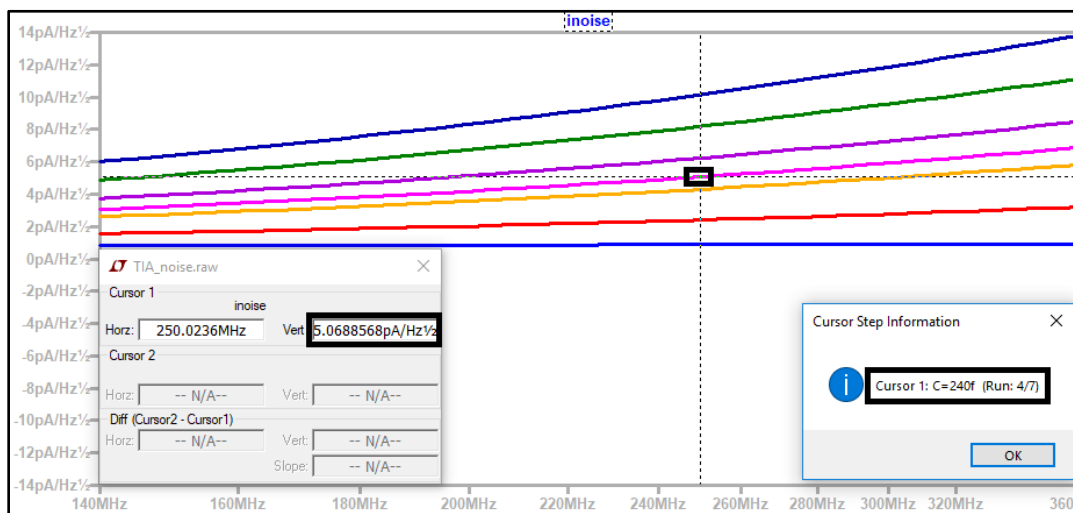

Figure 6 TIA input referred noise analysis modeling varying input capacitances

Table 3 summarizes the noise for varying input capacitances. Assuming the APD depletion capacitance is negligible leads to a best case input referred noise of 871fF/√Hz. Note, the TIA exceeds the maximum noise criteria for input capacitances above 240fF.

Input Capacitance(fF)	0	100	200	240	300	400	500
Input referred noise (pA/√Hz)	0.871	2.39	4.29	5.06	6.23	8.18	10.14

Table 3 Input referred noise for varying input capacitances

3.3 Voltage Amplifier Topology

The topology selected for the second stage amplifier was an NMOS differential amplifier with current source load. The initial selection for this stage was a DC-coupled series-shunt amplifier with a PMOS input and feedback resistors used to set the gain stage to 10V/V. This initial choice was made to take advantage of the extended bandwidth a feedback amplifier provides compared to a second stage differential amplifier. The decision to move to the differential amplifier came after initial attempts to properly bias the DC-coupled amplifier were unsuccessful.

The choice of the differential amplifier was made to simplify the biasing with the tradeoff being an overall reduction in bandwidth compared to the DC-coupled amplifier with feedback. Additionally, both PMOS and NMOS versions of this amplifier were designed with the NMOS diff pair resulting in better overall performance in both gain and bandwidth when compared to the PMOS diff pair. Specifically, the PMOS diff pair struggled to meet adequate bandwidth for even the lowest required gain. Also, the output swing of the first stage TIA is small enough to allow flexibility in the diff amp input voltage range for either topology.

The only drawback was the need for additional biasing for the NMOS tail current, but this was a simple decision due to the diff pair meeting all specifications. Lastly, an NMOS source follower was included as a buffer. The source follower gain is marginally less than one, so the amplifier requires a gain above 10V/V to meet the minimum criteria. The voltage amplifier design is displayed below in Figure 7.
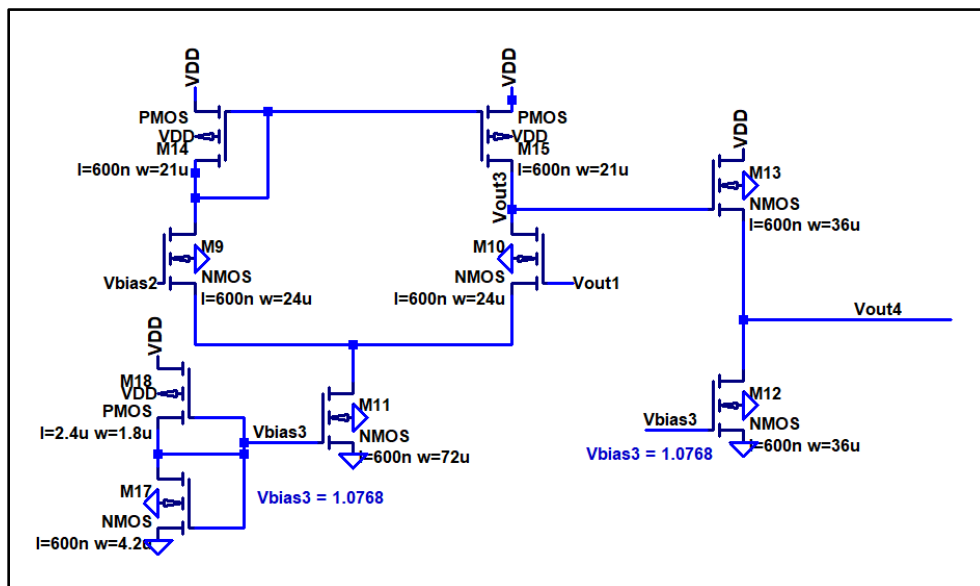

Figure 7 NMOS differential amplifier with source follower

3.4 Voltage Amplifier Simulations

The second stage voltage amplifier simulations demonstrate the NMOS differential amplifier meets the minimum design criteria. The gain was calculated, using output resistance and transconductance values from the file *Voltageamp_op*, as the following:

$$\frac{v_{out}}{v_{in}} = g_{mn,10} * r_{op,4}||r_{on,2} = 2.1x10^{-3} * \left(\frac{1}{54.5\mu}||\frac{1}{70.8\mu}\right) \approx 16.7V/V$$

```
Name:        m15          m10
Model:       pmos         nmos
Id:        -8.33e-04    8.33e-04
Vgs:       -2.02e+00    1.39e+00
Vds:       -2.72e+00    1.42e+00
Vbs:        0.00e+00   -8.54e-01
Vth:       -8.76e-01    7.60e-01
Vdsat:     -7.97e-01    4.06e-01
Gm:         1.12e-03    2.10e-03
Gds:        5.45e-05    7.08e-05
```

Figure 8 Voltage amplifier g_m and r_o

Next, the simulation for the frequency response of the amplifier, located in the file *VoltageAmp_AC,* is displayed below in Figure 9. The NMOS diff pair has a closed loop gain of approximately 16.5V/V, or 24.4dB, at Vout3 with a bandwidth of 322MHz. Adding the source follower reduced the gain to 14V/V at a bandwidth of 313MHz. The gain of the source follower is shown to be less than the ideal unity as predicted at 0.848V/V, or -1.43dB. A drawback to using the diff pair is the current consumption required to meet the bandwidth specification. The current consumption in this stage is 2.53mA, still within the 5mA consumption requirement, but a noticeable tradeoff to push the bandwidth out versus the potential savings in current for the same bandwidth using the feedback amplifier considered initially.
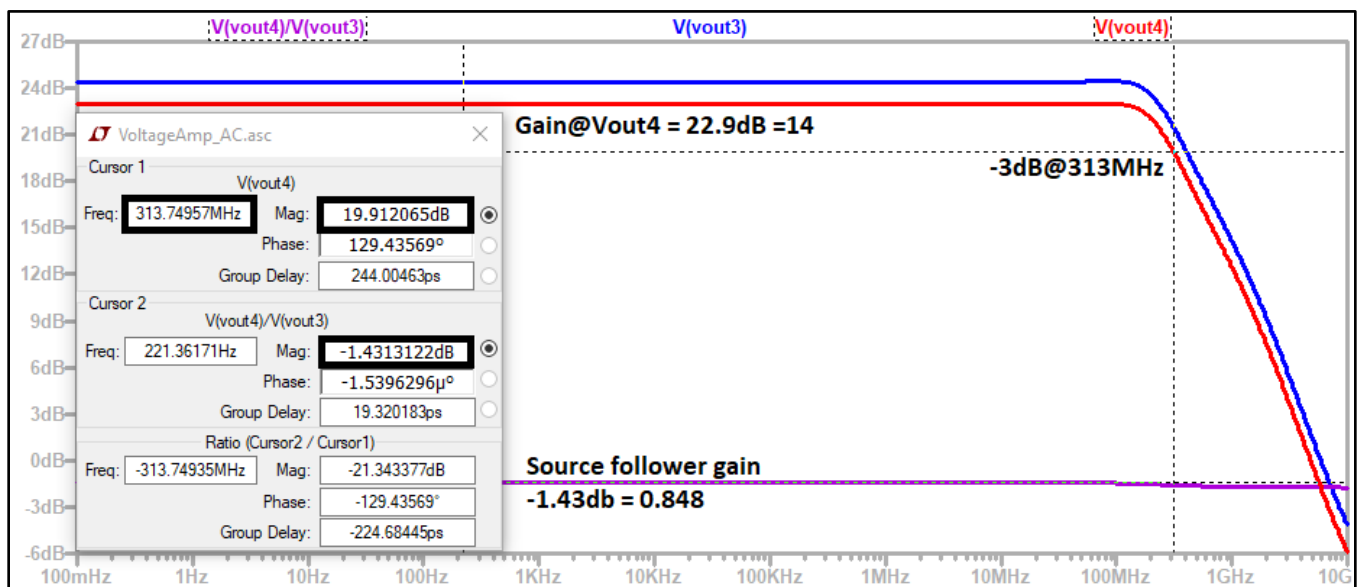

Figure 9 Second stage voltage amplifier AC response

Next, a transient simulation was performed using the file *VoltageAmp_transient* to determine large signal behavior. The TIA output was simulated swinging from 0V to -0.15V around a constant 2.239V that models the DC bias from the TIA output to the second stage amplifier input. The negative voltage swing is due to the inverting topology used for the TIA. The simulation results are displayed below in Figure 10 and clearly demonstrate the output swing exceeds the minimum 1.5V design specification at 1.67V.
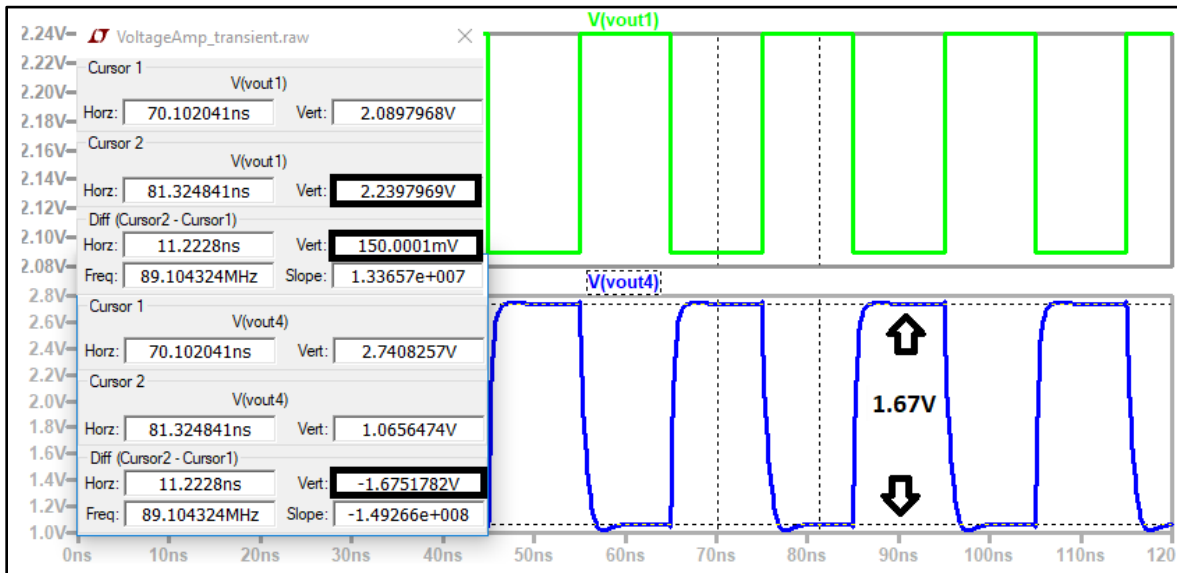

Figure 10 Voltage amplifier output swing

Moving on, the noise simulation located in the file *VoltageAmp_noise* results in an input referred noise of approximately 12nV/√Hz as displayed below in Figure11. The noise in the second stage is less critical than the first stage noise due to the large gain associated with the TIA. As a comparison, referencing the file *TIA_noise* shows the TIA output feeding into stage 2 has V(onoise) equal to 79nV/√Hz as a worst case for a 240fF input capacitance and 25nV/√Hz for no input capacitance.
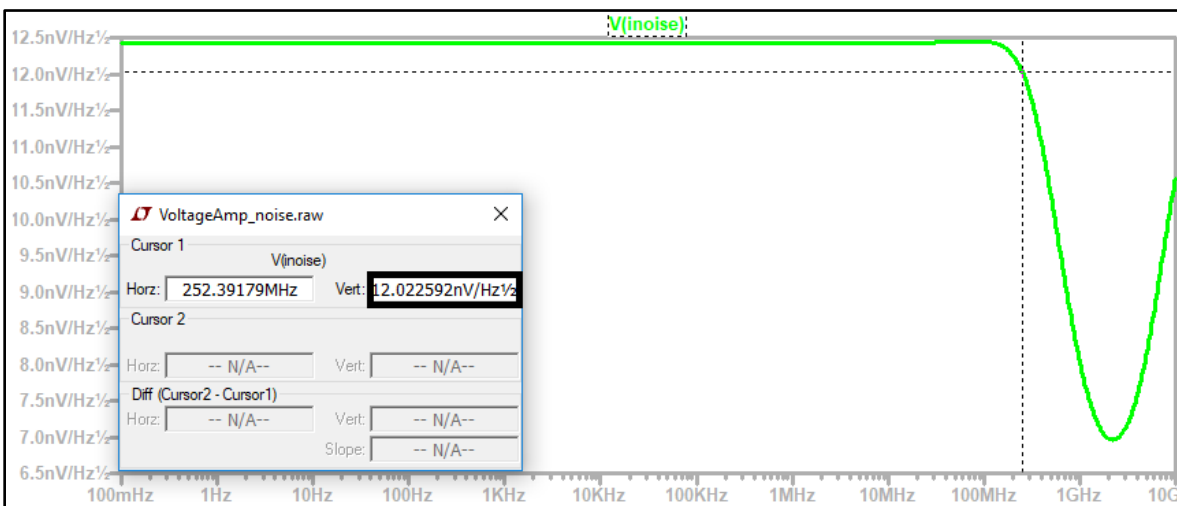

Figure 11 Voltage amplifier input referred noise

4. Final Amplifier Design

Putting the AFE together using the two stages previously discussed completed the design process. The final schematic for the two stage AFE is displayed below in Figure 12. The AFE as designed satisfies all design criteria with all results for the amplifier under max load of 1pF summarized at the end of the section.
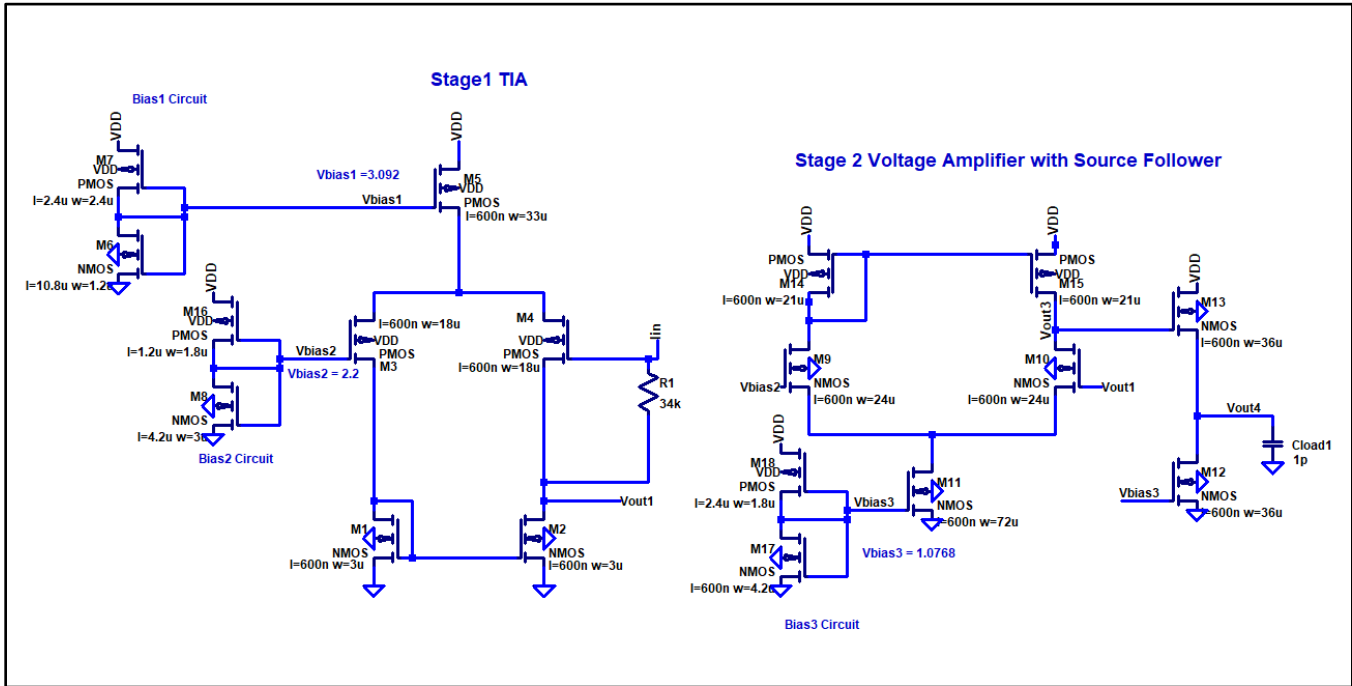

Figure 12 Final Analog front end schematic

To simulate for variations in VDD, the assumption was made that the power supply would vary by no more than $\pm2\%$. Thus, the value of VDD was stepped from 4.9V to 5.1V in 100mV increments with all simulation results below including a 1pF load to demonstrate the AFE meets or exceeds minimum design criteria. For simplicity, only the results for a 5V supply will be detailed in the next section with simulation results for power supply variations summarized at the end in Table 4.

4.1 Final Amplifier Simulation Results

The frequency response of the final amplifier design is located in the file *FinalAmplifier_AC* with simulation results displayed below in Figure 13. The results demonstrate the two stage amplifier exceeds the minimum criteria for both gain and bandwidth at 5VDD with values of 424kΩ and 289MHz, respectively. Note the rolloff is ideal with no peaking. The total current consumption for the design is approximately 3.4mA.
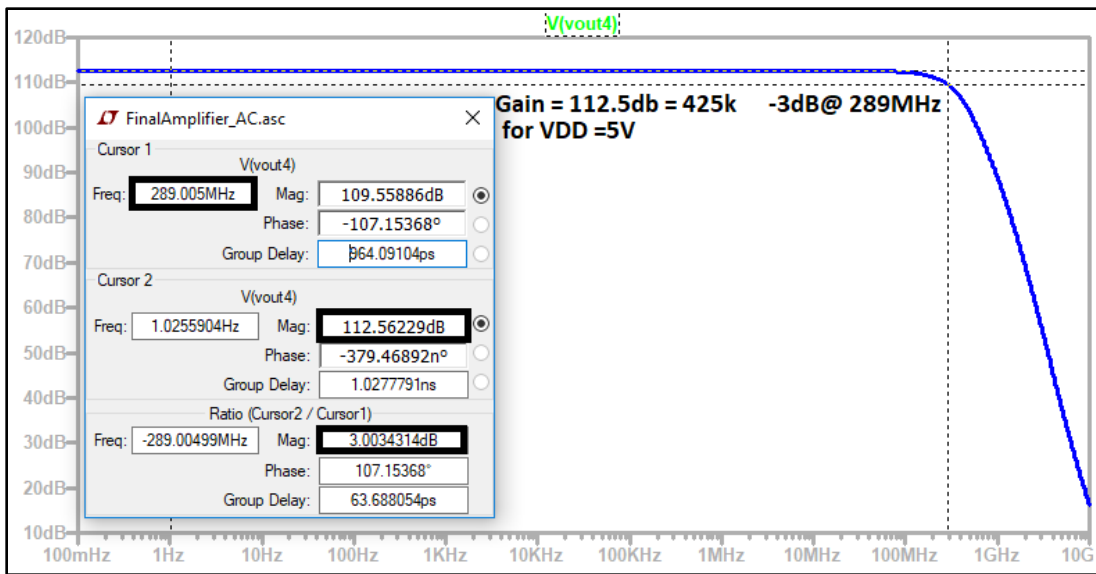
Figure 13 AC response for 5V power supply with 1pF load

Next, the output swing of the two stage amplifier was determined via a transient simulation located in the file *FinalAmplifier_transient.* Recall, an input current range of 5uA was determined to be capable of generating a 1.5V output swing for an amplifier with 300k gain as discussed earlier in Section 2. The simulation results are displayed below in Figure 14 and demonstrate the output swing meets the 1.5V-2V design criteria at a value of 1.68V. Also verified in Figure 14, the AFE meets the 100mV/ns slew-rate specification at 100mV/0.11ns for a falling edge and 100mV/0.056ns for a rising edge.
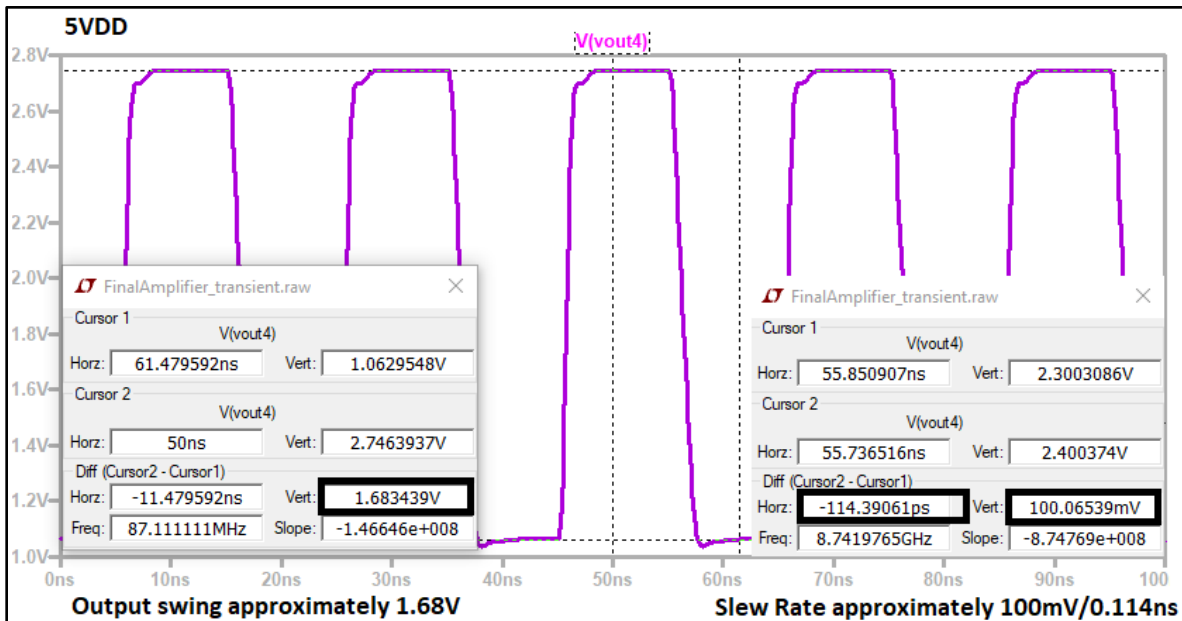

Figure 14 Final design transient response

Another specification of interest characterized with the transient simulation is the amplifier settling time, t_s. The settling time for this project is not defined to meet any specific criteria, so arbitrary values

of 2% and 5% have been selected to show the amplifier performance range. Figure 15 below shows results for a 5V supply and a 2% criteria. The settling time is 1.69ns for the rising edge and 2.99ns for the falling edge.
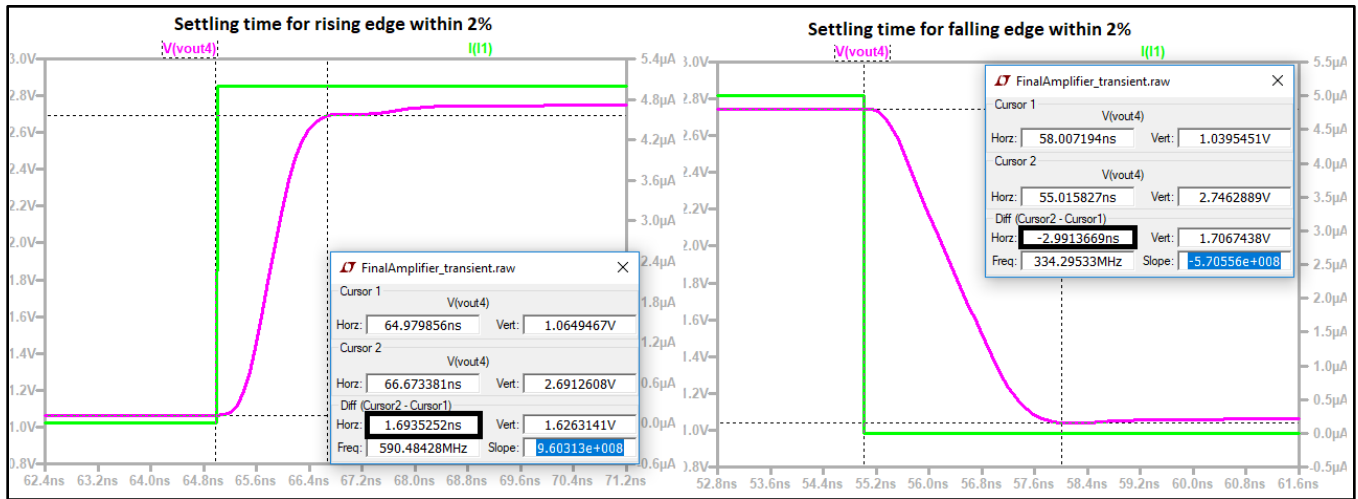

Figure 15 Settling time within 2%

The input referred noise was simulated with the design file titled *FinalAmplifier_noise.* Simulations once again included modeling input capacitances ranging from 0fF to 500fF to determine the maximum range the amplifier can operate and still meet the 5pA/$\sqrt{\text{Hz}}$ design criteria. The simulation results for 5VDD at the amplifier bandwidth, 290MHz, are displayed below in Figure 16. Note, for negligible input capacitance the amplifier has an input referred noise of 0.822pA/$\sqrt{\text{Hz}}$, below the design criteria. The model indicates the amplifier will exceed this specification once the input capacitance is greater than 240fF.
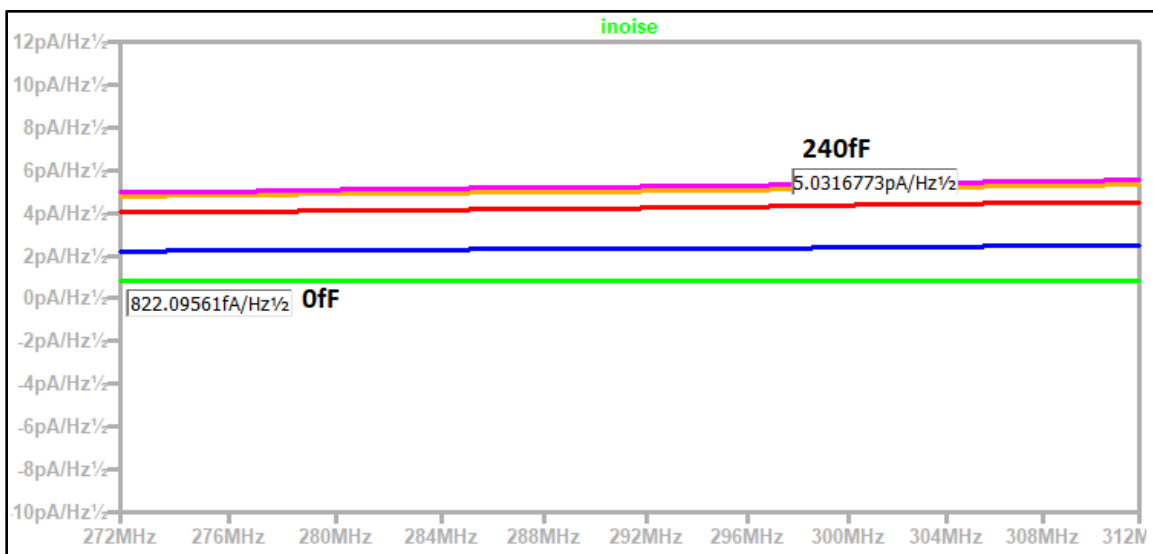

Figure 16 Final amplifier design input referred noise

Table 4 below summarizes the final amplifier design specifications for the maximum 1pF load and includes the results for the ±2% power supply variation discussed earlier. The next section will include details for the amplifier under varying load conditions.

VDD (V)	4.9	5.0	5.1
Gain (Ω)	434k	424k	413k
-3dB BW (Hz)	285M	289M	294M
Input -Referred Noise (pA/√Hz) 0fF input capacitance	0.824	0.821	0.820
Input-Referred Noise (pA/√Hz) 240fF input capacitance	5.07	5.01	4.95
Output Signal Swing (V)	1.64	1.68	1.72
Slew rate, rising (V/s)	100m/0.057n	100m/0.056n	100m/0.055n
Slew rate, falling (V/s)	100m/0.117n	100m/0.114n	100m/0.113m
Current Consumption (A)	3.28m	3.43m	3.58m
Power Consumption (W)	16.1m	17.2m	18.3m
Settling time rising, 2%	1.67ns	1.69ns	1.69ns
Settling time falling, 2%	3.24ns	2.99ns	3.13ns

Table 4 Final amplifier design simulation specifications

5. Final Amplifier Performance for Varying Loads

The performance of the amplifier met all design criteria for a maximum 1pF load. In this section, the amplifier will be tested under a variety of loads at a constant power supply of 5V. Table 5 presents a summary of the results for varying capacitive loads determined via the simulation files *FinalAmplifier_AC_sweepC* and *FinalAmplifier_transient_sweepC*.

Figure 17 below displays the frequency response and Figure 18 displays variations in the settling time. Note, the gains and output swings remain relatively constant for varying capacitive loads and were thus excluded from the results. Additionally, the maximum capacitive load the amplifier can drive and still meet the bandwidth specification is 1.45pF.

Capacitor (F)	0	250f	500f	750f	1p	1.45p
-3dB BW (Hz)	331M	342M	337M	315M	289M	250M
Slew rate, rising (V/s)	100m/.046n	100m/.044n	100m/.049n	100m/.050n	100m/.056n	100m/.058n
Slew rate,falling (V/s)	100m/.054n	100m/.056n	100m/.071n	100m/.092n	100m/.114n	100m/.163n
Settling time rising edge, 2% (s)	1.12n	1.17n	1.28n	1.43n	1.69n	2.35n
Settling time falling edge, 2% (s)	2.48n	2.53n	2.15n	2.16n	2.99n	3.48n

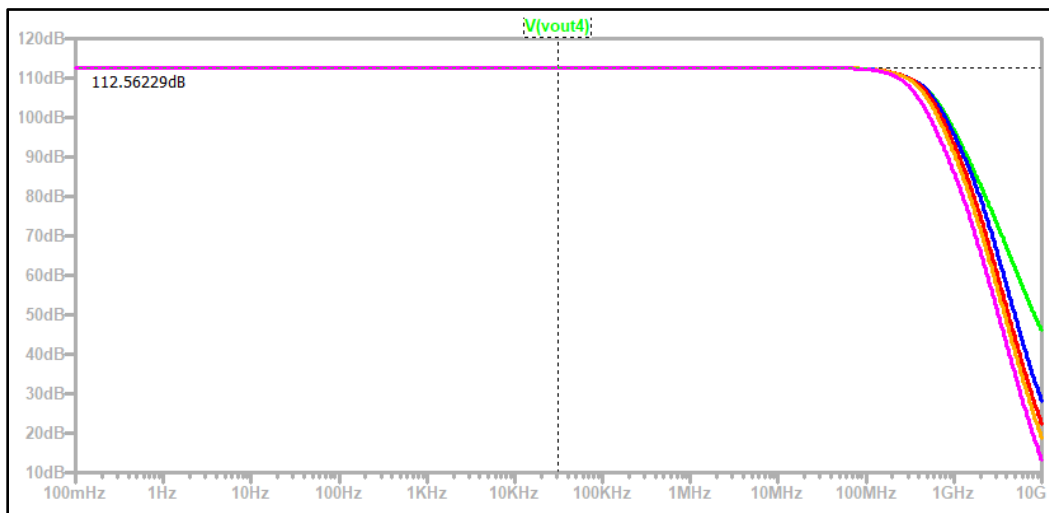Table 5 Final amplifier design performance for varying capacitive loads

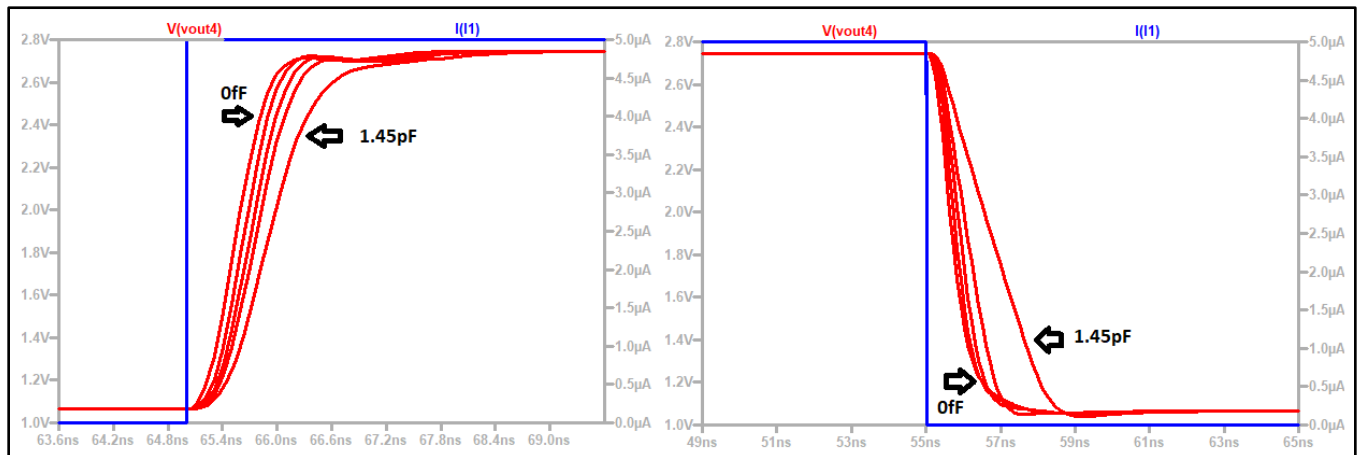Figure 17 Frequency response under varying capacitive loads

Figure 18 Settling time for varying capacitive loads

Next, simulations for a 1pF load with varying parallel resistive loads were performed using the files *FinalAmplifier_AC_RCload* and *FinalAmplifier_transient_RCload*. The gain clearly decreases as the load decreases with the most significant drop from 10kΩ to 1kΩ. As expected, the bandwidth shows an increase at the same time. Note, the output swing meets specifications for loads down to 2kΩ. The results are summarized below in Table 6. Figure 19 below displays sample slew-rate measurements for a 1kΩ resistor.

Resistor (Ω)	1k	2k	10k	50k	100k
Gain (Ω)	337k	373k	412k	422k	423k
-3dB BW (Hz)	295M	295M	290M	290M	290M
Output Swing (V)	1.34	1.48	1.63	1.67	1.68
Slew rate, rising (V/s)	100m/.082n	100m/.057n	100m/.057n	100m/.056n	100m/.056n
Slew rate,falling (V/s)	100m/.087n	100m/.081n	100m/.097n	100m/.112n	100m/.115n
Settling time rising edge, 2% (s)	1.42n	1.46n	1.60n	1.64n	1.65n
Settling time falling edge, 2% (s)	2.63n	2.39n	2.37n	2.53n	2.57n

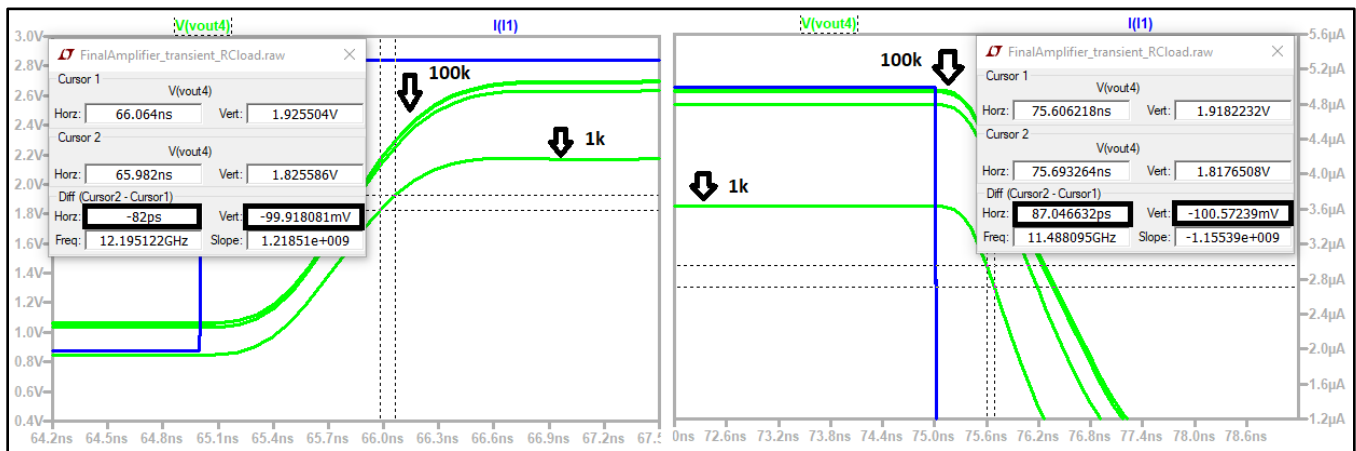Table 6 Final amplifier design performance for varying RC loads

Figure 19 Slew-rate measurements for rising and falling edges

6. Study of the Need for a Second Stage

The design project consists of a two-stage amplifier designed to convert a current input into a voltage output and meet the design specifications outlined in Section 2. However, a single-stage amplifier was also designed to meet the same specifications as the two-stage design required for the project. The design uses the same differential amplifier topology as the first stage TIA with a larger feedback resistor, as well as an NMOS source follower to buffer the load. The device sizes were changed to account for the differences in gain and bandwidth required from using a single stage. The topology is displayed below in Figure 20. Note, a 360k feedback resistor is used and there was a small margin relative to diff amp device sizing wherein the gain-bandwidth tradeoff allowed the amplifier to barely meet both specifications. Figure 22 shows the frequency response of the single-stage AFE.
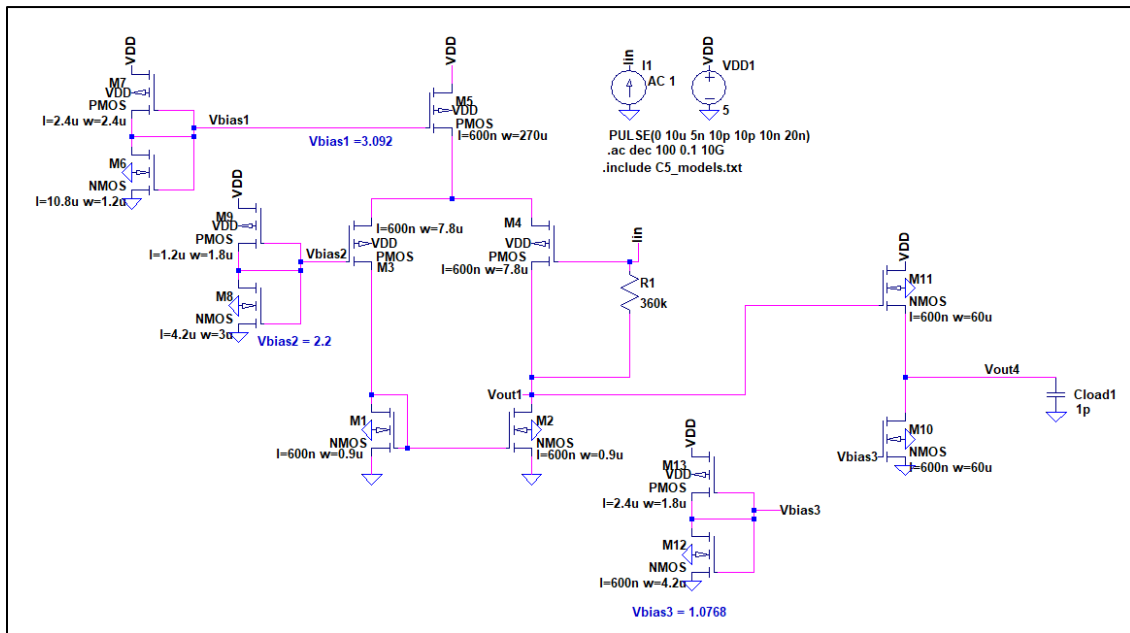

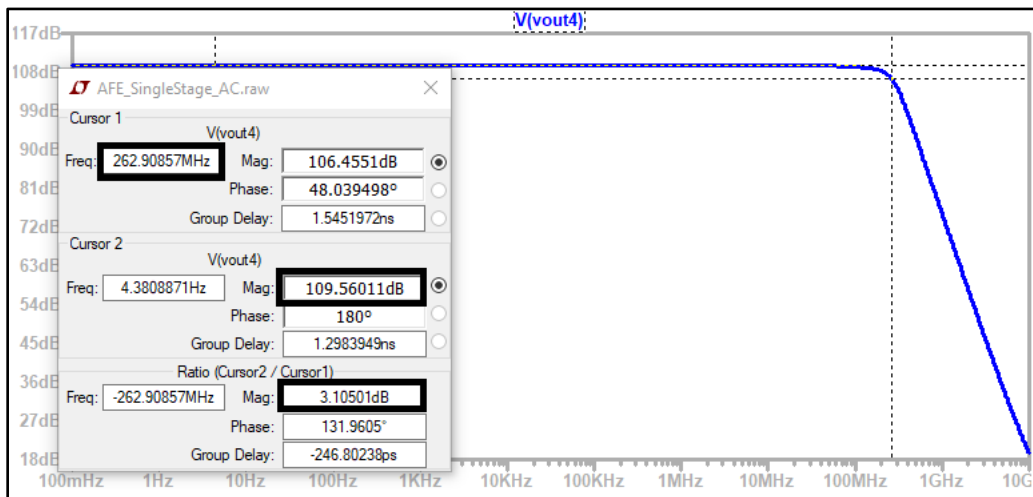
Figure 20 Single stage AFE with source follower

Figure 21 Single-stage AFE frequency response

Table 7 below shows a comparison of the single stage design versus the two-stage design. The design files for AC, transient, and noise simulations are all titled '*AFE_SingleStage_...*'. There are notable tradeoffs for using the single stage, including reduced gain, bandwidth, and speed. However, there is an almost 50% reduction in power due to lower current consumption.

	Single Stage	Two Stage
VDD (V)	5.0	5.0
Gain (Ω)	300.6k	424k
-3dB BW (Hz)	261M	289M
Input -Referred Noise (pA/√Hz) no input capacitance	0.268	0.821
Input-Referred Noise (pA/√Hz) 240fF input capacitance	3.47	5.01
Output Signal Swing (V)	1.53	1.68
Slew rate, rising (V/s)	100m/0.113n	100m/0.056n
Slew rate, falling (V/s)	100m/0.112n	100m/0.114n
Current Consumption (A)	1.88m	3.43m
Power Consumption (W)	9.43m	17.2m
Settling time rising, 2%	3.54ns	1.69n
Settling time falling, 2%	3.74ns	2.99n

Table 7 Single-stage AFE versus two-stage AFE

The single stage AFE is a more efficient design that would require less layout in the form of transistors, but requires a larger resistor than the two-stage AFE. The second stage amplifier does not appear to be necessary to meet the design criteria. However, the simulations for the single-stage AFE were not as comprehensive as for the two-stage AFE and this assessment is based solely on meeting the minimum design criteria.

7. APD Resistor Impact

The APD providing the input current will be reverse biased with the anode connected to ground via a resistor. Since the topology used for the AFE is a differential amplifier, the APD's current can be DC connected to the front-end's input. This is due to the diff amp self-adjusting such that Vout of the TIA will always try to match the constant DC bias on the opposite terminal. For the same reason, the resistor should also have no real impact on biasing unless it is small enough to be comparable to the approximate input resistance of 34kΩ such that it begins to lower the amplifier gain. At this point, the biasing is definitely altered and amplifier performance is reduced.

For this reason, the resistor to ground needs to be large enough such that the TIA gain is not impacted. First, simulations using the file *FinalAmplifier_AC_APD* tested resistor values to determine the

range of values that allow suitable gain and bandwidth. Additionally, capacitor values of 0fF and 240fF were simulated to model the amplifiers range for input capacitances, as previously discussed. Figure 22 below shows the amplifier gain drops below 300k for resistances less than 2.7MΩ with no input capacitance included. If we include the worst case of 240fF, the same resistor value holds for the gain, but the bandwidth is reduced below 250MHz to 147MHz. The maximum allowable input capacitance for a 2.7MΩ resistor to meet bandwidth is 140fF.
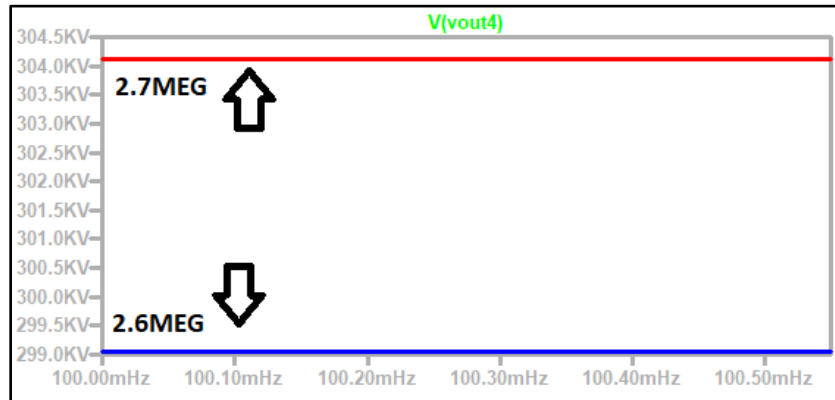

Figure 22 APD resistor-to-ground impact on gain

To determine the impact of the resistor on the SNR, the input referred noise simulations were repeated using the file *FinalAmplifier_APD_noise* with the input capacitances at 0fF and 140fF and a resistor to ground from the theoretical APD as seen below in Figure 23. As expected, due to the input-referred noise modeled by 4kT/R, as the resistance increases, the change in noise is negligible. However, as resistor size decreases, the SNR deteriorates. For this design, the minimum resistor value is approximately 2.7MΩ, as seen in Figure 24. The noise simulation results are summarized below in Table 8. Note, the 60kΩ and 80kΩ resistors were included simply to illustrate the point where the SNR violates the noise specification for the 0fF and 140fF input capacitances, respectively. These low resistor values are not realistic due to the reduction in gain and bandwidth previously discussed.
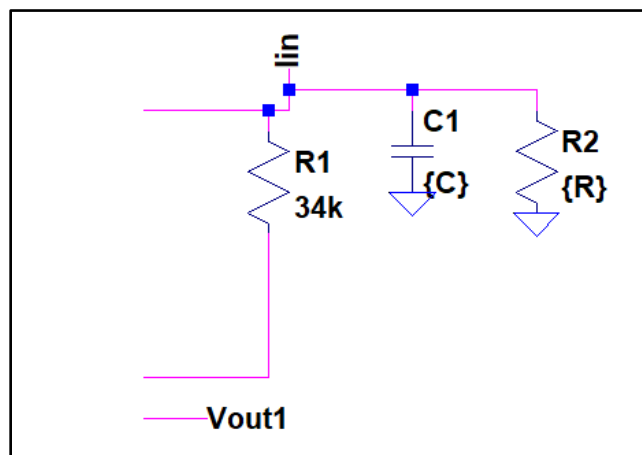

Figure 23 Adding resistance to ground to model APD connection

Input-Referred Noise (pA/√Hz) at Amplifier Bandwidth 290MHz

Resistor (Ω)	60k	80k	2.5MEG	2.7MEG	3MEG	5MEG	10MEG
Capacitor (F)							
0f	6.05	3.42	0.827	0.827	0.826	0.824	0.823
140fF	12.3	5.22	3.06	3.08	3.06	3.08	3.08

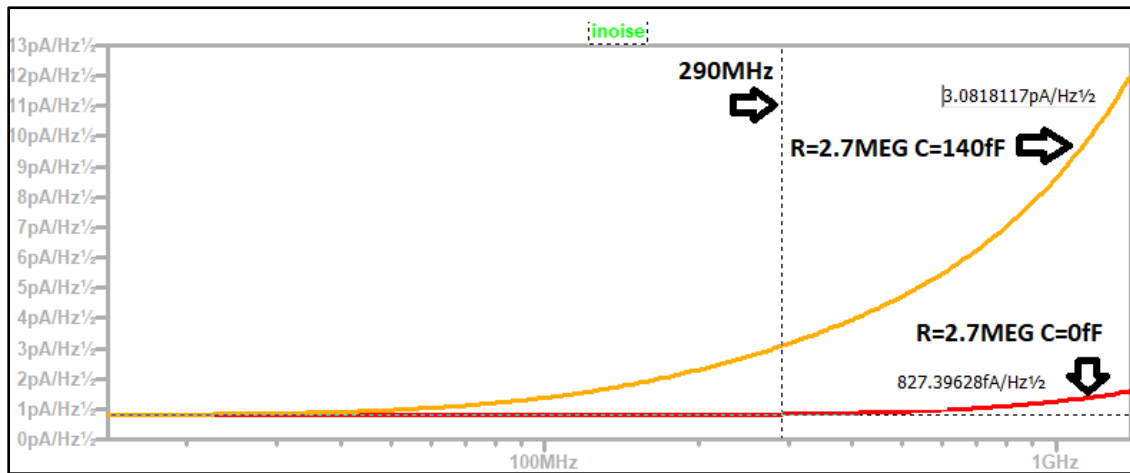Table 8 Input-referred noise for varying APD anode-to-ground resistances

Figure 24 Input-referred noise for 2.7MΩ APD resistor-to-ground

7. Conclusion

The ECG720 course design project, designing a high speed, low noise AFE, was initially a seemingly difficult project that required the correlation of topics covered during the duration of the course. There were numerous challenges throughout the design process that assisted in learning and enabled the creation of a functioning design. The project also provided an opportunity to analyze design process strengths and weaknesses and to learn from mistakes, while simultaneously increasing experience designing for real world applications. As an end result, a successfully functioning AFE that meets all required specifications as outlined in the project parameters was designed and is presented for evaluation.

LTspice Simulation File Index

1) NMOS_smallsignal_gm and PMOS_smallsignal_gm -small signal transconductance models

2) NMOS_smallsignal_ro and PMOS_smallsignal_ro - small signal output resistance models

3) TIA_op - operating point simulation for the TIA

4) TIA_AOL - open loop gain simulation for the TIA

5) TIA_ACanalysis - frequency response of TIA with no load

6) TIA_transient -output swing of first stage TIA for 5uA input current pulse

7) TIA_noise - input referred noise of TIA with varying input capacitances at 250MHz

8) Voltageamp_op - operating point simulation of second stage amplifier

9) Voltageamp_AC -no load frequency response of stage 2 with source follower

10) Voltageamp_transient -large signal specification of stage 2 amplifier

11) Voltageamp_noise - input referred noise of voltage amplifier with source follower, no load

12) FinalAmplifier_op - not referenced in report, shows operating point results for final design

13) FinalAmplifier_AC - frequency response of final 2 stage amplifier design with 1pF load

14) FinalAmplifier_transient - output swing of final 2 stage amplifier design

15) FinalAmplifier_noise - input-referred noise of final 2 stage amplifier design

16) FinalAmplifier_AC_sweepC- amplifier AC response under varying capacitive loads

17) FinalAmplifier_transient_sweepC - final transient response under varying capacitive loads

18) FinalAmplifier_AC_RCload- AC response varying parallel RC loads, C = constant 1pF

19) FinalAmplifier_transient_RCload - transient response varying parallel RC loads, C = constant 1pF

20) AFE_SingleStage_AC -single stage AFE frequency response

21) AFE_SingleStage_noise -single stage AFE input referred noise

22) AFE_SingleStage_transient-single stage AFE transient response

23) FinalAmplifier_AC_APD - sweep resistor values on input to model APD resistor to ground

24) FinalAmplifier_APD_noise - input referred noise range for APD resistor to ground

25) biasing_ckts - 3 biasing voltages