



NOVEMBER 28, 2016

COURSE PROJECT:  
CMOS SWITCHING POWER SUPPLY

EE 421 DIGITAL ELECTRONICS

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## 1. Introduction: CMOS Switching Power Supply

The course design project for EE 421 Digital Engineering requires the design of a CMOS switching power supply, a synchronous Buck converter. A traditional linear regulator operates by continuously adjusting a voltage divider network to produce a constant output voltage, however the circuit dissipates the difference between input and output voltage in the form of heat. The main advantage to a CMOS switching power supply versus a traditional linear regulator is the generation of a square waveform that minimizes power dissipation and then filters the waveform to generate a constant output voltage.

A brief synopsis of the synchronous Buck converter design is presented to clarify the basic operation of the circuit with specific details outlined in the report. The power supply design will consist of a bandgap which generates the reference voltage, a comparator, a set-reset (SR) latch based non-overlapping clock generation circuit, and a series of buffers. The bandgap voltage reference is used to provide a temperature independent voltage reference for the comparator. The comparator uses a feedback loop for comparison with the bandgap reference and adjusts the output voltage up or down when the circuit output voltage varies. This output is fed through a buffer to square up the signal such that the output provides satisfactory logic levels between 0V and VDD. The buffer output feeds into an SR-latch to provide a non-overlapping clock generation circuit. This circuit prevents the switches from being on at the same time, thus the amount of crossover current resulting from these periods is minimized. The output is then fed into a series of buffers designed to minimize the delay created by the capacitive loads between smaller and larger inverters. The resulting stages provide a resistance to step down VDD and pass it through a low pass filter for a constant DC output voltage. All simulation files are referenced in text and indexed at the conclusion of this report.

## 2. Project Design Specifications

The course project is to design a CMOS switching power supply, a synchronous Buck converter, that is powered with a VDD that can vary from 4 to 5.5 V. The power supply uses an off-chip inductor and capacitor to generate a constant output voltage of 2.5 V, which we'll call  $V_{out}$  below, for load currents ranging from 0 to 100 mA.

### Project Requirements:

- Part 1: In [bandgap.zip](#) is a bandgap voltage reference schematic designed for the C5 process. A bandgap is a common circuit used for generating a voltage reference of approximately 1.25 V that doesn't change [much] with temperature and VDD variations. The first part of this project is to lay out this bandgap.
- Part 2: Design a circuit that senses an input voltage  $V_{in}$  (this input is connected to the output voltage of the power supply,  $V_{out}$ , for feedback and control). Your design should use the bandgap from part 1.
  - The output (called Enable) of the circuit is a logic 1 (vdd) when  $V_{in}$  is greater than 2.5 V and a logic 0 (ground) when  $V_{in}$  is less than 2.5 V.
  - The circuit's input,  $V_{in}$ , should draw no more than 50  $\mu$ A of current and no less than 10  $\mu$ A of current.
  - A practical design concern pops-up when  $V_{in}$  is near 2.5 V, which it will be in these projects. What will happen, if the circuit isn't designed correctly, is that the signal Enable will oscillate since  $V_{in}$  is moving slightly above and below 2.5 V. To avoid these oscillations, design your circuit with a small amount of hysteresis.

- Your report, among other things, should show DC sweeps (Vin v. Enable), with varying temperature/VDD, of the performance of your design. Your design considerations (trade-offs), as mentioned above, should also be detailed.
- Part 3: Use the design from part 2, using Enable, to drive buffers (inverters) that enable/disable a PMOS switch connected between VDD and cell's output, out, and an NMOS switch connected between the cell's output, out, and ground. Your report, among other items, should discuss your thoughts on device sizing. Ensure the buffer you design has a lock-out feature to ensure that the PMOS and NMOS are never on at the same time to avoid cross-over current
- Part 4: The CMOS synchronous Buck switching power supply will be connected in 4 places: **VDD**, **gnd**, **out**, and **Vout**. What you LVS and DRC will be this cell; however, you will need to simulate this cell (generate a symbol view of your final design having 4 pins, or 2 pins if using global vdd! and gnd!) with the off-chip inductor and capacitor (the inductor and capacitor are not part of what we send out for fabrication).
  - The output of your design, **out**, is connected to the inductor.
  - The other side of the inductor is connected to **Vout** (the inductor is connected between out and Vout).
  - The capacitor is connected from **Vout** to ground. Your report should detail your selection of the inductor and capacitor along with simulation results showing performance with varying temperature and power supply (plot your design's efficiency vs load current with different temperatures and power supply voltages). Of course, again, you need to also provide the details indicated above.

### 3. Design Process

#### 3.1 Bandgap Voltage Reference

The first part of the project required the layout of a bandgap voltage reference circuit. The goal of the bandgap is to use proportional to absolute temperature (PTAT) and complementary to absolute temperature (CTAT) references to create a voltage reference that is ideally independent of changes in power supply voltage (VDD), temperature and process variations. The CTAT reference is a diode-referenced, self-biased circuit that has a negative current temperature coefficient. The current in this circuit decreases as the temperature increases. The PTAT reference is a thermal voltage referenced, self-biased circuit that results in current that is proportional to temperature. The CTAT and PTAT references are combined in the circuit displayed in Figure 1 below to create the Bandgap voltage reference.

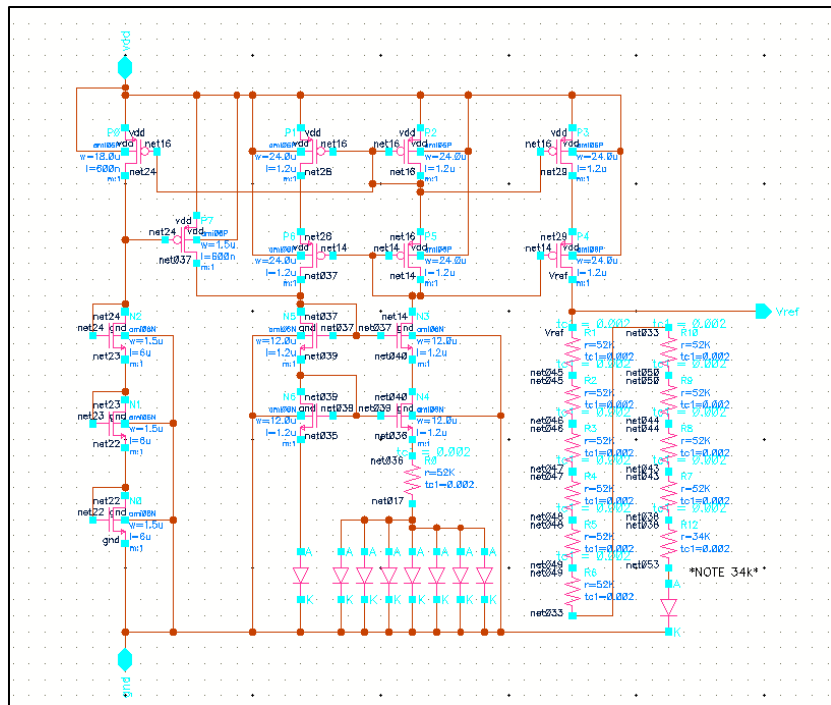


Fig. 1 Bandgap Voltage Reference Circuit

A parametric simulation for the above circuit for the relevant boundary values of temperature and VDD resulted in the output displayed below in Figure 2. Notice the voltage reference varies from 1.243V to 1.254V depending upon the temperature and VDD, but still provides a relatively constant reference voltage. The simulation files are titled *sim\_temp\_bandgap2* and for the parametric analysis *sim\_temp\_bg\_2.il*.

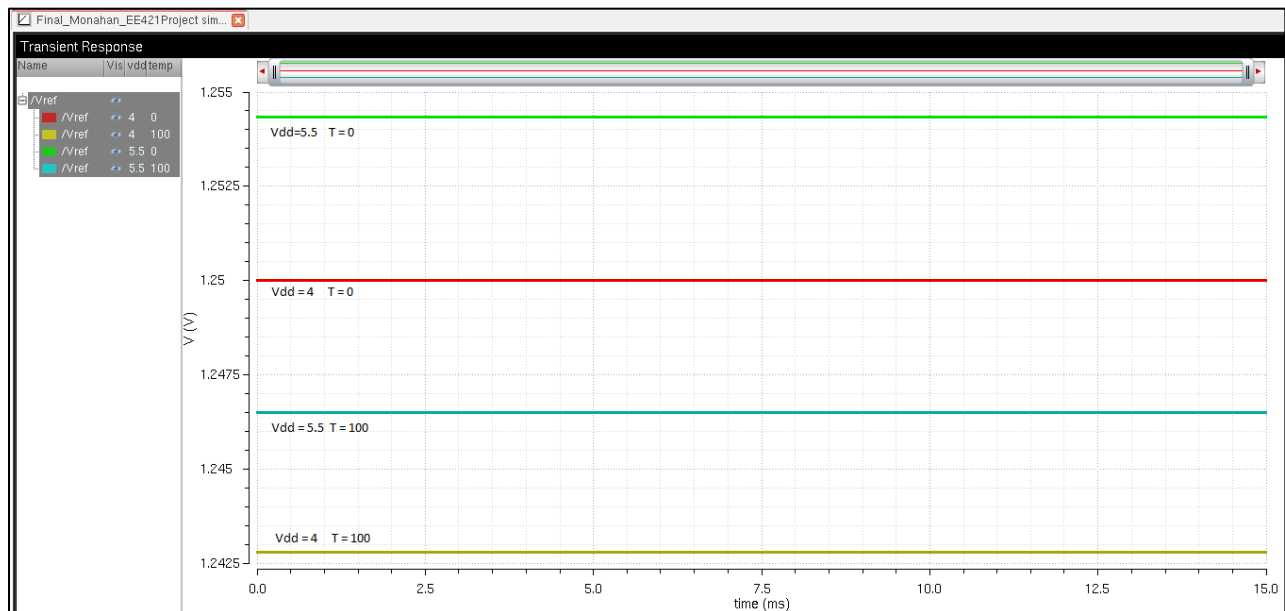


Fig. 2

As seen in Figure 3 below,  $V_{REF}$  begins a relatively linear droppoff at approximately  $3.7V_{DD}$ , noted 1 on the  $V_{REF}$  plot below, although at this voltage the total drop is less than 1% of the output at 6V of approximately 1.255V. At  $V_{DD} \approx 3.34V_{DD}$  and  $V_{DD} \approx 3.0V_{DD}$ , noted 2 and 3 respectively, on the  $V_{REF}$  plot,  $V_{REF}$  has seen drops of 5% to 1.192V and 10% to 1.125V, respectively. However,  $V_{REF}$  remains relatively constant for the range necessary for this design. Also, notice on the lower plot how the current drawn by the circuit increases with increasing VDD.

There is a linear draw from 2.1uA to 2.87uA as VDD increases from 3VDD to approximately 3.65VDD before the current flattens out around 2.9uA between 3.65VDD and approximately 4.25VDD. At this point, the current begins climbing somewhat linearly again. This illustrates our current draw will climb with increasing VDD. The simulation file is titled *sim\_bandgap*.

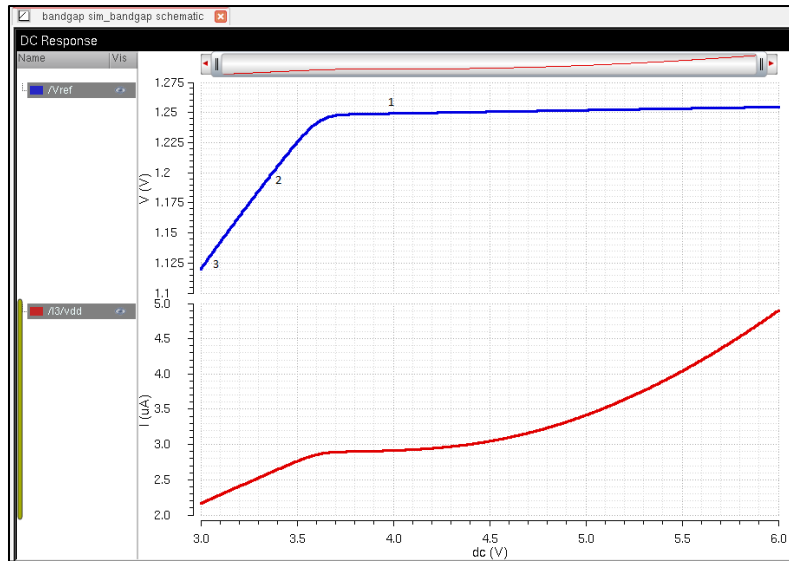


Fig. 3

Additionally, as expected, the current through the branches remains relatively constant due to the cascade structure. The plot in Figure 4 below shows the current through the left and right legs of the CTAT cascade structure remains constant for VDD ranging from 4VDD to 5.5VDD.

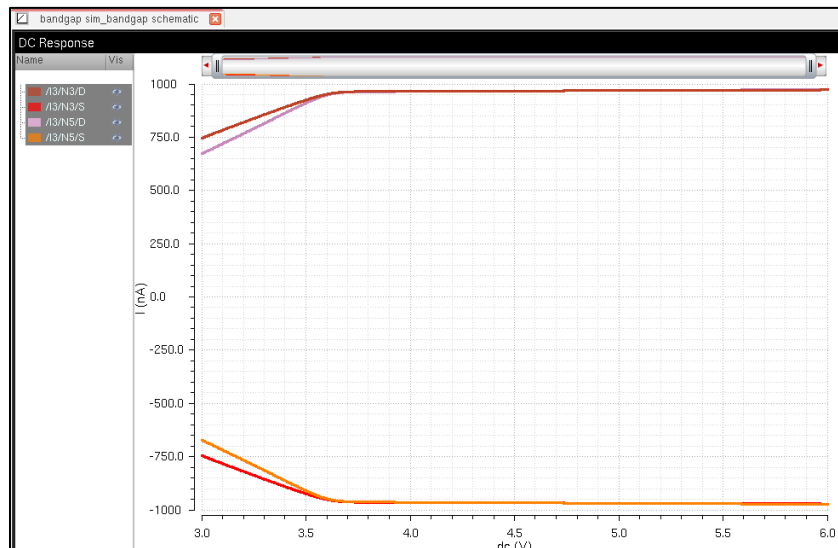


Fig. 4

$V_{REF}$  was also plotted against increasing temperature resulting in the plot displayed in Figure 5 below. As designed,  $V_{REF}$  experiences marginal changes in magnitude as temperature increases over a broad range of 100°C with a high of 1.253V at 0°C and 1.254V at 100°C. This is a variation of approximately 0.64%. At the lower end, from 0°C to 25°C there is a drop of approximately -40uV/C°. From 25°C to 75°C, the drop is approximately -80uV/C°. Lastly, from 75°C to 100°C the drop is approximately -100uV/C°. This averages out to approximately -80uV/C°. The

results indicate the temperature variations do cause the moderate variations in the bandgap voltage reference. The file used for this simulation is titled *sim\_temp\_bandgap*.

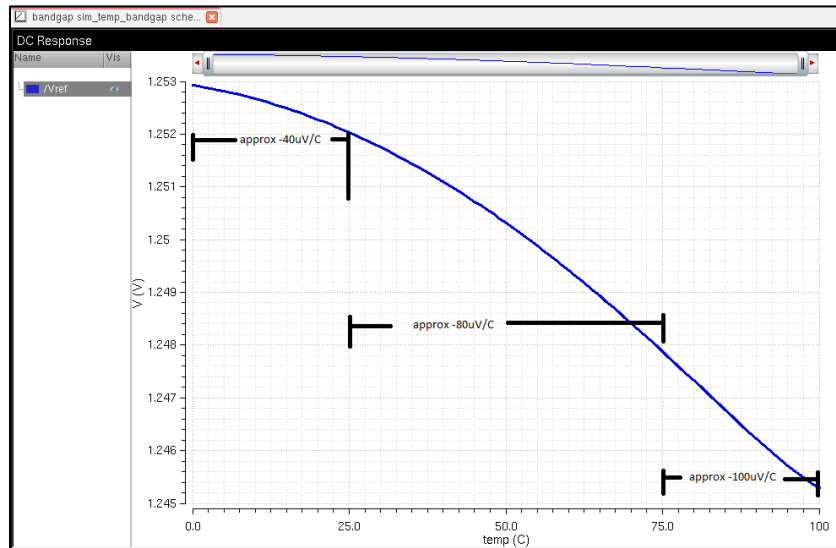


Fig. 5

### 3.2 MOSFET Device Sizing

The MOSFET sizing began with the sizing of the effective resistances of the PMOS/NMOS in the final buffer stage. The design strategy was to have a low enough resistance that at full load the voltage drop across the devices still provided enough voltage at the output of the circuit that there would be sufficient voltage across the inductor to allow for a steady 2.5V DC current. To this end, the following equations were used to start the process:

$$R_N = R'_N \frac{L}{W} \quad R_P = R'_P \frac{L}{W}$$

where  $R'_N = 15k\Omega$  and  $R'_P = 30k\Omega$ . However, this process also included the design of the entire buffer stage after the non-overlapping clock generation circuit. This stage was designed to minimize the delay between inverter stages by using a multiplier between each stage rather than a large jump from a small inverter to a much larger inverter with large capacitances. To make this design work, the desired output resistance was found by considering the current load and estimating the desired range of voltage required across the inductor. Once this was determined, the necessary resistance to induce this voltage drop was determined. An initial multiplier of eight was selected for the multiplier used for the buffer stage. Using this multiplier enabled the NMOS and PMOS resistances to approximate the value necessary to provide a current through the inductor that will allow for maximum efficiency. The initial resistance values were determined as follows:

$$R_N = 15k\Omega * \frac{0.6}{6 * 512} \approx 3\Omega \approx R_P = 30k\Omega * \frac{0.6}{12 * 512}$$

This value proved unsuccessful in later design simulations, discussed later, and was ultimately replaced with a value of approximately 12Ω. The 12Ω value is used for the inductor calculations in the next section.

### 3.3 Inductor and Capacitor Selection

The circuit implements an off-chip LC low pass filter to filter out AC signals and output a stepped down DC voltage. To minimize the band ripple, an inductor was selected to allow a current variation of  $\pm 10\%$  with an ideal frequency of 10MHz at the minimum current load and 100kHz at maximum current load. Assuming measured values at steady state, the design equations used to calculate the inductor value are as follows:

$$\text{Current vs. Time when PMOS is on} \quad \frac{I_{max} - I_{min}}{D * T} = \frac{V_{DD} - V_{out}}{L}$$

$$\text{Current vs. Time when NMOS is on} \quad \frac{I_{max} - I_{min}}{(1 - D) * T} = \frac{0 - V_{out}}{L}$$

where D is the duty cycle of the circuit and the relationship

$$V_{out} = D * V_{DD}$$

is used to solve for the above. The duty cycle for this design will be 50% with the goal of designing for a low frequency of approximately 100kHz and a high frequency of approximately 1MHz. The periods, T, for the low and high frequency range are as follows:

$$T_{low} = \frac{1}{100kHz} = 10\mu s \quad T_{high} = \frac{1}{10MHz} = 0.10\mu s$$

Using the above values resulted in an inductor value of 330uH as displayed below. This was later increased to 500uH when the 330uH value proved too small.

$$L = \frac{(5 - 100mA * 12\Omega) * \left(\frac{2.5V}{5V}\right) * 10us}{100mA} = 330uH$$

The capacitor value was selected minimize the change in the output voltage. The main goal was to design a capacitor to supply the necessary charge to keep the output at a steady 2.5V . The governing design equations used to determine the capacitor size are as follows:

$$Q = CV \quad I = C \frac{dv}{dt} = \frac{dQ}{dt} \quad \text{solving for } C = \frac{I * dt}{dV}$$

Choosing the low frequency period of 10us with a change in time for each switch of 5us and a voltage change, dV of  $\pm 0.005$  for a total dV =0.01, the capacitor value result is as follows:

$$C = \frac{100mA * 0.5us}{0.01V} = 50uF$$

### 3.4 Comparator Design

The comparator design for the circuit requires a high enough gain to allow the output of full logic level transitions. A two stage differential amplifier is used for the comparator and is fed by the bandgap voltage reference and the feedback,  $V_{out}$ , from the circuit. The differential amplifier senses changes in either the positive or negative inputs and adjusts the output voltage accordingly to respond to changes in  $V_{out}$ . Theoretically, the bandgap voltage reference remains a constant 1.25V as designed, however as previously discussed, there are slight variations in the bandgap reference that will also influence  $V_{out}$ .

The comparator positive terminal is connected to the bandgap voltage and the negative terminal is connected to the  $V_{out}$  feedback loop. The feedback loop runs through a 50k $\Omega$  voltage divider to step it down to 1.25V and is then fed into the negative comparator terminal. This also results in a 25 $\mu$ A current through the circuit input fed back from  $V_{out}$ . When  $V_{out}$  drops below 2.5V, the feedback input will be below 1.25V and the comparator will increase the output voltage to drive  $V_{out}$  back up to 2.5V. When  $V_{out}$  goes above 2.5V, the opposite occurs. The comparator was built using 12 $\mu$ /0.6 $\mu$  PMOS and 6 $\mu$ /0.6 $\mu$  NMOS devices for the branches and 3 $\mu$ /15 $\mu$  NMOS devices on the bottom of each stage. The increased resistance on the long bottom devices reduces the current and results in increased gain. The comparator schematic and symbol are included below in Fig.6 and can be found in the file *comparator\_EM\_f16*. Comparator gain results are included at the end of this section.

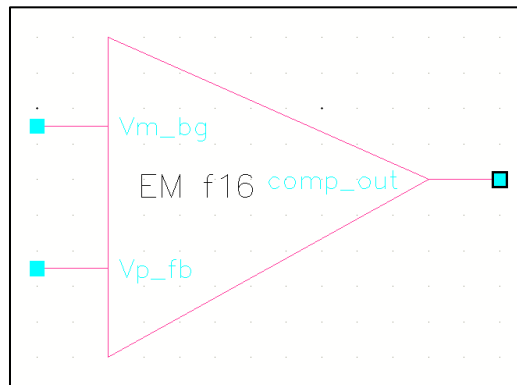
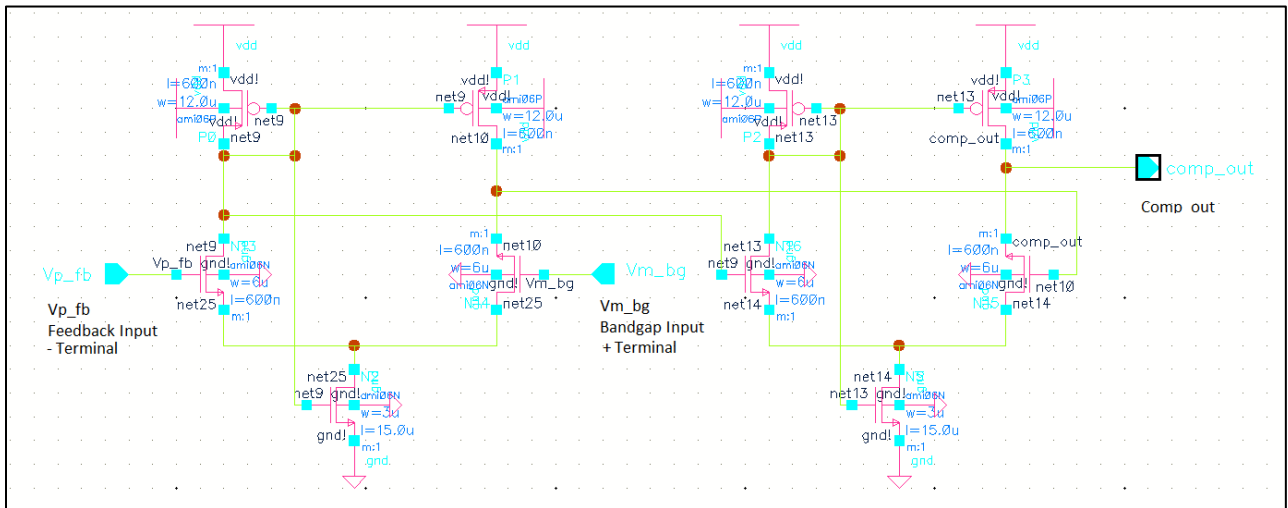


Fig. 6

An initial parametric analysis of the comparator was performed to determine the switching point required to ensure the comparator always has enough gain for the range of VDD relevant to the project, 4VDD to 5.5VDD. The simulation schematic and results are displayed below in Figures 7 and 8, respectively. The final simulation file is titled *sim\_comparator\_EM\_f16* and the saved parametric file is titled *sim\_comparator\_parametric.il*.



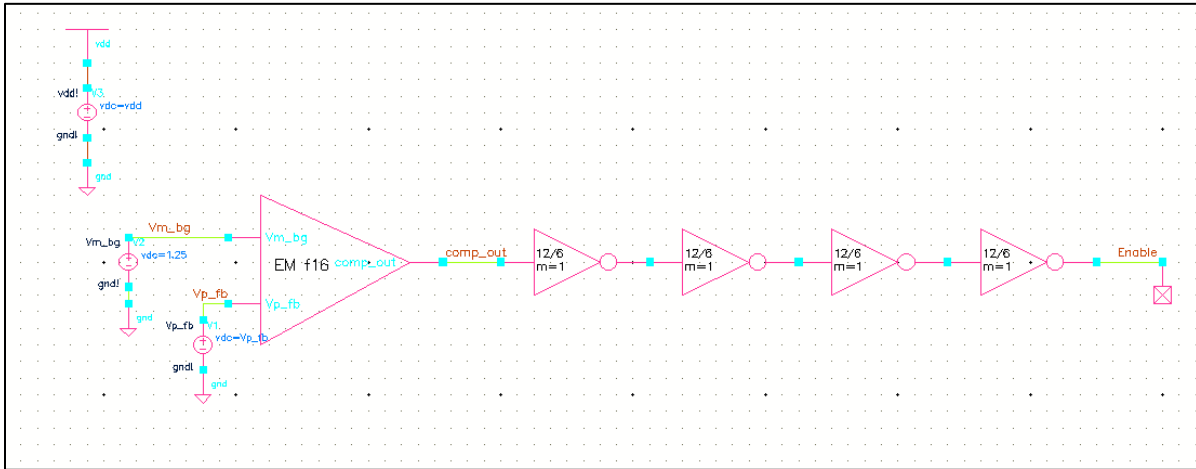


Fig. 7

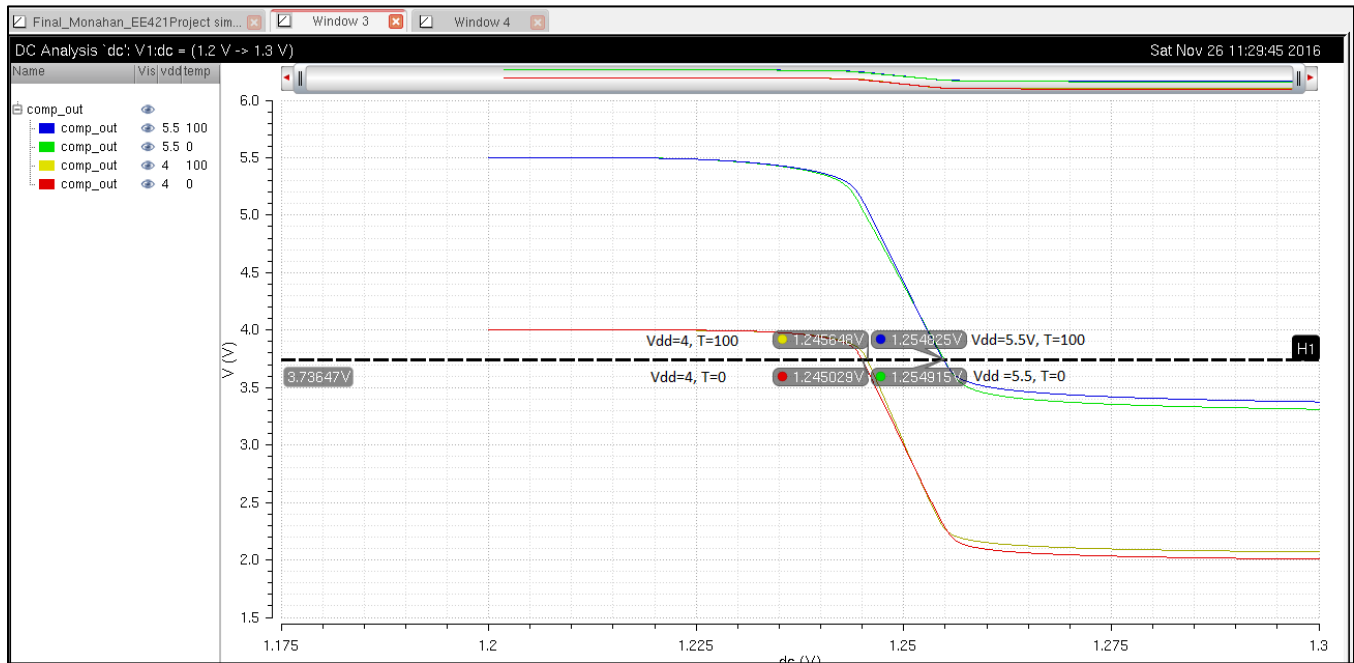


Fig. 8

As seen above in Fig. 8, the horizontal marker displays the desired switching point, approximately 3.73V, for the buffer connected to the comparator output. This value falls in the range where the feedback voltage is centered around 1.25V and ensures the maximum comparator gain is achieved for the range of VDD required. To set the switching point to this value, a 12u/6u inverter was simulated and the sizes of the NMOS and PMOS were varied to move the switching point as necessary. The simulation schematic is displayed in Figure 9 below with the simulation file found in *sim\_comp\_buff*.

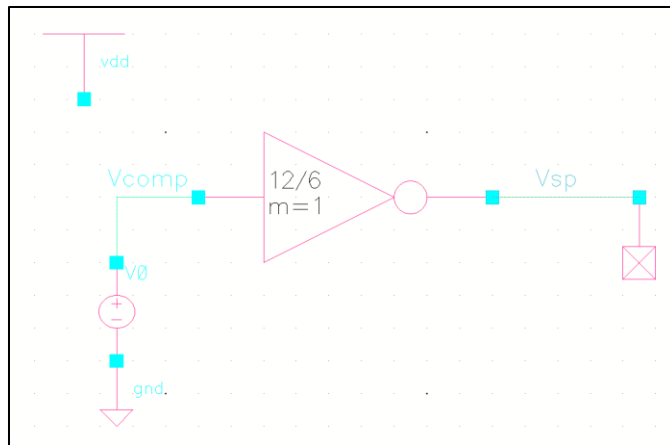


Fig. 9

The initial switching point using a 12u/6u inverter is displayed below in Figure 10. Note the switching point is approximately centered at 2.5V for a sweep from 0V to 5V for NMOS and PMOS devices sized with a 2:1 ratio.

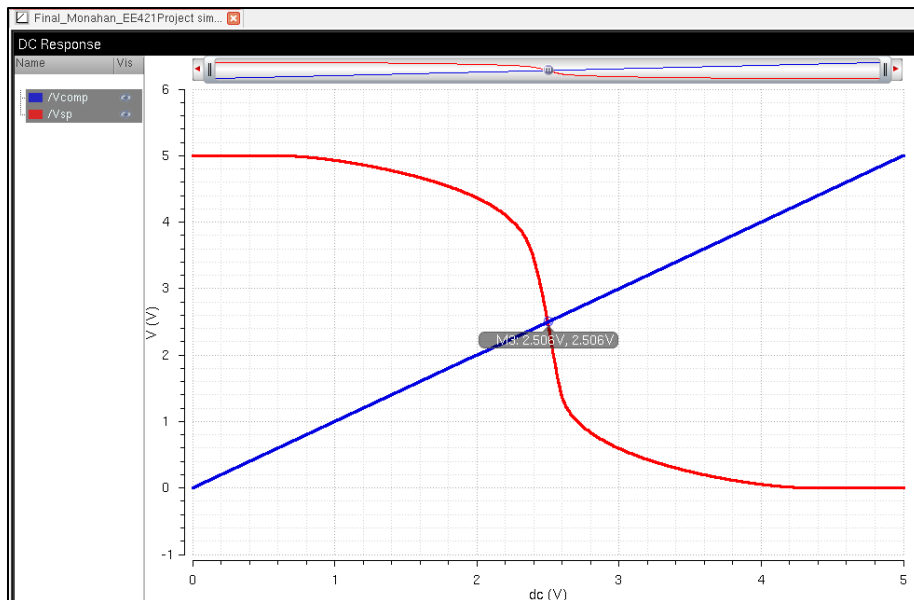


Fig. 10

To move the switching point further from the origin to the approximately 3.73V desired, the NMOS was made weak relative to the PMOS, effectively increasing the NMOS resistance. The final device sizing that enabled the switching point to move to the desired switching point was a PMOS sized 12u/0.6u and an NMOS sized 1.5u/3u. The simulation schematic and results are displayed below in Figure 11 and Figure 12, respectively. The simulation file is titled *sim\_inv\_EM\_f16*. Notice the switching point moved to approximately 3.75V, within the desired range shown in Fig. 8.

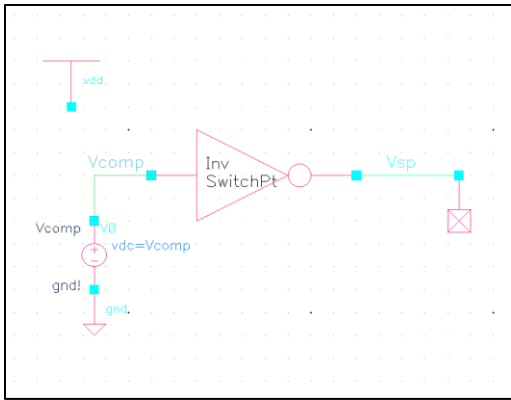


Fig. 11

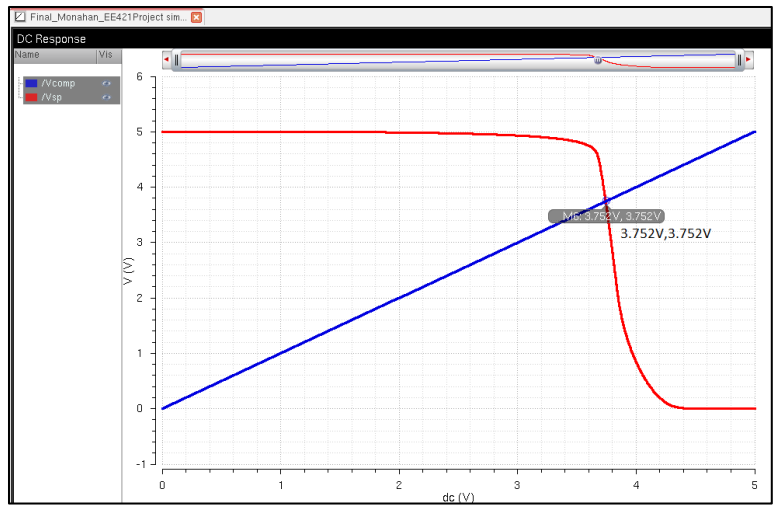


Fig. 12

Once the switching points were found, the buffer stage out of the comparator was completed. The last two stages of the buffer are sized  $12u/6u$  to increase the output gain, reduce switching frequency and thus increase circuit efficiency. These inverters are found in the file *inv\_12\_6\_EM\_f16*. The final comparator stage is displayed below in Figure 13. The first two inverters out of the comparator are the inverters used to move the switching point, found in the file *inv\_switchpoint\_EM\_f16*. Note the final output is labeled 'Enable' and will later be fed into the non-overlapping clock generation circuit.

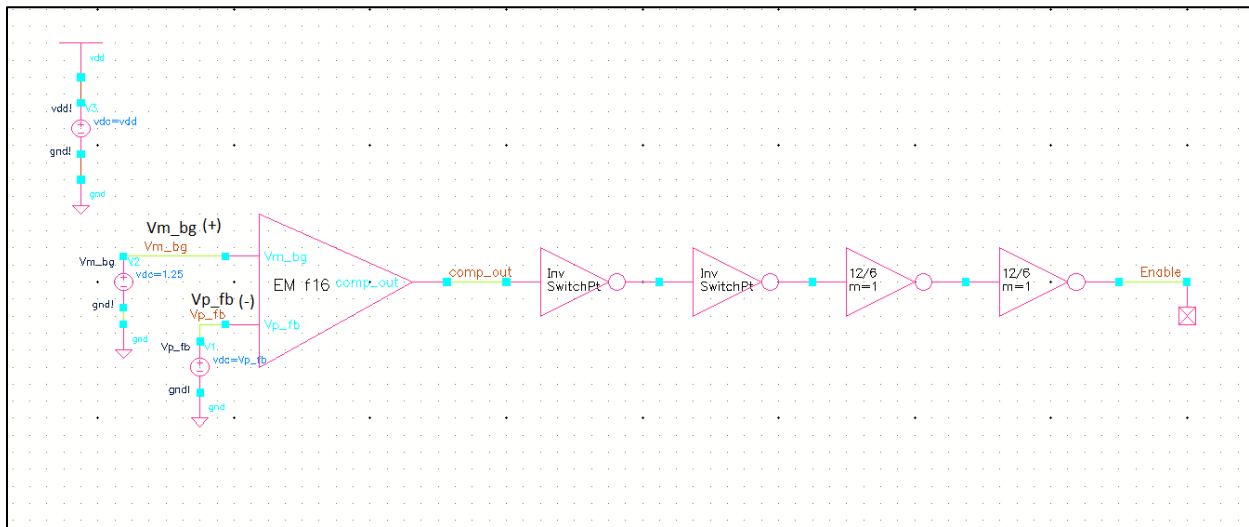


Figure 13

Next, a parametric analysis was performed using the same files, *sim\_comparator\_EM\_f16* and *sim\_comparator\_parametric*, updated to include the redesigned buffer stage. Figure 14 below displays the gain plotted at 'Enable' for VDD at 4V and 5.5V with temperatures at 0°C and 100°C and the feedback voltage,  $Vp\_fb$ , at the negative terminal swept from 1.2V to 1.3V. A summary of the comparator-buffer simulation results is included in Section 5 of this report in Table 3.4.1.

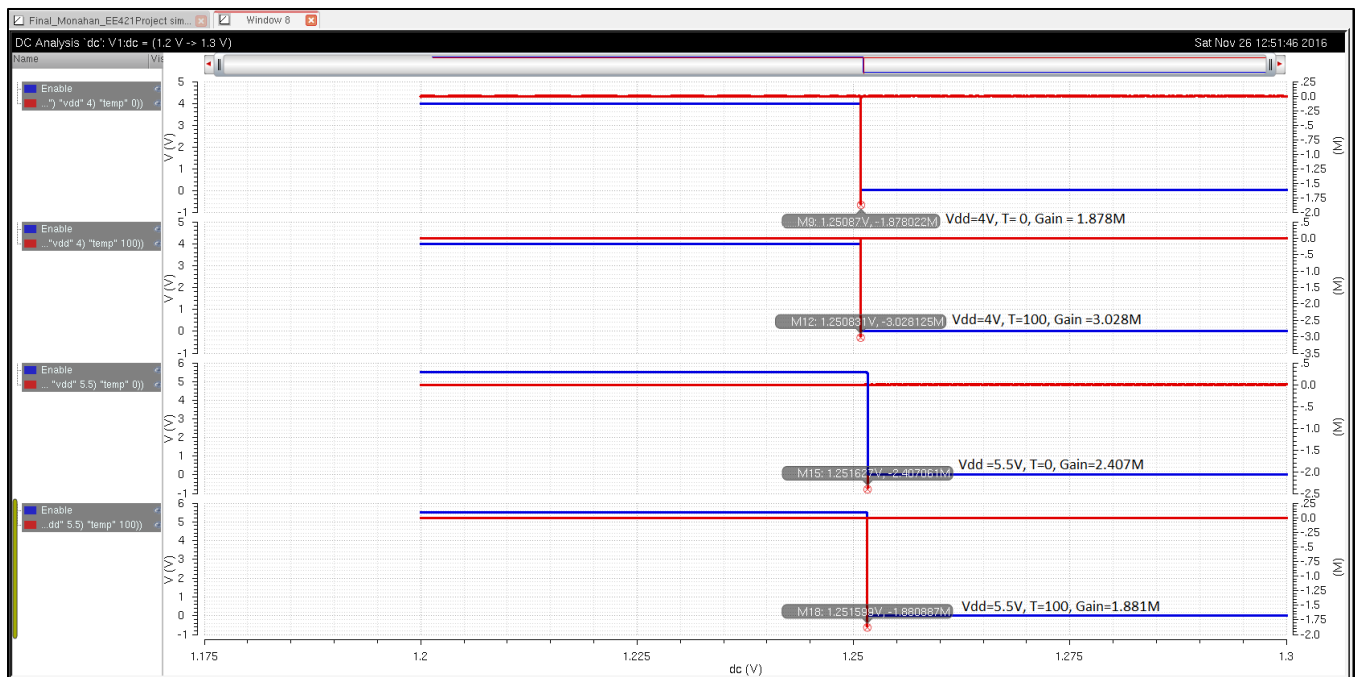


Fig. 14

The simulation results show the gain is high for the comparator and buffer stage at the final output, Enable, and the comparator signal has been squared up by the buffer stage to output strong logic levels into the non-overlapping clock generation circuit, as intended.

### 3.5 Non-Overlapping Clock Generation Circuit

The non-overlapping clock generation circuit consists of an SR-latch and inverters after the SR-latch, as displayed below in Figure 15. This circuit sends output signals, P and N, to the inputs of the final driver stage of the switching power supply design. To avoid both devices being on at the same time, the circuit introduces a separation between the signals set by the delay through the NAND gates and the inverters on the NAND output. For example, in Fig. 15 the output at Clk 1 can never change until the output at Clk 2 changes, thus the NMOS and PMOS devices in the final inverter stage can never be on at the same time, effectively marginalizing the crossover current. This circuit, symbol and layout are found in the file *SR\_EM\_f16*.

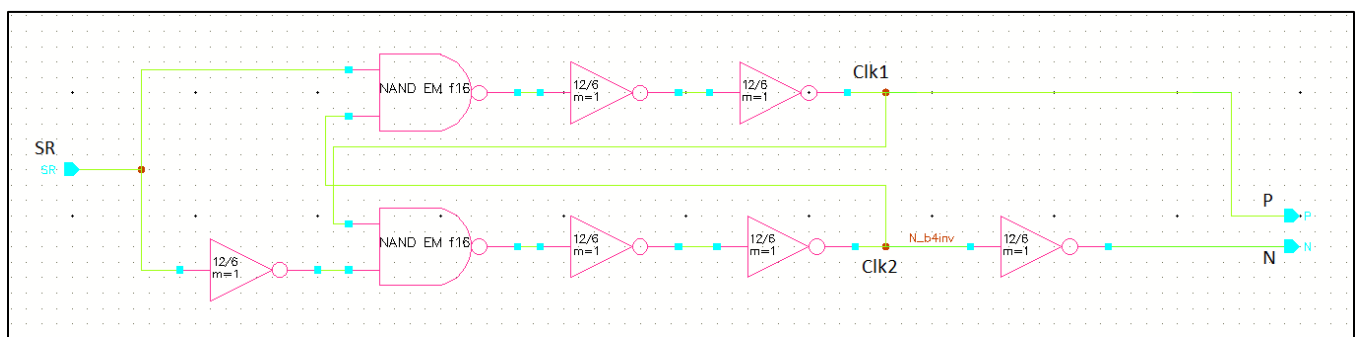


Fig. 15

To verify the non-overlapping clock generation circuit was performing as intended, the outputs P and N were plotted using a parametric analysis and the delays were confirmed for loads from 1mA to 100mA, VDD from 4VDD to 5VDD and temperature from 0°C to 100°C. The results are summarized in Table 3.5.1 in Section 5 with sample simulation results included in Figures 16 and 17 below. The delay times in Table 3.5.1 indicate the down time

between one device switching off and the other device switching on with a range of 1.872ns to 3.273ns. The files used for the simulation are titled *sim\_SyncBuckConv\_EM\_f16* with the parametric analysis load file titled *sim1.il* with IO.Pin and IO.Nin representing the PMOS and NMOS signals out, respectively.

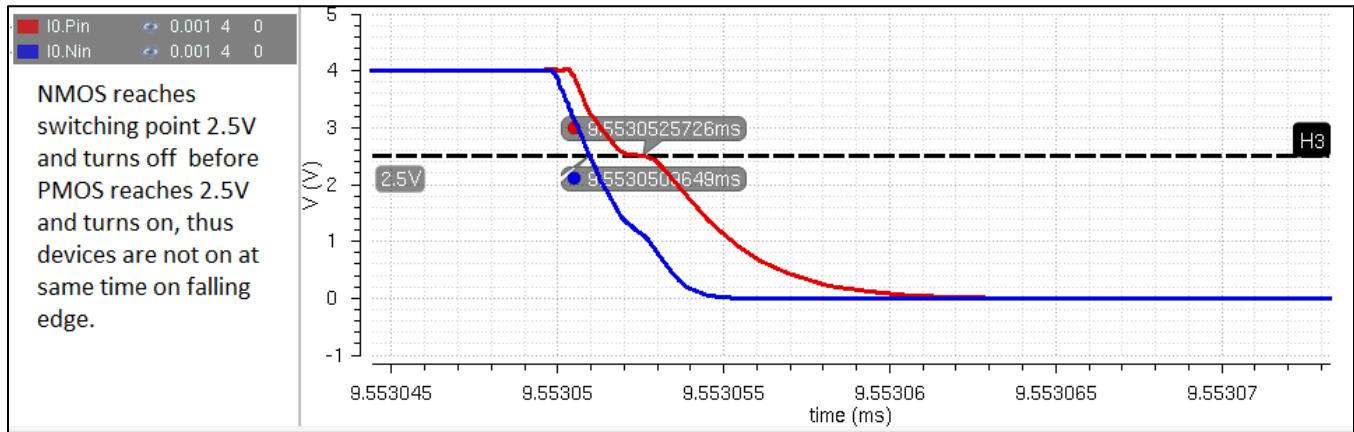


Fig. 16

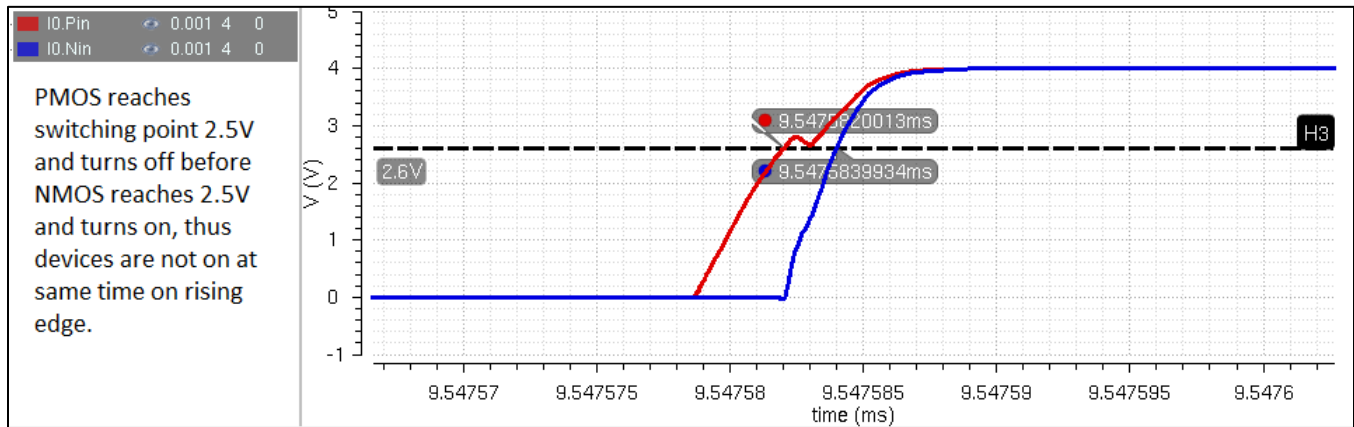


Fig. 17

The results confirm the circuit functions as designed with the outputs delayed sufficiently enough to prevent both devices from turning on at the same time. Figure 16 displays a sample delay for a falling edge showing the NMOS switching off prior to the 2.5V switching point and the PMOS turning on after the NMOS has already turned off. Similarly, Figure 17 shows the PMOS turning off prior to the NMOS turning on at the 2.5V switching point.

### 3.6 Buffer Output Stage

The final stage of the switching power supply on chip circuit is the output buffer stage. The initial design called for a series of buffers starting with a 12u/6u inverter and using a multiplier of eight to add stages of 12u/6u\*8, 12u/6u\*8<sup>2</sup> and lastly 12u/6u\*8<sup>3</sup> exiting the clock generation circuit. However, using this method resulted in the circuit being unstable for all values of VDD simulated. The initial method was repeated using various multiplier stages with new design calculations, different inductor and capacitor values, and different comparator gains. Regardless, the current through the circuit was unstable for all low current loads. Removing the multipliers and using the output buffer included in the final design provided the most optimal, yet still unsatisfactory, results. The final output stage was 24u/12u with minimum lengths and a multiplier of 64. The multiplier was varied as high as 160 and as low as 32 with unsuccessful results. The resistance out of the final driver stage using the resistance design calculations discussed in Section 3.2 is approximately 12Ω.

#### 4. Final Power Supply Design and Simulation

Putting the circuit together using the components previously discussed completed the design process. The final schematic and symbol for the CMOS switching power supply design are displayed below in Figures 18 and 19, respectively. The file for the final Synchronous Buck Converter can be found in *SyncBuckConv\_EM\_f16*.

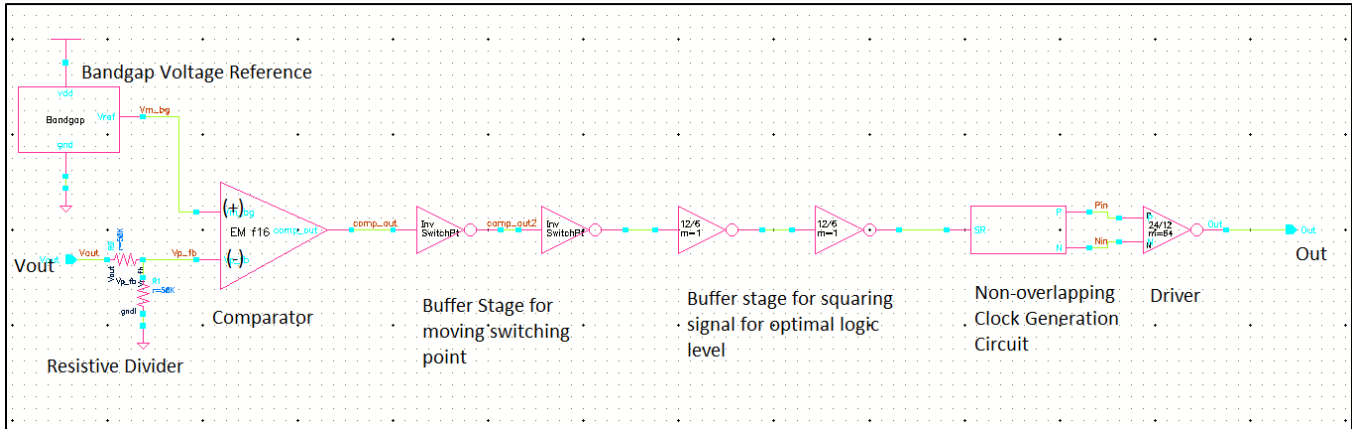


Fig. 18

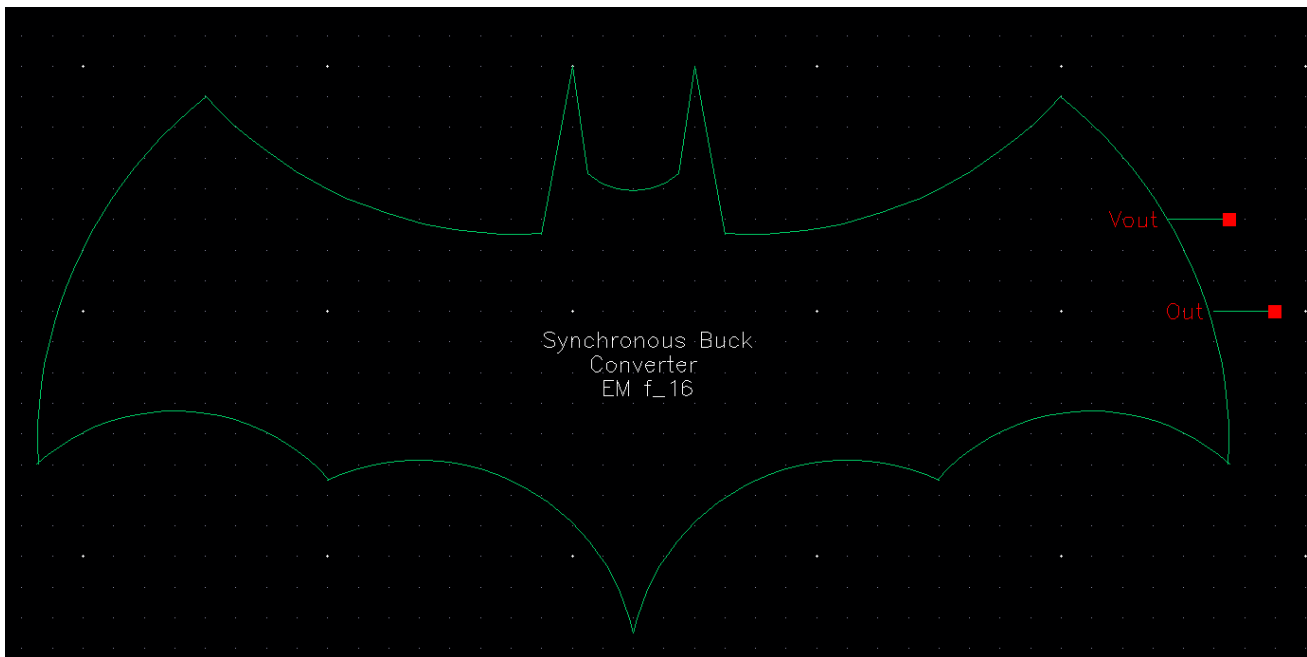


Fig. 19

The last step in the design process was to run a parametric analysis for temperature, current load and VDD. The first simulation will sweep these parameters according to project specifications and can be found in the file *sim\_SyncBuckConv\_EM\_f16* with the parametric analysis file titled *sim1.il*. Simulation results including output voltage, V<sub>out</sub>, current into the synchronous Buck Converter input through V<sub>out</sub>/V<sub>in</sub>, current through the inductor, and output switching frequency, are summarized in Tables 4.1, 4.2 and 4.3 in Section 5. Switching frequency was obtained using the circuit output 'Out' and the calculator 'frequency' function. Sample simulation

results are included below in Figures 20 and 21. Fig. 20 displays  $V_{out}$  ranging from 2.4867V to 2.512V and Fig. 21 displays the current into the circuit ranging from 24.872uA to 25.131uA, well within project design specifications.

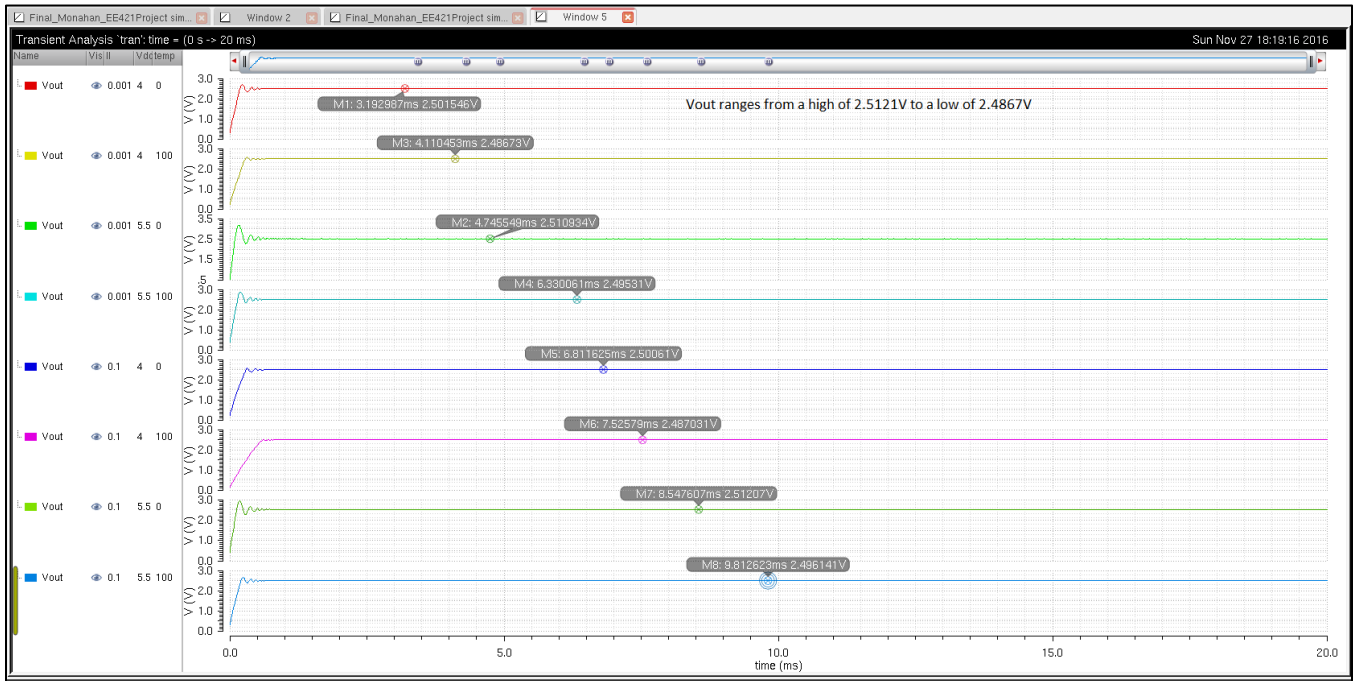


Fig. 20  $V_{out}$  simulation results with varying VDD, current load and temperature.



Figure 21 Current into comparator with varying VDD, current load and temperature.

Additionally, the same simulations were completed to show the circuit responses for a pulsing current load with an arbitrarily selected delay time of 3ms and pulse width of 3ms with a period of 6ms. The point of this

simulation is to demonstrate circuit response to rapid changes in load currents. The simulation files used for this are *sim2\_SyncBuckConv\_EM\_f16* with the parametric analysis file titled *sim2.il*. The results for this simulation are summarized in Tables 4.4, 4.5, and 4.6 in Section 5. Sample simulation results for the pulse load current simulations are displayed in Figures 22 and 23. Note in Fig. 23, the current stays within project specifications.

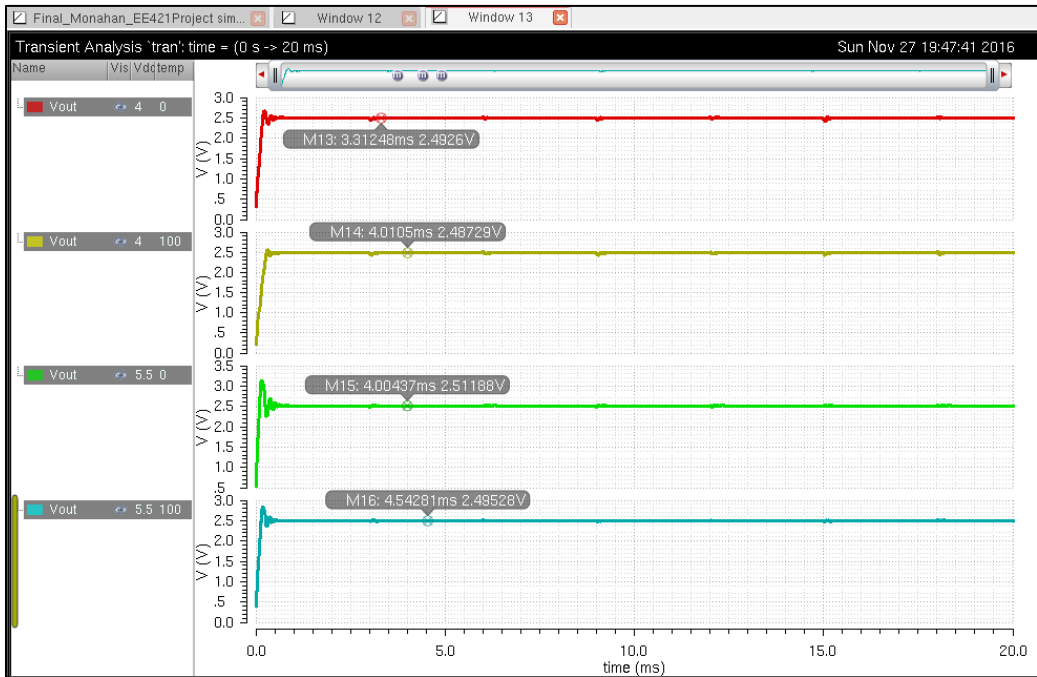


Fig. 22 Vout for varying VDD and temperature with a 0A to100mA pulse current load.

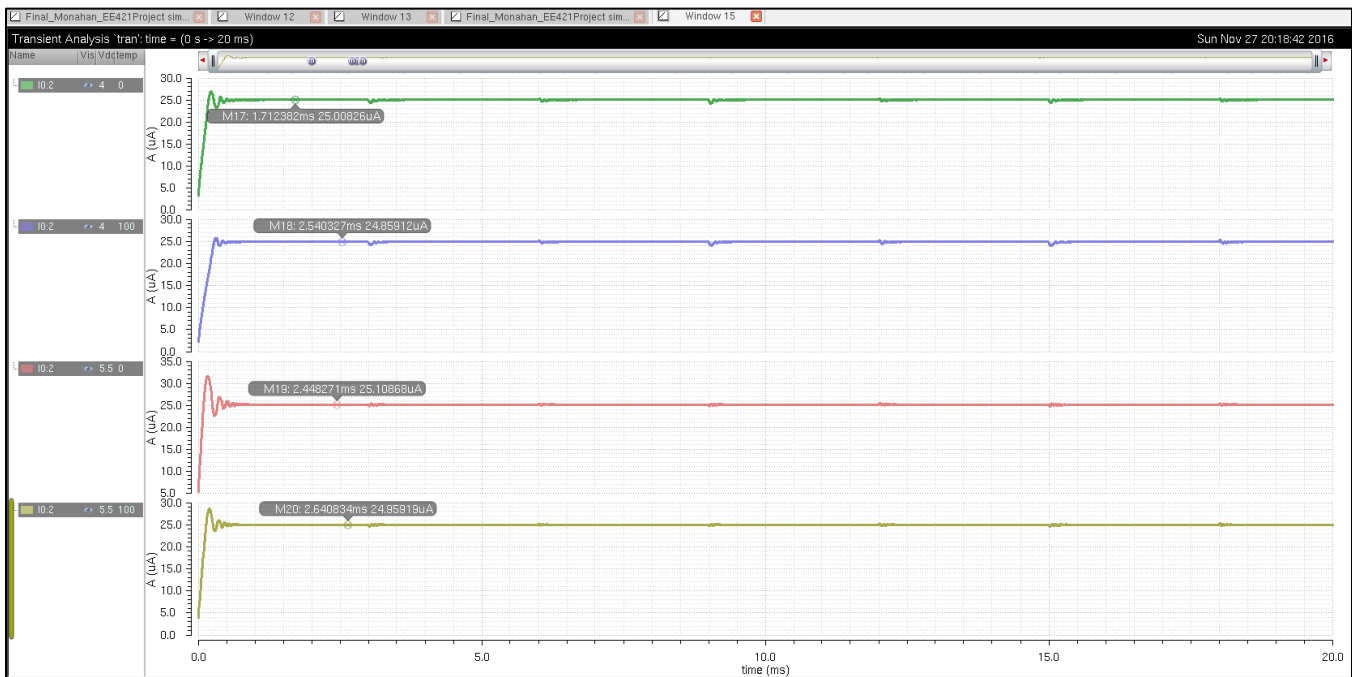


Fig.23 Current into comparator for varying VDD and temperature with a 0A to100mA pulse current load

Finally, the circuit efficiency was calculated using the following:



$$\varepsilon = \frac{I_{Load} * V_{out}}{I_{VDD,avg} * V_{DD}}$$

with results summarized in Section 5, Table 4.7. The efficiency hand calculations ranged from 67.95% at the lowest end up to 83.28% at the high end. Figure 24 displays a plot of Efficiency versus varying load currents over a range of VDD. The excel file used for this data, *efficiency\_excel.csv*, is included in the project file. The simulation to accumulate the data used for this table is found in the file *sim\_efficiency\_SyncBuckConv-EM\_f16* with parametric analysis file *sim\_efficiency*. The table indicates efficiency decreases as VDD increases for smaller loads and trends upward as the current load increases.

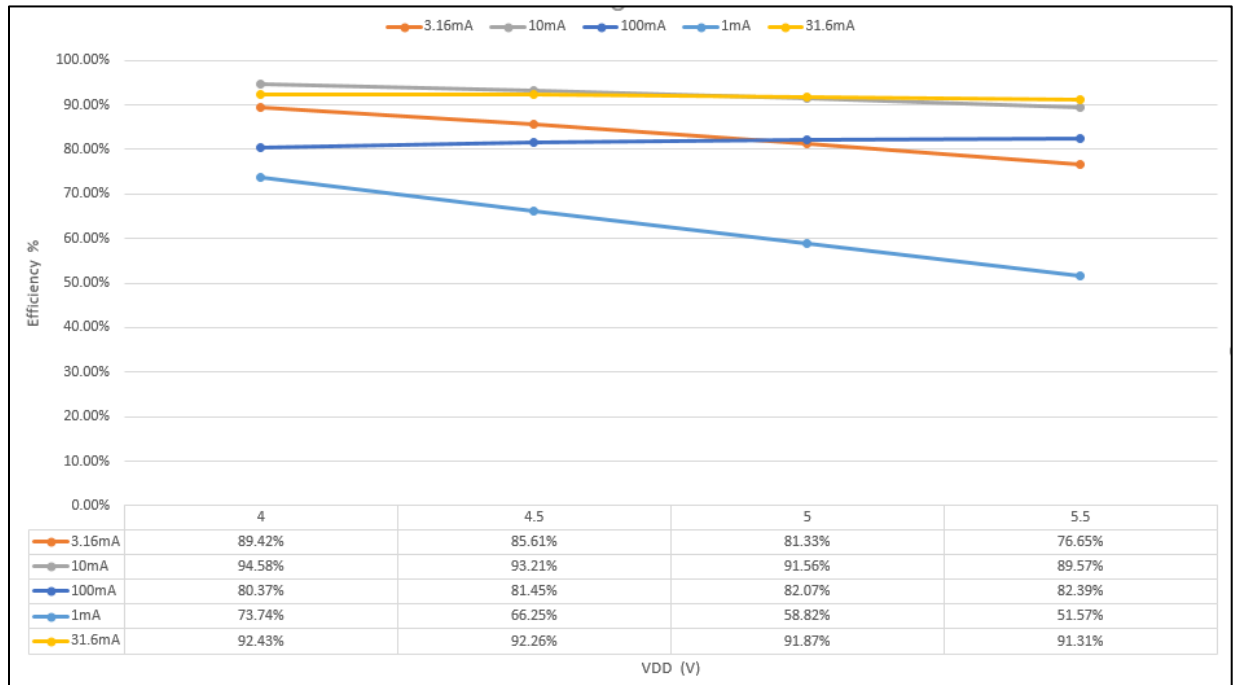


Fig. 24

## 5. Summary of Results

The following tables present a summary of the results determined via the design process outlined above.

### Comparator gain under varying VDD and Temperature

VDD (V)	Temperature (°C)	Vp_fb (V)	Gain
4	0	1.2508	-1.878M
4	100	1.2508	-3.028M
5.5	0	1.2516	-2.407M
5.5	100	1.2516	-1.881M

Table 3.4.1

### Non-Overlapping Clock Generation Circuit Delays on Rising and Falling Edges

Iload (mA)	VDD (V)	Temp (°C)	Rising Edge Delay(ns)	Falling Edge Delay (ns)
1	4	0	2.079	1.608
1	4	100	2.889	1.973
100	4	0	1.872	1.160
100	4	100	2.617	1.262
1	5.5	0	2.225	2.385
1	5.5	100	2.976	2.896
100	5.5	0	2.409	2.266
100	5.5	100	3.273	2.547

Table 3.5.1

CMOS switching power supply results for *sim\_SyncBuckConv\_EM\_f16* (Tables 4.1-4.3)

VDD (V)	Temperature (°C)	Iload (mA)	Vout (V)
4	0	1	2.5015
4	0	100	2.5006
4	100	1	2.4867
4	100	100	2.4870
5.5	0	1	2.5109
5.5	0	100	2.5121
5.5	100	1	2.4953
5.5	100	100	2.4961

Table 4.1 Voltage Out

VDD (V)	Temperature (°C)	Iload (mA)	Inductor Current (mA)	Switching Power Supply Input Current (uA)
4	0	1	13.801	25.019
4	0	100	100.235	25.014
4	100	1	-7.554	24.874
4	100	100	90.403	24.872
5.5	0	1	-3.887	25.131
5.5	0	100	90.363	25.128
5.5	100	1	-10.383	24.975
5.5	100	100	119.01	24.962

Table4.2 Currents

VDD (V)	Temperature (°C)	Iload (mA)	Switching Frequency
---------	------------------	------------	---------------------

			measured at Out (kHz)
4	0	1	66.46
4	0	100	64.37
4	100	1	64.29
4	100	100	56.34
5.5	0	1	72.84
5.5	0	100	76.03
5.5	100	1	70.01
5.5	100	100	62.27

Table 4.3 Switching Frequency

CMOS switching power supply results for *sim2\_SyncBuckConv\_EM\_f16* using Pulse Current

VDD (V)	Temperature (°C)	Vout (V)
4	0	2.493
4	100	2.487
5.5	0	2.512
5.5	100	2.495

Table 4.4 Voltage with Pulse Current Load

VDD (V)	Temperature (°C)	Inductor Current Low(mA)	Inductor Current High (mA)	Switching Power Supply Circuit Current (uA)
4	0	-12.994	104.214	25.008
4	100	-12.160	108.103	24.859
5.5	0	-13.281	113.214	25.109
5.5	100	2.723	116.163	24.959

Table 4.5 Currents with Pulse Current Load

VDD (V)	Temperature (°C)	Switching Frequency measured at Out (kHz)
4	0	56.95
4	100	55.11
5.5	0	64.87
5.5	100	59.59

Table 4.6 Switching Frequency with Pulsed Current Load

VDD (V)	Temperature (°C)	$I_{VDD,avg}$ (mA)	Efficiency %
4	0	76.29	81.92

4	100	91.97	67.95
5.5	0	54.58	83.28
5.5	100	56.07	81.07

Table 4.7 Efficiency at 100mA Current Load

## 6. CMOS Switching Supply Layout

The bandgap layout is displayed below in Figure 25. File: **bandgap**

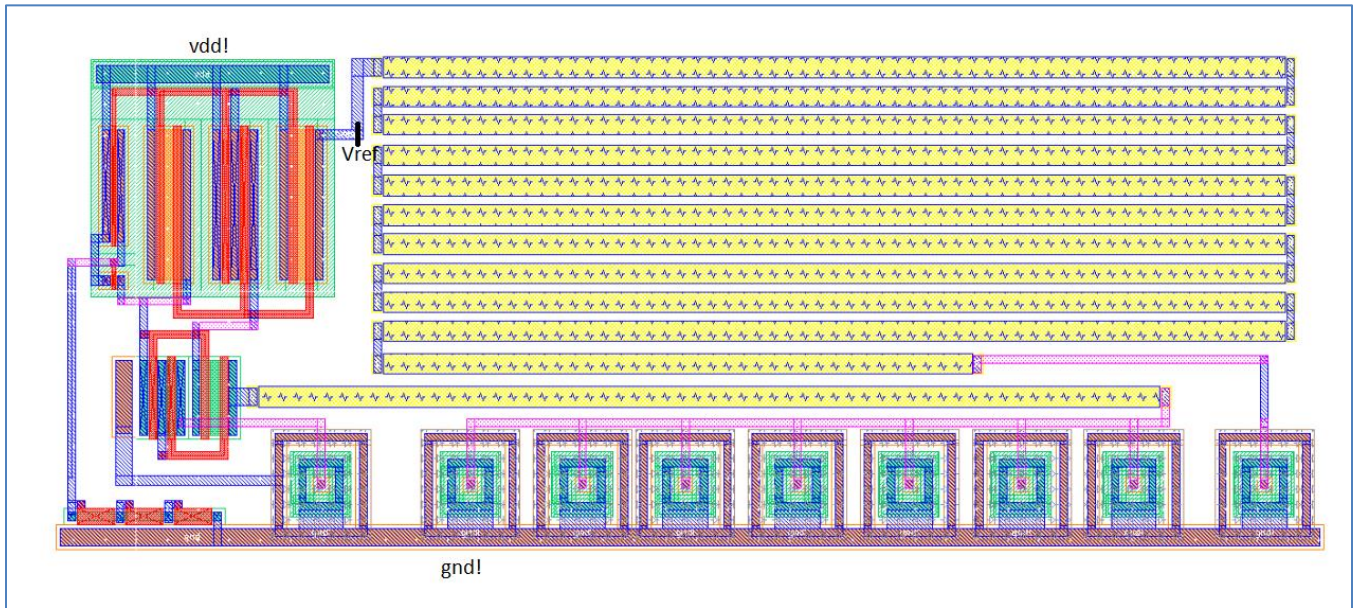


Fig. 25

The comparator layout is displayed below in Figure 26. File: **comparator\_EM\_f16**.

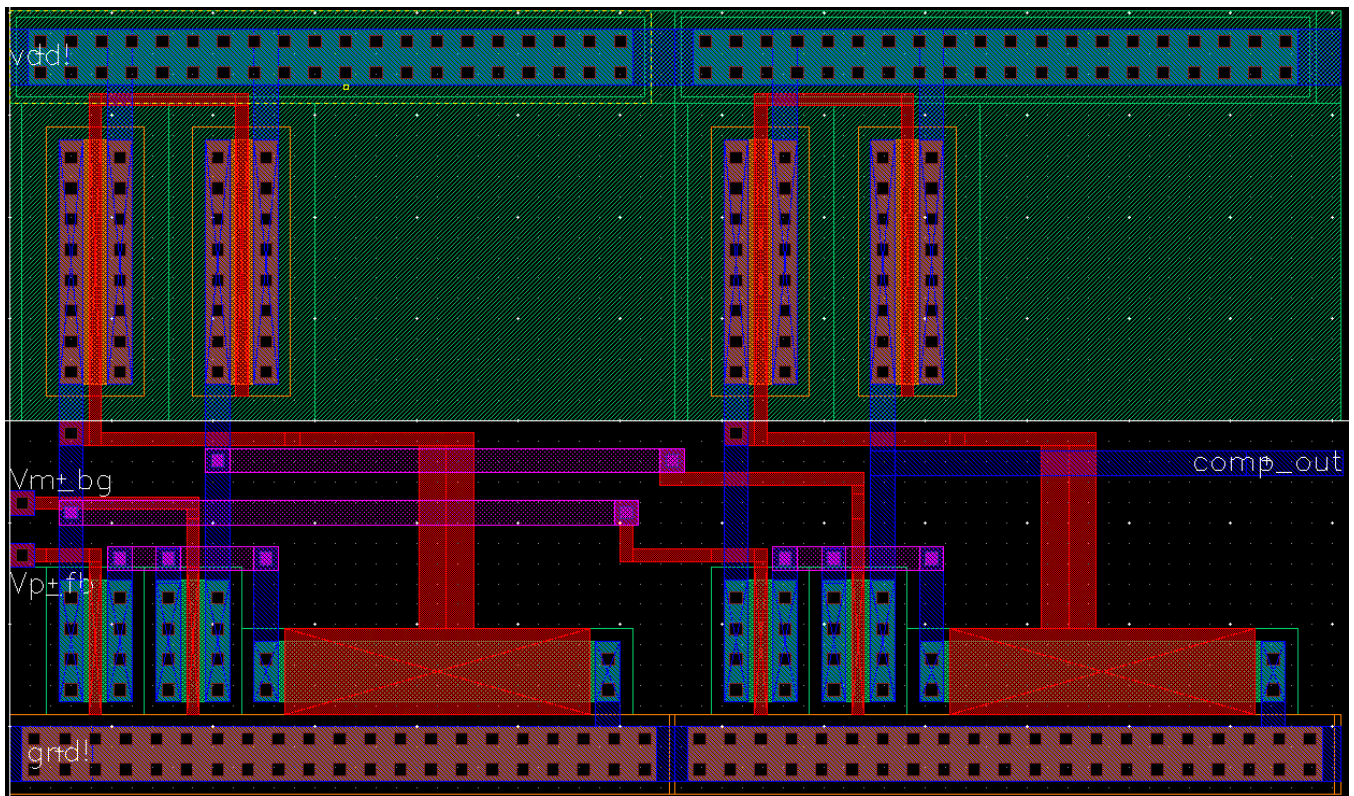


Fig. 26

The 12u/6u inverters used in the buffers and non-overlapping clock generation circuit have the same layout displayed below in Figure 27. File: `inv_12_6_EM_f16`.

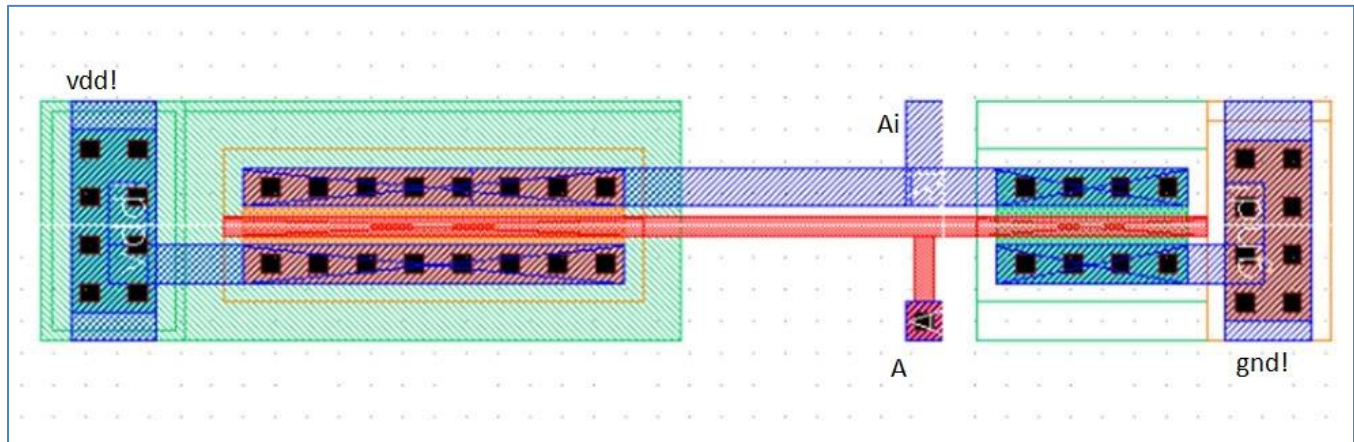


Fig. 27

The non-overlapping clock generation circuit layout is displayed below in Figure 28.

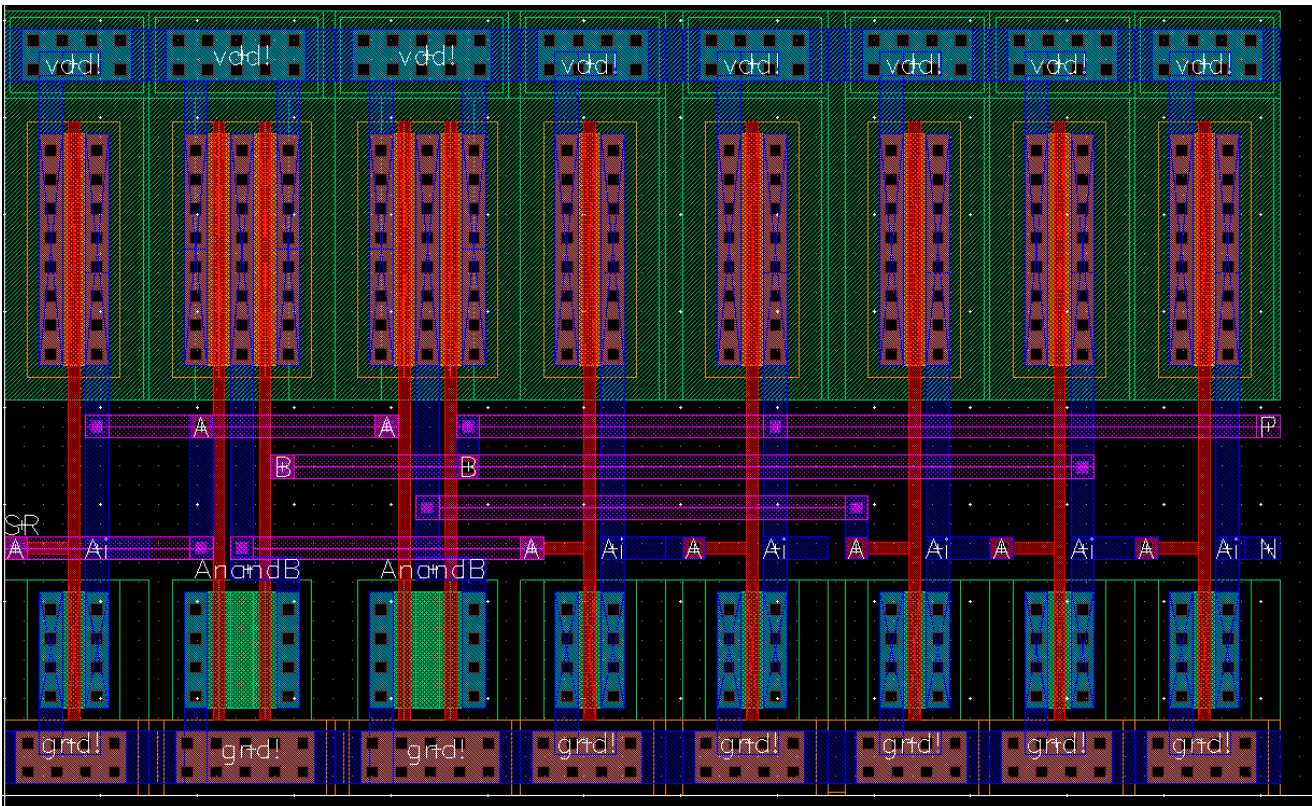


Fig. 28

The final buffer stage layout is displayed in Figure 29. This is a 24u/12u stage with a multiplier of 64 and minimum lengths. File: `inv_1_2_IP_EM_f16`.

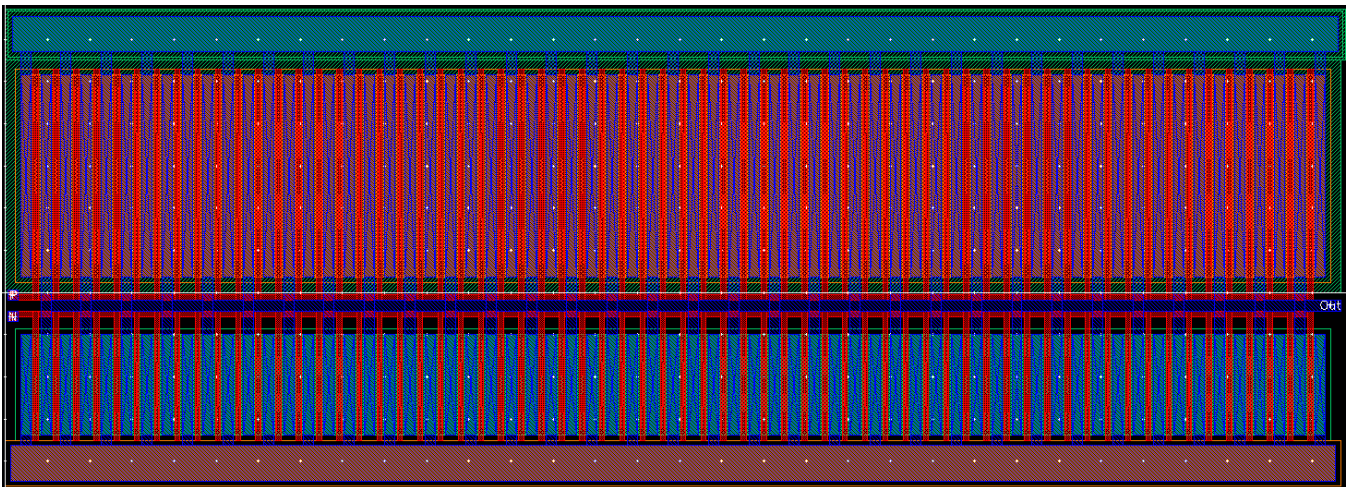


Fig. 29

The final Synchronous Buck Converter layout putting all components together is displayed below in Figure 30.  
File: SyncBuckConv\_EM\_f16.

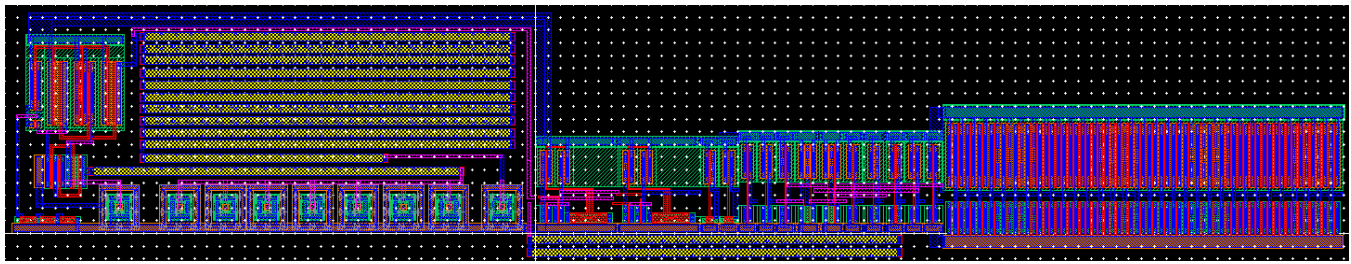
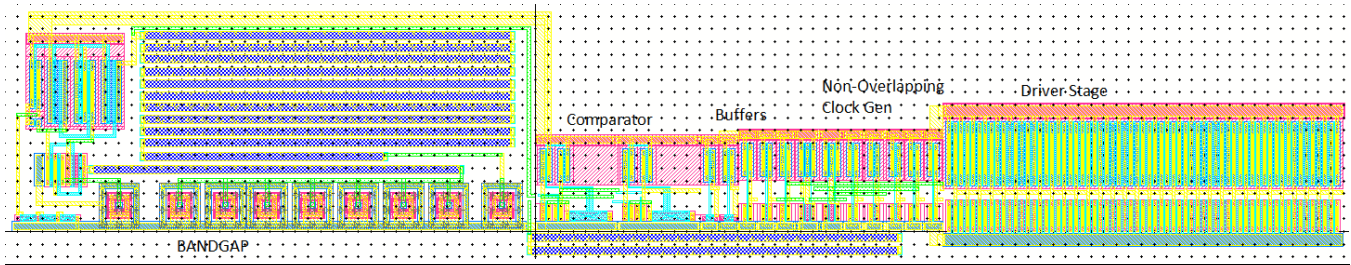


Fig. 30

The Synchronous Buck Converter connected to a padframe is seen in Figures 31 , 32 and 33. File:  
SyncBuckConv\_Pad\_EM\_f16.

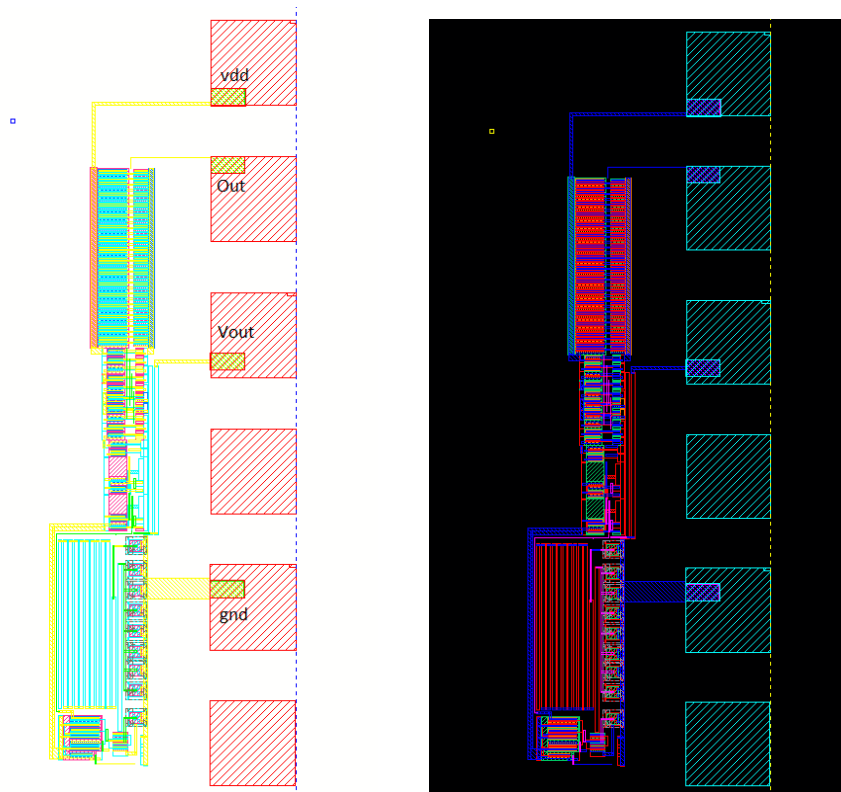


Fig. 31

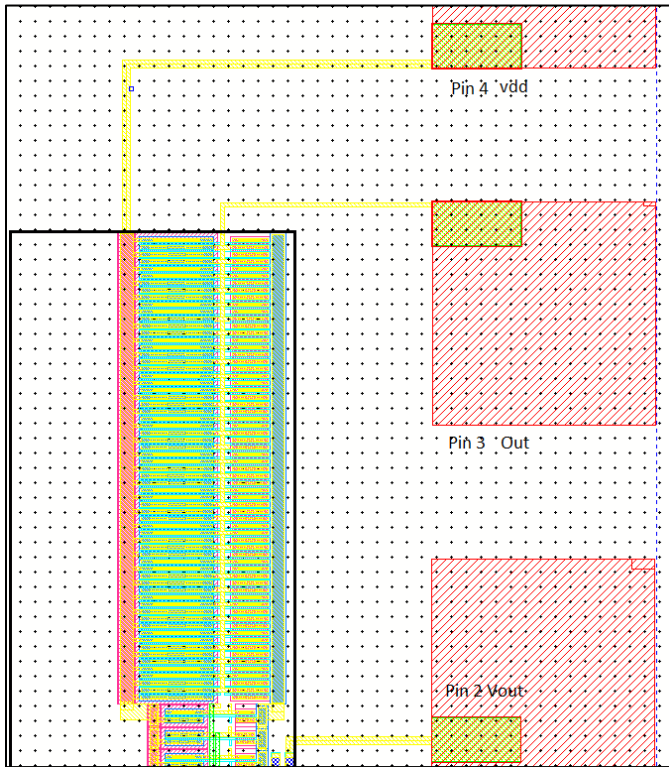


Fig. 32

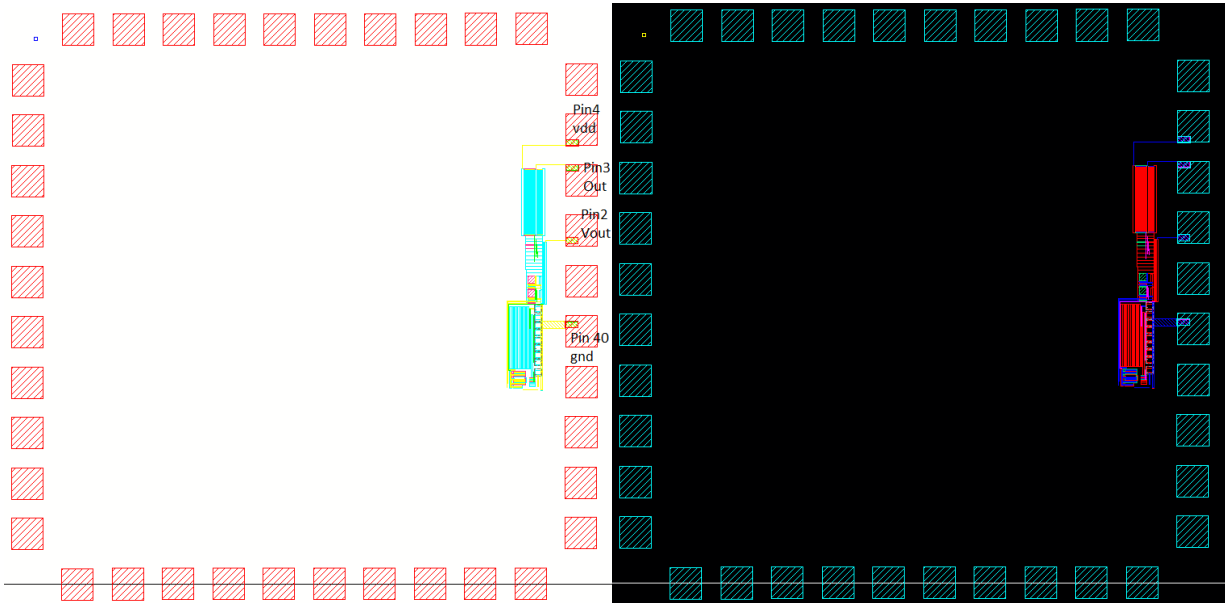
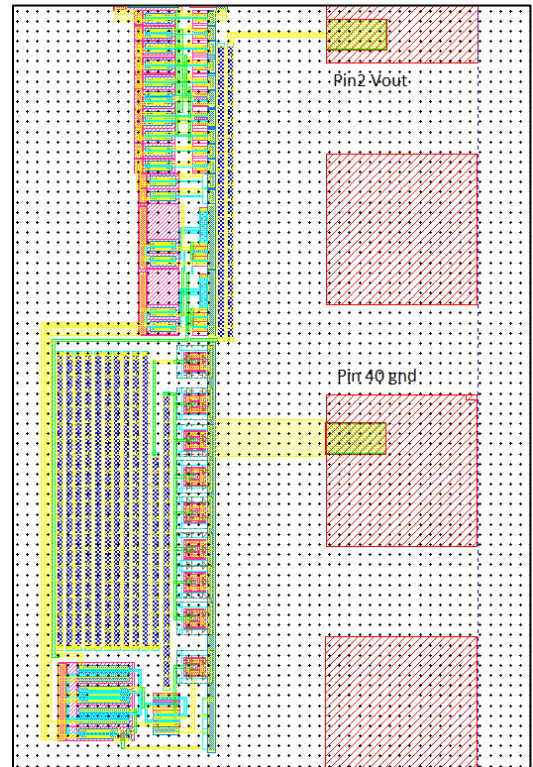


Fig. 33



## Pin Diagram

The Synchronous Buck Converter pin diagram is displayed below in Figure 32.

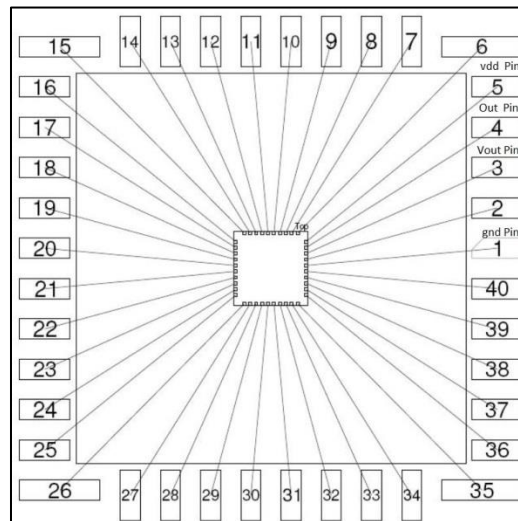


Fig. 32

The pins are connected as follows:

- Pin 40- gnd
- Pin 2 - Vout
- Pin 3 - Out
- Pin 4 - vdd

## 7. Conclusion

The CMOS switching power supply design was initially a seemingly difficult project that required the correlation of topics covered during the duration of the course. There were numerous failures throughout the design process that assisted in learning and creating a moderately functioning design. The project also provided an opportunity to analyze my strengths and weaknesses as a designer and to learn from the mistakes made during the design process. Despite these mistakes and failures, a successfully functioning Synchronous Buck Converter that meets required specifications as outlined in the project parameters was designed and is presented for evaluation.

## Index

### Simulation File Reference Page

1. sim\_SyncBuckConv\_EM\_f16 - parametric analysis with variables current load, I<sub>L</sub>, VDD, and temperature using file sim1.il.
2. sim2\_SyncBuckConv\_EM\_f16 - parametric analysis with variables VDD, and temperature and a pulsed current load using file sim2.il.
3. sim\_efficiency\_SyncBuckConv\_EM\_f16 - parametric analysis for collecting data points to plot efficiency for varying loads and VDD. Uses parametric analysis file sim\_efficiency.il with results in file efficiency\_excel.csv.
4. sim\_bandgap = simulation showing bandgap voltage reference and temperature effects.
5. sim\_comp\_buff = simulation showing switching point for 12u/6u inverter in buffer stage
6. sim\_switchptbuff = simulation showing switching point adjustment out of comparator
7. sim\_temp\_bandgap = demonstrated temperature variations in bandgap
8. sim\_temp\_bandgap2= parametric analysis demonstrating bandgap operation for variations in temperature and VDD
9. sim\_comparator\_EM\_f16 = simulations demonstrating comparator operation