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## DAVID SANTIAGO

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[CMOSedu.com/jbaker/students/david/david.htm](http://CMOSedu.com/jbaker/students/david/david.htm)

### EDUCATION

University of Nevada, Las Vegas – B.S. in Electrical Engineering, May 2020

GPA: 3.64

University of Nevada, Las Vegas – M.S. in Electrical Engineering, Est. Fall 2022

GPA: 4.00

### PROJECTS

#### **Design of a High-Speed Transimpedance Amplifier (w/2<sup>nd</sup> Stage Voltage Amplifier)**

A current-input, voltage-output, Transimpedance Amplifier (TIA) that has a gain of 30kΩ used to detect current pulses from an Avalanche Photo-Diode (APD) at high speeds. A voltage amplifier with a voltage-input, voltage-output gain of 10 is used to extend the bandwidth of the TIA and to have a lower output resistance to be able to drive a 1pF capacitive load.

#### **Automated Photon Counting System**

An automated test equipment system that automates a Stanford Research Systems Photon Counter and power supplies. This system was created using each instrument's respective GPIB interface and MATLAB. The system was provided automated data collecting and data analysis. A tutorial (in text and video form) was also created to explain the process.

#### **A K-Delta 1-Sigma Noise Shaping Modulator**

An analog-to-digital 1-bit converter that uses 8 feedback paths (8-delta) all clocked out of phase by 1/8<sup>th</sup> of a clock cycle to create an summation node at an integrator (1-sigma) that produces an oversampling effect. The main property of the K-Delta 1-Sigma modulator is to push unwanted noise into a very high frequency range so that the operating frequency will have high Signal-to-Noise ratio. Four topologies were simulated, with a resistive topology to be the simplest to implement.

**More projects with pictures and details can be viewed at: [CMOSedu.com/jbaker/students/david/david.htm](http://CMOSedu.com/jbaker/students/david/david.htm)**

### EXPERIENCE

#### **Freedom Photonics Layout Design Engineering Intern**

**December 2021 – June 2022**

- Completed layout designs in TowerJazz's SBC18HA 180nm process with radiation hardening techniques
- Successfully completed a 5mm<sup>2</sup> tape-out mission

#### **UNLV Teaching Assistant**

**August 2020 – Present**

- Prepared remote lesson plans for electrical and computer engineering students
- Provided quality feedback to enhance student learning
- Courses: Signal Processing (Analog/Digital), Circuits, Electromagnetics

#### **UNLV Research Assistant**

**January 2019 - Present**

- Conducted research for Dr. R. Jacob Baker at UNLV, with a focus on data analysis, circuit design, instrumentation, and board debugging
- IC design/ layout using Cadence Virtuoso in ON Semiconductor's C5 and TowerJazz's SBC18HA 180nm processes

#### **Tau Beta Pi, The Nevada Beta Chapter Leadership: Fall 2019 VP, President 2020**

**Fall 2019 – Fall 2020**

- Managed the only engineering honor society at the UNLV College of Engineering
- Maintained good communication with the college, members, future initiates, as well as with the national executives
- Attended multiple Tau Beta Pi leadership, professional, and national conferences

### ADDITIONAL SKILLS

Affinity Designer/Photo, Analog/Digital Circuit Design, Assembly Language, Audacity, Automatic Test Equipment, C, C++, CAD, Cadence Virtuoso, Digital Filter Design, Diva DRC, Eagle, Embedded Systems Design, FL Studio, GPIB Interfacing, IC Design/Layout, IoT, Linux Command Line, LTspice, MATLAB, ModelSim, OBS, PCB Design, Quartus, Signal Processing, Soldering, Sony Vegas, Verilog

### REFERENCES:

Dr. R. Jacob Baker – [rjacobbaker@gmail.com](mailto:rjacobbaker@gmail.com) – (702)-895-4125

Dr. Peter Stubberud – [peter.stubberud@unlv.edu](mailto:peter.stubberud@unlv.edu) – (702)-895-0869

Dr. Robert A. Schill Jr. – [robert.schill@unlv.edu](mailto:robert.schill@unlv.edu) – (702)-895-4075

ADDITIONAL REFERENCES AVAILABLE UPON REQUEST