# EE 421 – Digital Electronics

# Course Project: Negative Charge Pump

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University of Nevada, Las Vegas

Professor Baker

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# Forward

Dr. Baker:

The library I sent you is titled “OfficialProject”. The cell containing my schematic, layout, and extracted layout which yields a successful LVS is titled “BAKER”. The cell containing my overall schematic for which to simulate is titled “BAKERsimthis”. I hope this clearly allows you to simulate my project without any difficulties, and I would like to thank you for yet another wonderful semester and learning experience.

# Introduction

The objective of this course project is to design and layout a charge pump circuit using Cadence. The project was prefaced with a bandgap reference circuit schematic provided by Professor Baker for which a layout was created. The purpose of the bandgap circuit implemented is to generate a reference voltage of approximately 1.25 V despite temperature and VDD variations. The next portion of the project consisted of designing a circuit to sense the input voltage, *Vin*, of the bandgap and output a voltage, *Enable*, to be a logic 1 (VDD) for *Vin* greater than -2.5 V and a logic 0 (ground = 0 V) for *Vin* less than -2.5 V. Furthermore, the project should implement a ring oscillator, designed to be enabled by *Enable*, which will drive a charge pump that supplies -2.5 V with load currents ranging from 0 to 200 uA. Lastly, the design should meet the design constraints stated below.

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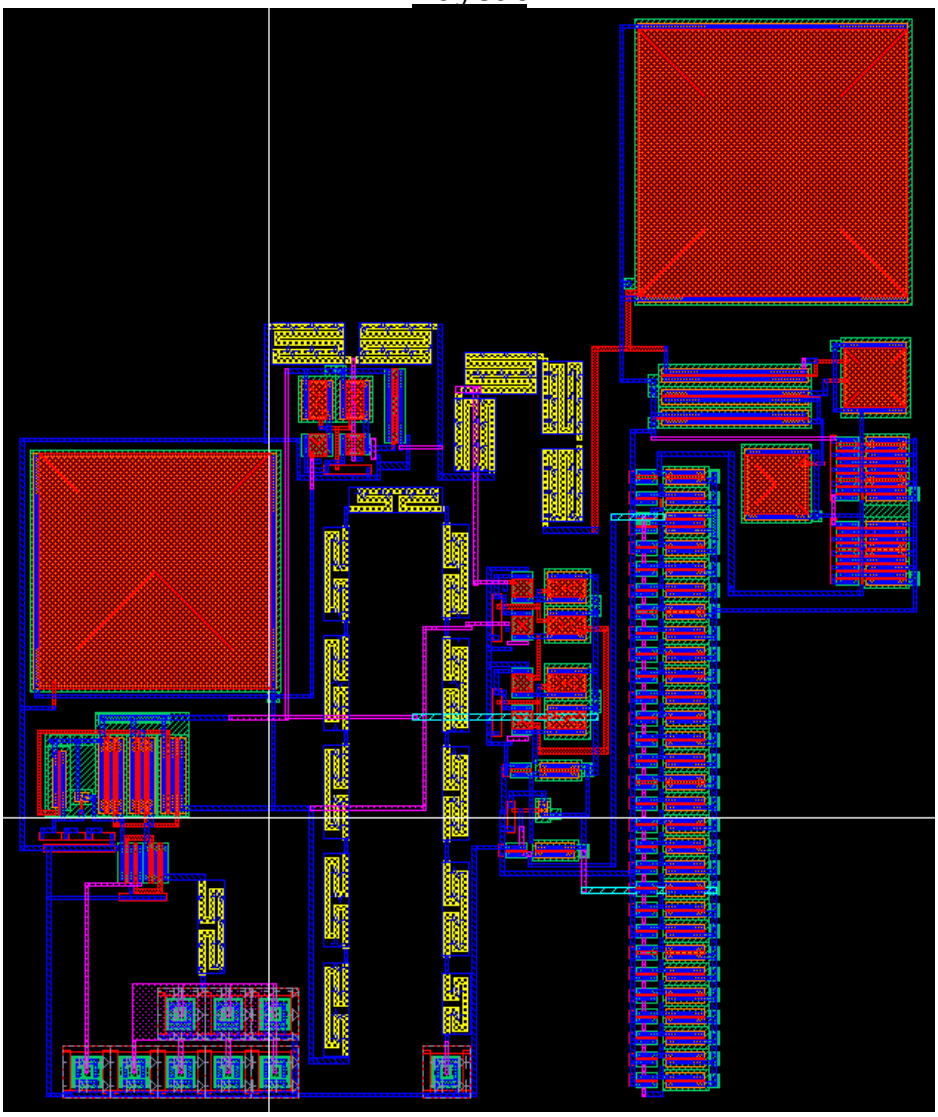
# Design Constraints

- *Vin* should draw between 10 and 50 uA of current
- Sensing circuit should have at least a 100 mV built in hysteresis
    - *Vin* > -2.45 V ➔ *Enable* = Logic 1 & *Vin* < -2.55 V ➔ *Enable* = Logic 0
- Design characterized for VDD ranging from 4.5 to 5.5 V
- Design characterized for temperature ranging from 0 to 100C

# Complete Design

**Layout**



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## DRC

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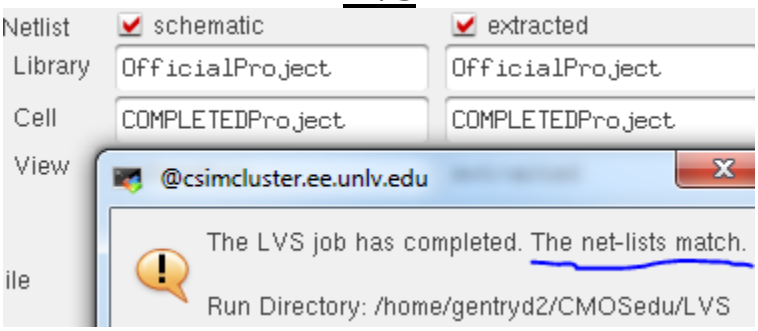
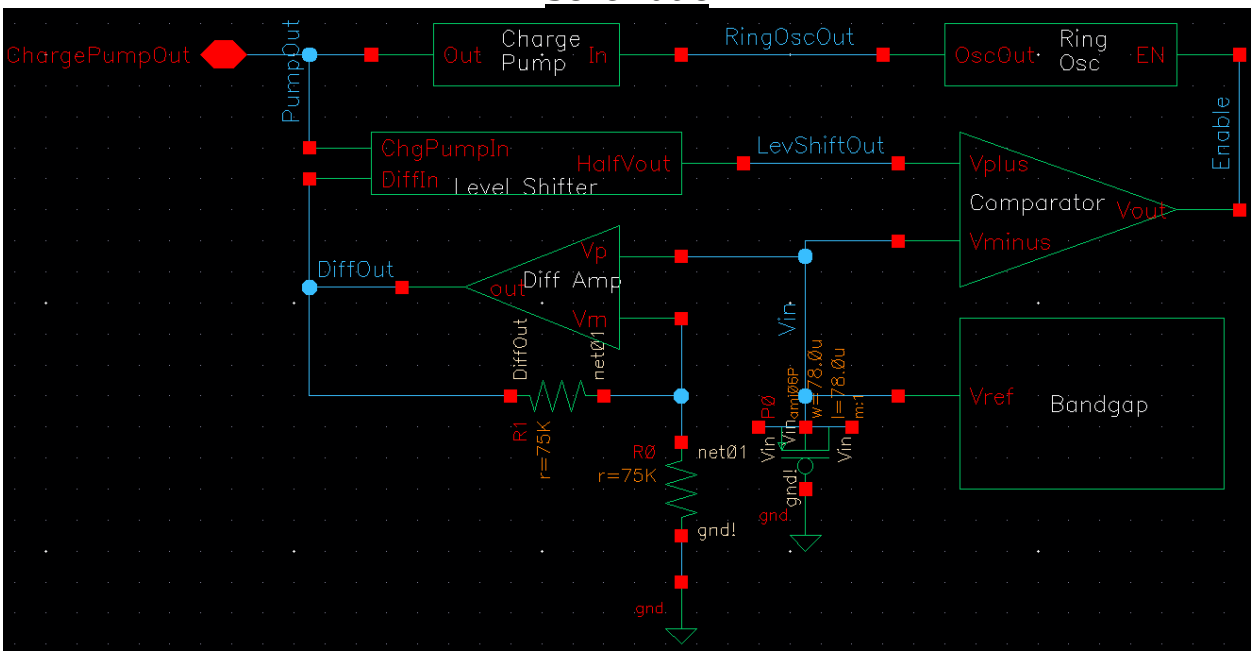
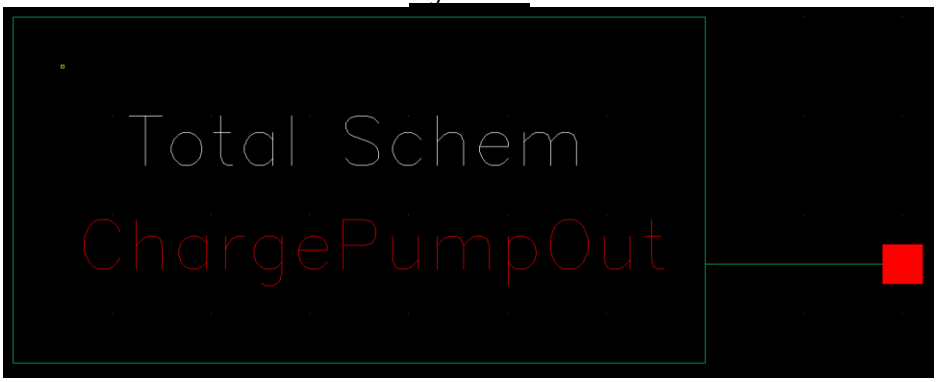
## LVS




## Schematic




## Symbol



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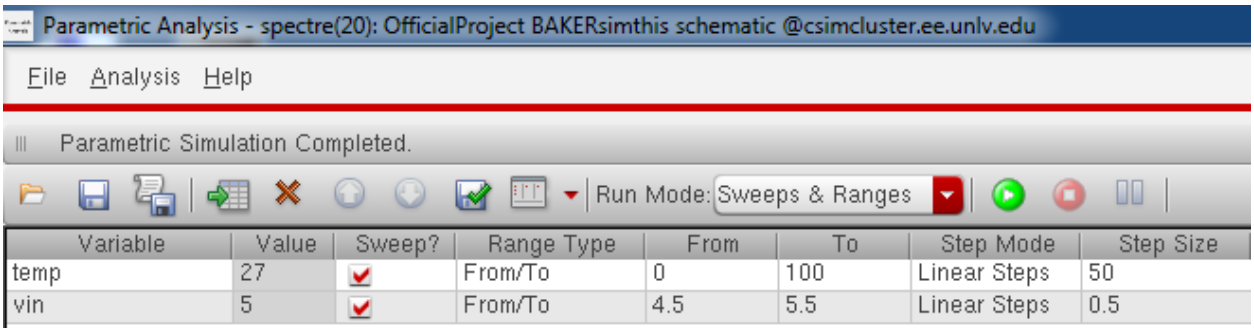
# Simulation

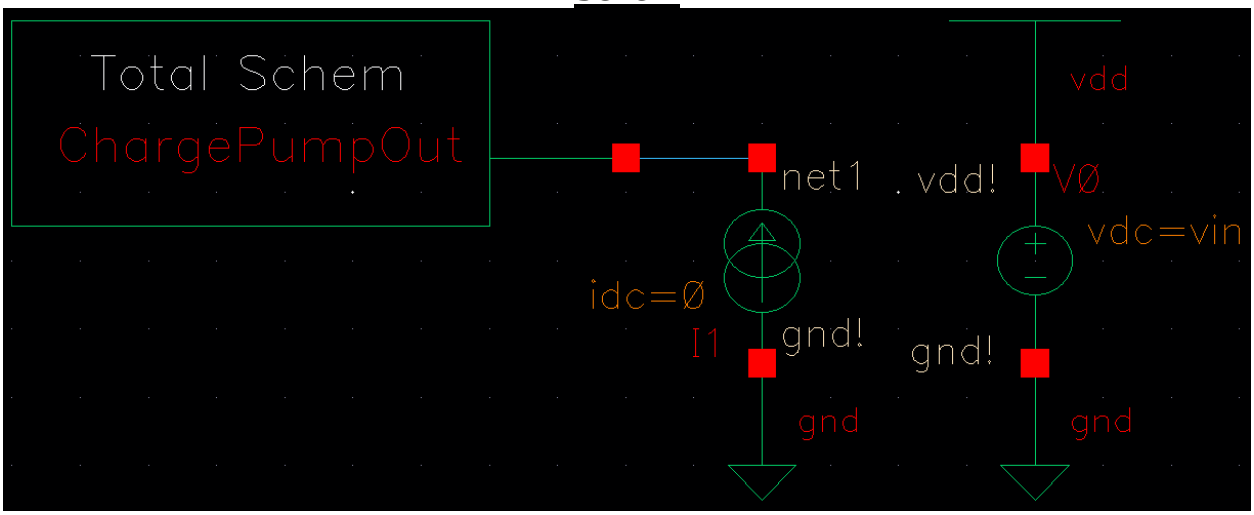
Sweeping temperature from 0 to 100C & Sweeping VDD=Vin from 4.5 to 5.5V




| Variable | Value | Sweep? | Range Type | From | To | Step Mode | Step Size |
|---|---|---|---|---|---|---|---|
| temp | 27 | ☑ | From/To | 0 | 100 | Linear Steps | 50 |
| vin | 5 | ☑ | From/To | 4.5 | 5.5 | Linear Steps | 0.5 |

Idc Current source load of (I = 0uA):

**Schem**

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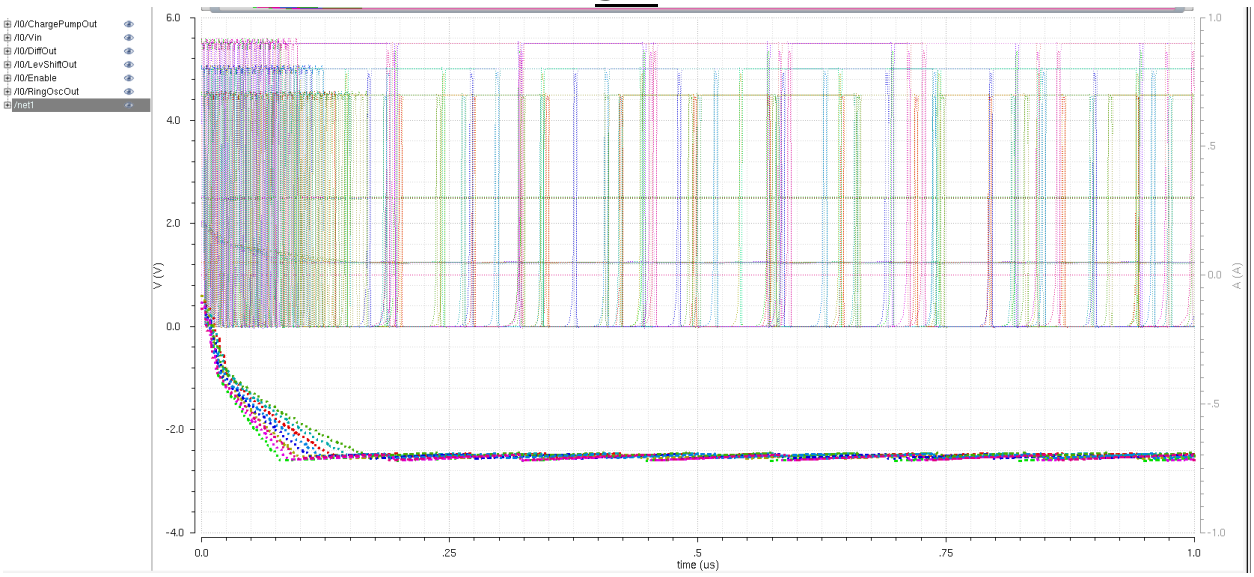

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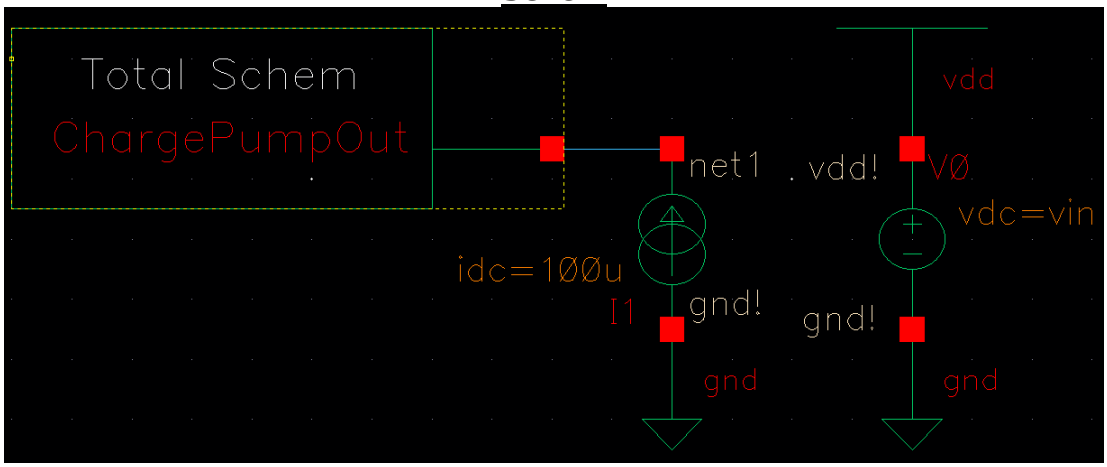
**Schem**

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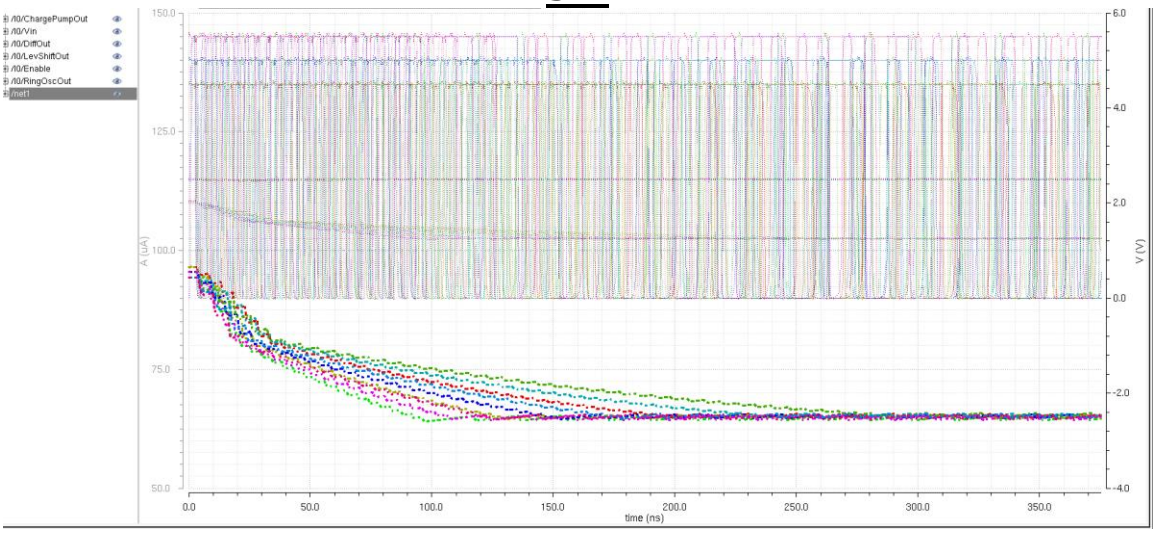


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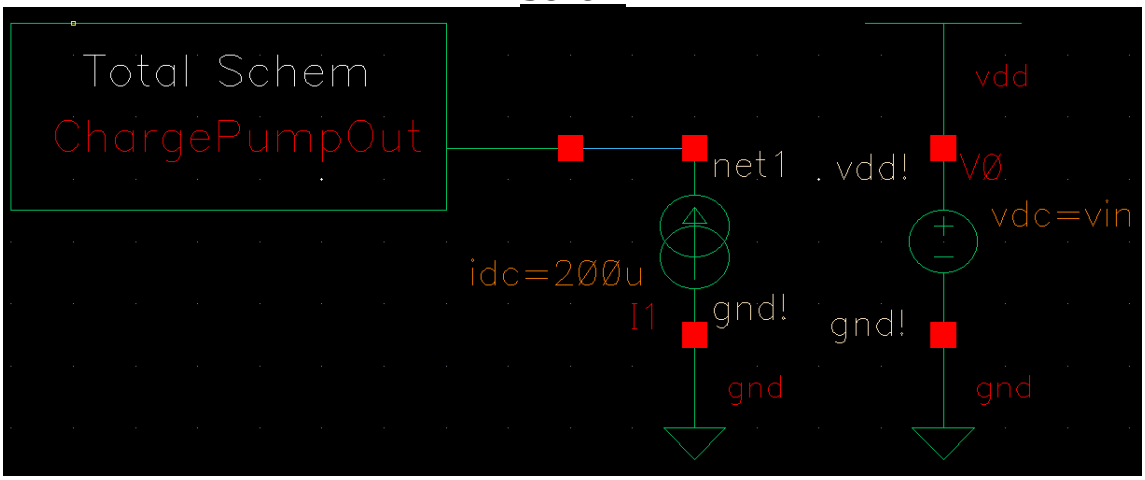
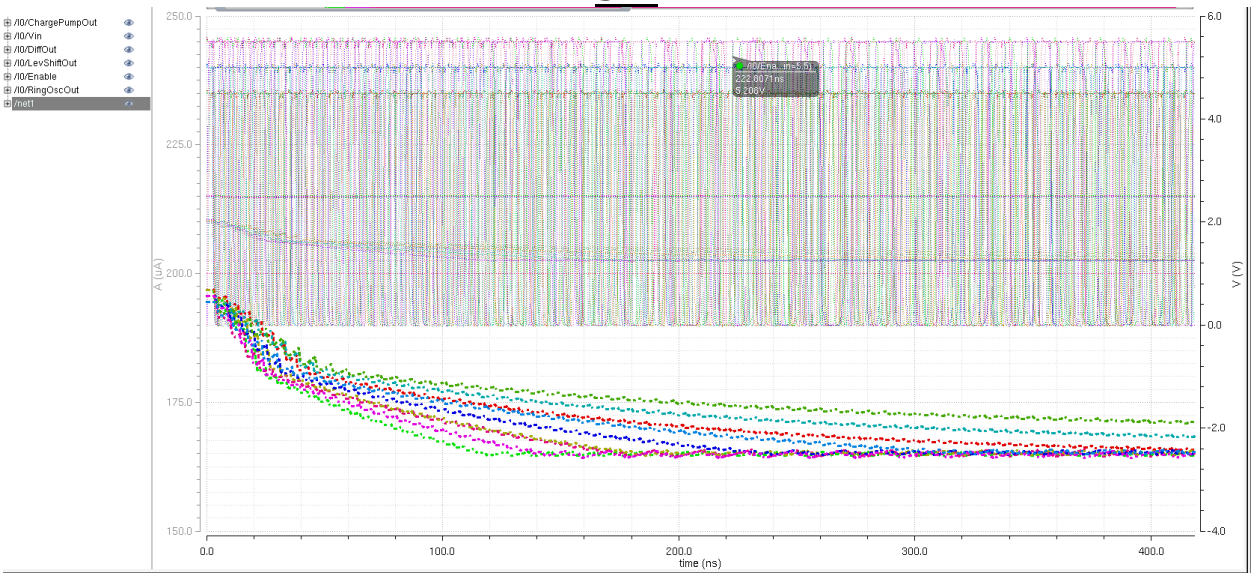
**Schem**

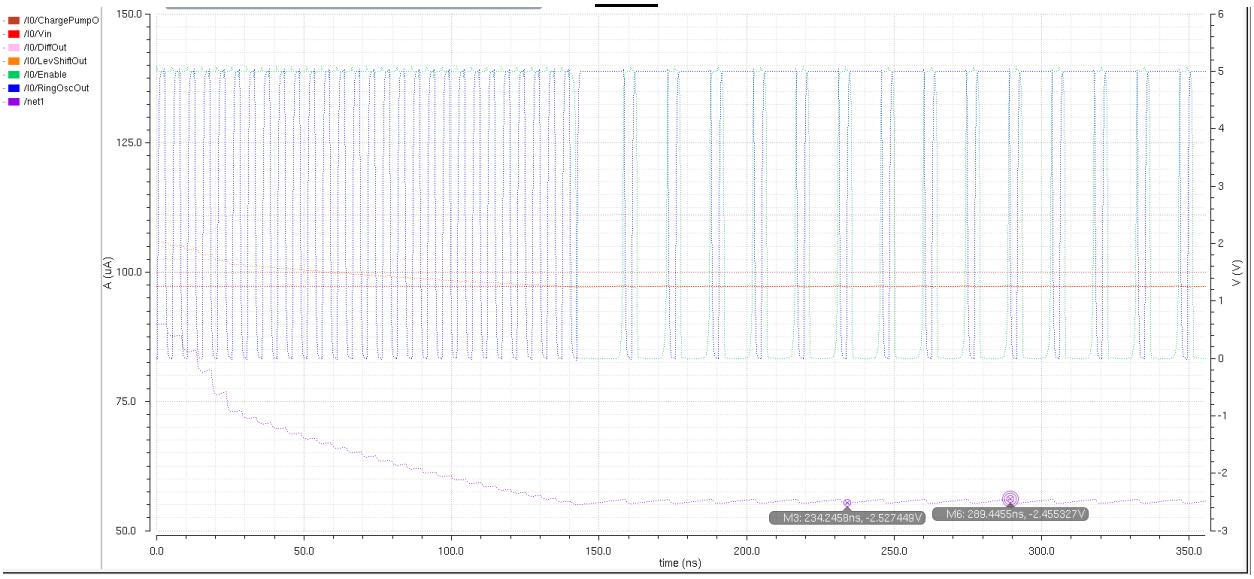


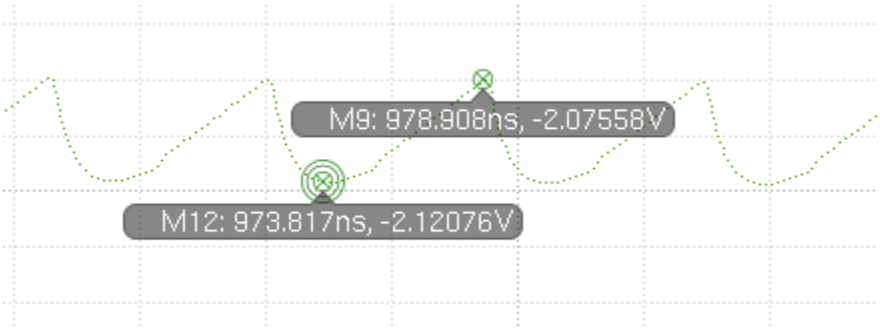
## Sim




Hysteresis

## Sim



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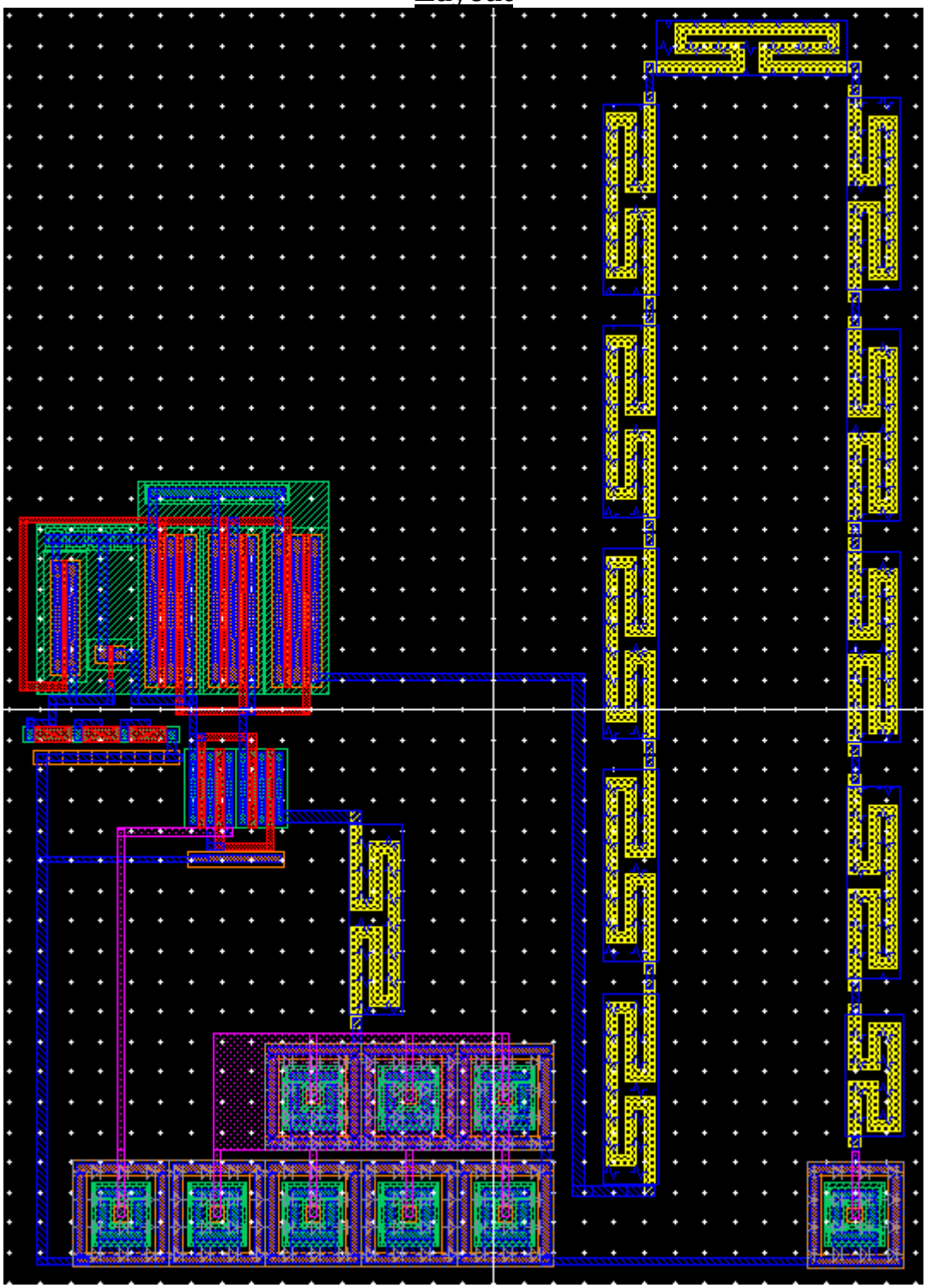
# Bandgap

## Layout



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## DRC

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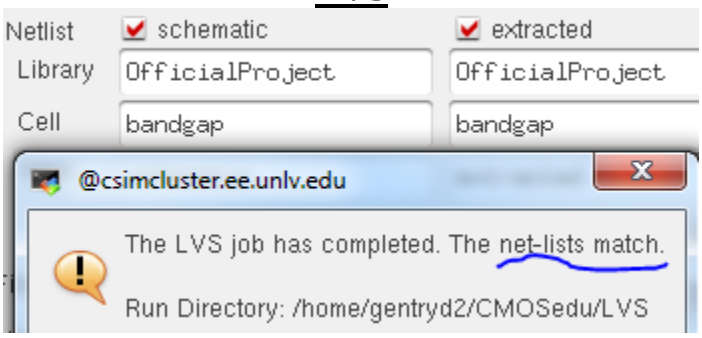
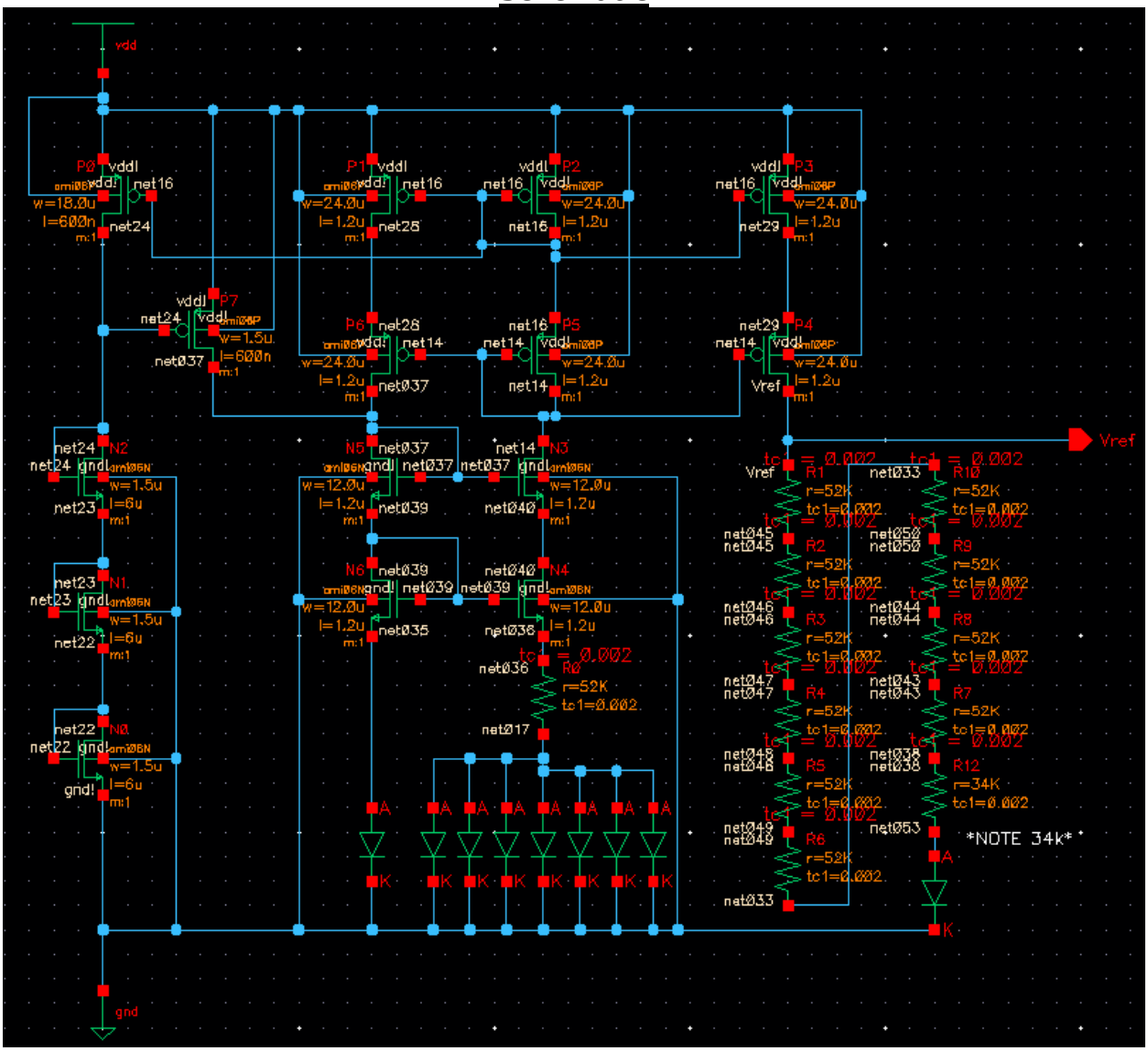
## LVS



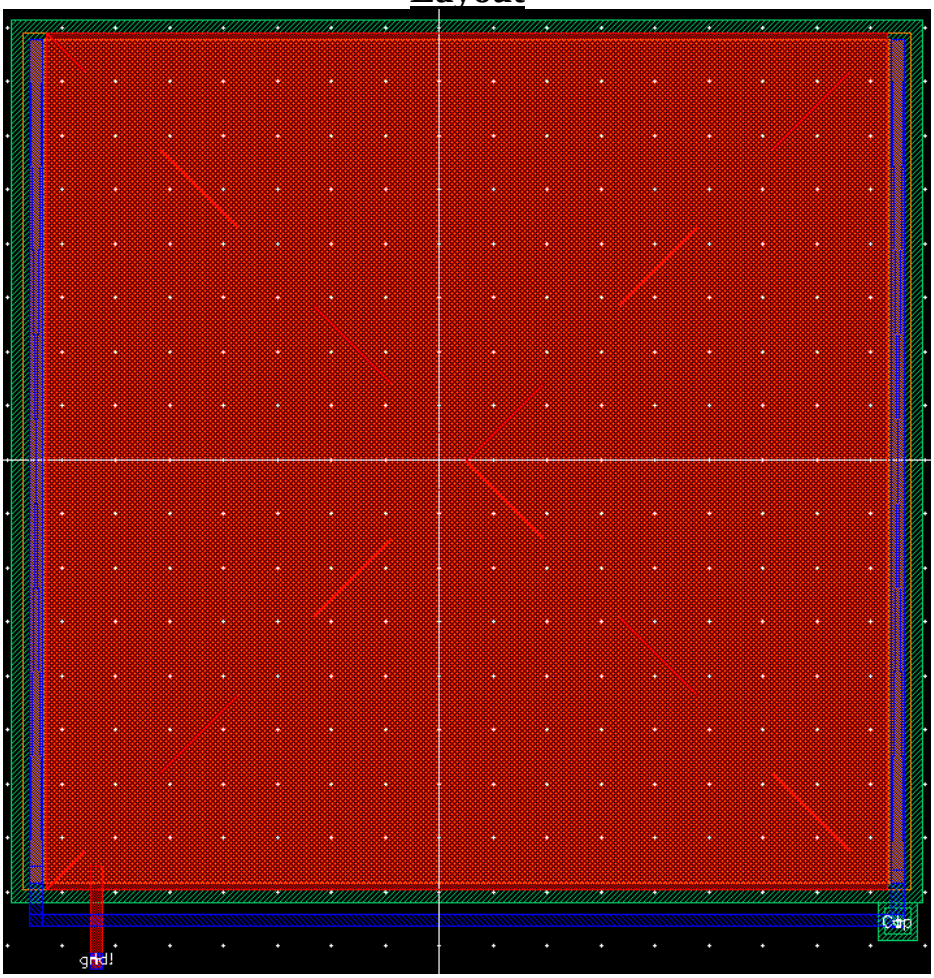

## Schematic



**Symbol**


# Decoupling Capacitor

**Layout**



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## DRC

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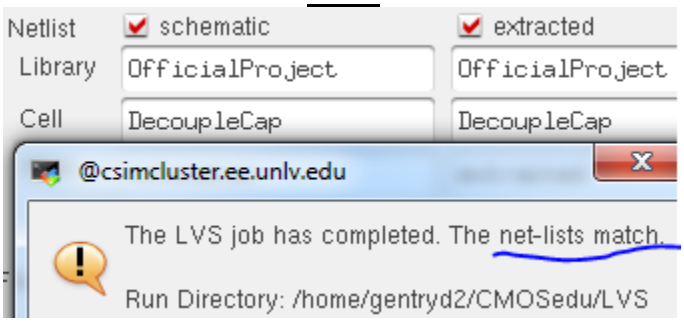
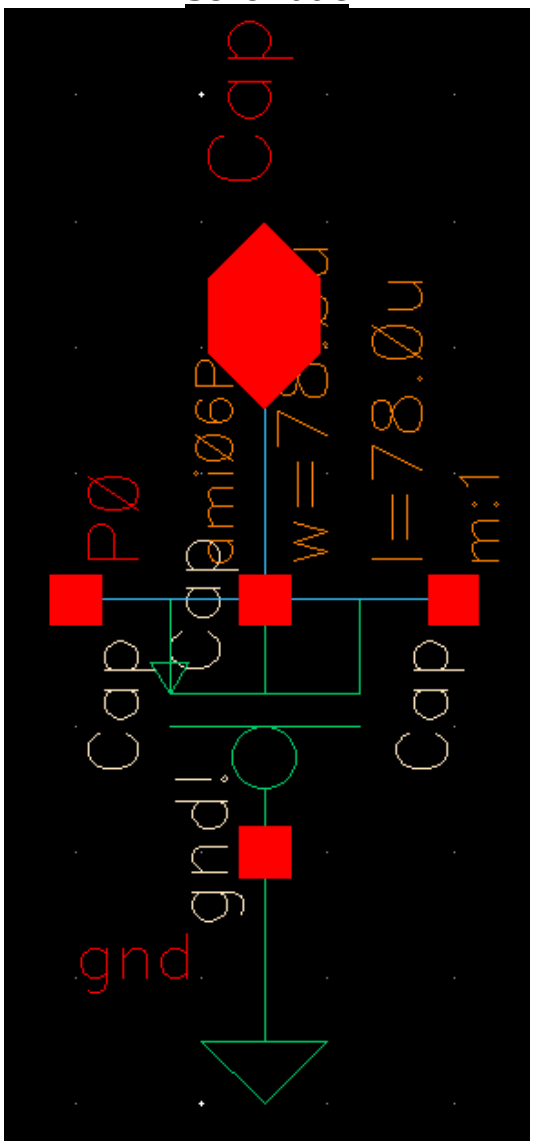
## LVS

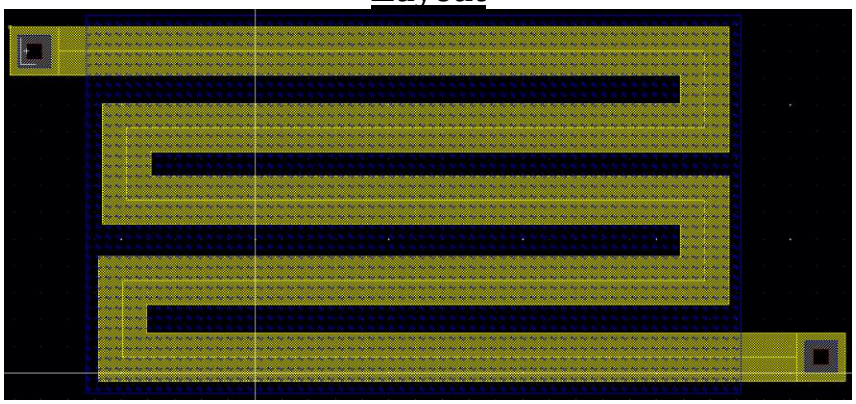



## Schematic



# Feedback Resistors

## Layout



## DRC

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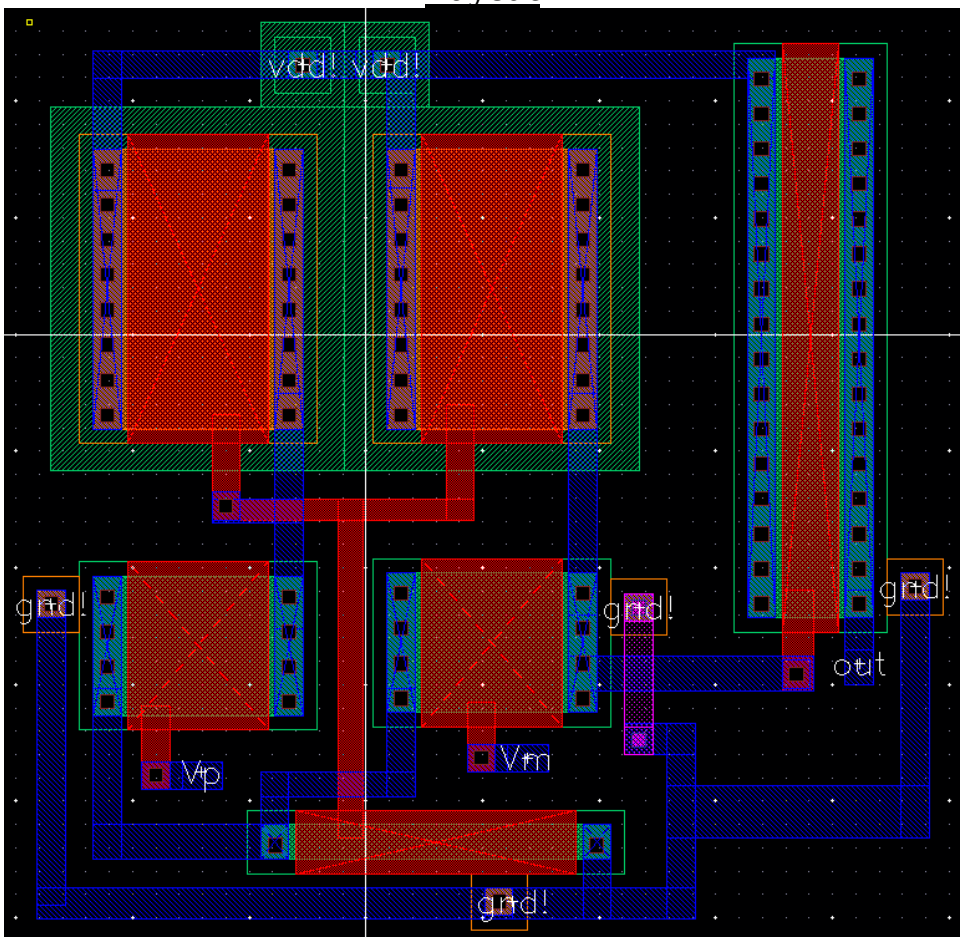
# Difference Amplifier

## Layout



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## DRC

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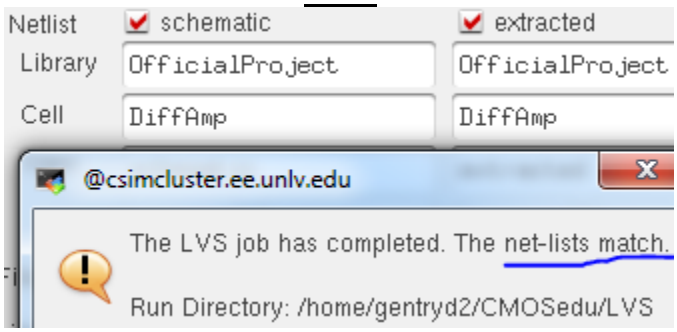
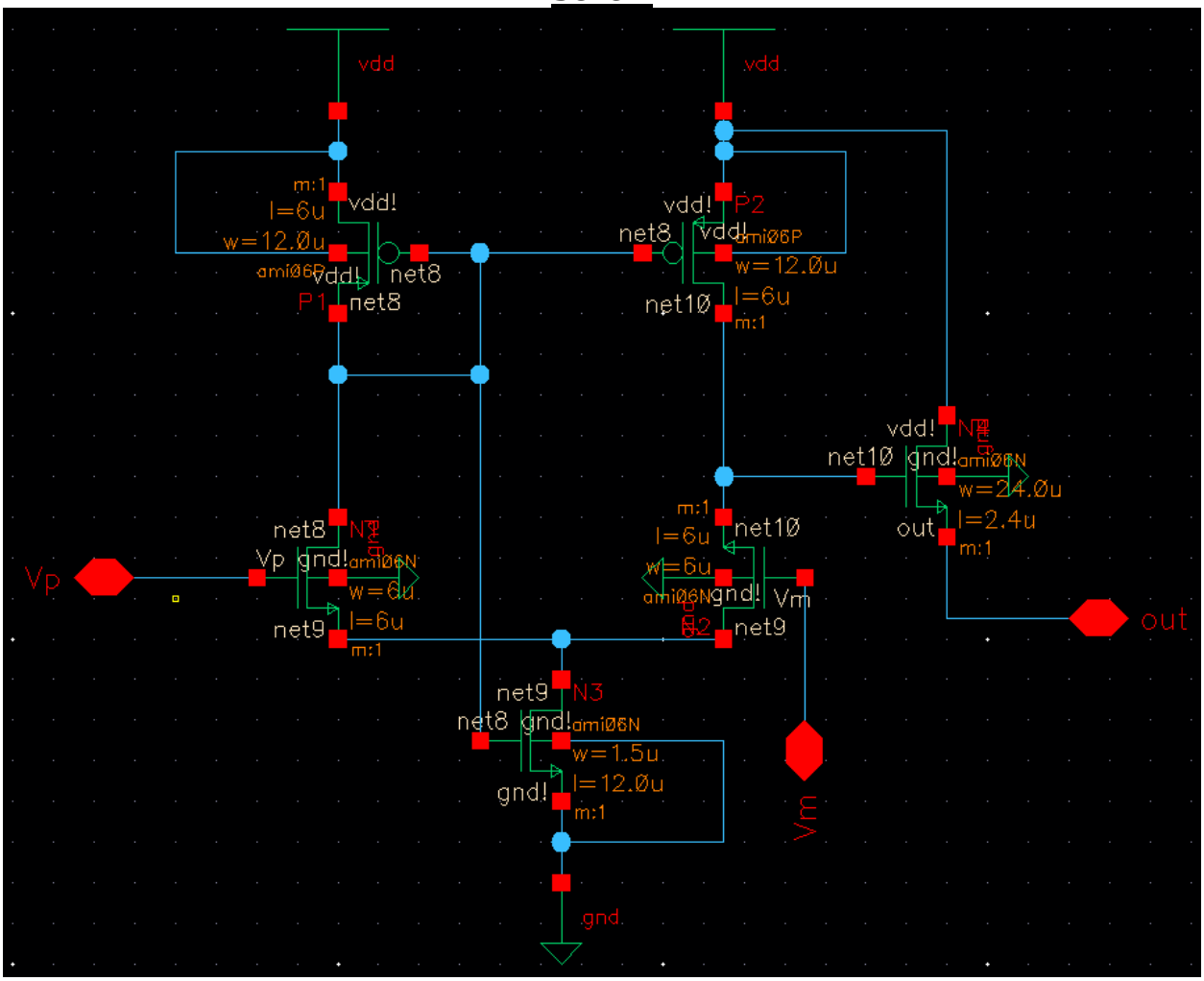
## LVS




## Schem



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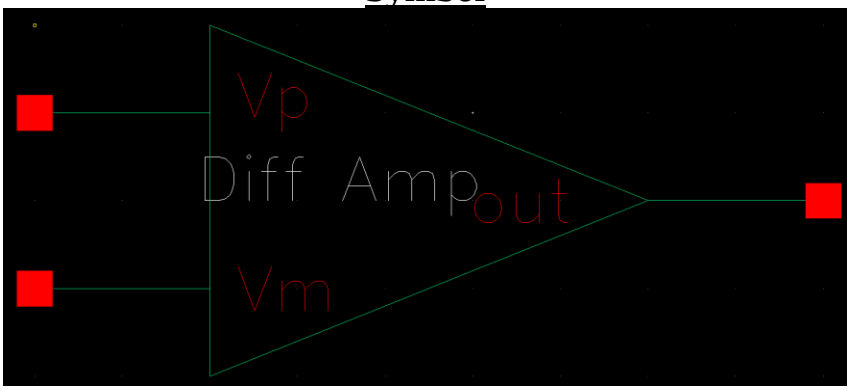
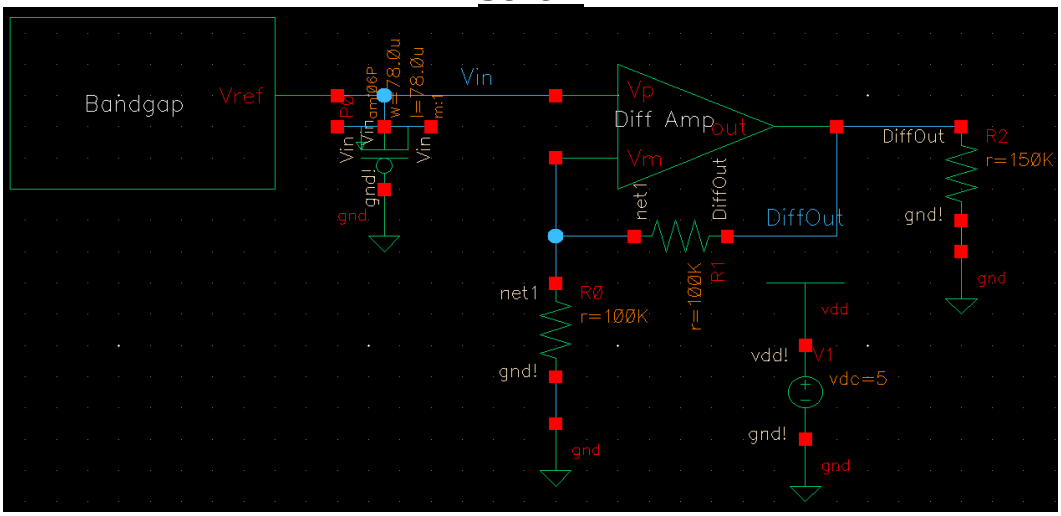
## Symbol

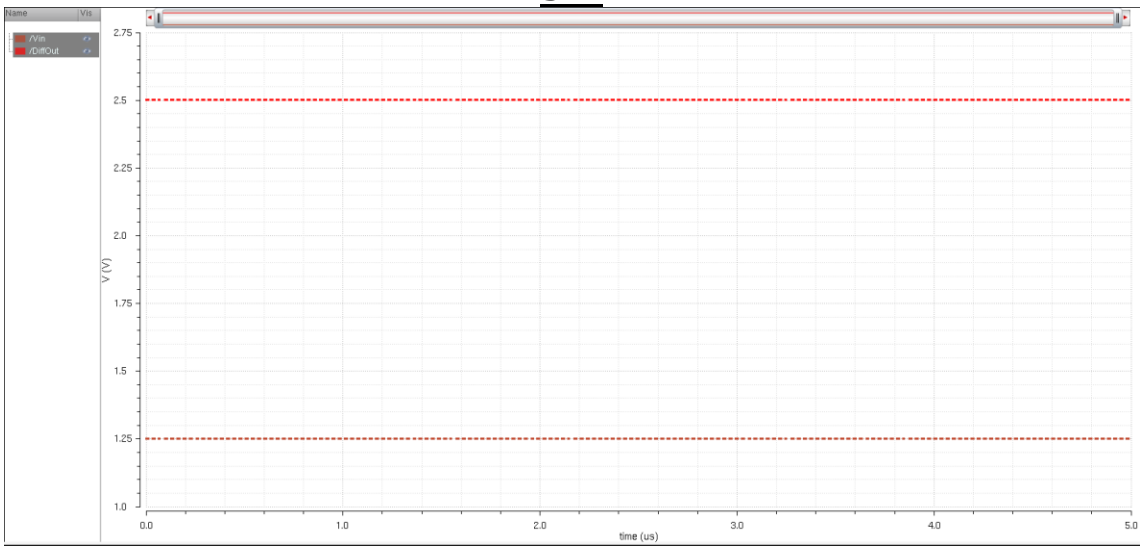



# Simulation

## Schem




## Sim



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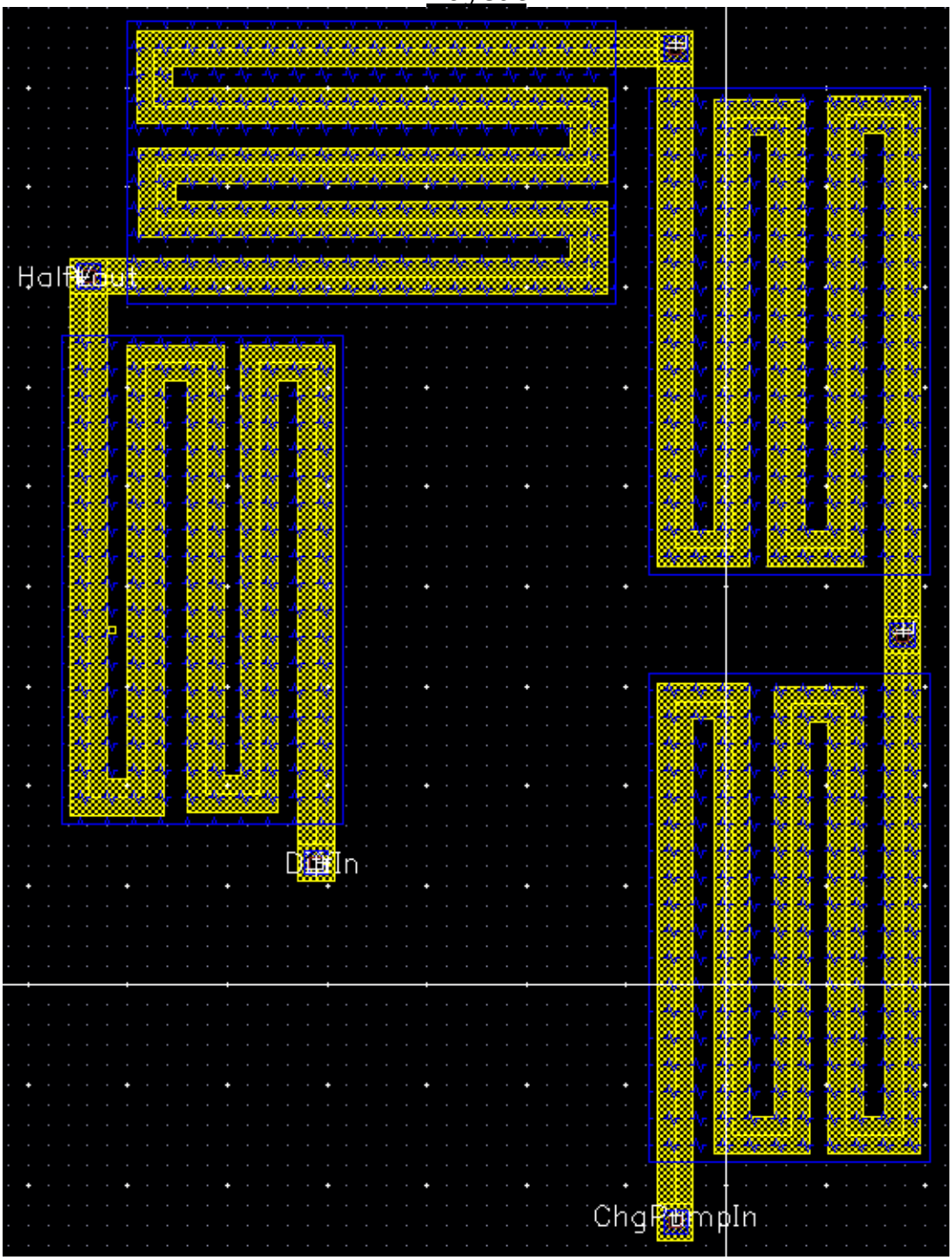
# Level Shifter

## Layout




## DRC

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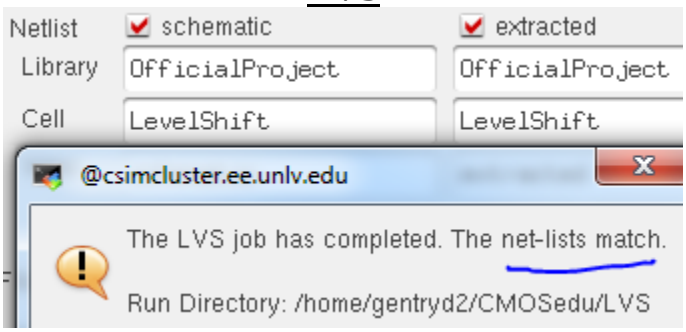
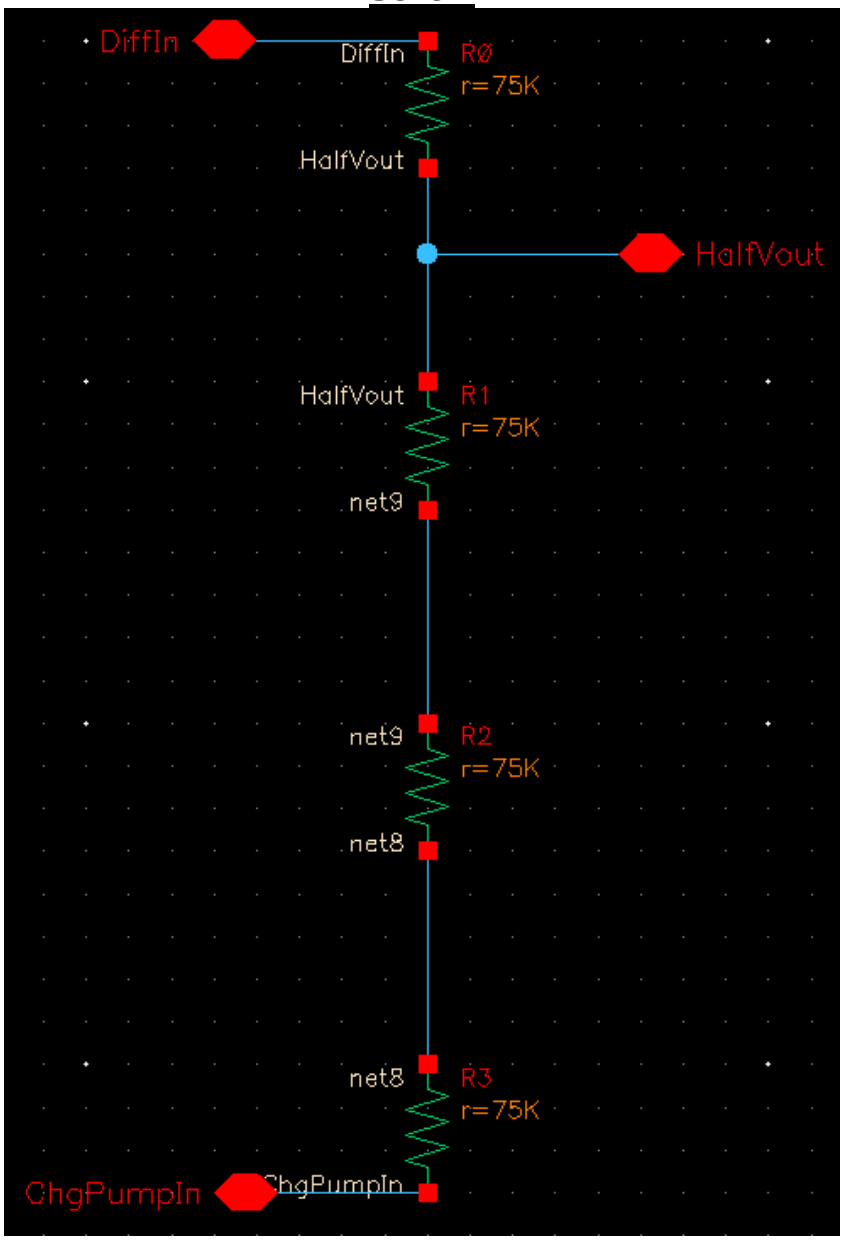
## LVS


Netlist
schematic
extracted
Library
OfficialProject
OfficialProject
Cell
LevelShift
LevelShift
@csimcluster.ee.unlv.edu
The LVS job has completed. The net-lists match.
Run Directory: /home/gentryd2/CMOSedu/LVS

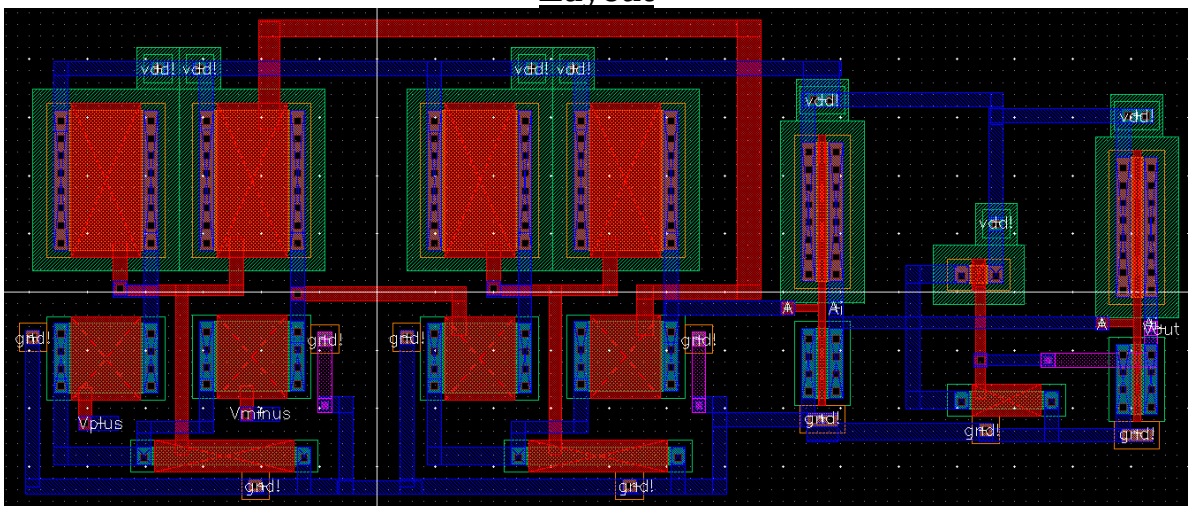
## Schem


DiffIn
DiffIn
R0
r=75K
HalfVout
HalfVout
HalfVout
R1
r=75K
net9
net9
R2
r=75K
net8
net8
R3
r=75K
ChgPumpIn
ChgPumpIn

**Symbol**


# Comparator

**Layout**




**DRC**

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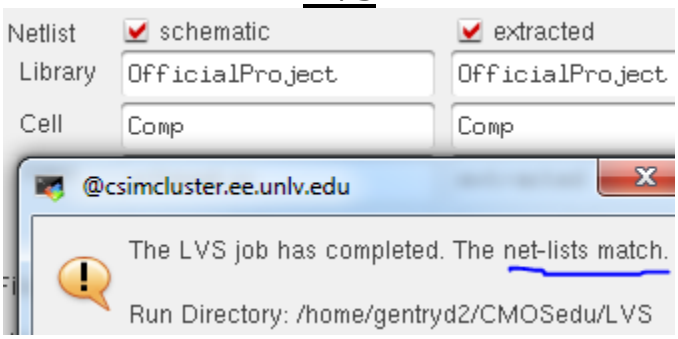
**LVS**



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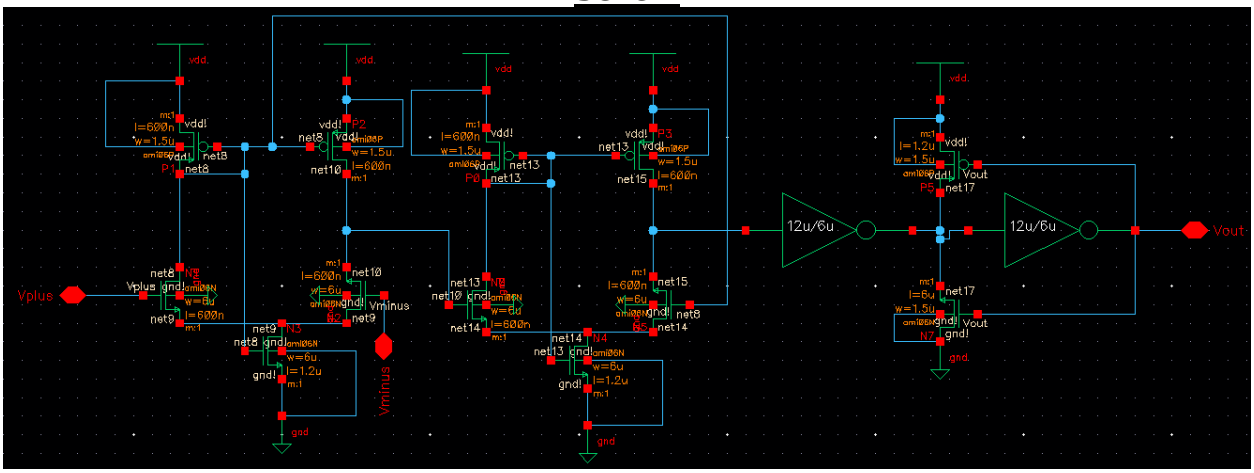
## Schem

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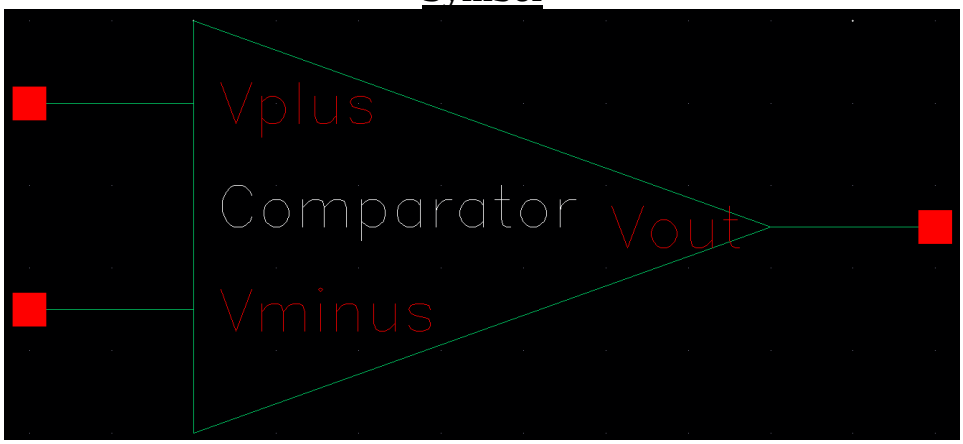
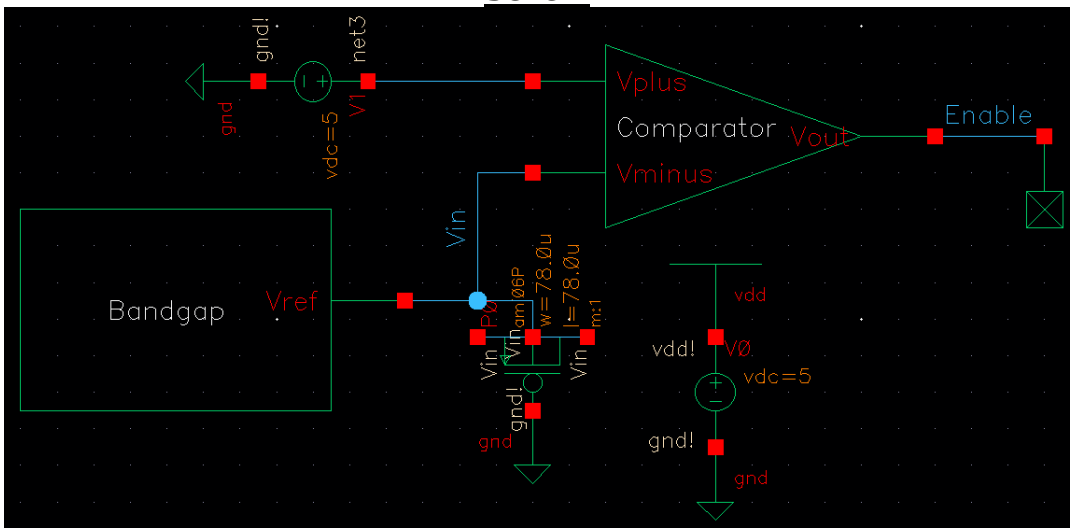
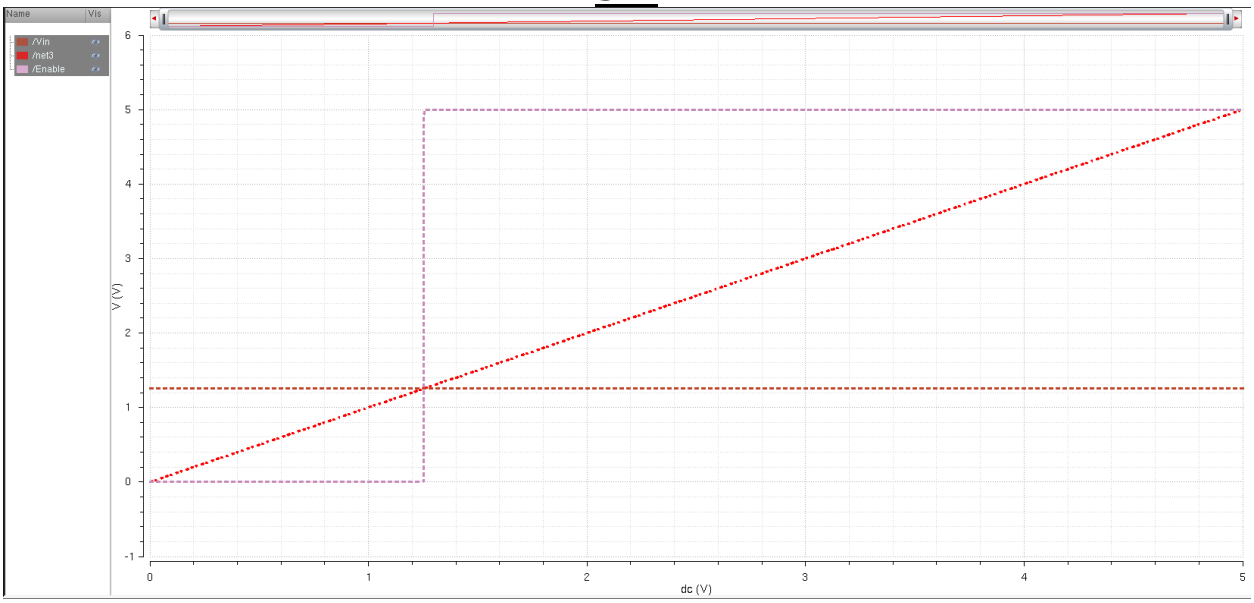



# Simulation

## Schem

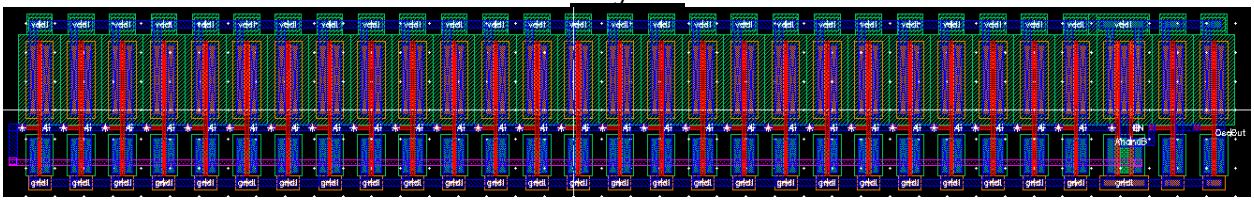


## Sim




# Ring Oscillator w/ Buffer

## Layout



## DRC

```
******   Summary of rule violations for cell "RingOscBuffer layout"
Total errors found: 0
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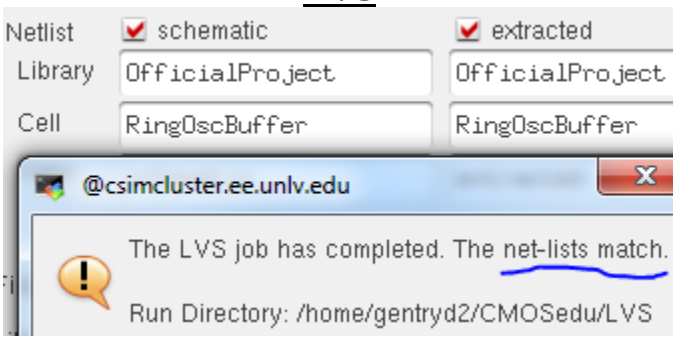
## LVS



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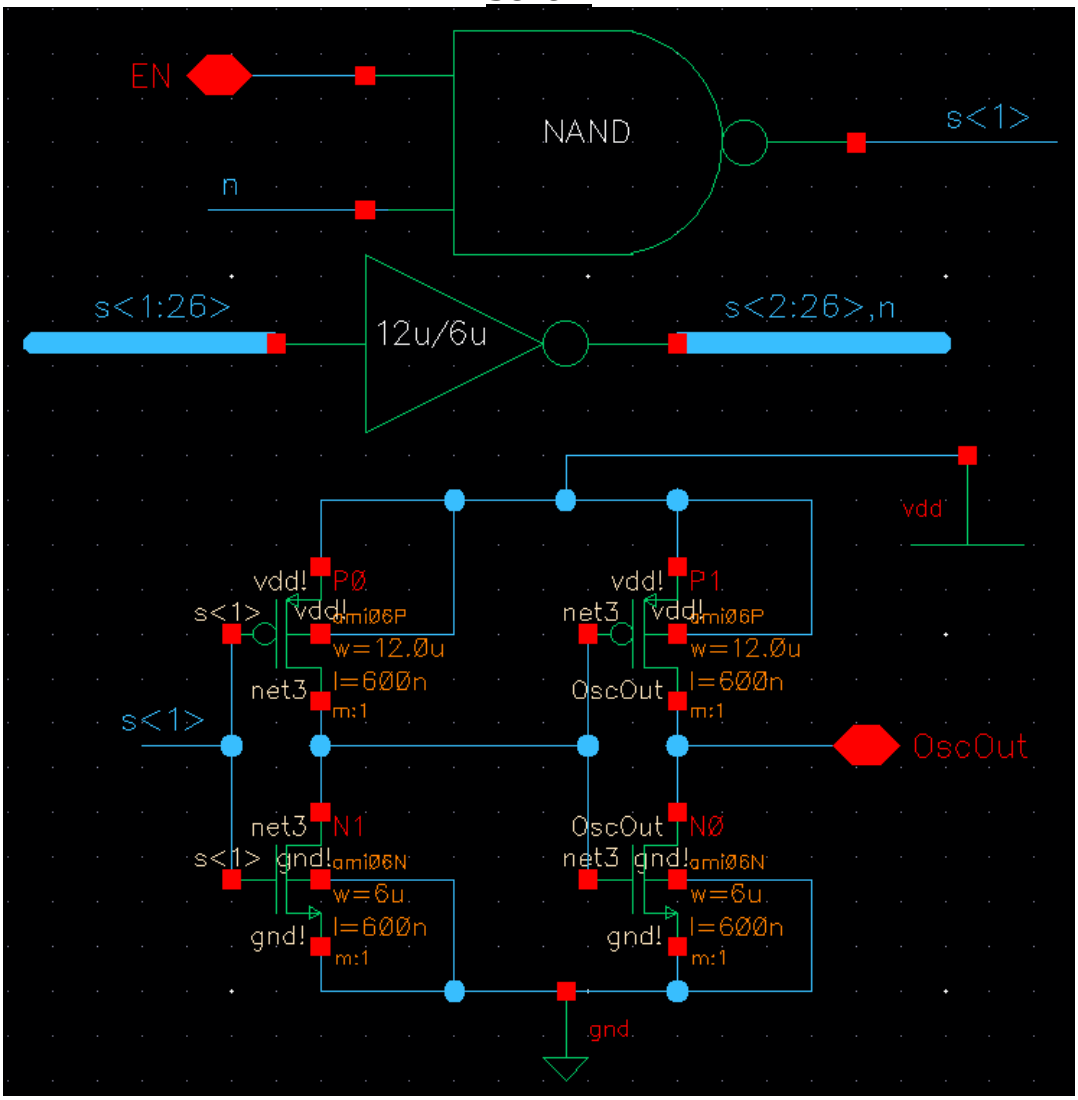
## Schem




## Symbol


Determination of number of stages to be used in Ring Oscillator in addition to the 2 inverter buffer and nand gate.

22 stages ➔ freq. = 229MHz

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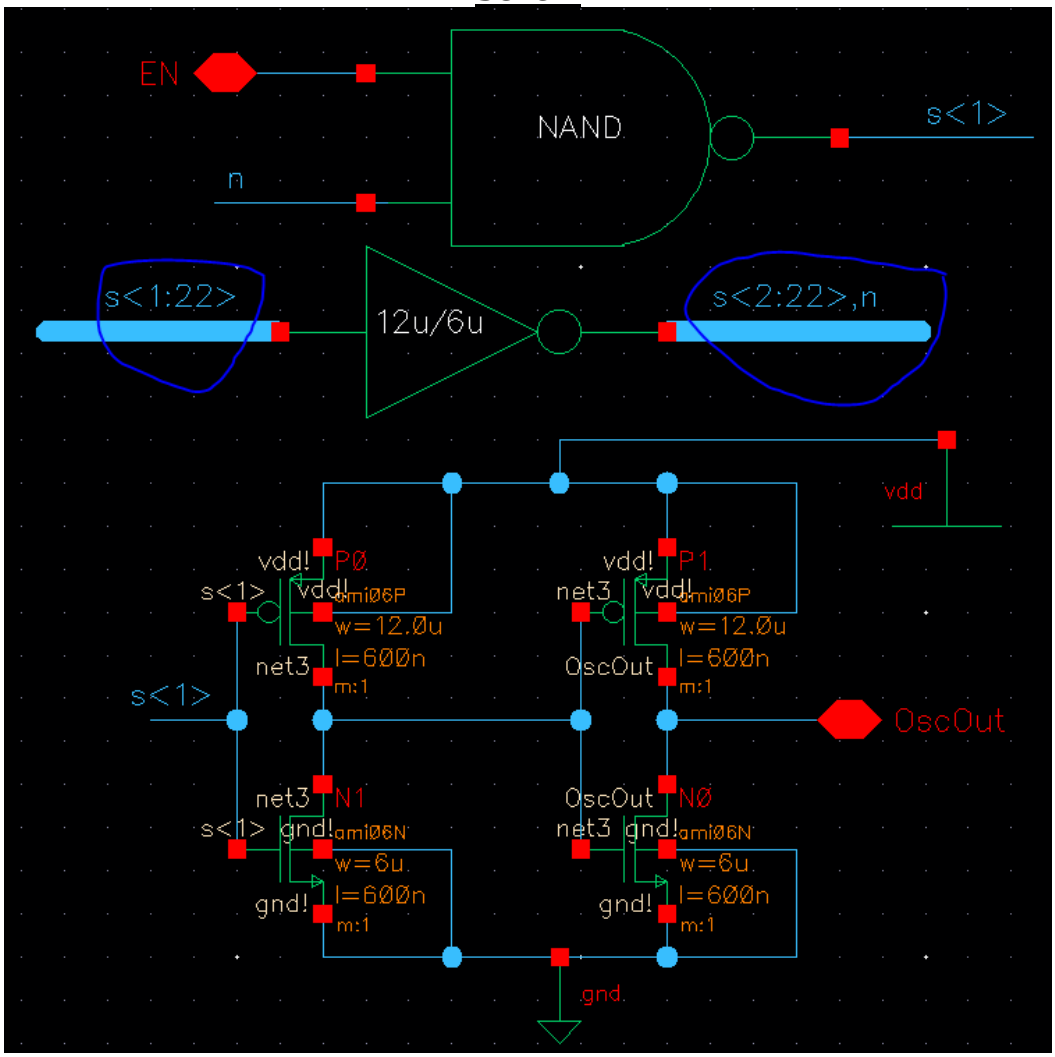
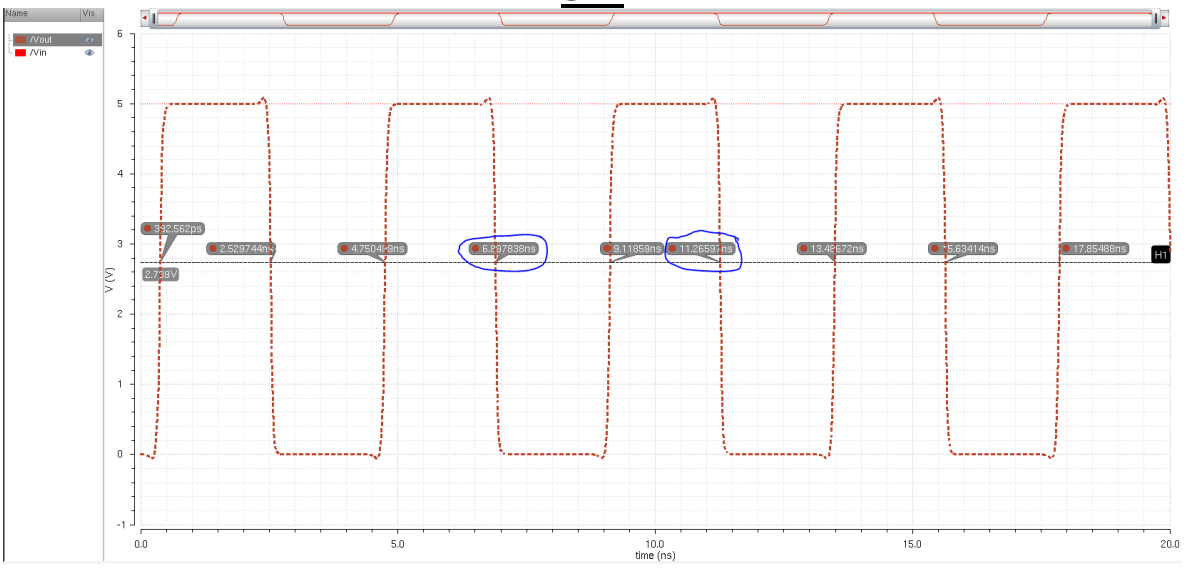
## Schem




## Sim

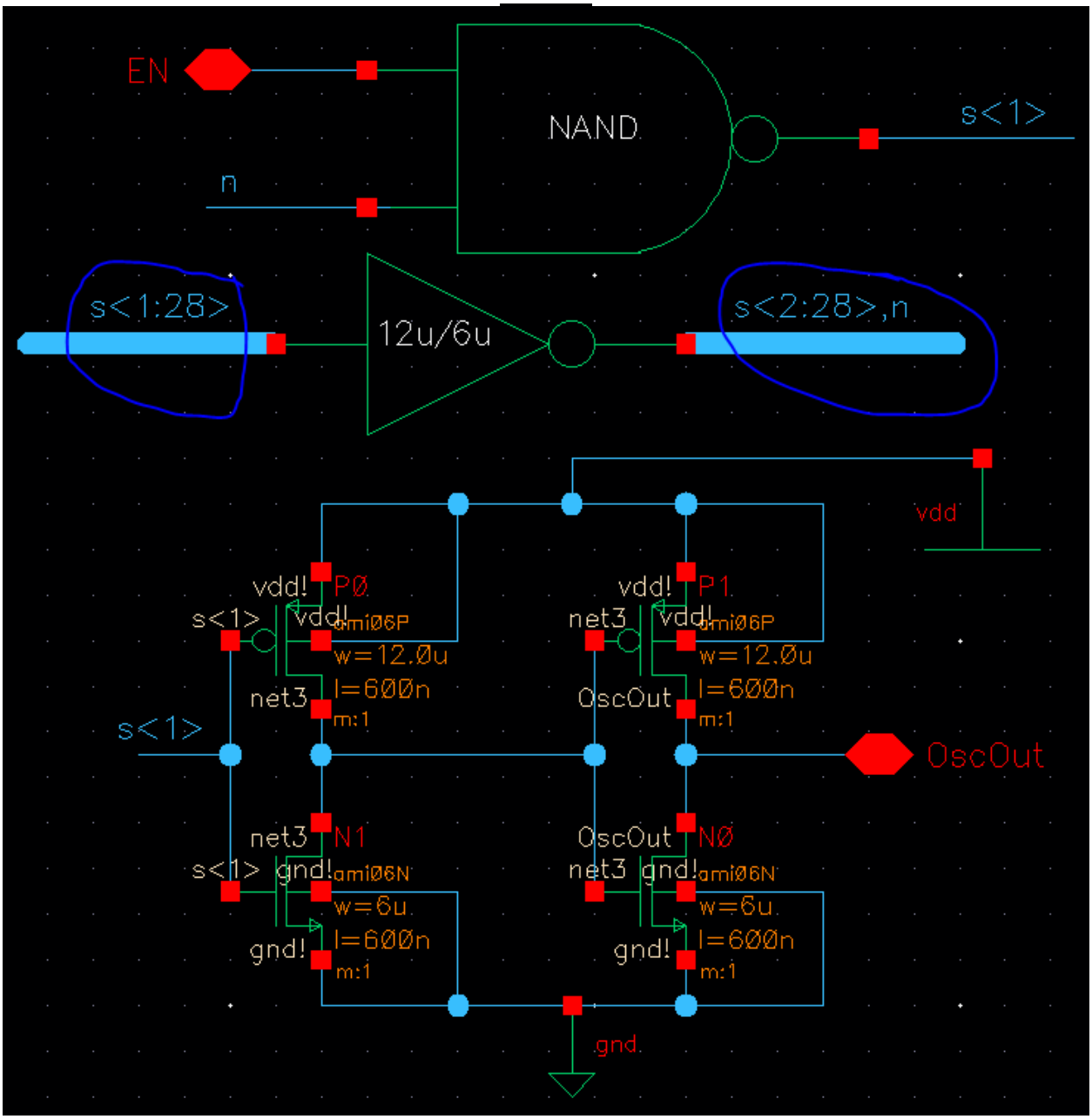


Freq. = 1/Period = 1/(11.26597-6.897838)ns = 229 MHz

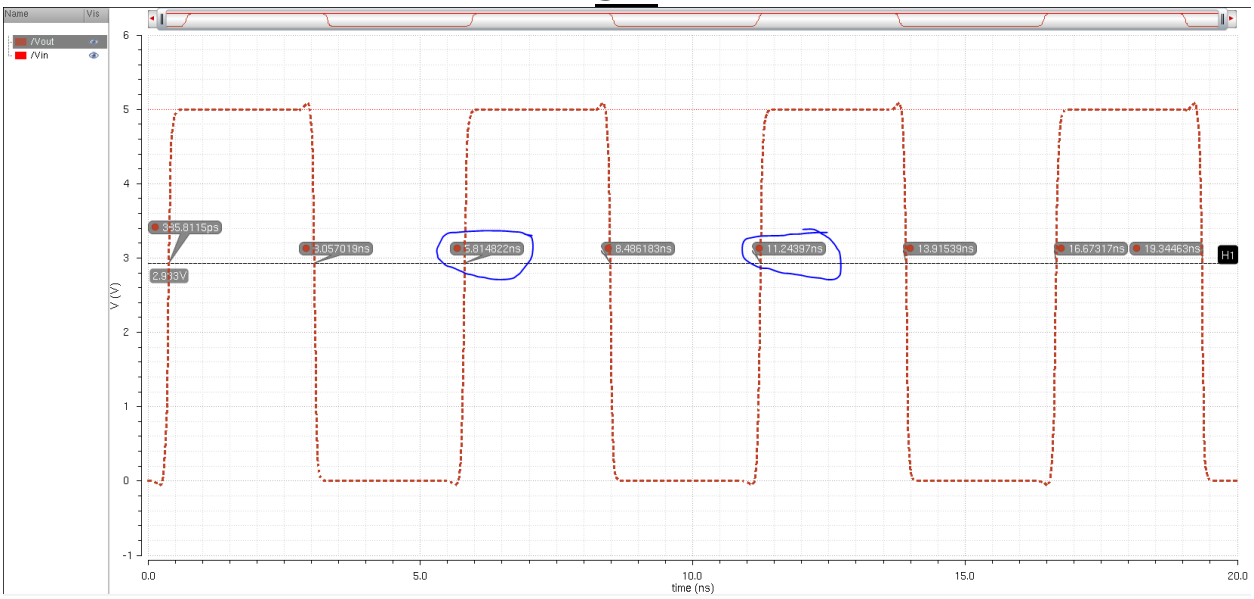
229 MHz is too fast. I'm shooting for 200MHz. This prompted me to increase the number of stages to 28 stages in order to increase delay and slow down the frequency.

28 stages ➔ freq. = 184MHz

## Schem



# Sim




Freq. = 1/Period = 1/(11.24397-5.814822)ns = 184 MHz

Given: 22 stages ➔ 229 MHz & 28 stages ➔ 184 MHz

Calculated: (229-184)MHz/(28-22)stages = 7.5 MHz/stage

This gives that 26 stages will yield a oscillation frequency of 197 MHz

26 ➔ 197MHz

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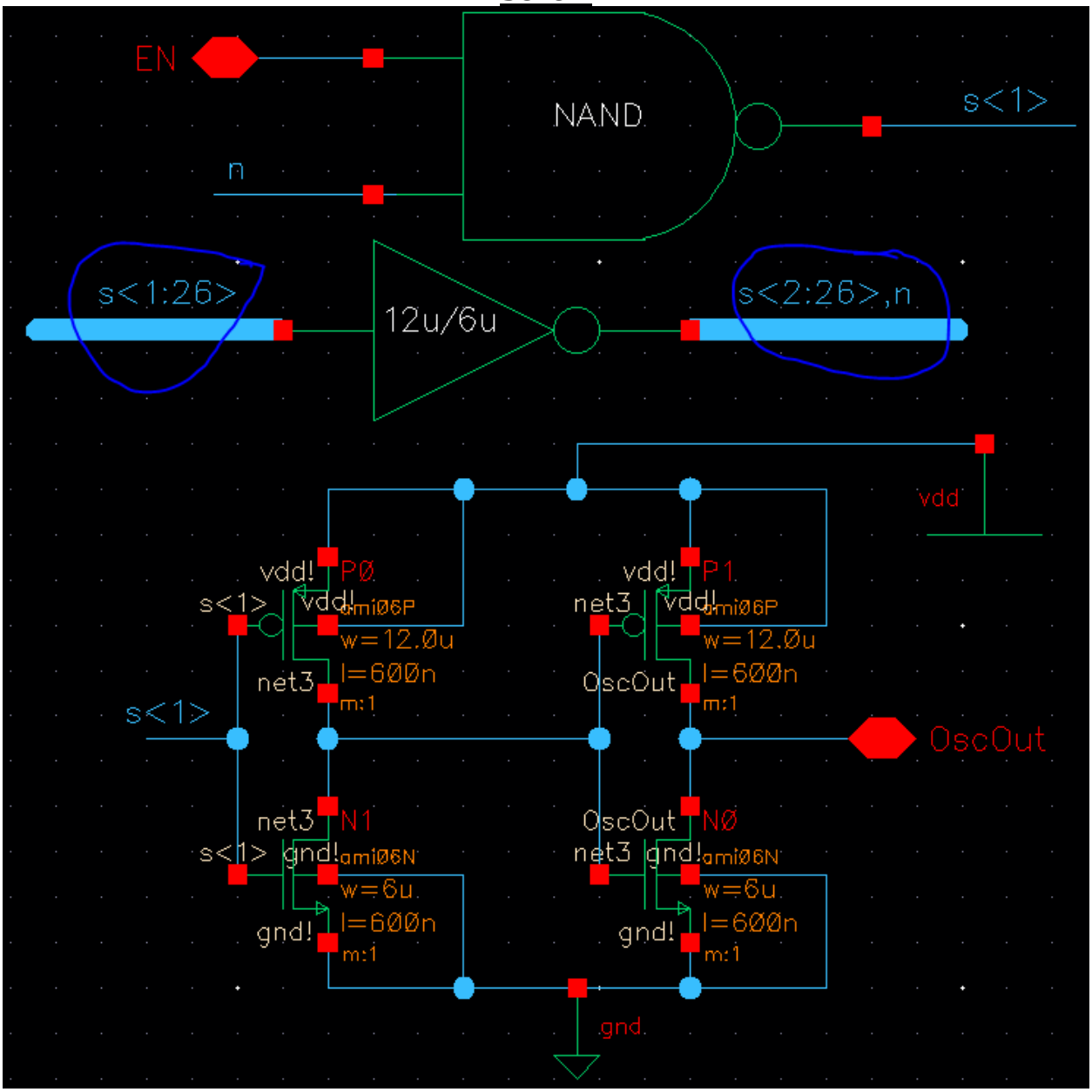
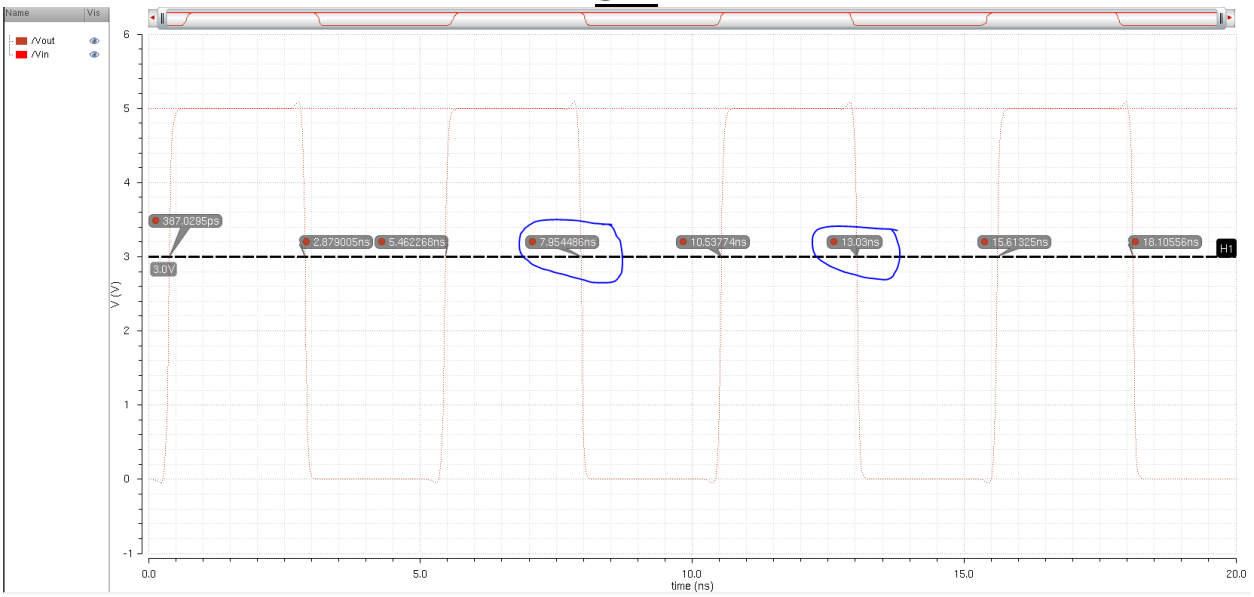
**Schem**

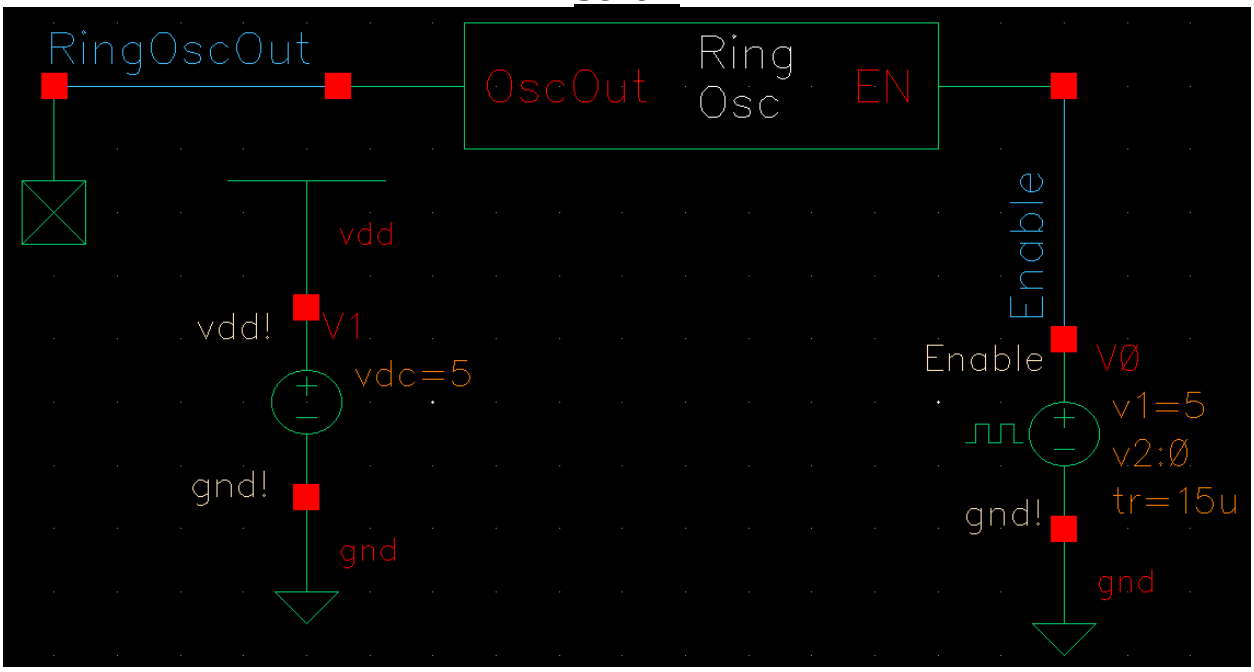


## Sim

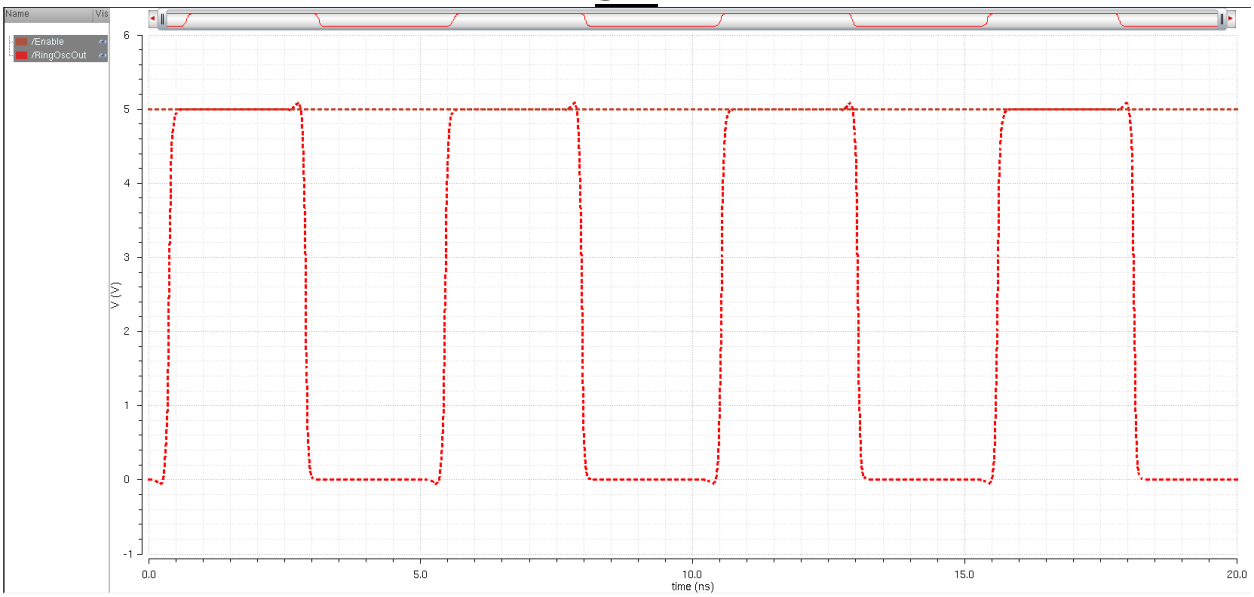



# Simulation

## Schem

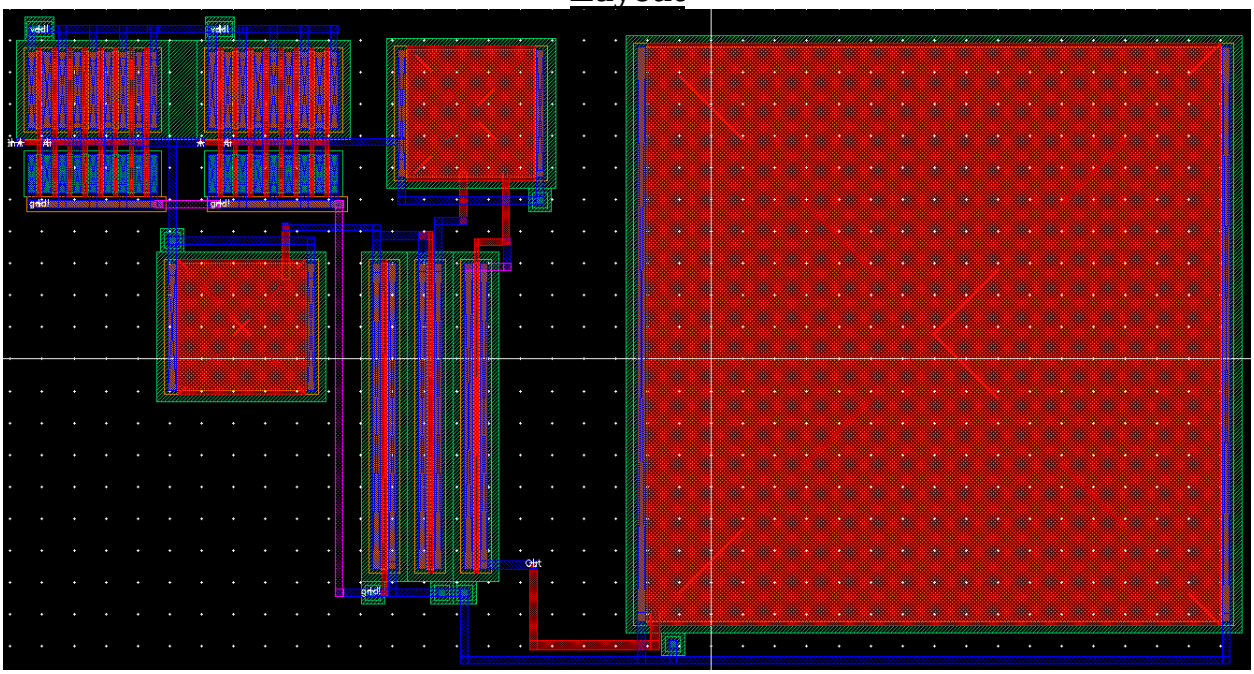


## Sim




# Negative Charge Pump

## Layout




## DRC

```
******  Summary of rule violations for cell "ChgPump layout"
Total errors found: 0
```

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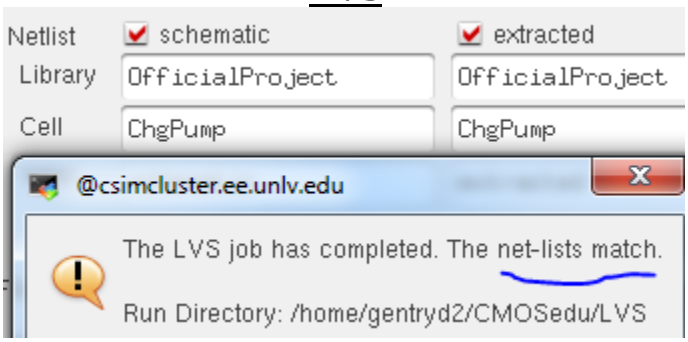
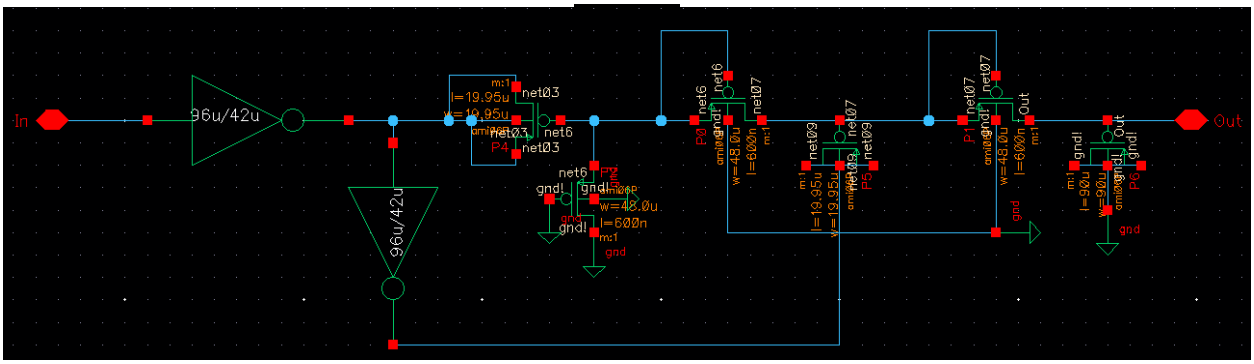
# LVS




# Schem



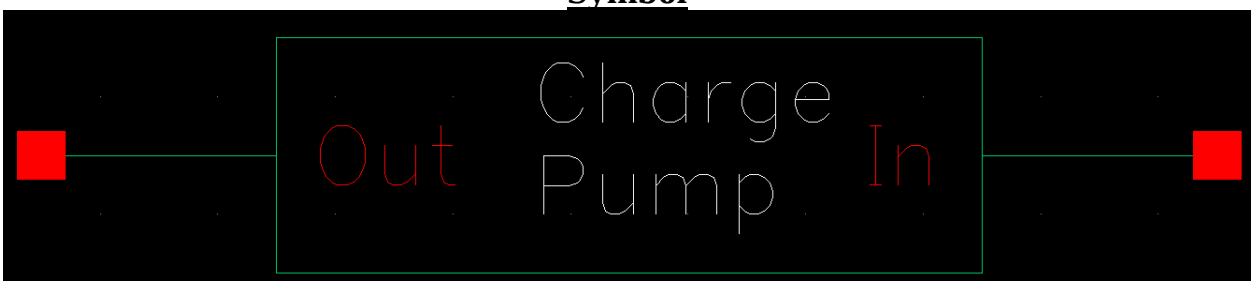

For the charge pump schematic, I wanted 15pF capacitors, so I sized the pmos capacitors using:

$$C = 2.5fF/um^2 * L * W$$

I decided to have my length equal width which yielded:

$$15pF = 2.5fF/um^2 * L * W \rightarrow L=W=20u$$

# Symbol



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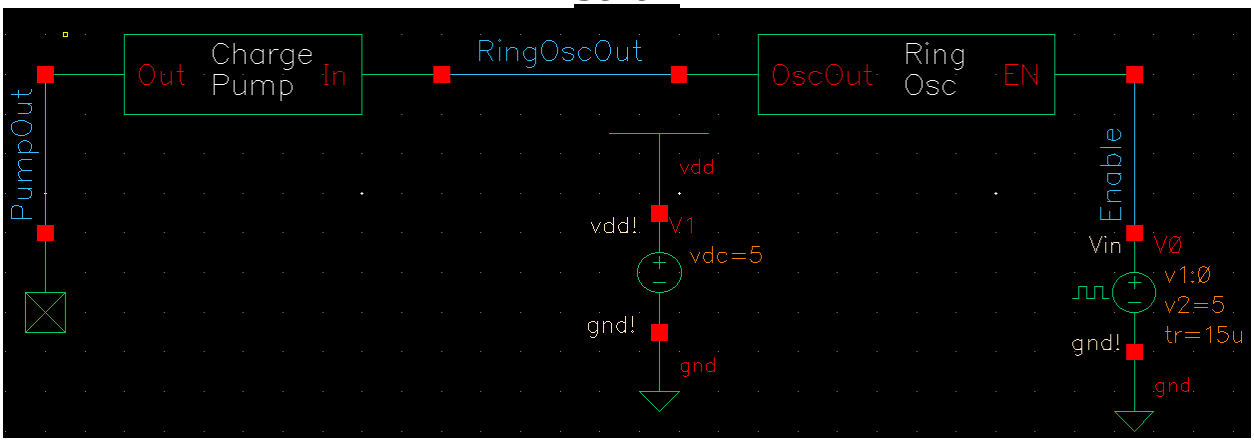
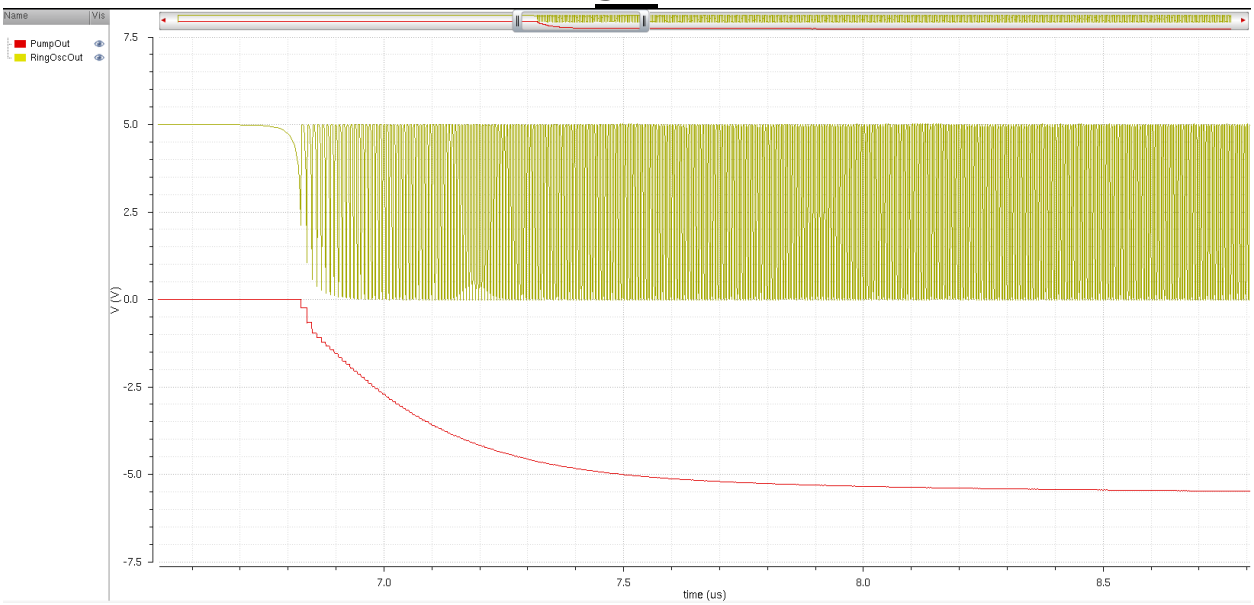
# Simulation

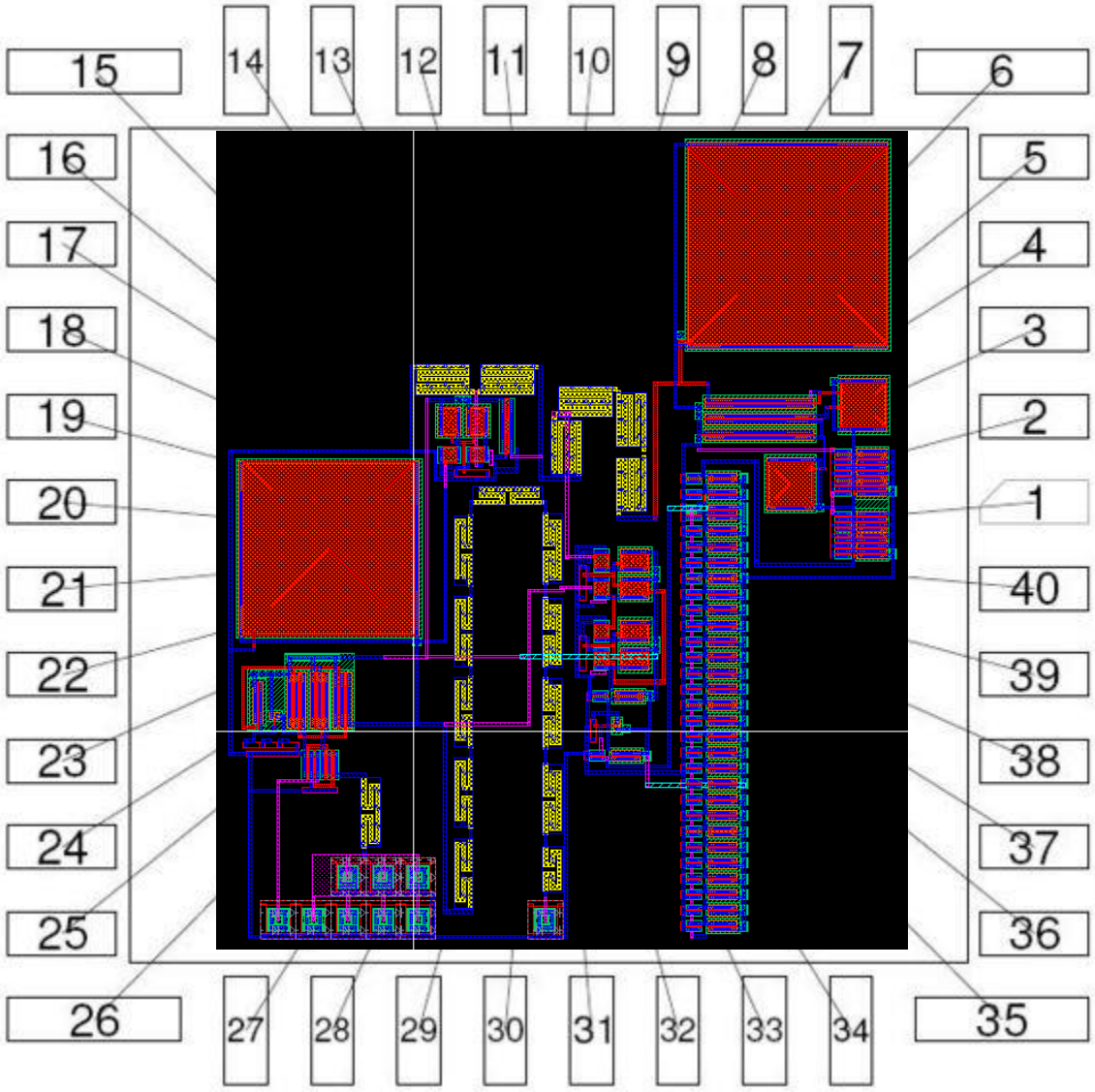
## Schem




## Sim



# Pin Diagram




For the above pin diagram, I would connect my GND to pin 1, my VDD to pin 2, and my bandgap out pin to pin 3.

To calculate power efficiency, I would average the current over the time of one period. Unfortunately, I did not simulate this.

# Conclusion

The overall charge pump design and layout perform considerably well. All layouts yield no DRC errors as well as successful LVS, and, in addition, a pin diagram for the design's layout has been provided so that the layout could potentially be connected to bond pads and the design fabricated. I encountered numerous issues throughout the project including designing the overall charge pump to meet all the design requirements and perform as well as possible, and Cadence presented a great deal of various problems especially in referencing the model library for the diodes used in the bandgap. This issue was especially apparent because the bandgap that was initially provided to us had to be changed due to sizing oversights on a few PMOS. This led to multiple occurences of the parasitic pnp diode model library, but after much time and frustration, I was able to get my bandgap and all associated cells to LVS successfully. Despite any setbacks, all issues were overcome with time and yielded a better knowledge of Cadence and circuit design in general. Having successfully completed this course project has certainly resulted in my becoming a more confident and experienced circuit designer as well as engineer.