Forward

Dr. Baker:

The zipped filed I sent you is titled “Final Project” and has two different designs in it titled “Design 1” and “Design 2”. I included both designs because my first design “Design 1” seems to have better overall performance, but I had spent so much time troubleshooting “Design 2” that I figured I would include it. I hope this clearly allows you to simulate my project without any difficulties, and I would like to thank you for yet another wonderful semester and learning

Introduction

The objective of this course project is to use On’s C5 process to design a voltage follower using an op-amp that can operate with a VDD between 3V and 5V while driving a 10pF (max) and 1kΩ (min) load. The input voltage should be connected to the noninverting "+" input of the op-amp and the output voltage connected back to the inverting "-" input of the op-amp. Lastly, the design should meet the design constraints stated below.

Design Constraints

- The error (difference) between the input signal and output signal should be < 0.1%
- Bandwidth of the follower should be > 100MHz
- Slew-rate with maximum load > 100V/microsecond
- Current draw from VDD should be less than 10mA under full load conditions
- Output swing should be 80% of VDD (e.g. 0.5V to 4.5V when VDD=5V or 0.12V to 2.88V when VDD=3V. The output swing doesn't have to be centered as these examples are, that is, 0.25V to 4.25V when VDD=5 V is fine too).

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Transconductance Matching

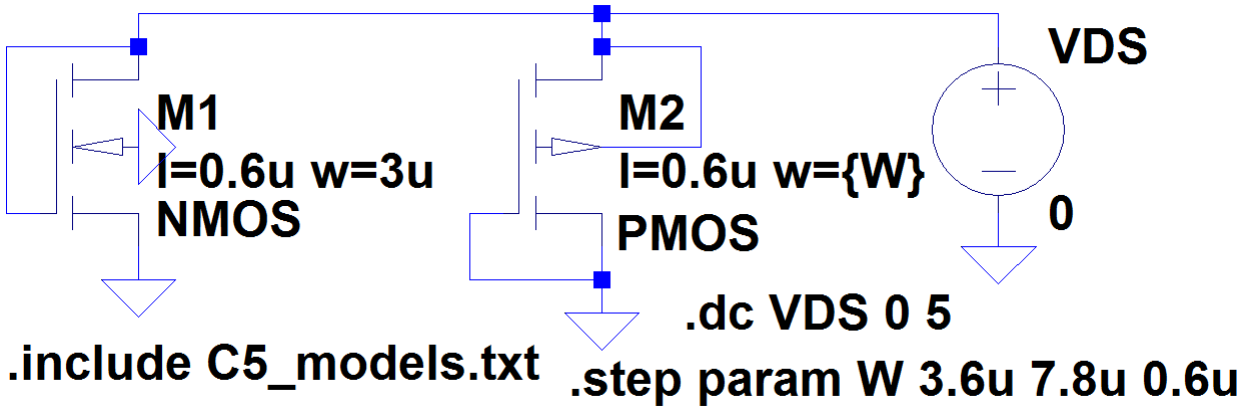
The purpose of this section is to use On's C5 process information in order to match the transconductances of an NMOS and PMOS (g_{mn} and g_{mp}, respectively) based off their sizes. On's C5 process Spice models detailed in C5_models.txt are shown in **Fig. 1**.

```
* BSIM3 models for AMI Semiconductor's C5 process
*
* Don't forget the .options scale=300nm if using drawn lengths
* and the MOSIS SUBM design rules
*
* 2<Ldrawn<500   10<Wdrawn<10000 Vdd=5V
* Note minimum L is 0.6 um while minimum W is 3 um
* Change to level=49 when using HSPICE or SmartSpice

.MODEL NMOS NMOS (                                LEVEL   = 8
+VERSION = 3.1           TNOM    = 27             TOX     = 1.39E-8
+XJ      = 1.5E-7        NCH     = 1.7E17         VTH0    = 0.6696061
+K1      = 0.8351612     K2      = -0.0839158     K3      = 23.1023856
+K3B     = -7.6841108    W0      = 1E-8           NLX     = 1E-9
+DVT0W   = 0             DVT1W   = 0              DVT2W   = 0
+DVT0    = 2.9047241     DVT1    = 0.4302695      DVT2    = -0.134857
+U0      = 458.439679    UA      = 1E-13          UB      = 1.485499E-18
+UC      = 1.629939E-11  VSAT    = 1.643993E5     A0      = 0.6103537
+AGS     = 0.1194608     B0      = 2.674756E-6    B1      = 5E-6
+KETA    = -2.640681E-3  A1      = 8.219585E-5    A2      = 0.3564792
+RDSW    = 1.387108E3    PRWG    = 0.0299916      PRWB    = 0.0363981
+WR      = 1             WINT    = 2.472348E-7    LINT    = 3.597605E-8
+XL      = 0             XW      = 0              DWG     = -1.287163E-8
+DWB     = 5.306586E-8   VOFF    = 0              NFACTOR = 0.8365585
+CIT     = 0             CDSC    = 2.4E-4         CDSCD   = 0
+CDSCB   = 0             ETA0    = 0.0246738      ETAB    = -1.406123E-3
+DSUB    = 0.2543458     PCLM    = 2.5945188      PDIBLC1 = -0.4282336
+PDIBLC2 = 2.311743E-3   PDIBLCB = -0.0272914     DROUT   = 0.7283566
+PSCBE1  = 5.598623E8    PSCBE2  = 5.461645E-5    PVAG    = 0
+DELTA   = 0.01          RSH     = 81.8           MOBMOD  = 1
+PRT     = 8.621         UTE     = -1             KT1     = -0.2501
+KT1L    = -2.58E-9      KT2     = 0              UA1     = 5.4E-10
+UB1     = -4.8E-19      UC1     = -7.5E-11       AT      = 1E5
+WL      = 0             WLN     = 1              WW      = 0
+WWN     = 1             WWL     = 0              LL      = 0
+LLN     = 1             LW      = 0              LWN     = 1
+LWL     = 0             CAPMOD  = 2              XPART   = 0.5
+CGDO    = 2E-10         CGSO    = 2E-10          CGBO    = 1E-9
+CJ      = 4.197772E-4   PB      = 0.99           MJ      = 0.4515044
+CJSW    = 3.242724E-10  PBSW    = 0.1            MJSW    = 0.1153991
+CJSWG   = 1.64E-10      PBSWG   = 0.1            MJSWG   = 0.1153991
+CF      = 0             PVTH0   = 0.0585501      PRDSW   = 133.285505
+PK2     = -0.0299638    WKETA   = -0.0248758     LKETA   = 1.173187E-3
+AF      = 1             KF      = 0)
*
.MODEL PMOS PMOS (                                LEVEL   = 8
+VERSION = 3.1           TNOM    = 27             TOX     = 1.39E-8
+XJ      = 1.5E-7        NCH     = 1.7E17         VTH0    = -0.9214347
+K1      = 0.5553722     K2      = 8.763328E-3    K3      = 6.3063558
+K3B     = -0.6487362    W0      = 1.280703E-8    NLX     = 2.593997E-8
+DVT0W   = 0             DVT1W   = 0              DVT2W   = 0
+DVT0    = 2.5131165     DVT1    = 0.5480536      DVT2    = -0.1186489
+U0      = 212.0166131   UA      = 2.807115E-9    UB      = 1E-21
+UC      = -5.82128E-11  VSAT    = 1.713601E5     A0      = 0.8430019
+AGS     = 0.1328608     B0      = 7.117912E-7    B1      = 5E-6
+KETA    = -3.674859E-3  A1      = 4.77502E-5     A2      = 0.3
+RDSW    = 2.837206E3    PRWG    = -0.0363908     PRWB    = -1.016722E-5
+WR      = 1             WINT    = 2.838038E-7    LINT    = 5.528807E-8
+XL      = 0             XW      = 0              DWG     = -1.606385E-8
+DWB     = 2.266386E-8   VOFF    = -0.0558512     NFACTOR = 0.9342488
+CIT     = 0             CDSC    = 2.4E-4         CDSCD   = 0
+CDSCB   = 0             ETA0    = 0.3251882      ETAB    = -0.0580325
+DSUB    = 1             PCLM    = 2.2409567      PDIBLC1 = 0.0411445
+PDIBLC2 = 3.355575E-3   PDIBLCB = -0.0551797     DROUT   = 0.2036901
+PSCBE1  = 6.44809E9     PSCBE2  = 6.300848E-10    PVAG    = 0
+DELTA   = 0.01          RSH     = 101.6          MOBMOD  = 1
+PRT     = 59.494        UTE     = -1             KT1     = -0.2942
+KT1L    = 1.68E-9       KT2     = 0              UA1     = 4.5E-9
+UB1     = -6.3E-18      UC1     = -1E-10         AT      = 1E3
+WL      = 0             WLN     = 1              WW      = 0
+WWN     = 1             WWL     = 0              LL      = 0
+LLN     = 1             LW      = 0              LWN     = 1
+LWL     = 0             CAPMOD  = 2              XPART   = 0.5
+CGDO    = 2.9E-10       CGSO    = 2.9E-10        CGBO    = 1E-9
+CJ      = 7.235528E-4   PB      = 0.9527355      MJ      = 0.4955293
+CJSW    = 2.692786E-10  PBSW    = 0.99           MJSW    = 0.2958392
+CJSWG   = 6.4E-11       PBSWG   = 0.99           MJSWG   = 0.2958392
+CF      = 0             PVTH0   = 5.98016E-3     PRDSW   = 14.8598424
+PK2     = 3.73981E-3    WKETA   = 5.292165E-3    LKETA   = -4.205905E-3
+AF      = 1             KF      = 0)
```

Fig. 1 – On's C5 Process Spice Models (C5_models.txt)

Schem. 1 shows the NMOS and PMOS connected to one another (NMOS drain connected to PMOS source) for transconductance matching. Both the NMOS and PMOS are drain-gate connected to ensure they are each operating in saturation, and their bodies are connected to their sources (GND and VDD, respectively) to eliminate body effect. The size of the NMOS is chosen to be minimum length (Lmin=0.6um=600nm) and minimum width (Wmin=3um) based off On's C5 process information detailed in C5_models.txt shown in **Fig. 1**.



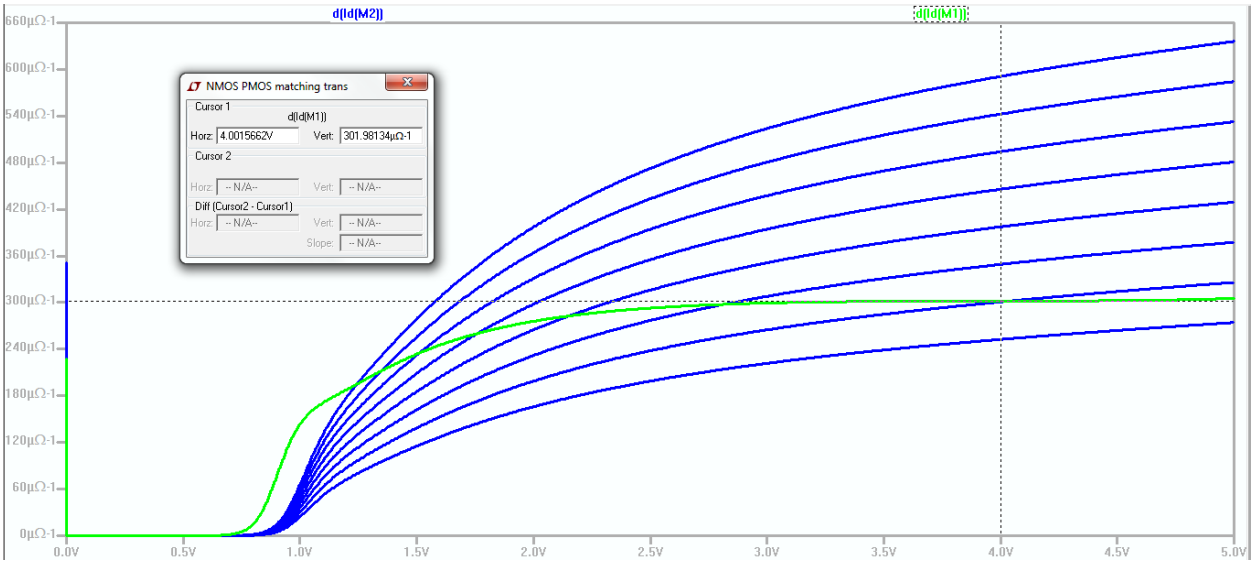
Schem. 1 – Matching NMOS & PMOS Transconductances (g_{mn} & g_{mp})

It is noted that "…we use 2-5 times minimum length for general design" and "…we use minimum length for high-speed design" (Baker, pg. 297). It is also important to know that "…using minimum channel lengths results in large mismatches between devices and low MOSFET output resistance" which results in "low gain and large input-referred offset voltages" (Baker, pg. 863). In addition, "…to minimize power and maximize speed, we will use minimum size devices (Baker, pg. 863). This information suggests we should not have started with minimum sizing for the NMOS since we are not designing for high speed since (bandwidth only needs to be greater than 100MHz) or minimized power, we do not want large mismatches between our NMOS and PMOS, and we do not want low MOSFET output resistance which will result in low gain and large input-referred offset voltages. However, we will use minimum sizing for the NMOS as a starting point and note that we can always come back and repeat the

following process starting with a different sized NMOS. The PMOS in **Schem. 1** has the same length as the NMOS (Lmin=0.6um=600nm) for good matching, and its width is stepped to determine which width gives the closest PMOS transconductance (g_{mp}) to the NMOS transconductance (g_{mn}) as VDS=VSD=VGS=VSG=VDD is swept from 0V to 5V. **Sim. 1** shows the transconductances of the NMOS and PMOS (g_{mn} and g_{mp}, respectively) by plotting the derivative of their drain currents. See Eq. (9.57).

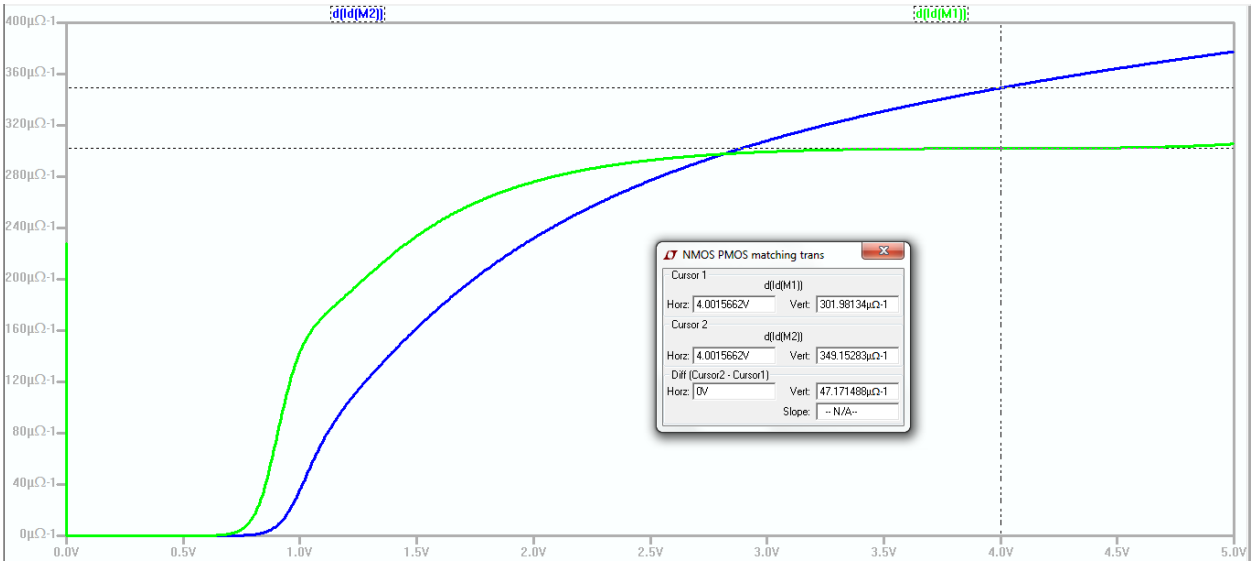
$$g_m = \left[\frac{\partial i_D}{\partial v_{GS}}\right]_{\substack{I_D = \text{constant} \\ V_{GS} = \text{constant}}} = v_{sat} \cdot C'_{ox} \cdot W \qquad (9.57)$$

By averaging the area (over 0V to 5V) of the various PMOS transconductance curves (corresponding to the various PMOS widths), it can be seen that the third curve from the bottom (corresponding to W_{PMOS}=4.8um) best matches the NMOS transconductance curve.



Sim. 1 – Matching NMOS & PMOS Transconductances (g_{mn} & g_{mp})

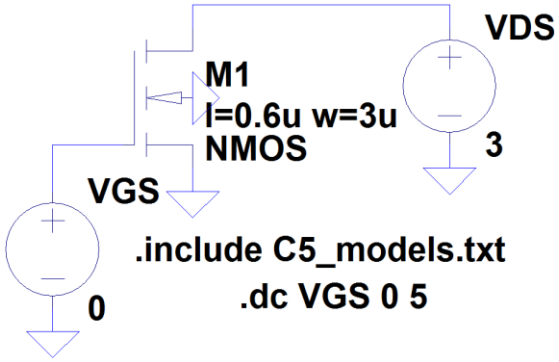
Sim. 1-1 shows the PMOS transconductance (g_{mp}=349uA/V) for W_{PMOS}=4.8um and NMOS transconductance (g_{mn}=302uA/V) for VDS=VSD=VDD=4V. This result simply shows the NMOS and PMOS transconductances (g_{mn} and g_{mp}, respectively) are relatively closely matched for the specified sizes.



Sim. 1-1 – Matching NMOS & PMOS Transconductances (g_{mn} & g_{mp}) (W_{PMOS}=4.8um)

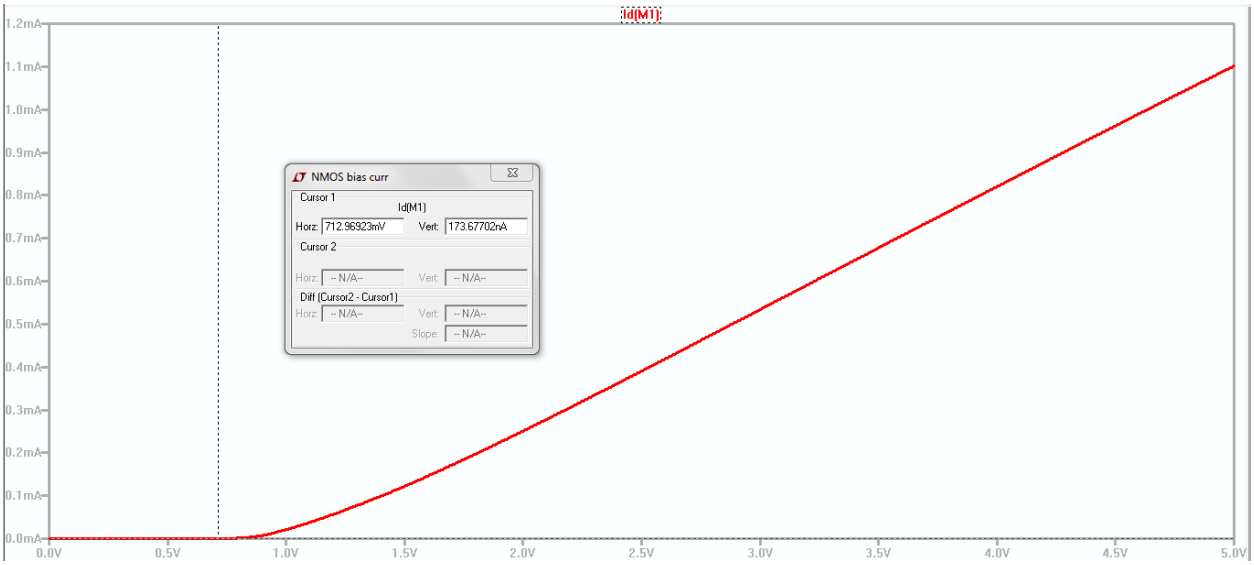
NMOS Characterization

The purpose of this section is to sweep VGS in order to determine threshold voltage (Vthn), bias current (Ibiasn), and bias voltage (Vbiasn=VGS) to then determine output resistance (r_{on}), transconductance (g_{mn}), and transition frequency (f_T) for the NMOS. **Schem. 2** shows the NMOS (3um/0.6um) with VDS=3V in order to characterize the NMOS on the lower end of VDD.



Schem. 2 – NMOS: VGS Sweep

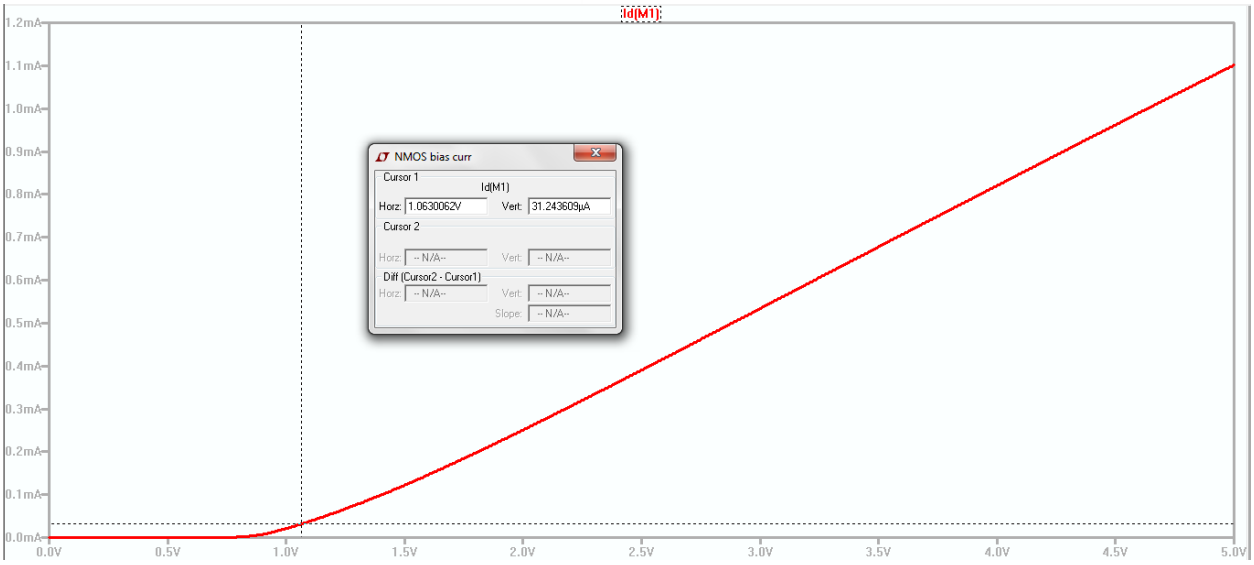
Sweeping VGS from 0V to 5V results in **Sim. 2** which shows VGS=Vthn=713mV. This is the voltage in which the NMOS turns on.



Sim. 2 – NMOS: VGS Sweep to determine Vthn=713mV

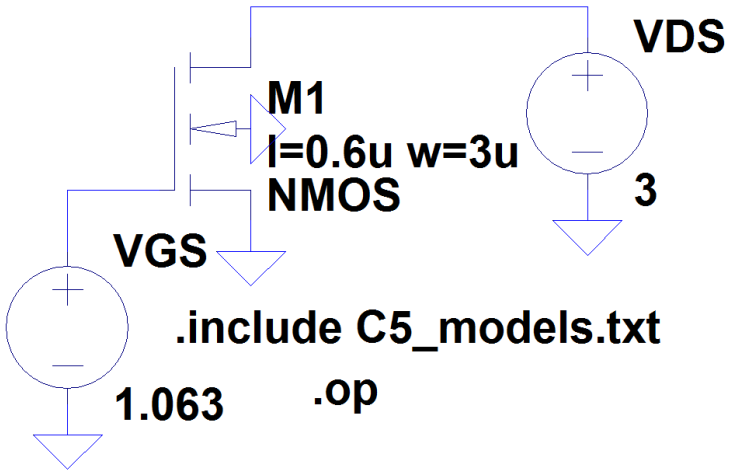
Referring to Eq. (9.54) and noting "…For general analog design, we set the overdrive voltage to 5% of VDD. For high-speed design, we might set the overdrive voltage to 10% of VDD or larger" (Baker, pg. 863), we can estimate Vovn=7%(VDD)=7%(5V)=350mV and can calculate VGS=Vovn+Vthn=(350+713)mV=1.063V. **Sim. 2-1** shows Ibiasn=31.2uA at Vbiasn=VGS =1.063V.

$$V_{ovn} = V_{GS} - V_{THN} \neq V_{DS,sat} \qquad (9.54)$$

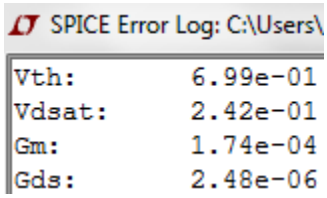


Sim. 2-1 - Ibiasn=31.2uA at Vbiasn=1.063V

Schem. 3 shows the NMOS with VGS=Vbiasn=1.063V and VDS=3V, and **Sim. 3** shows various DC operating point values from the Spice error log including Vthn=699mV, g_{mn}=174uA/V, r_{on}=1/Gds=1/(2.48x10^{-6})=403,226Ω, and VDS,sat (here Vovn)=242mV.

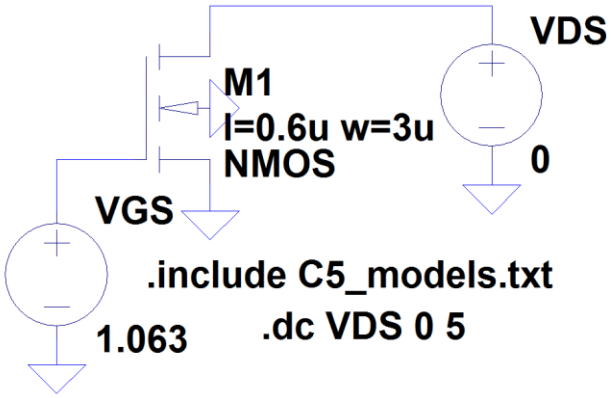


Schem. 3 – NMOS: .op (DC Operating Point)

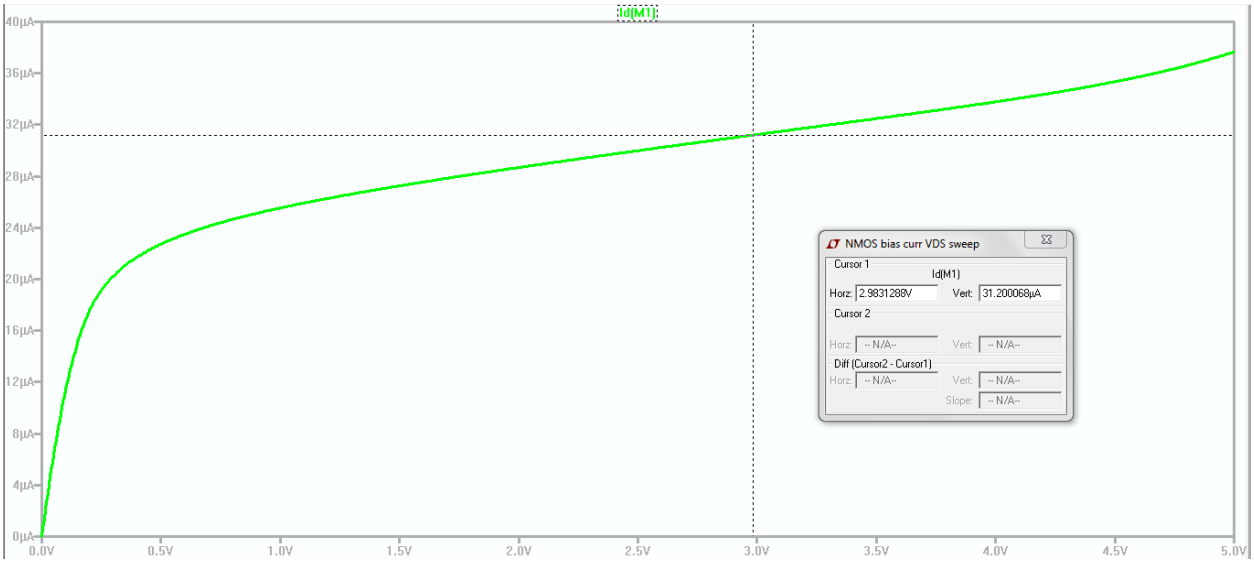


Sim. 3 – NMOS: .op (DC Operating Point)

In order to ensure the NMOS is in saturation when Ibiasn=31.2uA at Vbiasn=1.063V, **Schem. 4** shows VDS being swept from 0V to 5V with VGS=1.063V. **Sim. 4** shows the NMOS is, in fact, in saturation when Ibiasn=31.2uA and gives VDS=2.98V.

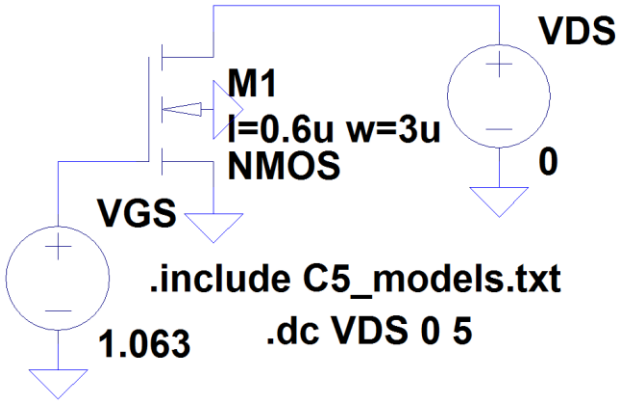


Schem. 4 – NMOS: VDS sweep to ensure Saturation

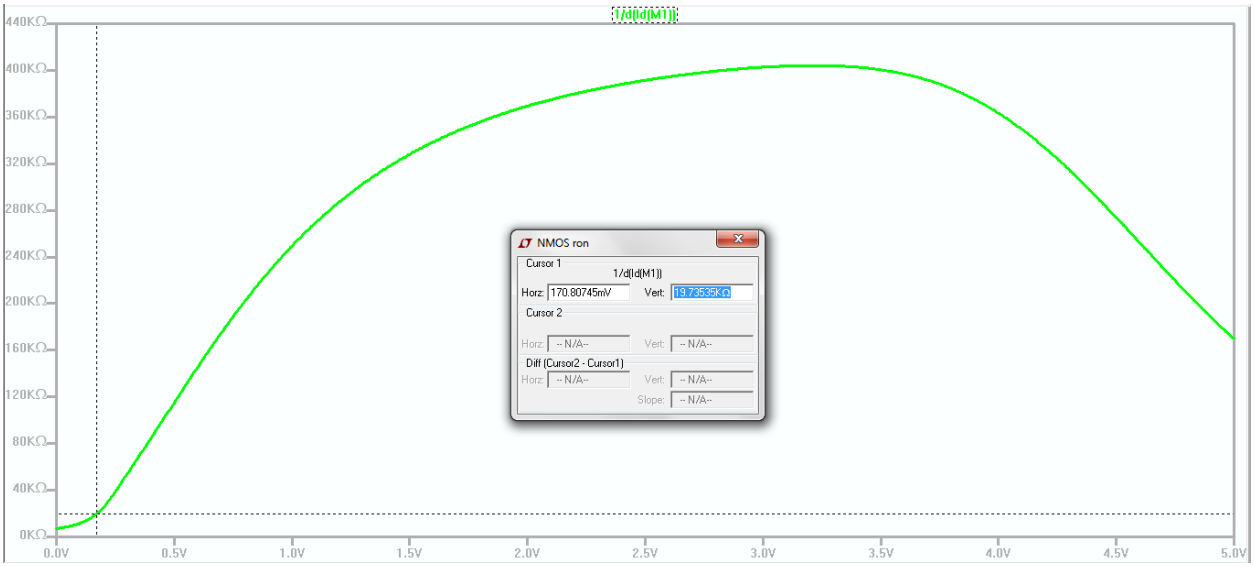


Sim. 4 – NMOS: VDS sweep to ensure Saturation

In order to determine the output resistance (r_{on}) of the NMOS, **Schem.** 5 shows VDS being swept from 0V to 5V with VGS=1.063V. **Sim. 5** shows the output resistance (r_{on}) plotted as the reciprocal of the derivative of the drain current (1/deriv(I_D)). VDS,sat (here Vovn) is approximated as the voltage where the output resistance begins to increase. This results in VDS,sat=170.8mV (approx.) and gives r_{on}=19.74kΩ.



Schem. 5 – NMOS: Output Resistance (r_{on})



Sim. 5 – NMOS: Output Resistance (r_{on})

Table 1 shows values for r_{on} at varying voltages of VDS

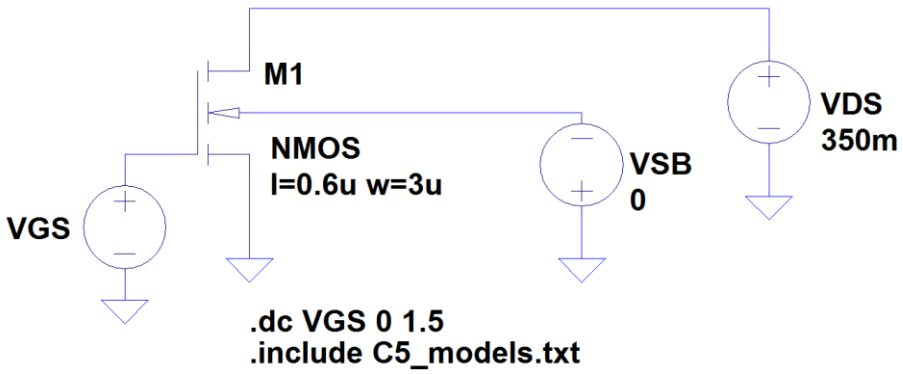
VDS=0V	r_{on}=7.2kΩ
VDS,sat=170.8mV	r_{on}=19.7kΩ
VDS=3 V	r_{on}=402.7kΩ
VDS=4 V	r_{on}=363.0kΩ
VDS=5 V	r_{on}=170.2kΩ

Table 1 – r_{on} for various values of VDS

Lambda can be calculated as $\lambda_n=1/(r_{on}*I_D)=1/(r_{on}*Ibiasn)$ using r_{on}=402.7kΩ @ VDS=3V from **Sim. 5** and using Ibiasn=31.2uA ➔:

- $\lambda_n=1/(r_{on}*I_D)=1/(r_{on}*Ibiasn)=1/((402.7k\Omega)*(31.2uA))=0.0796V^{-1}$
- $\lambda_n=0.0796V^{-1}$

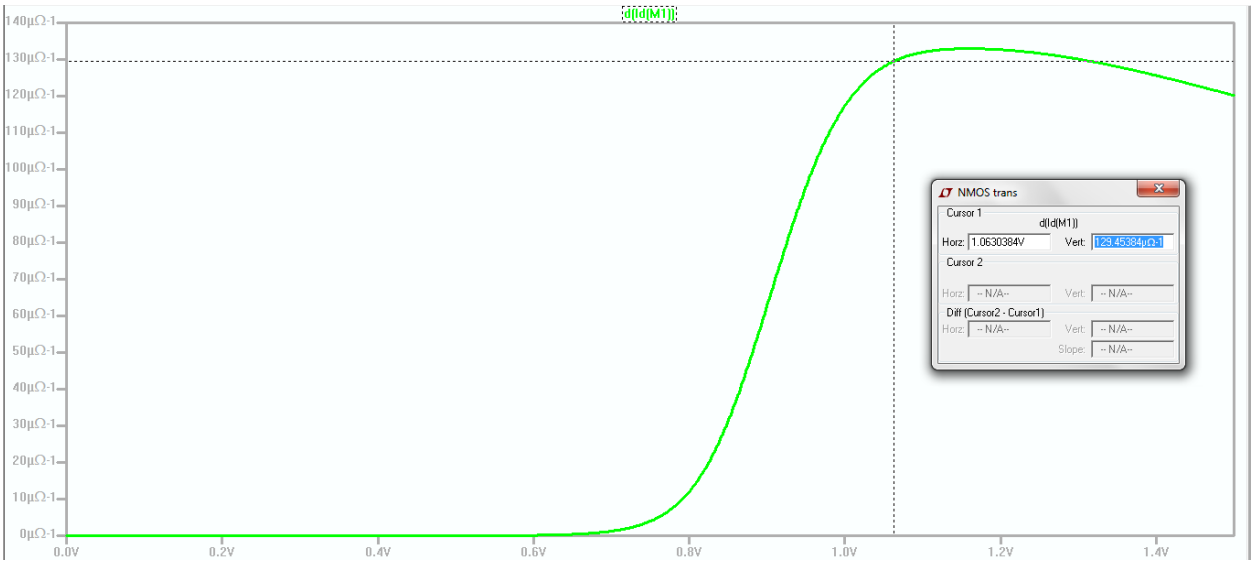
Determining the forward transconductance (g_{mn}) of the NMOS is modeled in **Schem. 6** in which VDS=VDS,sat(= Vovn)=350mV and VGS is swept from 0V to 1.5V in order to show a clear plot.



Schem. 6 – NMOS: Forward Transconductance (g_{mn})

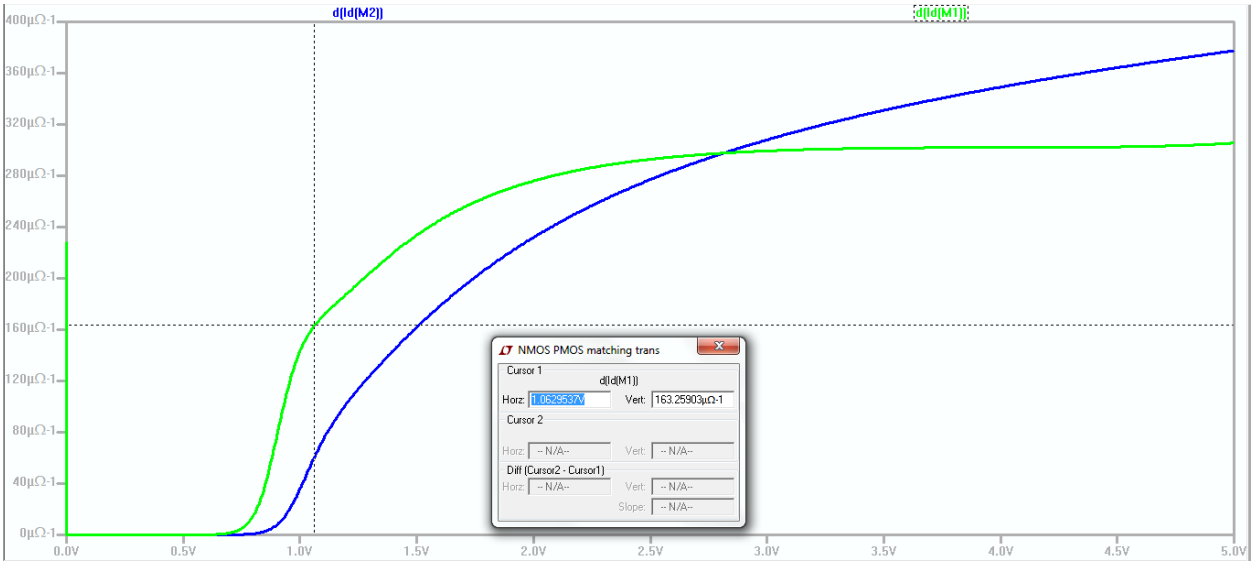
Sim. 6 shows the transconductance (g_{mn}) plotted as the derivative of the drain current (deriv(I_D)) and gives g_{mn}=129.5uA/V at VGS=1.063V. It should be noted that "…g_{mn} does change with VGS, unlike what was indicated in Eq. (9.57). This is because the saturation velocity isn't exactly constant and depends on both VGS and VDS" (Baker, pg. 298-299). The gain can then be calculated using r_{on}=402.7kΩ @ VDS=3V from **Sim. 5** and using g_{mn}=129.5uA/V at VGS=1.063V from **Sim. 6.**

- Gain=$g_{mn}r_{on}$=(129.5uA/V)*(402.7kΩ)=52V/V
- Gain=52V/V



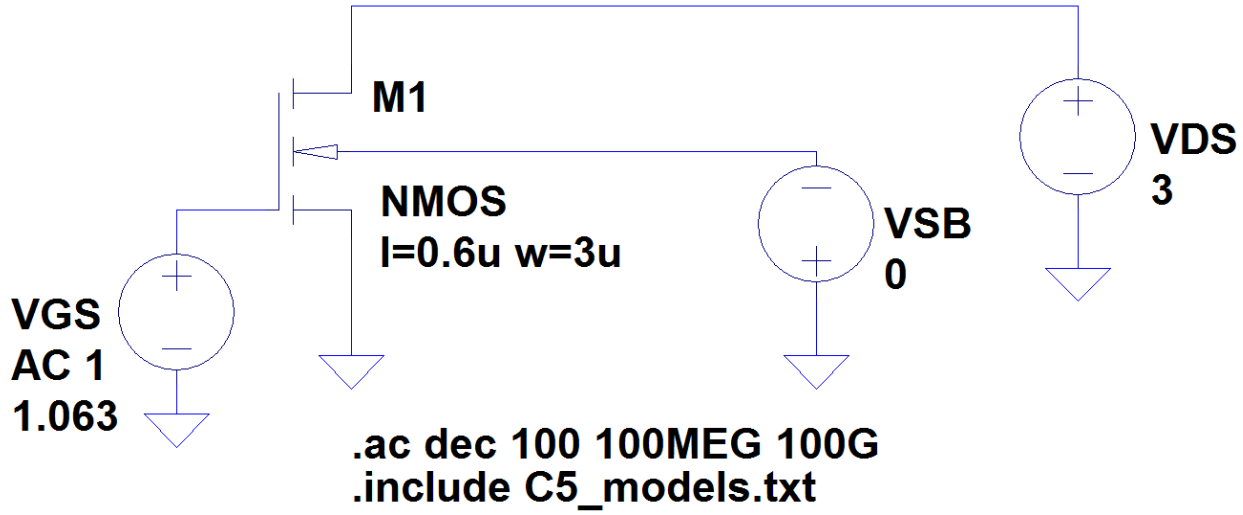
Sim. 6 – NMOS: Forward Transconductance (g_{mn})

Additionally, **Schem. 1** can be referred to for **Sim. 6-1** which shows g_{mn}=163.3uA/V for VDS=VGS=Vbiasn=1.063V.



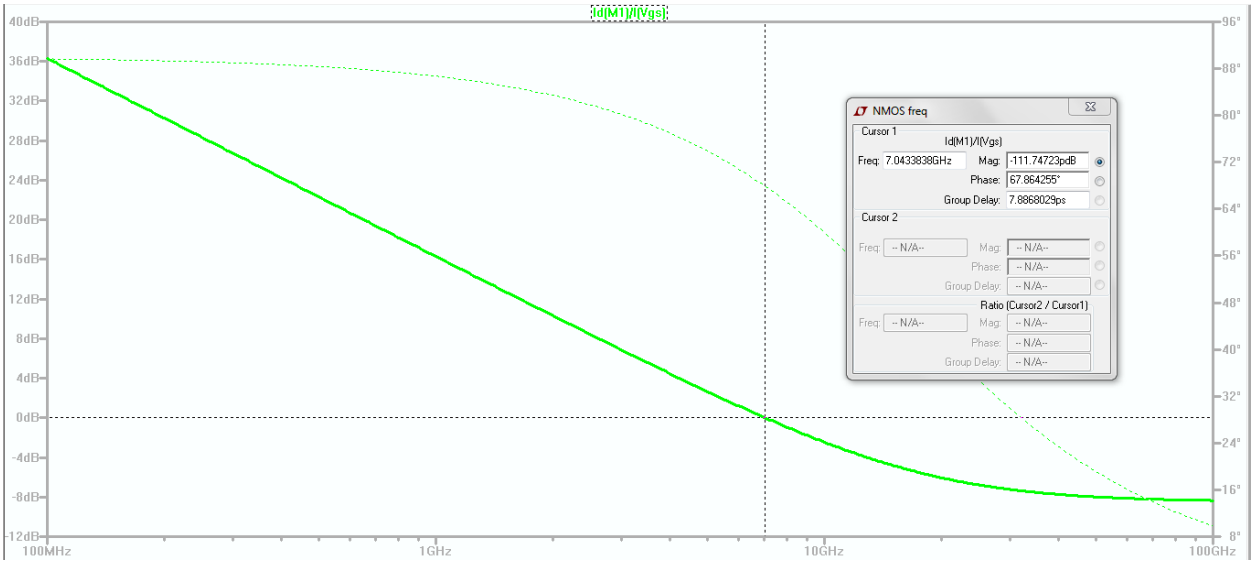
Sim. 6-1 – NMOS: Forward Transconductance (g_{mn}) (Referring to Schem. 1)

Determining the transition frequency (f_{Tn}) of the NMOS is modeled in **Schem. 7** in which VDS=VDS,sat(= Vovn)=350mV, VGS=1.063(AC 1), and an ac simulation is swept from 100MHz to 100GHz in order to show a clear plot.



Schem. 7 – NMOS: Transition Frequency (f_{Tn})

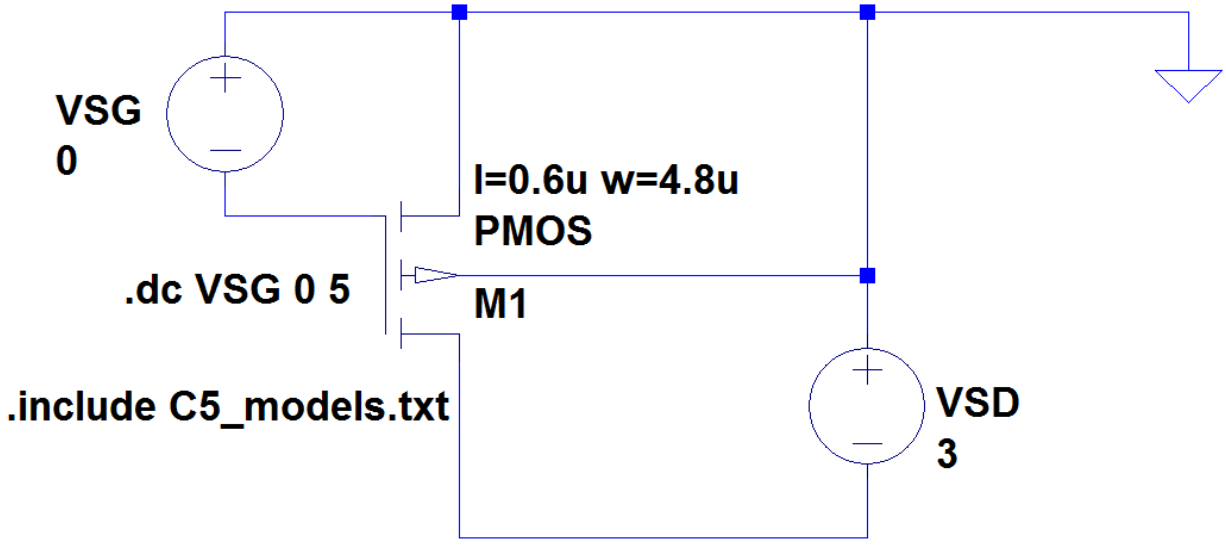
The transition frequency (f_{Tn}) is determined in **Sim. 7** by plotting the drain current divided by the current through VGS (I_D/I_{VGS}) which gives $f_{Tn}=f_{un}$=7.04GHz at 0dB.



Sim. 7 – NMOS: Transition Frequency (f_{Tn})

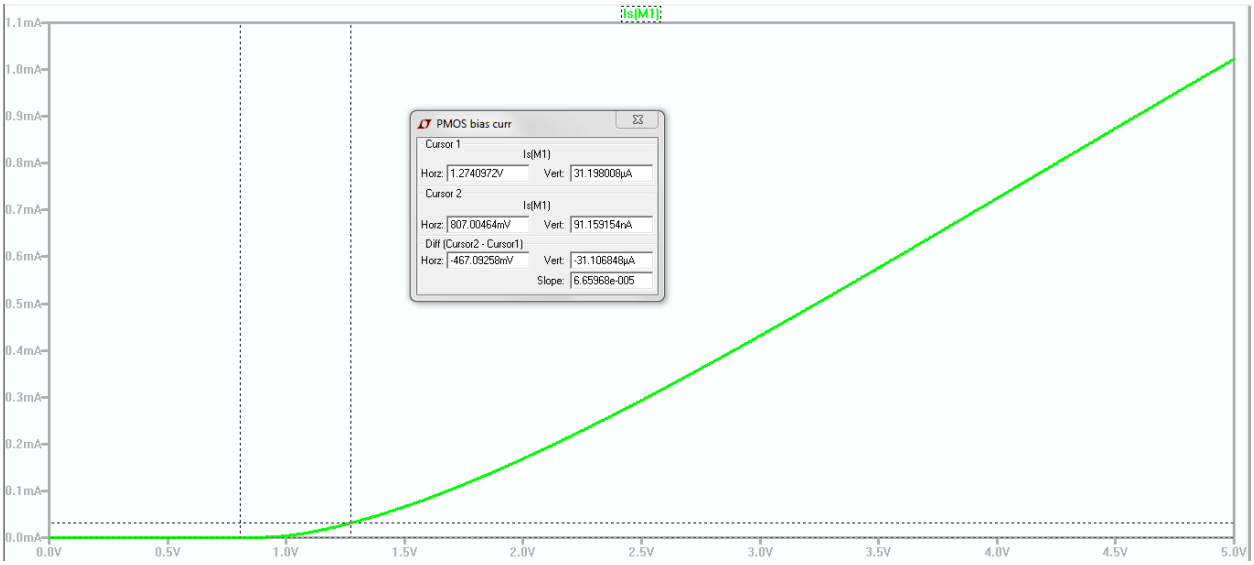
PMOS Characterization

The purpose of this section is to sweep VSG in order to determine threshold voltage (Vthp) and bias voltage (Vbiasp=VSG) based on the NMOS bias current (Ibiasn=Ibiasp=31.2uA) to then determine output resistance (r_{op}), transconductance (g_{mp}), and transition frequency (f_T) for the PMOS. **Schem. 8** shows the PMOS (4.8um/0.6um) with VSD=3V in order to characterize the PMOS on the lower end of VDD.



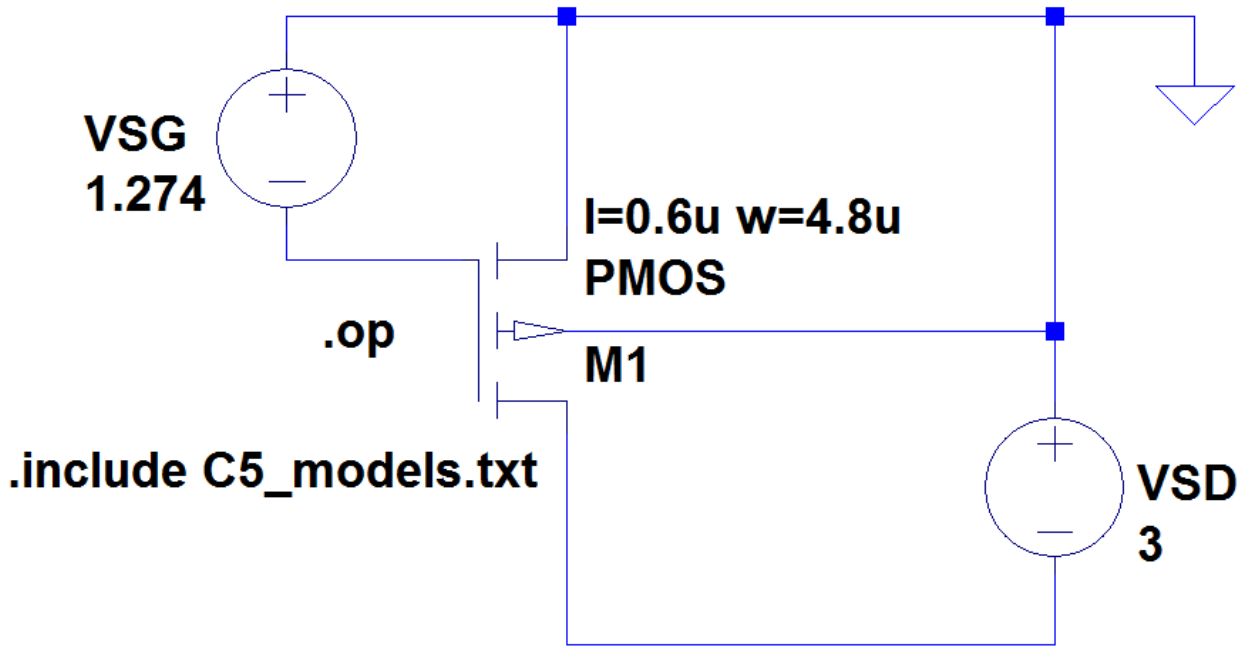
Schem. 8 – PMOS: VSG Sweep

Sweeping VSG from 0V to 5V results in **Sim. 8** which shows VSG=Vthp=807mV (the voltage in which the PMOS turns on) as well as the voltage VSG=Vbiasp=1.274V at Ibiasn=Ibiasp=31.2uA.

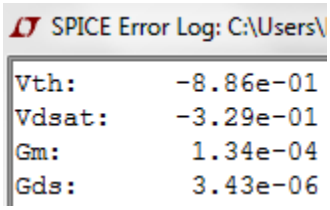


Sim. 8 – PMOS: VSG Sweep to determine Vthp=807mV & Vbiasp=1.274 at Ibiasp=31.2uA

Schem. 9 shows the PMOS with VSG=Vbiasp=1.274V and VSD=3V, and **Sim. 9** shows various DC operating point values from the Spice error log including Vthp=886mV, g_{mp}=134uA/V, r_{op}=1/Gds=1/(3.43x10^{-6})=291,545Ω, and VSD,sat=329mV.

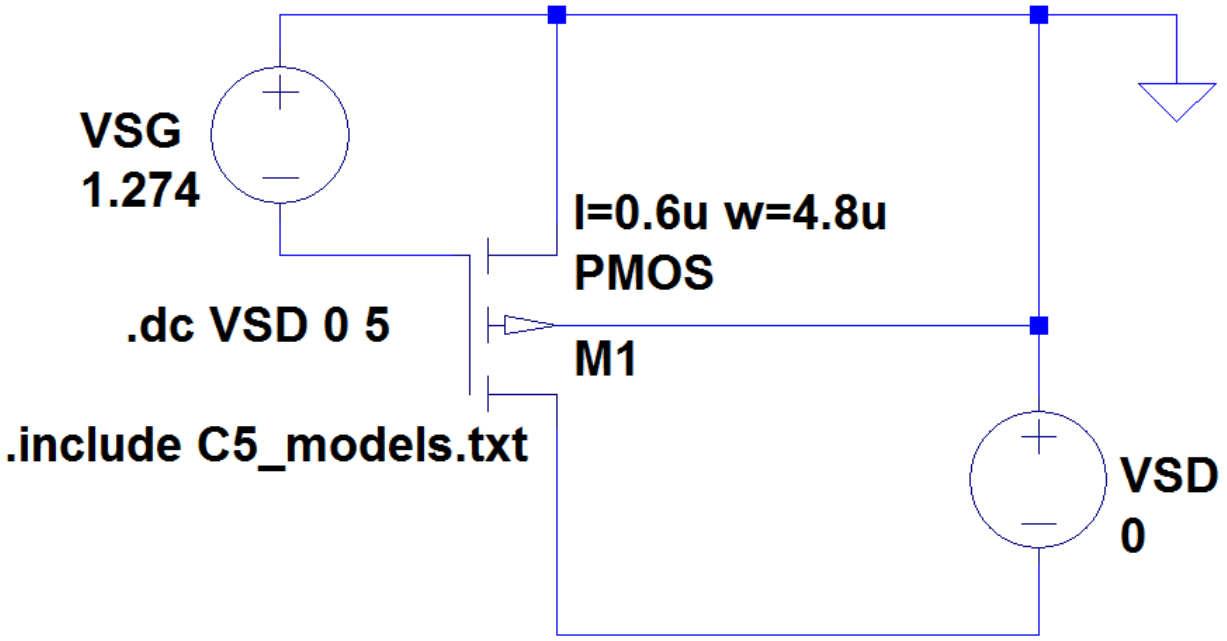


Schem. 9 – PMOS: .op (DC Operating Point)

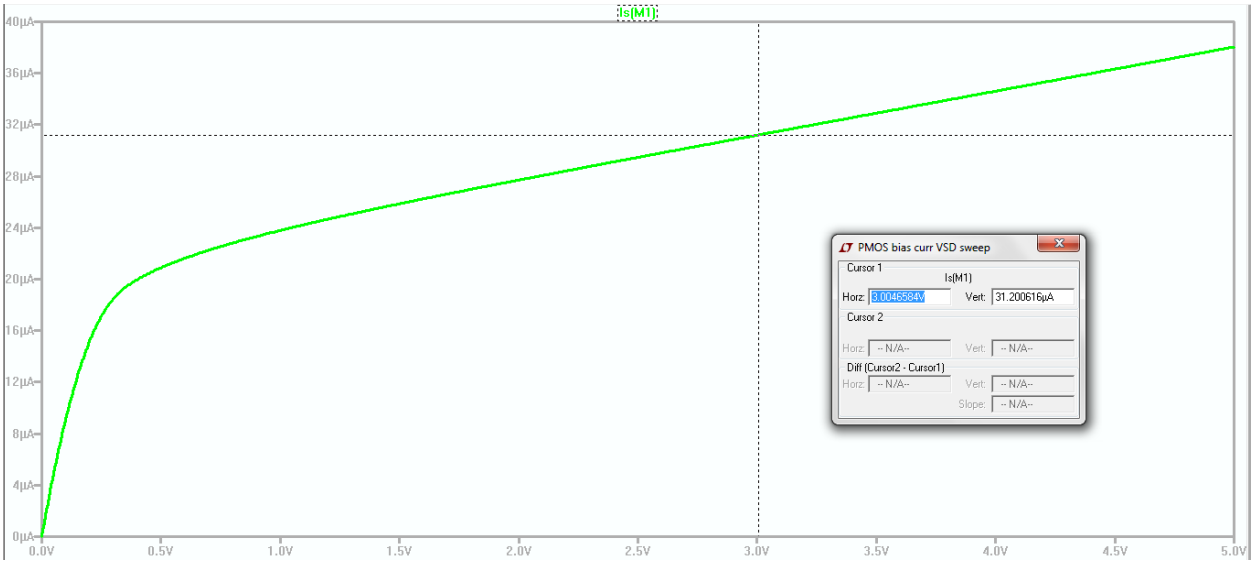


Sim. 9 – PMOS: .op (DC Operating Point)

In order to ensure the PMOS is in saturation when Ibiasp=31.2uA at Vbiasp=1.274V, **Schem. 10** shows VSD being swept from 0V to 5V with VSG=1.274V. **Sim. 10** shows the PMOS is, in fact, in saturation when Ibiasp=31.2uA and gives VSD=3.005V.

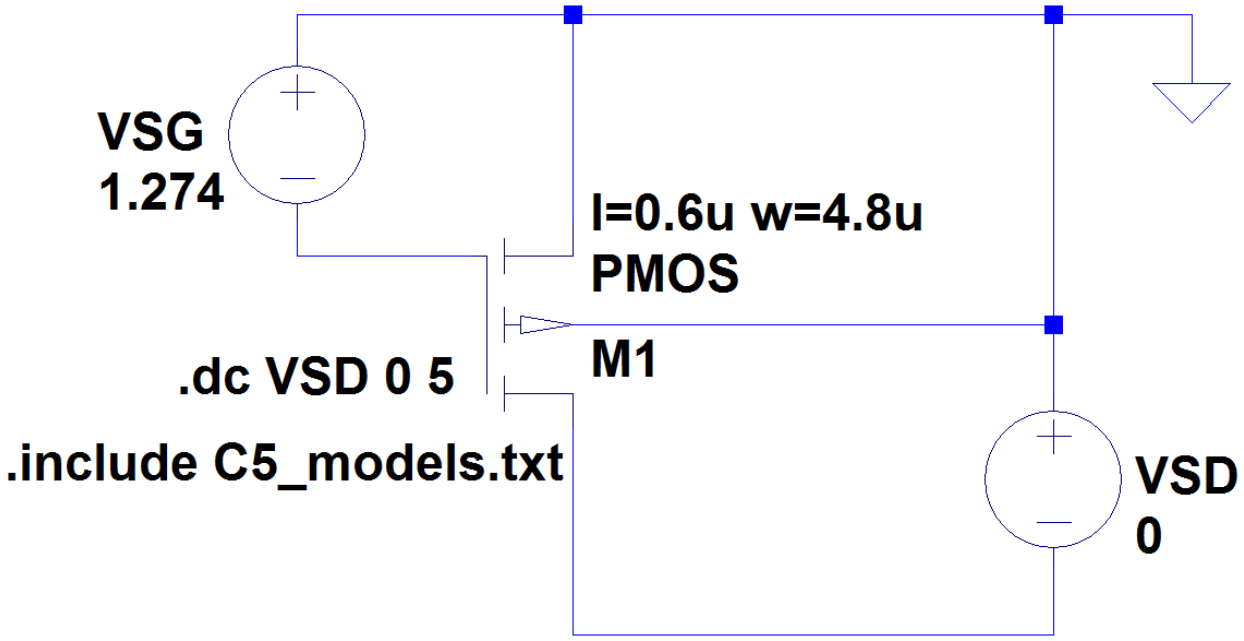


Schem. 10 – PMOS: VSD sweep to ensure Saturation

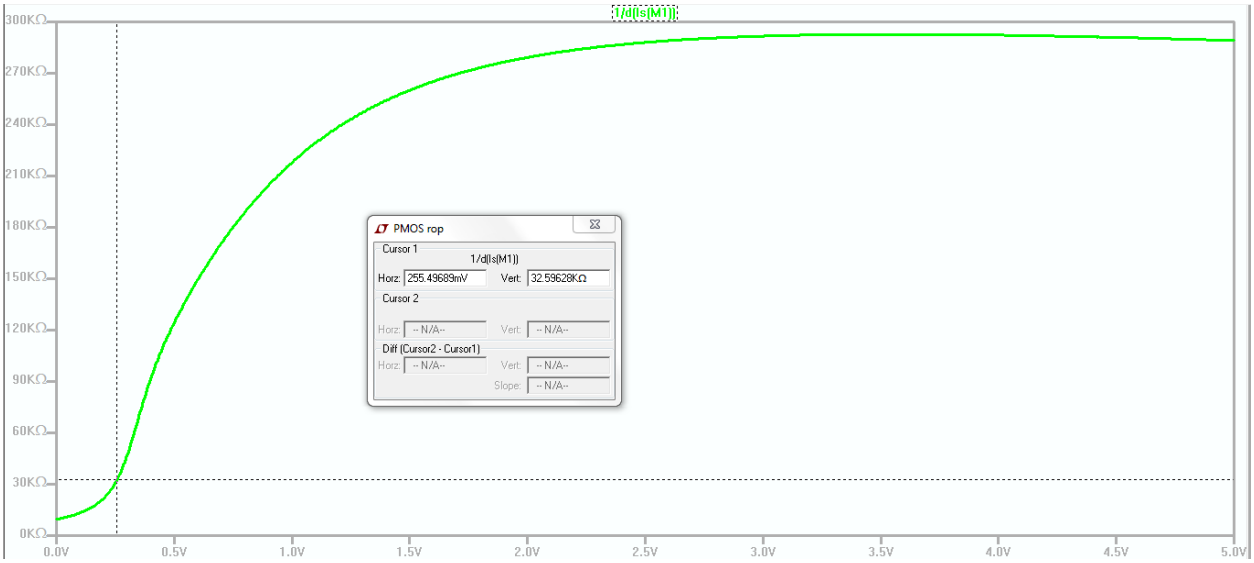


Sim. 10 – PMOS: VSD sweep to ensure Saturation

In order to determine the output resistance (r_{op}) of the PMOS, **Schem. 11** shows VSD being swept from 0V to 5V with VSG=1.274V. **Sim. 11** shows the output resistance (r_{op}) plotted as the reciprocal of the derivative of the drain current ($1/\text{deriv}(I_D)$). VSD,sat is approximated as the voltage where the output resistance begins to increase. This results in VSD,sat=255.5mV (approx.) and gives r_{op}=32.6kΩ.



Schem. 11 – PMOS: Output Resistance (r_{op})



Schem. 11 – PMOS: Output Resistance (r_{op})

Table 2 shows values for r_{op} at varying voltages of VSD

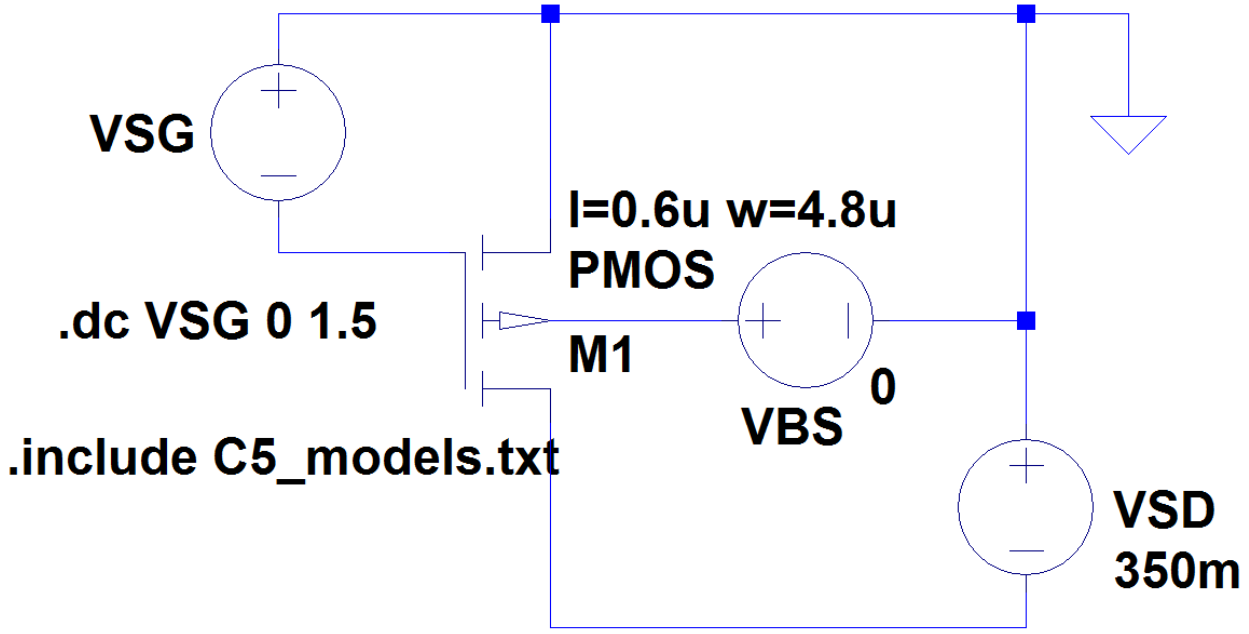
VSD=0V	r_{op}=9.5kΩ
VSD,sat=255.5mV	r_{op}=32.6kΩ
VSD=3 V	r_{op}=291.7kΩ
VSD=4 V	r_{op}=292.3kΩ
VSD=5 V	r_{op}=289.0kΩ

Table 2 – r_{op} for various values of VSD

Lambda can be calculated as $\lambda_p=1/(r_{op}*I_D)=1/(r_{op}*Ibiasp)$ using $r_{op}=291.7k\Omega$ @ VSD=3V from **Sim. 11** and using Ibiasp=31.2uA ➔:

- $\lambda_p=1/(r_{op}*I_D)=1/(r_{op}*Ibiasp)=1/((291.7k\Omega)*(31.2uA))=0.1099V^{-1}$
- $\lambda_p=0.1099V^{-1}$

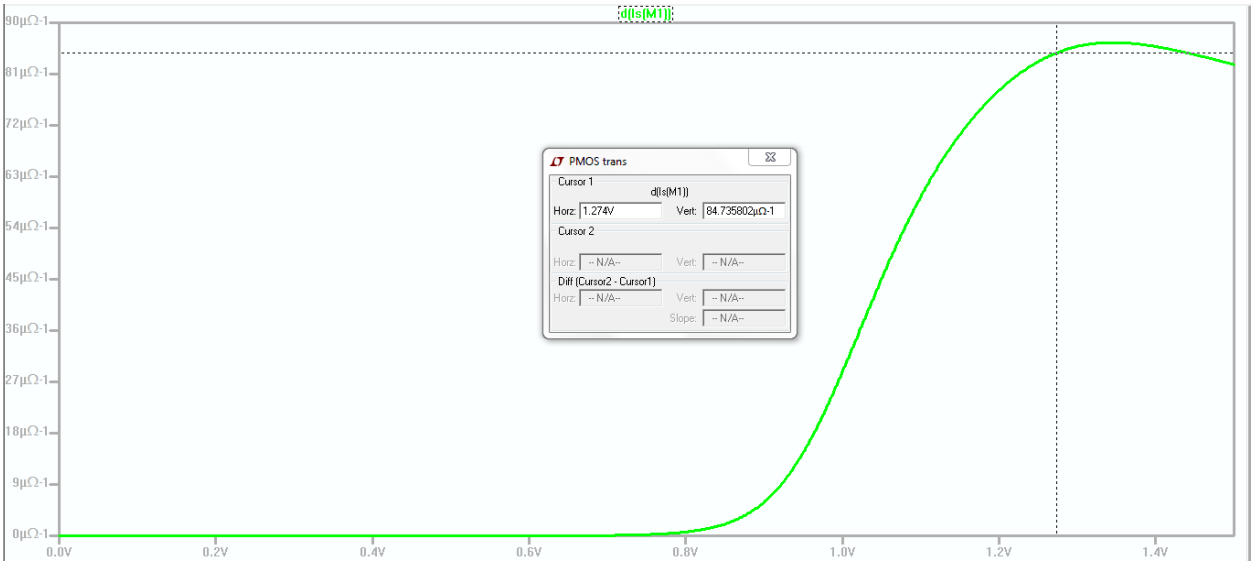
Determining the forward transconductance (g_{mp}) of the PMOS is modeled in **Schem. 12** in which VSD=VSD,sat=350mV and VSG is swept from 0V to 1.5V in order to show a clear plot.



Schem. 12 – PMOS: Forward Transconductance (g_{mp})

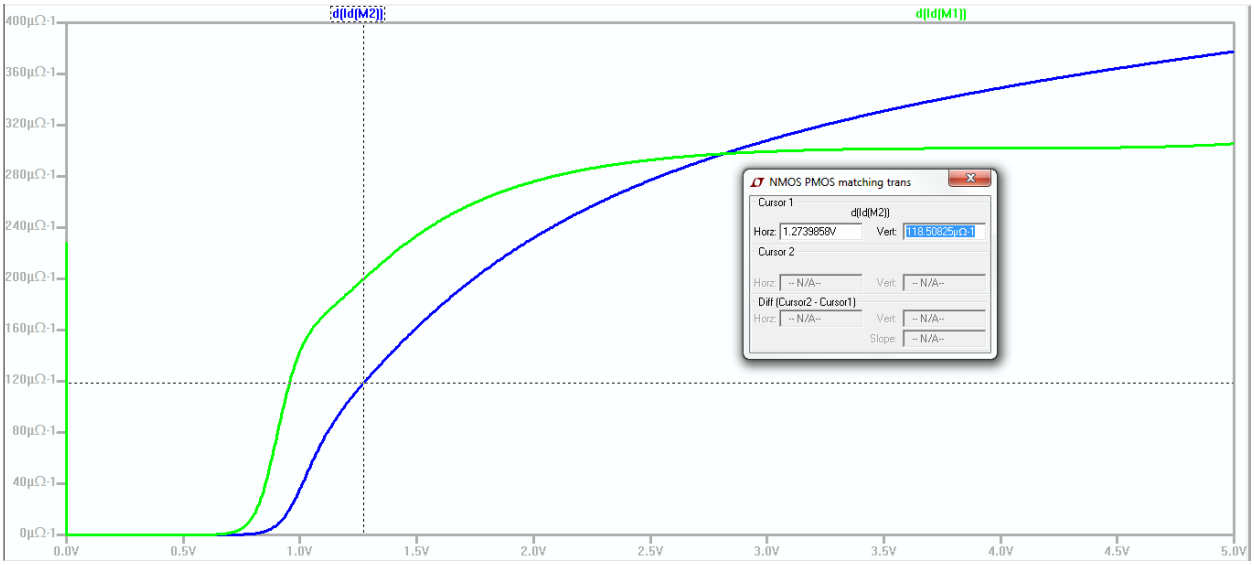
Sim. 12 shows the transconductance (g_{mp}) plotted as the derivative of the drain current (deriv(I_D)) and gives $g_{mp}=84.7uA/V$ at VGS=1.274V. The gain can then be calculated using $r_{op}=291.7k\Omega$ @ VSD=3V from **Sim. 11** and using $g_{mp}=84.7uA/V$ at VSG=1.274V from **Sim. 12.**

- Gain=$g_{mp}r_{op}=(84.7uA/V)*(291.7k\Omega)=24.7V/V$
- Gain=24.7V/V



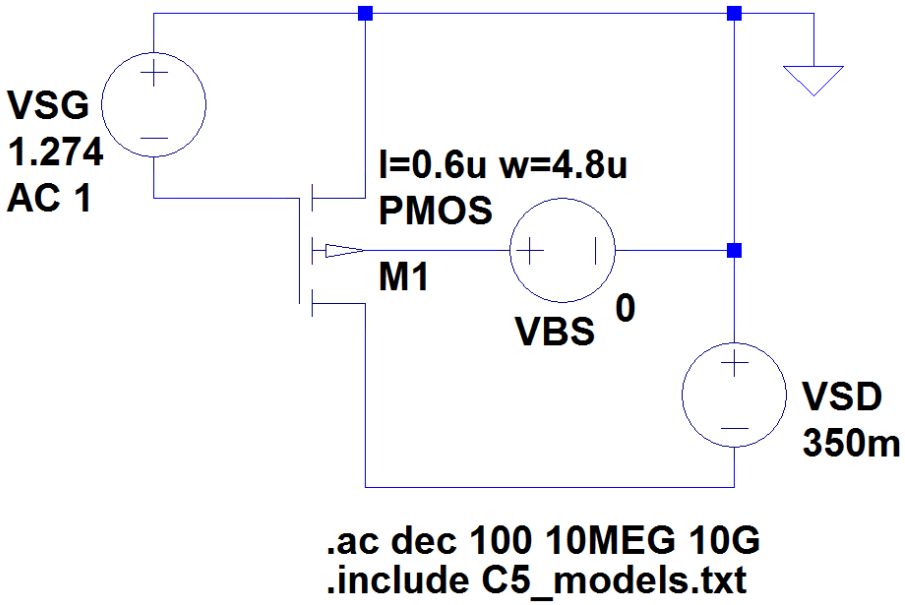
Sim. 12 – PMOS: Forward Transconductance (g_{mp})

Additionally, **Schem. 1** can be referred to for **Sim. 12-1** which shows g_{mp}=118.5uA/V for VDS=VSD=VSG=Vbiasp=1.274V for W_{PMOS}=4.8u.



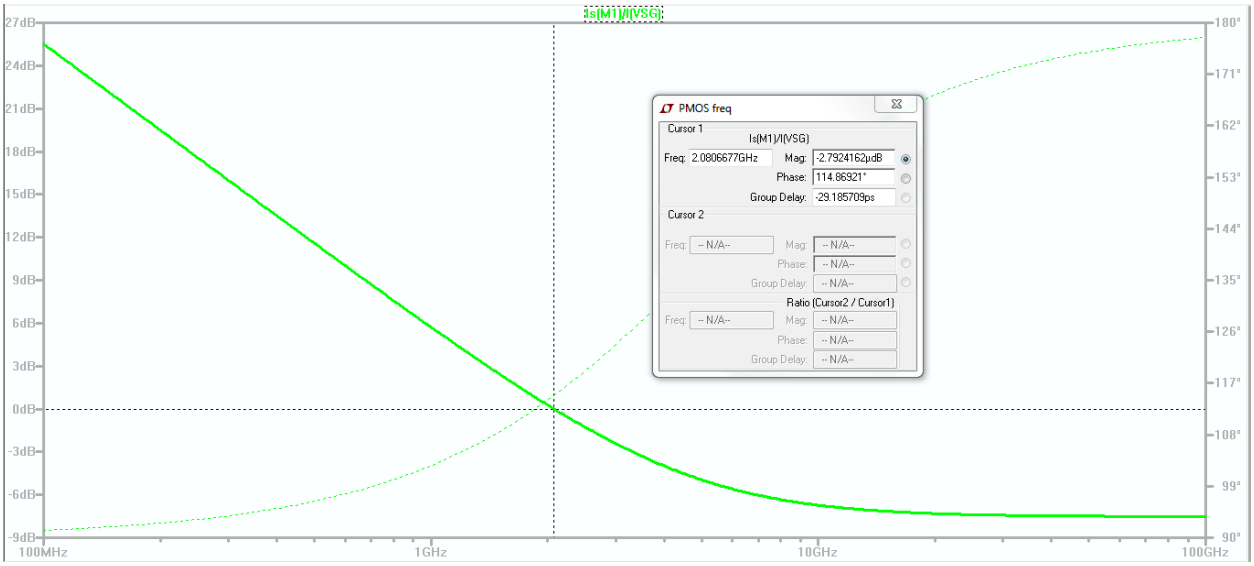
Sim. 12-1 – PMOS: Forward Transconductance (g_{mp}) (Referring to Schem. 1)

Determining the transition frequency (f_{Tp}) of the PMOS is modeled in **Schem. 13** in which VSD=VSD,sat=350mV, VSG=1.274(AC 1), and an ac simulation is swept from 10MHz to 10GHz in order to show a clear plot.



Schem. 13 – PMOS: Transition Frequency (f_{Tp})

The transition frequency (f_{Tp}) is determined in **Sim. 13** by plotting the drain current divided by the current through VSG (I_D/I_{VSG}) which gives $f_{Tp}=f_{un}=2.08GHz$ at 0dB.



Sim. 13 – PMOS: Transition Frequency (f_{Tp})

Table Summary of Characterization

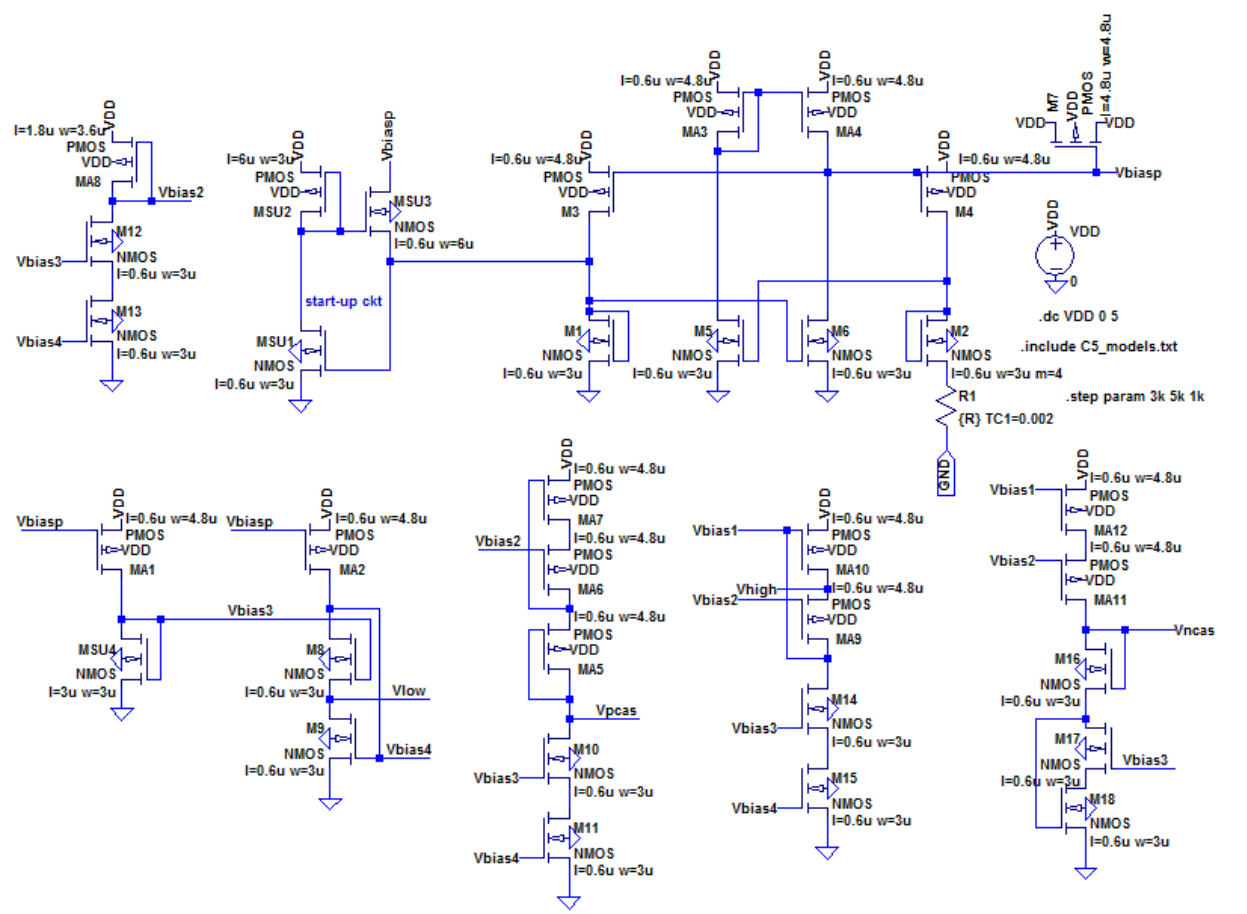
Table 3 was generated using the information captured from the previous simulations.

On's C5 Process MOSFET Parameters VDD=3V to 5V (VDD=3V Used) and a scale factor of 1um (scale=$1x10^{-6}$)			
Parameter	**NMOS**	**PMOS**	**Comments**
Bias Current, I_D	31.2uA (=Ibiasn)	31.2uA (=Ibiasp)	Approximate, see **Sim. 2-1**
W/L	3/0.6 (Min. length, Min. width)	4.8/0.6 (Min. length)	PMOS width based on **Sim. 1**
VDS,sat & VSD,sat	*350mV (Vovn calc.) *242mV (**Sim. 3**)	329mV (**Sim. 9**)	
VGS & VSG	*1.063V (=Vbiasn) (Calc. based on Vovn & Vthn)	*1.274V (=Vbiasp) (**Sim. 8** – based on Ibiasp=Ibiasn & Vthp)	No Body Effect
Vthn & Vthp	*713mV (**Sim. 2**) *699mV (**Sim. 3**)	*807mV (**Sim. 8**) *886mV (**Sim. 9**)	Approx. & .op values
g_{mn} & g_{mp}	*174uA/V (**Sim. 3**) *129.5uA/V (**Sim. 6**) *163.3uA/V (**Sim. 6-1**)	*134uA/V (**Sim. 9**) *84.7uA/V (**Sim. 12**) *118.5uA/V (**Sim. 12-1**)	Similar values for different sim's
r_{on} & r_{op}	*403.2kΩ (**Sim. 3**) *402.7kΩ (Refer to **Sim. 5** & **Table 1**)	*291.6kΩ (**Sim. 9**) *291.7kΩ (Refer to **Sim. 11** & **Table 2**)	Similar values for different sim's
Gain: $g_{mn}r_{on}$ & $g_{mp}r_{op}$	52V/V	24.7V/V	!!Open circuit gain!! See calc. before **Sim. 6** & **Sim. 12**, respectively
λ_n & λ_p	$0.0796V^{-1}$	$0.1099V^{-1}$	See calculation after **Table 1** & **Table 2**
f_{Tn} & f_{Tn}	7.04GHz	2.08GHz	See **Sim. 7** & **Sim. 13**

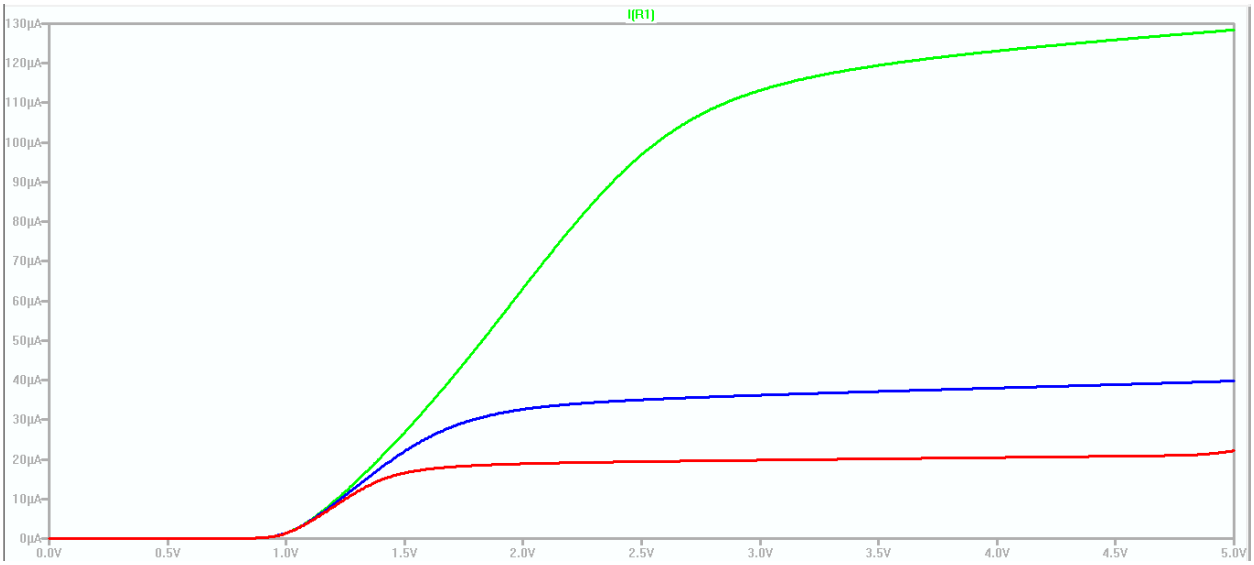
Table 3 - On's C5 Process MOSFET Parameters

Beta-Multiplier Reference (BMR)

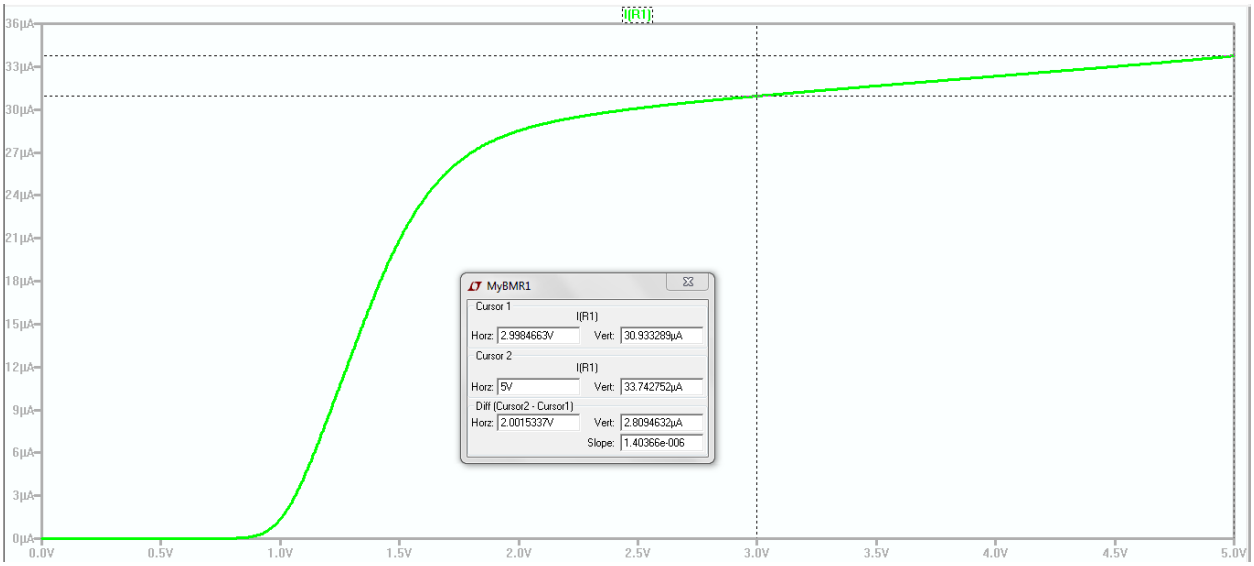
The Beta-Multiplier Reference (BMR) in Fig. 20.47 of the CMOSedu book was used to generate the BMR shown in **Schem. 14.** Except for a few different sized devices, all the NMOS are 3u/0.6u and the PMOS are 4.8u/0.6u. The PMOS in the startup circuit (MSU2) is meant to operate as a large resistor, so its length is greatly increased in order to prevent MSU3 from turning on, preventing Vbiasp from stealing current from Vbiasn. **Schem. 14** shows the resistor (R1) being stepped for different values in order to determine which resistor value results in Iref=Ibiasn=Ibiasp=31.2uA. **Sim. 14** shows R1=4.2k sets Iref=Ibiasn=Ibiasp=31.2uA.



Schem. 14 – BMR (Stepping R1 to get Iref=Ibias=31.2uA)



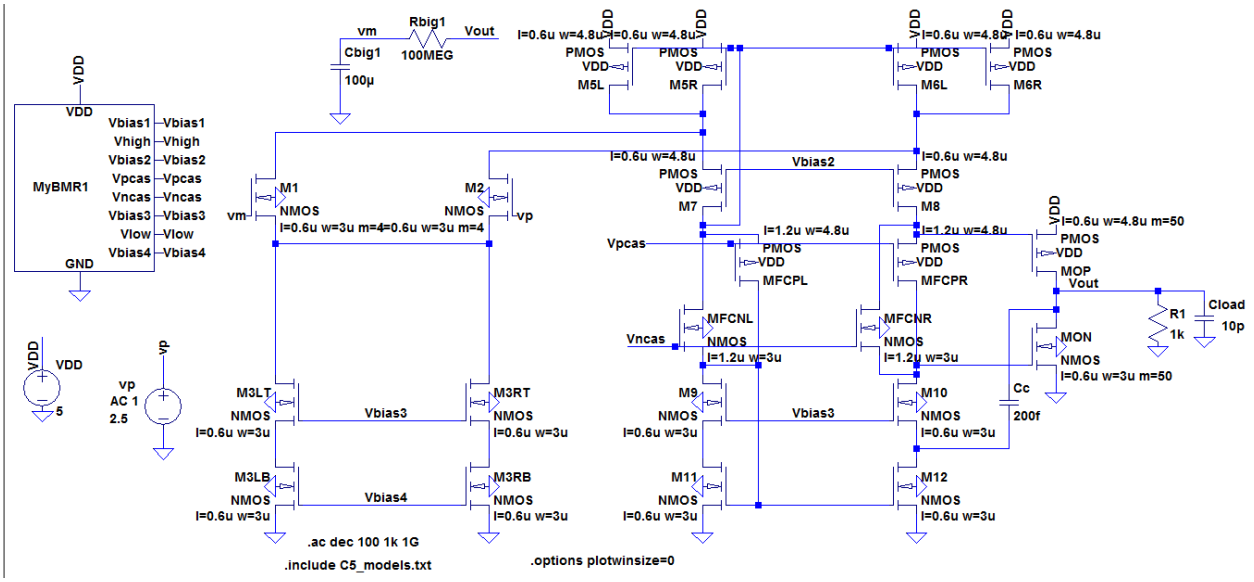
Sim. 14 – BMR (Stepping R1 to get Iref=Ibias=31.2uA)



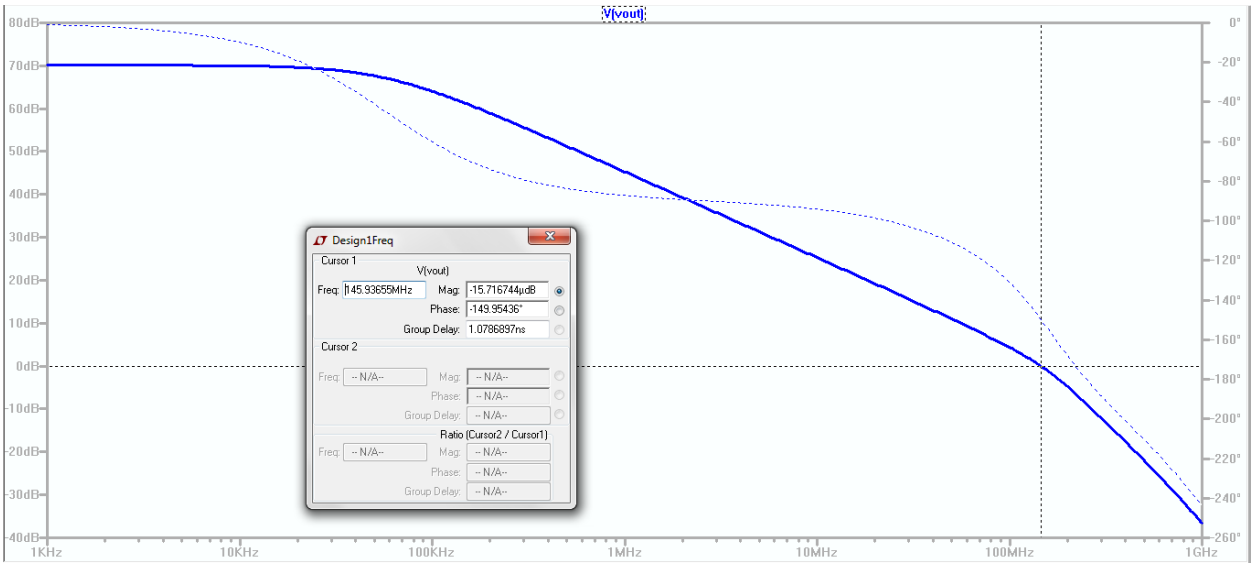
Sim. 14-1 – BMR (R1=4.2k to get Iref=Ibias=31.2uA)

Voltage Follower: Design 1

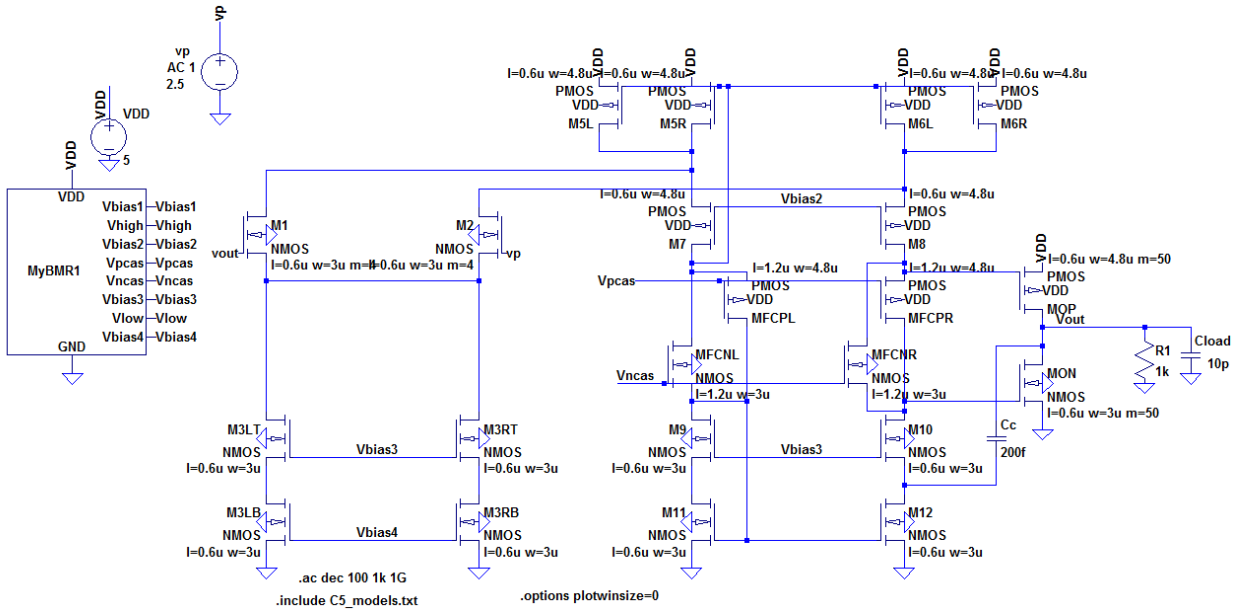
The op-amp design in Fig. 20.44 from the CMOSedu book was used as a starting point for the design of the voltage follower for Design 1. Except for a few different sized devices, all the NMOS are 3u/0.6u and the PMOS are 4.8u/0.6u. **Sim. 15** corresponding to **Schem. 15** shows the unity gain frequency at 0dB and gives f_{un}=145.9MHz.



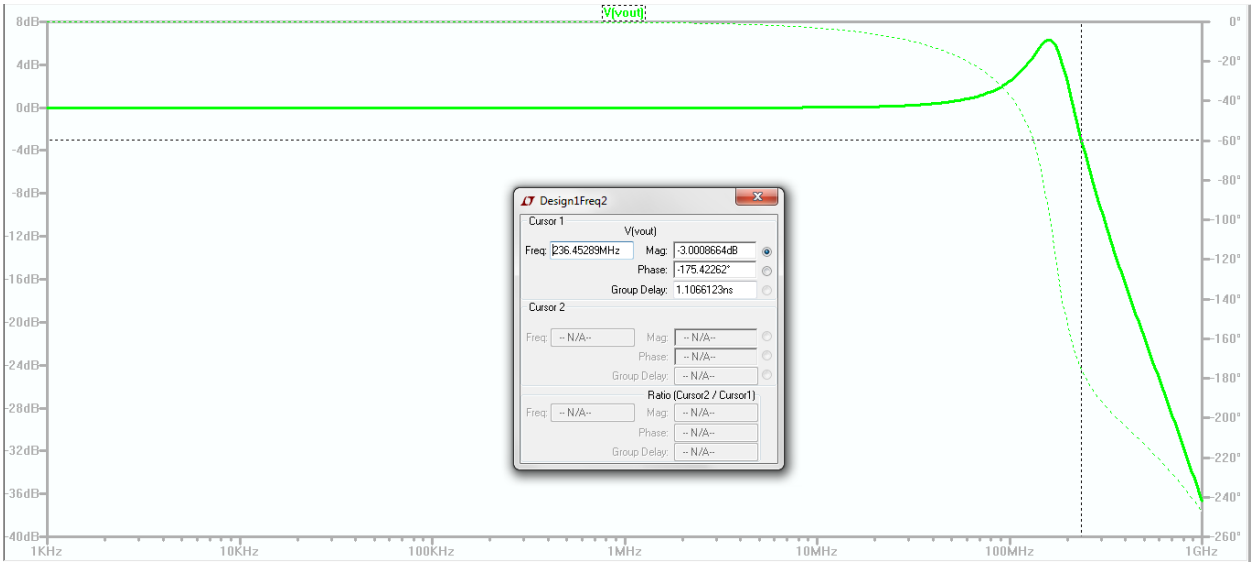
Schem. 15 – Frequency Response



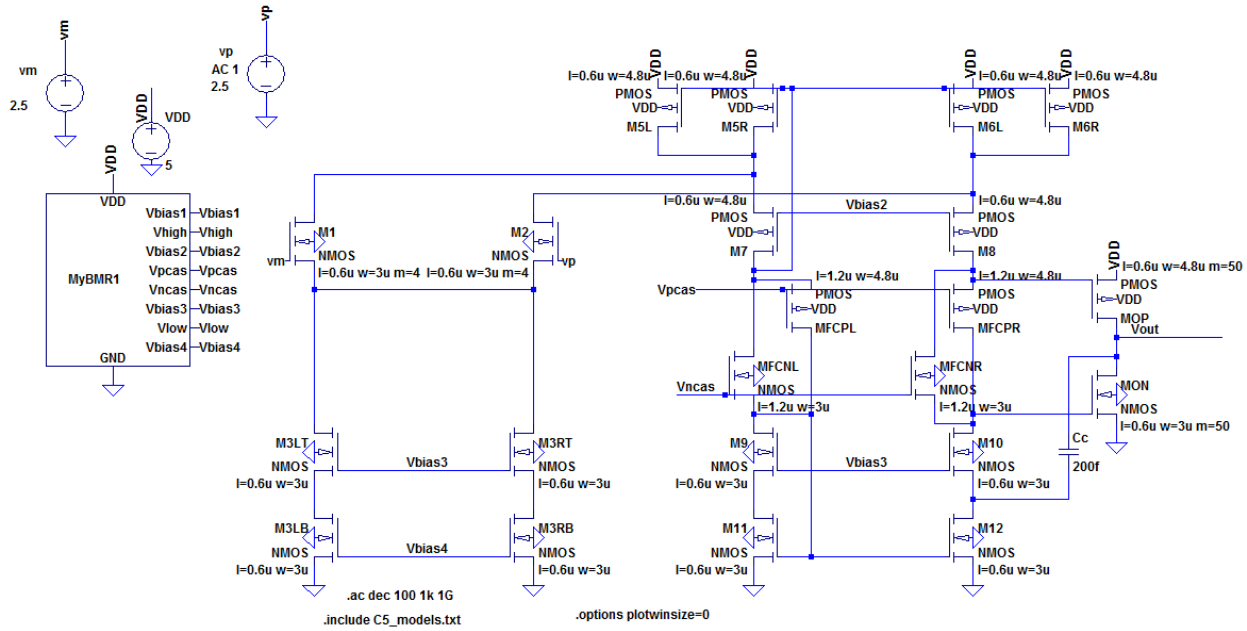
Sim. 15 – Frequency Response (f_{un}=145.9MHz)



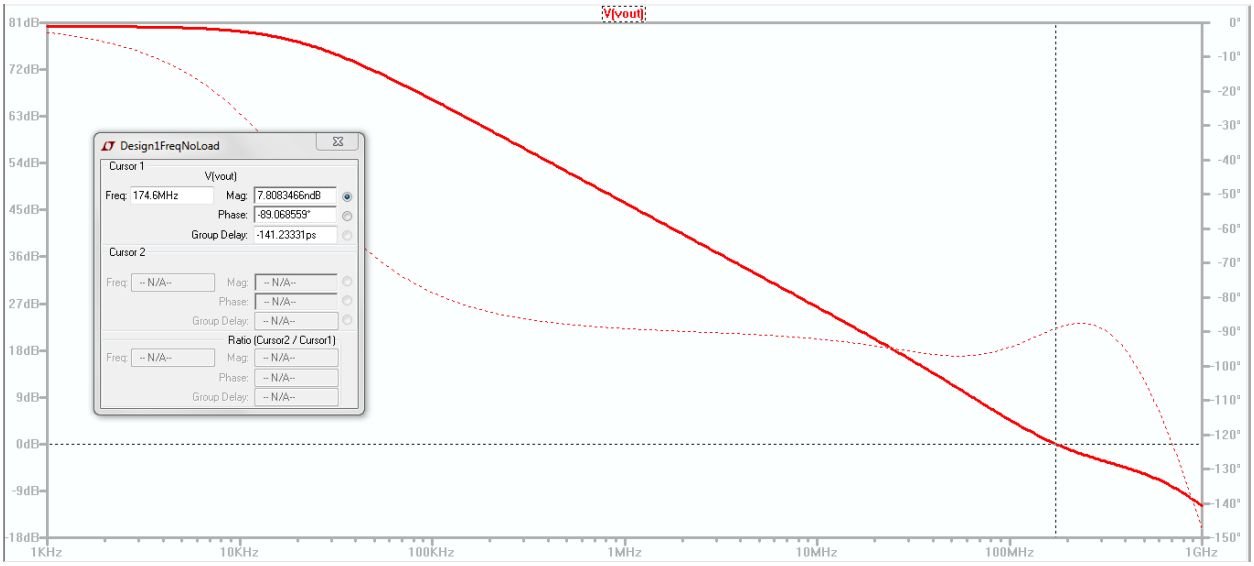
Schem. 16 – Frequency Response



Sim. 16 – Frequency Response

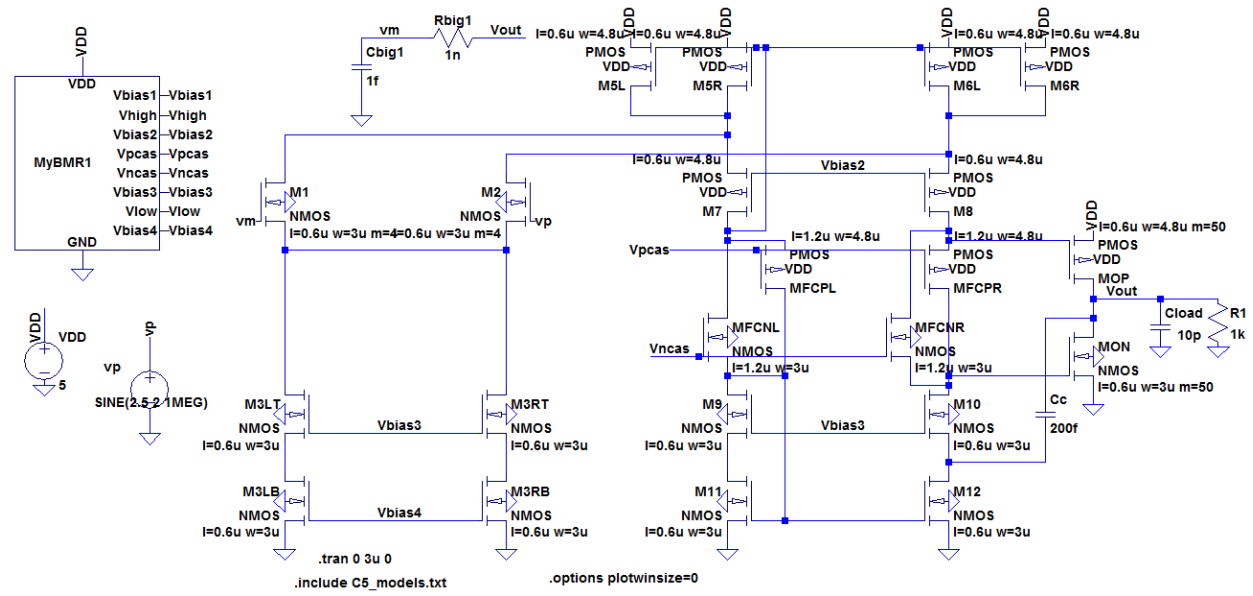


Schem. 17 – Frequency Response

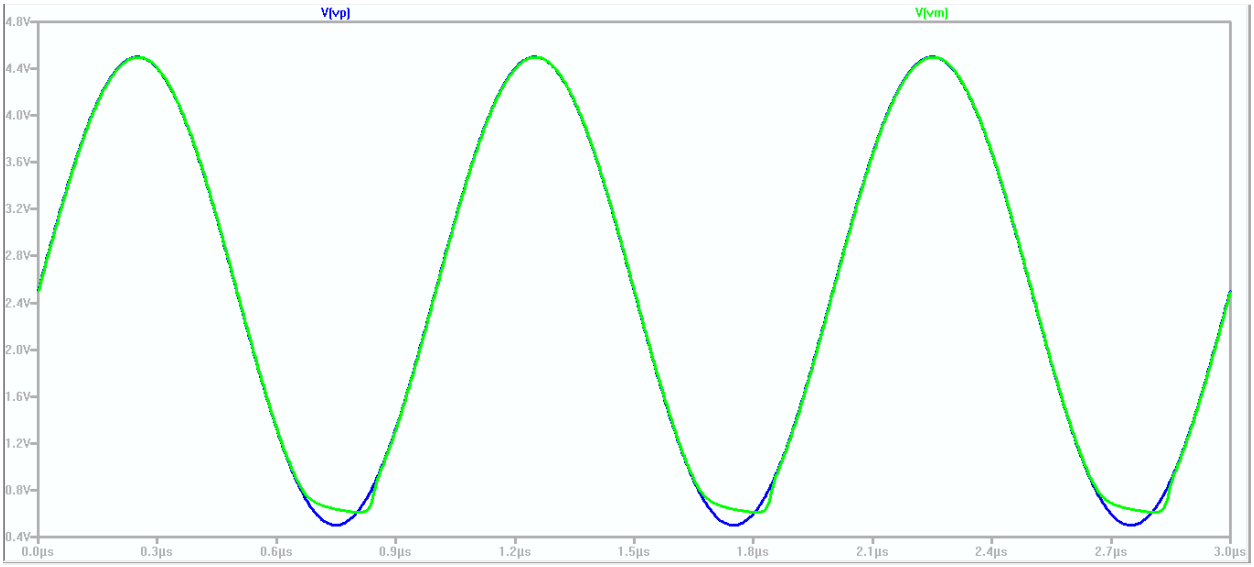


Sim. 17 – Frequency Response

Schem. 18 and the corresponding **Sim. 18** show the output swing of voltage follower for Design 1. The output closely follows the input, but there is unwanted clipping on the bottom swing of the output.



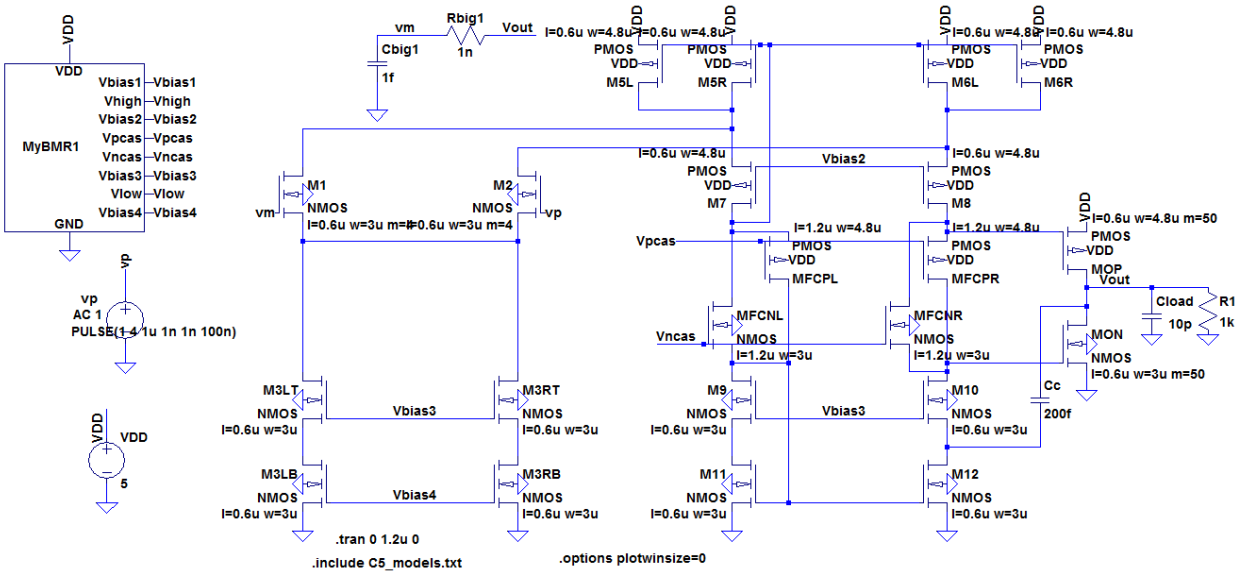
Schem. 18 – Output Swing



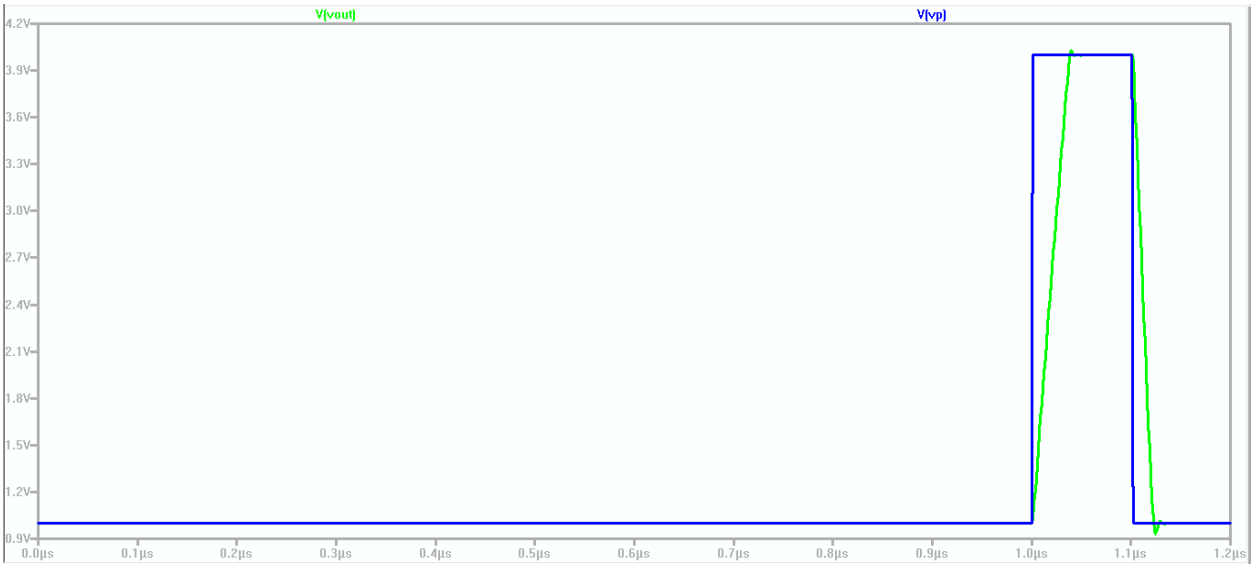
Sim. 18 – Output Swing

Schem. 19 and **Sim. 19** shows a pulse input and the corresponding output. This is used to calculate the percent error difference as ((Vin-Vout)/(Vin+Vout))*100. The percent error difference for Design 1 can then be calculated from **Sim. 19** as ((4.0014-4)/(4.0014+4))*100 = 0.012%.

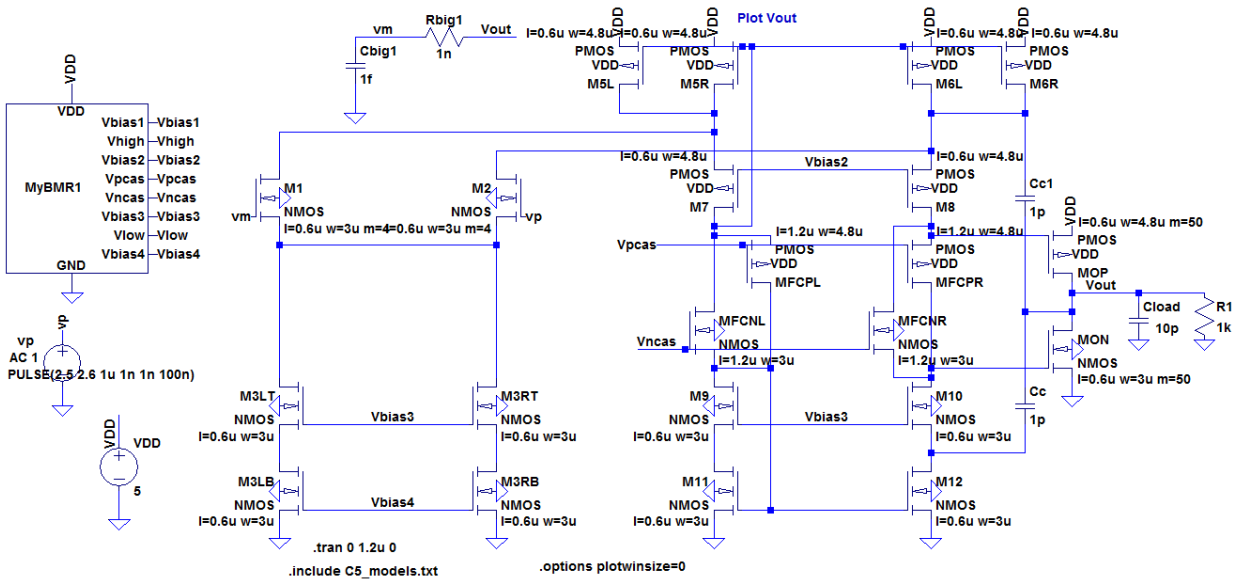
⇨ % Error = 0.012%.



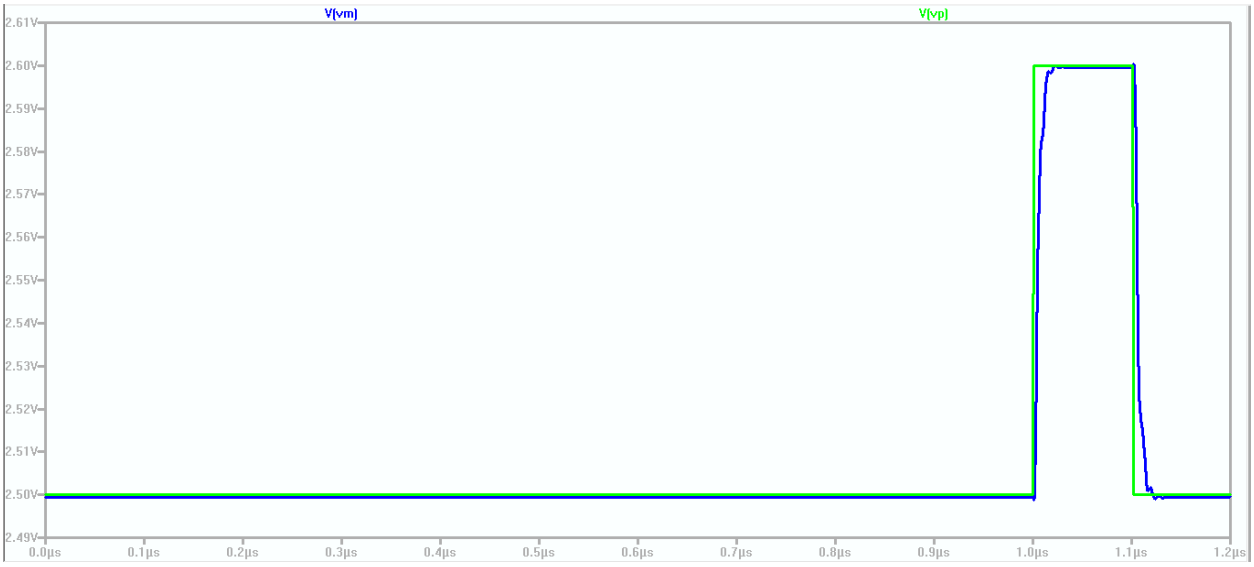
Schem. 19 - % Error Difference



Sim. 19 - % Error Difference = 0.012%

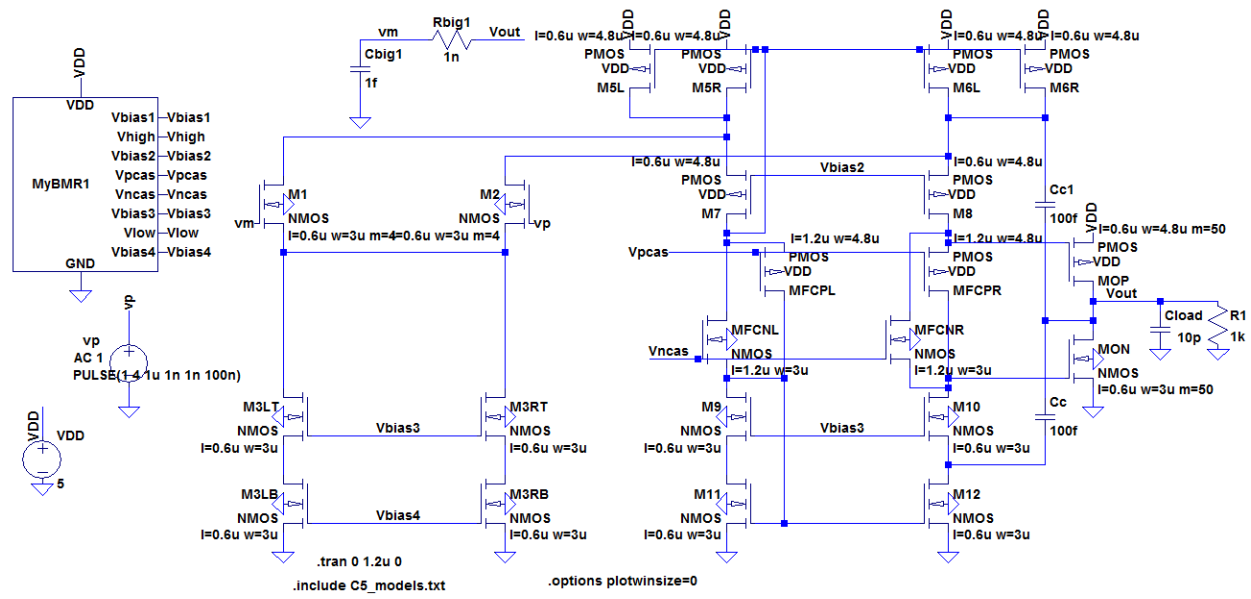


Schem. 20 - % Error Difference

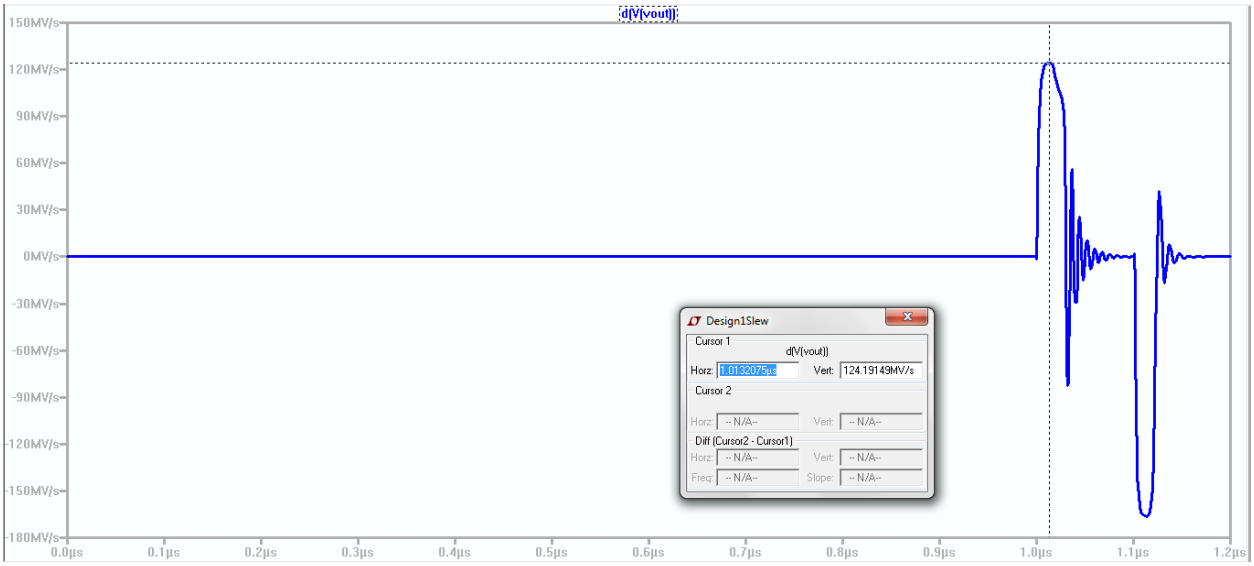


Sim. 20 % - Error Difference

Schem. 21 and **Sim. 21** show the slew rate of the output by plotting the derivative of the output voltage (deriv(vout)). **Sim. 21** shows the slew rate for Design 1 is 124.2MV/s=124.2V/us.

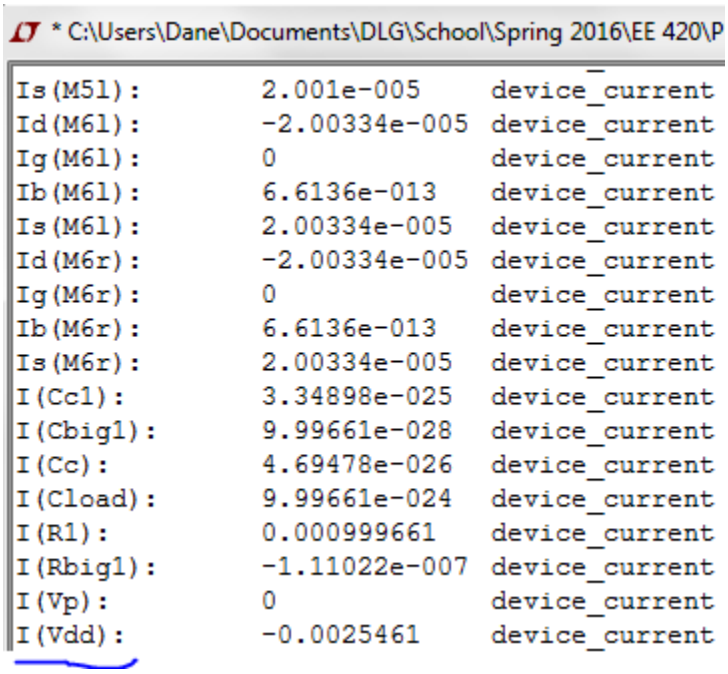


Schem. 21 – Slew Rate



Sim. 21 – Slew Rate=124.2MV/s=124.2V/us

Sim. Design 1 .op shows the total current draw from VDD for Design 1 as I(VDD)=2.55mA.



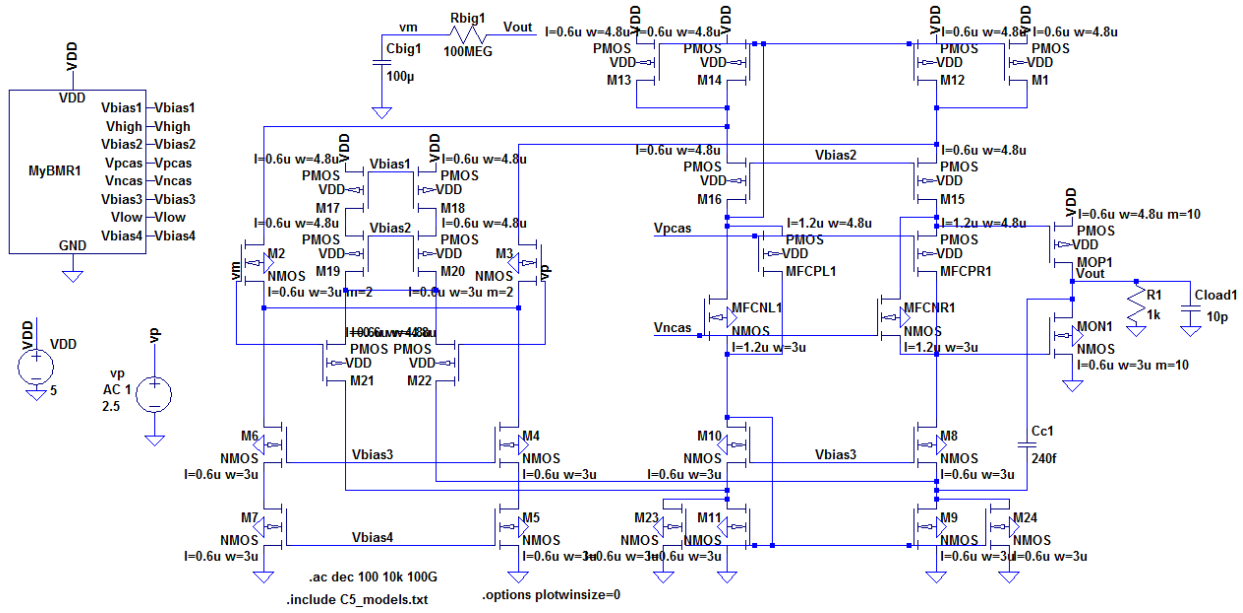
* C:\Users\Dane\Documents\DLG\School\Spring 2016\EE 420\P

Is(M5l):	2.001e-005	device_current
Id(M6l):	-2.00334e-005	device_current
Ig(M6l):	0	device_current
Ib(M6l):	6.6136e-013	device_current
Is(M6l):	2.00334e-005	device_current
Id(M6r):	-2.00334e-005	device_current
Ig(M6r):	0	device_current
Ib(M6r):	6.6136e-013	device_current
Is(M6r):	2.00334e-005	device_current
I(Cc1):	3.34898e-025	device_current
I(Cbig1):	9.99661e-028	device_current
I(Cc):	4.69478e-026	device_current
I(Cload):	9.99661e-024	device_current
I(R1):	0.000999661	device_current
I(Rbig1):	-1.11022e-007	device_current
I(Vp):	0	device_current
I(Vdd):	-0.0025461	device_current

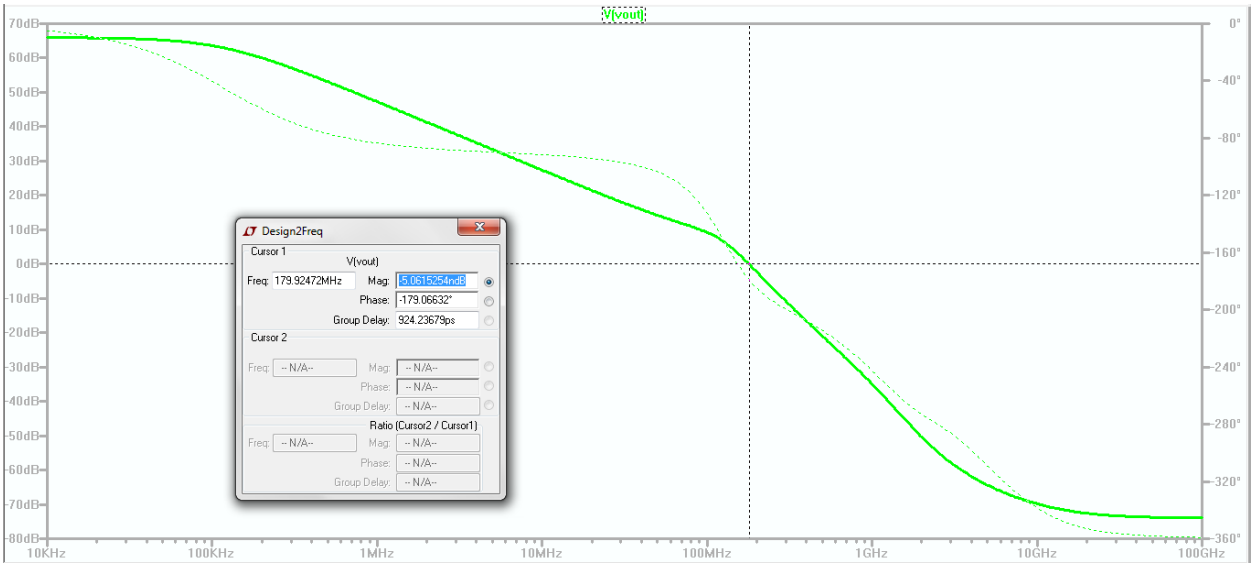
Sim. Design 1 .op – Total Current Draw from VDD

Voltage Follower: Design 2

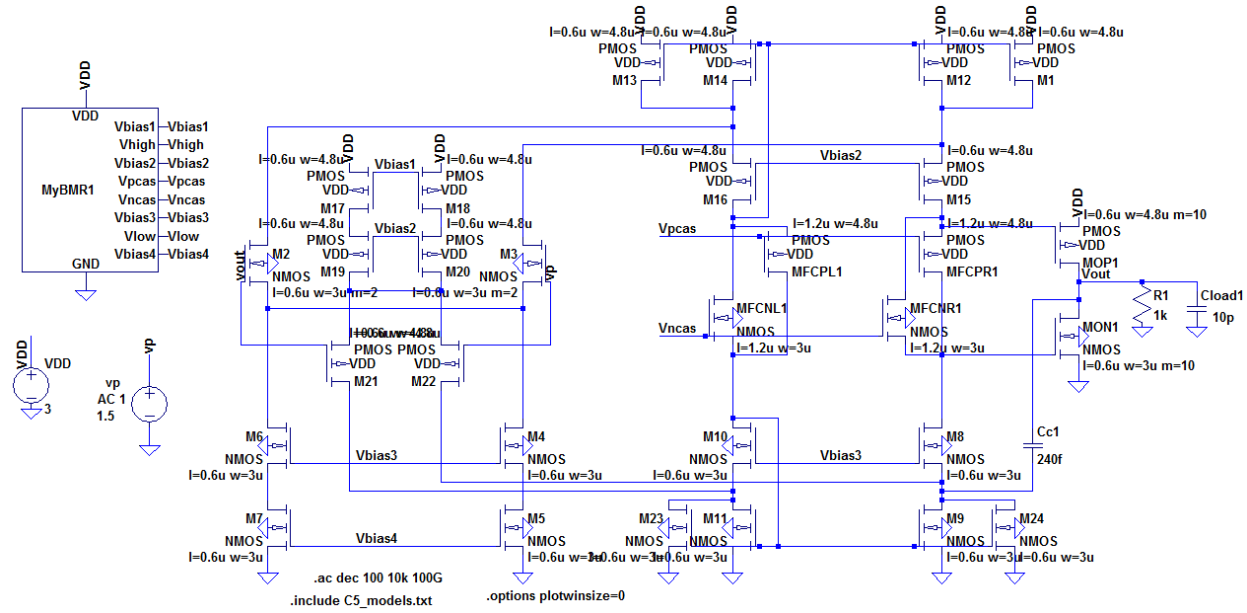
The op-amp design in Fig. 20.48 from the CMOSedu book was used as a starting point for the design of the voltage follower for Design 2. Except for a few different sized devices, all the NMOS are 3u/0.6u and the PMOS are 4.8u/0.6u. The width of the NMOS diff-pair is increased by setting m=2 for both the NMOS in the NMOS diff-pair. The NMOS and PMOS on the output act as a push-pull amplifier, and their widths are each increased by setting m=10. **Sim. 22** corresponding to **Schem. 22** shows the unity gain frequency at 0dB and gives f_{un}=179.9MHz.



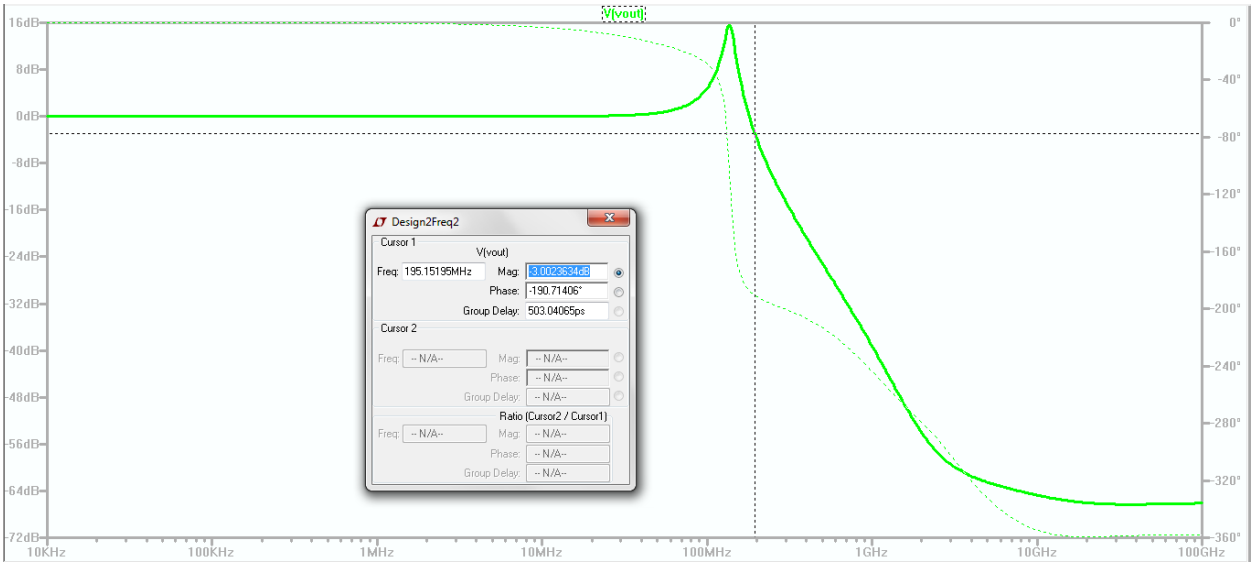
Schem. 22 – Frequency Response



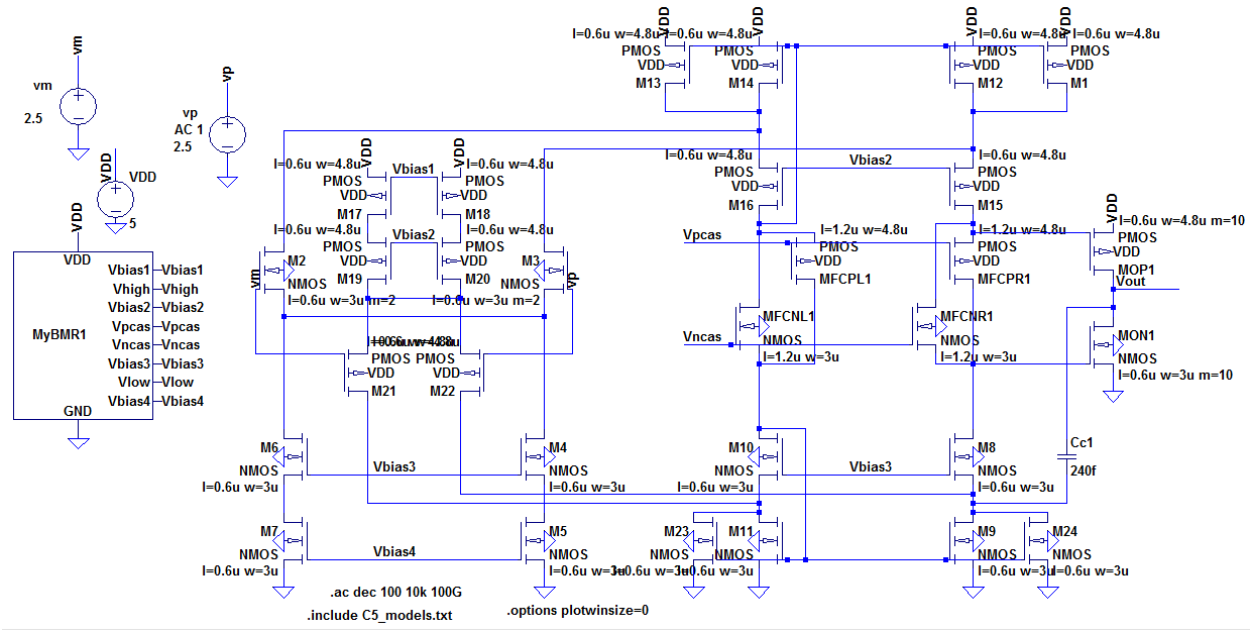
Sim. 22 – Frequency Response(f_{un}=179.9MHz)



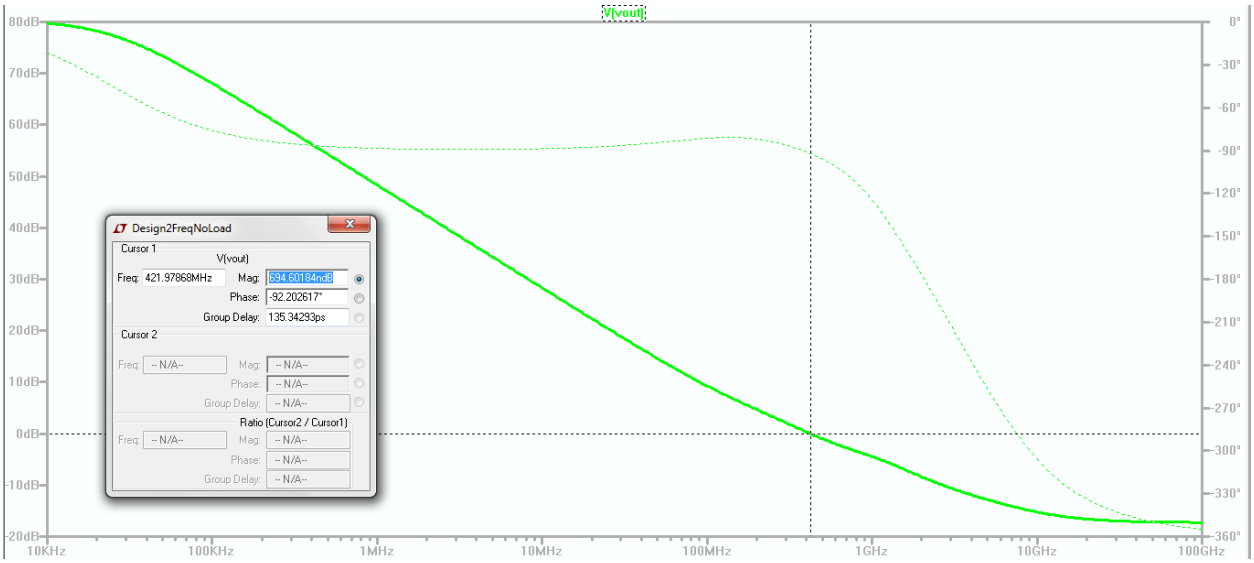
Schem. 23 – Frequency Response



Sim. 23 – Frequency Response

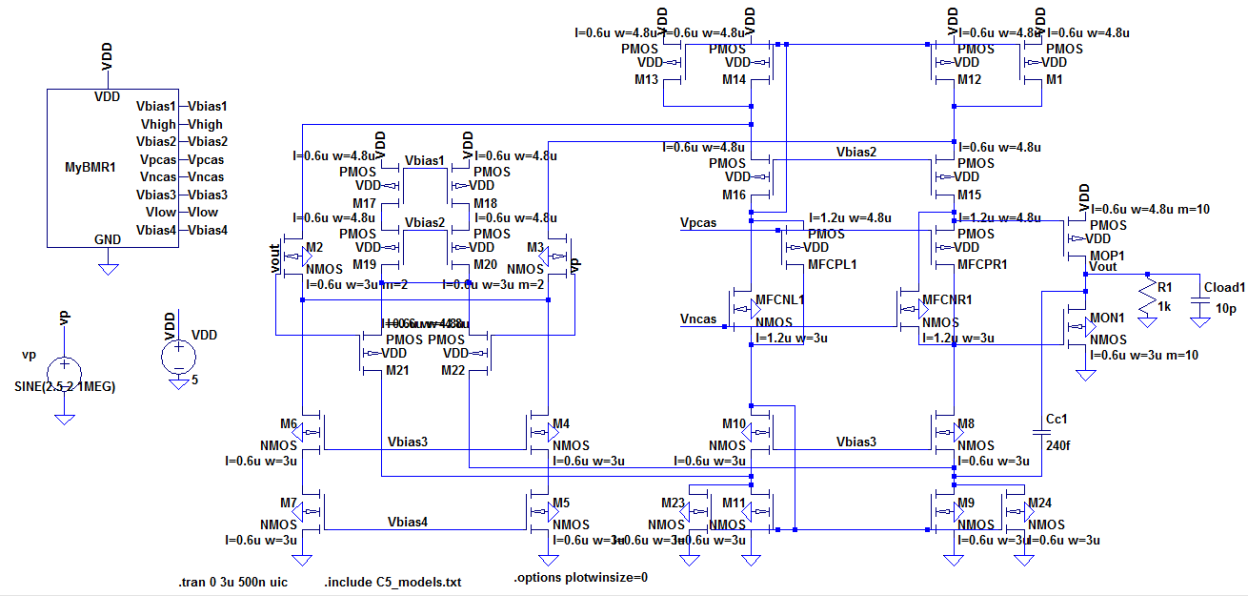


Schem. 24 – Frequency Response

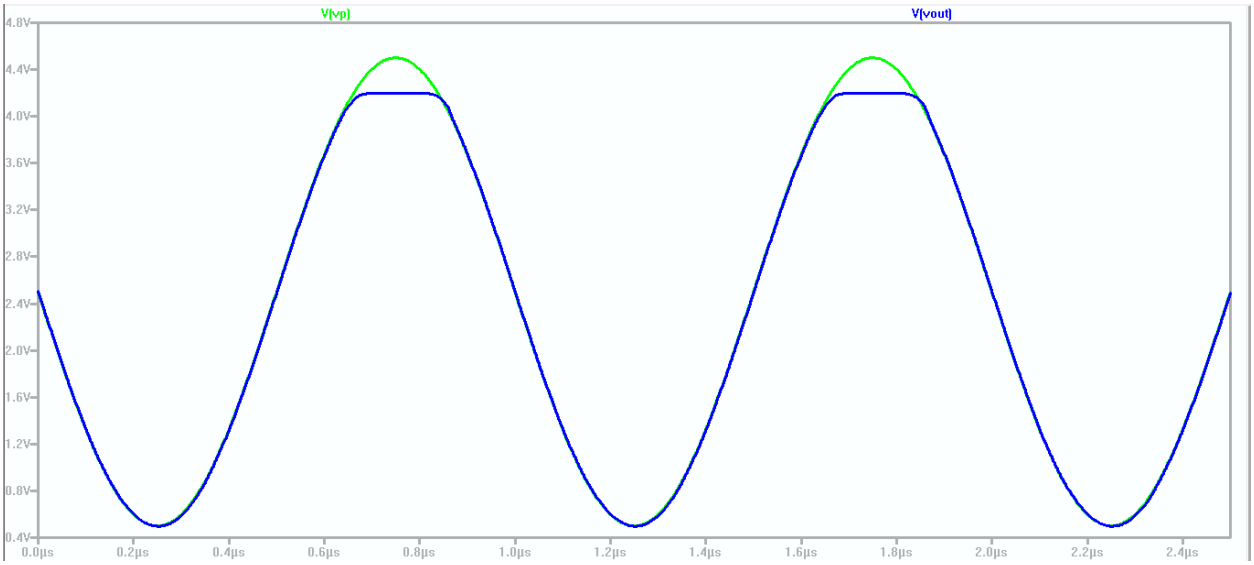


Sim. 24 – Frequency Response

Schem. 25 and the corresponding **Sim. 25** show the output swing of voltage follower for Design 2.



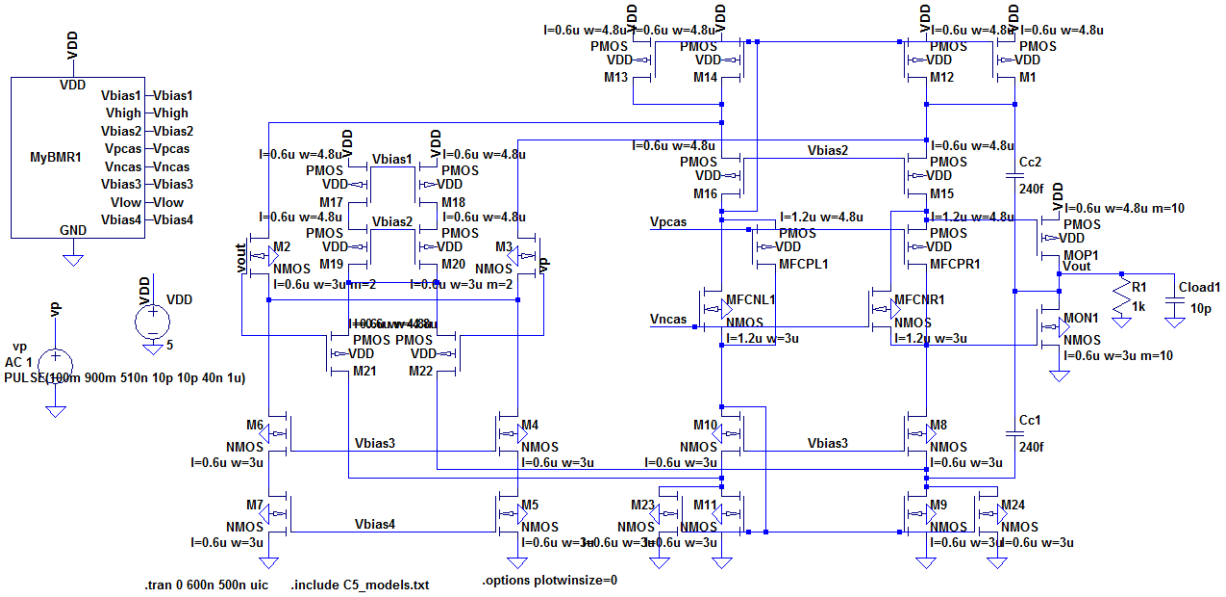
Schem. 25 – Output Swing



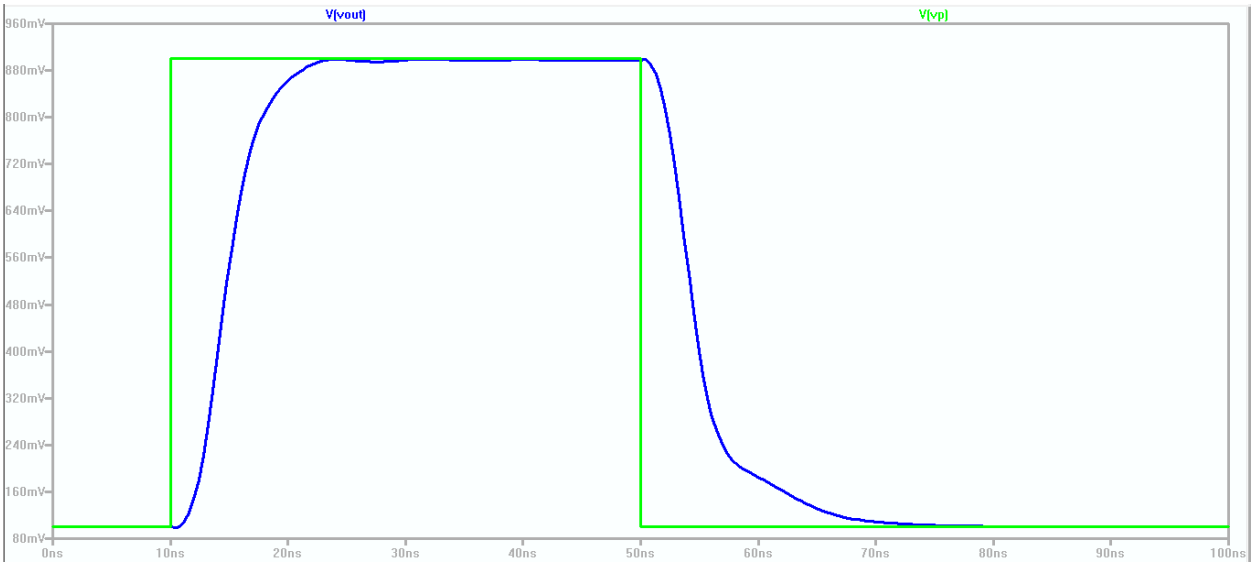
Sim. 25 – Output Swing

Schem. 26 and **Sim. 26** shows a pulse input and the corresponding output. This is used to calculate the percent error difference as ((Vin-Vout)/(Vin+Vout))*100. The percent error difference for Design 1 can then be calculated from **Sim. 26** as ((0.9-0.8973)/(0.9+0.8973))*100 = 0.15%.

⇨ % Error = 0.15%.

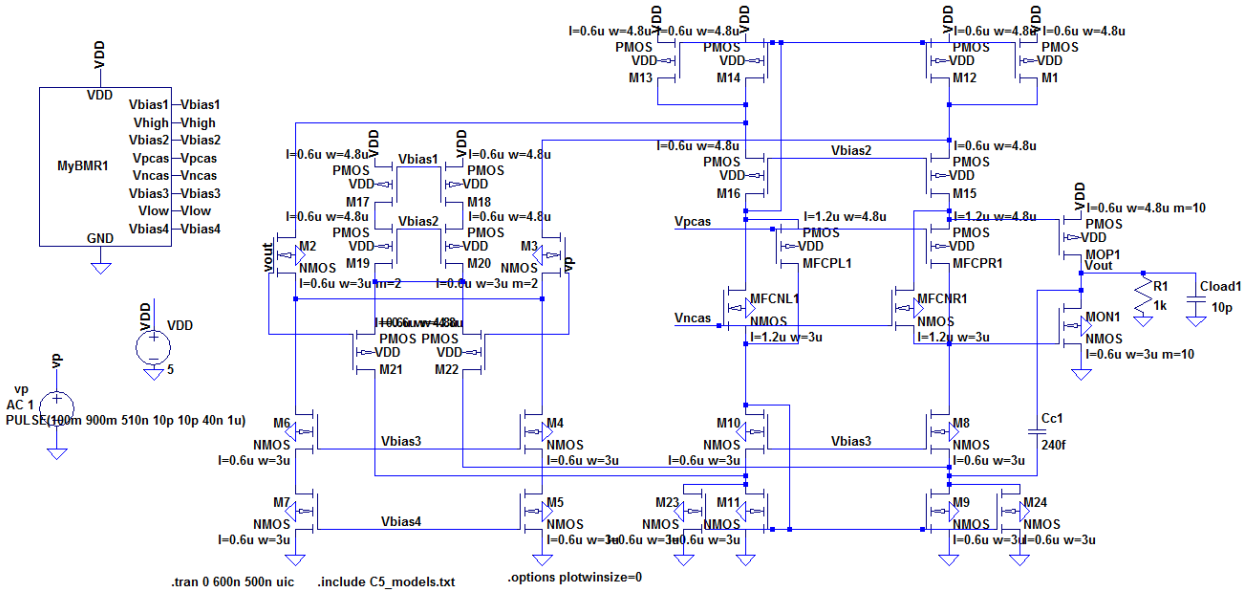


Schem. 26 - % Error Difference

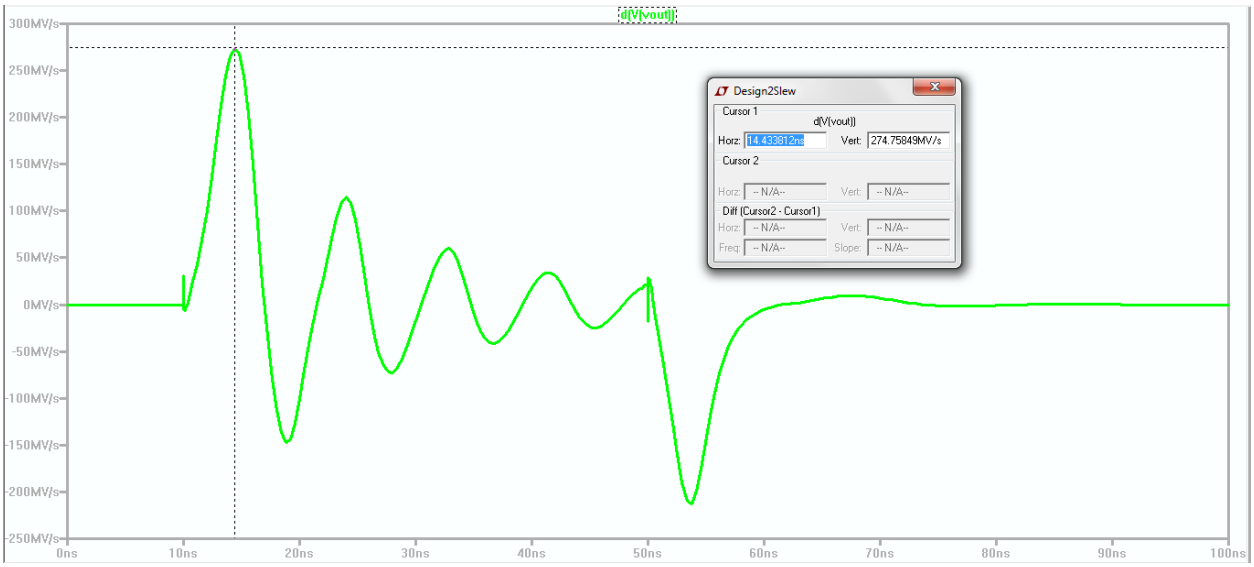


Sim. 26 - % Error Difference=0.15%

Schem. 27 and **Sim. 27** show the slew rate of the output by plotting the derivative of the output voltage (deriv(vout)). **Sim. 27** shows the slew rate for Design 2 is 274.8MV/s=274.8V/us.

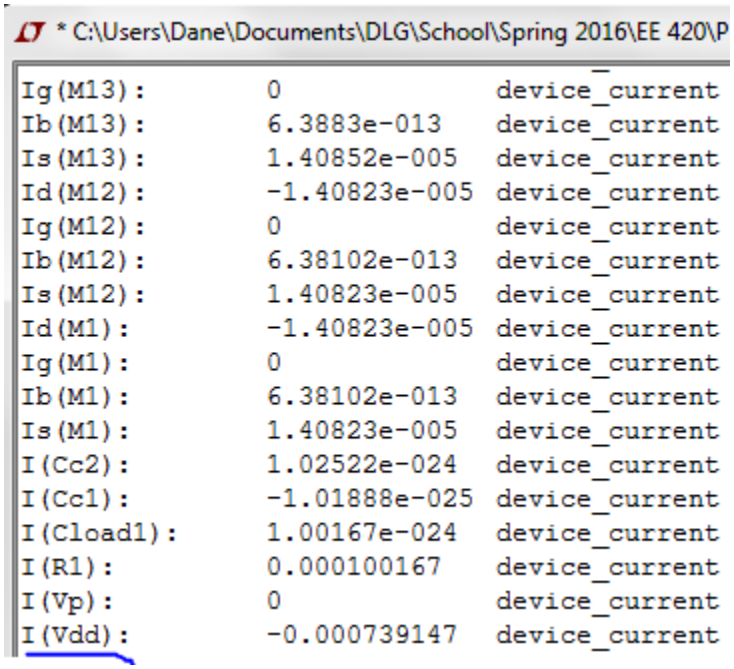


Schem. 27 – Slew Rate



Sim. 27 – Slew Rate=274.8MV/s=274.8V/us

Sim. Design 2 .op shows the total current draw from VDD for Design 2 as I(VDD)=739uA.



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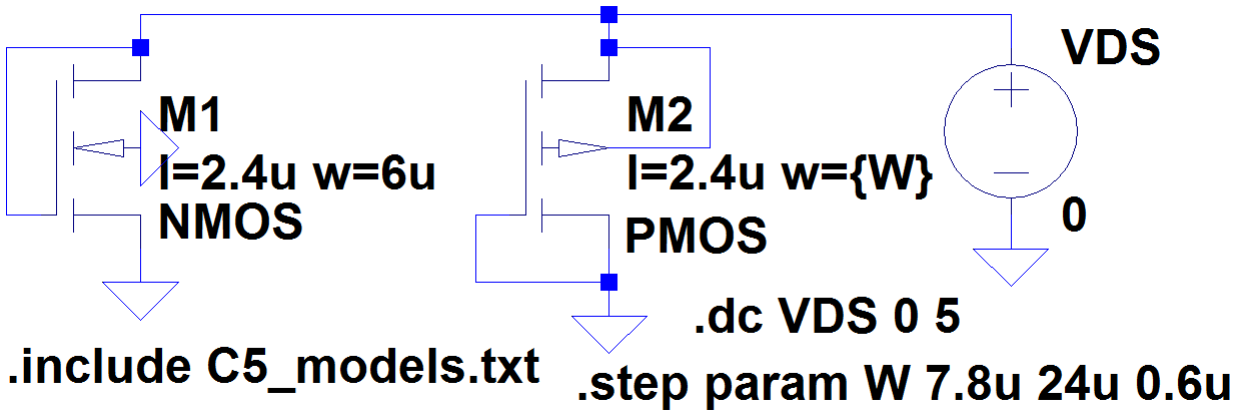
Ig(M13):	0	device_current
Ib(M13):	6.3883e-013	device_current
Is(M13):	1.40852e-005	device_current
Id(M12):	-1.40823e-005	device_current
Ig(M12):	0	device_current
Ib(M12):	6.38102e-013	device_current
Is(M12):	1.40823e-005	device_current
Id(M1):	-1.40823e-005	device_current
Ig(M1):	0	device_current
Ib(M1):	6.38102e-013	device_current
Is(M1):	1.40823e-005	device_current
I(Cc2):	1.02522e-024	device_current
I(Cc1):	-1.01888e-025	device_current
I(Cload1):	1.00167e-024	device_current
I(R1):	0.000100167	device_current
I(Vp):	0	device_current
I(Vdd):	-0.000739147	device_current

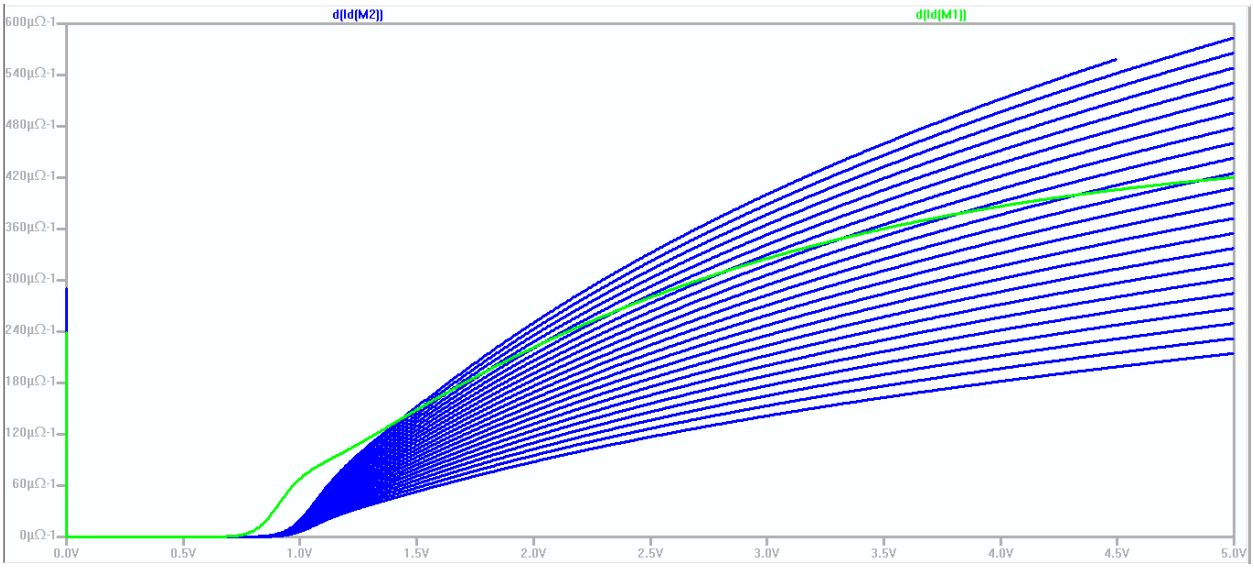
Sim. Design 2 .op – Total Current Draw from VDD

Voltage Follower: Design 3

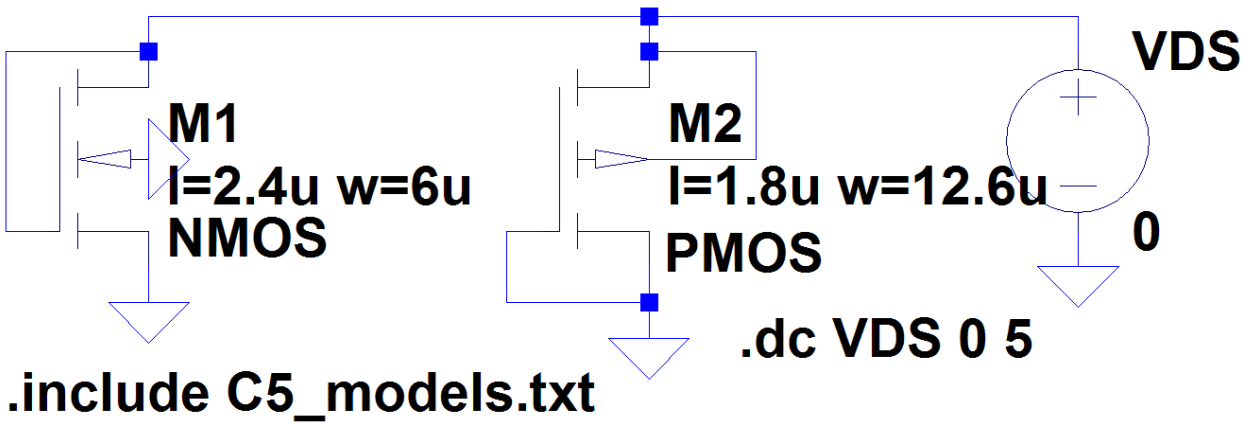
The op-amp design in Fig. 20.48 from the CMOSedu book was used as a starting point for the design of the voltage follower for Design 3. The use of minimum sizes (Lmin=0.6um, Wmin=3um) in Design 1 and Design 2 resulted in poor performance in certain aspects and did not meet all the required specifications due to certain characteristics related to minimum sizing including low gain. Design 3 was implemented by choosing the NMOS size to be 6u/2.4u. Matching the transconductances of a 6u/2.4u NMOS to a PMOS with a length of 1.8u is shown in **Schem. 28** and **Sim. 28** in which the width of the PMOS is stepped to determine what width of the PMOS gives the best matching of transconductances. **Schem 29** and **Sim. 29** show the PMOS width should be chosen to be 12.6u.



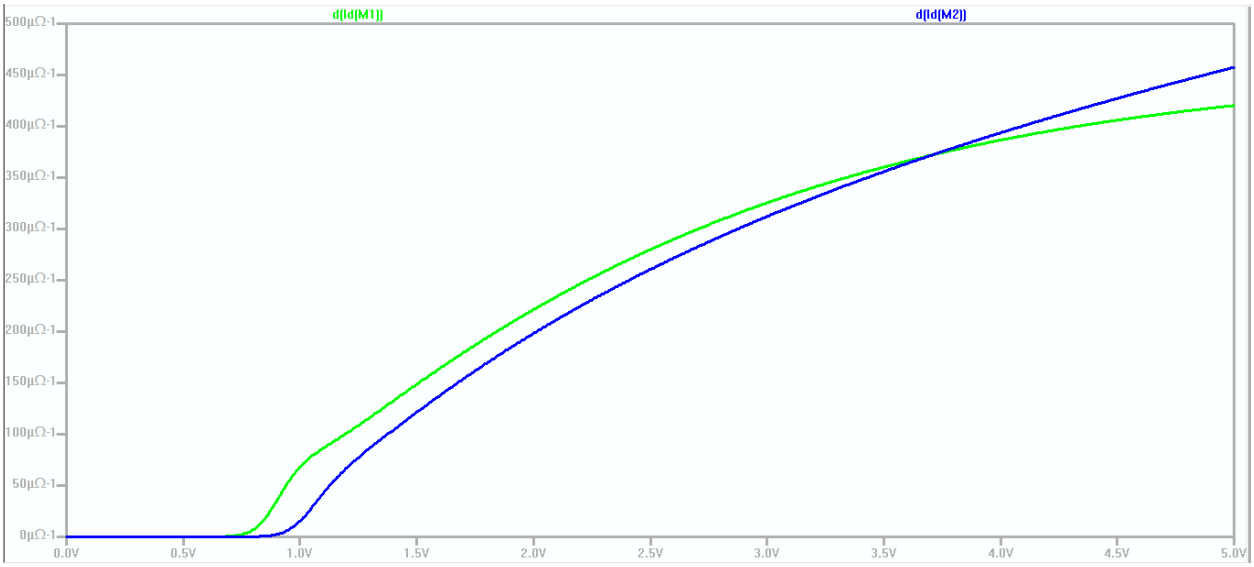
Schem. 28 - Matching NMOS & PMOS Transconductances (g_{mn} & g_{mp})



Sim. 28 - Matching NMOS & PMOS Transconductances (g_{mn} & g_{mp})

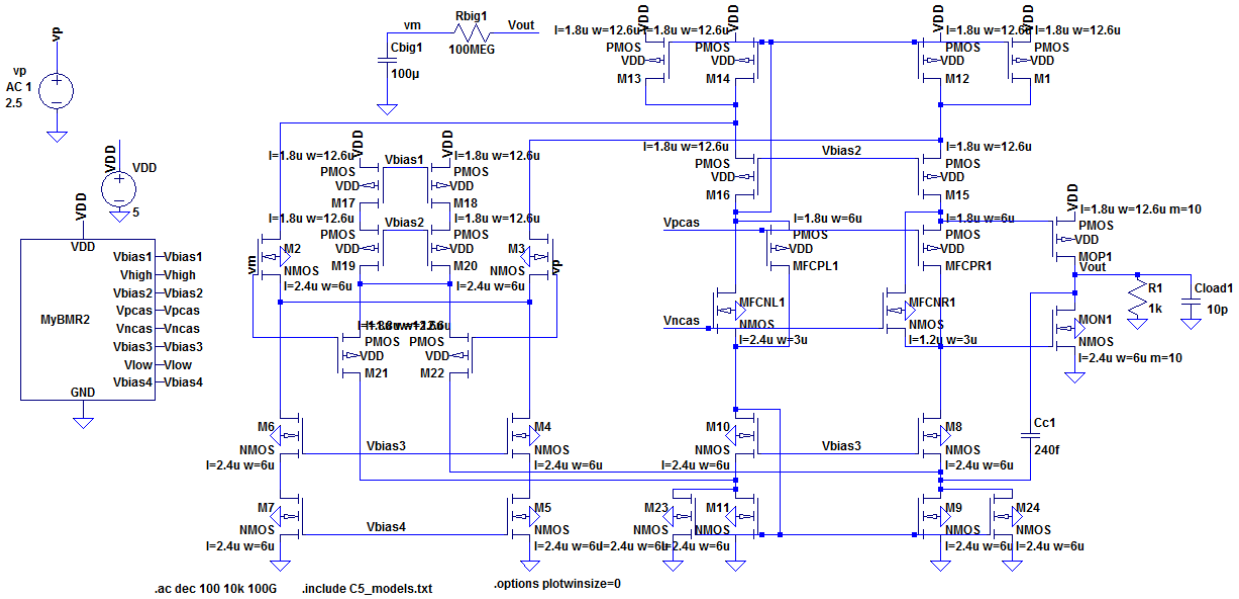


Schem. 29 - Matching NMOS & PMOS Transconductances (g_{mn} & g_{mp}) (W_{PMOS}=12.6u)

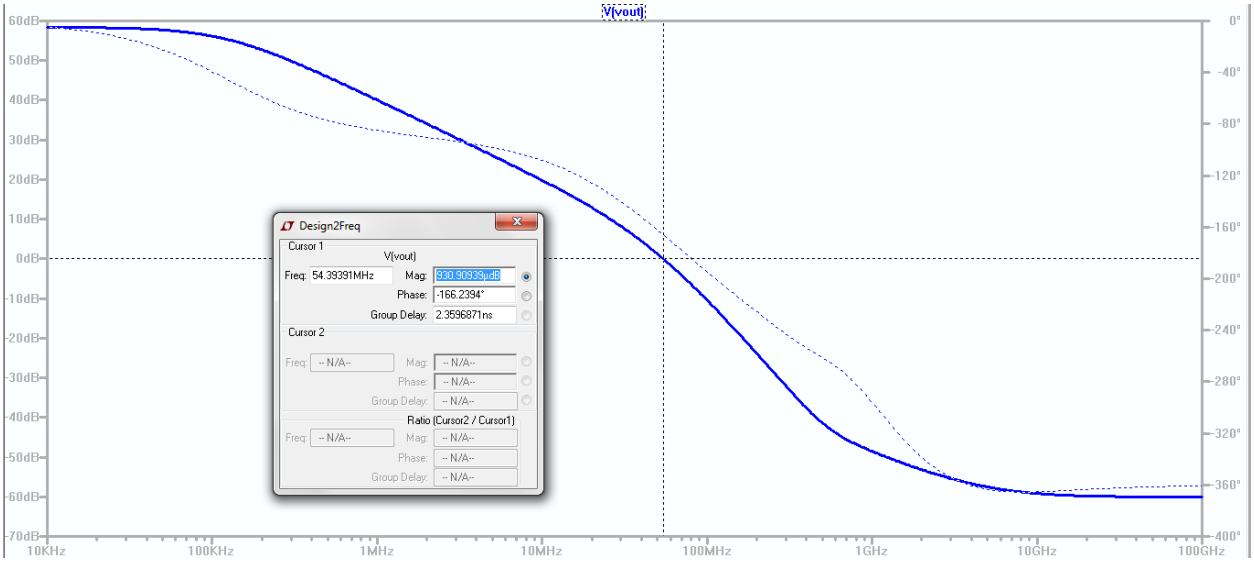


Sim. 29 - Matching NMOS & PMOS Transconductances (g_{mn} & g_{mp}) (W_{PMOS}=12.6u)

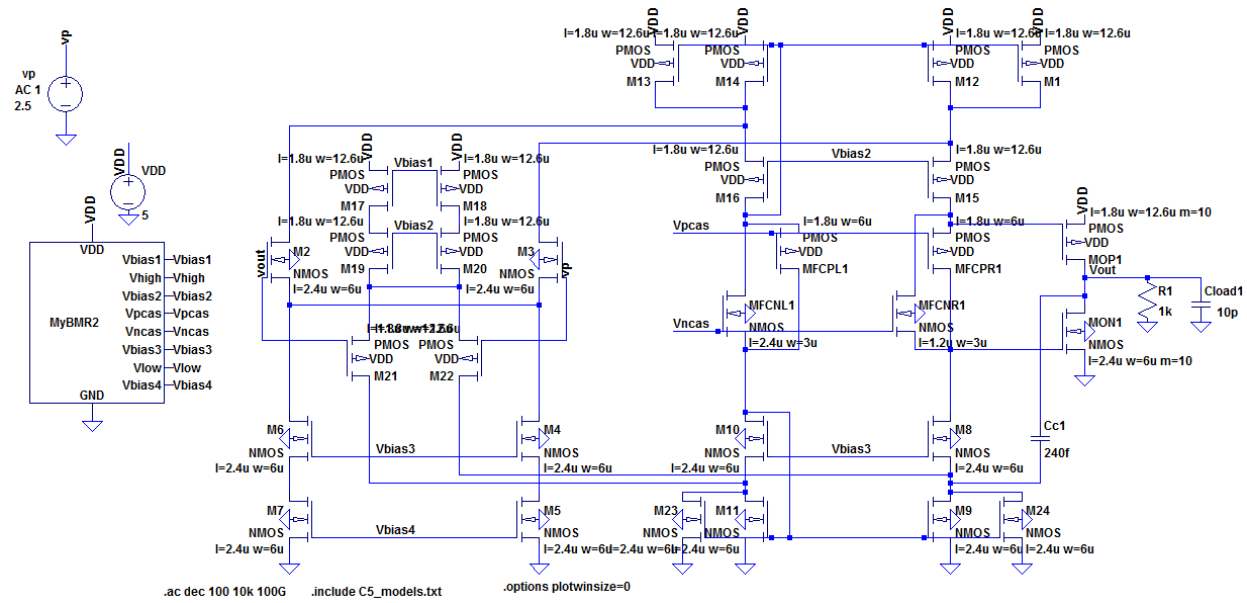
Except for a few different sized devices, Design 3 was implemented with all the NMOS sized as 6u/2.4u and the PMOS sized as 12.6u/1.8u. The width of the NMOS diff-pair is increased by setting m=2 for both the NMOS in the NMOS diff-pair. The NMOS and PMOS on the output act as a push-pull amplifier, and their widths are each increased by setting m=10. **Sim. 29** corresponding to **Schem. 29** shows the unity gain frequency at 0dB and gives f_{un}=54.4MHz.



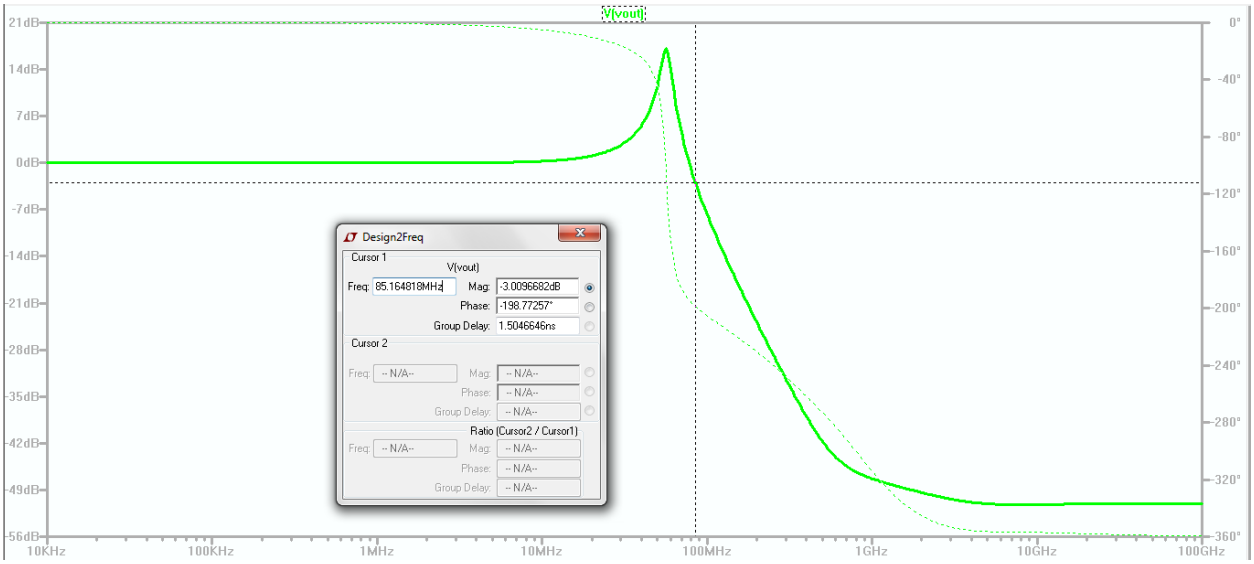
Schem. 30 – Frequency Response



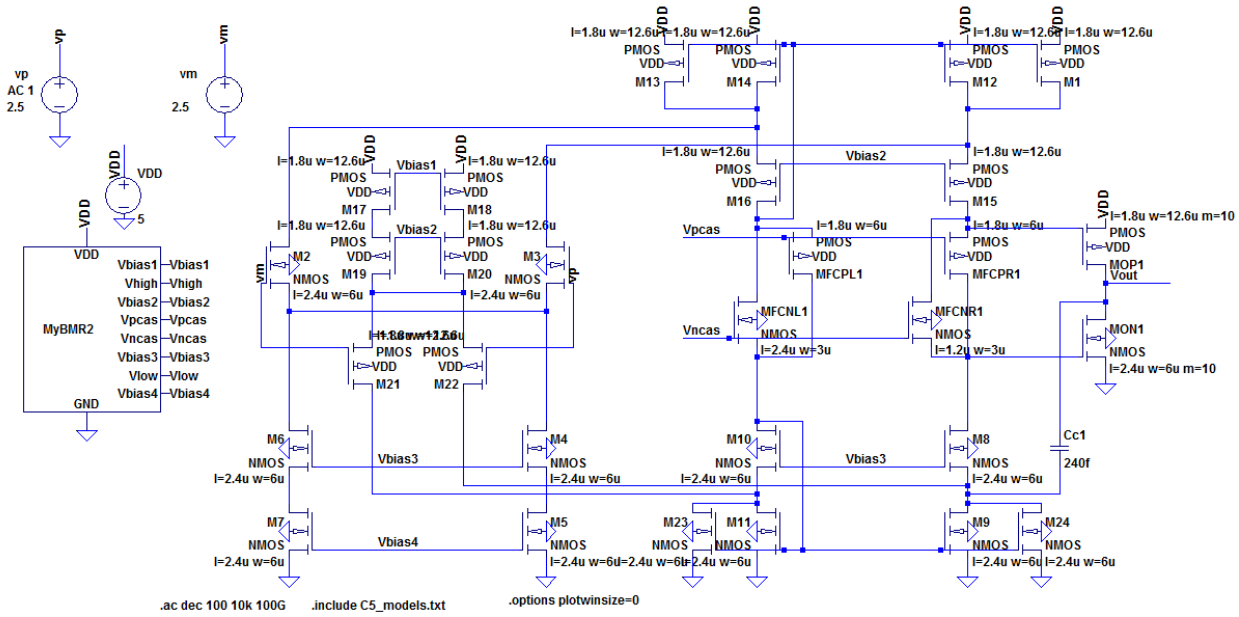
Sim. 30 – Frequency Response (f_{un}=54.4MHz)



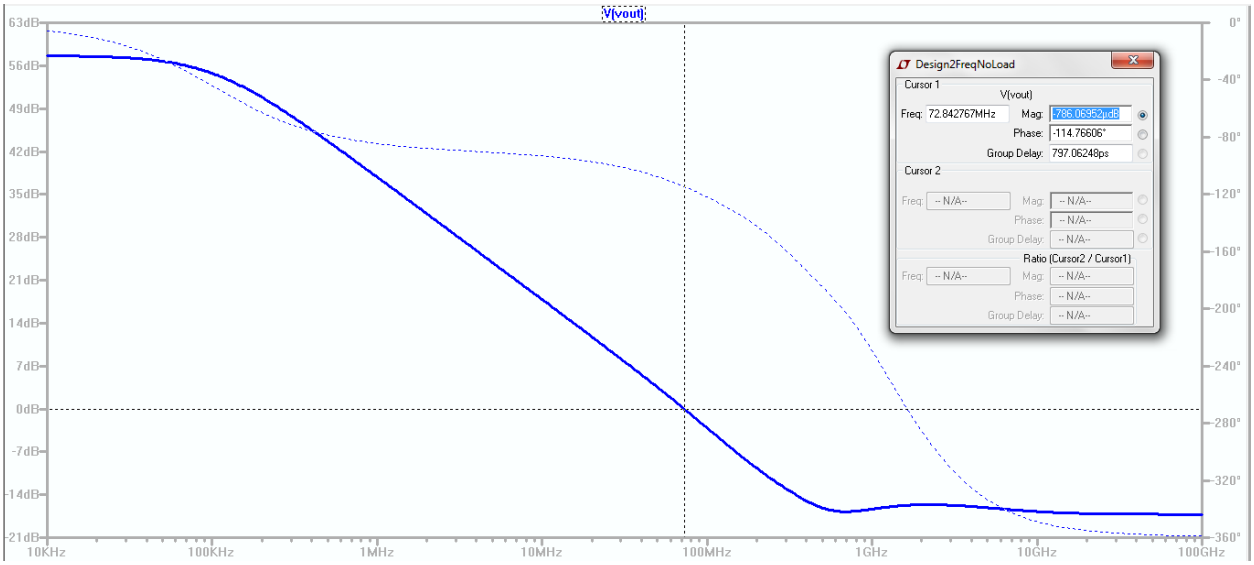
Schem. 31 – Frequency Response



Sim. 31 – Frequency Response

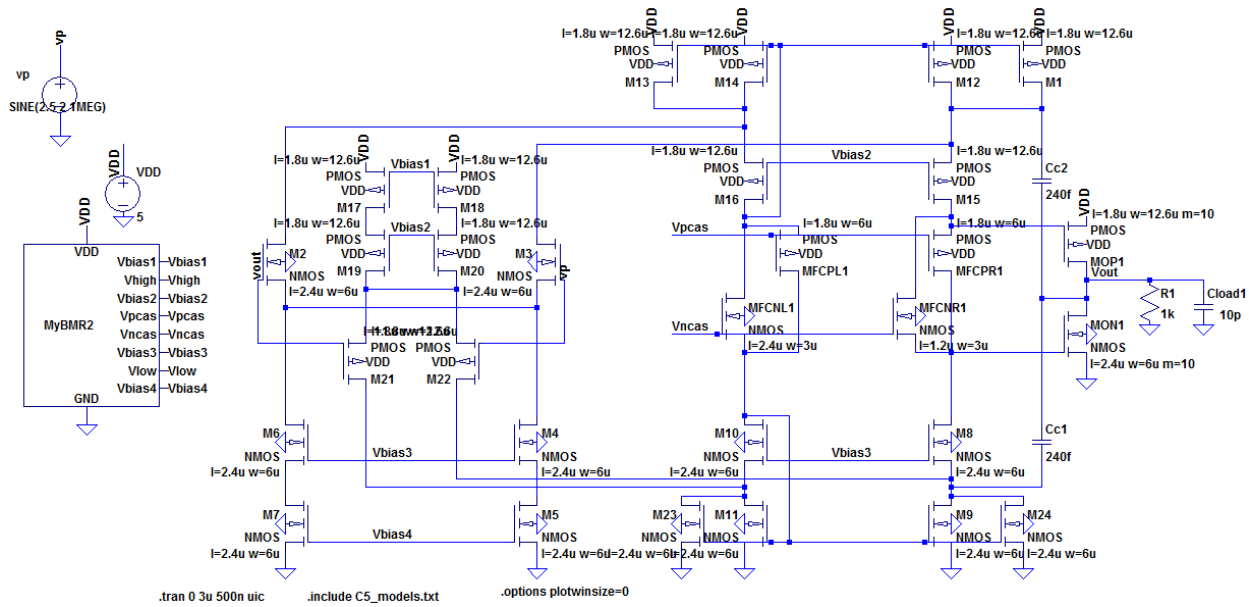


Schem. 32 – Frequency Response

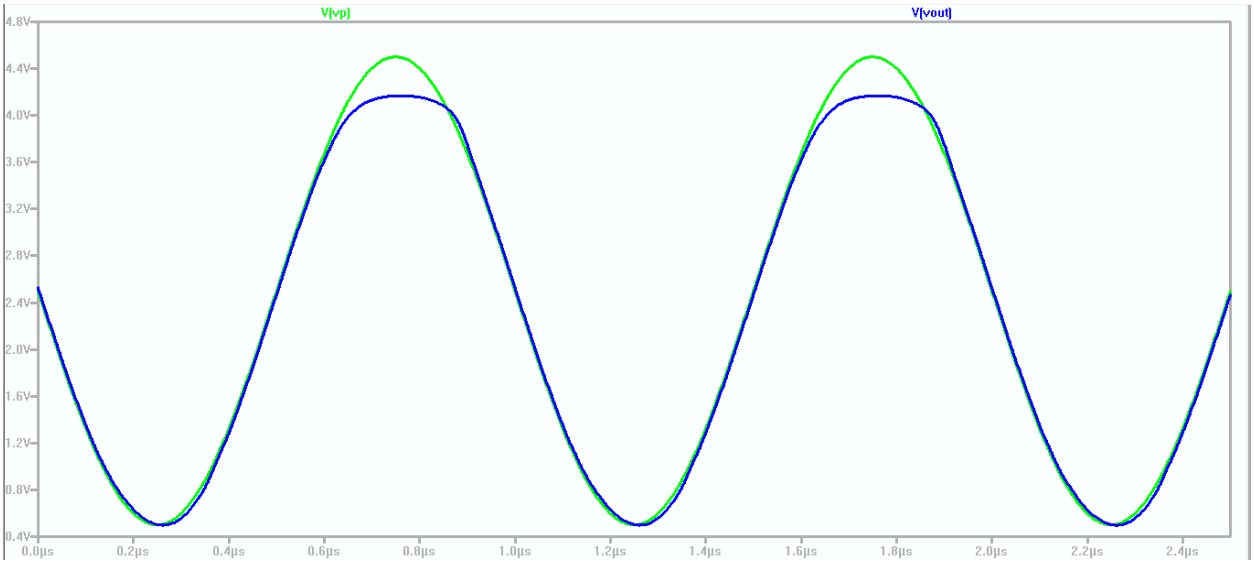


Sim. 32 – Frequency Response

Schem. 33 and the corresponding **Sim. 33** show the output swing of voltage follower for Design 3.



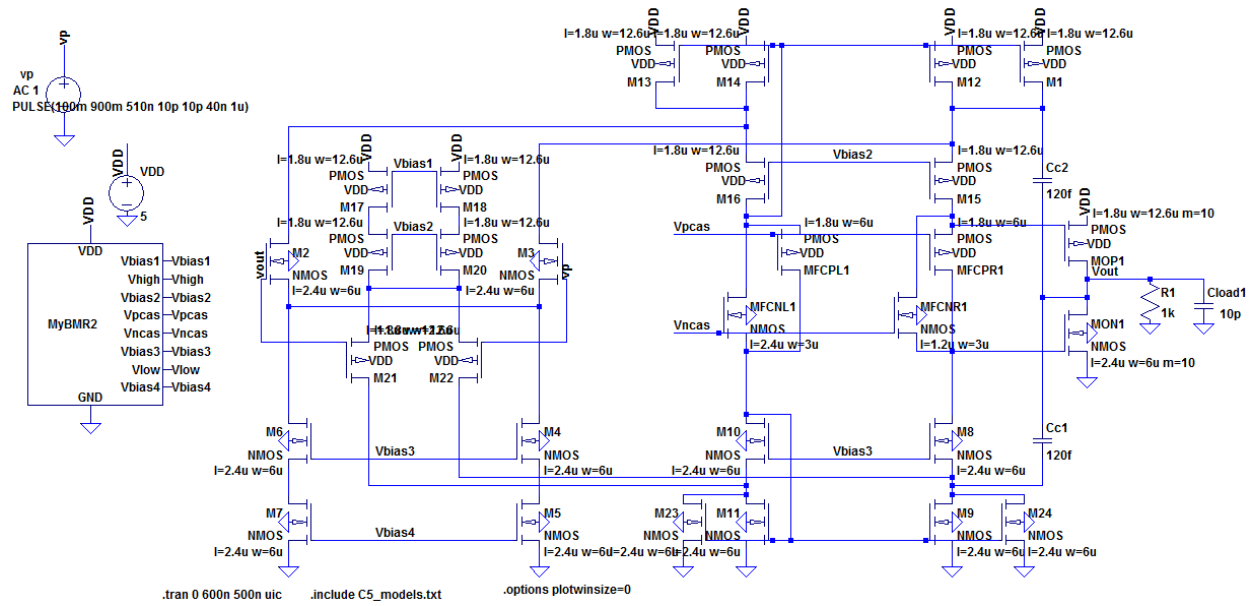
Schem. 33 – Output Swing



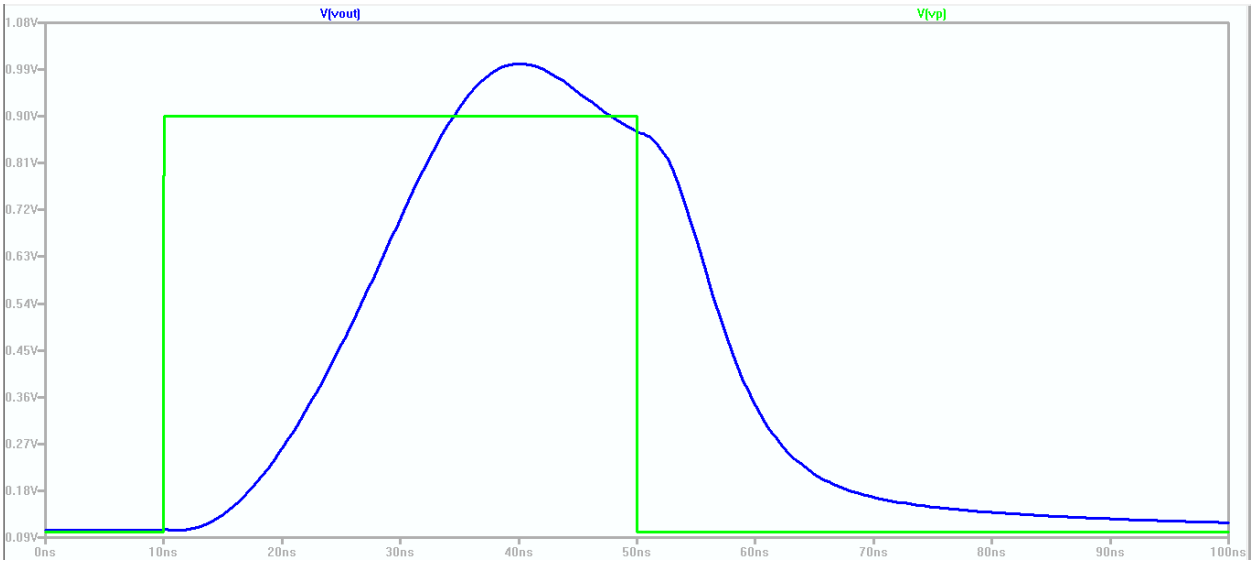
Sim. 33 – Output Swing

Schem. 34 and **Sim. 34** shows a pulse input and the corresponding output. This is used to calculate the percent error difference as ((Vin-Vout)/(Vin+Vout))*100. The percent error difference for Design 1 can then be calculated from **Sim. 26** as ((1-0.9)/(1+0.9))*100 = 5.26%.

⇨ % Error = 5.26%.

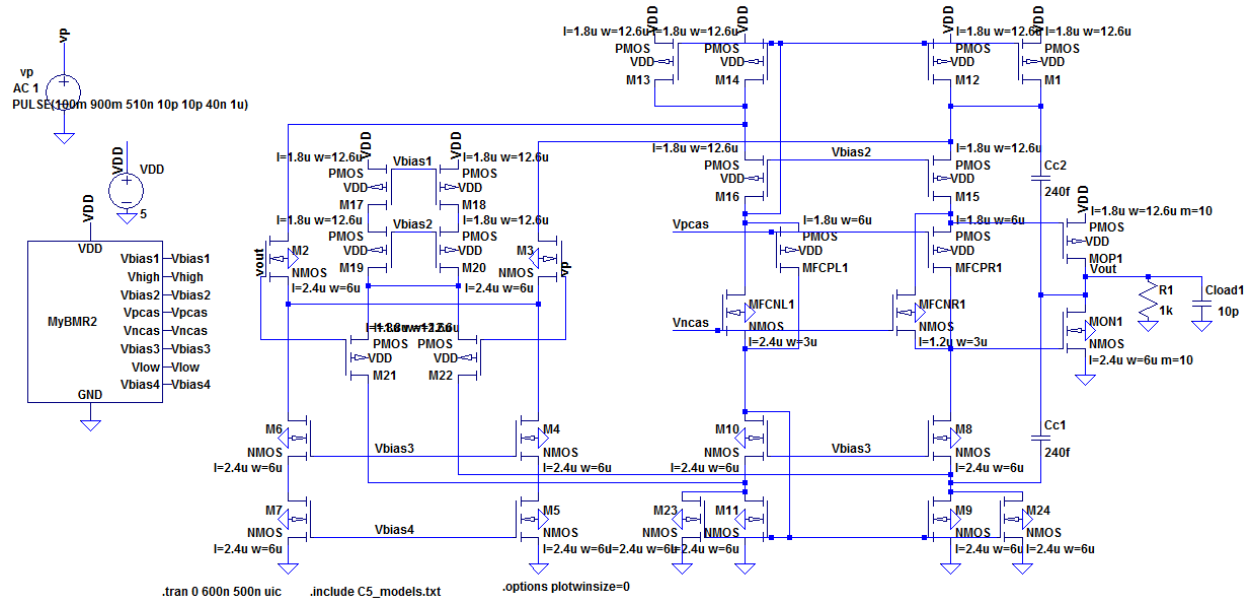


Schem. 34 - % Error Difference

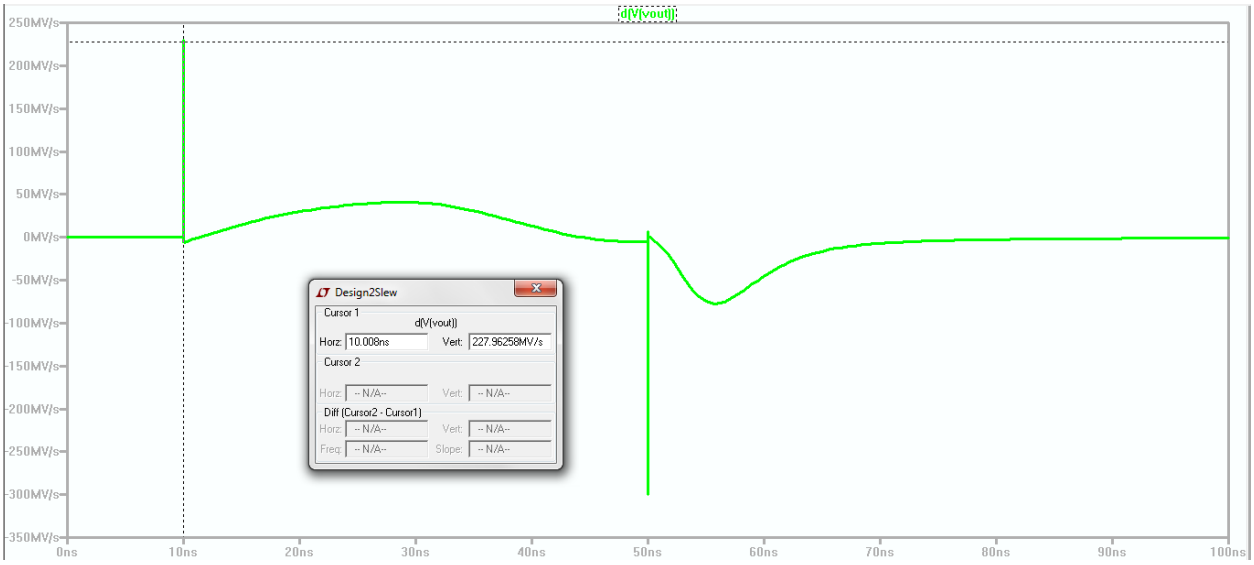


Sim. 34 % - Error Difference=5.26%

Schem. 35 and **Sim. 35** show the slew rate of the output by plotting the derivative of the output voltage (deriv(vout)). **Sim. 35** shows the slew rate for Design 3 is 228.0MV/s=228.0V/us.

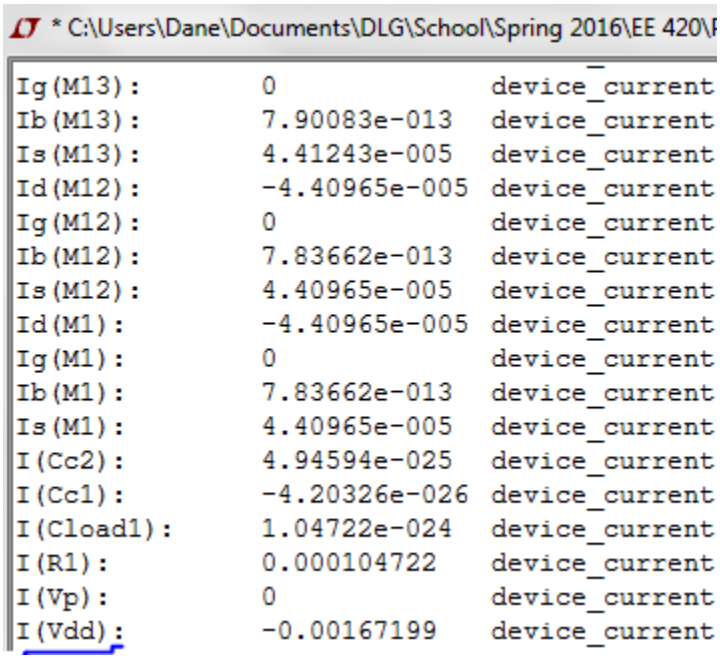


Schem. 35 – Slew Rate



Sim. 35 – Slew Rate=228.0MV/s=228.0V/us

Sim. Design 3 .op shows the total current draw from VDD for Design 3 as I(VDD)=1.67mA.



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Ig(M13):	0	device_current
Ib(M13):	7.90083e-013	device_current
Is(M13):	4.41243e-005	device_current
Id(M12):	-4.40965e-005	device_current
Ig(M12):	0	device_current
Ib(M12):	7.83662e-013	device_current
Is(M12):	4.40965e-005	device_current
Id(M1):	-4.40965e-005	device_current
Ig(M1):	0	device_current
Ib(M1):	7.83662e-013	device_current
Is(M1):	4.40965e-005	device_current
I(Cc2):	4.94594e-025	device_current
I(Cc1):	-4.20326e-026	device_current
I(Cload1):	1.04722e-024	device_current
I(R1):	0.000104722	device_current
I(Vp):	0	device_current
I(Vdd):	-0.00167199	device_current

Sim. Design 3 .op – Total Current Draw from VDD

Table Summary of Design Results

Table 4 summarizes some important performance information for the three designs

	Design 1	Design 2	Design 3
f_{un}	145.9MHz	179.9MHz	54.4MHz
% Error	0.012%	0.15%	5.26%
Slew Rate	124.2V/us	274.8V/us	228.0V/us
Current Draw from VDD	2.55mA	739uA	1.67mA

Table 4 – Performance of the three designs

Conclusion

Of the three designs included in this report, the first design (Design 1) performed the best as it was closest to the required specifications, though it did not meet every specification. Design 2 had the largest unity gain frequency while Design 1 had the lowest percent error difference. In addition, Design 2 had the largest slew rate yet lowest total current drawn from VDD while Design 1 had the smallest slew rate and largest total current drawn from VDD. In regard to the simulations presented in this report for each of the three designs, Design 1 seems to have the best overall performance in regard to meeting the required specifications. Much experience and knowledge was gained from this project, and over time I gained a good understanding of the expectations of the project as well as the process necessary in fulfilling these expectations. With more time, I would have continued trying different sizes based on known tradeoffs such as gain and speed in order to get my BMR to have better biasing for my design circuit. I encountered numerous issues throughout the project including designing the overall voltage follower to meet all the design requirements and perform as well as possible, and LTSpice presented a great deal of various problems especially in generating symbols for schematics in a hierarchy, but after much time and frustration, I was able to improve each of my designs. Despite any setbacks, many issues were overcome with time and yielded a better knowledge of LTSpice and circuit design in general. Having successfully completed this course project has certainly resulted in my becoming a more confident and experienced circuit designer as well as engineer.

References

[1] Baker, R. J., CMOS: Circuit Design, Layout, and Simulation, 3rd ed., IEEE Press. John Wiley & Sons Inc. 2010.