CMOS Boost Switching Power Supply in the C5 Process

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1. Introduction

This report contains the design, simulation and layout of a CMOS Boost Switching Power Supply in On Semiconductor's C5 process. The power supply consists of an integrated circuit and three discrete components. The integrated circuit will include feedback control circuitry. The discrete circuitry includes a discrete Schottky diode, inductor, and capacitor. A boost switching power supply (or simply boost SPS) is a DC-DC converter that steps up a DC voltage. Or in

other words, an input voltage, v, is boosted to an output voltage of $v \cdot m$. Where m represents the factor by which the input voltage is stepped up. The power supply is expected to be powered by a *VDD* that can vary from 3.75 to 5.25V. The power supply is expected to generate a constant output voltage, *Vout*, of 7.5V for load currents ranging from 0 to 20mA.

2. Summary of Performance

Varying Temperature

Load Current = 20mA

VDD = 4.5 V

Table 1: Many Parameters Under Varying Temperature

Temp (ºC)	Min. Vout (V)	Avg. Vout (V)	Max. Vout (V)	Ripple (mV)	Avg(I(VDD)) (mA)	Efficiency (%)
0	7.501	7.505	7.509	8.561	38.32	87.26
20	7.497	7.503	7.508	11.097	37.80	88.18
40	7.490	7.492	7.494	4.196	37.59	88.68
60	7.480	7.483	7.486	5.523	37.36	89.22
80	7.468	7.471	7.474	6.471	37.42	89.08
100	7.455	7.460	7.464	8.165	37.05	89.97

Table 2: Averages of Each Column in Table 1

	Min. Vout (V)	Avg. Vout (V)	Max. Vout (V)	Ripple (mV)	Avg(I(VDD)) (mA)	Efficiency (%)
Average	7.482	7.486	7.489	7.336	37.59	88.73

Varying VDD

Load Current = 20mA

Temperature = 27ºC

Table 3: Many Parameters Under Varying VDD

VDD (V)	Min. Vout (V)	Avg. Vout (V)	Max. Vout (V)	Ripple (mV)	Avg(I(VDD)) (mA)	Efficiency (%)
3.75	7.484	7.487	7.493	9.137	44.65	89.59
4.00	7.489	7.491	7.499	10.170	41.82	89.67
4.25	7.492	7.494	7.495	3.207	39.55	89.24
4.50	7.495	7.497	7.498	3.425	37.80	88.18
4.75	7.497	7.500	7.501	3.674	36.00	87.72
5.00	7.499	7.501	7.503	3.960	34.64	86.61
5.25	7.499	7.501	7.503	4.250	33.52	85.20

Table 4: Averages of Each Column in Table 3

	Min. Vout (V)	Avg. Vout (V)	Max. Vout (V)	Ripple (mV)	Avg(I(VDD)) (mA)	Efficiency (%)
Average	7.494	7.496	7.499	5.403	38.28	88.03

Varying Load

VDD = 4.5V

Temperature = 27ºC

According to the design requirements, the boost SPS system must be able to provide 7.5V to the load varying from 0-20mA. However, what happens if the load exceeds 20mA? The rows in Table 5 that are highlighted in grey are loads that exceed the maximum load requirement specified by the design requirements. The design continues to work at greater current loads, but the ripple voltage considerably increases.

Table 5: Many Parameters Under Varying VDD

Load (mA)	Min. Vout (V)	Avg. Vout (V)	Max. Vout (V)	Ripple (mV)	Avg(I(VDD)) (mA)	Efficiency (%)
0	7.497	7.500	7.502	5.537	1.98	N/A
2.5	7.497	7.499	7.502	5.258	6.30	66.14
5	7.496	7.499	7.501	4.801	10.97	75.96
7.5	7.496	7.499	7.501	4.656	15.75	79.21
10	7.496	7.498	7.500	4.432	19.94	83.58
12.5	7.496	7.498	7.500	4.166	24.08	86.52
15	7.496	7.498	7.500	3.911	28.32	88.28
17.5	7.495	7.497	7.499	3.640	37.77	89.00
20	7.495	7.497	7.498	3.425	37.80	88.18
30	7.493	7.505	7.517	24.07	53.69	93.13
40	7.491	7.509	7.529	38.34	75.00	88.89
50	7.488	7.513	7.543	54.71	95.32	87.42
75	7.478	7.529	7.593	115.13	136.60	91.86
100	7.462	7.553	7.673	211.25	208.8	59.56

Table 6: Averages for Each of the Non-Highlighted Columns in Table 5

	Min. Vout (V)	Avg. Vout (V)	Max. Vout (V)	Ripple (mV)	Avg(I(VDD)) (mA)	Efficiency (%)
Average	7.496	7.498	7.500	4.23	20.32	82.10

3. Design of the Boost SPS System

The boost SPS system contains an integrated circuit and three off chip components that can deliver a stepped-up voltage to a load (refer to Figure 1). The design of the system will be divided into two subsections. The first subsection will involve the design and layout of the boost SPS Integrated Circuit and the second will regard the selection of the three off chip components.

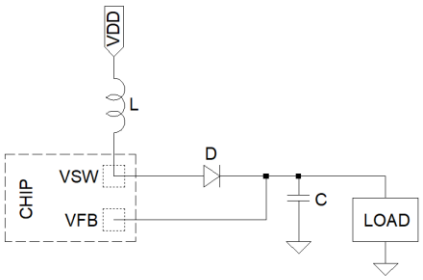

Figure 1: Boost SPS System

3.1 Design and Layout of the Boost SPS Integrated Circuit

The boost SPS integrated circuit provides the system feedback control. The on-chip circuitry includes a resistive voltage divider, bandgap voltage reference, voltage comparator, enabled ring oscillator, large buffer, and a large switching NMOS (see Figure 2). As indicated before, a *VDD* voltage (3.75 to 5.25V), is stepped up to *Vout* of 7.5V. The output of the bandgap voltage reference (BGR) is 1.25V. For feedback control *Vout* is compared to the reference voltage. A 1/6 voltage divider attenuates *Vout* so that it can be compared to the voltage reference. When *Vout* is exactly 7.5V, the output of the voltage divider should be precisely 1.25V. Due to the charging and discharging of the off-chip capacitor, *Vout* varies below and above the intended output voltage. The voltage comparator compares the attenuated *Vout* and the voltage reference. When *Vout* is lower than 7.5V, the output of the comparator is active high. To the contrary, when *Vout* is higher than 7.5V, then the output of the voltage comparator is active low. Simply put, the output of the voltage comparator will either enable or disable the ring oscillator. The ring oscillator has an 80% duty cycle and has a frequency of 1MHz. The output signal of the ring oscillator is buffered so that the signal can drive the input capacitance of the large switching NMOS.

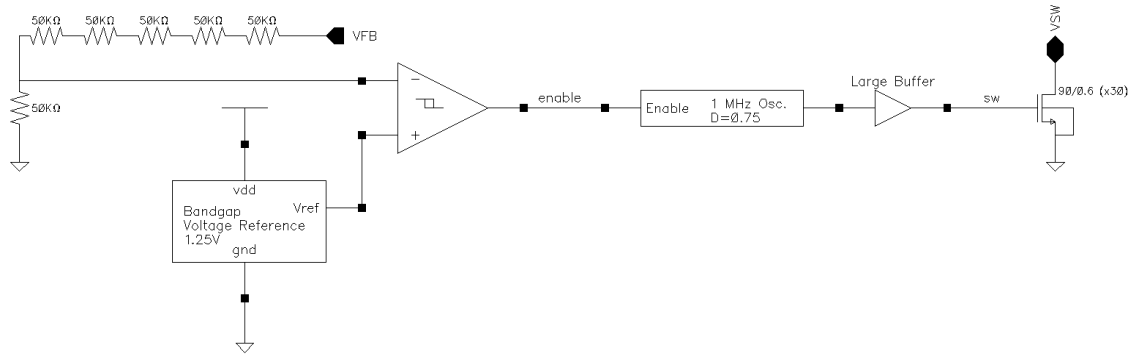

Figure 2: Boost SPS On-Chip Circuitry

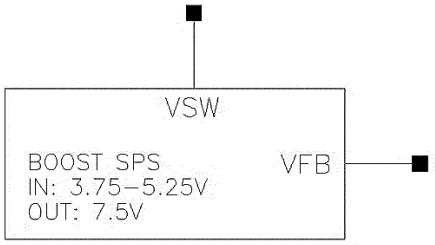

Figure 3: Boost SPS Integrated Circuit Symbol

3.1.1 The Layout

Regarding the layout of the boost SPS IC, a 27µm cell frame will be used throughout all the design except for the layout of the BGR and the large switching NMOS. A cell frame is a module that is of a certain height, such that all circuitry is contained between the NTAP and the PTAP. Cell frames allow one to easily connect modules together while saving layout space. Generally, a power rail is routed across all the NTAPs and a ground rail is routed across all the PTAPs.

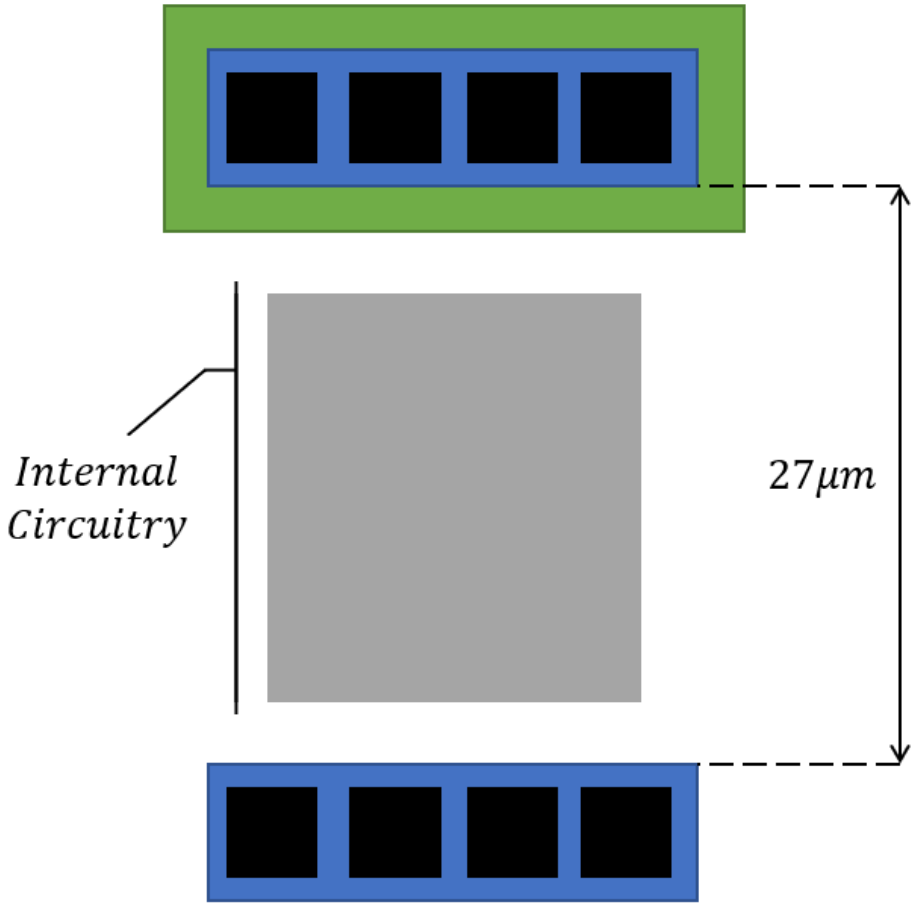

Figure 4: The 27µm Cell Frame

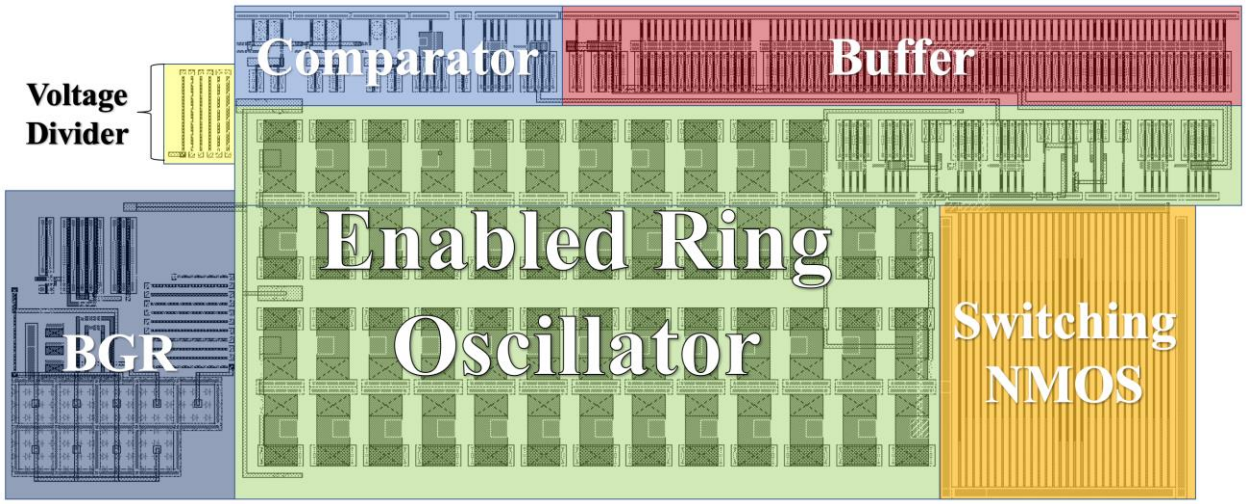

Figure 5: Floor Plan of the Boost SPS Chip

Figure 5 depicts the floor plan of the entire boost SPS IC. The BGR, voltage divider, comparator, buffer, enabled ring oscillator, and the switching NMOS are all present in the layout. The comparator, buffer, and enabled ring oscillator consist of five rows of cell frames. To minimize the length of the overall design, the cell frames were folded in a manner depicted in Figure 6.[i] The signal path is described by the arrows. The NTAPs are all connected and connected to VDD. Likewise, all the PTAPs are connected and connected to GND. The final layout with labeled input, output, and power terminals can be seen in Figure 7.

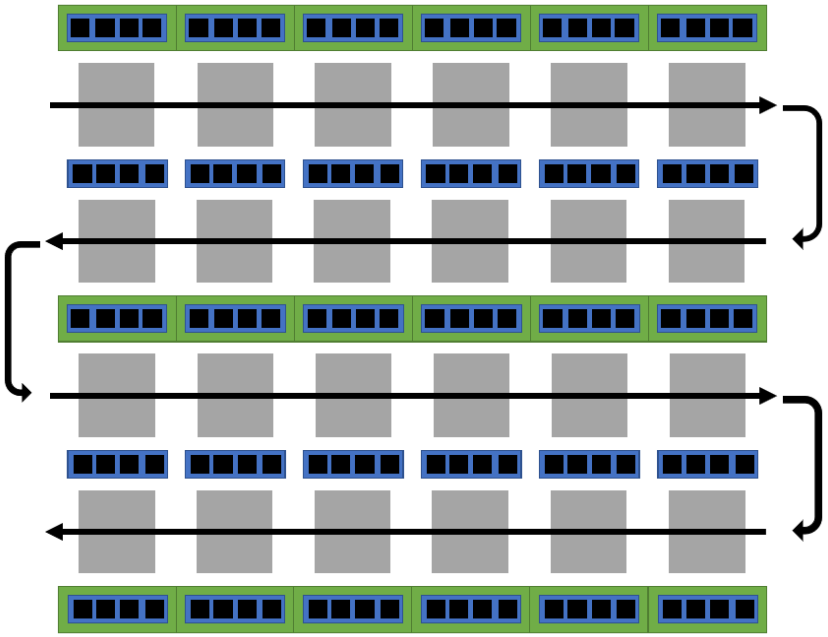

Figure 6: Connected Cell Frame Strings

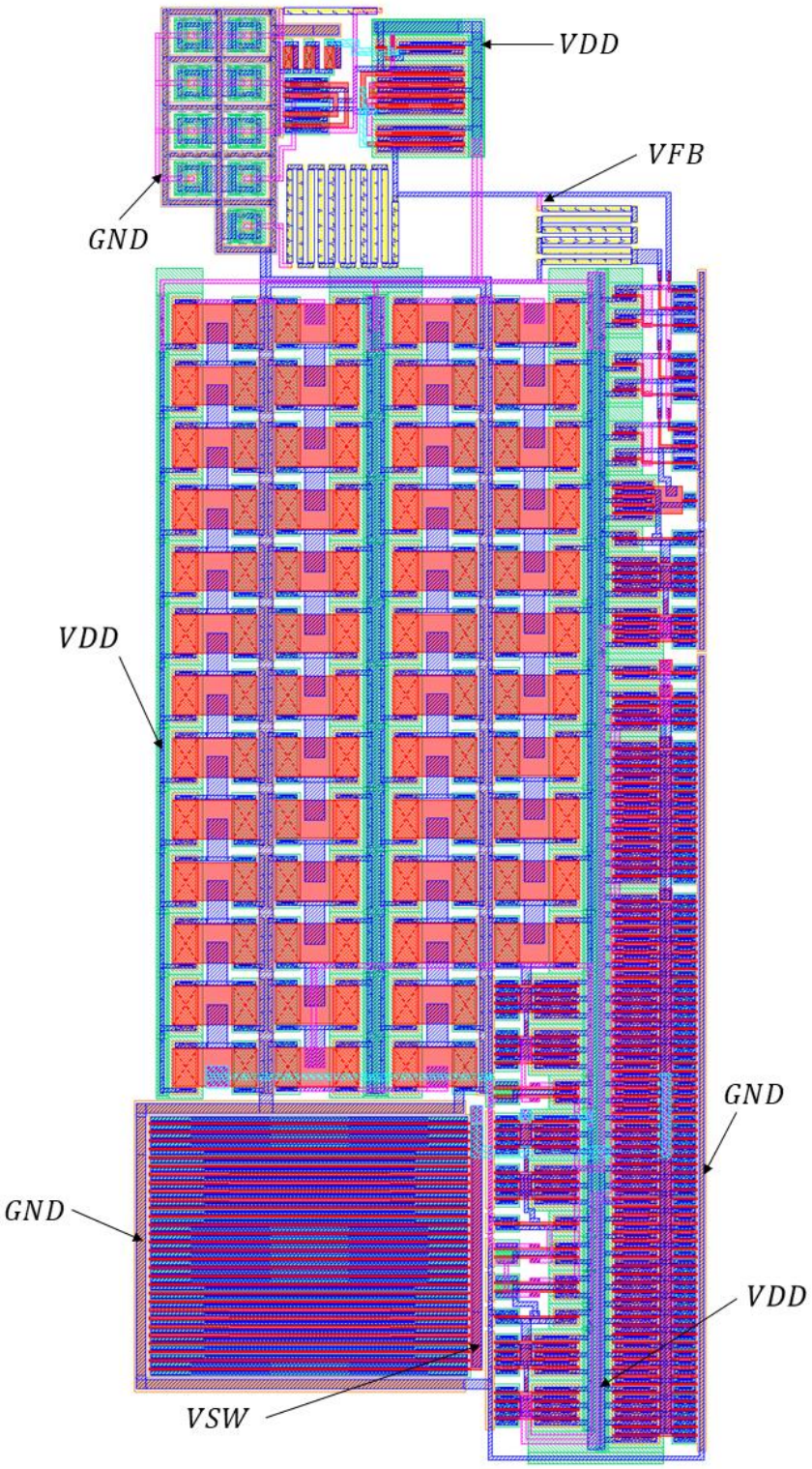

Figure 7: Entire Boost SPS Layout

3.1.2 Basic Building Blocks

Common components are found throughout the design. These components include an inverter, long length inverter, NAND logic gate, AND logic gate, and a small buffer.

Inverter

An inverter negates a logic signal. The device geometries used for both the NMOS and the PMOS is 6µ/600n.

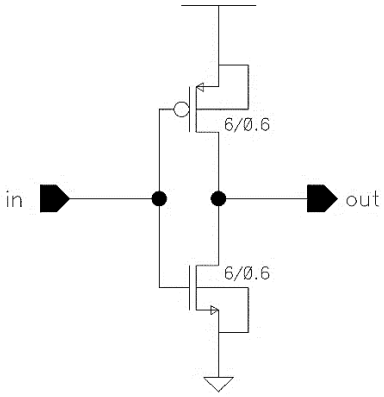

Figure 8: Inverter Circuit

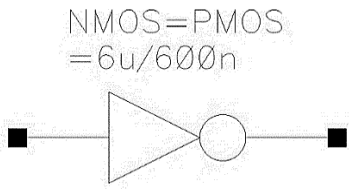

Figure 9: Inverter Symbol

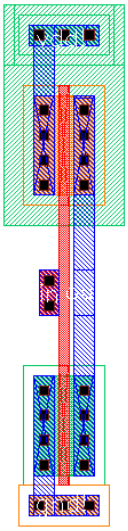

Figure 10: Inverter Layout

Long Length Inverter

Usually, in digital circuit design, fast switching speeds are the goal. However, this is not always the case. Occasionally, longer switching speeds are needed.[ii] The ring oscillator needs to long delays. Therefore, an inverter with long lengths was designed. The device geometries used for both the NMOS and the PMOS is 6µ/10.95µ.

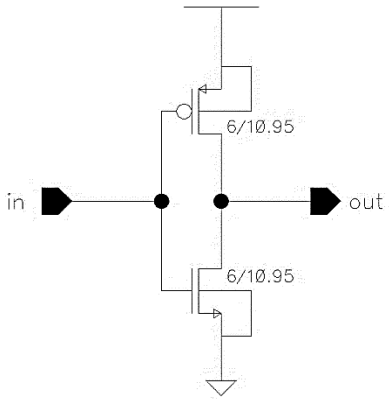

Figure 11

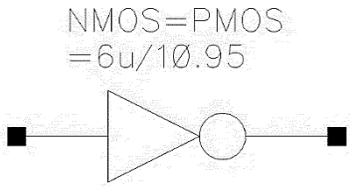

Figure 12

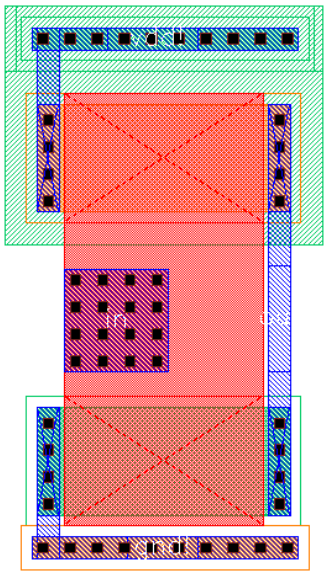

Figure 13: Long Length Inverter

NAND Logic Gate

The NAND logic gate is the complementary form of the AND logic gate. The truth table for a two input NAND gate is depicted in Table 3. The digital circuitry to describe logic displayed in the truth table can be developed using complex logic design (see Figure 14).

Table 7

A	*B*	*AnandB*
0	0	1
0	1	1
1	0	1
1	1	0

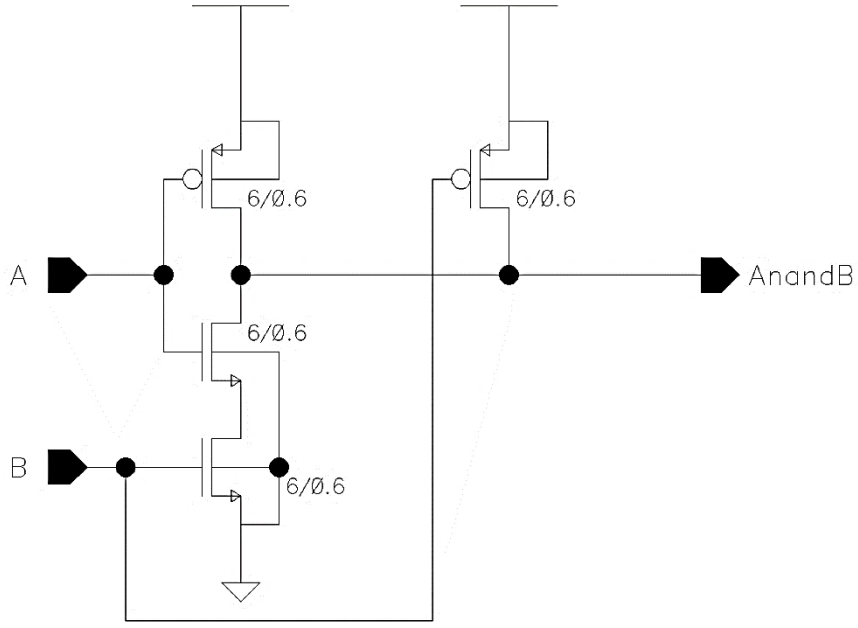

Figure 14: NAND Gate Circuitry

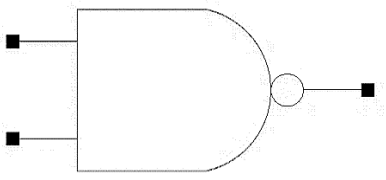

Figure 15: NAND Gate Symbol

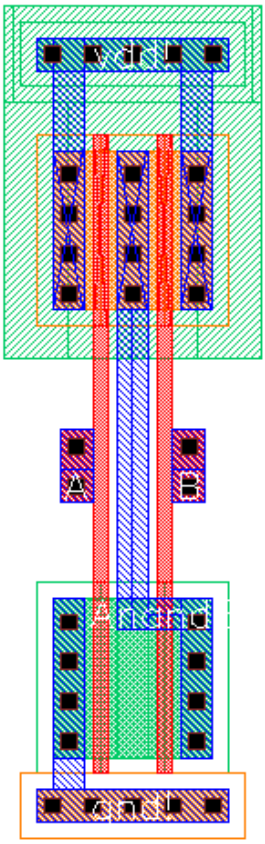

Figure 16: NAND Gate Layout

AND Logic Gate

The created NAND logic gate and inverter can be combined to form a AND logic gate.

Table 8

A	*B*	*AandB*
0	0	0
0	1	0
1	0	0
1	1	1

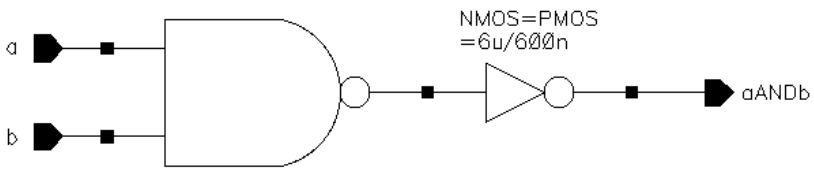

Figure 17: AND Logic Gate Circuitry

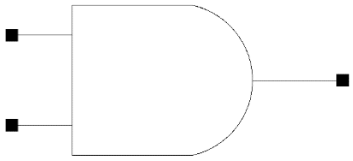

Figure 18: AND Logic Gate Symbol

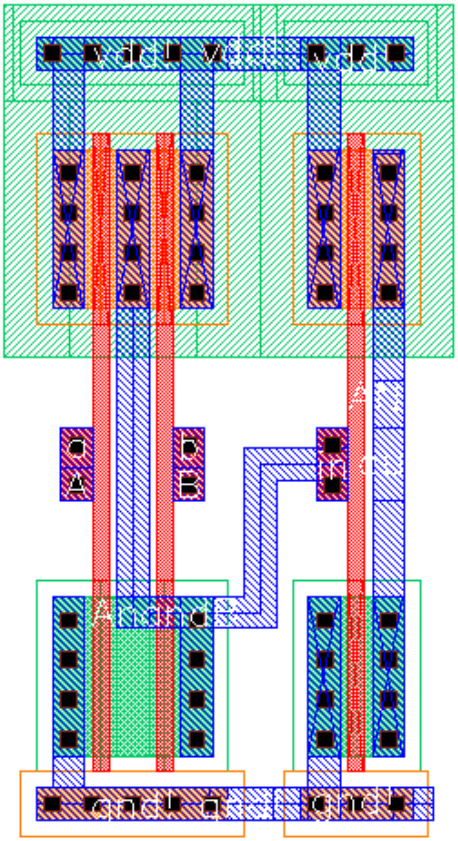

Figure 19: AND Gate Layout

Small Buffer

A small buffer is found throughout the design to ensure that the rise and fall times of the digital signals are quick. It should be noted that fast rise and fall times in digital design is preferred.

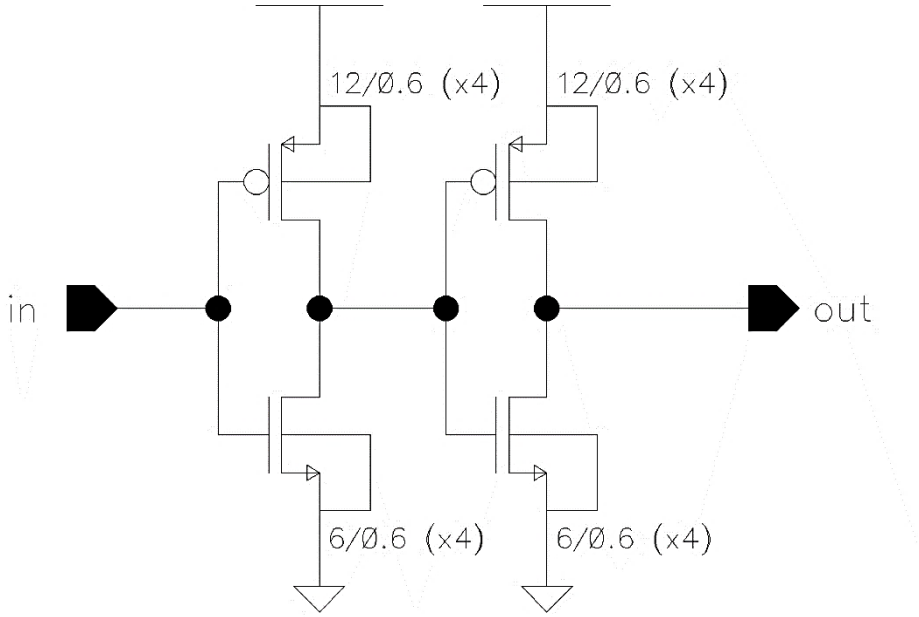

Figure 20: Small Buffer Circuit

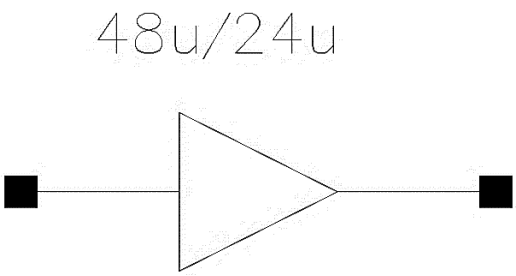

Figure 21: Small Buffer Symbol

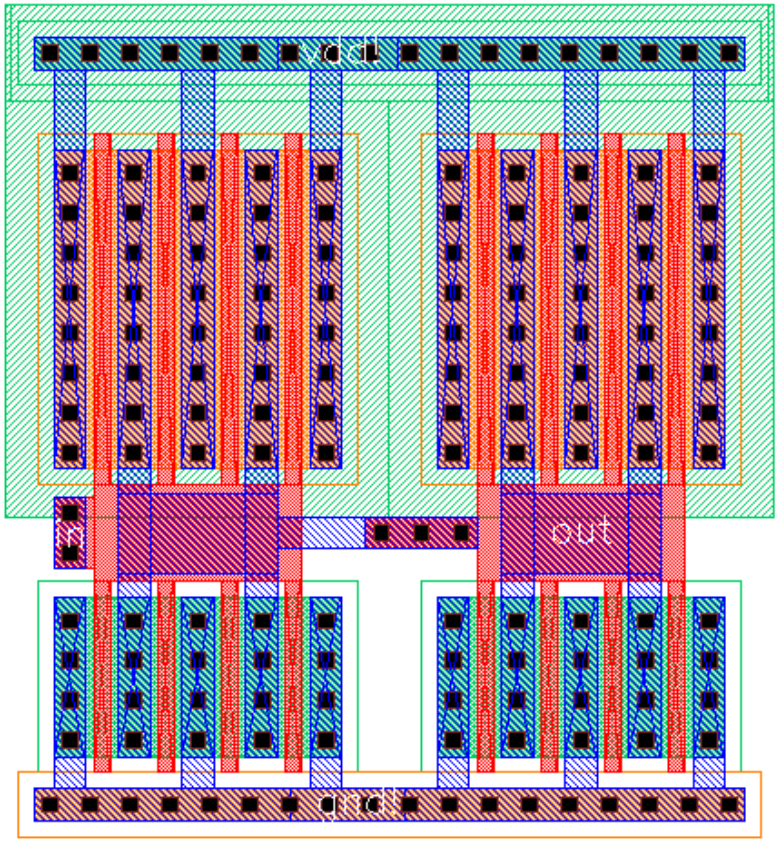

Figure 22: Small Buffer Layout

3.1.3 Resistive Voltage Divider

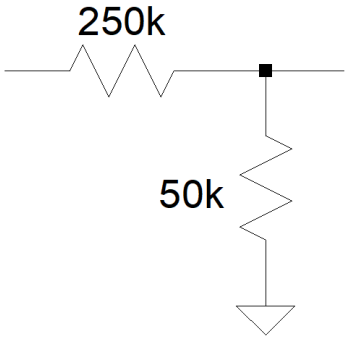

Figure 23: Implemented Resistive Voltage Divider

As described previously, a resistive voltage divider (or attenuator) will be used to attenuate *Vout* so that *Vout* can be compared to the output voltage of the BGR. In the design requirements it is made clear that the voltage divider can draw no more than 50µA from the node *Vout* and no less than 10µA in current. This current restriction in current draw is made to reduce the loading effect. Adding an attenuator to the output of out boost SPS system, loads the output of the boost SPS system. For further emphasis, consider a voltmeter. A voltmeter must not affect the design under test. Therefore, to minimize the loading effect, the voltmeter should have high impedance

and connected in parallel. Like a voltmeter, our attenuator should have a high impedance to minimize the loading effect.

The output of the bandgap voltage reference is 1.25V. *Vout/6* is 1.25V. Therefore, to compare the two voltages with one another, a 1/6 attenuator is necessary. To increase matching, a 50kΩ unit cell resistor will be used. Six 50kΩ unit cell resistors will be used. To implement a 1/6 voltage divider with 50kΩ resistors, two resistances need to be achieved. The first resistance of the voltage divider is 250kΩ and the second resistance of the voltage divider is 50kΩ (see figure 23).

The total impedance between *Vout* and ground will be 300kΩ. Therefore, the current flowing through the attenuator can be determined in the following manner:

$$\frac{7.5V}{300k\Omega} = 25\mu A$$

25µA is well within the current draw range given by the design requirements. The following figure depicts the voltage divider as implemented in layout. The resistors are formed by the *elec* poly layer. Then *hires* layer is then placed over the *elec* resistor. The *hires* acts like a mask during the doping process. This *hires* mask ensures that the resistivity of the *elec* material remains high. The width of the resistors is kept at the minimum *elec* size of 600nm. The resistors are connected in a serpentine manner. The geometries were determined by an online IC Resistor Geometry Calculator that I developed in HTML and JavaScript.[iii] This calculator has proved to be useful as it has three modes of operation and alleviates tedious simple resistance calculation. [iv]

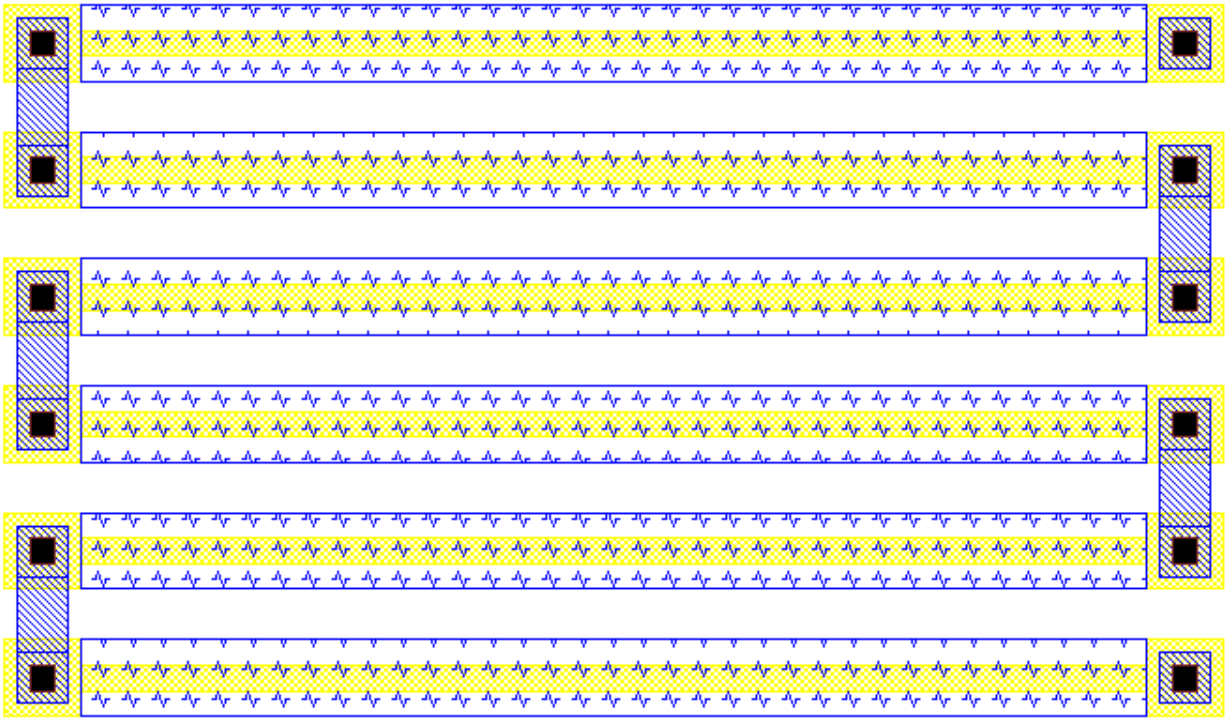

Figure 24: The Resistive Voltage Divider Layout

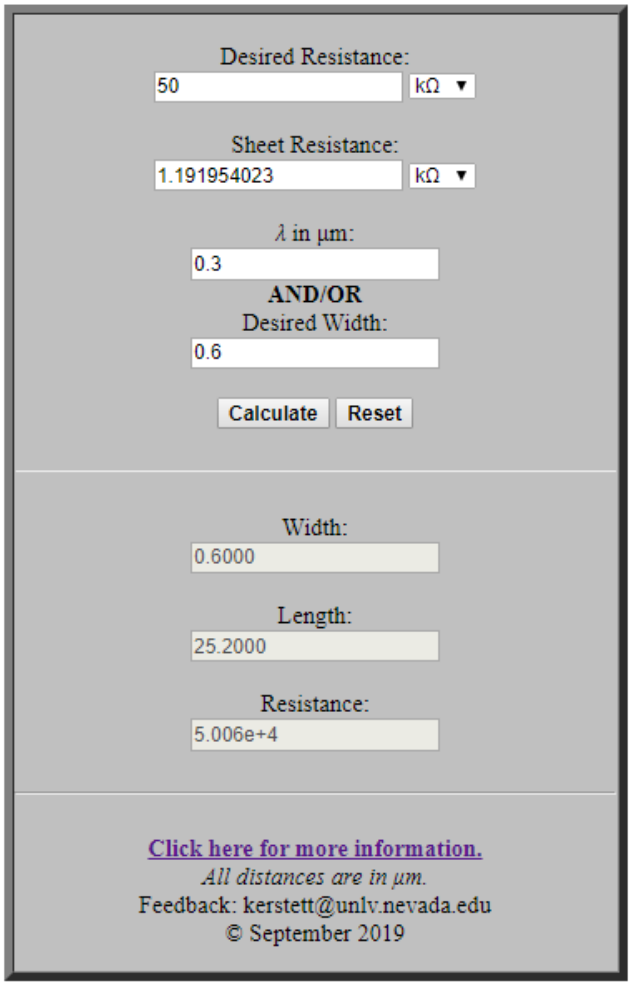

Figure 25: The IC Resistor Geometry Calculator Used for Resistor Geometry Calculations

The voltage divider implements unit cell techniques. Therefore, the exact value of a 50k**Ω** resistor is not necessary, if all six implemented resistors in the voltage divider are of the same resistance. The following shows the extracted resistance value of one 50k unit cell resistor which is 50.06k**Ω**. Which is precisely the resistance value calculated by the IC Resistor Geometry Calculator.

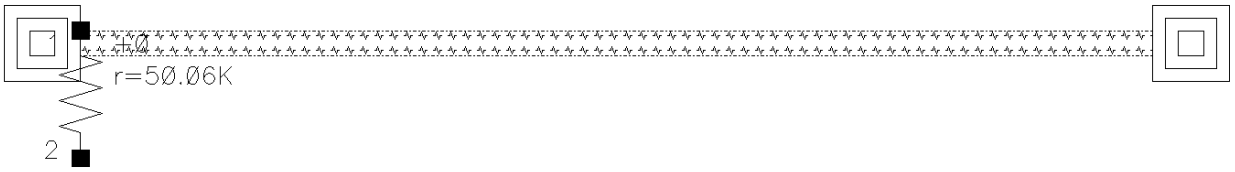

*Figure 26: 50k**Ω** Unit Cell Resistor with Extracted Resistance Value*

3.1.4 Bandgap Voltage Reference (BGR)

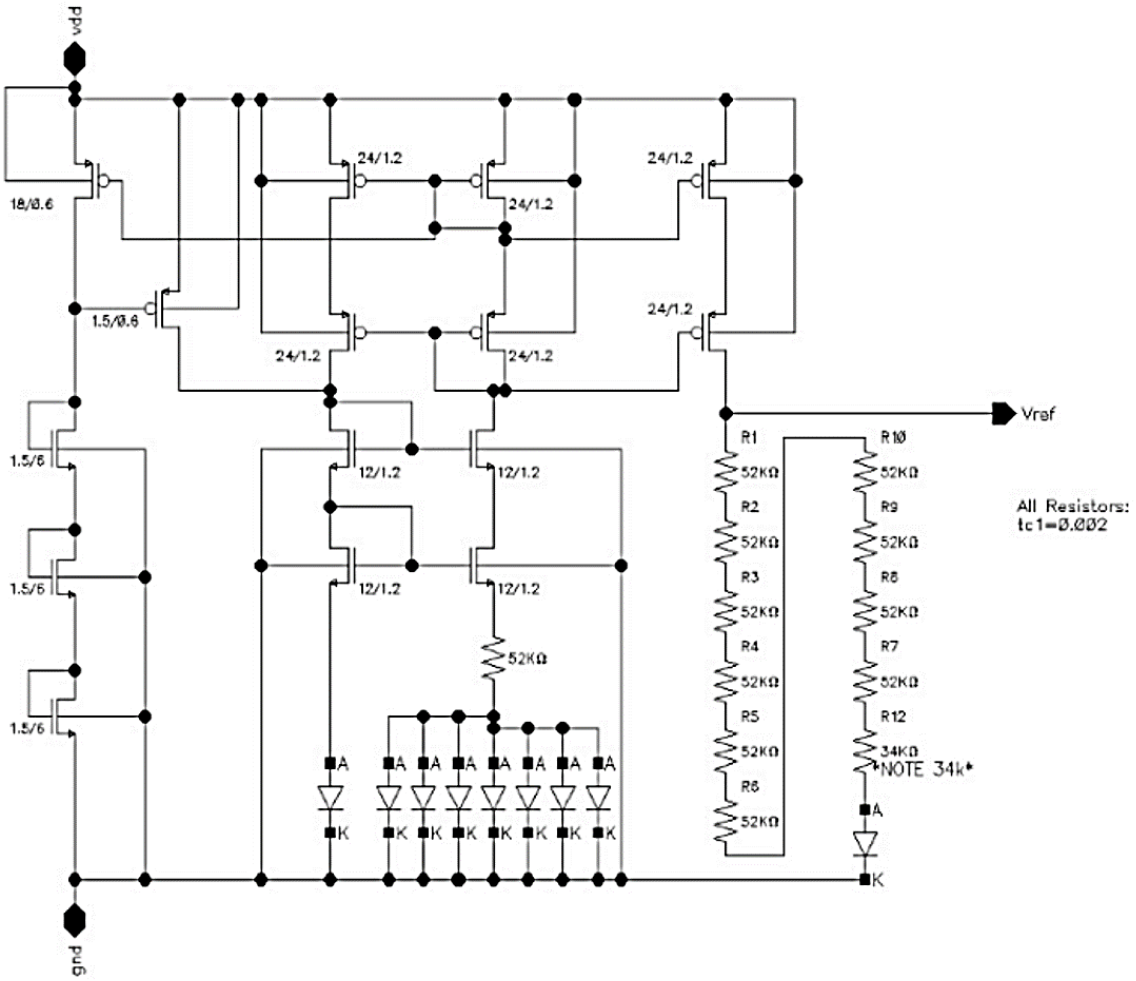

Figure 27: 1.25V Bandgap Voltage Reference Circuit

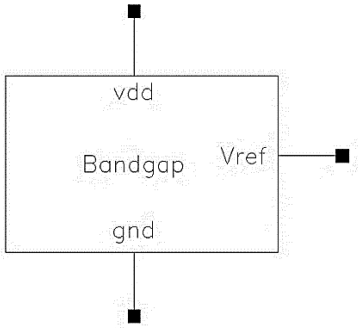

Figure 28: 1.25V Bandgap Voltage Reference Symbol

A crucial design issue in this project is to produce a voltage reference 1.25V that is ideally independent from the power supply voltage and temperature. A bandgap voltage reference can be designed to create a reference voltage that does not vary much with the power supply voltage and temperature. The circuit of the bandgap voltage reference uses parasitic pnp diodes.

Characterization of the Parastic PNP Diode

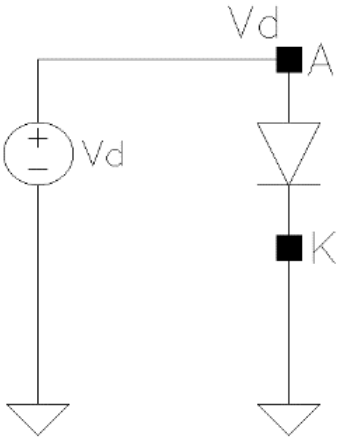

Figure 29: Circuit Used to Characterize the Diode

The IV curve of the parasitic PNP diode is seen in the subsequent plot. The threshold voltage of the diode is 700mV. Therefore, the voltage drop over the diode is 700mV.

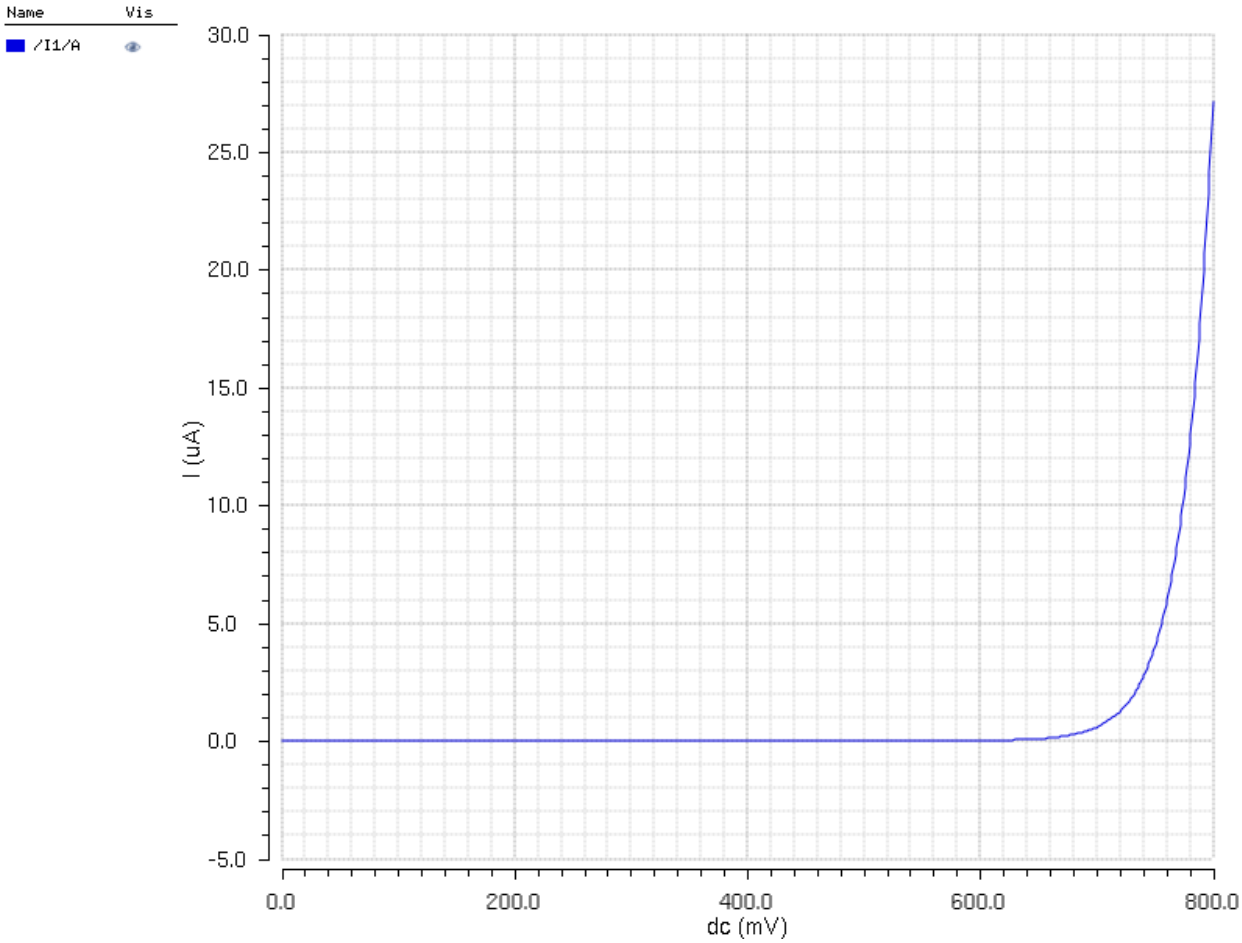

Figure 30: Parasitic PNP Diode – Varying Diode Voltage

Figure 31: Circuit to Test Parasitic PNP Diode's Response to Temperature

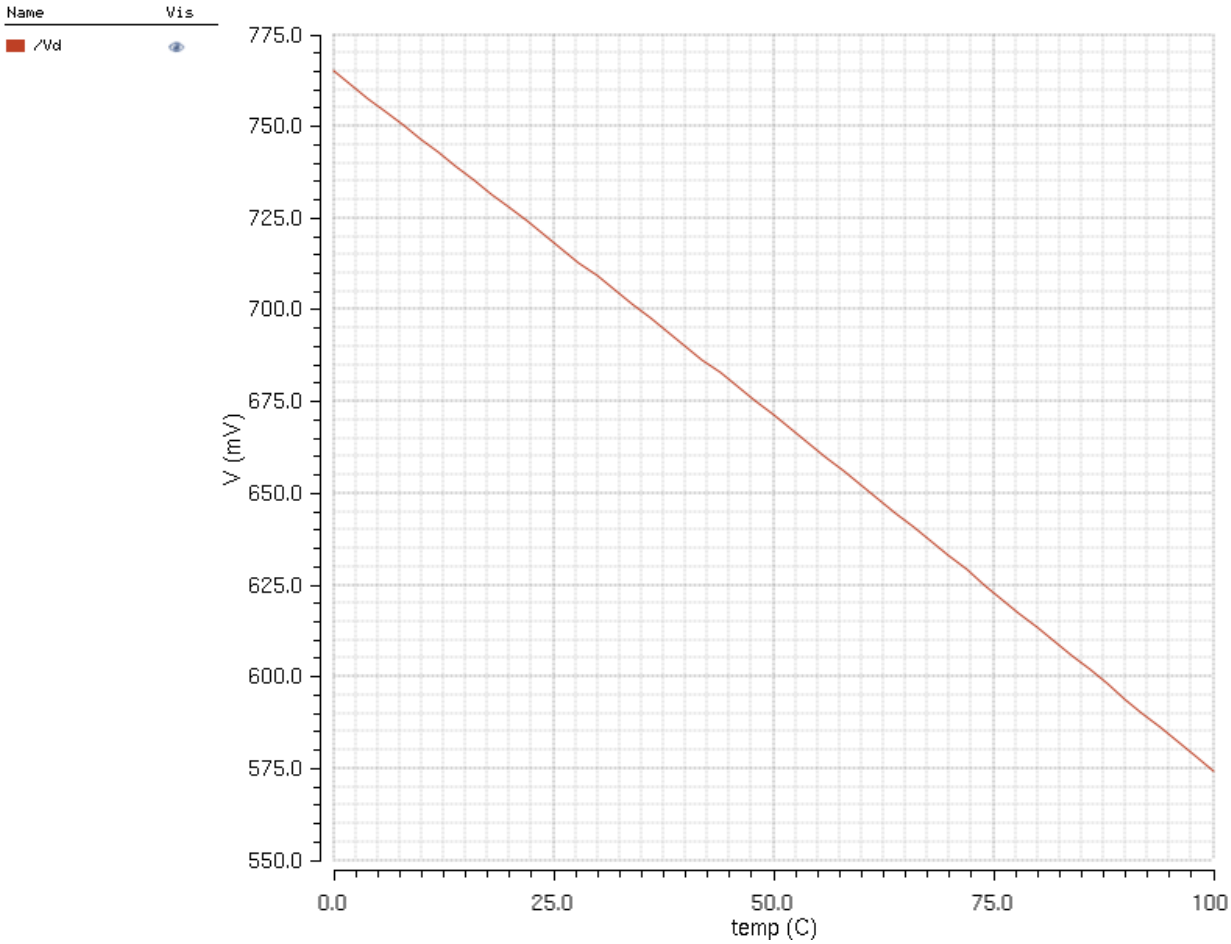

Figure 32: Parasitic PNP Diode – Varying Temperature

The circuit depicted in Figure 31 was designed to test the temperature response of the parasitic PNP diode. As seen in Figure 32, the parasitic PNP diode's temperature response is CTAT (Complementary To Absolute Temperature).

Simulation of the Bandgap Voltage Reference

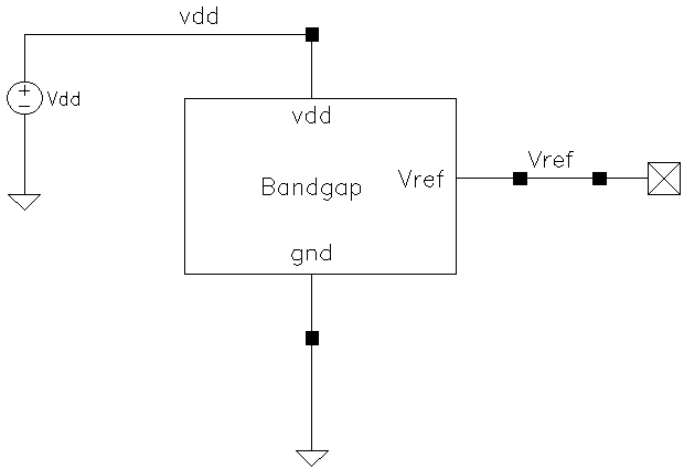

Figure 33: Circuit to Test Bandgap Voltage Reference

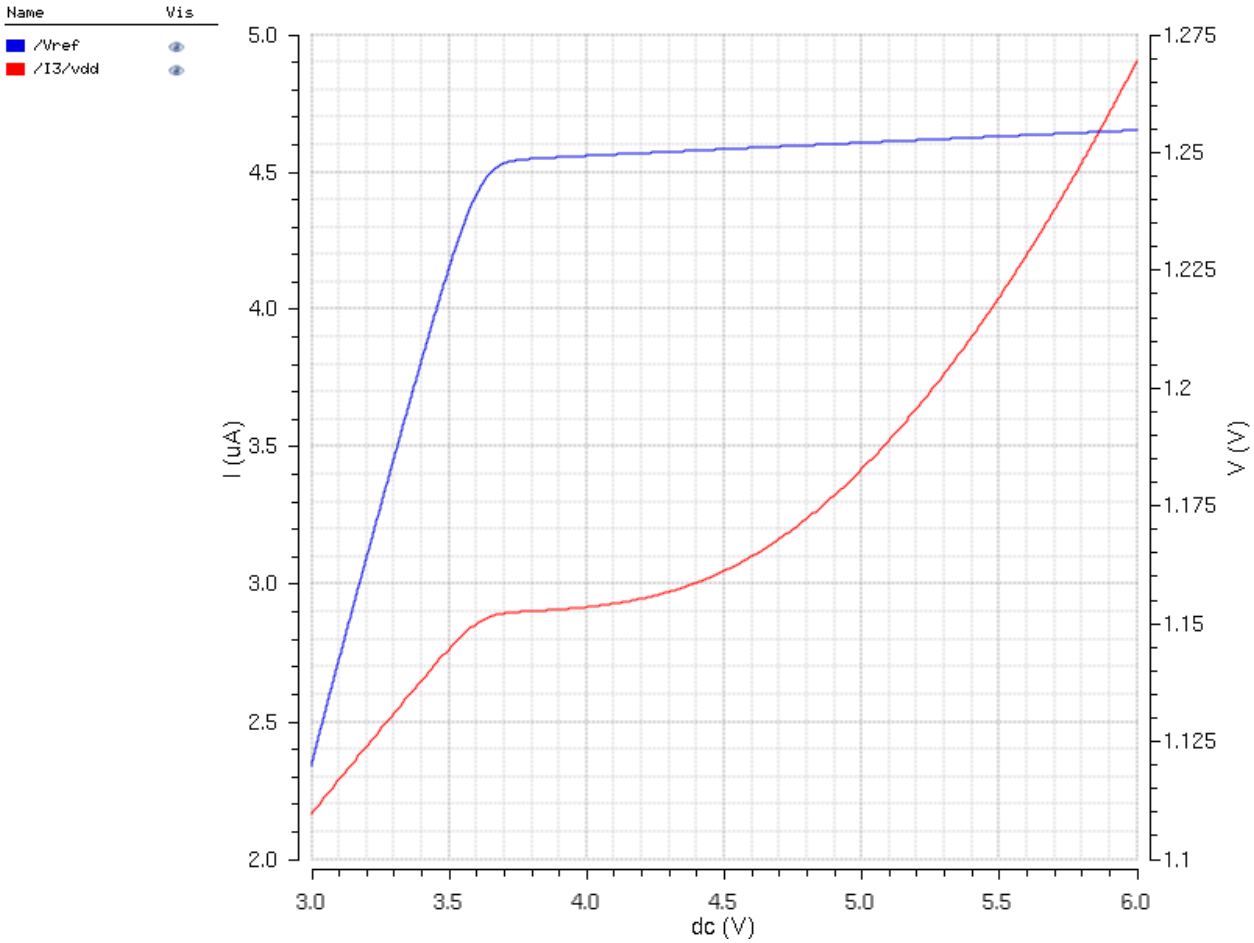

Figure 34: Bandgap Simulation – Varying VDD

The power supply voltage can be lowered to ~3.6V before the bandgap output voltage drops (see Figure 34). After ~3.6V, the bandgap output voltage remains close 1.25V. This minimum voltage power supply voltage is well within the range of the *VDD* range given in the design requirements (3.75-5.25V). The bandgap circuit draws between 3µA and 5µA during operating VDD conditions (Figure 34). At quiescent conditions the current draw is 2.16µA.

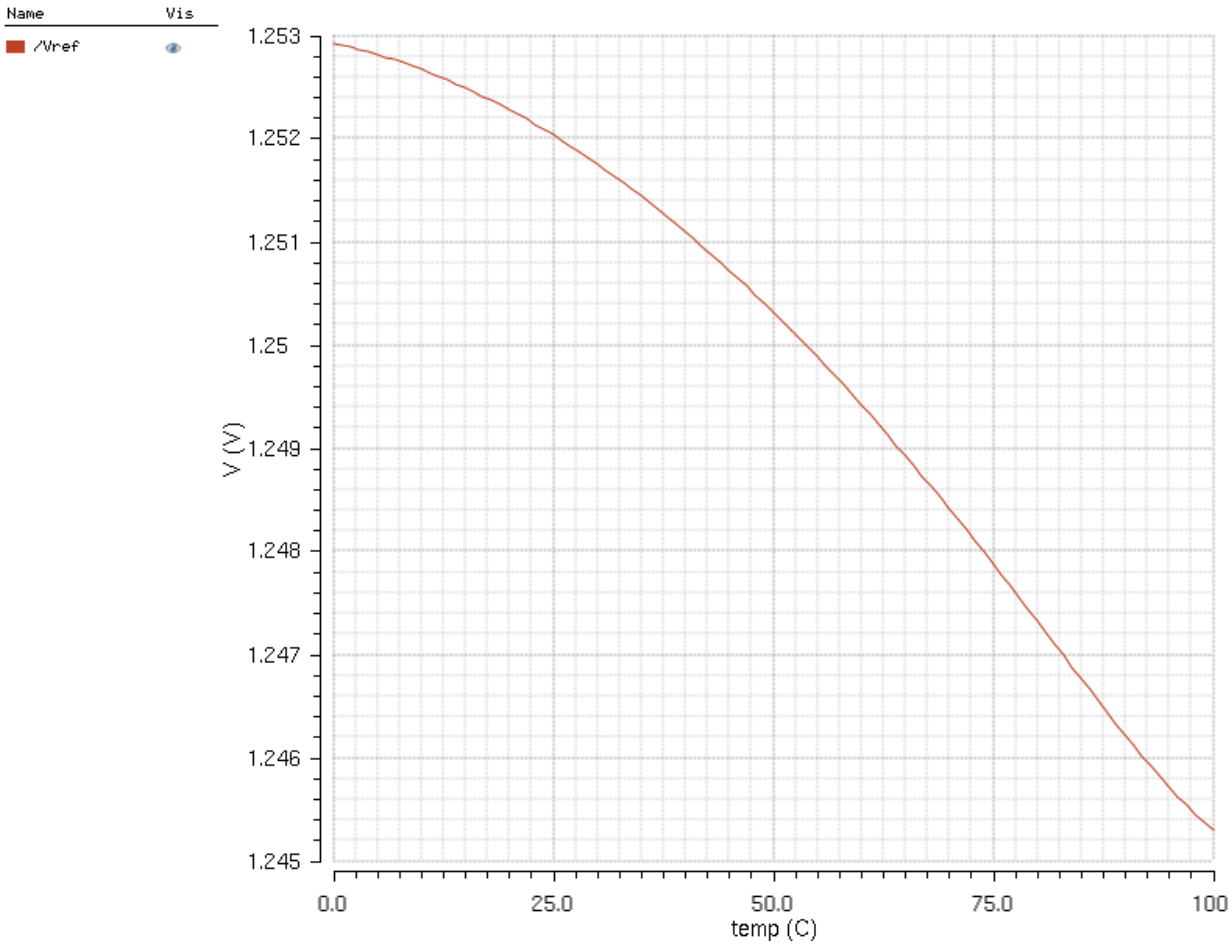

Figure 35: The Bandgap Voltage Reference's Response to Temperature

The reference voltage varies very little for the temperature range of freezing point (0 degrees Celsius) to the boiling point (100 degrees Celsius) of water (see Figure 35). At 0 degrees Celsius the bandgap output voltage is at 1.253V. At 100 degrees Celsius the bandgap output voltage is roughly 1.245. Therefore, we may develop a rough linear model describing the temperature response of the circuit.

$$\frac{\partial V_{REF}}{\partial T} = \frac{\triangle V_{REF}}{\triangle T} = \frac{(1.253 - 1.245)V}{(0 - 100)℃} = \frac{0.008V}{-100℃} = -80\mu V/℃$$

$$\therefore V(T) = -80\mu \cdot T + 1.253$$

As seen above, the voltage varies $-80\mu V/℃$, which is not much change in voltage considering the large change in temperature. Additionally, it can also be said that the bandgap output voltage

can be classified as CTAT (as can be said about the parasitic PNP diode's temperature response). The typology of the bandgap is given in Figure 36[v].

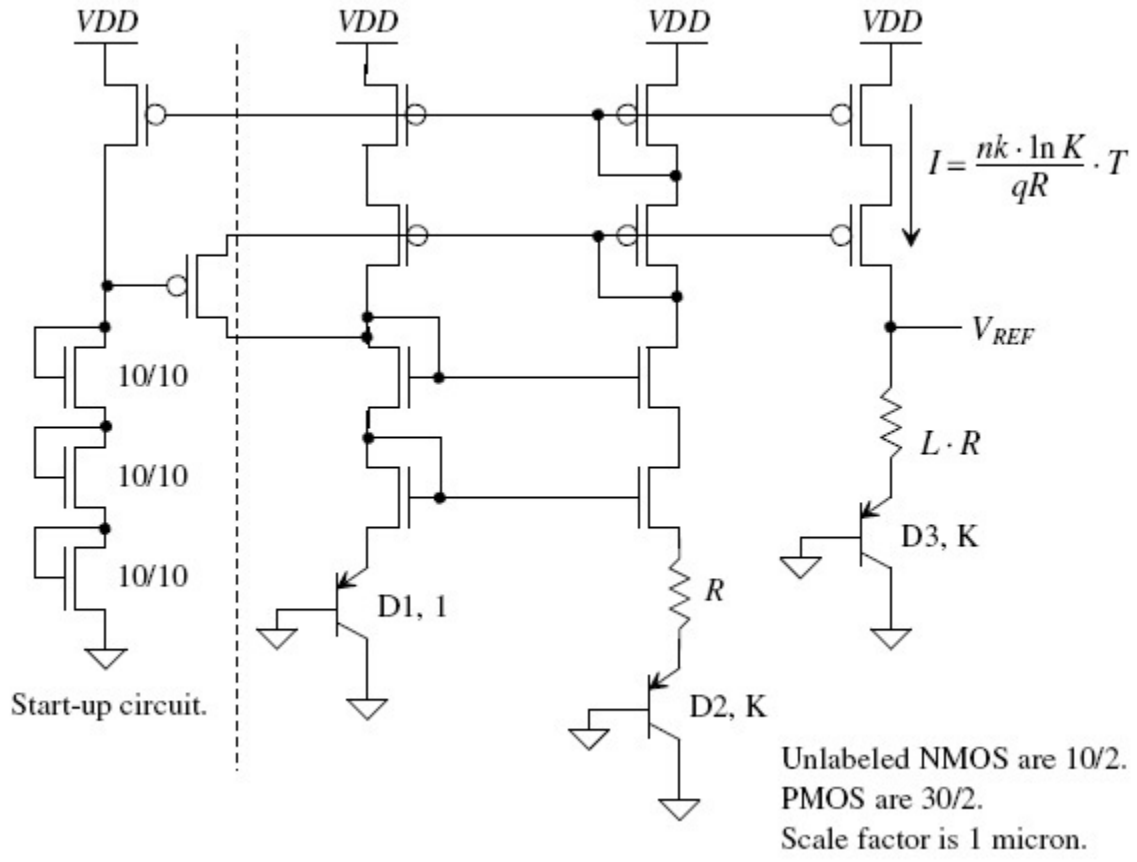

Figure 36: Bandgap Topology Implemented Given in Dr. Baker's CMOS Book

In reference to the topology given in Figure 36, the reference voltage is described by the following equation[vi].

$$V_{REF} = V_{D3} + I \cdot L \cdot R = V_{D3} + L \cdot n \cdot \ln k \cdot V_T$$

Highlighting the change in the reference voltage with temperature is[vii]:

$$\frac{\partial V_{REF}}{\partial T} = \frac{\partial V_{D3}}{\partial T} + L \cdot n \cdot \ln k \cdot \frac{\partial V_T}{\partial T}$$

$$\frac{\partial V_{D3}}{\partial T} = Diode's\ Temperature\ Response$$

$$L \cdot n \cdot \ln k \cdot \frac{\partial V_T}{\partial T} = Resistor's\ Temperature\ Response$$

Here we see that the bandgap reference's response is dependednt upon two terms. The first term is the diodes response to temperature. The second term is the resistor's response to temperature. Generally, a resistor's response to temperature is PTAT (Proportional To Absolute Temperature)

and a diode's temperature response is CTAT. In simulations it become clearly evident that the temperature response of the bandgap reference is CTAT (see Figure 37). Why is this the case? The rate of change of the resistor's temperature response is much lower compared to the rate of change of the diode's temperature response. Therefore, it can be said that the CTAT of the diode overpowers the PTAT of the resistors. Due to this fact, it becomes evident why the bandgap voltage reference is CTAT. This is further demonstrated in another simulation.

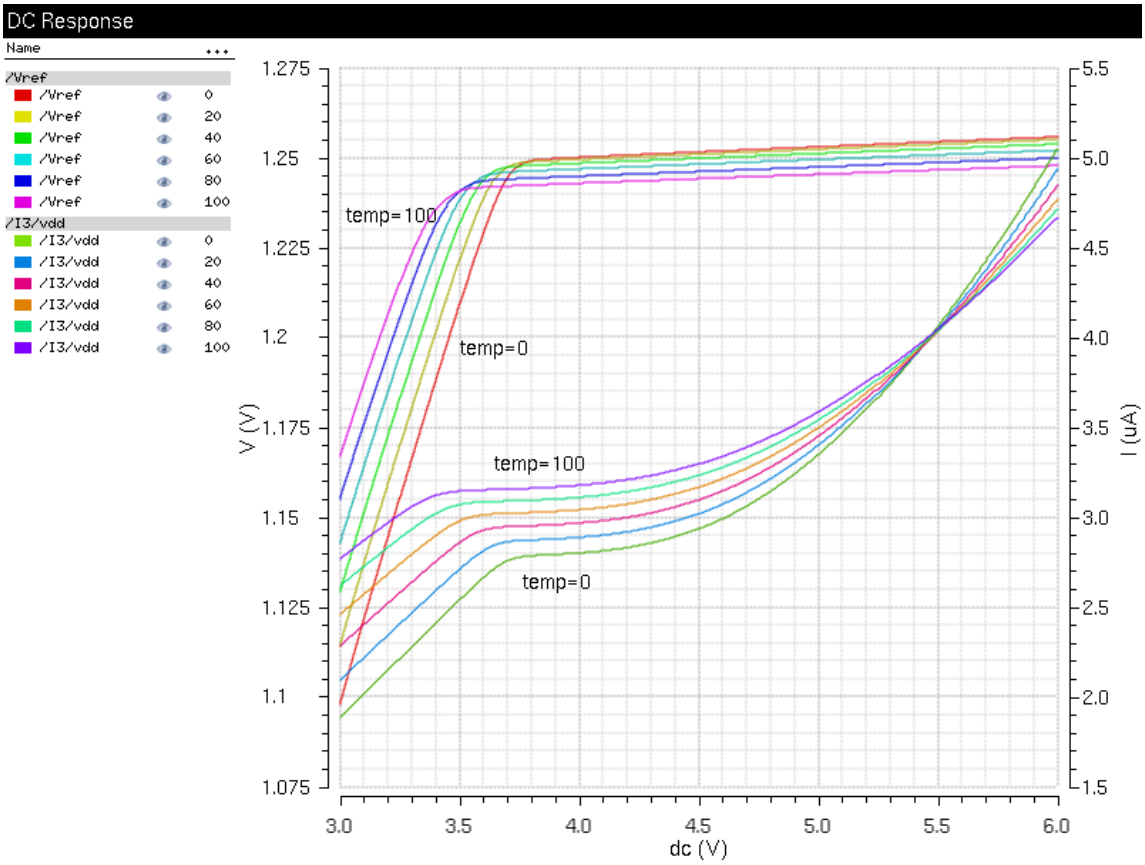

Figure 37: The Bandgap Voltage Reference's Response to Temperature – DC Sweep

A Fial Note on the Bandgap Voltage Reference

The bandgap voltage reference's response to varing VDD and temeprature introduces another thing to consider. The foundation of the boost SPS feedback control loop is the reference voltage of 1.25V. Without the bandgap voltage reference, the boost SPS system could only work for a very small VDD and temperature range. However, one fact has been made absolutely clear in this section; that is, the BGR output voltage varies slightly with variences in temperature and power supply voltage. Therefore, the conclusion is that the BGR produces a great, but not perfect voltage reference. Variences in BGR's output will lead to variences in *Vout*. The badgap circuit given in Figure 27 was laid out. The layout can be seen in Figure 38.

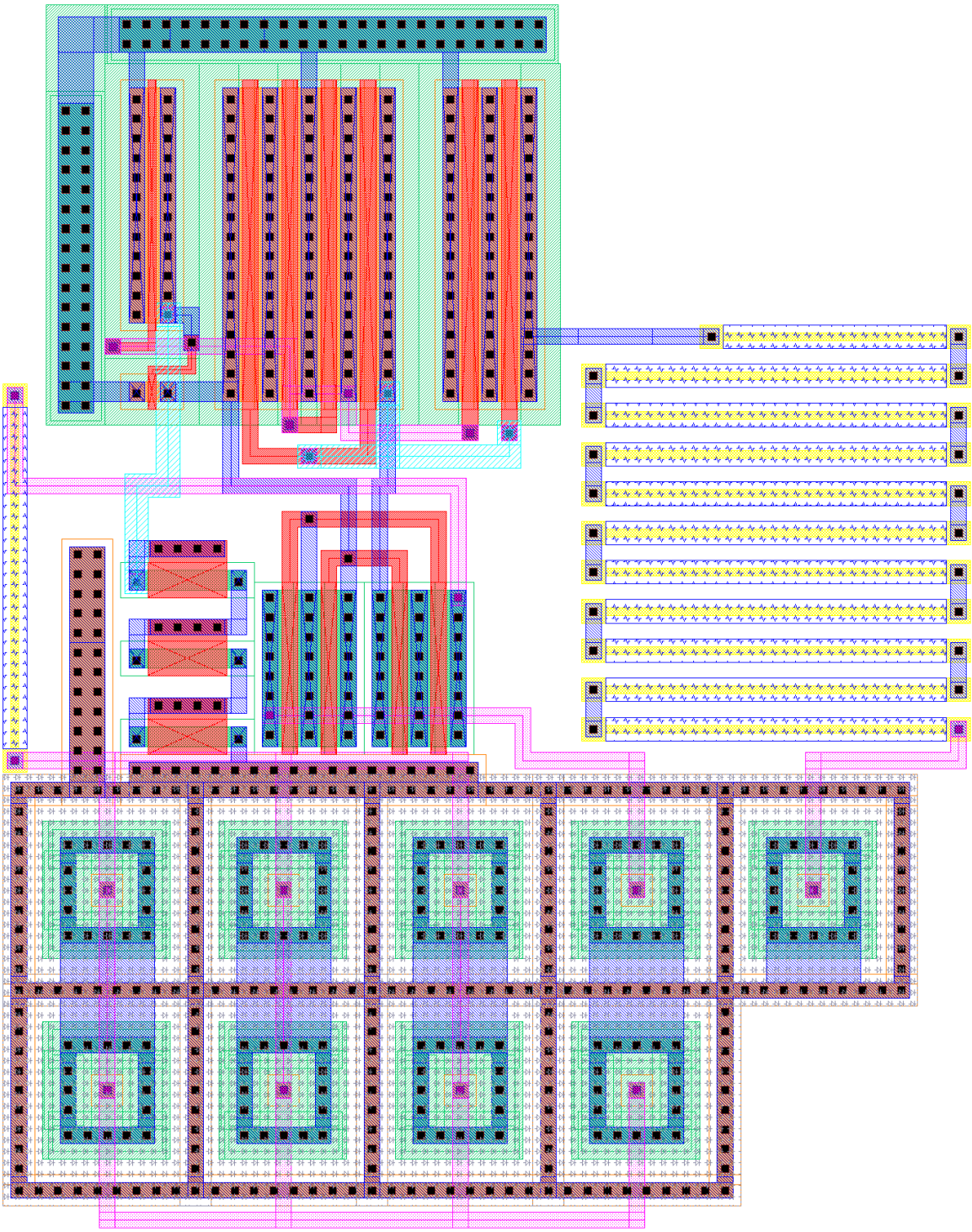

Figure 38: Bandgap Voltage Reference Layout

3.1.5 Voltage Comparator

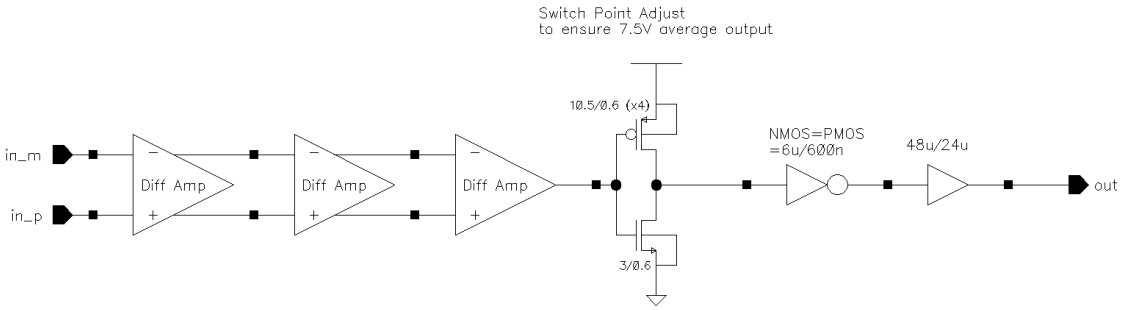

Figure 39: Voltage Comparator Circuit

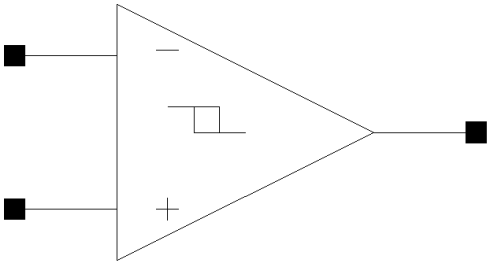

Figure 40: Voltage Comparator Symbol

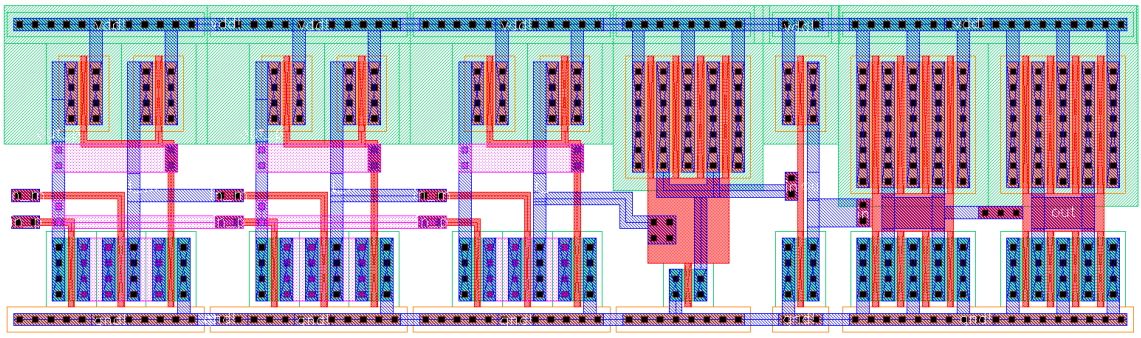

Figure 41: Voltage Comparator Layout

A voltage comparator compares two voltages and outputs a Boolean value regarding the state of the values. The comparator has two terminals, the plus and minus terminals. If the voltage on the plus terminal is greater than the minus terminal, then the comparator will output active high. Otherwise, the comparator will output active low. As described the goal is to produce a device to detect when *Vout* drops below the intended voltage of 7.5V and then consequently output active high. The device should then output active low in all other situations (i.e. when *Vout* is greater than 7.5V). The comparator design involved three cascaded differential amplifiers. The first two amplifiers have differential inputs and outputs (see Figures 42-44). Whereas, the third

differential amplifier has a differential input and a single-ended output (see Figures 45-47). Depending upon the state of the voltage on the two terminals, the output of the differential amplifiers will force the signal to go to ground or *VDD.* After the differential amplifiers, the single propagates through a string of inverters. This string of inverters converts the analog output of the differential amplifier to a digital value of active high or active low.

After the differential amplifiers, there is an inverter that has a strong PMOS. This strong PMOS inverter is added to adjust the switching point of the inverter. By adjusting the switching point of the inverter, the switch is ensured to occur precisely at the value that is needed (see Figure 49). Additionally, it was seen in simulation, that by adjusting the switching point, the efficiency and the precision of the boost SPS system increased. Another inverter is added to ensure that the proper logic is preserved. Finally, a small buffer is added to the output to ensure that rising and falling edges remain quick.

Differential Amplifier with Differential Output

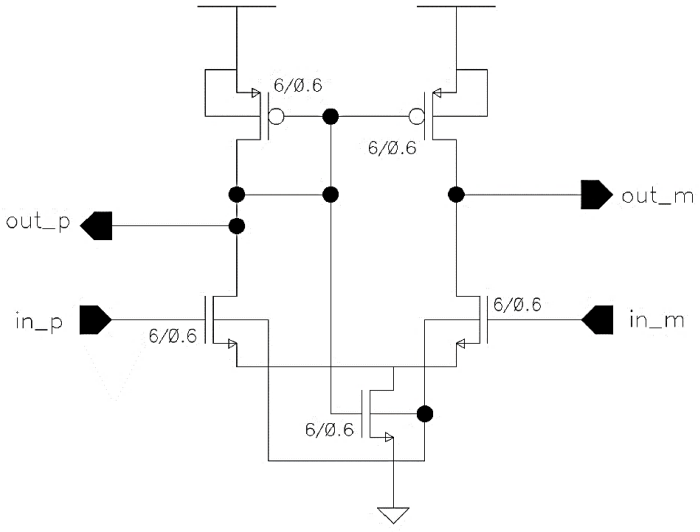

Figure 42: Differential Amplifier with Differential Output Circuit

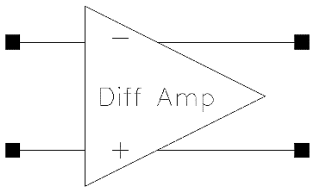

Figure 43: Differential Amplifier with Differential Output Symbol

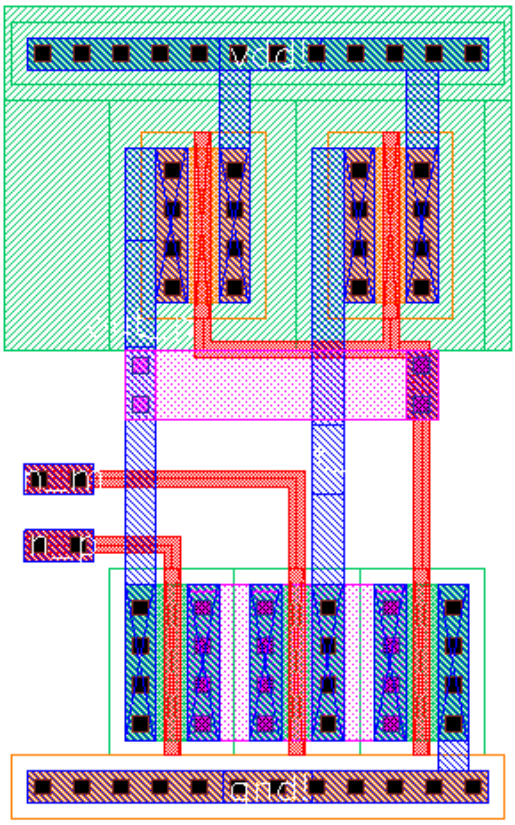

Figure 44: Differential Amplifier with Differential Output Layout

Differential Amplifier with Single-Ended Output

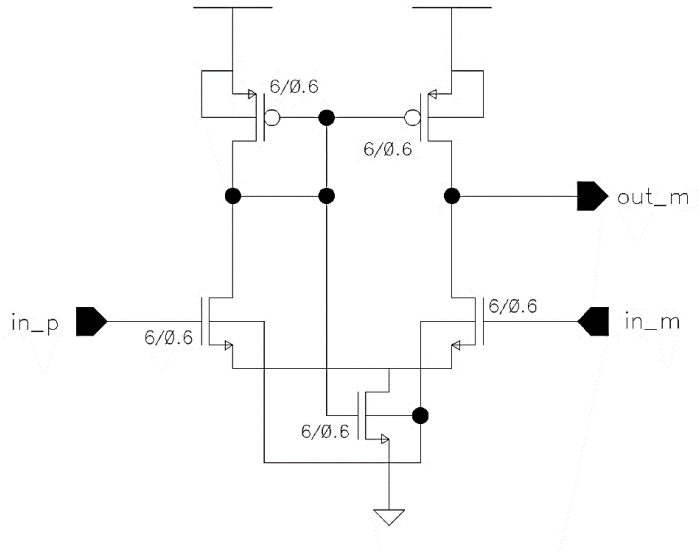

Figure 45: Differential Amplifier with Single-Ended Output Circuit

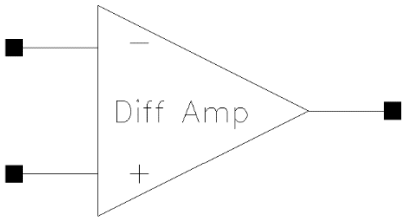

Figure 46: Differential Amplifier with Single-Ended Output Symbol

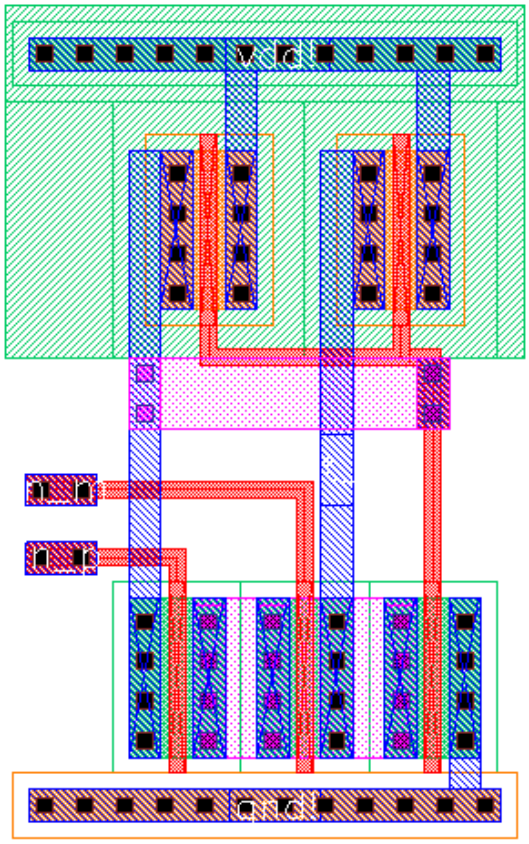

Figure 47: Differential Amplifier with Single-Ended Output

Comparator Simulation

To ensure proper operation of the comparator two simulations were conducted. The first simulation tested the switching point of the comparator. The second simulation simulates how the comparator might behave while functioning in the boost SPS system. Therefore, a schematic was drafted in Figure 48 to conduct such described simulations. The results of the first simulation can be seen in Figure 49.

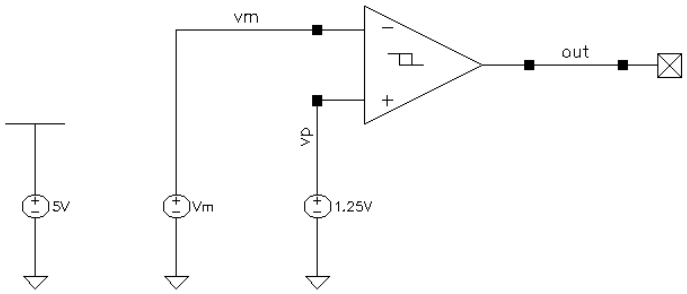

Figure 48: Circuit to Test the Comparator Design

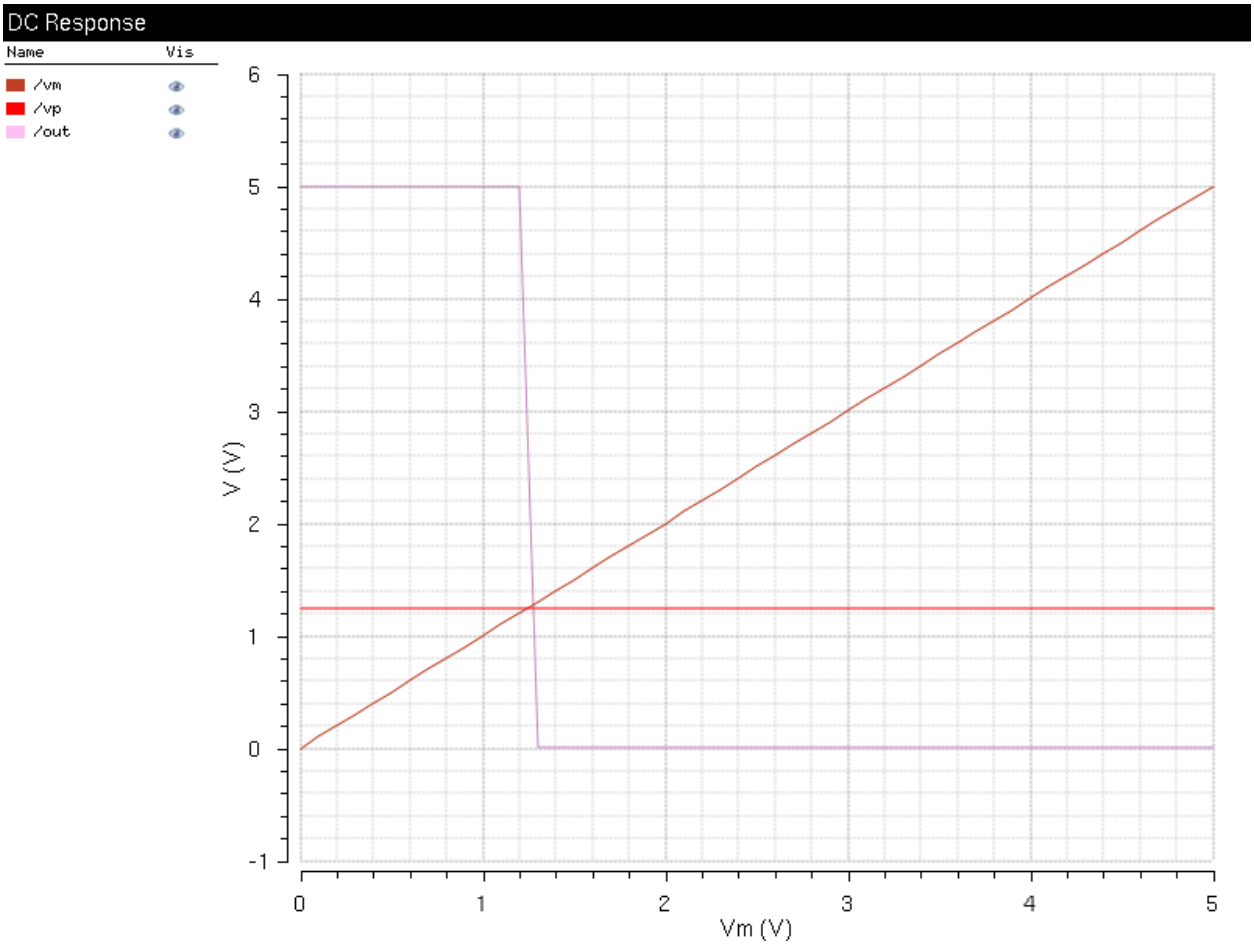

Figure 49: Comparator Simulation

In Figure 49, the comparator functions as intended. When *Vm* is below approximately 1.25V, the output of the comparator is active high. Whereas, when *Vm* is above approximatively 1.25V, the output of the comparator is active low. Now, a simulation will occur that will simulate how the comparator will function while in the boost SPS system (see Figure 50).

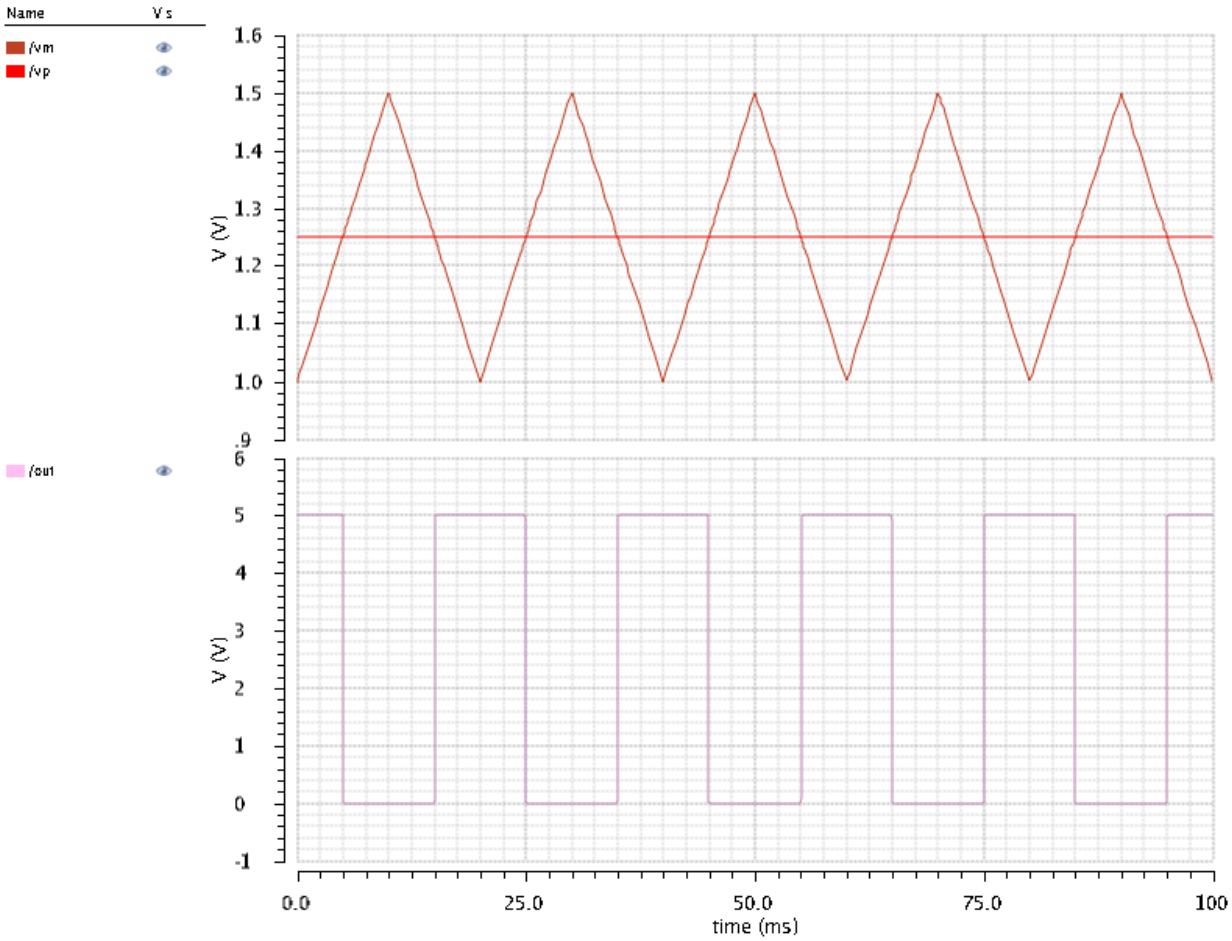

Figure 50: Comparator Boost SPS System Simulation

In Figure 50, a simulation of how the comparator would behave in the boost SPS system. *Vp* will be at a constant point of around 1.25V (due to the bandgap voltage reference). Then *Vout* voltage which will be at 7.5V will be attenuated to 1.25V. Therefore, when *Vm* is below *Vp*, that means that *Vout* is below 7.5V. Likewise, when *Vm* is higher than *Vp*, then that means that *Vout* is higher than 7.5V. The correct logic levels are seen to be the output of the comparator.

A Note Regarding Hysteresis

Consider a cruise control system in an automobile. The cruise control system is a feedback system consisting of a controller, process and a means of taking measurement. The controller generally is a microcontroller. The process is engaging the engine. The means of measurement is the speedometer. The actual speed is compared to the desired speed. The comparison produces an error value. This error value then is sent to the microcontroller. The microcontroller either engages or disengages the throttle based upon the determined error. If there is no delay in the

system, high frequency oscillations can occur. As soon as the actual speed is above the desired speed, the controller immediately disengages the engine. Likewise, when the actual speed is below the desired speed, the controller immediately engages the engine. It can easily be seen why high frequency oscillations in the control system would occur. These high frequency oscillations could cause the engine to wear out. Delay in the feedback loop can be added to prevent such high frequency oscillation. For instance, the controller will not engage or disengage the engine until the actual speed is ±1 mph above or below the desired speed. Therefore, it can be said that the hysteresis is 1 mph for a setpoint of the desired speed. This everyday example gives a great foundation in feedback control theory and hysteresis.

As stated before, the boost SPS system is a feedback control system. The block diagram of the feedback control system can be seen in the following figure. The process in this case is the switching of the NMOS. The measurement is conducted by the comparator, attenuator, and bandgap voltage reference. Finally, the controller is the output of the comparator. If there is no delay between the sensing of *Vout* and the action to enable the switching of the NMOS, high frequency oscillations can take place. These high frequency oscillations are not wanted and reduce overall efficiency. Therefore, to prevent this scenario, hysteresis can be implemented into the design to ensure that inefficient high frequency oscillations are avoided. Hysteresis can be implemented by adding delay between sensing and action. The feedback control system implemented on the boost SPS IC involves a lot of circuitry (the comparator, enabled ring oscillator, buffer, and NMOS). All this circuity produces an inherent delay between sensing and action. An inherent delay produces inherent hysteresis implementation allowing high frequency oscillations to be avoided. This is seen clearly in the simulation of the system.

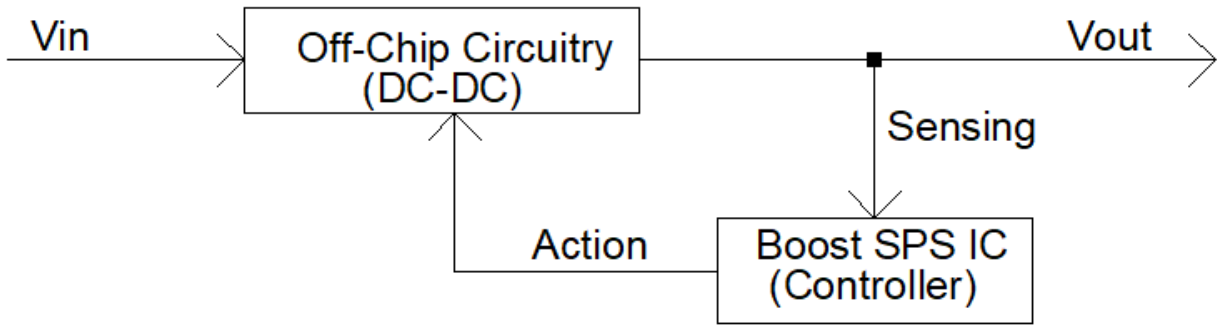

Figure 51: A Block Diagram of the Feedback Control Loop in the Boost SPS System

3.1.6 Enabled Ring Oscillator

A ring oscillator is a string of inverters that produce a digital clock. The ring oscillator implemented in the boost SPS chip circuitry must have an enable. The function of the ring oscillator should be oscillating when enable is high and active low when the enable signal is low.

The Duty Cycle

A design consideration to consider, is the duty cycle of the ring oscillator. The duty cycle contributes to how high the output voltage can be boosted. Additionally, the duty cycle effects

the inductance and capacitance values for the off-chip circuitry. Consider the following equation[viii]:

$$V_{OUT} = \frac{V_S}{1 - D}$$

The maximum output voltage of a boost SPS system is dependent upon two factors, V_S and D. Where V_S is the supply voltage and D is the duty cycle of the ring oscillator. For instance, if the duty cycle is 50% then the maximum V_{out} will be $2 \cdot V_S$. According to the design requirements, our supply voltage will vary from 3.75-5.25V. Therefore, if our supply voltage is 5.25V then our voltage has to be scaled by a factor of 1.43 to get an output voltage of 7.5V. Likewise, if our supply voltage is 3.75V then our voltage has to be scaled by a factor of 2 to get an output voltage of 7.5V. It becomes evident that in our boost SPS system the power supply voltage, V_S, must be multiplied by 1.43 to 2 to get an output voltage of 7.5V. In theory, a 50% duty cycle would work on our design, but it would work poorly. One complication would be that enable would always be on in some situations. Additionally, in the event of a variable boost SPS system (see Section 5.3) the voltage could not be multiplier more than a factor of 2. Therefore, a greater duty cycle is necessary. A duty cycle of 75% will be chosen. A 75% duty will provide a maximum scale factor of 4. However, a question arises: If the duty cycle is 75%, will the scale factor always be 4? The answer is no because the oscillator will not always be enabled. Due to the feedback control loop, the oscillator is controlled by the enable signal that we will call *enable.* Consider the following equation:

$$V_{OUT} = \frac{V_S}{1 - D} \cdot D_E$$

D_E is the duty cycle of *enable*, the controlling signal. Due to the feedback control system (i.e. the boost SPS IC circuitry) the signal enable will implicitly modulate itself to ensure that *Vout* is 7.5V by controlling D_E.

The Frequency

Yet another design consideration to consider is the frequency of the oscillation. Later it will be demonstrated in section 3.2 how frequency is also a factor that determines the selection the inductor and capacitor. Additionally, more design tradeoffs to consider are the following proportionalities:

$$frequency \propto \frac{1}{efficieny}$$

$$frequency \propto power\ supply\ responsiveness$$

We see that as the frequency increases, the efficiency decreases. Additionally, as the frequency increases the power supply responsiveness increases. Power efficiency is a design factor that needs to be optimized. Therefore, the selected frequency should not be too fast or too slow. If it is too fast, the power supply will not be efficient. Or if the selected frequency is too slow the

power supply will not respond quickly in variances in current demand (i.e. pulsed current loads). Therefore, a golden median must be determined. 1MHz was selected to be the frequency.

Creating an Enabled Ring Oscillator

An enabled oscillator can be created by adding a NAND gate within the ring oscillator. When enable goes high, the NAND gate acts like an inverter and allows the oscillation to occur. To the contrary, when enable goes low, the NAND gate prevents the oscillations from occurring. Table 9 illustrates this fact. The non-highlighted portions of the table depict when the oscillator is disabled. Likewise, the grey-highlighted portion depicts when the oscillator is enabled. The NAND gate is specifically placed where it is to ensure that the oscillations start and stop promptly. Additionally, a second NAND gate was used to ensure that the correct duty cycle of 75% was achieved. Finally, a AND gate was used to ensure that when the oscillator is disabled, the oscillations stop on demand. The final enabled ring oscillator schematic and symbol is seen in Figure 52 and 53. The layout of the ring oscillator is seen Figure 54 and Figure 55.

Table 9

enable	*clk*	*ENABLEnandCLK =OSC*
0	0	1
0	1	1
1	0	1
1	1	0

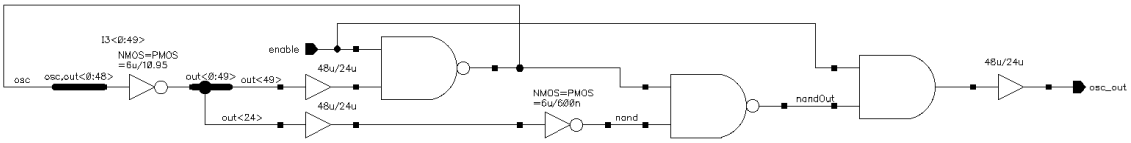

Figure 52: Enabled Ring Oscillator Circuit

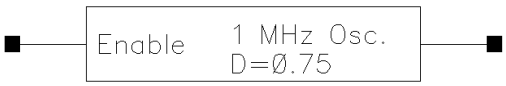

Figure 53: Enabled Ring Oscillator Symbol

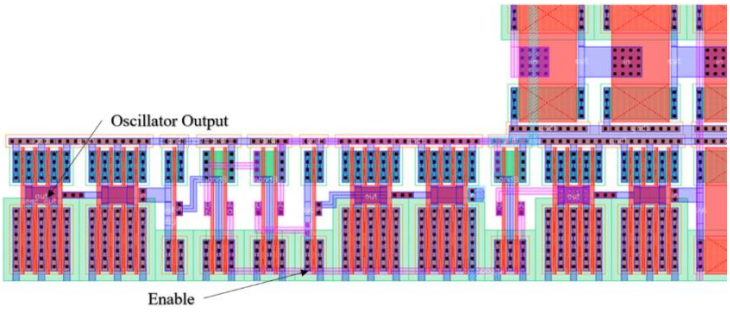

Figure 54: Oscillator Logic Portion of Enabled Ring Oscillator Layout

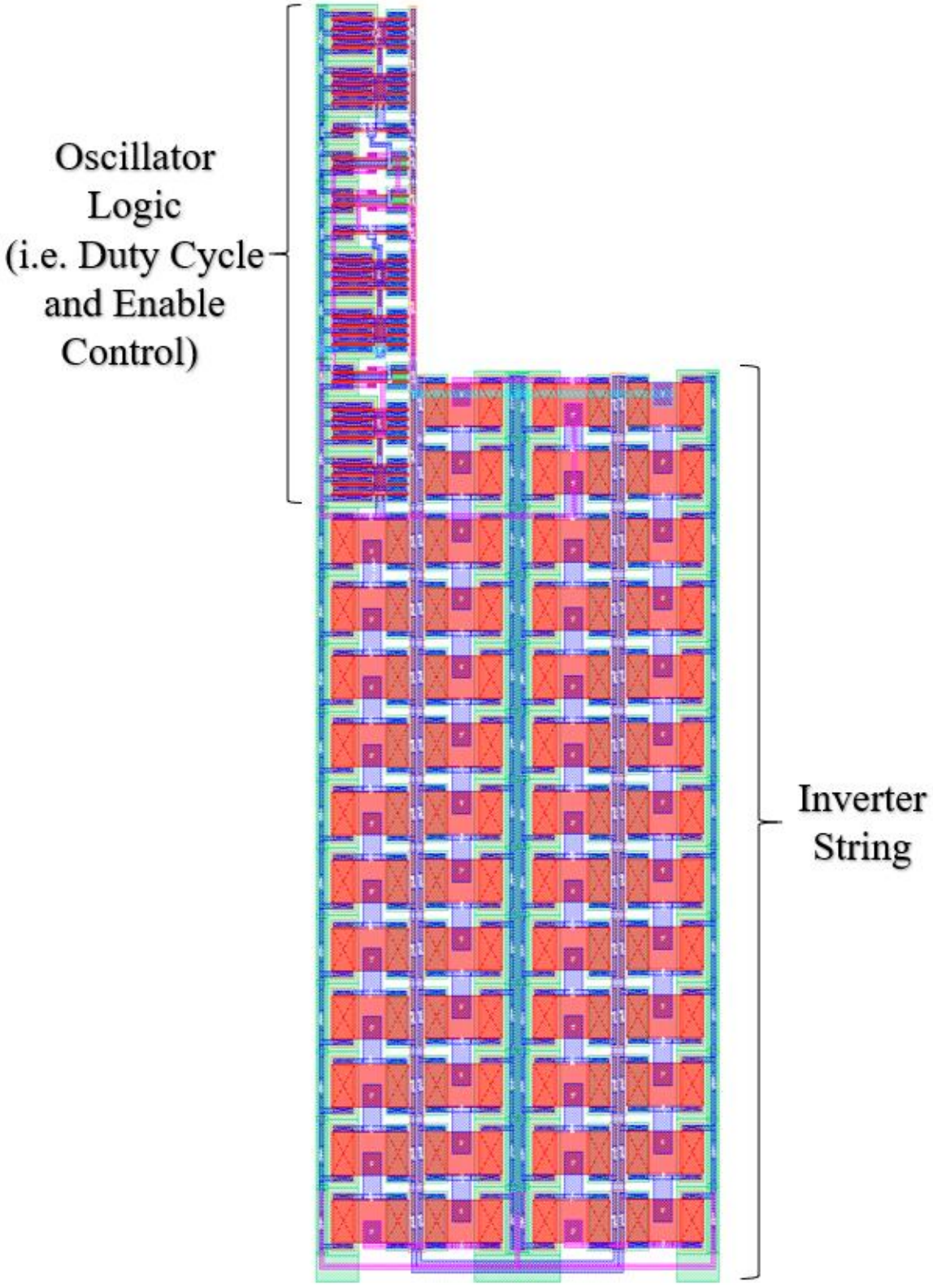

Figure 55: Full Enabled Oscillator Layout

Ring Oscillator Calculations

We know the following regarding the C5 process:

$$C_{ox}^{I} = 2.5 \, {fF}/{\mu m^2}$$

$$R_p^I = 40k\Omega$$

$$R_n^I = 20k\Omega$$

Regarding our long length inverters:

$$w = w_p = w_n = 6\mu m$$

$$l = l_p = l_n = 10.95\mu m$$

Therefore:

$$C_{ox,p} = C_{ox,n} = C_{ox}^{I} \cdot w \cdot l = 2.5 \, {fF}/{\mu m^2} \cdot 6\mu m \cdot 10.95\mu m = 2.5f \cdot 65.7 = 164.25fF$$

$$C_{TOTAl} = \frac{5}{2}\left(C_{ox,p} + C_{ox,n}\right) = 5 \cdot 164.25fF = 821.25fF$$

$$R_p = R_p^I \cdot \frac{l}{w} = 40k \cdot \frac{10.95}{6} = 73k$$

$$R_n = R_n^I \cdot \frac{l}{w} = 20k \cdot \frac{10.95}{6} = 36.5k$$

$$t_{PLH} = 0.7 \cdot R_p \cdot C_{TOTAl} = 0.7 \cdot 73k \cdot 821.25fF = 41.966ns$$

$$t_{PHL} = 0.7 \cdot R_n \cdot C_{TOTAl} = 0.7 \cdot 36.5k \cdot 821.25fF = 20.983ns$$

$$t_{PLH} + t_{PHL} \quad = 62.949ns$$

Consider the following equation[ix]:

$$f_{OSC} = \frac{1}{n(t_{PLH} + t_{PHL})}$$

$$n = \frac{1}{1MHz \cdot 62.949ns} = \boxed{\textbf{16 } \boldsymbol{inverters}}$$

A ring oscillator with 16 inverters was created, but the oscillator did not have frequency of 1MHz. Therefore, the number of inverters were adjusted until 1 MHz was achieved. Currently, the ring oscillator has 50 inverters and a NAND gate.

Ring Oscillator Simulation

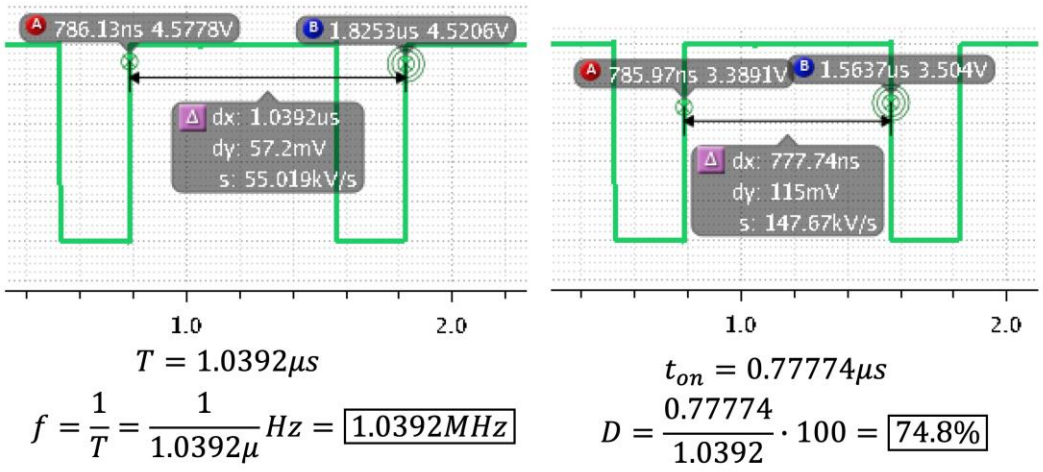

Figure 56: Determining the Frequency and the Duty Cycle of the Oscillator

Figure 56 proves by both simulation and calculation that the frequency generated by oscillator is 1.04 MHz and the duty cycle is 74.8%.

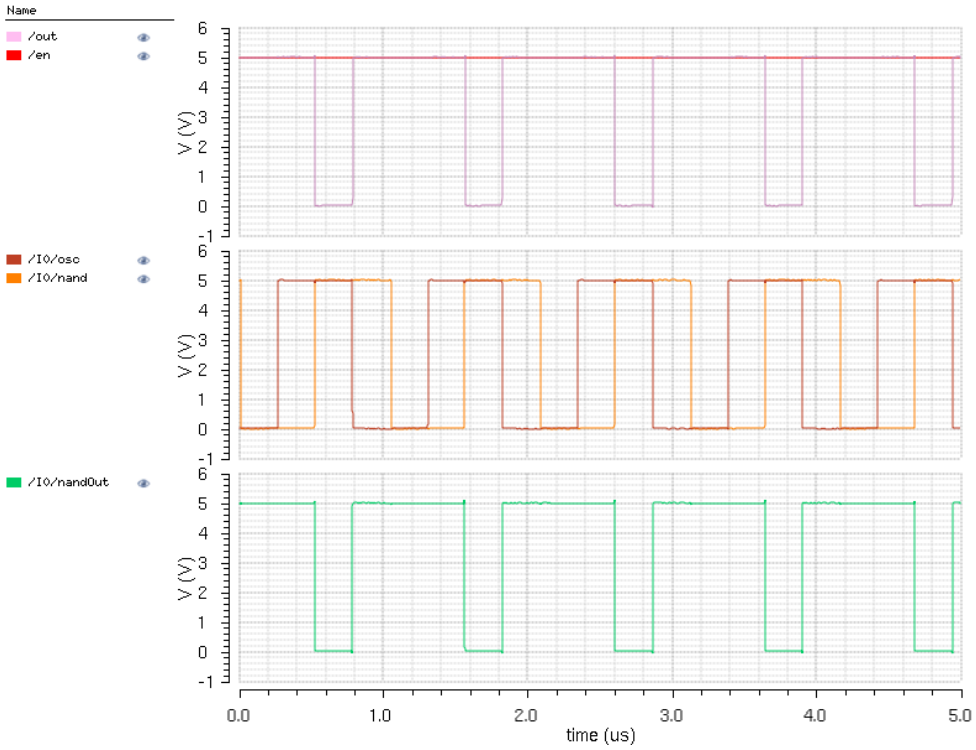

Figure 57: Further Oscillator Operation – 75% Duty Cycle Generation

Figure 57 depicts three trisections of simulation. The top trisection sows that when enable is high, oscillations occur. The middle trisection shows the two inputs of the second NAND gate in the enabled ring oscillator. We see that one input is delayed by *T/4*. The output of the NAND gate is active low when both inputs are active high. Finally, in the bottom trisection we see that a

75% duty cycle is achieved. Figure 58 demonstrates that when the enable signal is low, there is no oscillation. Additionally, while the enable signal is high there is oscillation. Due to the final AND gate the oscillations stop immediately when enable signal goes low.

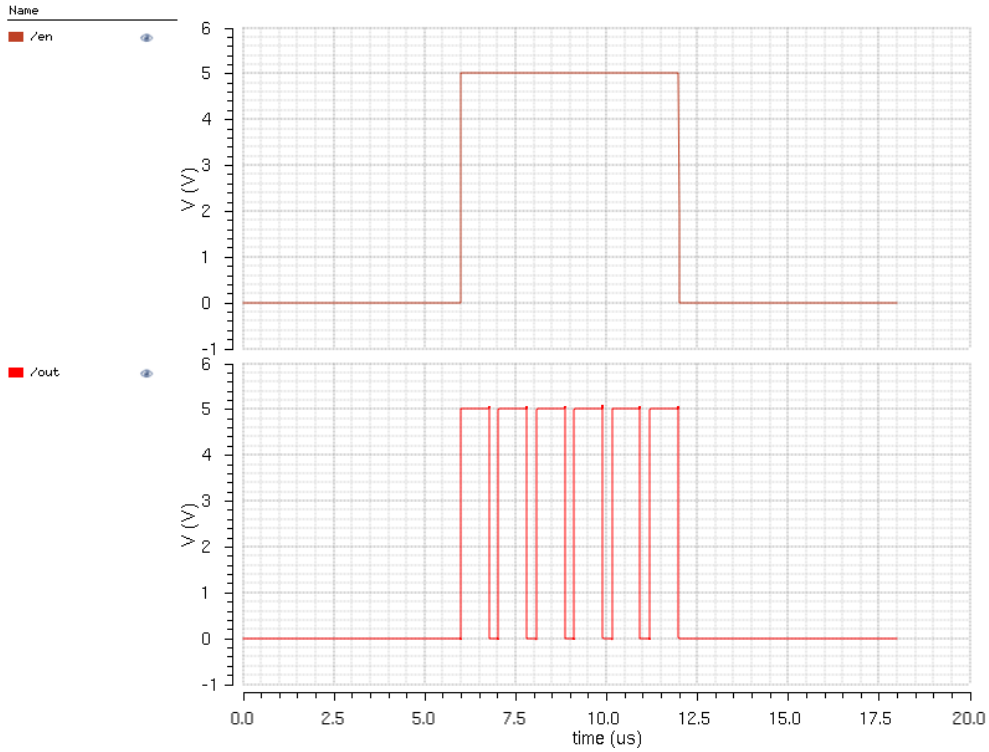

Figure 58: Even Further Oscillator Operation – Enable Demonstration

3.1.7 Large Switching NMOS

A large switching NMOS is implemented in the boost SPS system to act like a switch. Therefore, ideally, when the switch is closed, the node *VSW* should be pulled down to ground. For this to occur, the drain-to-source resistance of NMOS should be small. Therefore, the NMOS switch should have a large width and minimum length. The geometry of the NMOS switch was decided to be 2700µm by 0.6µm. The drain-to-source capacitance of the NMOS can be calculated in the following manner:

$$R_n^I = 20k\Omega$$

$$R_n = R_n^I \cdot \frac{l}{w} = 20k \cdot \frac{0.6}{2700} = \boxed{\mathbf{4.444\Omega}}$$

Consequently, due to the size of the NMOS, the transistor has an inherent associated capacitance. This capacitance will be called the load capacitance of the NMOS. The load capacitance of the switching NMOS can be calculated by the following set of equations:

$$C_{ox}^I = 2.5\ {}^{fF}\!/_{\mu m^2}$$

$$C_{LOAD} = C_{ox}^I \cdot w \cdot l$$

Where *w* and *l* are the width and length of the NMOS respectively.

$$C_{LOAD} = 2.5\ fF \cdot 2700 \cdot 0.6 = \boxed{\mathbf{4.05\ pF}}$$

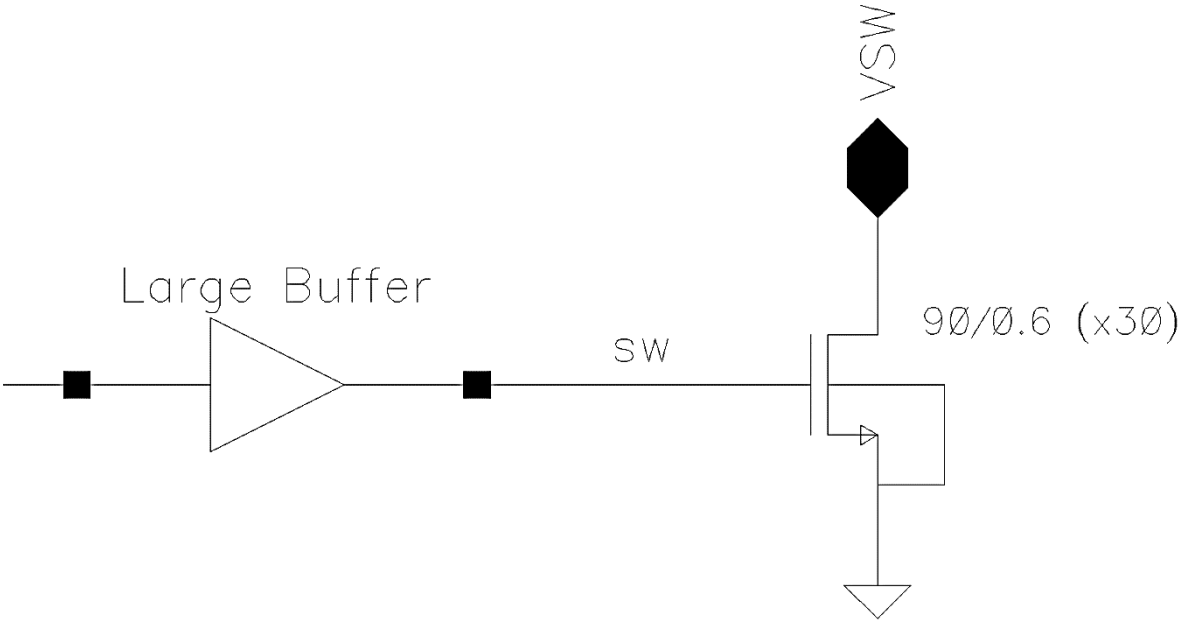

Figure 59: Large Buffer with Large Switching NMOS

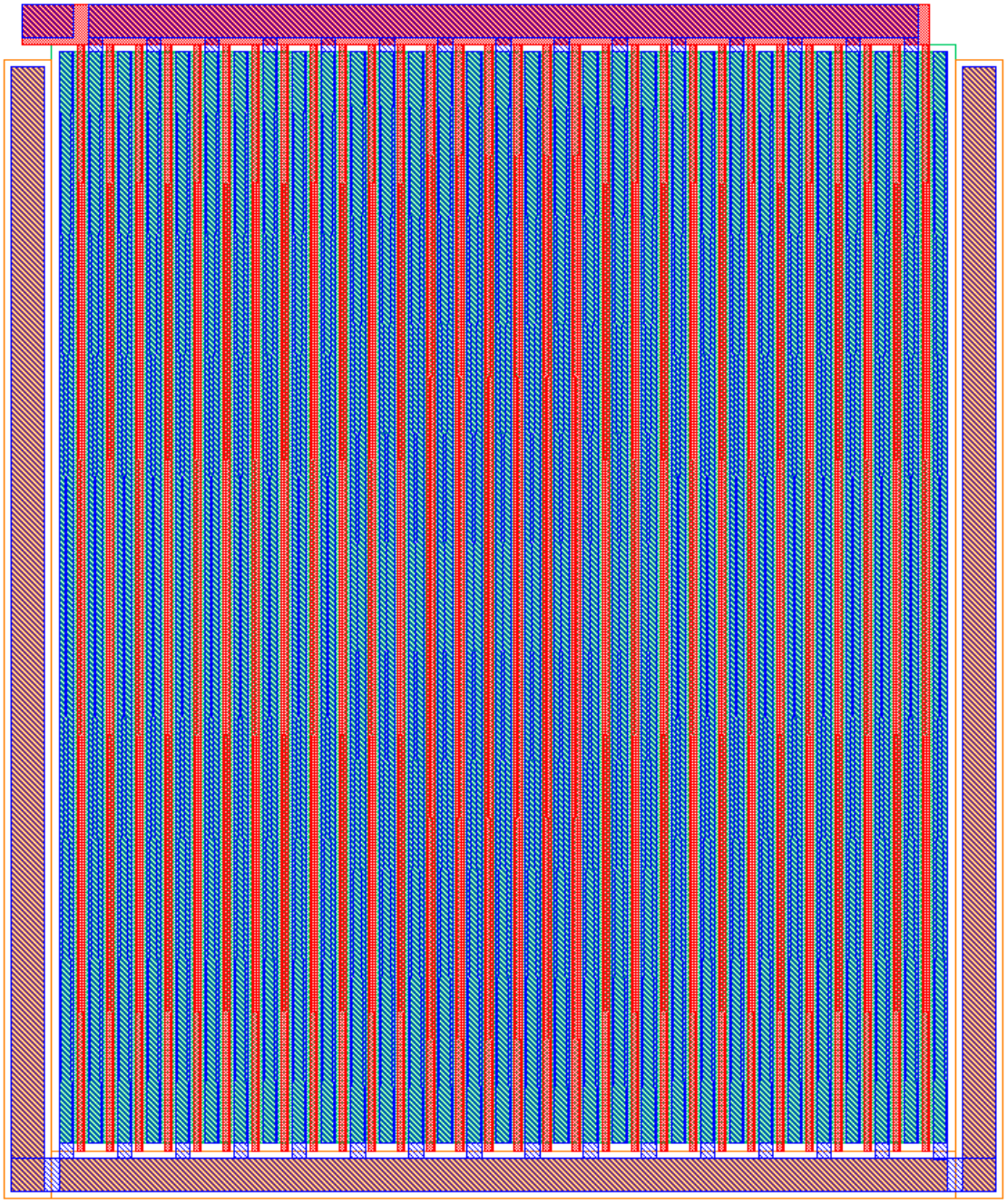

Figure 60: Large Switching NMOS Layout

3.1.8 Large Buffer

The signal output from the enabled ring oscillator will not be strong enough to drive a huge switching NMOS, due to the NMOS's input capacitance of 4.05pF. Therefore, a buffer must be designed to ensure that the signal is able to drive the NMOS with such a capacitance. The following buffer was designed to drive large capacitive loads according to the topology given in Figure 51.

$$For\ each\ stage:$$
$$A \cdot \frac{w_p}{l_p};\ A \cdot \frac{w_n}{l_n}$$
$$Where, A = a^{n-1}, \text{see below:}$$

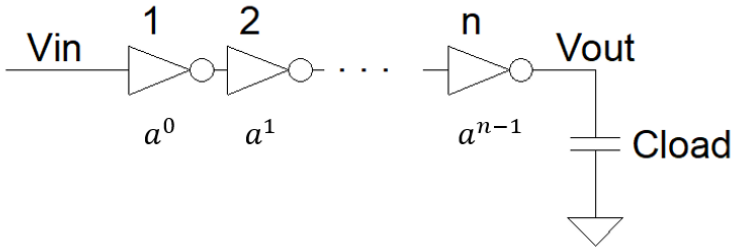

Figure 61: Typology of Buffer to Drive Large Loads

After seeing the above topology, it became evident that an *A* value must be selected. The *A* value selected was 4. Now the question is, how many stages? The following series of equations can be used to calculate the number of stages[x].

$$N \cdot \ln A = ln \frac{C_{load}}{C_{in1}}$$

While considering the following to be true:

$$C_{ox,n} = C_{ox}^{I} \cdot W_n \cdot L_n = 2.5\ {}^{fF}\!/_{\mu m^2} \cdot 6\mu m \cdot 0.6\mu m = 9fF$$

$$C_{ox,p} = C_{op}^{I} \cdot W_p \cdot L_p = 2.5\ {}^{fF}\!/_{\mu m^2} \cdot 12\mu m \cdot 0.6\mu m = 18fF$$

The input capacitance of the first inverter can be found by Miller's theorem:

$$C_{in} = \frac{3}{2}(9fF + 18fF) = 40.5fF$$

Let A =4, and now we may use the first equation and solve:

$$N \cdot \ln 4 = ln \frac{4.05pF}{40.5fF}$$

$$N \cdot 1.386 = ln \frac{4.05pF}{40.5fF}$$

$$N \cdot 1.386 = 4.605$$

$$N = \frac{4.605}{1.386} = \boxed{\mathbf{3.3\ stages}}$$

By calculations the necessary number of stages required to drive the load capacitance of the switching NMOS is 3.3 stages. One however, cannot have 3.3 stages. Therefore, the buffer should have 4 stages.

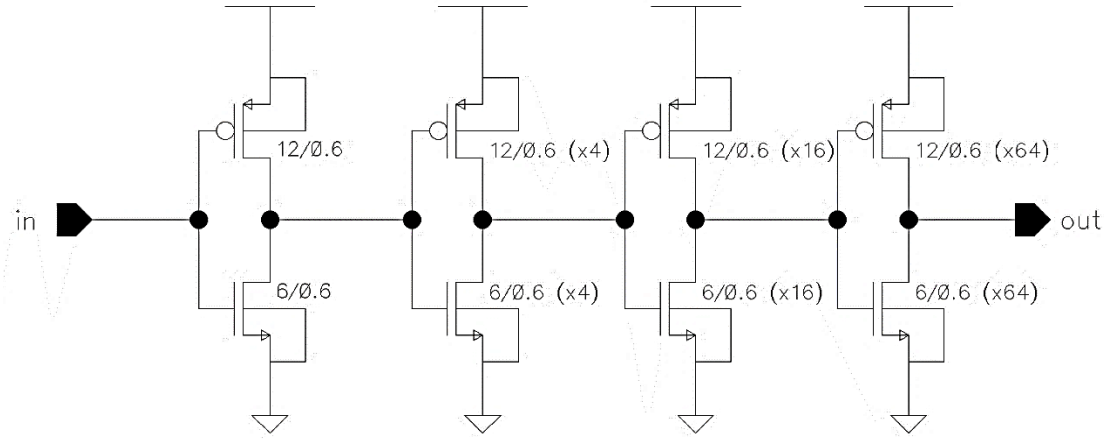

Figure 62: Large Buffer Circuit

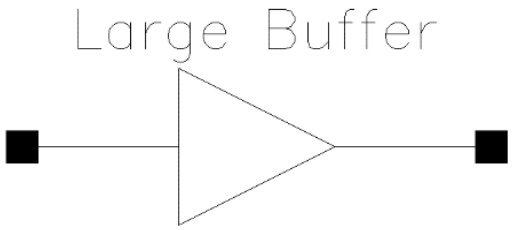

Figure 63: Large Buffer Symbol

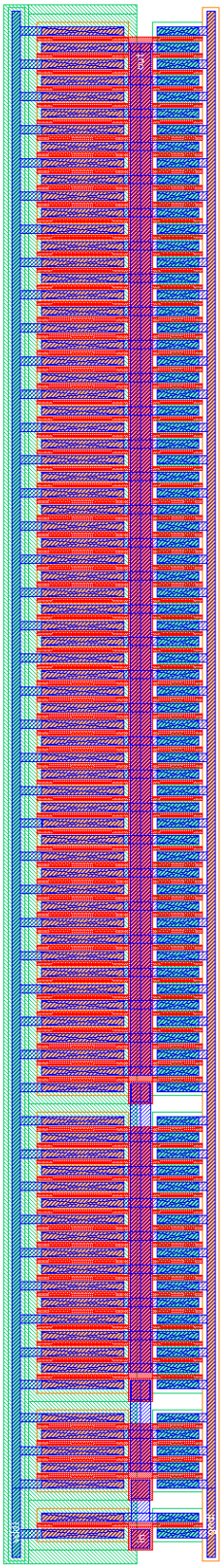

Figure 64: Large Buffer Layout

1.1 Design of the Off-Chip Circuitry

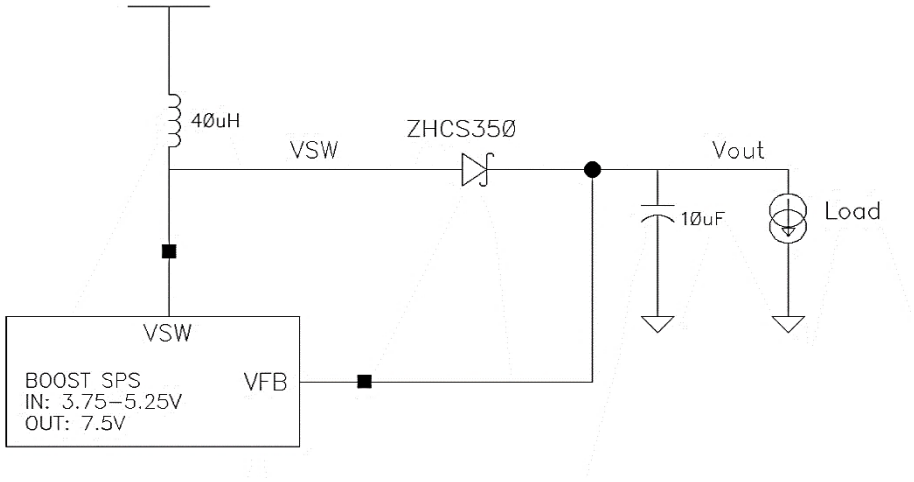

Figure 65: The Boost SPS IC with Off-Chip Circuitry

The boost SPS IC alone is unable to produce a functioning boost SPS system. Three crucial components are necessary to create a working boost SPS system. An inductor, Schottky diode, and capacitor must be selected. While selecting the values for these components; circuit performance, component size, and component cost were all taken into consideration when selecting the component. For a quantity of one, the total cost of these three components are $1.08.

1.1.1 Inductor

Figure 66: A Graphical Representation of the MLZ2012N100LT000 Inductor

The inductor in the boost SPS can be calculated by the following formula[xi]:

$$L = \frac{V_{OUT} \cdot D \cdot (1 - D)}{f \cdot \Delta i_L}$$

Where:

$$I_L = \frac{I_R}{1-D} = \frac{20mA}{1-0.75} = 80mA$$

We can set the current change in the inductor to be 5% the maximum average current:

$$\Delta i_L = 80mA \cdot 0.05 = 4mA$$

Finally, we may use the initial formula to solve for the inductance:

$$L = \frac{7.5 \cdot 0.75 \cdot (1-0.75)}{1MHz \cdot 4mA} = \boxed{\mathbf{351.563\mu H}}$$

The calculated inductance was much greater than the final selected inductance. The calculated result was used as a ballpark solution. From this ballpark solution, the inductance was further optimized to minimize ripple voltage.

The MLZ2012N100LT000[xii] 10µH inductor was chosen. This inductor is a 0805 surface mount device; allowing for minimized size on the board. A huge selling point of this inductor is the price. The price for a single diode is $0.14. However, at larger quantities, the diode decreases in price according to Table 10[xiii]. To get the desired inductance multiple inductors can be added in series.

Table 10: The Unit Price of the MLZ2012N100LT000 Inductor at Varying Price Breaks

Price Break	Unit Price
1	$0.14
10	$0.13
100	$0.09
500	$0.07
1,000	$0.06

1.1.2 Schottky Diode

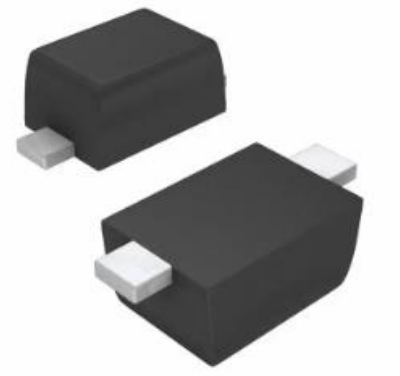

Figure 67: Graphical Representation of the ZHCS350's SOD-23 Package

The diode used in this design is the Diodes Incorporated's ZHCS350 Surface Mount Schottky Barrier Diode[xiv]. The diode was selected because its low capacitance of 3.3pF. Additionally, the forward voltage drop is 0.81V. Interestingly, in Diodes Incorporated's overview on the diode, one of the listed applications of the diode include DC-DC converters and charger circuits. The price for a single diode is $0.41. However, at larger quantities, the diode decreases in price according to Table 11[xv].

Table 11: The Unit Price of the ZHCS350 Diode at Varying Price Breaks

Price Break	Unit Price
1	$0.41
10	$0.35
100	$0.24
500	$0.19
1,000	$0.15

Maximum Ratings @T_A = 25°C unless otherwise specified

Characteristic		Symbol	Value	Units
Continuous Reverse Voltage		V_R	40	V
Continuous Forward Current		I_F	350	mA
Average Peak Forward Current; D.C. = 50%		I_{FAV}	510	mA
Non Repetitive Forward Current	t ≤ 100μs	I_{FSM}	4.2	A
	t ≤ 10ms		910	mA

Thermal Characteristics

Characteristic		Symbol	Value	Unit
Power Dissipation, T_A = 25°C	(Note 5)	P_D	285	mW
	(Note 6)		330	
Thermal Resistance, Junction to Ambient	(Note 5)	$R_{\theta JA}$	350	
	(Note 6)		303	
Junction Temperature		T_J	125	°C
Storage Temperature Range		T_{STG}	-55 to +150	°C

Notes: 5. For a single device surface mounted on 25mm x 25mm x 1.6mm FR4 PCB with high coverage of 1oz copper in still air conditions.
6. As Note 5, measured at t ≤ 5 secs.

Figure 68: Maximum Ratings and Thermal Characteristics as given by the ZHCS350 datasheet

Electrical Characteristics @T_A = 25°C unless otherwise specified

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
Reverse Breakdown Voltage	$V_{(BR)R}$	40	60	-	V	I_R = 100μA
Forward Voltage (Note 7)	V_F	-	300	325	mV	I_F = 30mA
		-	335	370		I_F = 50mA
		-	405	460		I_F = 100mA
		-	730	810		I_F = 350mA
Reverse Current	I_R	-	7	12	μA	V_R = 30V
Diode Capacitance	C_D	-	3.3	6	pF	f = 1MHz, V_R = 25V
Reverse Recovery Time	trr	-	1.6	-	ns	Switched from I_F = 100mA to I_R = 100mA Measured @ I_R = 10mA

Notes: 7. Measured under pulsed conditions. Pulse width = 300μS. Duty cycle ≤ 2%.

Figure 69: Electrical Characteristics as given by the ZHCS350 datasheet

The ZHCS350 SPICE Model (provided by Diodes Incorporated)

```
*ZETEX ZHCS350 Spice Model v1.0 Last Revised 26/04/2005
*
.MODEL ZHCS350 D IS=1.35e-7 N=1.06 ISR=6e-7 NR=1.1 RS=0.9
+IKF=0.2 BV=65 TRS1=6.5e-3 XTI=2 EG=0.63 Fc=0.5 CJO=18.84e-12
+M=0.5 VJ=0.33 TT=1.6e-9
*
*$
*
```

1.1.3 Capacitor

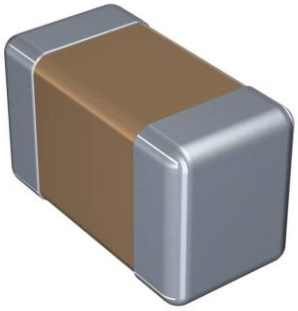

Figure 70: A Graphical Representation of the C0603C106M8PAC7867 10µF Surface Mount Capacitor

The capacitor can be selected based upon the following formula[xvi]:

$$C_{min} = \frac{D}{R \cdot f \cdot \left({}^{\Delta V_{out}}/_{V_{out}}\right)} = \frac{0.75}{R \cdot 1MHz \left({}^{\Delta V_{out}}/_{7.5V}\right)}$$

Where, R represents the impedance of the load at the maximum current and ΔV_{out} represents the ripple voltage. Now, let us assert a ripple voltage less than 15mV. The following equation can be valuated to find the capacitance.

$$C_{min} = \frac{0.75}{375\Omega \cdot 1MHz\left({}^{0.015}/_{7.5V}\right)} = \boxed{\boldsymbol{1\mu H}}$$

The final capacitance decided upon was 10µF to further minimize ripple voltage. The capacitor to be selected was the C0603C106M8PAC7867[xvii] capacitor by KEMET. This capacitor is a 10µF 0603 surface mount capacitor with a voltage rating 10V. The price for a single capacitor is $0.53. However, at larger quantities, the diode decreases in price according to Table 12[xviii].

Table 12

Price Break	Unit Price
1	$0.53
10	$0.37
100	$0.24
500	$0.18
1,000	$0.15

It should be noted that selecting the capacitor requires an analysis of design tradeoffs. For instance, the greater the capacitance, the smaller ripple voltage. However, larger capacitance sizes result in increased price and decreased power supply responsiveness. If power supply responsiveness is preferred over the ripple voltage amount, then a smaller capacitor should be selected. In this project, the responsiveness was not a specified design requirement. Therefore, smaller ripple voltage was prioritized over quick responsiveness. It is due to these reasons that a larger capacitance was selected. Size was also a consideration; therefore, a large surface mount capacitor was finally selected.

2. Simulation of the Boost SPS System

Now that the Boost SPS IC and off-chip circuitry has been designed, the entire boost SPS system may be simulated. **The complete summary of the simulation results can be found in Section 2 (Summary of Performance).** To provide expansive system simulation in a wide range of operating conditions; the temperature, VDD, and load will all be varied. Under all conditions, the minimum value of *Vout*, average *Vout*, maximum value of *Vout*, ripple voltage, average current drawn from the power supply, and the efficiency will all be considered. It should be noted that the efficiency was calculated by the following formula:

$$Efficiency = \frac{Power\ Delivered}{Power\ Spent} = \frac{V_{OUT} \cdot I_{LOAD}}{V_{DD} \cdot average(I(V_{DD}))}$$

The average voltage and average current were found by sending the signals to the Cadence Virtuoso Visualization & Analysis XL Calculator and setting the calculator to calculate the average value.

2.1 Operation

The following three figures demonstrate the general operation of the boost SPS system. In the following figure we see that the NMOS is being modulated at precisely the correct signal pattern that is needed to ensure that the output voltage is 7.5V. It is also apparent that *VSW*, is pulled down to ground when the switch is on, due to the NMOS's low drain-to-source resistance. This proves that our large buffer and switching NMOS are each the appropriate size.

Regarding simulation in the following three figures:

VDD = 3.75V

Current = 20mA

Temperature = 27 ºC

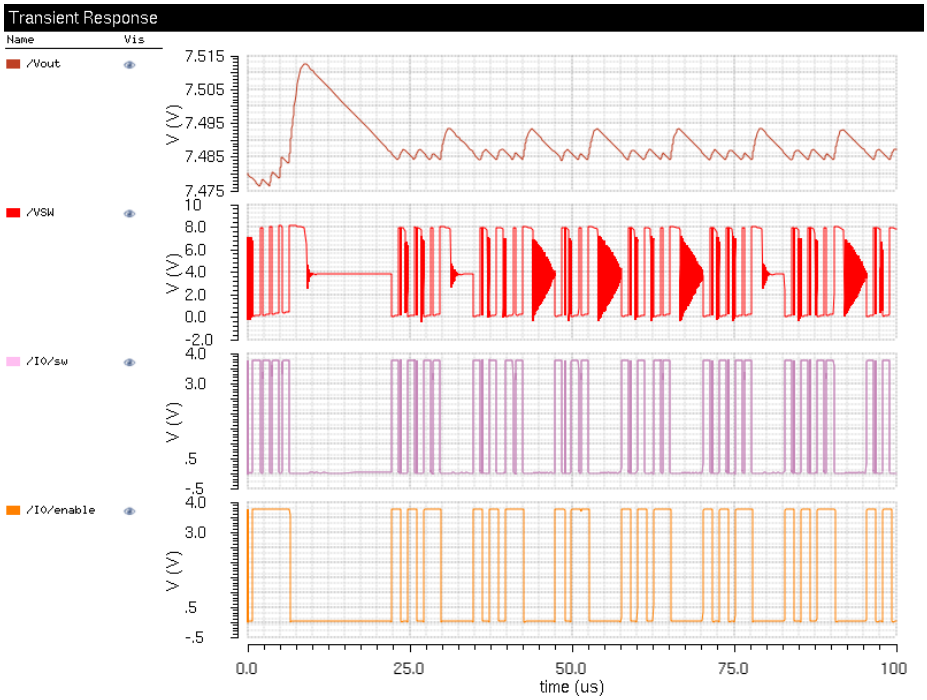

Figure 71:General Operation of the Boost SPS System

The next simulations show the output of the bandgap voltage reference and the attenuated *Vout* signal. Here we see that the compactor is properly working to ensure that the output is forced to 7.5V. The DC bias of the attenuated *Vout* is below the reference voltage because of the switching point of the comparator.

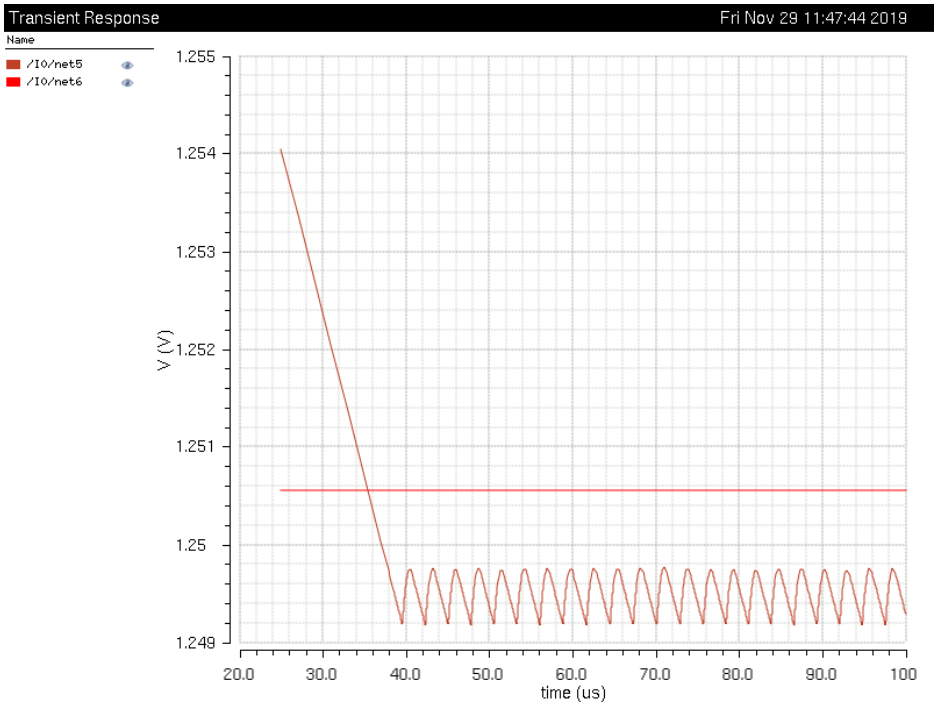

Figure 72: Reference from the Bandgap Voltage and the Attenuated Vout

The next figure depicts the current through the inductor along with the output voltage. These signals can then be compared to the enable signal and one can see that, these signals correlate properly when compared to the enable signal.

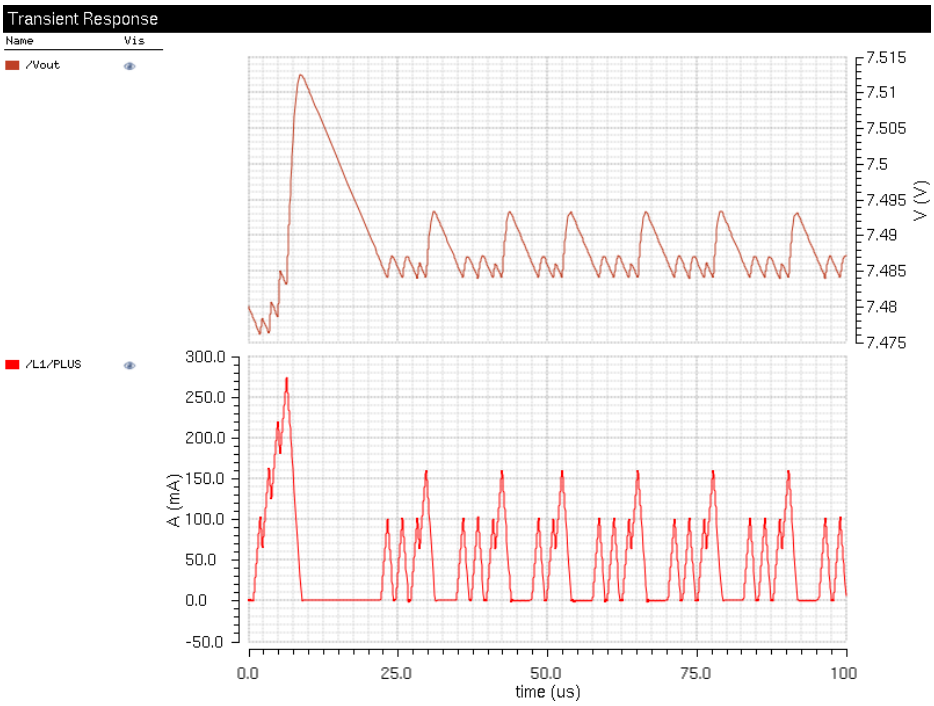

Figure 73: The Output Voltage and The Current Through the Inductor

2.2 Varying Temperature

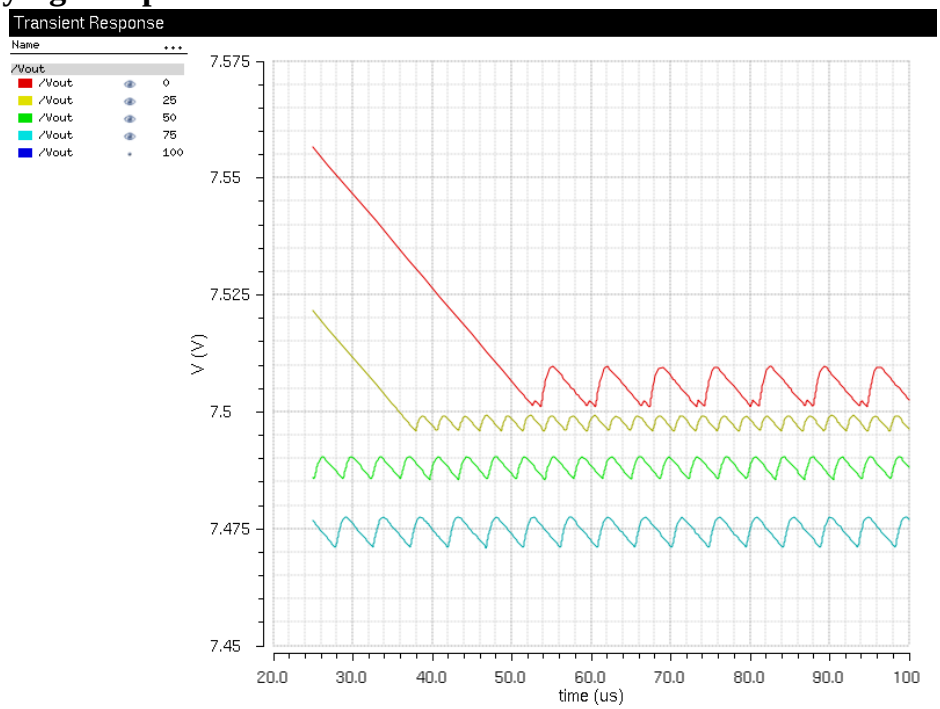

Figure 74: Transient Simulation at Varying Temperatures

The designed boost SPS has a good response to temperature variance. Interestingly, it is apparent that the boost SPS's response to temperature is CTAT. As the temperature increases, *Vout* decreases. The boost SPS is CTAT because the bandgap reference voltage is also CTAT. The boost SPS was designed to have the value of *Vout* closest to 7.5V at room temperature (27 ºC). The ripple voltage averages at 7.336mV and the efficiency averages at 88.73% across the specified temperature range. Also, a trend is identified regarding temperature and the boost SPS system efficiency, as the temperature increases, so does the efficiency.

Set Parameters for Simulation:

Load Current = 20mA

VDD = 4.5 V

Temperature Range: 0-100 ºC

Table 13: Average Values for Set Parameters While Varying Temperature

	Min. Vout (V)	**Avg. Vout (V)**	**Max. Vout (V)**	**Ripple (mV)**	**Avg(I(VDD)) (mA)**	**Efficiency (%)**
Average	7.482	7.486	7.489	7.336	37.59	88.73

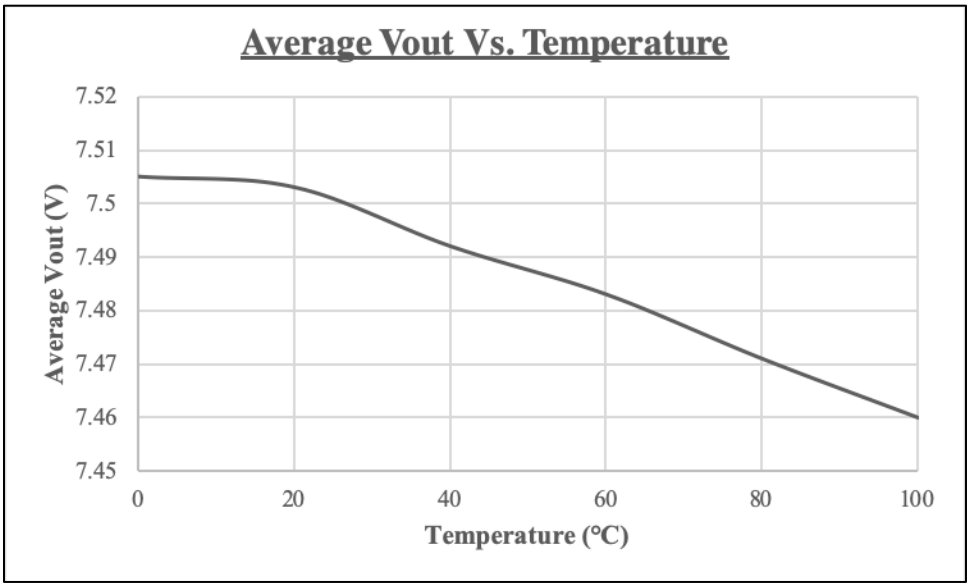

Figure 75: Average Vout Vs. Temperature Plot

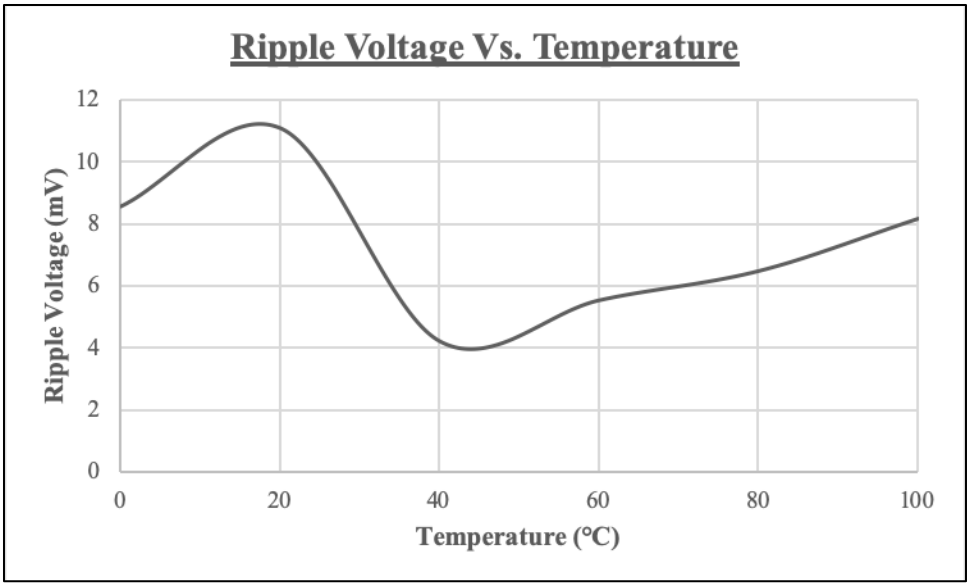

Figure 76: Ripple Voltage Vs. Temperature Plot

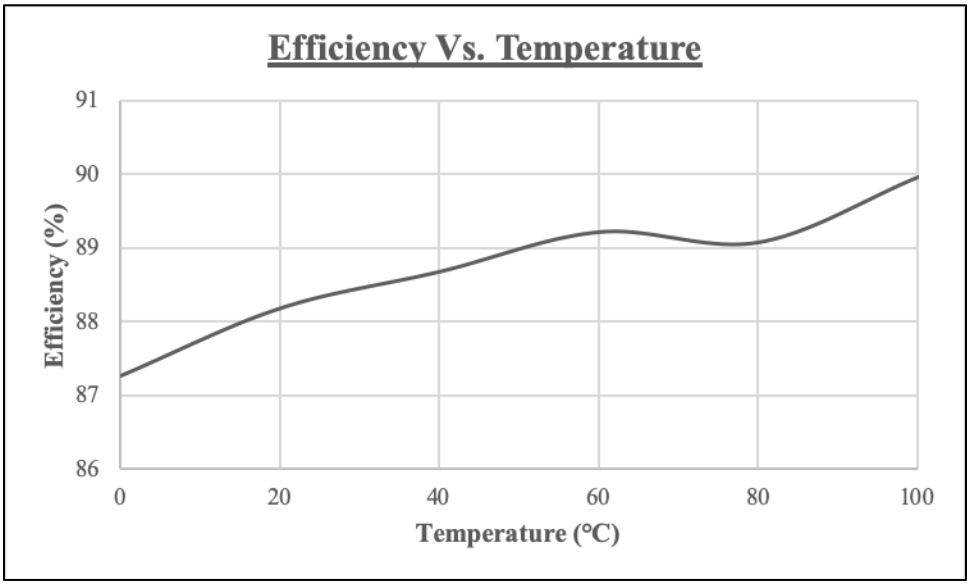

Figure 77: Efficiency Vs. Temperature Plot

2.3 Varying VDD

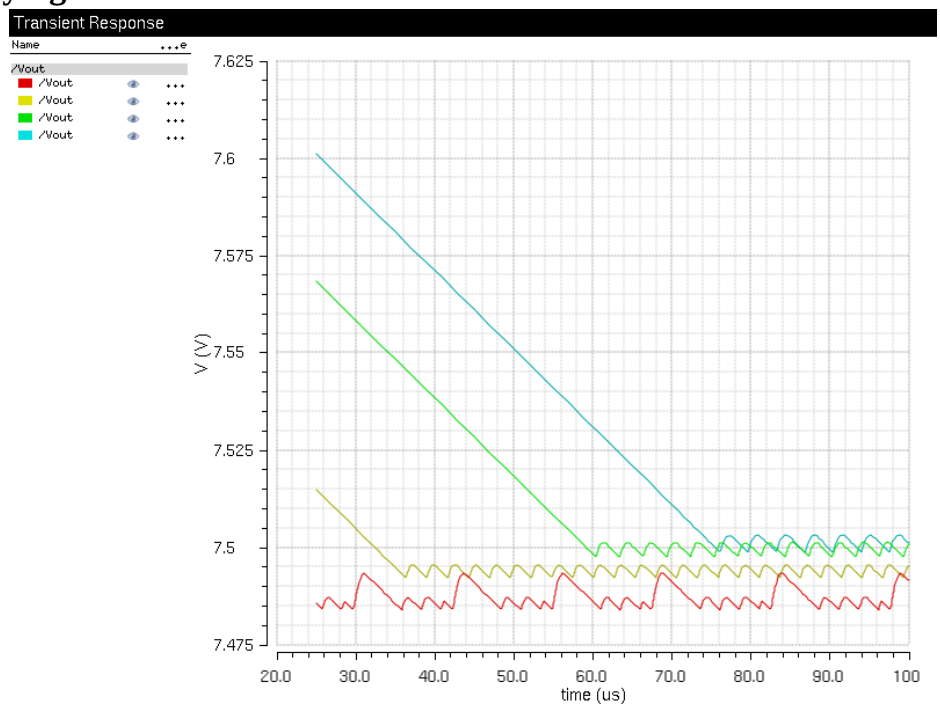

Figure 78: Transient Simulation of Varying VDD

According to the design requirements, the design must be able to accommodate power supply voltages ranging from 3.75-5.25V. The implemented feedback control system ensures that the power supply voltage is scaled properly. As seen in Table 14, the average *Vout*, minimum *Vout*, and maximum *Vout* are all near to the target voltage of 7.5V. The ripple voltage averages at 5.403mV and the efficiency averages at 88.03% across the specified temperature ranges. Two, trends were clearly demonstrated in our simulations. The first trend is that that as VDD increases, the average *Vout* also increases. This is because of the bandgap reference. Yes, as demonstrated in section 3.1.4, the bandgap reference remains *relatively steady* at power supply variances. Simply put, *relatively steady* is not perfect. As the bandgap voltage reference increases due to the power supply voltage increasing, the average *Vout* of the boost SPS system will also increase.

Set Parameters for Simulation:

Load Current = 20mA

Temperature = 27ºC

VDD Range: 3.75-5.25V

Table 14: Average Values at Set Parameters While Varying VDD

	Min. Vout (V)	**Avg. Vout (V)**	**Max. Vout (V)**	**Ripple (mV)**	**Avg(I(VDD)) (mA)**	**Efficiency (%)**
Average	7.494	7.496	7.499	5.403	38.28	88.03

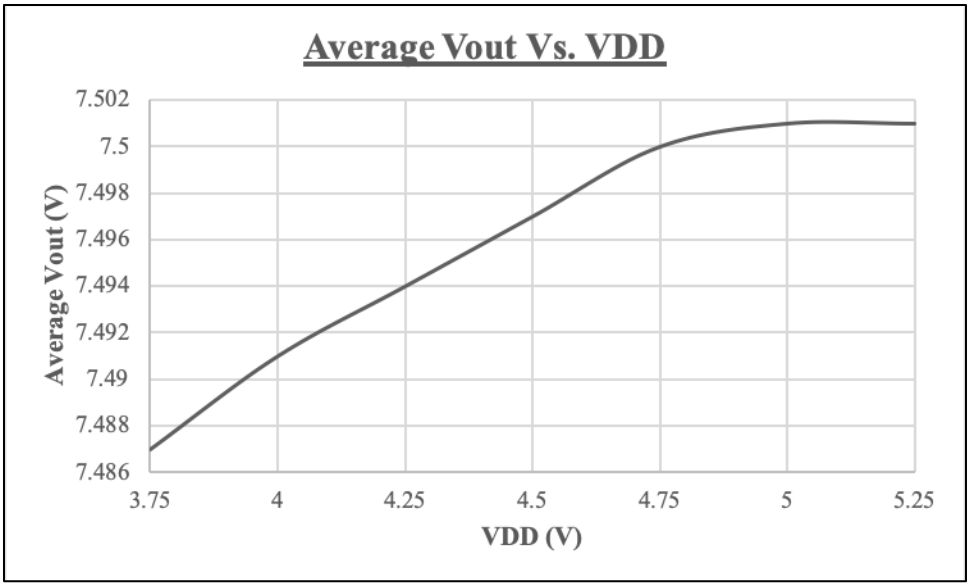

Figure 79: Average Vout Vs. VDD Plot

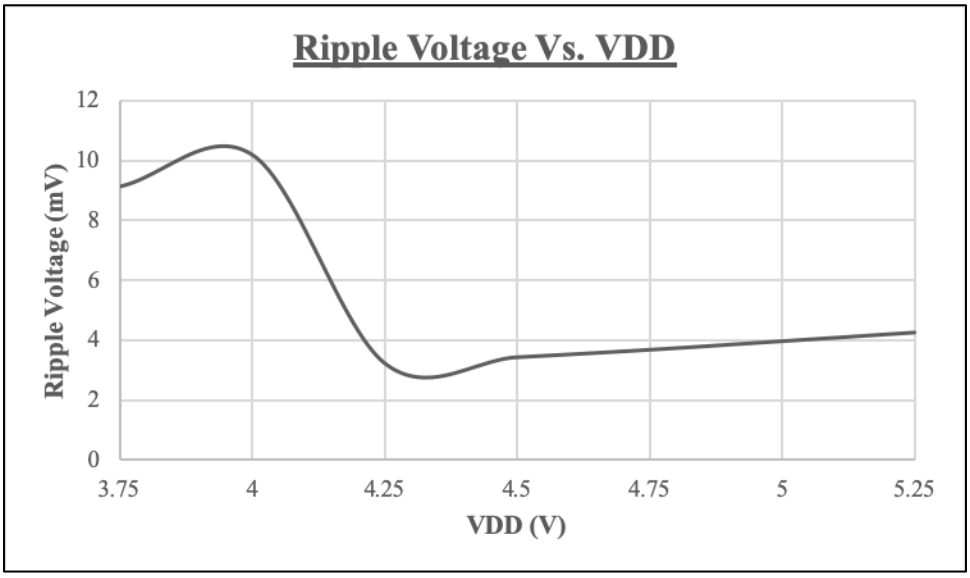

Figure 80: Ripple Voltage Vs. VDD Plot

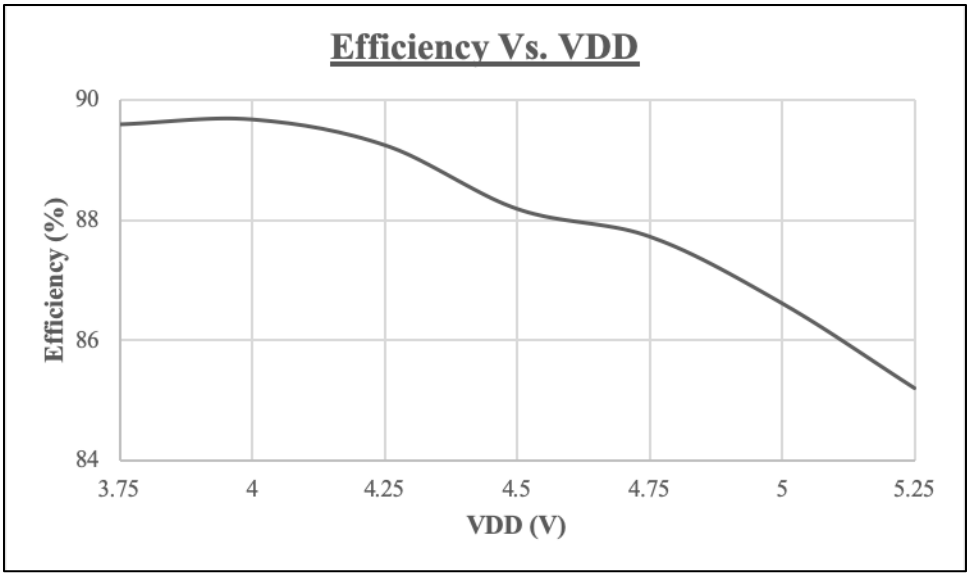

Figure 81: Efficiecny Vs. VDD Plot

2.4 Varying Load

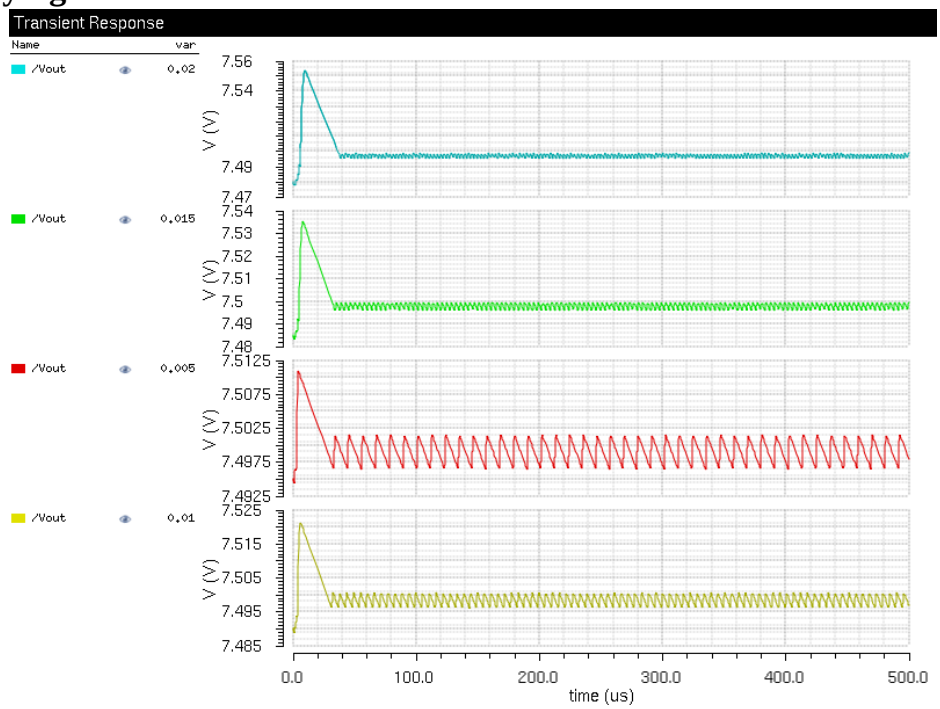

Figure 82: Transient Simulation of varying Load

According to the specified design requirements the design must accommodate the loads of 0-20mA. Simulations proved that as the load increases, *Vout* and the ripple voltage decreases. However, simulations also confirmed that as the load increases, the efficiency also increases. Why does this occur? Consider that the boost SPS system draws a certain amount of current regardless of circuit operation. Therefore, at lower loads. The current draw due to the boost SPS system itself plays a larger role in the net current causing the efficiency to be lower. However, at

higher loads, the current draw due to the boost SPS plays a smaller role in the net current drawn from the power supply.

Set Parameters for Simulation:

VDD = 4.5V

Temperature = 27 ºC

Load Range: 0-20mA

Table 15: Average Values at Set Parameters While Varying Load

	Min. Vout (V)	**Avg. Vout (V)**	**Max. Vout (V)**	**Ripple (mV)**	**Avg(I(VDD)) (mA)**	**Efficiency (%)**
Average	7.496	7.498	7.500	4.23	20.32	82.10

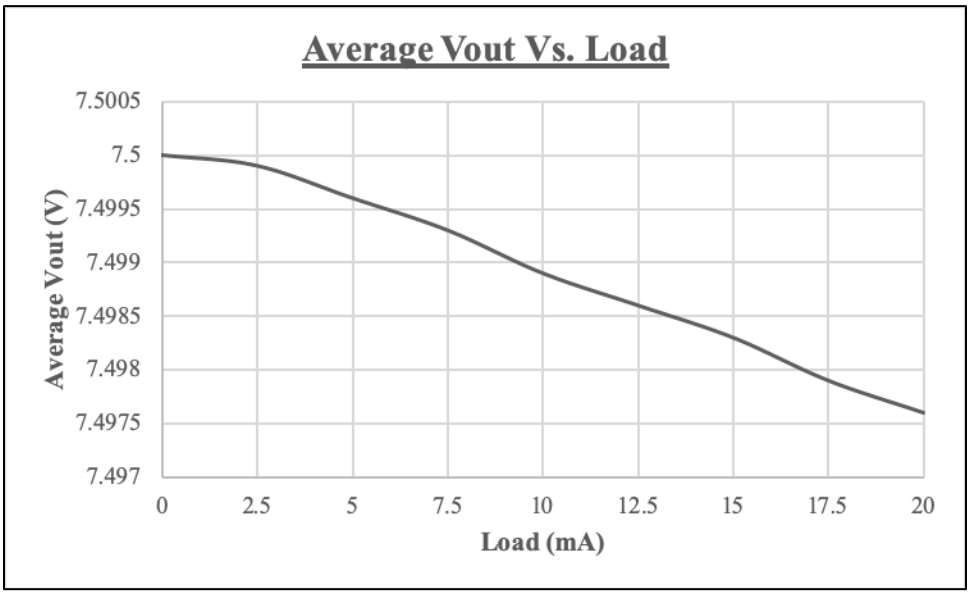

Figure 83: Average Vout Vs. Load Plot

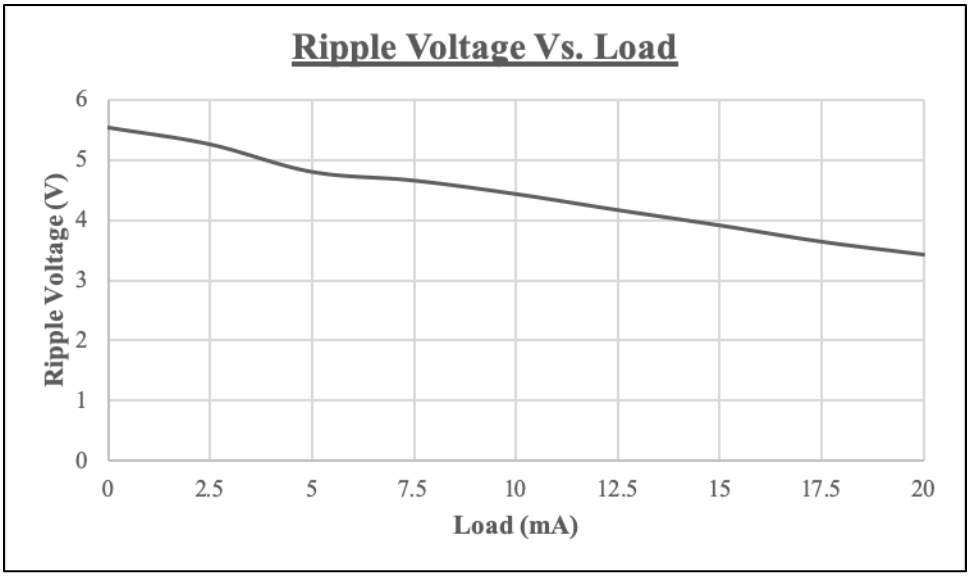

Figure 84: Ripple Voltage Vs. Load

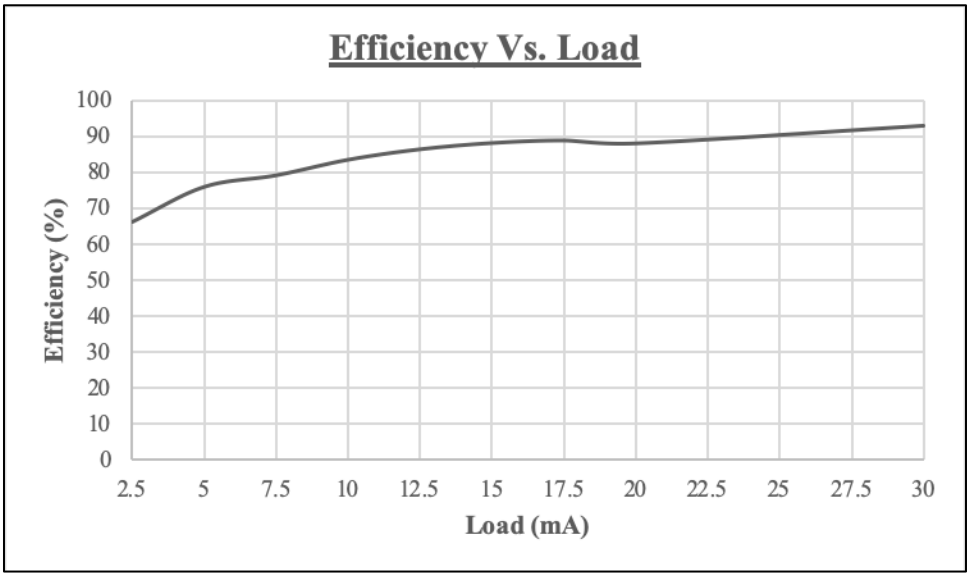

Figure 85: Efficiency Vs. Load

2.5 Pulsed Current Source

One advantage of implementing a feedback control loop in the boost SPS system design, is the ability for the system to automatically accommodate for varying temperatures, supply voltages, and loads. Suppose the load itself varies as function of time. How will the boost SPS system respond to such a load? In the following plot a pulsed current source is the load. The current initially is zero, then the current is a ramp that ascends to 20mA. The current then remains constant at 20mA for a moment. Then, the current is a ramp descends to 0mA. This current pulse then repeats in a periodic manner. This plot shows that despite the varying current pulse, the output remains at 7.5V. This is due to the feedback control system controlling the duty cycle of *enable* (as explained in the section 3.1.6). The ability for a power supply to handle currents that

are not constant, but rather functions of time can be referred to the responsiveness of the power supply. Two contributing factors in the boost SPS system to the responsiveness of the circuit is the frequency of the oscillator and the off-chip capacitance. Greater oscillator frequency equates to greater responsiveness. Likewise, a greater capacitance also equates to greater responsiveness.

Regarding Simulation:

VDD = 4.5V

Temperature = 27 ºC

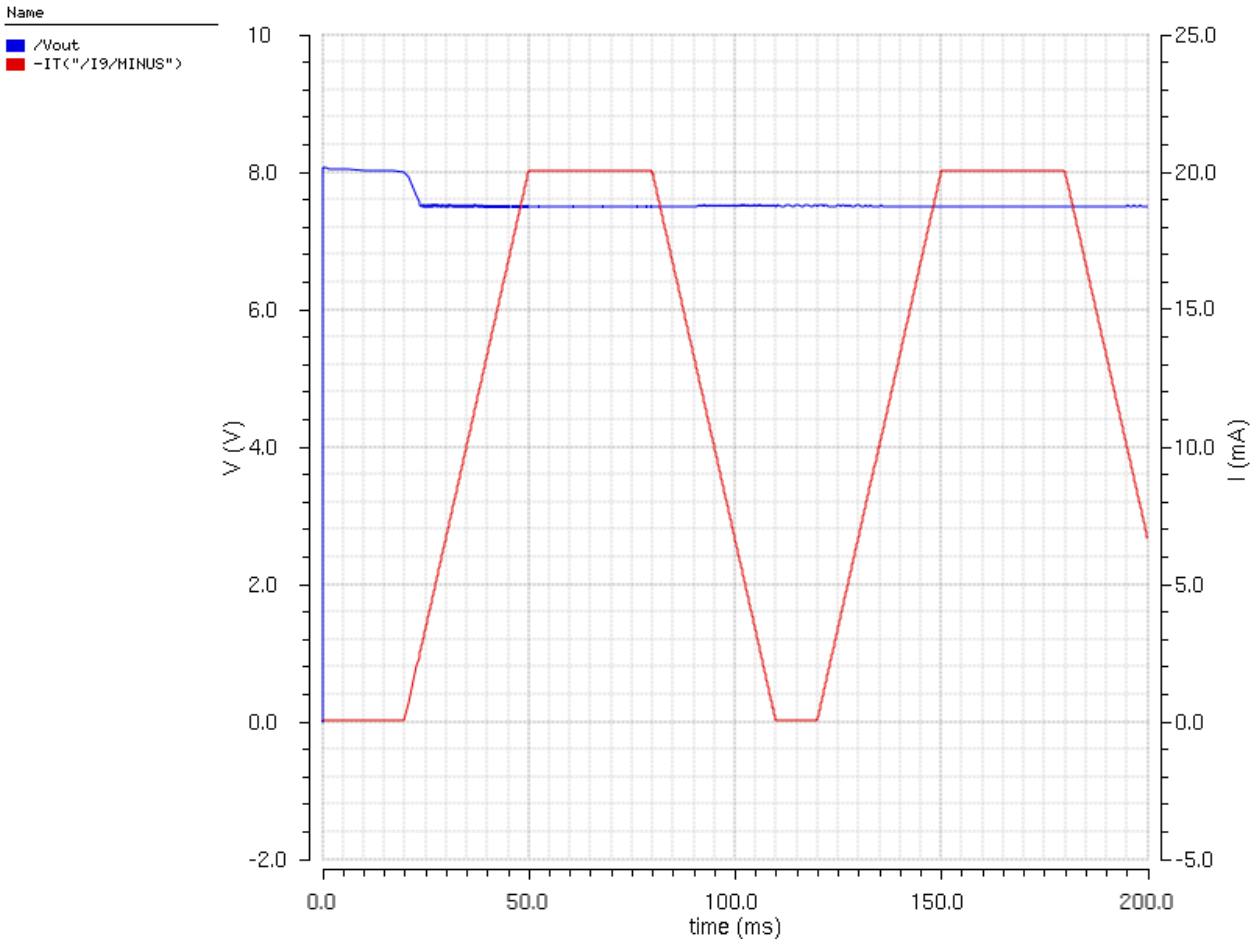

Figure 86: Current Pulse Load (3 Hour Simulation)

3. Future Work

3.1 Padframe

A padframe is the frame of pads implemented on an integrated circuit. The terminals of an integrated circuit are routed to pads. Then wires are then bonded from the chip to the package. To ensure that our designed boost SPS IC can be fabricated we must create a padframe. The following table and schematic were drafted to represent our connections from the boost SPS to the pads. Additionally, the completed padframe is included to show what our design would look like on a chip.

Table 16

Pin on Padframe	Connection
6	GND
7	VSW
8	GND
9	VFB
10	GND
13	VDD
14	VDD
15	VDD
1-5, 11-12, 16-40	No Connection

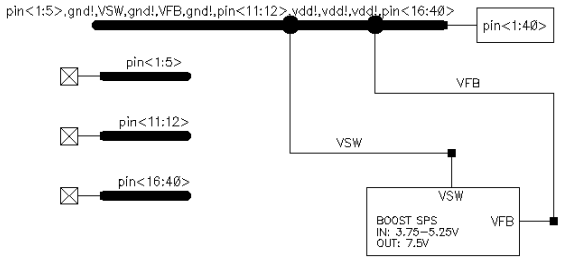

Figure 87: The Boost SPS Padframe Schematic

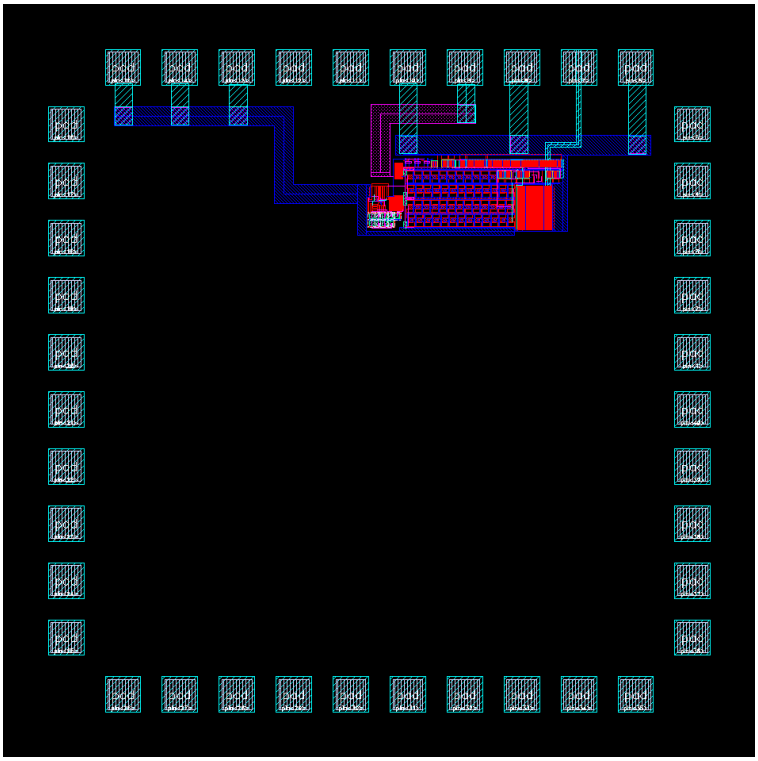

Figure 88: Padframe for the Boost SPS IC

3.2 Printed Circuit Board

After the boost SPS IC has been fabricated, the IC needs to be experimentally characterized to ensure proper operation of the boost SPS system. A printed circuit board can be designed to house the boost SPS system. The integrated circuit will need to be epoxied to a package. Then wires will bond the pins on the package to the pads on the chip (according to a bond plan). The package will then be soldered onto the PCB.

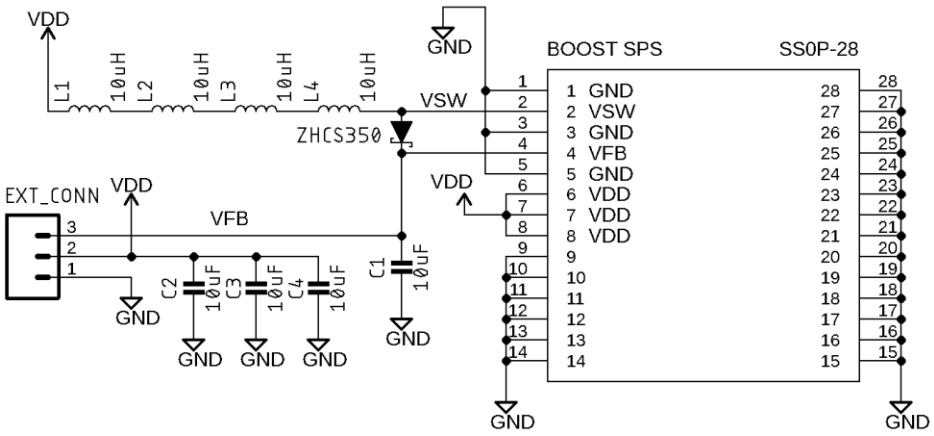

Figure 89: Boost SPS PCB Schematic

A printed circuit board has already been designed to accommodate the boost SPS system. Figure 89 depicts the schematic of the board. The selected package is the SSOP-28. As described before, four 10µH inductors are connected in series to form a 40µH inductor (see L1-L4 on the PCB). The Schottky diode and the 10µH capacitor are included on the board as well (see the ZHCS350 and C1 on the PCB). As seen in the pad frame, the chip's VDD and GND connections have three connections each. This ensures that VDD and GND are well connected. Additionally, three VDD decoupling capacitors are added (see C2-C4 on the PCB). A three-pin male header is added to the board to ensure that there is access to VDD, GND, and *Vout*. The final PCB, as developed in Eagle, can be seen in Figure 90. Board previews of the top and bottom can be seen in Figures 91 and 92. Five boards can be produced for $2 from JLCPCB.

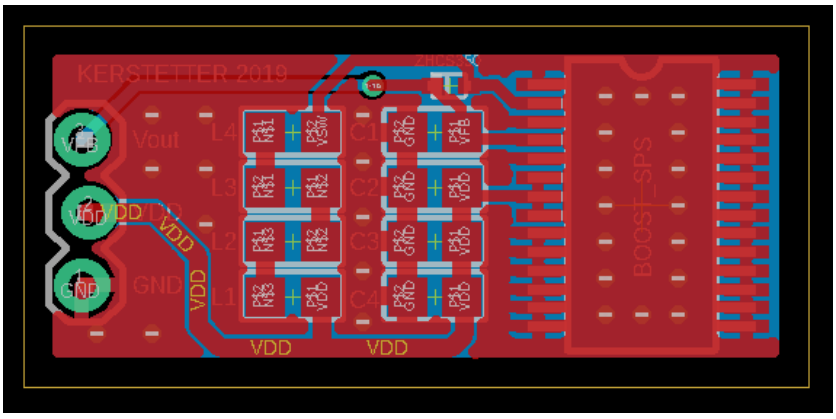

Figure 90: Laid-Out PCB as Seen in Eagle

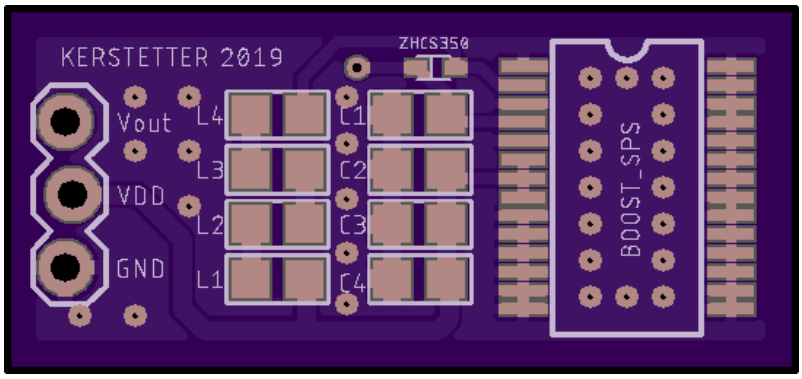

Figure 91: Top PCB Preview

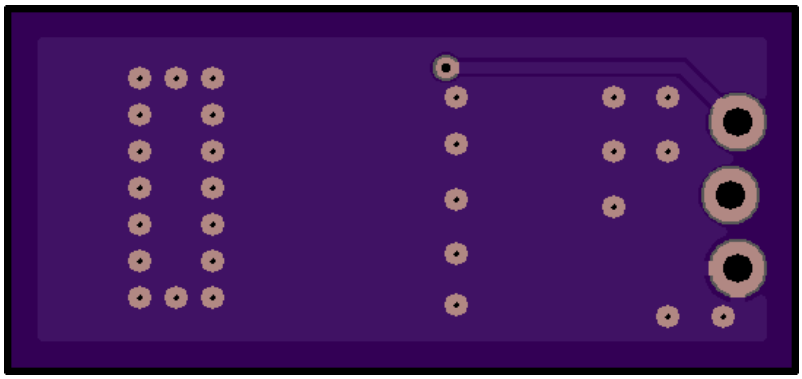

Figure 92: Bottom PCB Preview

3.3 Variable Boost SPS System

The boost SPS system scales up 3.75-5.25V to 7.5V. This is set by the voltage divider. One may adjust the output of the boost SPS system by adjusting the voltage divider. The following equation explains how the output voltage can be determined by adjusting the parameters of the voltage divider. Where *a* is the attenuation factor of the voltage divider and *Vout* is the boost SPS output voltage.

$$a = 1.25/Vout$$

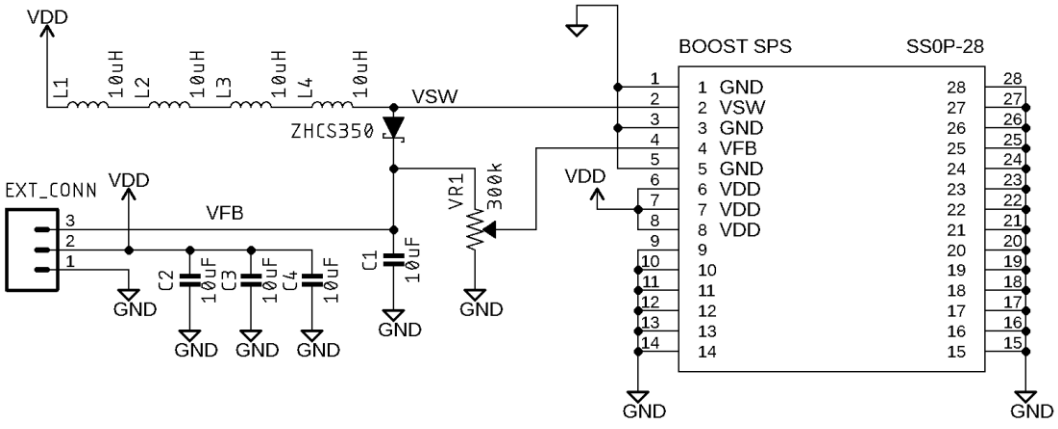

Figure 93: Variable Boost SPS System Schematic

It may be possible to implement the voltage divider off-chip. Where the voltage divider itself could be implemented with a potentiometer. This potentiometer could be added to the PCB. The result would be a variable boost SPS system. This could be achieved with little modification to the boost SPS IC design. However, the 1/6 voltage divider would have to be completely removed. Resulting in *VFB* expecting an attenuated signal. In theory, the range of *Vout* would be *VDD* to $4 \cdot VDD$ (as determined by the duty cycle of the enabled ring oscillator). The schematic of the proposed variable boost SPS system can be seen in Figure 93.

4. Conclusion

The motivation of this project was to design, simulate, and layout a CMOS Boost Switching Power Supply in On Semiconductor's C5 process. The power supply consists of an integrated circuit and an off chip inductor, Schottky diode, and capacitor. The design requirements required the supply voltage to be between 3.75-5.25V. The power supply voltage is then scaled to 7.5V. Simulations, proved that the final design was able to create a steady 7.5V and was able to drive loads that drew 0-20mA across the required supply voltage range. The design minimized ripple voltage and maximized efficiency. Further research and design efforts should be taken to further minimize the ripple voltage and further maximize efficiency, if possible. The layout of the boost SPS IC used cell frames to ensure that the layout size is minimized. However, one criticism of the layout is the size of the largest module, the enabled ring oscillator. In the future, it may be possible to reduce the size of the ring oscillator by increasing the oscillation frequency at the cost of efficiency. Additionally, the lengths of the inverters in the ring oscillator could be increased (allowing less inverters in the inverter string). This action may allow for the further reduction of the layout size. Another criticism of the layout is that there was no implementation of a standard cell decoupling capacitor. No implementation of such a decoupling capacitor may result in the slight introduction of noise. Implementing a standard cell capacitor would help minimize such noise. The padframe can be used as a template for the fabrication of a chip. If fabricated, the chip could then be implemented on the designed printed circuit board. This printed circuit board could then be featured in applications where 3.75-5.25V needs to be scaled to 7.5V. Overall, this project was a great learning experience and introduction to integrated DC-DC converters.

5. Endnotes

All layouts featured in this report pass both DRC and LVS verification while ensuring that FET parameters are checked.

This report heavily references the fourth edition of Dr. R. Jacob Baker's CMOS: Circuit Design, Layout, and Simulation.[xix]

[i] Refer to page 430 in the CMOS book
[ii] An example where longer switching speeds is needed is ring oscillators and delay elements. Delay elements can be used to create a clock multiplier. A clock multiplier designed in the laboratory associated with this class can be found at the following link: http://cmosedu.com/jbaker/courses/ee421L/f19/students/kerstett/project/project.htm
[iii] IC Resistor Geometry Calculator: http://cmosedu.com/jbaker/students/bryan/resistorCalc/resistorCalc.html
[iv] IC Resistor Geometry Calculator Information: http://cmosedu.com/jbaker/students/bryan/resistorCalc/resCalcInfo.htm
[v] Figure 23.27 in CMOS book

[vi] Equation 23.34 in CMOS book
[vii] Equation 23.35 in CMOS book
[viii] Equation 32.45 in CMOS book
[ix] Equation 11.11 in CMOS book
[x] Refer to page 362 of CMOS book
[xi] Equation 32.51 in CMOS book
[xii] MLZ2012N100LT000 Inductor Datasheet:
https://product.tdk.com/info/en/catalog/datasheets/inductor_commercial_decoupling_mlz2012_en.pdf?ref_disty=digikey
[xiii] Price according to Digi-Key Electronics as of 11/24/2019: https://www.digikey.com/product-detail/en/tdk-corporation/MLZ2012N100LT000/445-6762-1-ND/2523583
[xiv] The ZHCS350 Schottky barrier diode is manufactured by Diodes Incorporated and they provide both a datasheet and a SPICE model for their diode at the following link:
https://www.diodes.com/part/view/ZHCS350?BackID=8333#tab-details
[xv] Price according to Digi-Key Electronics as of 11/24/2019: https://www.digikey.com/product-detail/en/ZHCS350TA/ZHCS350TACTND/1137353?WT.z_cid=ref_netcomponents_dkc_buynow&utm_source=netcomponents&utm_medium=aggregator&utm_campaign=buynow

[xvi] Equation 32.53 in CMOS book
[xvii] C0603C106M8PAC7867 Capacitor Datasheet:
https://content.kemet.com/datasheets/KEM_C1006_X5R_SMD.pdf
[xviii] Price according to Digi-Key Electronics as of 11/25/2019: https://www.digikey.com/product-detail/en/kemet/C0603C106M8PAC7867/399-14945-1-ND/7382494
[xix] http://cmosedu.com/cmos1/book.htm