C5 Op-Amp Design

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I. Introduction

An op amp was designed to meet the given specifications. On Semiconductor's 500 nm process (C5) was characterized and used. Two requirements regarding power supply and load conditions are as follows:

1. Operate properly with a power supply range of 2-5V
2. Drive a 100pF (max) and a 1k (min) load

The op amp must then meet all the following requirements under all power and load conditions:

- DC open-loop gain > 66 dB
- Gain-bandwidth product > 1 MHz
- CMRR > 90 dB at 100 kHz
- PSRR > 60 dB at 1 kHz
- Slew-rate with maximum load > 1V/µs

While designing the op amp, the goal was to meet all the necessary requirements while minimizing power consumption.

I.A. C5 MOSFET Parameters

Table 1

The selected C5 MOSFET parameters to meet project specifications. Assuming VDD = 2V and a scale factor of **0.6µm** (*scale* = 0.6e-6)			
Parameter	**NMOS**	**PMOS**	**Comments**
Bias Current, I_D	5µA	5µA	Approximate
W/L	45/1 (27µm/0.6µm)	45/1 (54µm/0.6µm)	Selected based upon I_D and $V_{DS,\,sat}$
$V_{DS,\,sat}$ and $V_{SD,\,sat}$	0.100 V	0.100 V	For sizes listed
V_{GS} and V_{SG}	0.663 V	0.912 V	No body effect
V_{THN} and V_{THP}	0.670 V	0.920 V	Typical
KP_n and KP_p			t_{ox}=1.39E-8m
t_{ox}	1.39E-8m	1.39E-8m	
$C_{ox}^1 = \varepsilon_{ox}/t_{ox}$	2.53 fF/µm^2	2.53 fF/µm^2	$C_{ox} = C_{ox}^1 WL \cdot (scale)^2$
C_{oxn} and C_{oxp}	40.99 fF	81.97 fF	PMOS is two times wider
C_{gsn} and C_{sgp}	5.30 fF	15.5 fF	
C_{gdn} and C_{dgp}	5.30 fF	15.5 fF	
g_{mn} and g_{mp}	106 µA/V	121 µA/V	AT I_D =10 µA
r_{on} and r_{op}	11 MΩ	12.5 MΩ	
$g_{mn}r_{on}$ and $g_{mp}r_{op}$	1177 V/V	1513 V/V	!! Open Circuit Gain !!
λ_n and λ_p	0.018 V^{-1}	0.016 V^{-1}	$\lambda = slope/I_{D,sat}$

I.B. Summary of Op-Amp Performance

Table 2

Parameter	VDD=2V	VDD=5V
DC Open Loop Gain ***No Load***	89.27 dB	82.36 dB
Unit Gain Frequency ***No Load***	3.98 MHz	4.49 MHz
Phase Margin ***No Load***	95°	89.24°
DC Open Loop Gain ***Load: 1kΩ ‖ 100pF***	83.20 dB	78.3 dB
Unit Gain Frequency ***Load: 1kΩ ‖ 100pF***	3.43 MHz	3.86 MHz
Phase Margin ***Load: 1kΩ ‖ 100pF***	107.48°	98.33°
CMRR (at 100kHz) ***No Load***	96.77 dB	118.95 dB
CMRR (at 100kHz) ***Load: 1kΩ ‖ 100pF***	102.54 dB	118.59 dB
PSRR+ (at 1kHz)	72.40 dB	73.80 dB
PSRR- (at 1kHz)	170.24 dB	156.84 dB
Max Slew Rate ***Load: 1kΩ ‖ 100pF***	1.02 V/µs	1.75 V/µs
Current Draw ***Under Quiescent Conditions***	65.50 µA	81.54 µA
Power Consumption ***Under Quiescent Conditions***	131.02 µW	407.72 µW

Table 2 summarizes the performance of the designed op-amp. The designed op-amp meets or exceeds all the designed requirements.

The following LTspice models were the models used to design and simulate the op-amp.

I.C. C5 LTspice Model

```
* BSIM3 models for AMI Semiconductor's C5 process
*
* Don't forget the .options scale=300nm if using drawn lengths
* and the MOSIS SUBM design rules
*
* 2<Ldrawn<500   10<Wdrawn<10000 Vdd=5V
* Note minimum L is 0.6 um while minimum W is 3 um
* Change to level=49 when using HSPICE or SmartSpice

.MODEL NMOS NMOS (                                LEVEL   = 8
```

```
+VERSION = 3.1            TNOM    = 27             TOX     = 1.39E-8
+XJ      = 1.5E-7         NCH     = 1.7E17         VTH0    = 0.6696061
+K1      = 0.8351612      K2      = -0.0839158     K3      = 23.1023856
+K3B     = -7.6841108     W0      = 1E-8           NLX     = 1E-9
+DVT0W   = 0              DVT1W   = 0              DVT2W   = 0
+DVT0    = 2.9047241      DVT1    = 0.4302695      DVT2    = -0.134857
+U0      = 458.439679     UA      = 1E-13          UB      = 1.485499E-18
+UC      = 1.629939E-11   VSAT    = 1.643993E5     A0      = 0.6103537
+AGS     = 0.1194608      B0      = 2.674756E-6    B1      = 5E-6
+KETA    = -2.640681E-3   A1      = 8.219585E-5    A2      = 0.3564792
+RDSW    = 1.387108E3     PRWG    = 0.0299916      PRWB    = 0.0363981
+WR      = 1              WINT    = 2.472348E-7    LINT    = 3.597605E-8
+XL      = 0              XW      = 0              DWG     = -1.287163E-8
+DWB     = 5.306586E-8    VOFF    = 0              NFACTOR = 0.8365585
+CIT     = 0              CDSC    = 2.4E-4         CDSCD   = 0
+CDSCB   = 0              ETA0    = 0.0246738      ETAB    = -1.406123E-3
+DSUB    = 0.2543458      PCLM    = 2.5945188      PDIBLC1 = -0.4282336
+PDIBLC2 = 2.311743E-3    PDIBLCB = -0.0272914     DROUT   = 0.7283566
+PSCBE1  = 5.598623E8     PSCBE2  = 5.461645E-5    PVAG    = 0
+DELTA   = 0.01           RSH     = 81.8           MOBMOD  = 1
+PRT     = 8.621          UTE     = -1             KT1     = -0.2501
+KT1L    = -2.58E-9       KT2     = 0              UA1     = 5.4E-10
+UB1     = -4.8E-19       UC1     = -7.5E-11       AT      = 1E5
+WL      = 0              WLN     = 1              WW      = 0
+WWN     = 1              WWL     = 0              LL      = 0
+LLN     = 1              LW      = 0              LWN     = 1
+LWL     = 0              CAPMOD  = 2              XPART   = 0.5
+CGDO    = 2E-10          CGSO    = 2E-10          CGBO    = 1E-9
+CJ      = 4.197772E-4    PB      = 0.99           MJ      = 0.4515044
+CJSW    = 3.242724E-10   PBSW    = 0.1            MJSW    = 0.1153991
+CJSWG   = 1.64E-10       PBSWG   = 0.1            MJSWG   = 0.1153991
+CF      = 0              PVTH0   = 0.0585501      PRDSW   = 133.285505
+PK2     = -0.0299638     WKETA   = -0.0248758     LKETA   = 1.173187E-3
+AF      = 1              KF      = 0)
*
.MODEL PMOS PMOS (                                LEVEL   = 8
+VERSION = 3.1            TNOM    = 27             TOX     = 1.39E-8
+XJ      = 1.5E-7         NCH     = 1.7E17         VTH0    = -0.9214347
+K1      = 0.5553722      K2      = 8.763328E-3    K3      = 6.3063558
+K3B     = -0.6487362     W0      = 1.280703E-8    NLX     = 2.593997E-8
+DVT0W   = 0              DVT1W   = 0              DVT2W   = 0
+DVT0    = 2.5131165      DVT1    = 0.5480536      DVT2    = -0.1186489
+U0      = 212.0166131    UA      = 2.807115E-9    UB      = 1E-21
+UC      = -5.82128E-11   VSAT    = 1.713601E5     A0      = 0.8430019
+AGS     = 0.1328608      B0      = 7.117912E-7    B1      = 5E-6
+KETA    = -3.674859E-3   A1      = 4.77502E-5     A2      = 0.3
+RDSW    = 2.837206E3     PRWG    = -0.0363908     PRWB    = -1.016722E-5
+WR      = 1              WINT    = 2.838038E-7    LINT    = 5.528807E-8
+XL      = 0              XW      = 0              DWG     = -1.606385E-8
+DWB     = 2.266386E-8    VOFF    = -0.0558512     NFACTOR = 0.9342488
+CIT     = 0              CDSC    = 2.4E-4         CDSCD   = 0
+CDSCB   = 0              ETA0    = 0.3251882      ETAB    = -0.0580325
+DSUB    = 1              PCLM    = 2.2409567      PDIBLC1 = 0.0411445
+PDIBLC2 = 3.355575E-3    PDIBLCB = -0.0551797     DROUT   = 0.2036901
+PSCBE1  = 6.44809E9      PSCBE2  = 6.300848E-10   PVAG    = 0
+DELTA   = 0.01           RSH     = 101.6          MOBMOD  = 1
+PRT     = 59.494         UTE     = -1             KT1     = -0.2942
```

```
+KT1L     = 1.68E-9          KT2      = 0               UA1      = 4.5E-9
+UB1      = -6.3E-18         UC1      = -1E-10          AT       = 1E3
+WL       = 0                WLN      = 1               WW       = 0
+WWN      = 1                WWL      = 0               LL       = 0
+LLN      = 1                LW       = 0               LWN      = 1
+LWL      = 0                CAPMOD   = 2               XPART    = 0.5
+CGDO     = 2.9E-10          CGSO     = 2.9E-10         CGBO     = 1E-9
+CJ       = 7.235528E-4      PB       = 0.9527355       MJ       = 0.4955293
+CJSW     = 2.692786E-10     PBSW     = 0.99            MJSW     = 0.2958392
+CJSWG    = 6.4E-11          PBSWG    = 0.99            MJSWG    = 0.2958392
+CF       = 0                PVTH0    = 5.98016E-3      PRDSW    = 14.8598424
+PK2      = 3.73981E-3       WKETA    = 5.292165E-3     LKETA    = -4.205905E-3
+AF       = 1                KF       = 0)
```

II. MOSFET Geometries

Looking at the LTspice model one can determine that the threshold voltage of the MOSFETs to be: $V_{THN} = 0.67\,V$ and $V_{THP} = 0.92\,V$. Alternatively, these values could have been found by running simulations of the MOSFETs to determine the threshold voltages. The minimum length for the c6 process is 0.6 µm. The minimum length is chosen for the length of both the NMOS and PMOS so that the open loop gain is maximized. We can assert the following notion (see CMOS Book; pg. 301):

$$I_D \propto V_{GS} \propto w \propto speed \propto \frac{1}{gain} \propto \frac{1}{L} \qquad [1]$$

This notion described in Equation 1 was used to select the device sizes. Additionally, we know that the device geometry must accommodate a selected drain current of 5µA and a $V_{DS,sat}$ and $V_{SD,sat}$ of 100mV. The following set of equations show that MOSFET geometry effect both the drain current and the saturation drain to source voltage.

$$I_D \propto \frac{W}{L} \qquad [2]$$

$$V_{DS,sat} = V_{SD,sat} \propto \frac{L}{W} \qquad [3]$$

The following geometries were chosen:

$$NMOS\ Geometry = \frac{27u}{0.6u}$$

$$PMOS\ Geometry = \frac{54u}{0.6u}$$

The follow LTspice parameter statements are made to define the geometry of the MOSFETs:

```
.param NL = 0.6u NW = 27u
.param PL = 0.6u PW = 54u
```

All incidences of *NL*, *PL*, *NW*, and *PW* will represent the values defined above. A small reference current and smaller widths were selected so that the power consumption of the op-amp would be minimized.

III. Beta-Multiplier Reference Design

To design an op-amp that functions properly on a power supply voltage range of 2-5V a supply independent biasing. A Beta-Multiplier Reference (BMR) will be used to create supply independent reference voltages.

One may use the square-law equations to illustrate the fact that the reference current through the BMR is virtually independent from the power supply (*Please note: The C5 models do not exactly adhere to the square-law equations)*. If the reference current of the BMR are supply independent, then the reference voltages *Vbiasp* and *Vbiasn* are supply independent. The reference current of a BMR can be defined by,

$$I_{REF} = \frac{V_{GS1} - V_{GS2}}{R} \quad [4]$$

Where V_{GS1} and V_{GS2} can be developed from the square law equations such that

$$V_{GS1} = V_{THN} + \sqrt{\frac{2 \cdot I_{REF}}{KP_n \cdot \frac{W}{L}}} \quad [5]$$

$$V_{GS2} = V_{THN} + \sqrt{\frac{2 \cdot I_{REF}}{KP_n \cdot \frac{W}{L} \cdot k}} \quad [6]$$

$$I_{REF} = \frac{\sqrt{\frac{2 \cdot I_{REF}}{KP_n \cdot \frac{W}{L}}} - \sqrt{\frac{2 \cdot I_{REF}}{KP_n \frac{W}{L} \cdot k}}}{R} \quad [7]$$

$$I_{REF} = \frac{1}{R}\sqrt{\frac{2 \cdot I_{REF}}{KP_n \cdot \frac{W}{L}}}\left(1 - \frac{1}{\sqrt{k}}\right) \quad [8]$$

$$\therefore I_{REF} = \frac{2}{R^2 \cdot KP_n \cdot \frac{W}{L}}\left(1 - \frac{1}{\sqrt{k}}\right)^2 \quad [9]$$

In Equation 6 the reference current is not dependent upon the supply voltage.

A self-biased circuit has two possible operating points. There preferred biasing point is where the correct currents are flowing in the circuit. However, there is also an unwanted operating point. This unwanted operating point is where zero current flows in the circuit. The unwanted operating point occurs when M2/M4 are grounded while the gates of M1/M3 are tied high (see CMOS Book; pg. 625). A startup circuit can be created to eliminate the unwanted operating point quicker. The start-up circuit causes the beta-multiplier to *quickly snap* to the desired operating point and MSU3 to turn off. Once the system *snaps* into a steady-state, the preferred operating point is achieved, and the unwanted operating point is effectively eliminated. It is possible for the reference current of the BMR to still vary with changes in VDD. This variance of the reference current with respect to VDD can be minimized by adding a differential amplifier to the beta-multiplier and start-up circuit. This differential amplifier forces the drains of the MOSFETs to the same voltage levels. The greater the gain of the differential amplifier, the further independent the reference current and voltages from the power supply. To ensure that the

reference voltages are stable, we may add a decoupling capacitor from the reference voltage to ground.

The intention of the start-up circuit is to *snap* the system out of the unwanted operating point and then shut off. The start-up circuit fails if *MSU3* turns on after the initial startup. If *MSU3* turns on, the NMOS injects current at a rate such that the reference currents through the beta-multiplier is proportional to VDD. The start-up circuit operates as intended, for greater VDD ranges, if *MSU1's* geometry is such that its $l >> w$. By making the *MSU1 w/l* ratio smaller, it extends the point at which the start-up circuit fails. Additionally, the geometry of *MSU2* should be such that $w>>l$. Figure 1 depicts the BMR design that was implemented in this project.

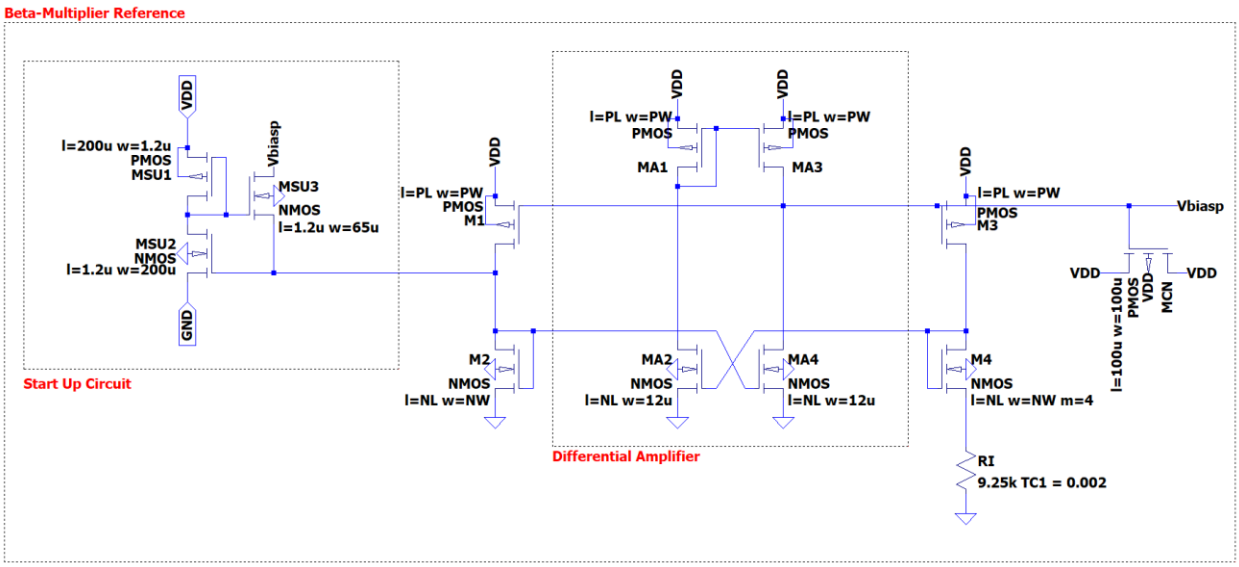

Figure 1

In Figure 2 a minuscule amount of current is being injected into the BMR from the start-up circuit. Figure 3 depicts shows how the reference current of the BMR varies with temperature and supply voltage.

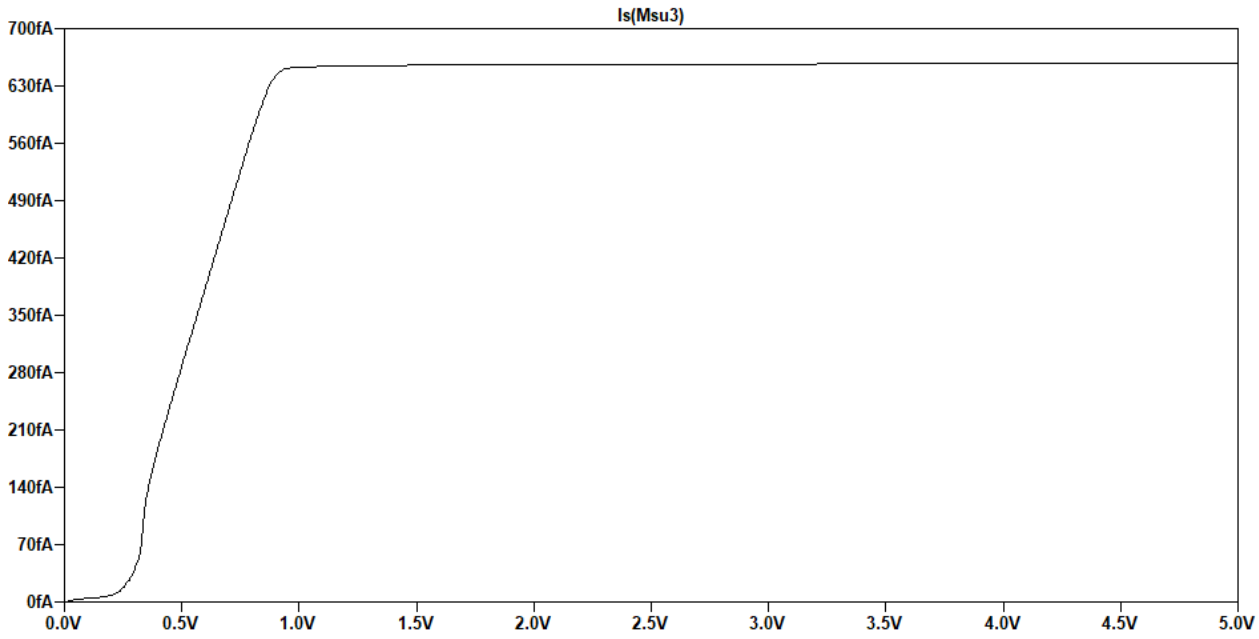

Figure 2

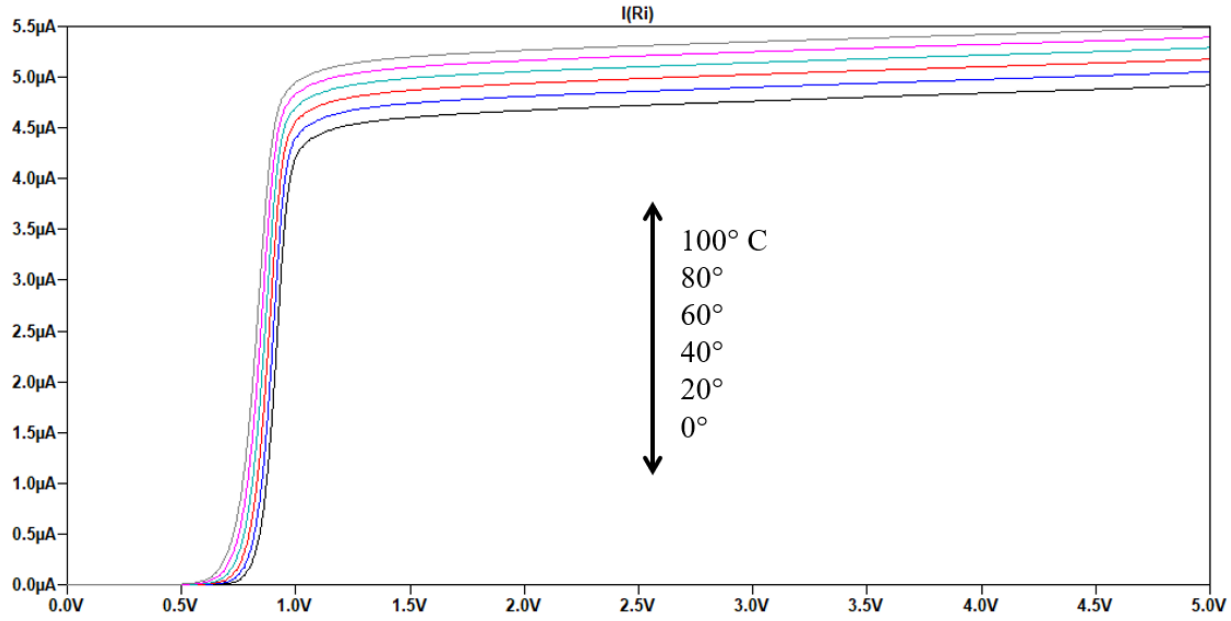

Figure 3

IV. Bias Circuit Design

The bias circuit takes *Vbiasp* from the BMR and creates additional reference voltages that will then be used to bias MOSFETs in the op-amp circuit. The biasing circuit (see Figure 4) used in this project is based upon Figure 20.47 of Dr. Baker's CMOS book.

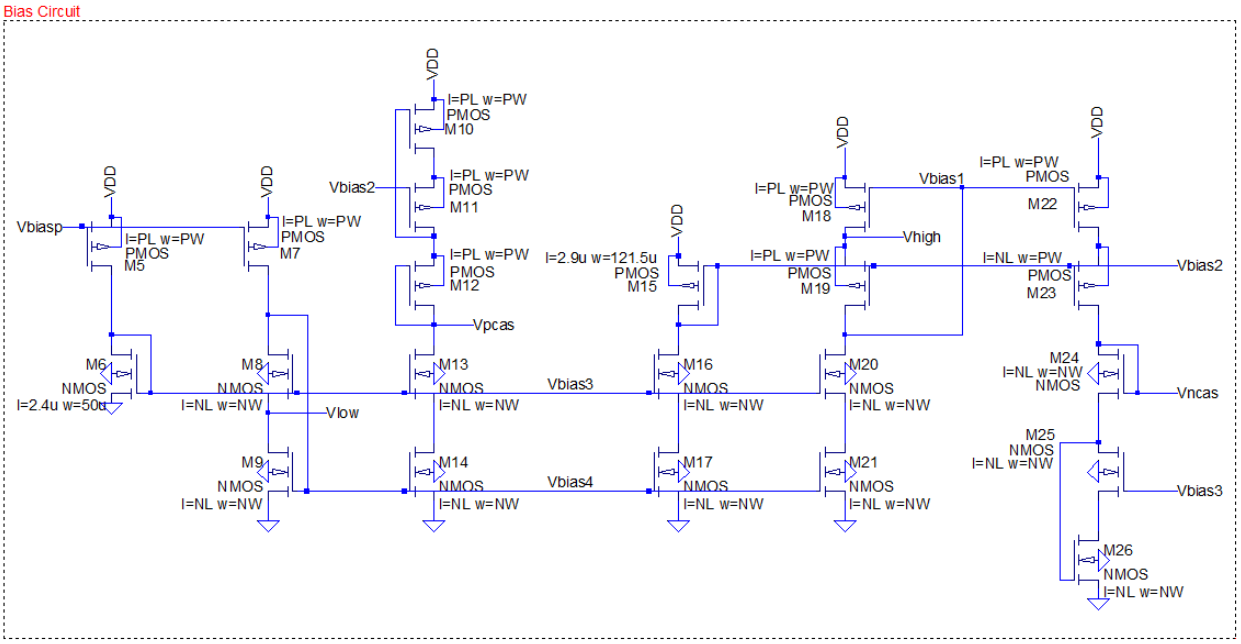

Figure 4

When designing the biasing circuit, it is good to have a ballpark range of the bias voltages that you are aiming for in your design. This ballpark range can be achieved by *labeling the voltages* in the following manner:

$$V_{bias1} = VDD - V_{SD,sat} - V_{THP} \quad [10]$$

$$V_{bias2} = VDD - 2V_{SD,sat} - V_{THP} \quad [11]$$

$$V_{bias3} = 2V_{DS,sat} + V_{THN} \quad [12]$$

$$V_{bias4} = V_{DS,sat} + V_{THN} \quad [13]$$

$$V_{pcas} = VDD - 2\left(V_{SD,sat} + V_{THP}\right) \quad [14]$$

$$V_{ncas} = 2\left(V_{DS,sat} + V_{THN}\right) \quad [15]$$

$$V_{low} = V_{DS,sat} \quad [16]$$

$$V_{high} = VDD - V_{SD,sat} \quad [17]$$

So that we can directly compare the NMOS and PMOS bias voltages in LTspice, we may now remove the effect of VDD in the labeled voltages:

$$V_{bias1} = V_{SD,sat} + V_{THP} \quad [18]$$

$$V_{bias2} = 2V_{SD,sat} + V_{THP} \quad [19]$$

$$V_{bias3} = 2V_{DS,sat} + V_{THN} \quad [20]$$

$$V_{bias4} = V_{DS,sat} + V_{THN} \quad [21]$$

$$V_{pcas} = 2\left(V_{SD,sat} + V_{THP}\right) \quad [22]$$

$$V_{ncas} = 2\left(V_{DS,sat} + V_{THN}\right) \quad [23]$$

$$V_{low} = V_{DS,sat} \quad [24]$$

$$V_{high} = V_{SD,sat} \quad [25]$$

Our biasing circuit must properly function at a power supply range of 2-5V. For general analog design, $V_{DS,sat}$ and $V_{SD,sat}$ should be around 5% of VDD (see CMOS Book; pg. 291). Our minimum VDD is 2V, therefore:

$$V_{DS,sat} = V_{SD,sat} = VDD \cdot 0.05 = 100mV \quad [26]$$

The approximate threshold voltages can be found by testing the C5 MOSFETs in LTspice or by looking the LTspice model parameters.

$$V_{THN} = 0.67\ V \quad [27]$$

$$V_{THP} = 0.92\ V \quad [28]$$

Substituting Equations 15-17 into Equations 7-14, give us the following approximate values:

$$V_{bias1} \approx 1.02\ V \quad [29]$$

$$V_{bias2} \approx 1.12\ V \quad [30]$$

$$V_{bias3} \approx 0.87\ V \quad [31]$$

$$V_{bias4} \approx 0.77\ V \quad [32]$$

$$V_{pcas} \approx 2.04\ V \quad [33]$$

$$V_{ncas} \approx 1.54\ V \quad [34]$$

$$V_{low} \approx 0.1\ V \quad [35]$$

$$V_{high} \approx 0.1\ V \quad [36]$$

V_{low} and V_{high} can be adjusting the geometries of *M6* and *M15* of the bias circuit (while adhering to the proportionality observed in Equation 3). Once $V_{low} = V_{high} \approx 0.1\ V$, if your selected device sizes are correct, all bias voltages will come close to the hand calculated voltage values as seen in Table 3. Additionally, Table 3 testifies to the fact that the bias voltages are virtually independent from the supply voltage.

Table 3: Information taken from Figure 6

Bias Voltages: Comparing Hand Calculations and LTspice Simulation Results			
Bias Voltage	**Hand Calculation**	**Simulation (at 25° C)**	
		VDD = 2V	**VDD = 5V**
Vbias1	1.020	0.912	0.917
Vbias2	1.120	0.994	1.000
Vbias3	0.870	0.775	0.778
Vbias4	0.770	0.663	0.666
Vpcas	2.040	1.801	1.812
Vncas	1.540	1.449	1.464
Vlow	0.100	0.100	0.101
Vhigh	0.100	0.100	0.101

A good op-amp design should be able to function properly from 0-100°C. Figure 7 show the bias voltages as supply voltages and temperature varies. Temperature simulations are assuming the following regarding the temperature coefficient of the resistors (see CMOS Book; pg. 634):

$$TCR = \frac{1}{R}\frac{\partial R}{\partial T} = 2000\,\frac{ppm}{C^{\circ}} (= 0.002) \qquad [37]$$

Figure 7 demonstrates the change in bias voltages as temperature increases. In section *VI* the effect of temperature on our op-amp will be explored.

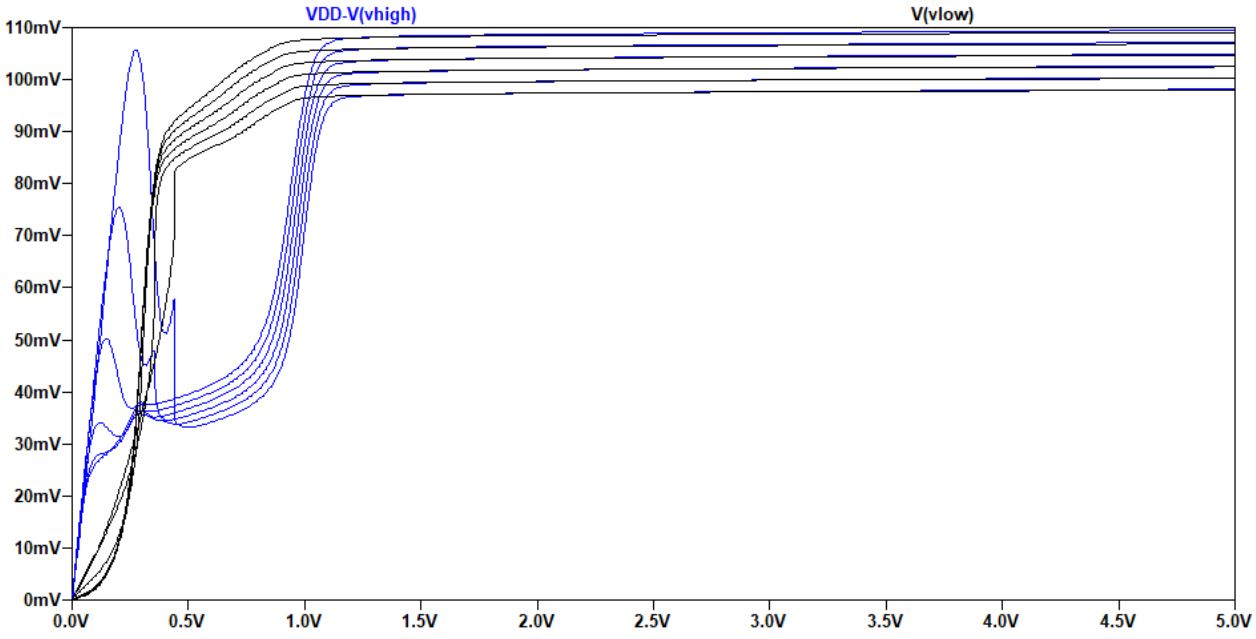

Figure 5: Vlow and Vhigh v. Supply Voltage; Temperature = 0-100°C

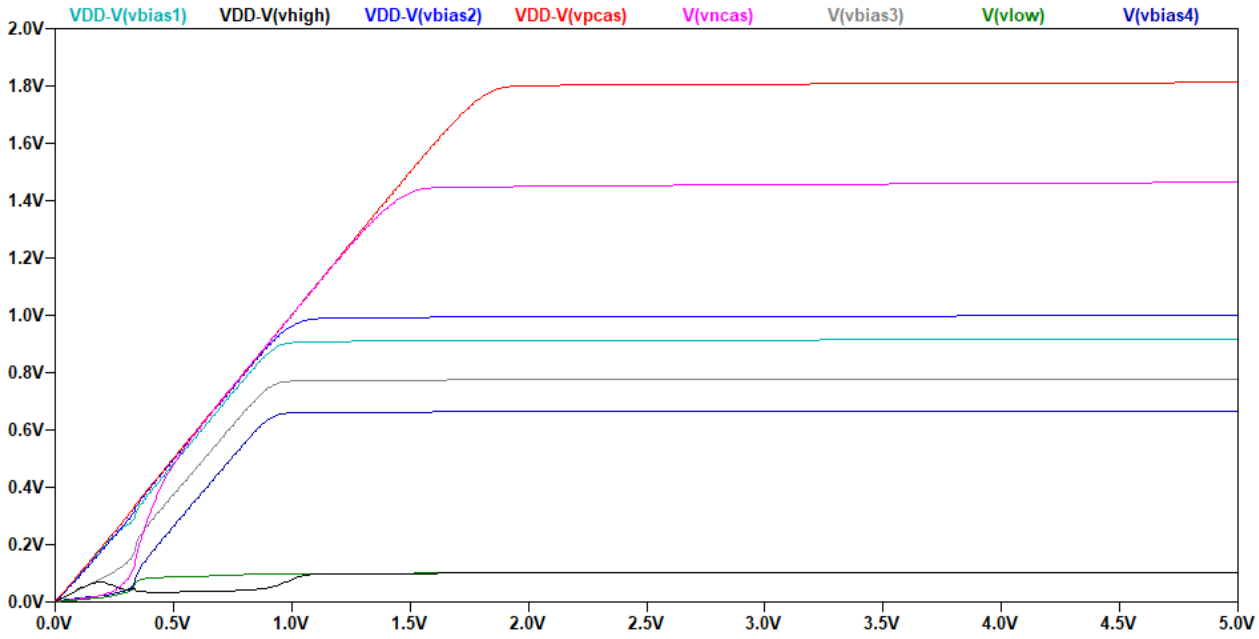

Figure 6: Bias Voltages v. Supply Voltage; Temperature = 25°C

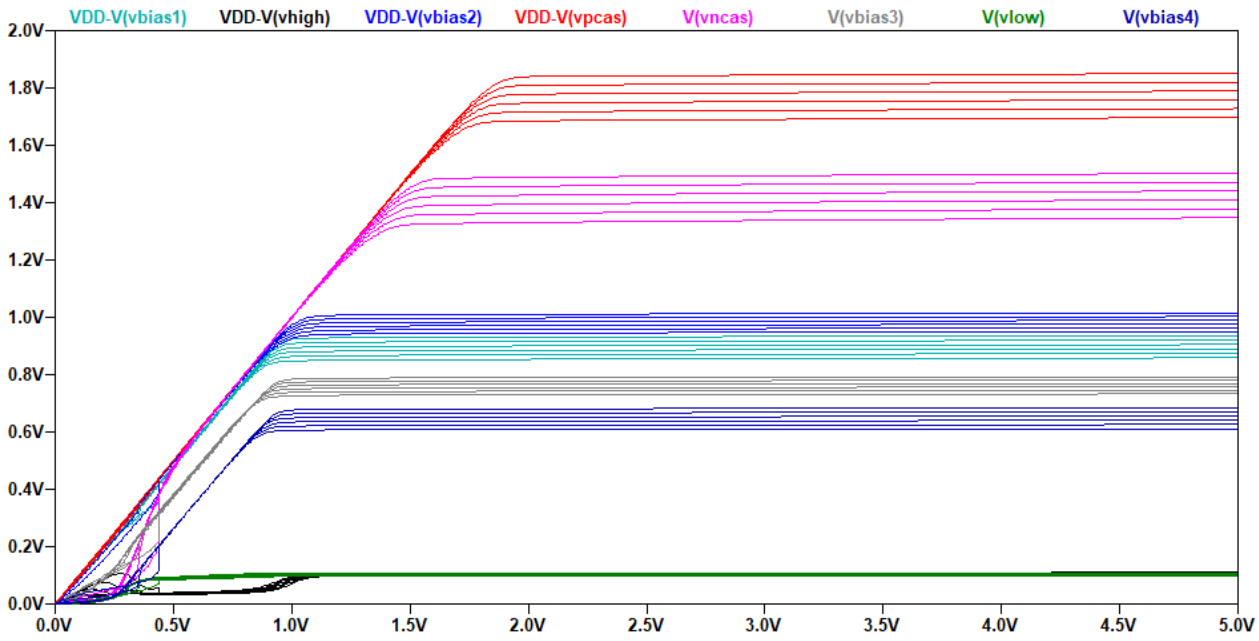

Figure 7: Bias Voltages v. Supply Voltage; Temperature = 0-100°C

V. Op-Amp Design

The op-Amp design is based upon a folded-cascode op-amp topology as seen in Figure 24.48 in Dr. Baker's CMOS book (see CMOS Book; pg. 807). The design has both a NMOS and PMOS differential amplifier stage. Having both a NMOS and a PMOS differential amplifier stage, allows the design to be considered as a wide-swing op-amp. When the common mode voltage approaches VDD, the PMOS differential amplifier stage will turn off. Likewise, when the common mode voltage approaches ground, the NMOS differential amplifier stage will turn off.

Table 4

Common Mode Voltage near…	Condition		Unity Gain Frequency (f_{un})
	NMOS Diff. Amp.	PMOS Diff. Amp.	
VDD	ON	OFF	$\frac{g_{mn}}{2\pi C_c}$
↕	ON	ON	$\frac{g_{mn}+g_{mp}}{2\pi C_c}$
Ground	OFF	ON	$\frac{g_{mp}}{2\pi C_c}$

Based upon Table 4, this specific op-amp topology can increase the unity-gain frequency and thereby, increasing the bandwidth. One issue presents itself regarding the gain-bandwidth product. Both the gain and the bandwidth are dependent upon the common mode voltage. If varying gain is an issue, the non-inverting op-amp topology can be used to ensure that the common-mode voltage is held at a constant. Floating current sources are added to stabilize and equalized the voltages across *M10* and *M8*. The widths of *MOP1* and *MON1* are increased to supply significant amounts of current to the load. Additionally, the widths of M2, *M21*, *M22* and *M3* are modestly increased to minimize the widths required at M10 and M8. There are 4 PMOSs (M13, M14, M12, & M1), that source current to the various components of the op-amp. Likewise, there are 4 NMOSs (M23, M11, M9, & M24) to sink the same magnitude of current sourced by the 4 PMOSs.

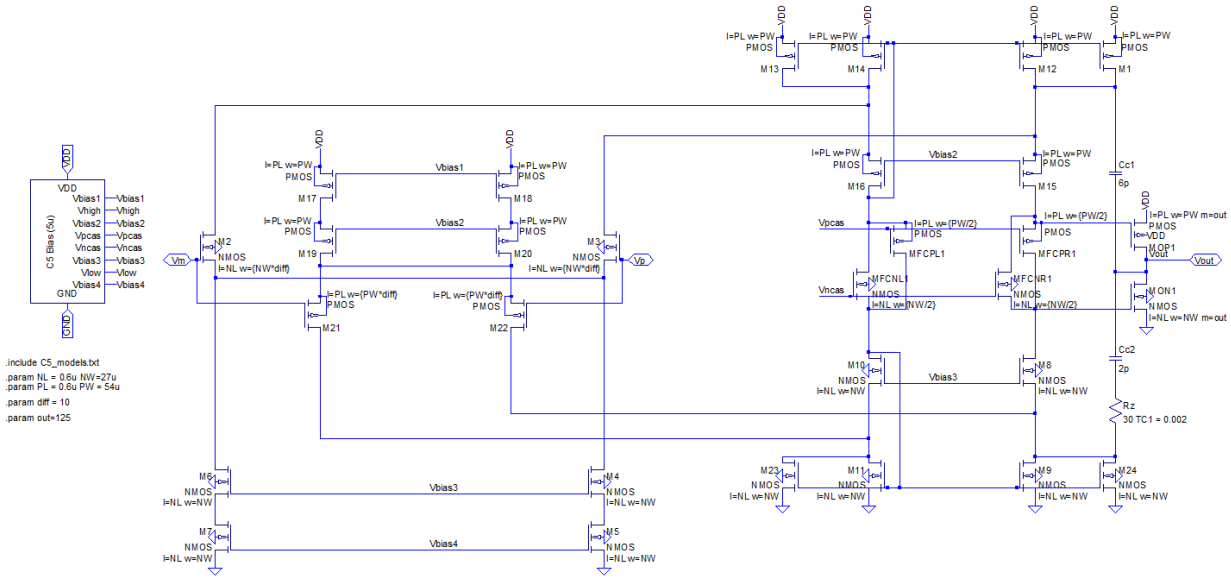

Figure 8

VI. Op-Amp Simulation

Simulations that state that the load conditions are implemented assume the load is a 100pF capacitor in parallel with a 1kΩ resistor. Additionally, in all simulations where the temperature is varied (stepped) the following statement is used – .step temp 0 100 20. All other simulations, 25°C is assumed.

VI.A. DC Open-Loop Gain and the Gain-Bandwidth Product

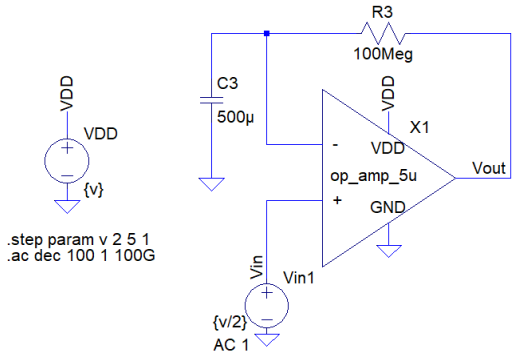

Figure 9

A circuit as seen in Figure 9 allows one to test the open loop gain. The resistor and the capacitor create a RC time constant so large that no AC output voltage is feed back into the non-inverting input of the op-amp. The capacitors, purpose is to ensure that the DC output at the output is fed back into the non-inverting input (ensuring all MOSFETs are operating in the saturation region). A LTspice simulation is created to observe the open-loop gain at all necessary supply voltage values.

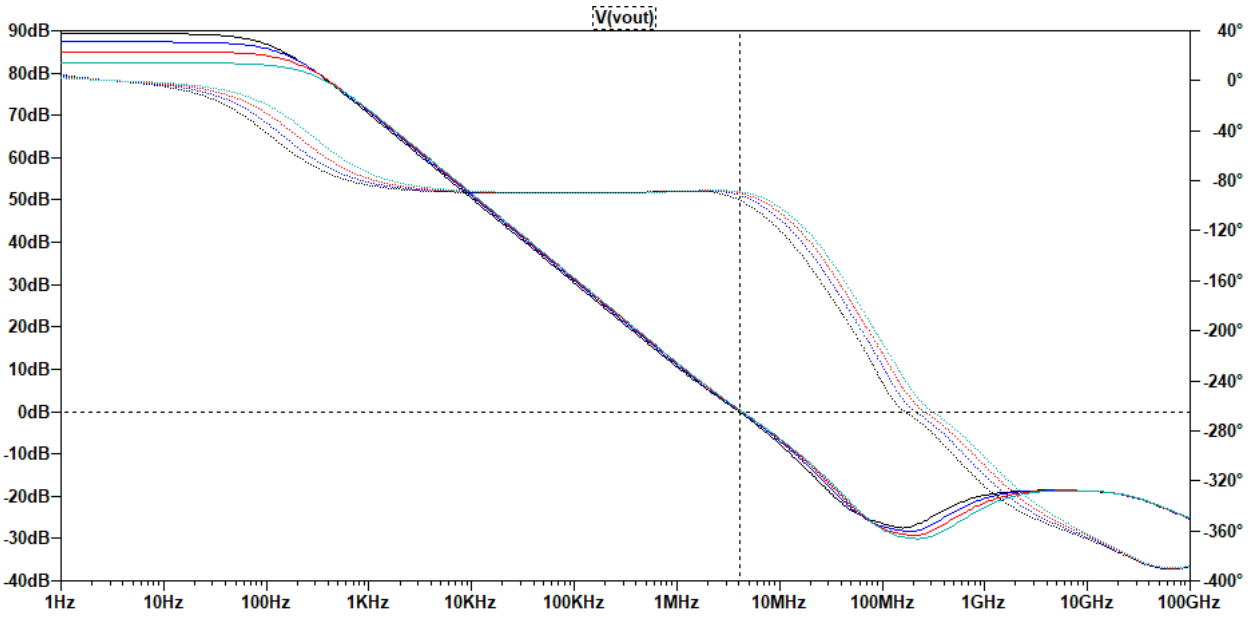

Figure 10: Open-loop gain with no load while stepping supply voltage

Table 5

Open-Loop Gain with no Load		
Parameter	**Value**	
	VDD = 2V	**VDD = 5V**
Open Loop Gain	89.27 dB	82.36 dB
Unity Gain Frequency	3.98 MHz	4.49 MHz
Phase Margin	95°	89.24°

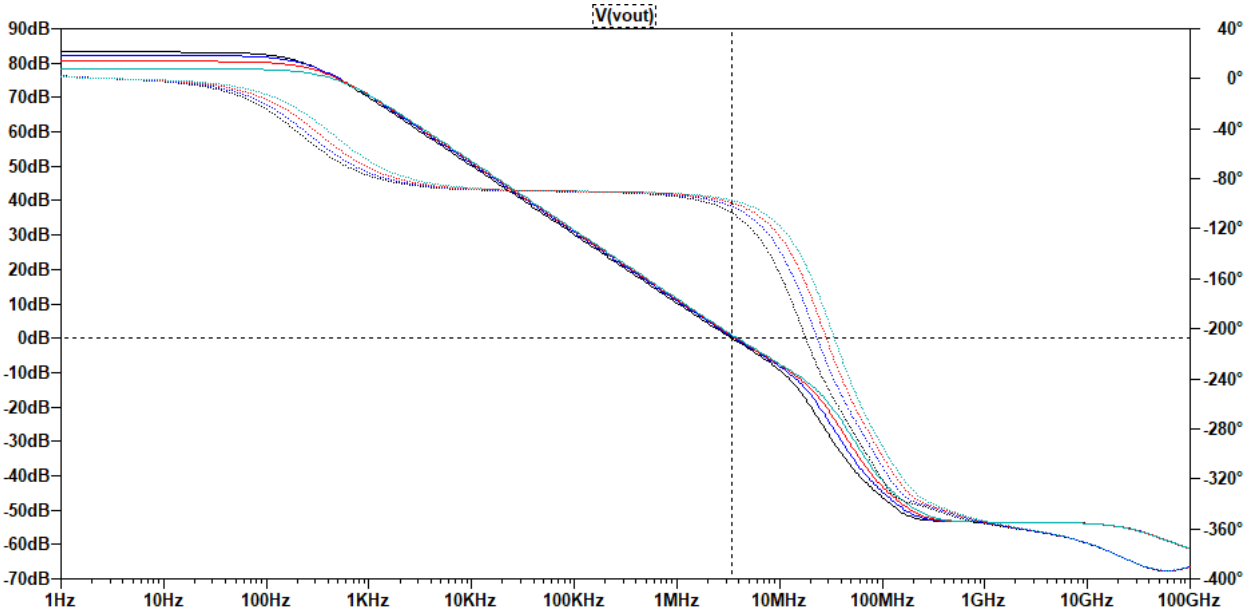

Figure 11: Open-loop gain with load while stepping supply voltage

Table 6

Open-Loop Gain with Load		
Parameter	**Value**	
	VDD = 2V	**VDD = 5V**
Open Loop Gain	83.20 dB	78.3 dB
Unity Gain Frequency	3.43 MHz	3.86 MHz
Phase Margin	107.48°	98.33°

The requirement regarding the DC open-loop gain is that the gain should be over 66 dB under all load and VDD conditions. The data seen in Table 6 indicate that the op-amp meets the requirements for the DC-open loop gain. Additionally, it seen that the unity gain frequency or the gain-bandwidth product is meet the requirement of being greater than 1 MHz. Additionally, it should be noted that the phase margin is near 90° (this will prove to be nice when it comes to the stability of the step-response). Additionally, we may see how the open loop gain varies with temperature (Figure 12). We can see that the op-amp remains relatively unaffected by temperature differences from 0-100°C.

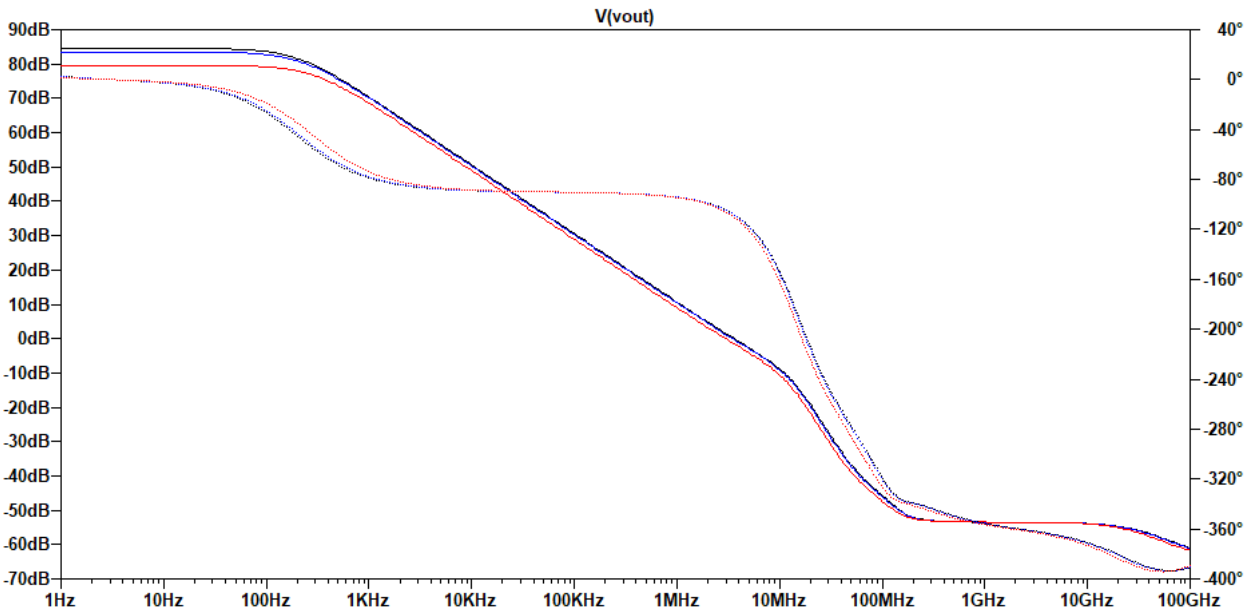

Figure 12

VI.B. Common-Mode Rejection Ratio (CMRR)

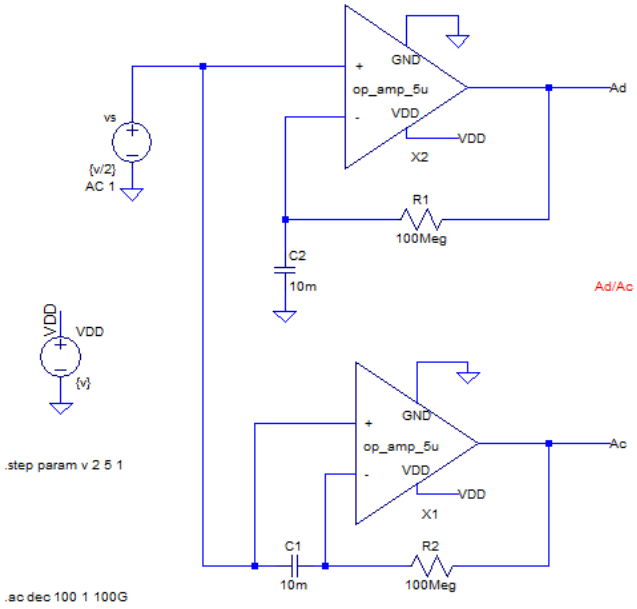

Figure 13

The circuit as seen in Figure 13 can be used to test the CMRR.

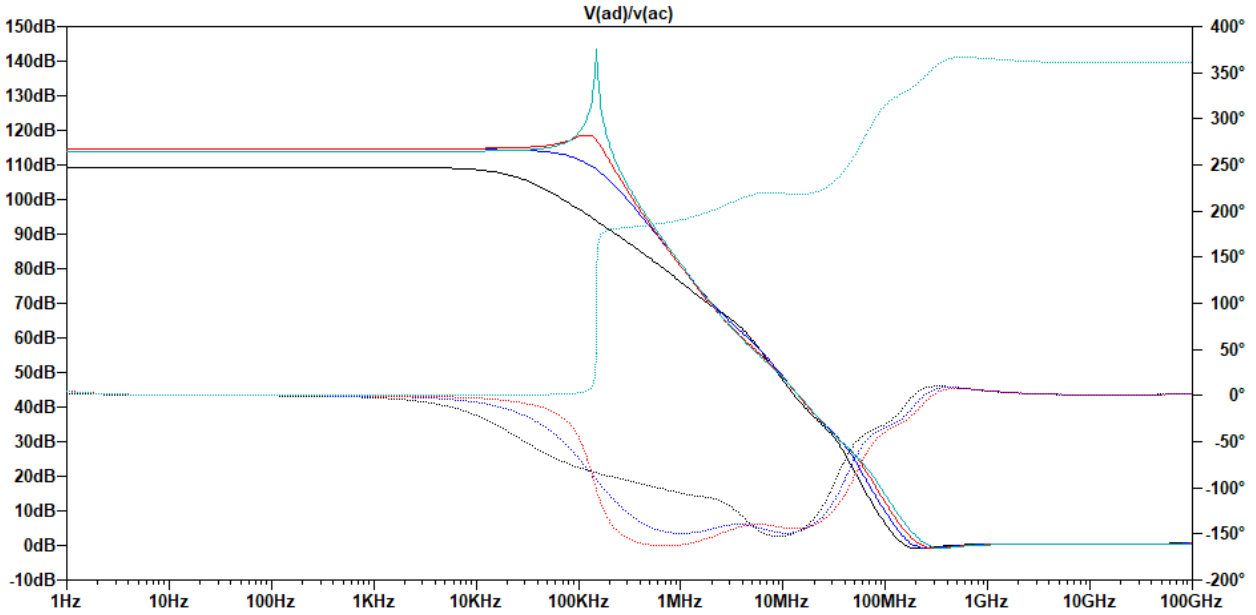

Figure 14: CMRR No Load

Table 7

Supply Voltage	**CMRR @ 100 kHz (No Load)**
VDD = 2V	96.77 dB
VDD = 5V	118.95 dB

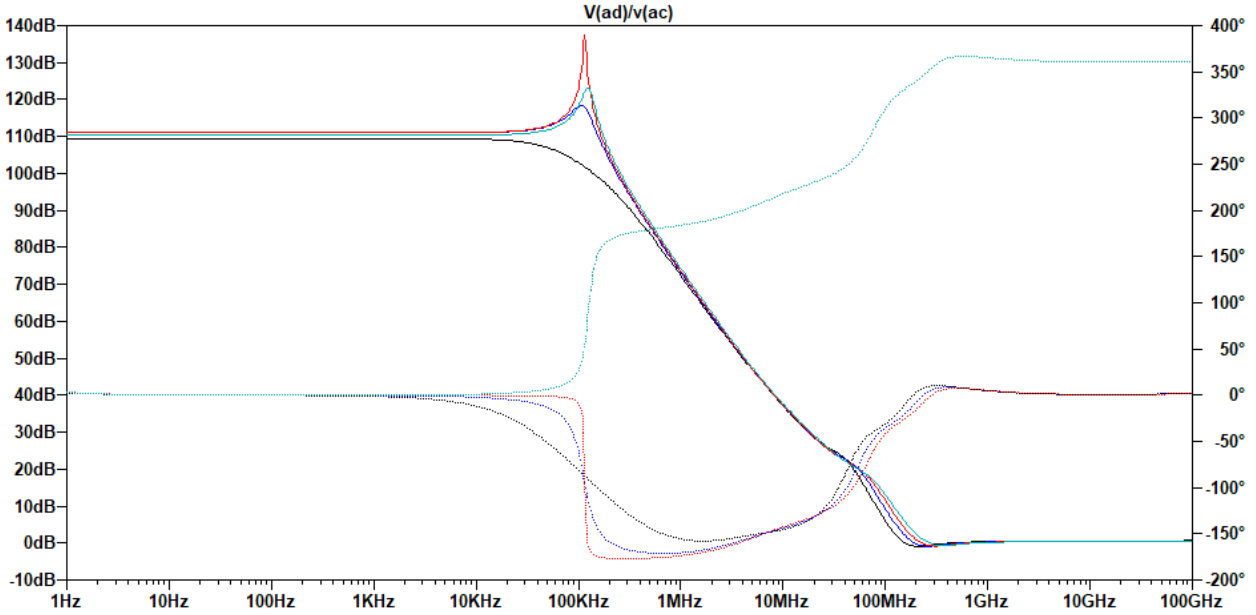

Figure 15

Table 8

Supply Voltage	CMRR @ 100 kHz (Load)
VDD = 2V	102.54 dB
VDD = 5V	118.59 dB

The design requirement for the CMRR is that at 100 kHz, the CMRR should be greater than 90 dB. Tables 7 and 8 testify to the fact that the designed op-amp meets the necessary specification by a great margin.

VI.C. Power Supply Rejection Ration (PSRR)

The PSRR refers to how well the amplifier rejects noise or changes on the VDD or ground rails (see CMOS Book; pg. 807). The test circuit as seen in Figure 16 and Figure 18 is one method to test the PSRR. In an ideal situation, the output signal is independent of VDD and ground variances. There is both positive and negative PSRR.

$$PSRR^{+} = \frac{A_{OL}(f)}{v_{out}/v^{+}} \qquad [38]$$

$$PSRR^{-} = \frac{A_{OL}(f)}{v_{out}/v^{-}} \qquad [39]$$

Measuring $PSRR^{+}$

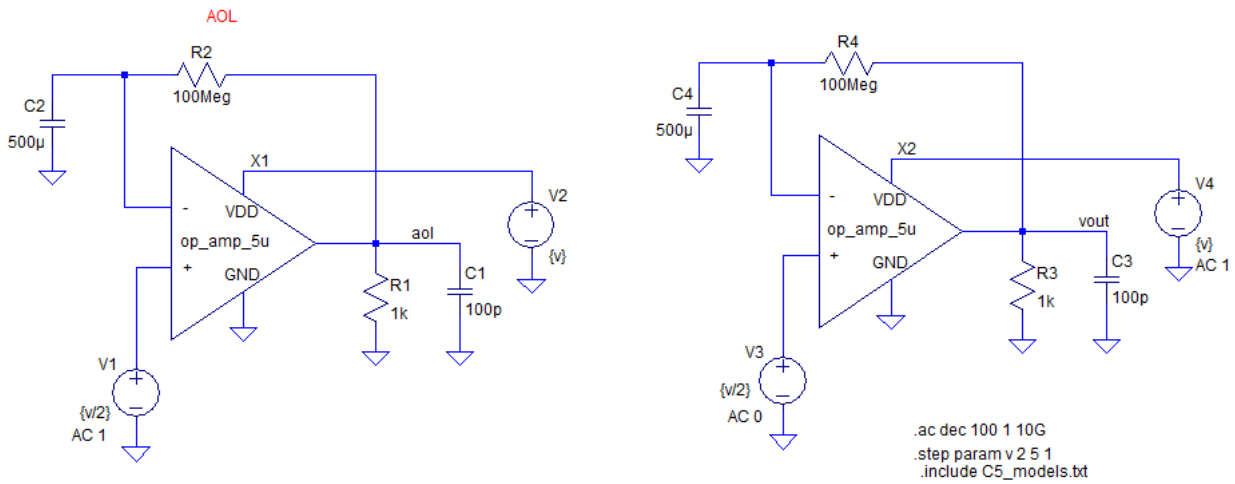

Figure 16: PSRR+ with Load Test Circuit

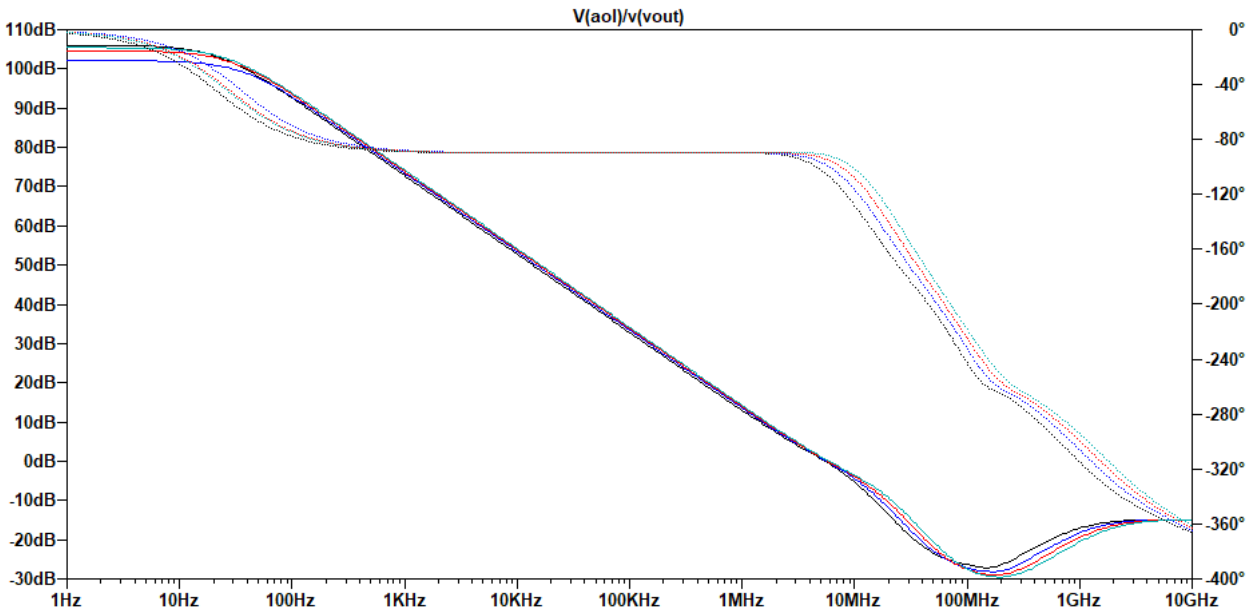

Figure 17: PSRR+ with load; stepping supply voltage

Table 9

Supply Voltage	**PSRR+ @ 1 kHz (Load)**
VDD = 2V	72.40 dB
VDD = 5V	73.80 dB

The requirement for $PSRR^+$ is that at a frequency of 1 kHz the $PSRR^+$ must be greater than 60 dB. The information presented in Figure 17 and Table 9 testify to the fact that the designed op-amp exceeds the $PSRR^+$ requirements.

Measuring PSRR⁻

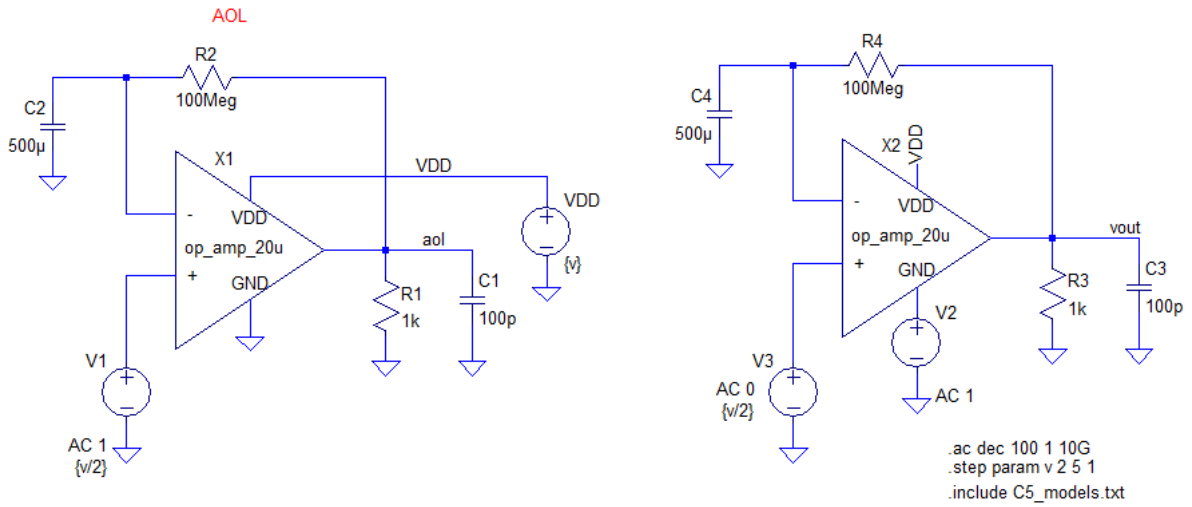

Figure 18: PSRR- with Load Test Circuit

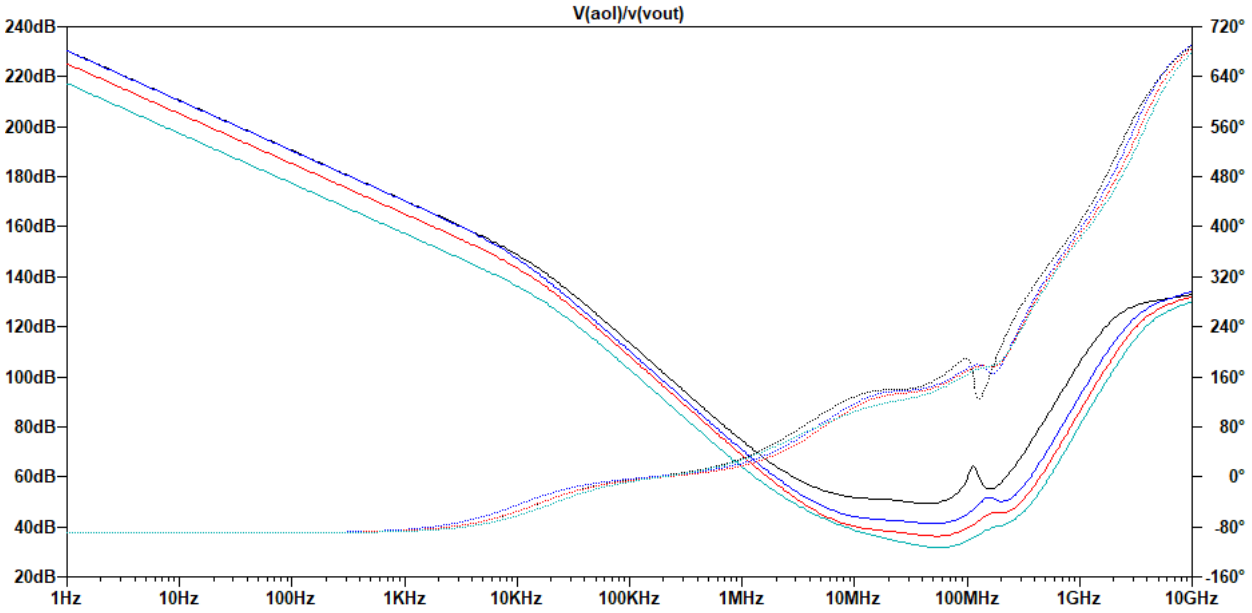

Figure 19: PSRR- with load; stepping supply voltage

Table 10

Supply Voltage	**PSRR- @ 1 kHz (Load)**
VDD = 2V	170.24 dB
VDD = 5V	156.84 dB

The requirement for $PSRR^-$ is that at a frequency of 1 kHz the $PSRR^-$ must be greater than 60 dB. The information presented in Figure 19 and Table 10 testify to the fact that the designed op-amp exceeds the $PSRR^-$ requirements.

VI.D. Step Response and Slew Rate

When the phase margin is 90°, the step-response of the op-amp will have a response of the first order. In other words, the step response will be like the response of an RC circuit (see CMOS Book; pg. 781). As seen previously, in section *VI.A.* the phase margin of the designed op-amp is approximately 90° for all load and supply voltage conditions. Therefore, our op-amp should have a first-order step response. A circuit as seen in Figure 20 can be used to determine the step response of our op-amp. The topology of the op-amp is a voltage follower. If the step response is not a first-order response, the op-amp can be said to be unstable. *Cc1, Cc2, Rz,* and the parameters *diff* and *out* effect the phase margin (i.e. stability) of the circuit. These aforementioned values and parameters need to be fine-tuned such that the op-amp is properly compensated. Figure 21 and 22 show the step response of the op-amp. It can clearly be seen that the op-amp has a first-order step and is, therefore, stable. Additionally, the step-response is a first-order response for all supply voltage conditions.

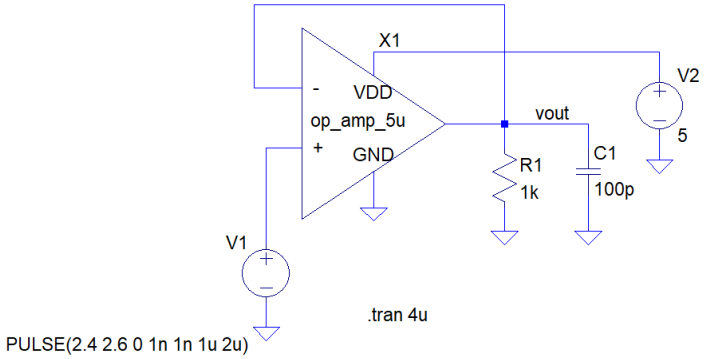

Figure 20

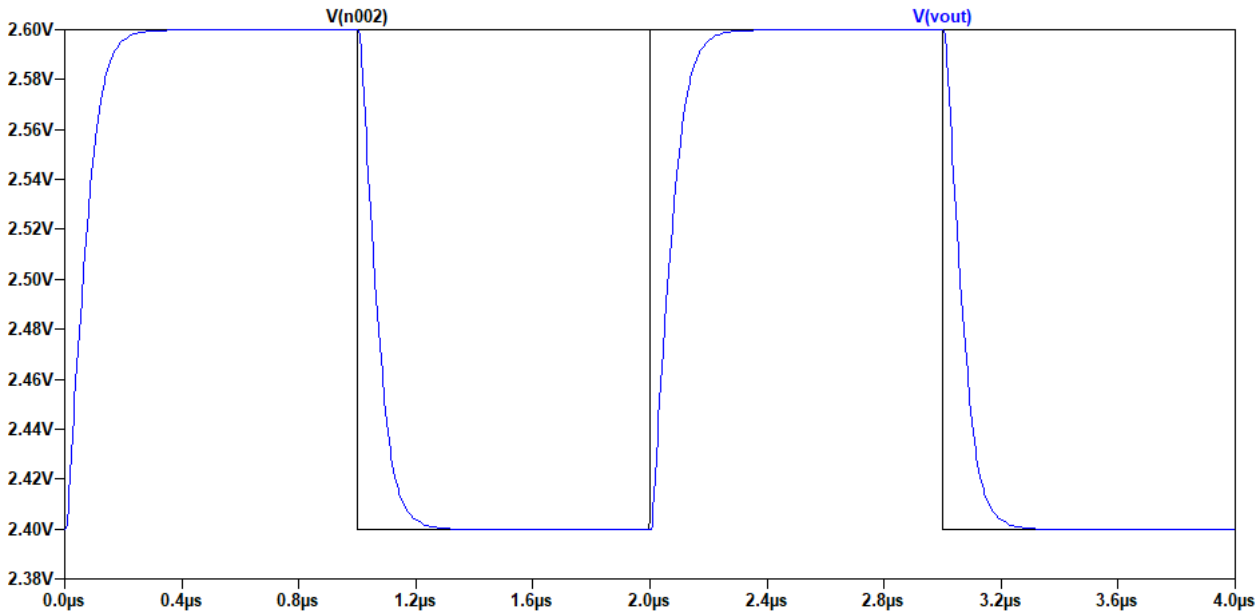

Figure 21

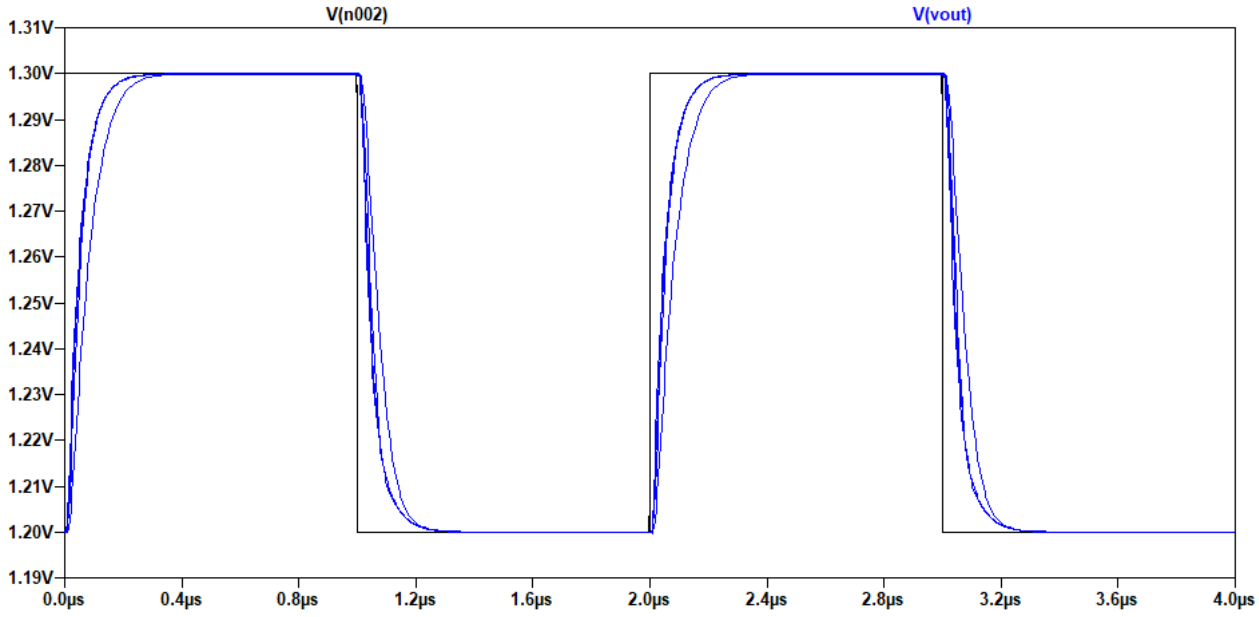

Figure 22: Step-response; stepping supply voltage

The speed of an op-amp can be determined how quickly the output voltage responds to a change in the input voltage. A good metric to measure speed is the slew rate. An amplifier's slew rate is the greatest rate at which the output voltage can change. The same circuit can be used to measure the slew rate of the op-amp.

$$Slew\ Rate = \frac{\triangle Voltage}{\triangle Time} = \frac{\boldsymbol{d}}{\boldsymbol{dt}} V(t) \qquad [40]$$

Table 11

Supply Voltage	Slew Rate (Load)
VDD = 2V	1.02 V/µs
VDD = 3V	1.46 V/µs
VDD = 4V	1.64 V/µs
VDD = 5V	1.75 V/µs

The design requirement for the slew rate is that the op-amp should have a slew rate greater than 1 V/µs while driving max load. Table 11 and Figure 22 testify that our op-amp meets or exceeds this requirement for all supply voltage conditions. One issue is that at a supply voltage of 2V, the slew rate requirement is just barely met. The reference current of the designed op-amp is 5 µA. Upon looking at Table 4, one can see that the unity gain frequency is proportional to the reference current. If the reference current is increased, the speed (slew-rate) of the op-amp will increase, but the gain will decrease. Therefore, one may fix this issue of slew rate, by increasing the reference current. However, a trade-off would occur. The power consumption would increase, and the gain would decrease. In fact, an op-amp with a 20 µA reference was created and its slew rate was in the range of 5 µA/V.

VI.E. Power Consumption

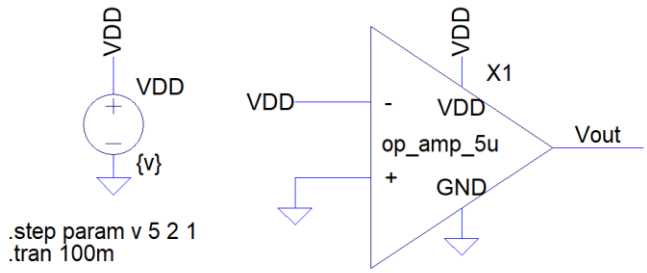

Figure 23

The circuit as seen in Figure 23 can be used to measure the power consumption of an op-amp at quiescent conditions.

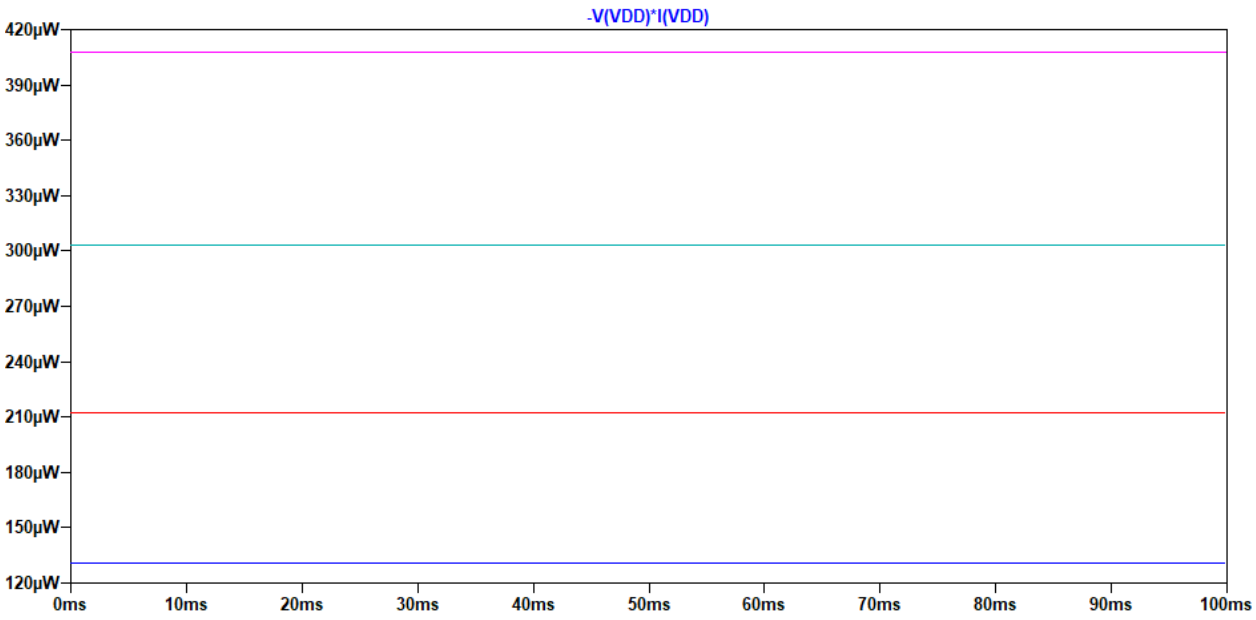

Figure 24: Power consumption; while stepping supply voltage

Table 12

Supply Voltage	**Power Consumption at Quiescent Conditions**
VDD = 2V	131.02 µW
VDD = 5V	407.72 µW

The same circuit as seen in Figure 23 can be used to measure the current draw of the op-amp at quiescent conditions.

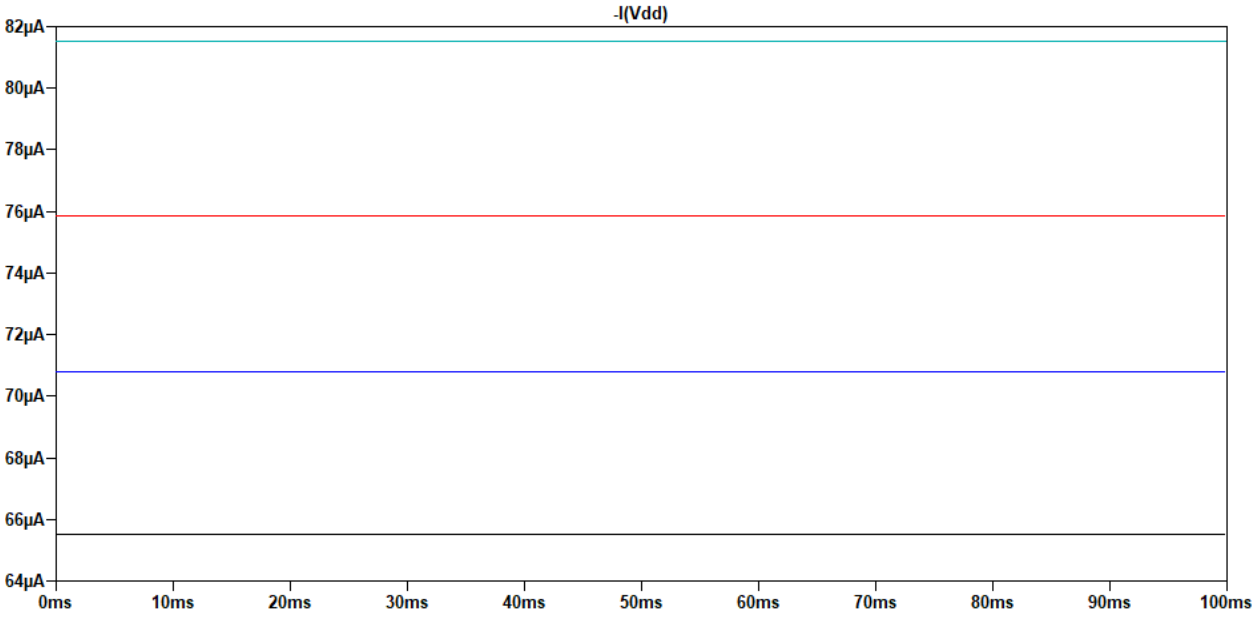

Table 13

Supply Voltage	Current Draw at Quiescent Conditions
VDD = 2V	65.50 µA
VDD = 5V	81.54 µA

VI.F. Output Swing

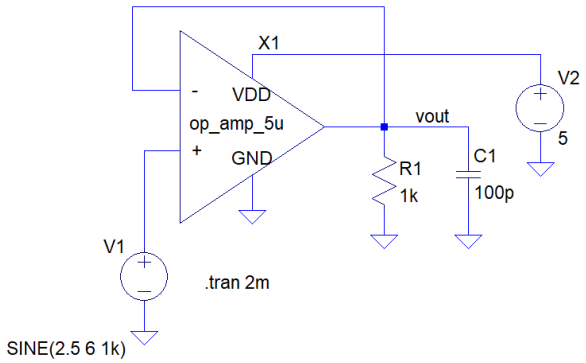

Figure 25

The voltage follower circuit as seen in Figure 25, can be used to determine the output swing of the op-amp when a large signal is inputted.

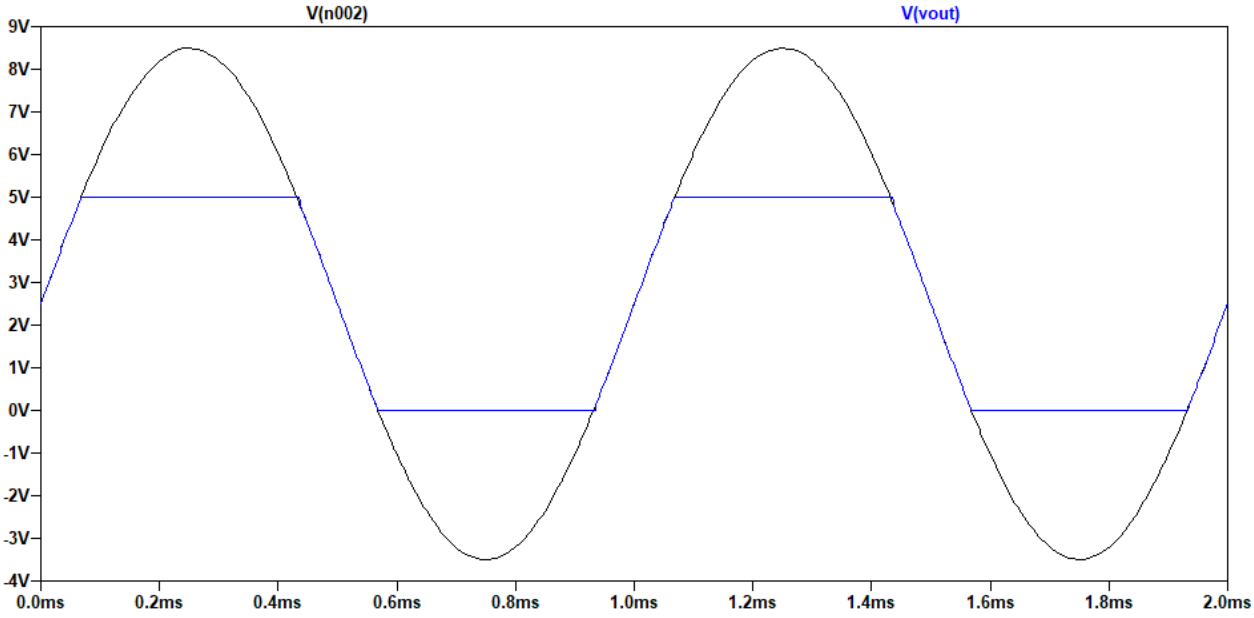

Figure 26

In Figure 26, the output swing of the op-amp is rail to rail (5V) with a supply voltage of 5V.

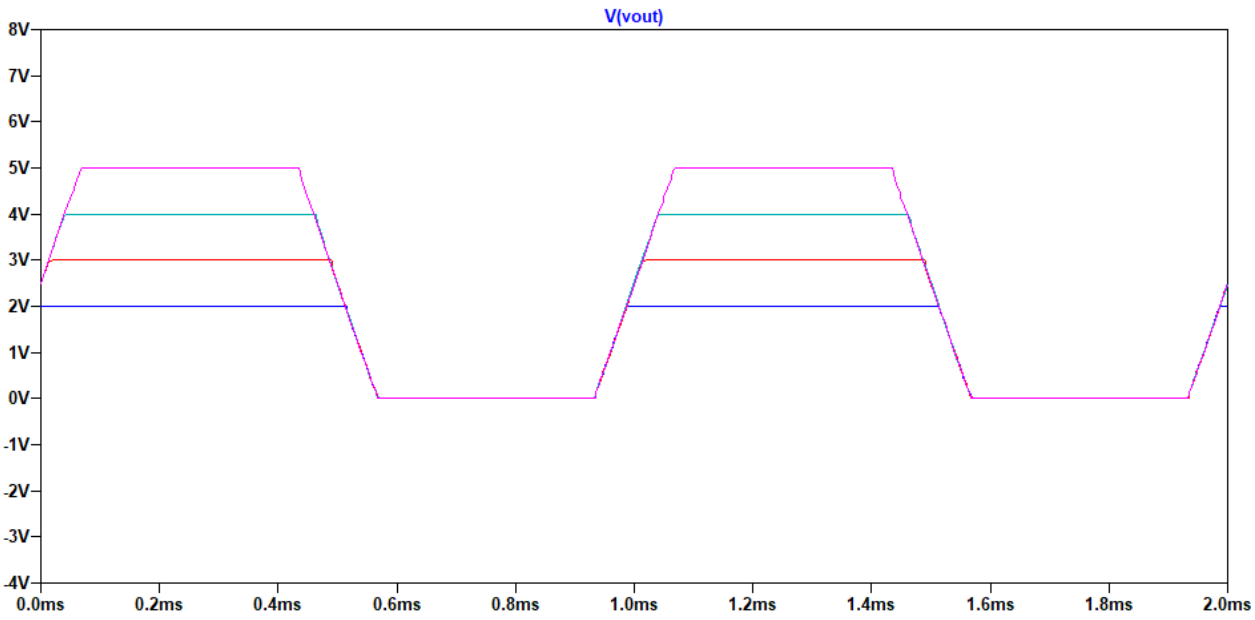

Figure 27

In Figure 27, we see that the output swing is 0-VDD.

VI.G. Implementation of Op-Amp into an Inverting Topology

The standard inverting op-amp topology can be seen in Figure 28. Equation 41 describes the gain of an inverting topology.

$$Gain = \frac{Vout}{Vin} = -\frac{RF}{RI} \quad [41]$$

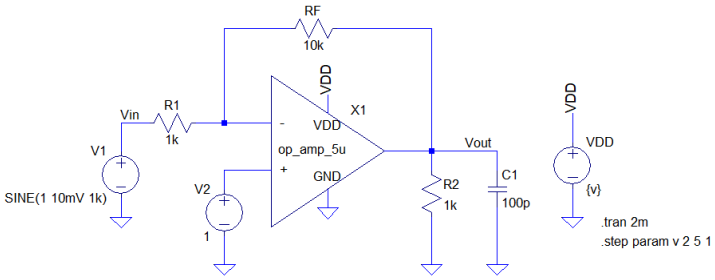

Figure 28

The gain of the op-amp given in Figure 28 can be found by implementing Equation 41.

$$Gain = \frac{Vout}{Vin} = -\frac{10k}{1k} = -10\ V/V \quad [42]$$

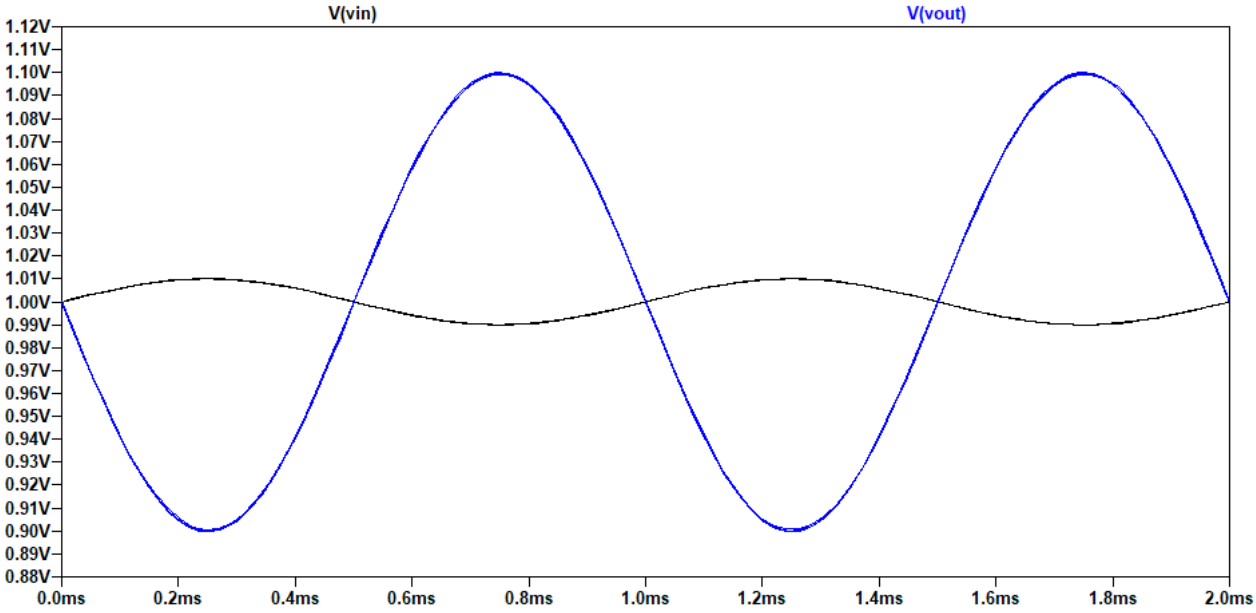

Figure 29: Test of an Inverting Topology

Figure 29 demonstrates the simulation of the inverting topology and demonstrates a gain of -10 V/V. In the simulation, the supply voltage is stepped from 2-5V in 1V increments. The inverting topology functions properly despite changes in the supply voltage.

VI.H. Implementation of Op-Amp into a Non-Inverting Topology

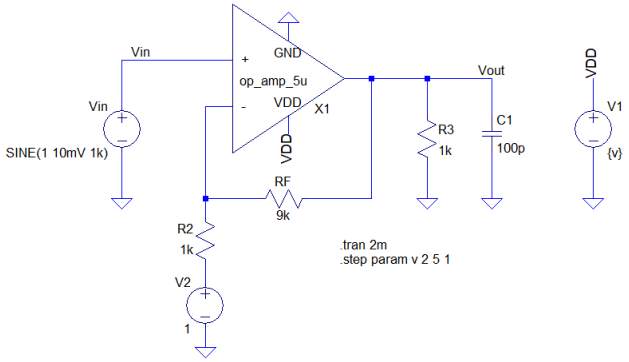

Figure 30

The standard non-inverting op-amp topology can be seen in Figure 30. Equation 43 describes the gain of a non-inverting topology.

$$Gain = \frac{Vout}{Vin} = 1 + \frac{RF}{R2} \quad [43]$$

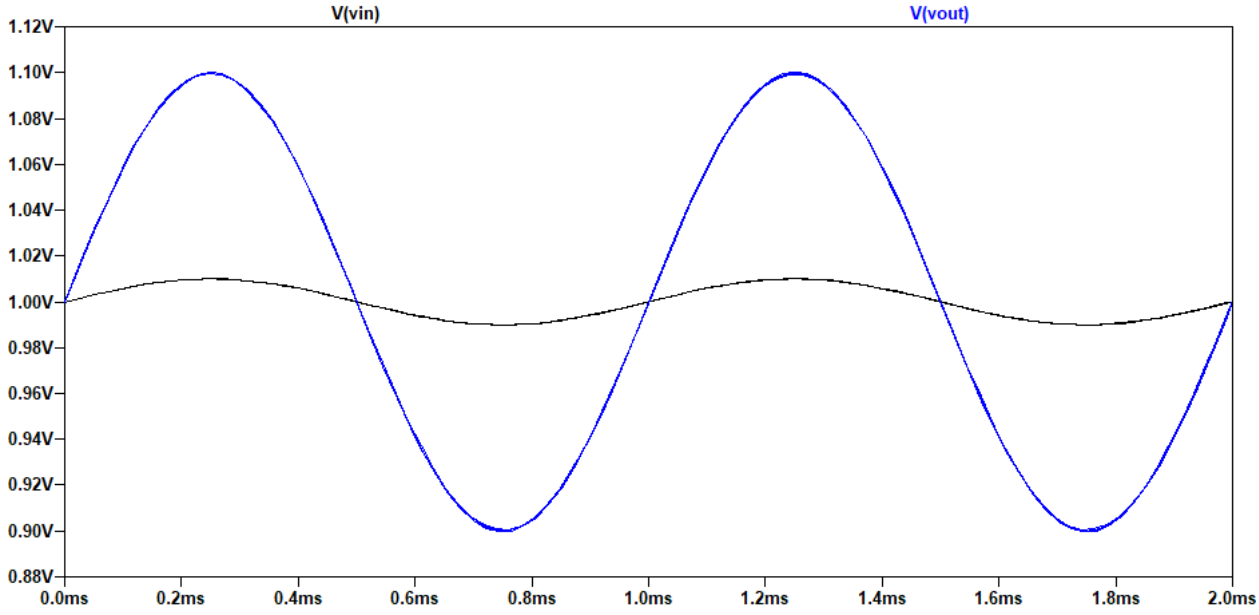

Figure 31

The gain of the op-amp given in Figure 30 can be found by implementing Equation 43.

$$Gain = \frac{Vout}{Vin} = 1 + \frac{9k}{1k} = 1 + 9 = 10\ V/V \quad [44]$$