THE DESIGN OF A VARIABLE DPLL CLOCK MULTIPLIER: A TUTORIAL PRESENTATION

A Course Presentation for ECG 721: Memory Circuit Design

Given By: Bryan Kerstetter

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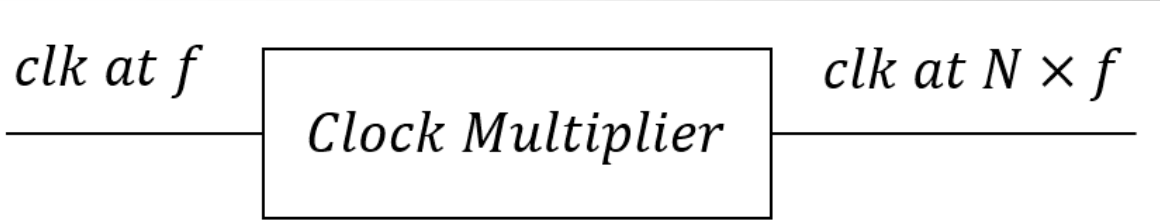
UNLV | HOWARD R. HUGHES COLLEGE OF ENGINEERING

CLOCK MULTIPLIERS

- A clock multiplier has an input clock signal with a frequency f, such that the output of the clock multiplier is a clock signal with a frequency $N \times f$.
- Where N is the multiplication factor of the clock multiplier.
- The output clock will have N cycles for every input clock cycle.

The Presentation:

- A previously designed clock multiplier and its flaws will be discussed.
- The design of a new Variable DPLL Clock Multiplier will be introduced.



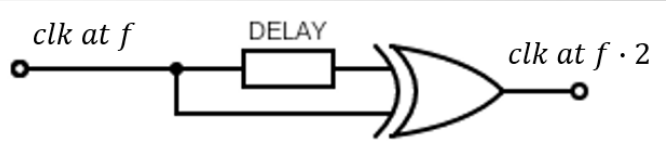
4X EDGE DETECTOR CLOCK MULTIPLIER

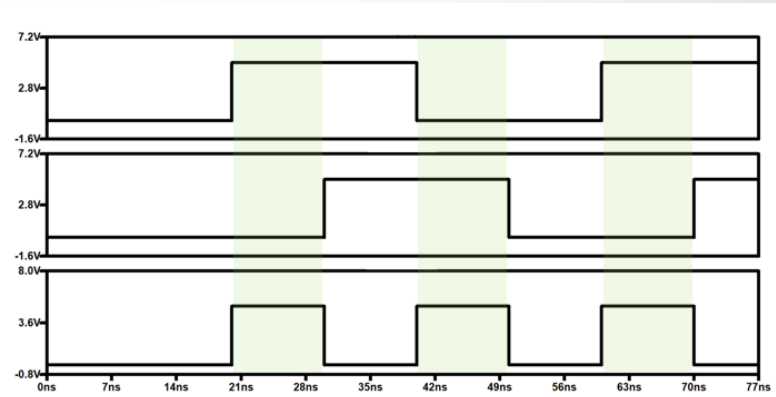
THE EDGE DETECTOR CLOCK MULTIPLIER

- Previously, I designed, simulated and laid out a CMOS 4x Clock Multiplier for EE 421L.
- A simple 2x Clock Multiplier can be created with an edge detector.
- The CMOS 4x Clock Multiplier design utilized two edge detectors in series, resulting in a multiplication factor of 4.
- This method allows you to get multiplication factors in multiples of 2.
- The length of each respective delay, to ensure an output duty cycle of 50%, is determined by the following equation:

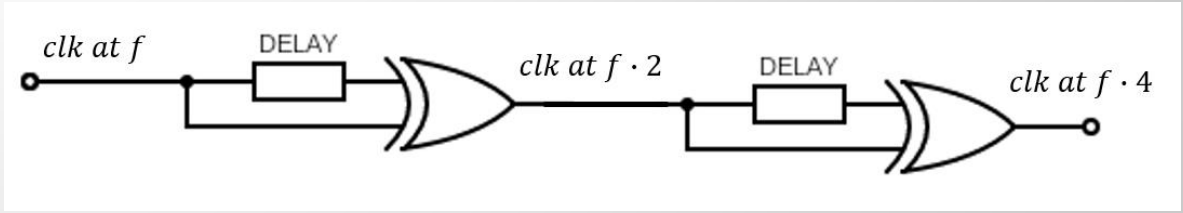
$$D_n = \frac{1}{f \cdot 2^{n+1}}$$

- Therefore, the length of the delays are directly dependent upon the input frequency.





A	B	$A \oplus B$
0	0	0
0	1	1
1	0	1
1	1	0



THE EDGE DETECTOR CLOCK MULTIPLIER: THE FLAW

- A huge shortcoming of the simple edge detector approach to create a clock multiplier, is that it only functions upon specific input frequencies.
- For a 4x Edge Detector Clock Multiplier, consider how greatly the length of the delays change for a small change in frequency:

9 MHz

$$D_1(9MHz) \approx 28ns$$

$$D_2(9MHz) \approx 14ns$$

10 MHz

$$D_1(9MHz) \approx 25ns$$

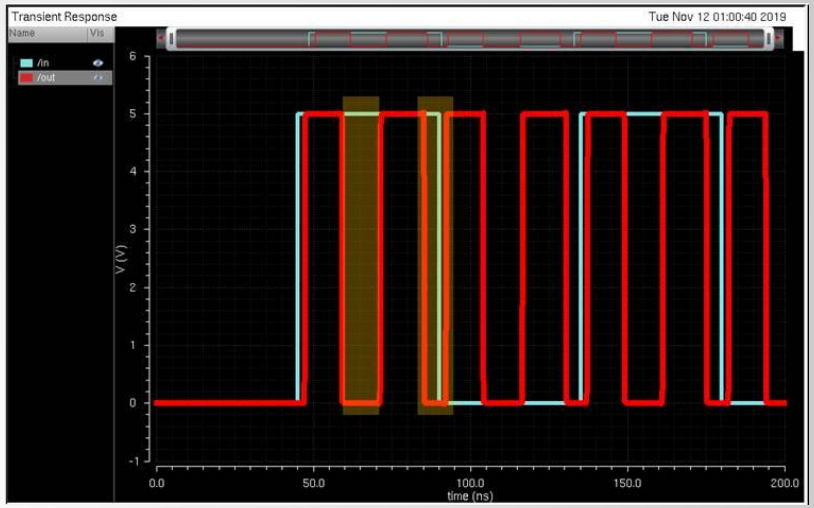
$$D_2(9MHz) \approx 12.5ns$$

11 MHz

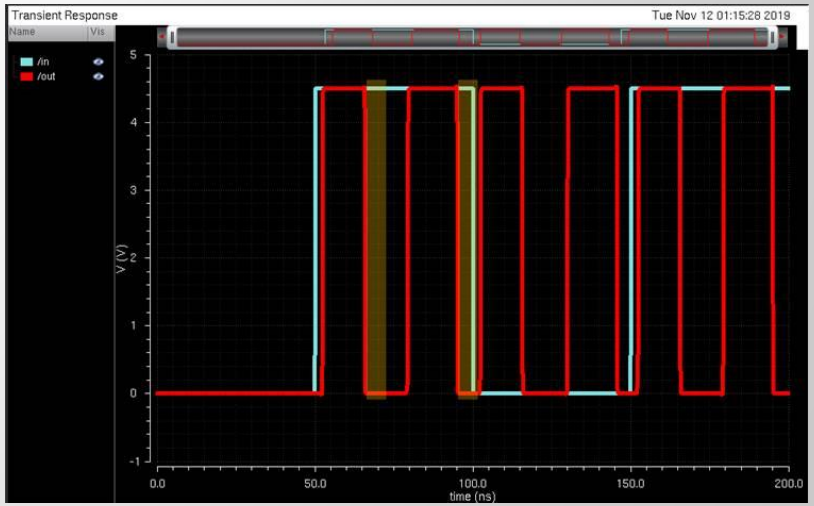
$$D_1(9MHz) \approx 22.73\,ns$$

$$D_2(9MHz) \approx 11.36ns$$

- If the input frequency of the Edge Detector Clock Multiplier is not the specific frequency that it was designed for, the output signal will have distortion and the duty cycle will not be 50%.

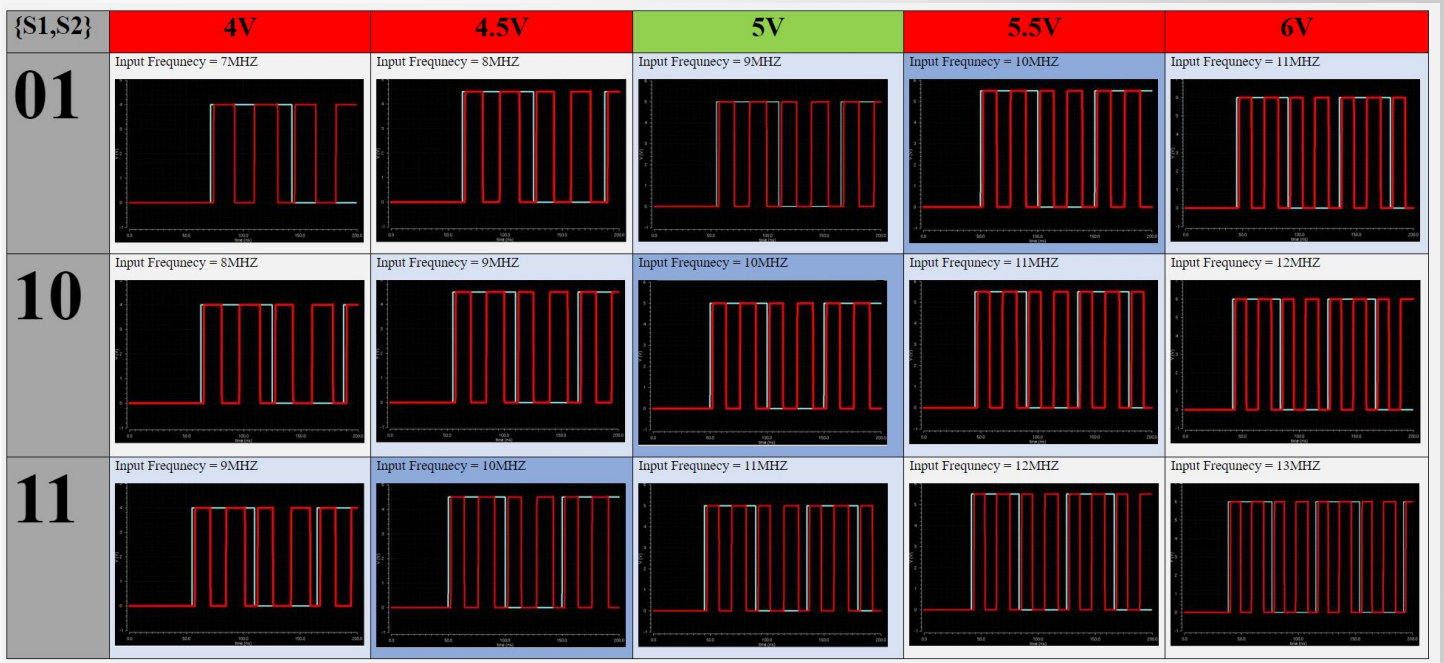


Duty Cycle ≠ 50%



THE EDGE DETECTOR CLOCK MULTIPLIER: AN UNIDEAL SOLUTION TO THE FLAW

- My solution at the time was to use voltage-controlled delays to have the ability to adjust the delay times. This would allow a broader, yet still restrictive, range of possible input frequencies.
- Issues with this solution:
  - Not Autonomous
    - The user must know both input frequency and supply voltage.
    - Then the user most program the correct select codes or provide the correct arbitrary voltage input.
  - The input frequency range is not wide.

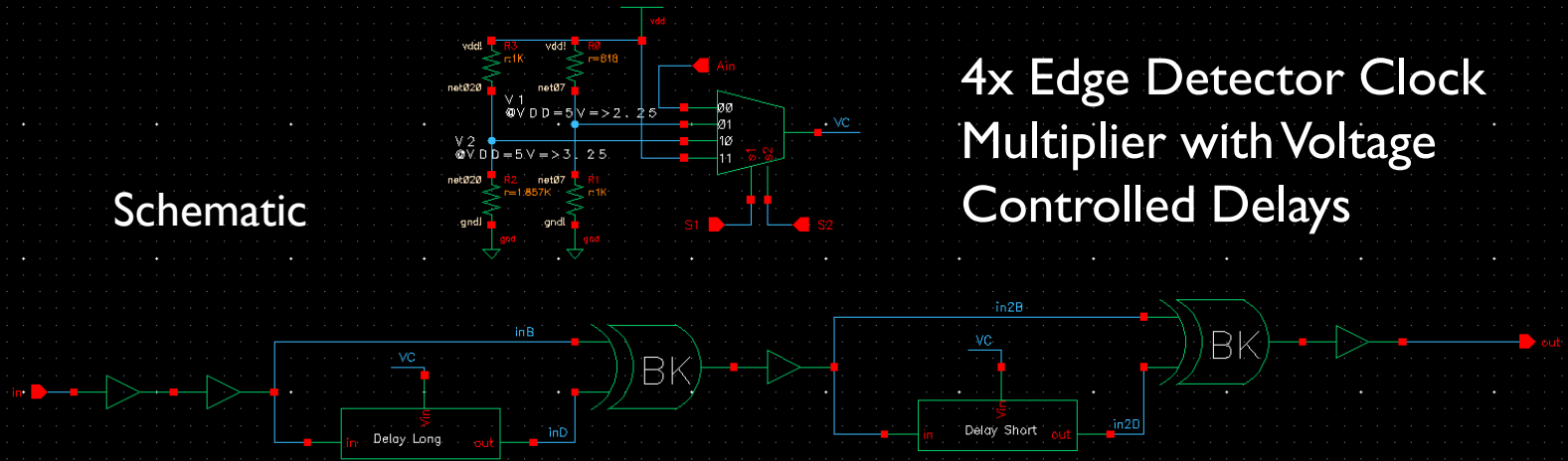


S1	S2	Voltage Control	VDD= 4	4.5	5	5.5	6
0	0	Ain	Ain	Ain	Ain	Ain	Ain
0	1	V1	7MHz	8MHz	9MHz	10MHz	11MHz
1	0	V2	8MHz	9MHz	10MHz	11MHz	12MHz
1	1	VDD	9MHz	10MHz	11MHz	12MHz	13MHz

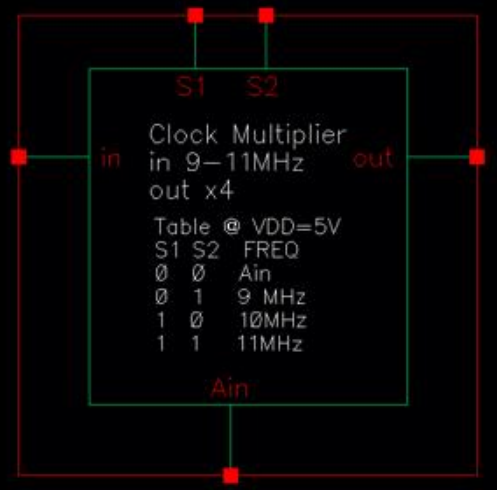
Voltage Control	VDD= 4	4.5	5	5.5	6
Ain	Ain	Ain	Ain	Ain	Ain
V1	2.20	2.48	2.75	3.03	3.30
V2	2.58	2.91	3.23	3.55	3.88
VDD	4V	4.5V	5V	5.5V	6V

4x Edge Detector Clock Multiplier with Voltage Controlled Delays

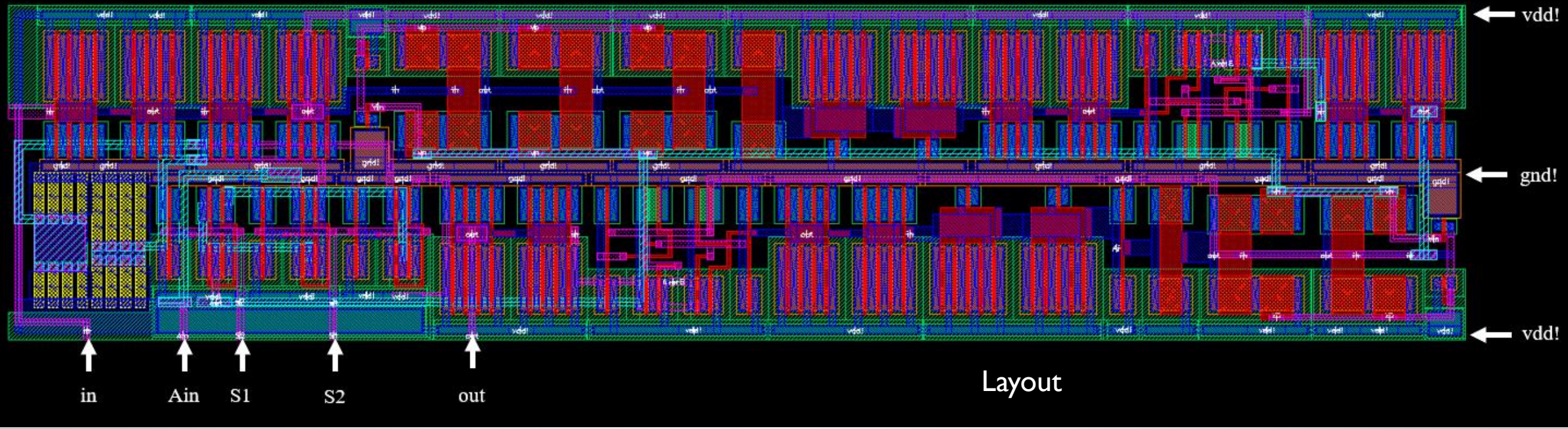
Schematic



Symbol



Layout



VARIABLE DPLL CLOCK MULTIPLIER

ON SEMICONDUCTOR'S NB3N511 CLOCK MULTIPLIER

- Considering, the issues exhibited in my previous 4x Edge Detector Clock Multiplier design, I was driven to find a better and more versatile clock multiplier methodology. I noticed that clock multipliers on the market used PLL design tecniques.
- NB3N511 Clock Multiplier Defining Characteristics:
  - Accommodates a wide range of input frequencies
  - Programmable multiplier
  - Guarantees a 45%-55% output duty cycle
  - Two possible input signal methods
    - Crystal Reference
    - Input Clock Frequency

Features

- Clock Output Frequencies up to 200 MHz
- Nine Selectable Multipliers of the Input Frequency
- Operating Range: V_{DD} = 3.3 V ±10% or 5.0 V ±5%
- Low Jitter Output of 25 ps One Sigma (rms)
- Zero ppm Clock Multiplication Error
- 45% – 55% Output Duty Cycle
- TTL/CMOS Output with 25 mA TTL Level Drive
- Crystal Reference Input Range of 5 – 32 MHz
- Input Clock Frequency Range of 1 – 50 MHz
- OE, Output Enable with Tri–State Output
- 8–Pin SOIC
- Industrial Temperature Range –40°C to +85°C
- These are Pb–Free Devices

MOTIVATION

- The goal was to design a clock multiplier with the aforementioned defining characteristics in the short channel process.
- The NB3N511 Logic Diagram will be used as a template.

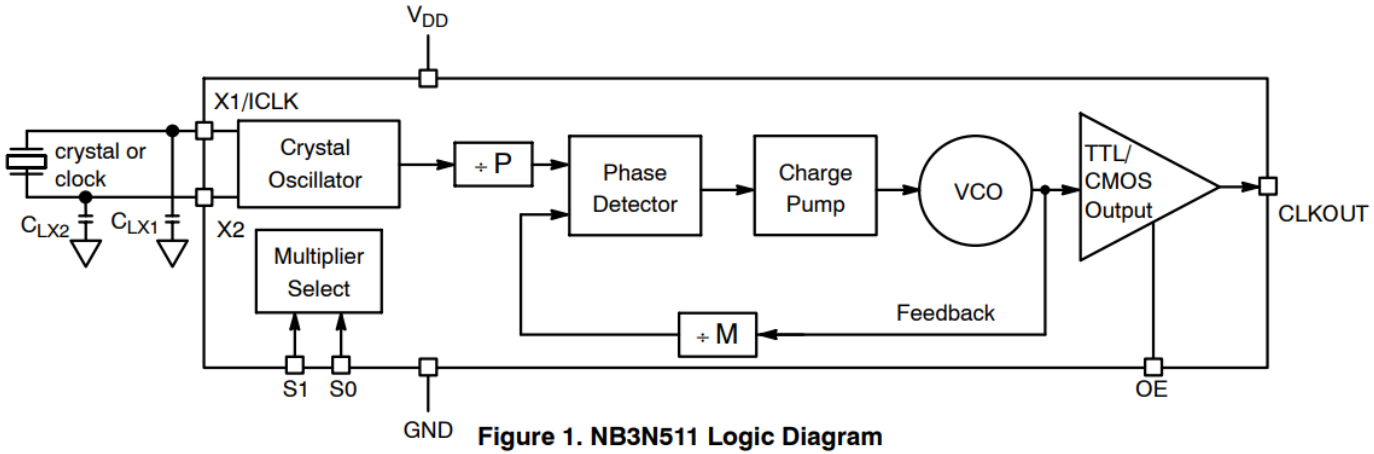


Figure 1. NB3N511 Logic Diagram

THE BK1VCMA: A VARIABLE DPLL CLOCK MULTIPLIER

- The logic diagram of the BK1VCMA (Bryan Kerstetter 1 Volt Clock Multiplier A) can be compared to that of the NB3N511.
- The BK1VCMA Design Consists of:
  - Crystal Interface
  - Phase Frequency Detector (PFD)
  - Charge Pump
  - Voltage-Controlled Oscillator (VCO)
  - Output Buffer
  - Variable Clock Divider
  - Beta Multiplier Reference (BMR) Bias Circuit
- The multiplier select codes adhere to the table below:

S1	S2	Multiplier
0	0	X2
0	1	X4
1	0	X6
1	1	X8

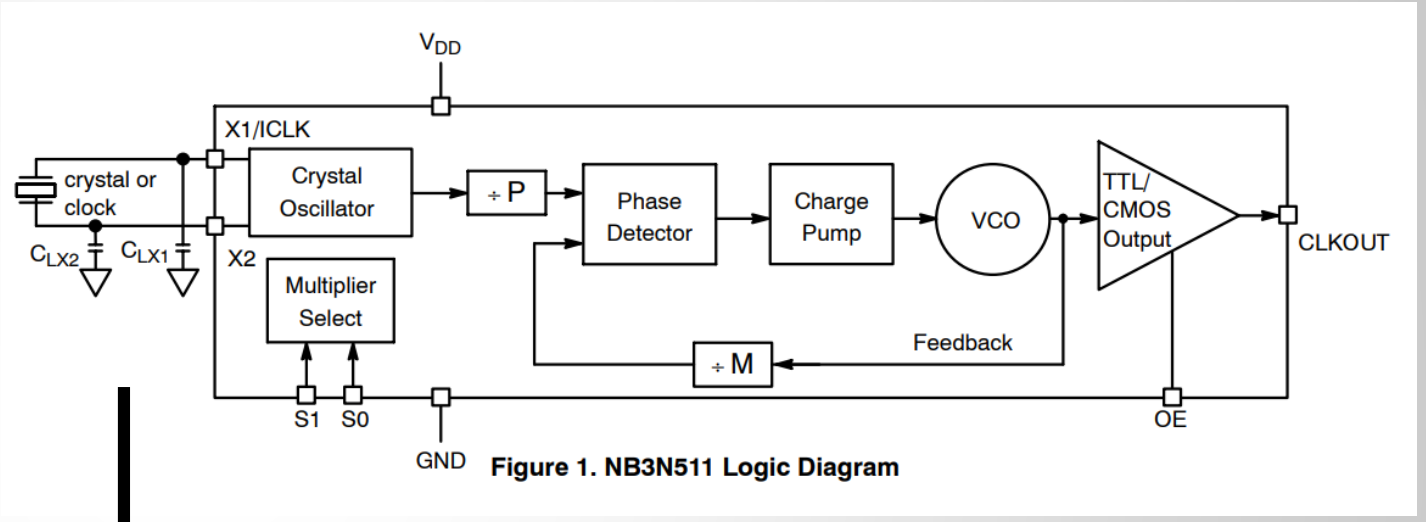
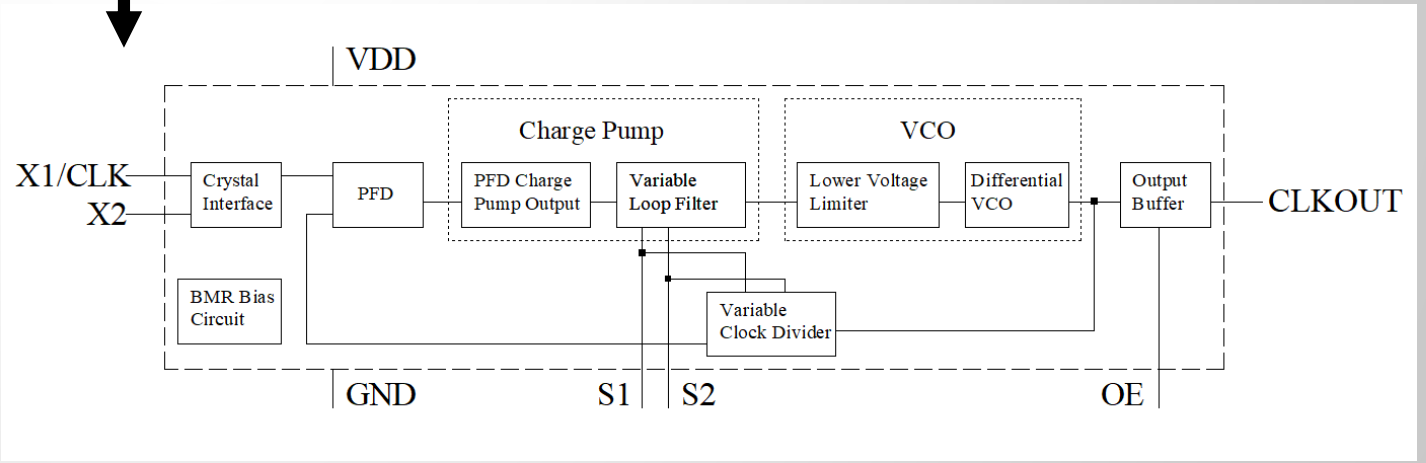
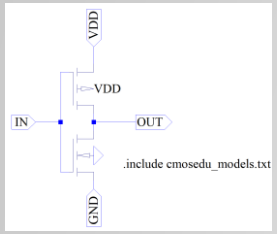


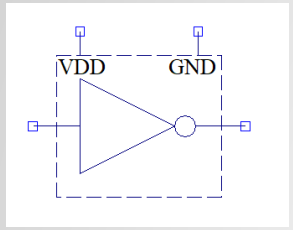
Figure 1. NB3N511 Logic Diagram



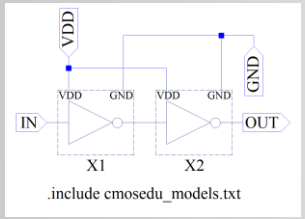
BUILDING BLOCKS

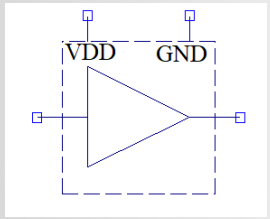
Inverter



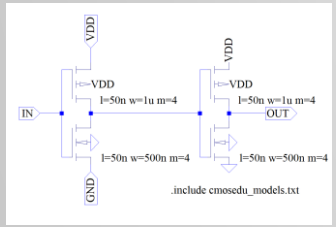


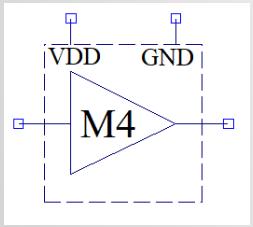
Buffer



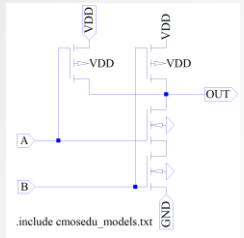


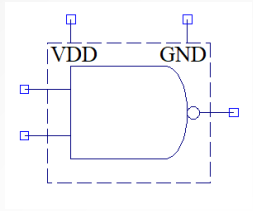
BufferM4



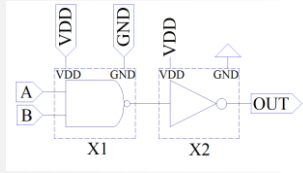


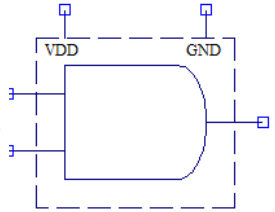
NAND



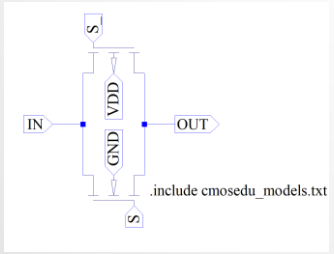


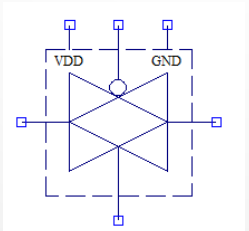
AND



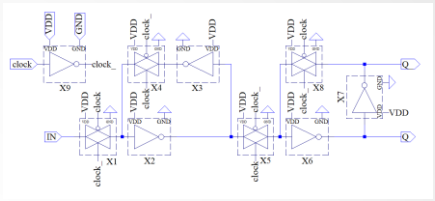


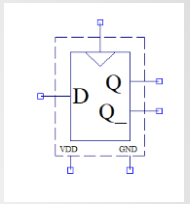
Transmission Gate



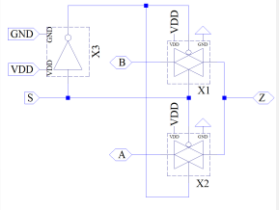


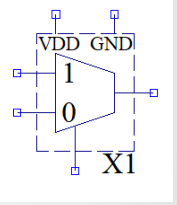
D-Flip-Flop



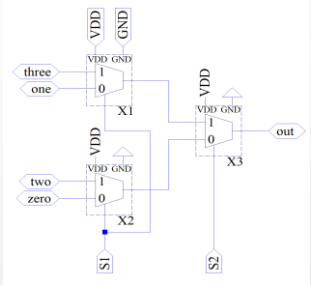


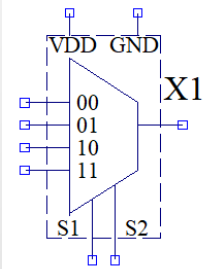
2:1 MUX/DEMUX





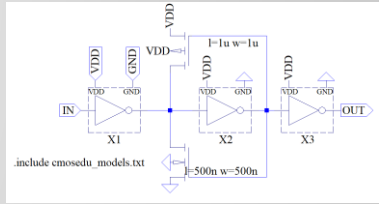
4:1 MUX/DEMUX

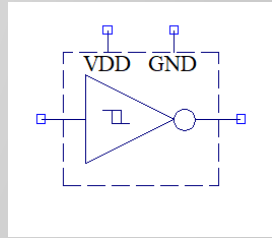




These devices will be used throughout the presentation.

Schmitt Trigger





Please consider the following geometries for all unmarked MOSFETs in the small channel process throughout this presentation:

NMOS: L=50n ; W=500n

PMOS: L=50n ; W=1μ

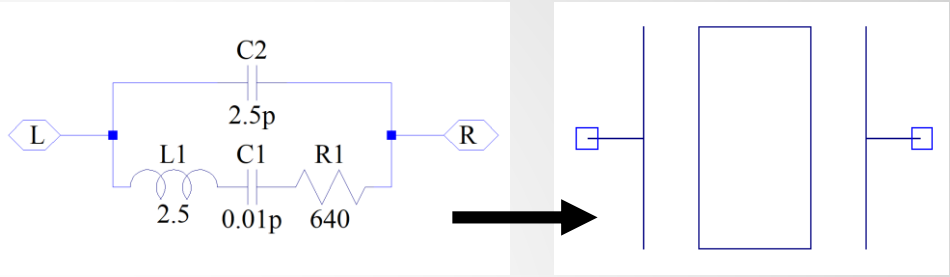
THE CRYSTAL INTERFACE I

- A crystal interface was created to accommodate either a crystal reference or an input clock.
- The goal of the interface:

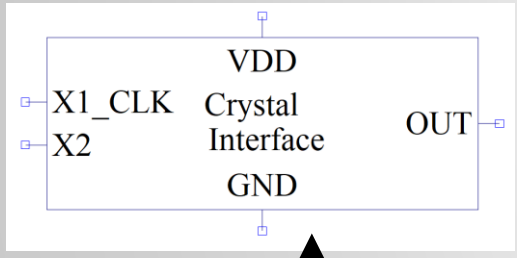
  Create square wave from crystal reference

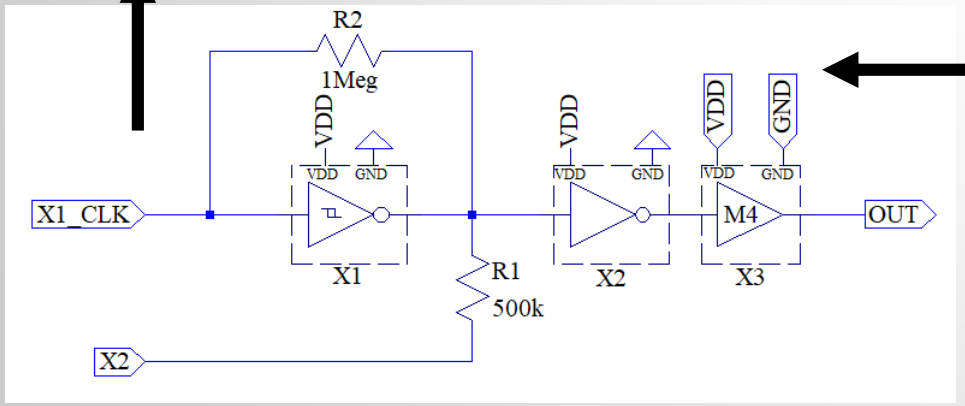
  OR

  Pass input clock through interface

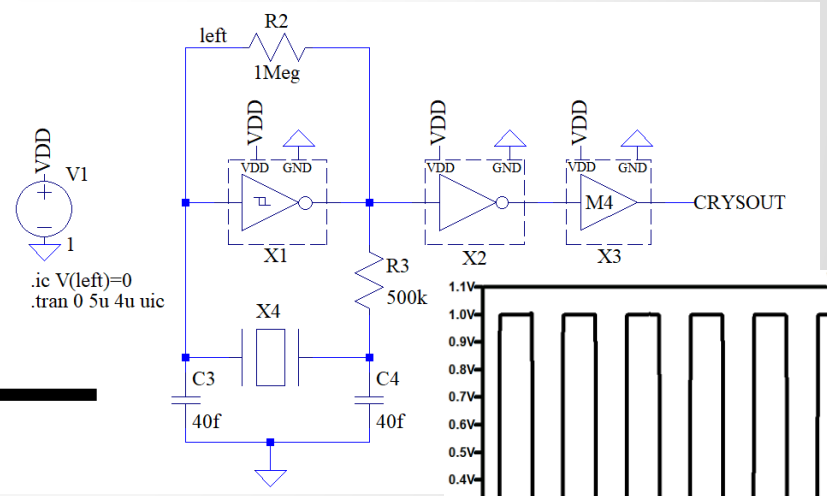


A Electrical Model of a Crystal Oscillator

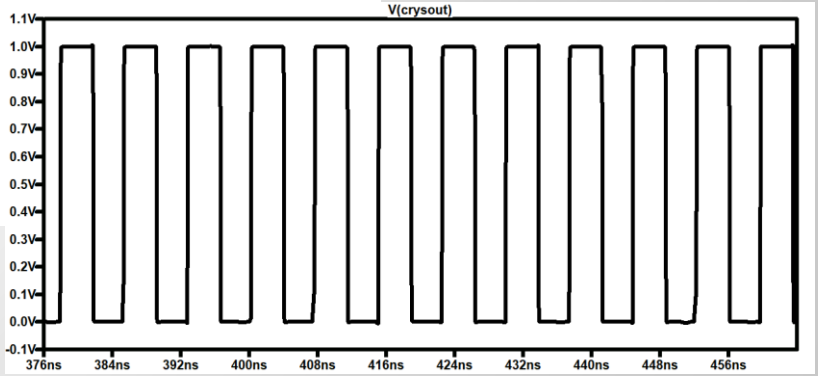




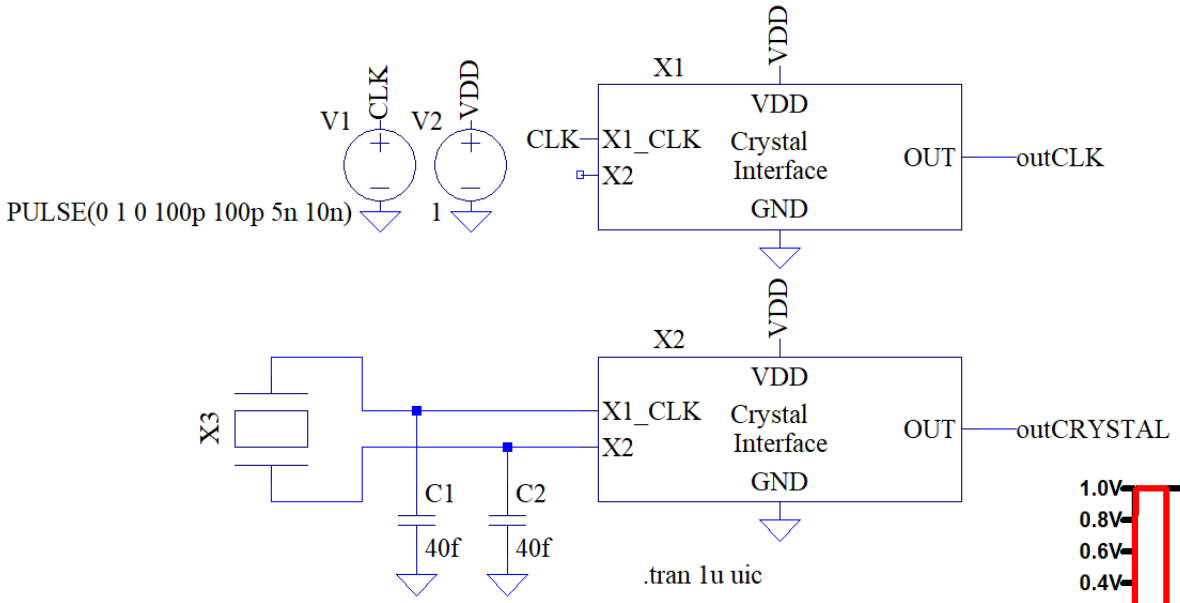
A Crystal Interface Circuit Can be Derived



Circuit to Derive a Square Wave From a Crystal Oscillator

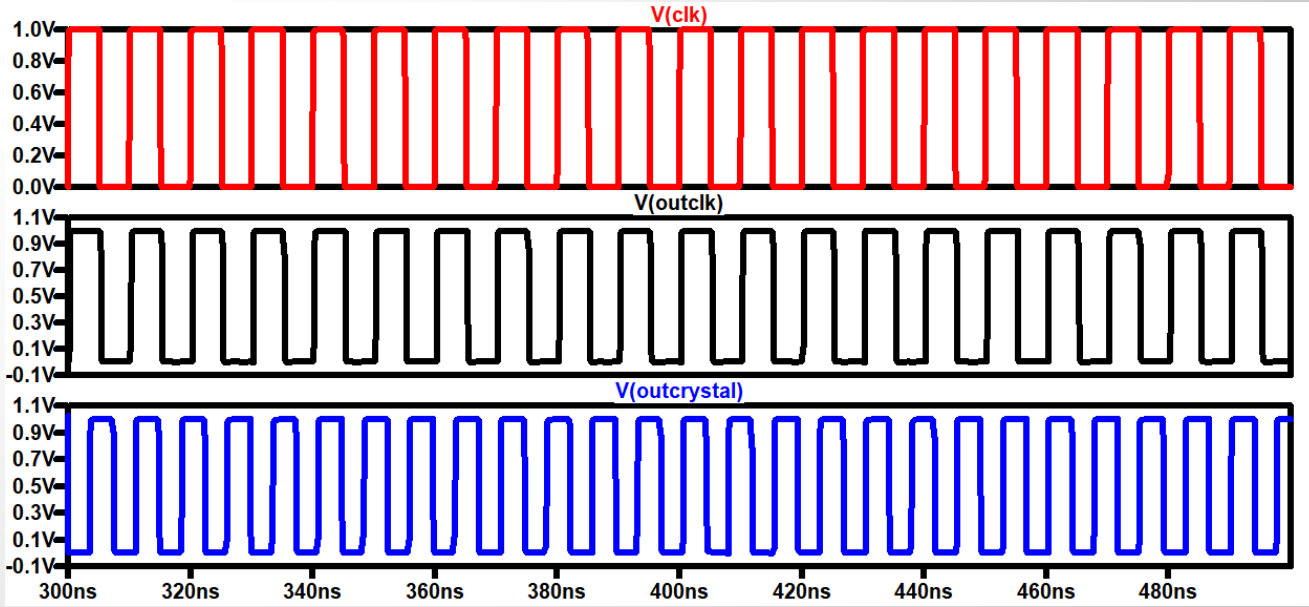


THE CRYSTAL INTERFACE II



Crystal Interface Test Circuit

- In this simulation, it can be demonstrated that the crystal interface functions as intended.
- This interface is used in the BK1VCMA design so that the clock multiplier can accommodate two input methods.



Simulation Results

A DIFFERENTIAL VCO I

- The differential VCO is an adaption of Figures 19.58 and 19.61 in Dr. Baker's CMOS book.
- This approach creates a practical VCO that is resistant to noise on the power rail.
- The half replica bias circuit creates bias voltages that causes the differential ring to swing from GND to Vref.
- Circuitry was also included to create linear voltage to current conversion.
- Vref is generated by the general bias circuit and should be VDD/2 or 0.5V.
- A self-biased PMOS differential amplifier is included in the replica bias circuit to force the drain of M10 to Vref.

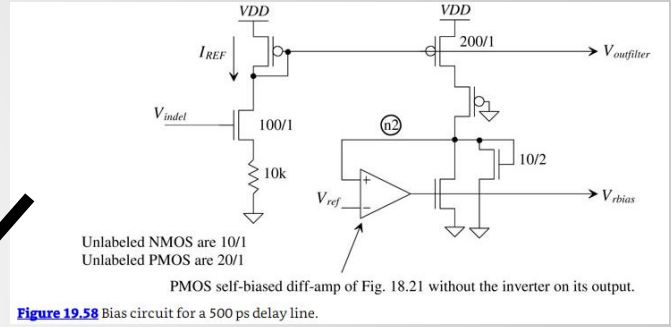
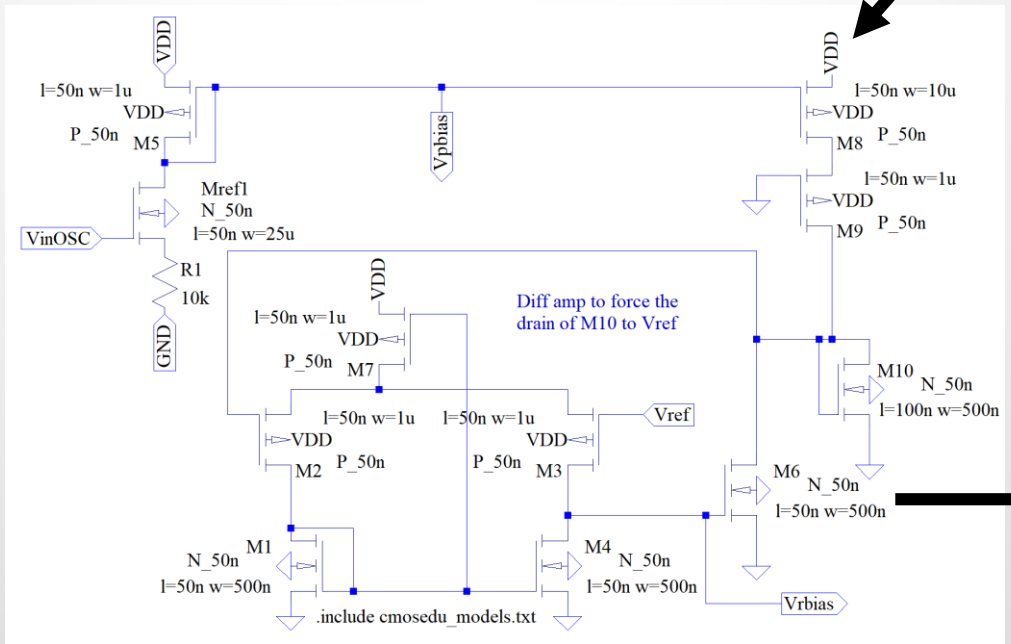
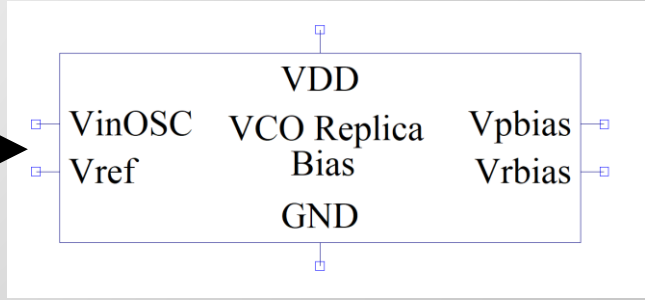
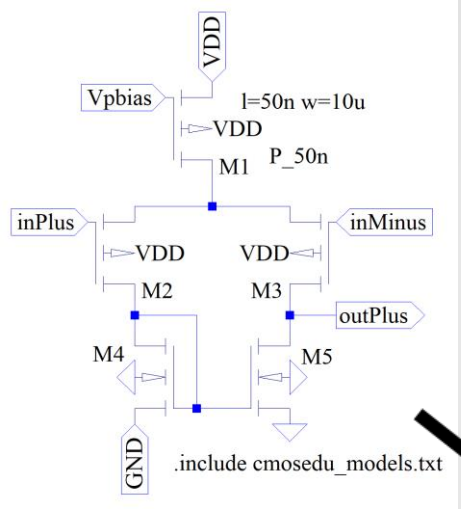


Figure 19.58 Bias circuit for a 500 ps delay line.





A DIFFERENTIAL VCO II



The eight stage Voltage-Controlled Delay (VCDL) was adapted to create a differential ring VCO.

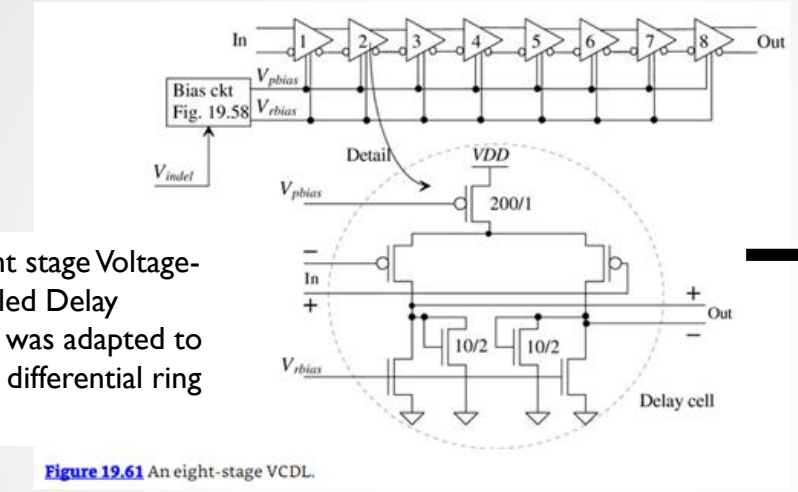
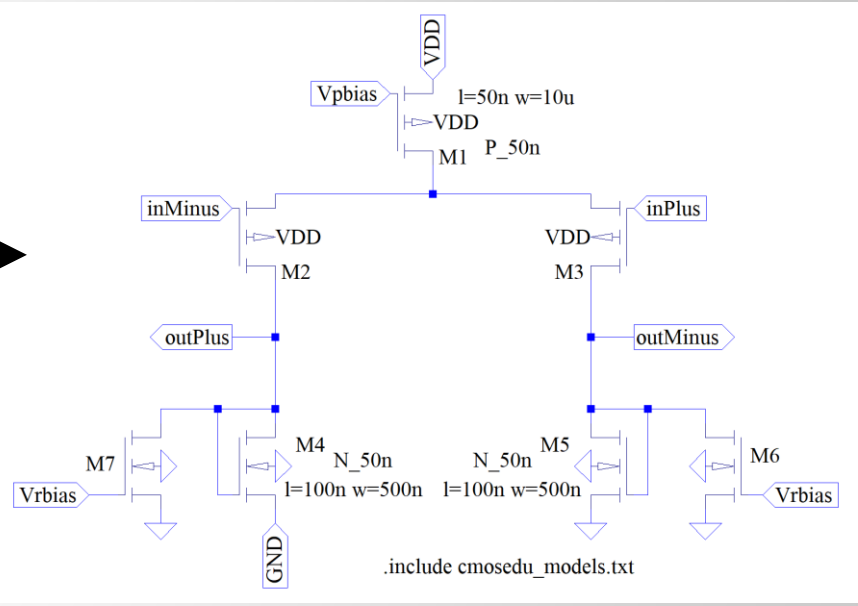
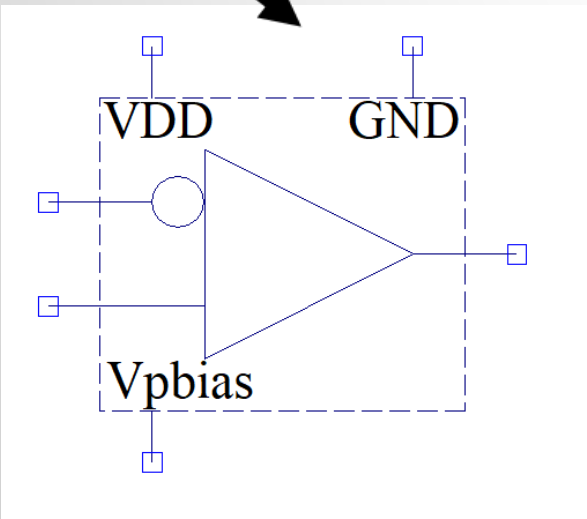
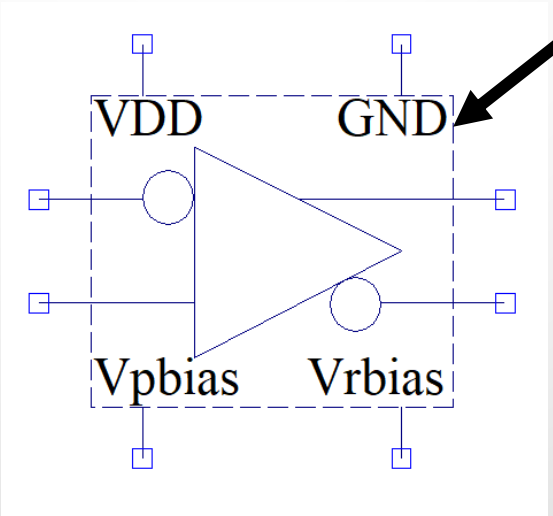


Figure 19.61 An eight-stage VCDL.



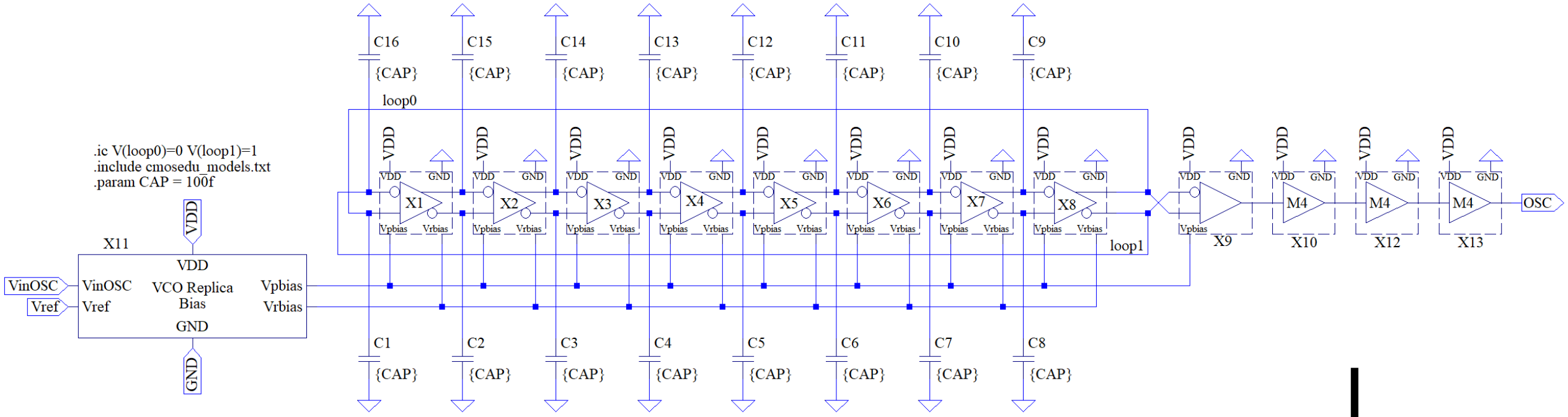
A simple single-ended differential amplifier is used to convert a differential signal to a single-ended signal.



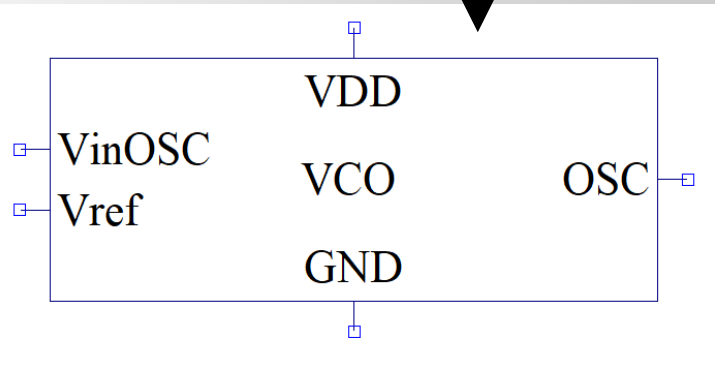


Eight VDCDL elements are used to create the differential ring oscillator.

A DIFFERENTIAL VCO III

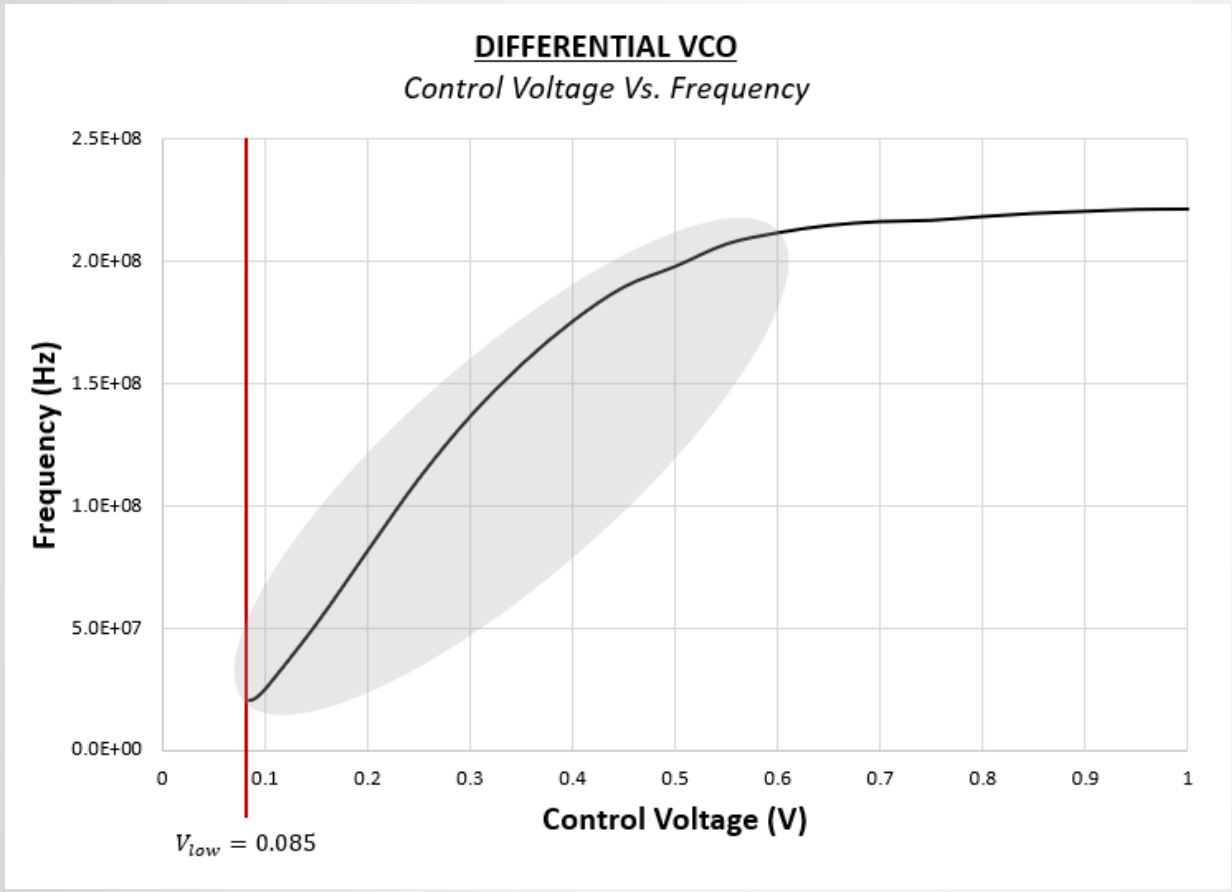


- The final VCO consists of the bias circuitry, differential ring, and output buffer
- There are capacitors are attached to each stage of the differential ring.
  - These capacitors allow for easy tuning of the oscillation frequency.
- The single-ended differential amplifier is used to tap a signal from within the differential ring.
- A set of three buffers are placed at the output to ensure that the edges are quick.



A DIFFERENTIAL VCO IV

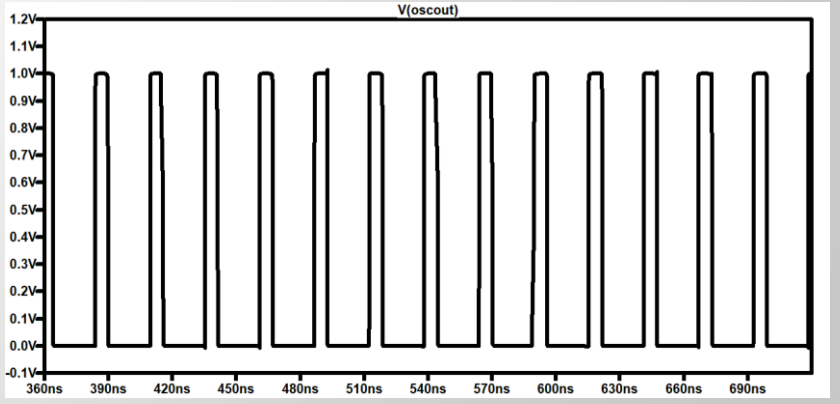
Control Voltage(V)	Frequency (Hz)
0.085	2.0560E+07
0.09	2.1254E+07
0.1	2.4995E+07
0.15	5.1657E+07
0.2	8.1538E+07
0.25	1.1105E+08
0.3	1.3647E+08
0.35	1.5767E+08
0.4	1.7539E+08
0.45	1.8941E+08
0.5	1.9779E+08
0.55	2.0696E+08
0.6	2.1154E+08
0.65	2.1457E+08
0.7	2.1613E+08
0.75	2.1665E+08
0.8	2.1819E+08
0.85	2.1950E+08
0.9	2.2033E+08
0.95	2.2108E+08
1	2.2122E+08



$$\therefore K_{VCO} = \frac{f_{max} - f_{min}}{V_{max} - V_{min}} = \frac{2\pi(2.1154\times10^{8} - 2.056\times10^{7})}{0.6 - 0.085} = 2.33 \times 10^{9} \ {}^{radians}/_{V\cdot s}$$

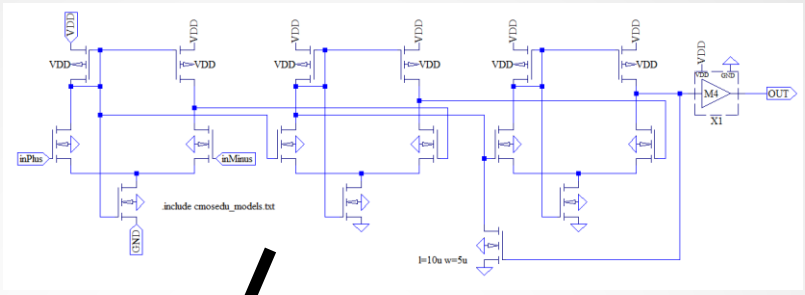
- In an effort to replicate the output frequency range of the NB3N51, frequency range was prioritized over linearity.
- Linearity was still considered (the linear section is highlighted in grey).
- If the control voltage dipped below 85 mV, the duty cycle would no longer be 50% (see simulation below).
- Range of VCO:
  20.56 MHz - 221.22 MHz

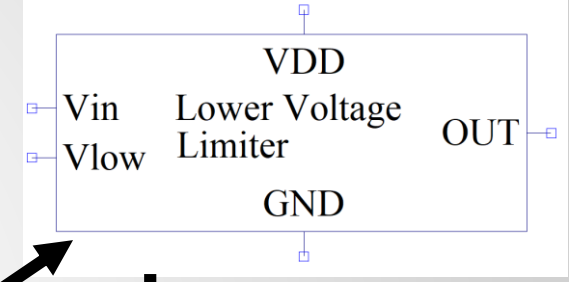
Simulation of Control Voltage at 0.7V:

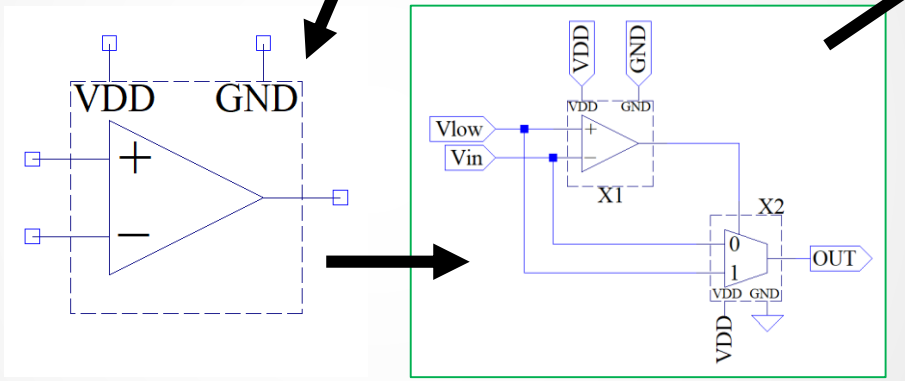


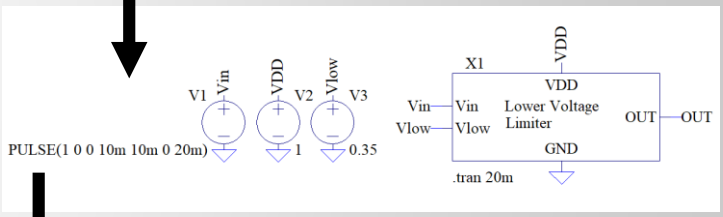
A DIFFERENTIAL VCO V

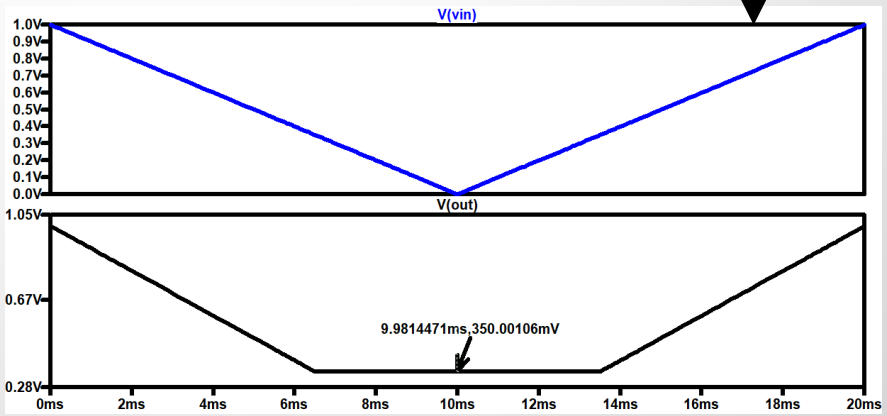
- To ensure that under all circumstances the VCO output signal has a 50% duty cycle, the control voltage of the VCO must not go below 0.085V.
- A circuit can be created with the following operation:
  - If the input voltage is below Vlow
    - Output Vlow
  - If the input voltage is greater than Vlow
    - Output input voltage
- This circuit can easily be created by using a comparator and a 2:1 MUX/DEMUX.
- This circuit is a crucial tool to ensure that the clock multiplier output always has around a 50% duty cycle.
- The Vlow voltage of 85 mV will be generated by the general bias circuit.











Notice how the voltage does not go below Vlow.

PHASE-FREQUENCY DETECTOR (PFD)

- An XOR DPLL (Digital Phase-Locked Loop) only functions properly when the input and output frequencies are very similar.
- In the case of a clock multiplier, the input and output frequencies are greatly different. Therefore, an XOR DPLL is not a good choice for a clock multiplier design.
- The PFD DPLL is preferable when designing a clock multiplier because the output is not only dependent upon the phase, but also the frequency.
- The output of the PFD are two signals referred to as *UP* and *DOWN*.
- These two signals must be used to produce a single signal.
- The gain for the PFD is:

$$K_{PDI} = \frac{I_{pump}}{2\pi}$$

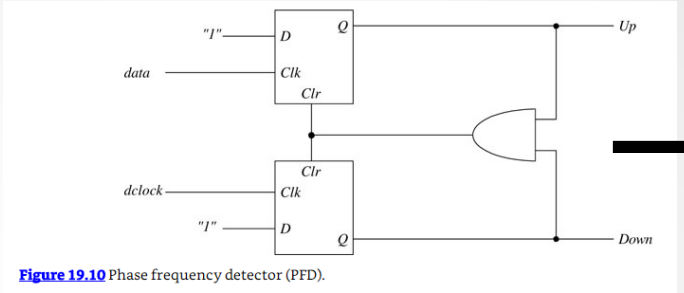


Figure 19.10 Phase frequency detector (PFD).

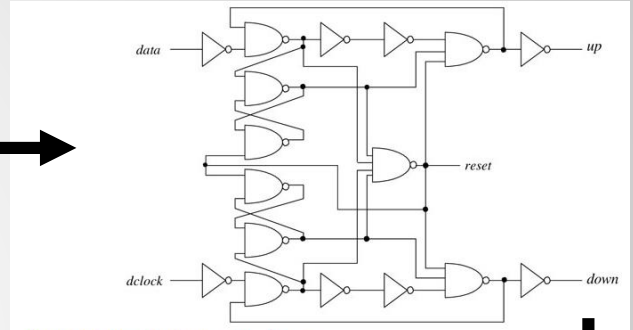
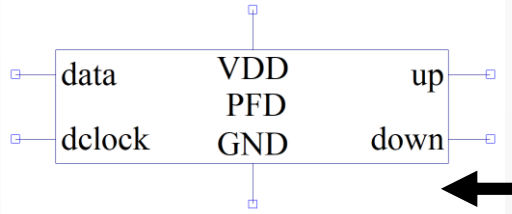
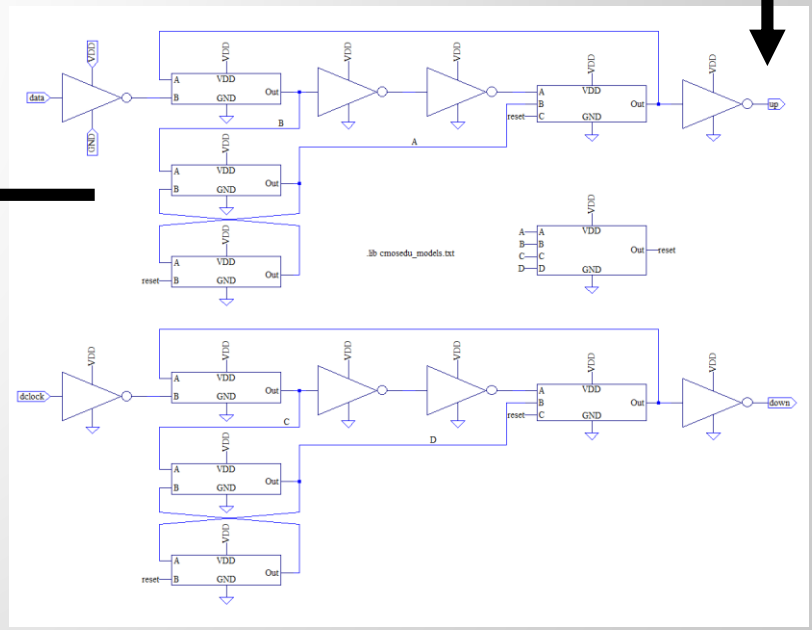


Figure 19.33 CMOS implementation of a PFD.





The PFD used is the PFD that Dr. Baker provides in his LTspice directory for CMOS Chapter 19.

PFD CHARGE PUMP OUTPUT I

- A circuit was drafted based upon the circuit topology given in Figure 19.37 in Dr. Baker's CMOS book.
- The loop transfer function can be derived in the following manner (while neglecting C_2; usually $C_2 = 0.1 \times C_1$):

$$F(s) = R + \frac{1}{sC_1} = \frac{sRC_1}{sC_1} + \frac{1}{sC_1} = \frac{1 + sRC_1}{sC_1}$$

- Therefore, the order of R and C_1 is not important. With respect to Figure 19.37, the order of R and C_1 will be swapped. This will allow the resistance to be variable with respect to the multiplier.
- A 4:1 MUX/DEMUX will be used to select the appropriate resistance for the selected multiplier.
- V_{biasp} and V_{biasn} will be generated by the general biasing circuit. These bias voltages will result in an I_{pump} of 10 µA.

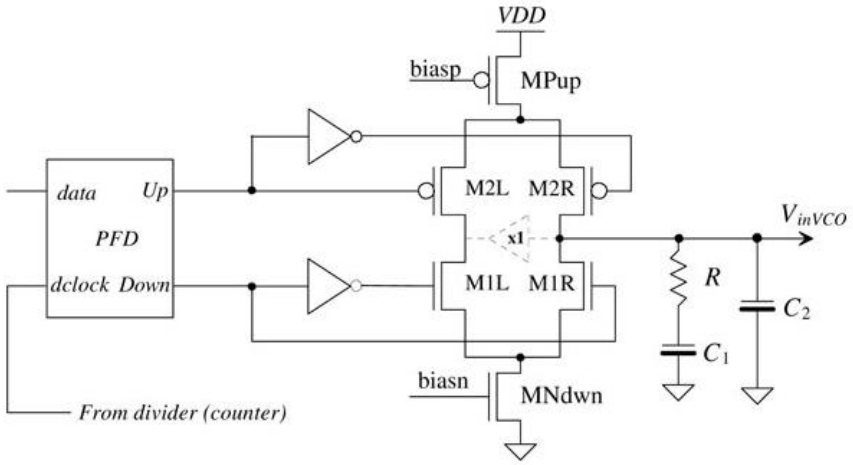
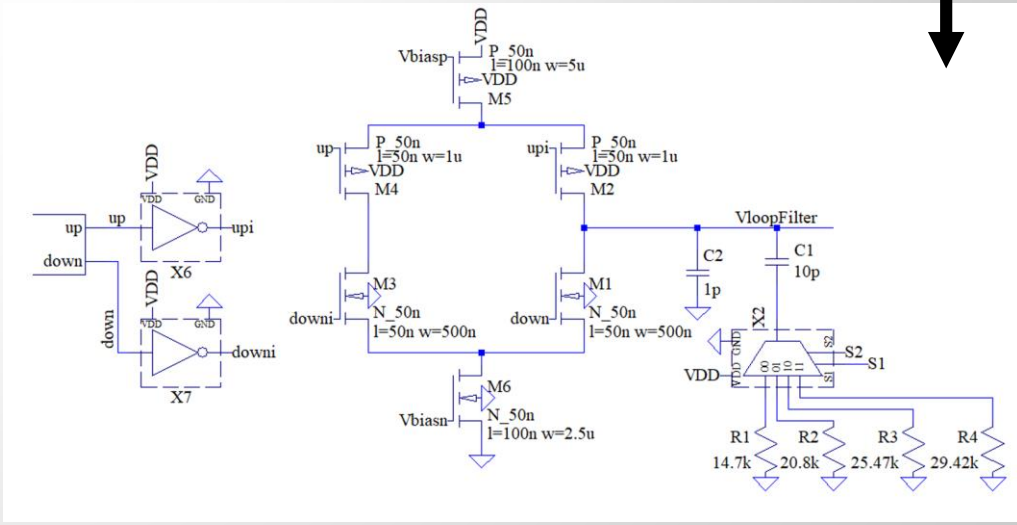


Figure 19.37 Practical implementation of the charge pump.



PFD CHARGE PUMP OUTPUT II: CALCULATING RESISTANCE VALUES FOR EACH MULTIPLIER

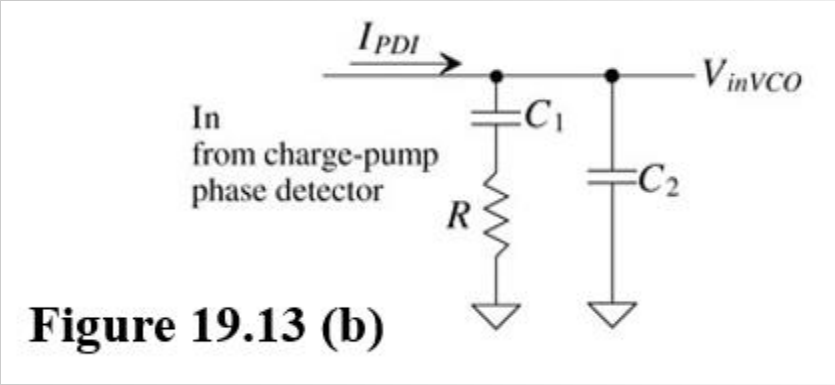


Figure 19.13 (b)

Equation 19.56-19.58 in Dr. Baker's CMOS book are:

Feedback Loop Transfer Function:

$$H(s) = \frac{\emptyset_{clock}}{\emptyset_{data}} = \frac{K_{PDI}K_{VCO}(1+sRC_1)/C_1}{s^2+s\left(\frac{K_{PDI}K_{VCO}R}{N}\right)+\frac{K_{PDI}K_{VCO}}{NC_1}}$$

Natural Frequency:

$$\omega_n = \sqrt{\frac{K_{PDI}K_{VCO}}{NC_1}}$$

Damping Factor:

$$\zeta = \frac{\omega_n}{2} RC_1$$

Therefore the following can be said:

$$\zeta = \frac{RC_1}{2\sqrt{N}} \cdot \sqrt{\frac{K_{PDI}K_{VCO}}{NC_1}}$$

Solving for R:

$$R = \frac{2\xi}{\underbrace{C_1\sqrt{\frac{K_{PDI}K_{VCO}}{C_1}}}_{z}} \cdot \sqrt{N} = Z\sqrt{N}$$

Substituting:

$$\zeta = 1$$
$$C_1 = 10\ pF$$
$$K_{PDI} = \frac{I_{pump}}{2\pi} = \frac{5\ \mu}{\pi}$$
$$K_{VCO} = 2.33\ G\ {}^{radians}/_{V \cdot S}$$

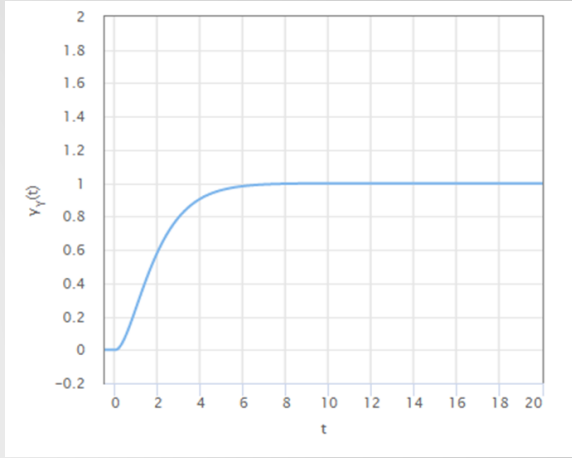
Therefore:

$$Z = \frac{2}{10\ p\sqrt{\frac{\frac{5\ \mu}{\pi} \cdot 2.33\ G}{10\ p}}} \approx 10.4\ k \rightarrow \therefore R(N) = 10.4k\sqrt{N}$$

Now we may calculate the associated R in the loop filter for each multiplier (i.e. 2, 4, 6, & 8).

$$\boldsymbol{R(2) = 14.70\ k\Omega}$$
$$\boldsymbol{R(4) = 20.80\ k\Omega}$$
$$\boldsymbol{R(6) = 25.47\ k\Omega}$$
$$\boldsymbol{R(8) = 29.42\ k\Omega}$$

This will ensure that for each multiplier, the damping factor will be 1 for all possible multipliers.



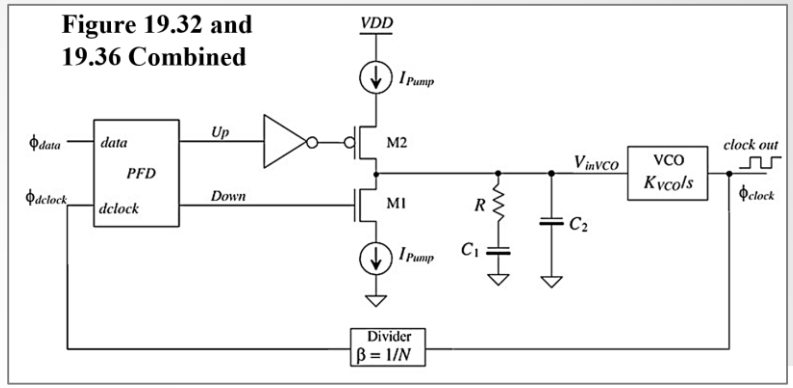
Unit Step Response of Second Order System with ζ=1

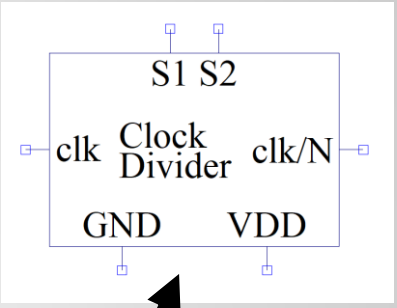
VARIABLE CLOCK DIVIDER

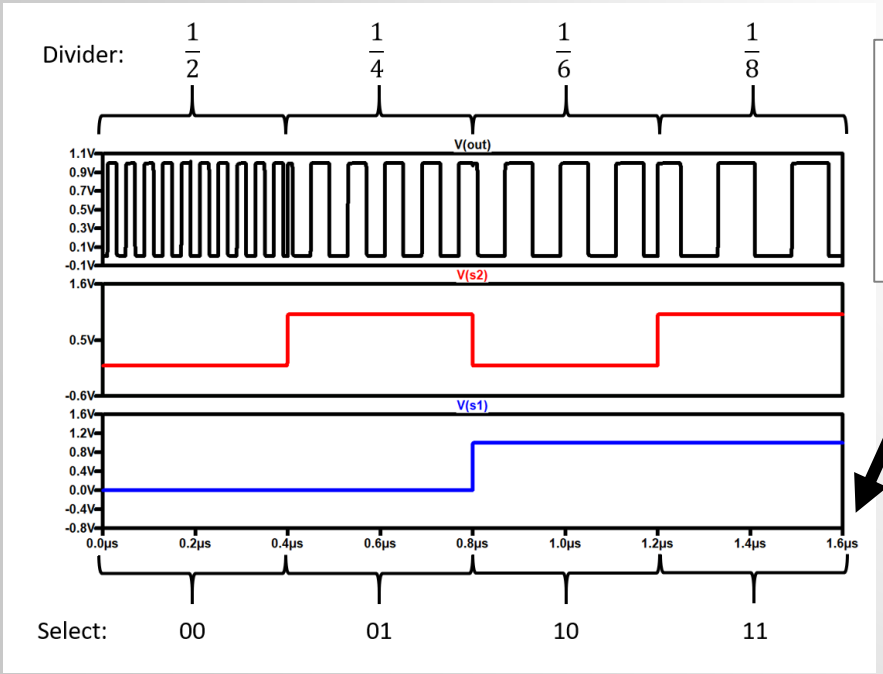
- Consider the PFD DPLL, a feedback loop forces *data* and *dclock* to be the same frequency. The following statements can be asserted:

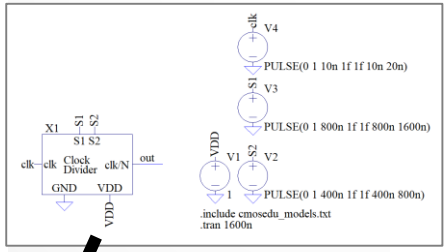
$$data = dclock$$
$$\frac{1}{N} clock = dclock$$
$$clock = N \times dclock$$
$$\therefore \boldsymbol{clock = N \times data}$$

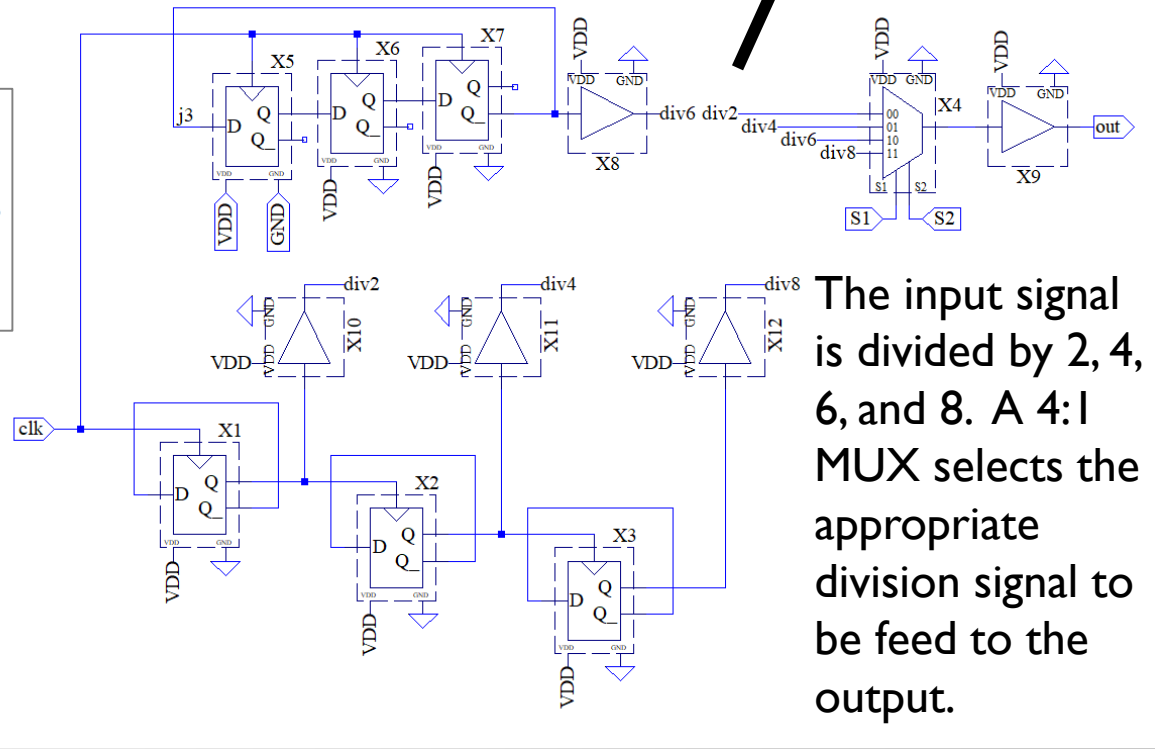
- The multiplier is equivalent to the N value. For example, to get a X6 clock multiplier, you must divide the clock signal by 6.











The input signal is divided by 2, 4, 6, and 8. A 4:1 MUX selects the appropriate division signal to be feed to the output.

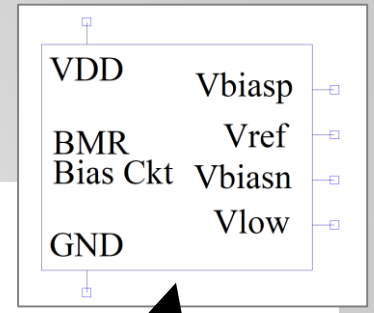
BIAS CIRCUIT

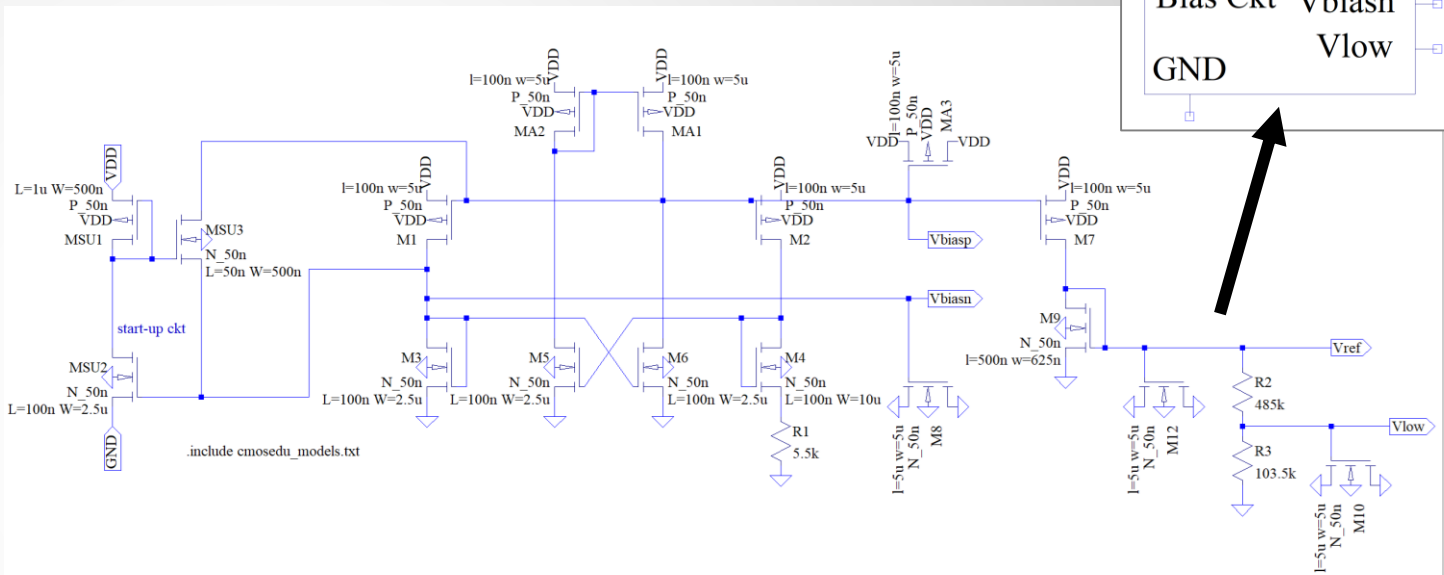
- A biasing circuit that generates voltage references independent of supply voltage and temperature.
- Made possible by implementing a Beta Multiplier Reference (BMR).
- MOSCAPs are used as decoupling capacitors.

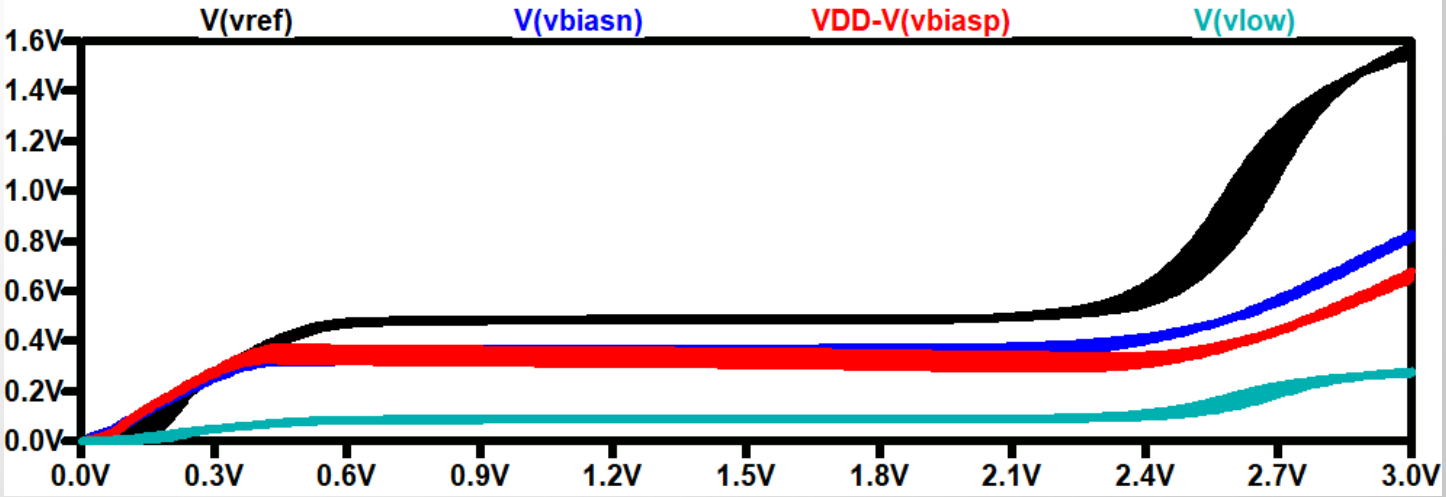
The following voltage are generated:

Voltage	Value (V)
VDD-Vbiasp	350 mV
Vref	500 mV
Vbiasn	85 mV
Vlow	350 mV

The simulation steps temperature from 0-100° C.

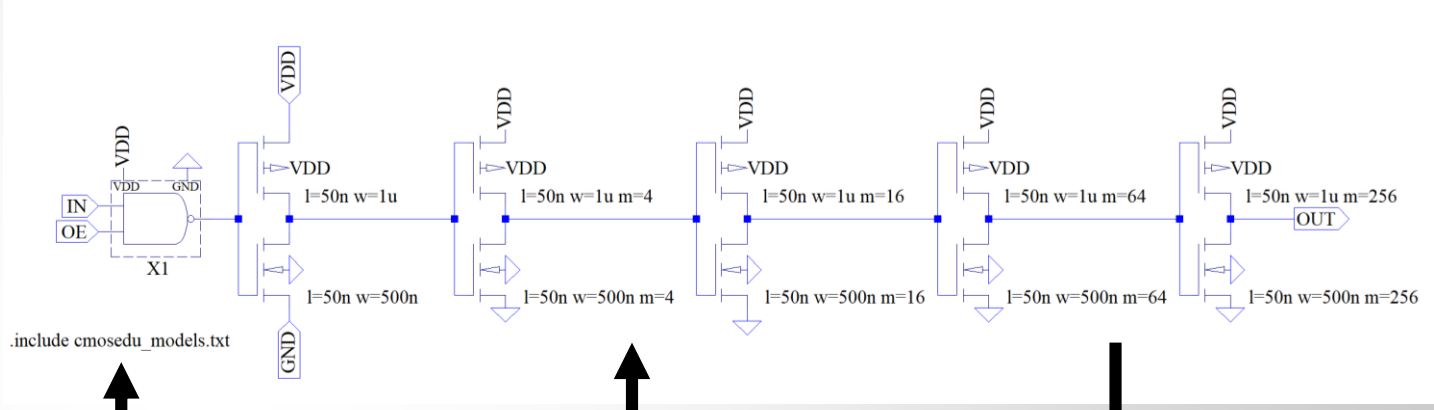


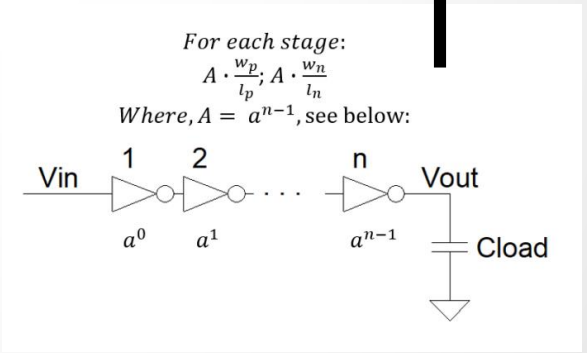


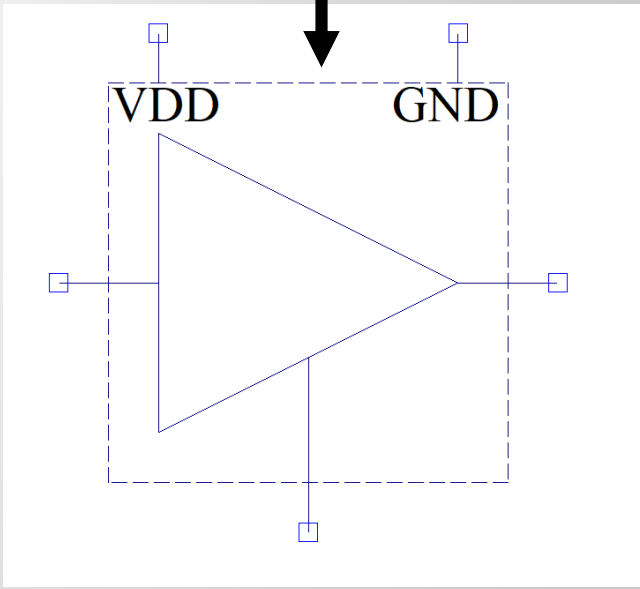


OUTPUT BUFFER

- An output buffer is required to drive off-chip loads
- To follow the template of the NB3N511 Clock Multiplier, an output enable is included
- To achieve, output enable functionality a NAND gate is used as an *enabled inverter*.
- When OE is high, the signal passes through to the output. Otherwise, the signal does not pass through.

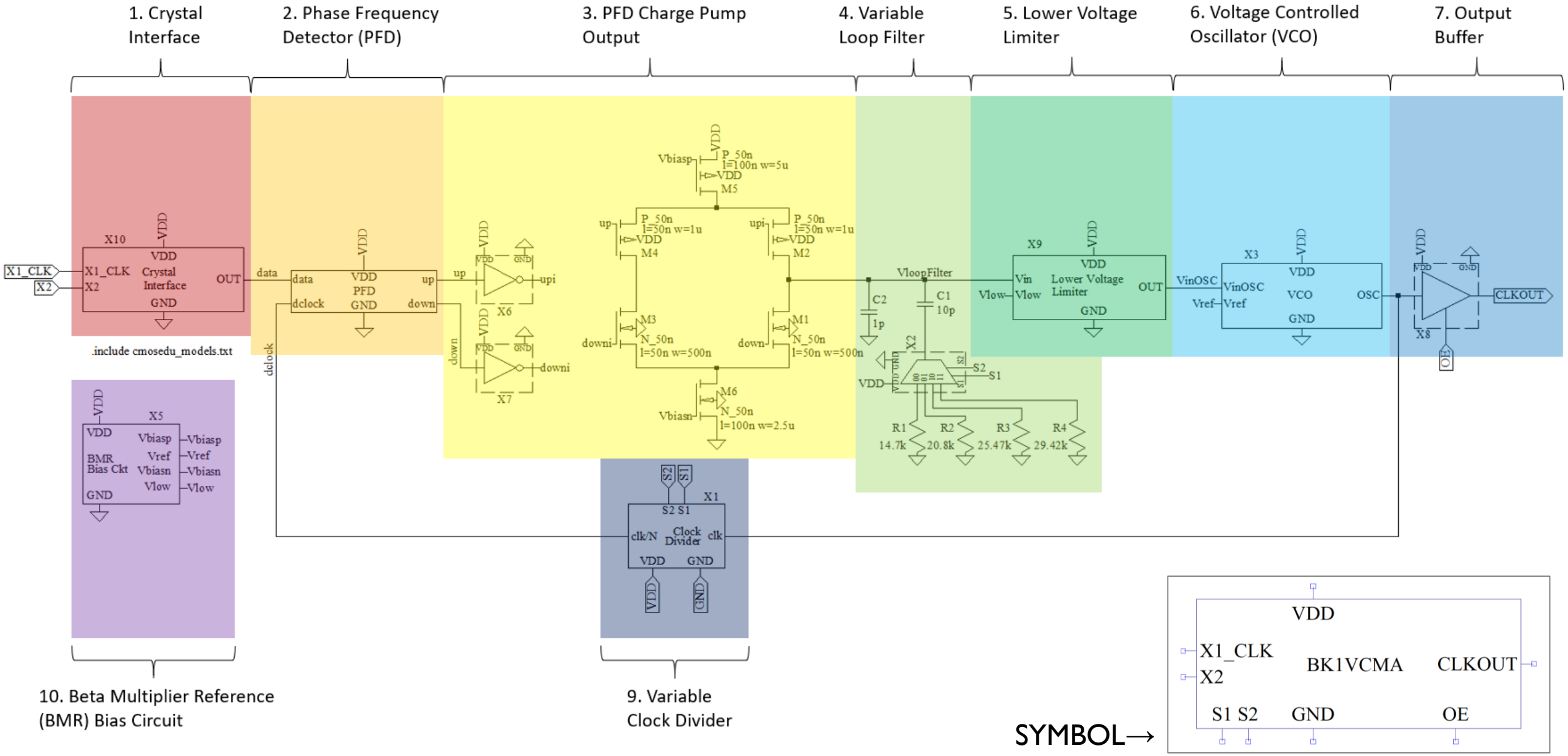




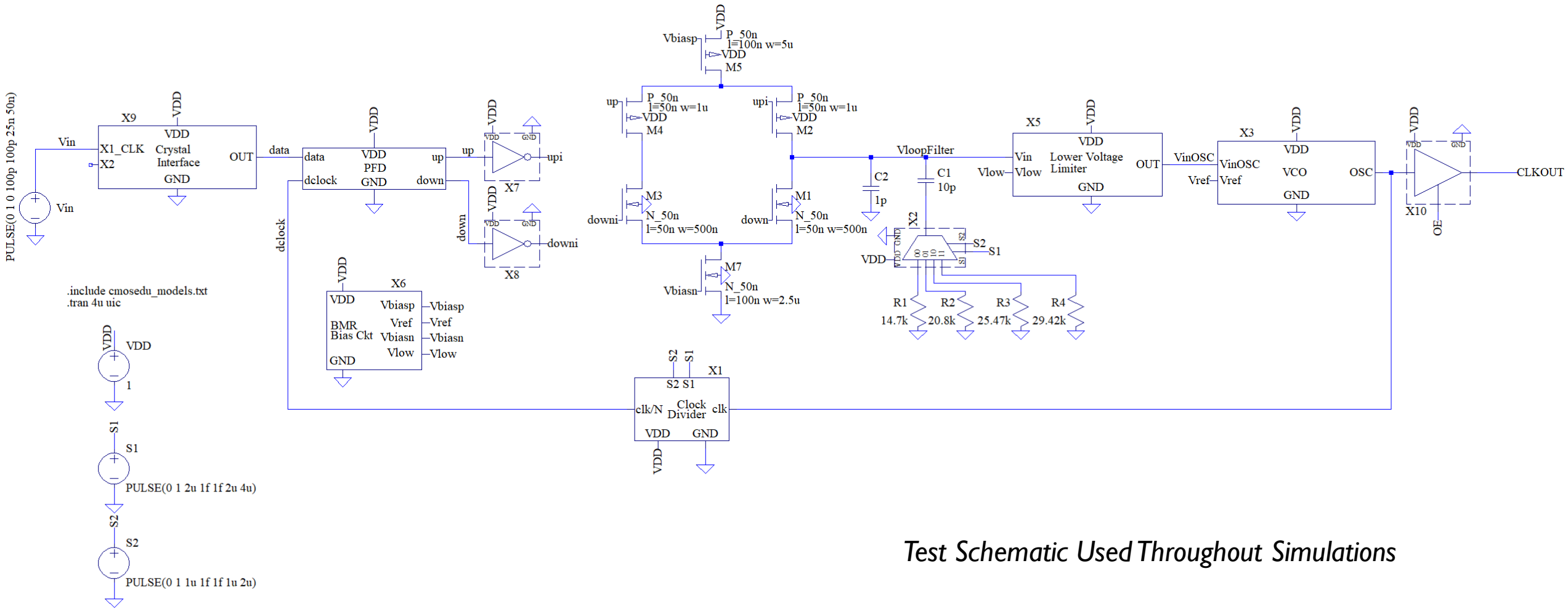


enable	*clk*	*ENABLEnandCLK =OSC*
0	0	1
0	1	1
1	0	1
1	1	0

THE COMPLETE BK1VCMA CIRCUIT



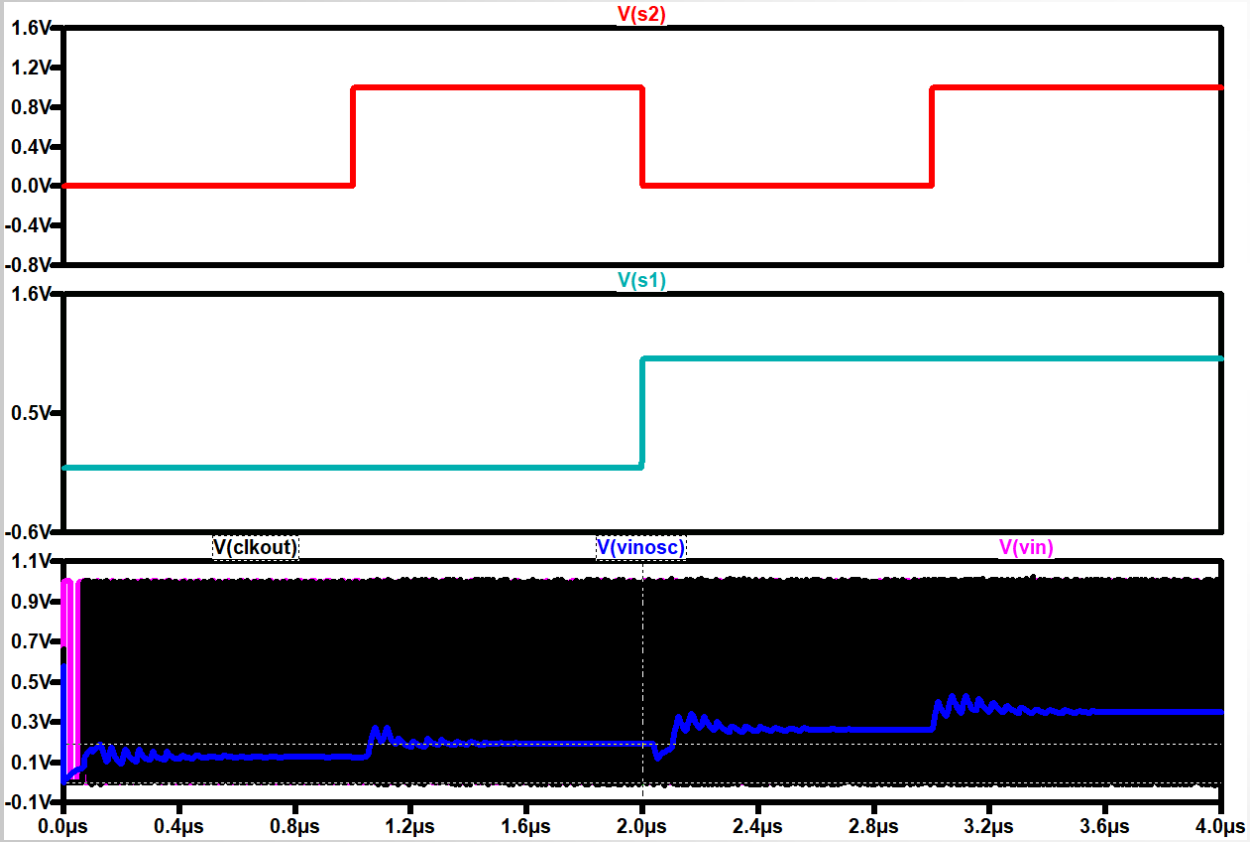
BK1VCMA SIMULATION: INPUT CLOCK TEST A1



Test Schematic Used Throughout Simulations

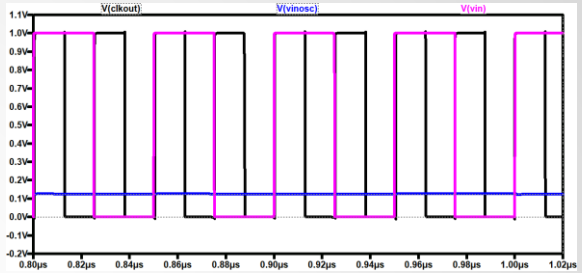
BK1VCMA SIMULATION: INPUT CLOCK TEST A II

Input Frequency: 20MHz
VDD = 1V



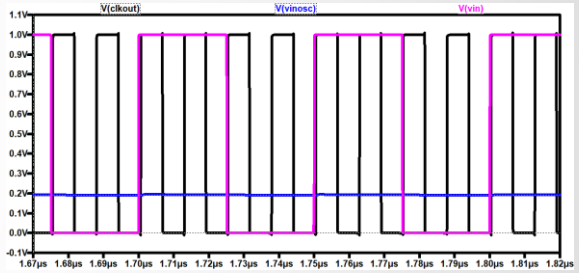
Notice: The damping factor is satisfactory for all multipliers.

X2



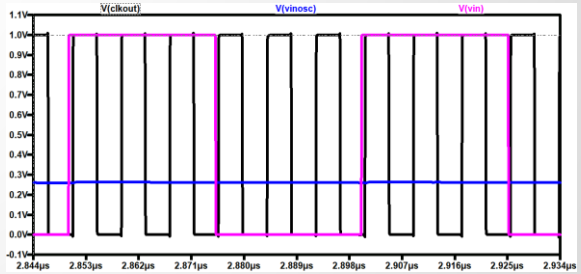
Frequency: 40MHz

X4



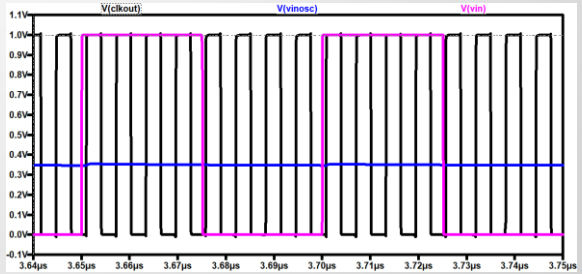
Frequency: 80MHz

X6



Frequency: 120MHz

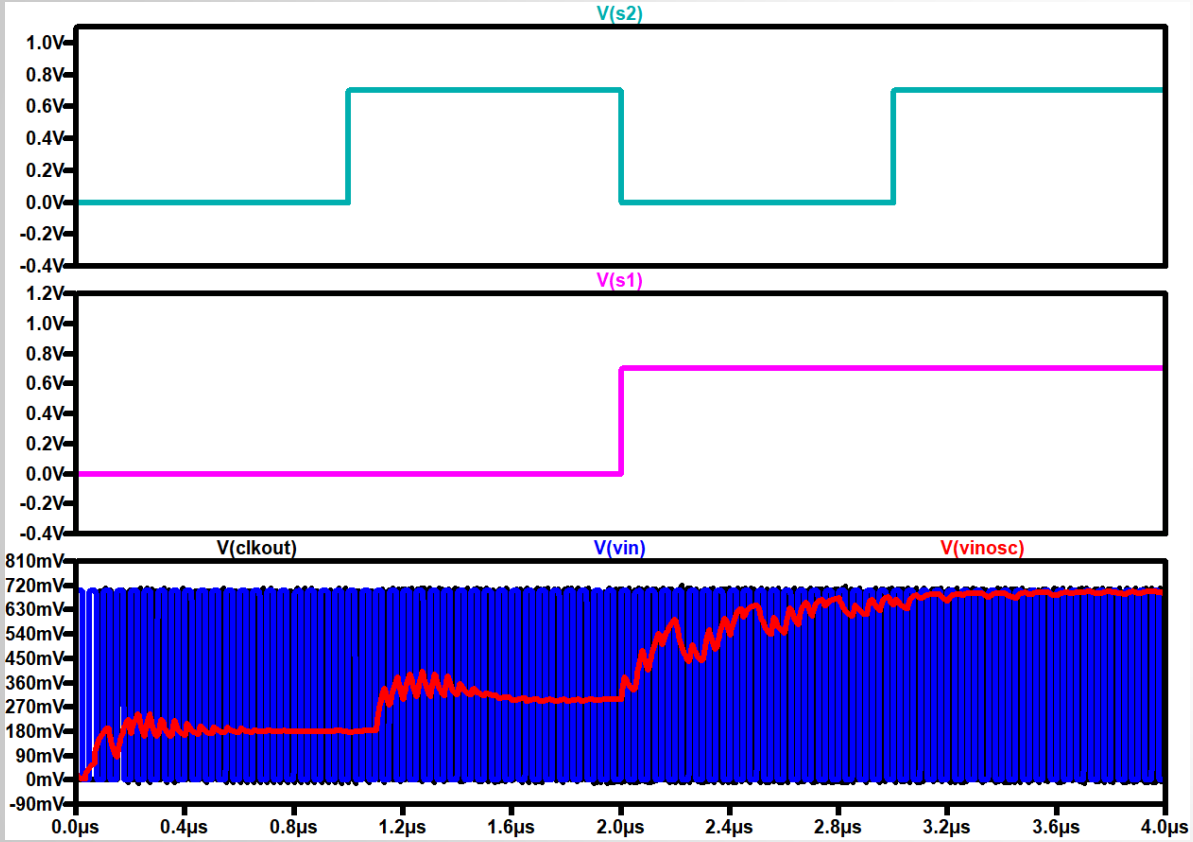
X8



Frequency: 160MHz

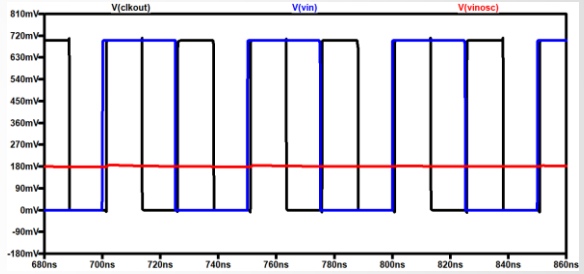
BK1VCMA SIMULATION: INPUT CLOCK TEST & LOW VDD

Input Frequency: 20MHz
VDD: 0.7V



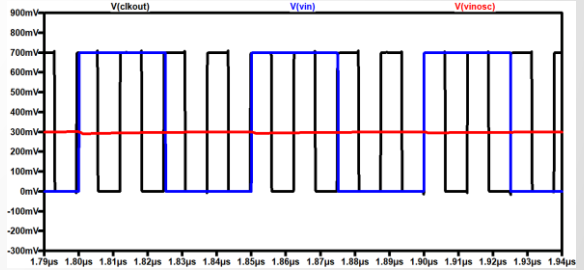
Notice: Due to the low VDD, the output did not lock for X6 and X8.

X2



Frequency: 40MHz

X4



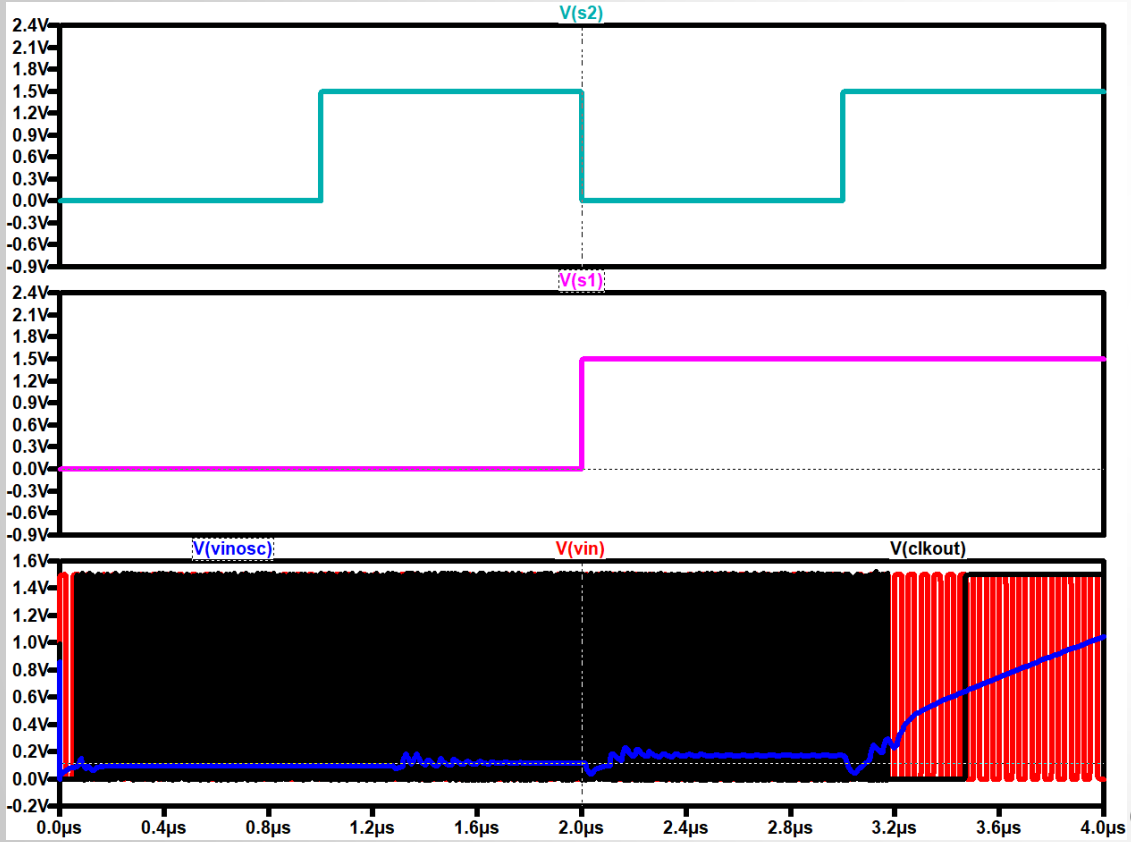
Frequency: 80MHz

Conclusion: Under certain circumstances the BK1VCMA can operate properly with considerably low supply voltages.

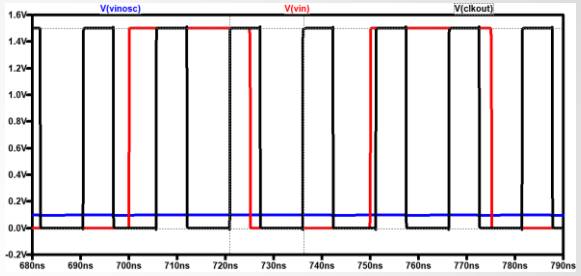
Lowering the supply voltage, reduces the frequency range of the output signal.

BK1VCMA SIMULATION: INPUT CLOCK TEST & HIGH VDD

Input Frequency: 20MHz
VDD: 1.5V

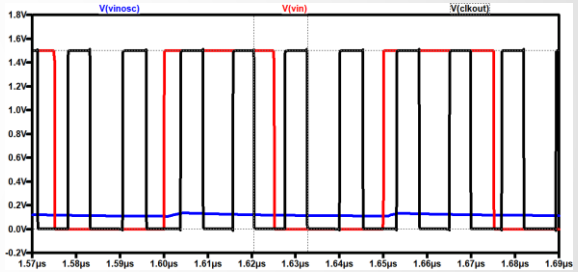


X2



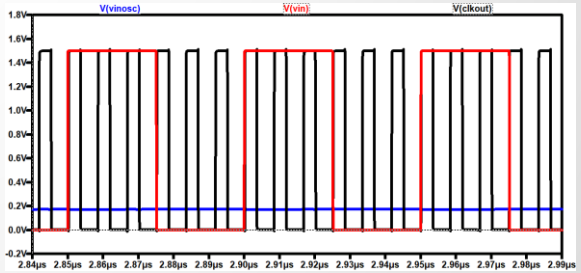
Frequency: 65MHz
Some distortion

X4



Frequency: 80MHz

X6



Frequency: 120MHz

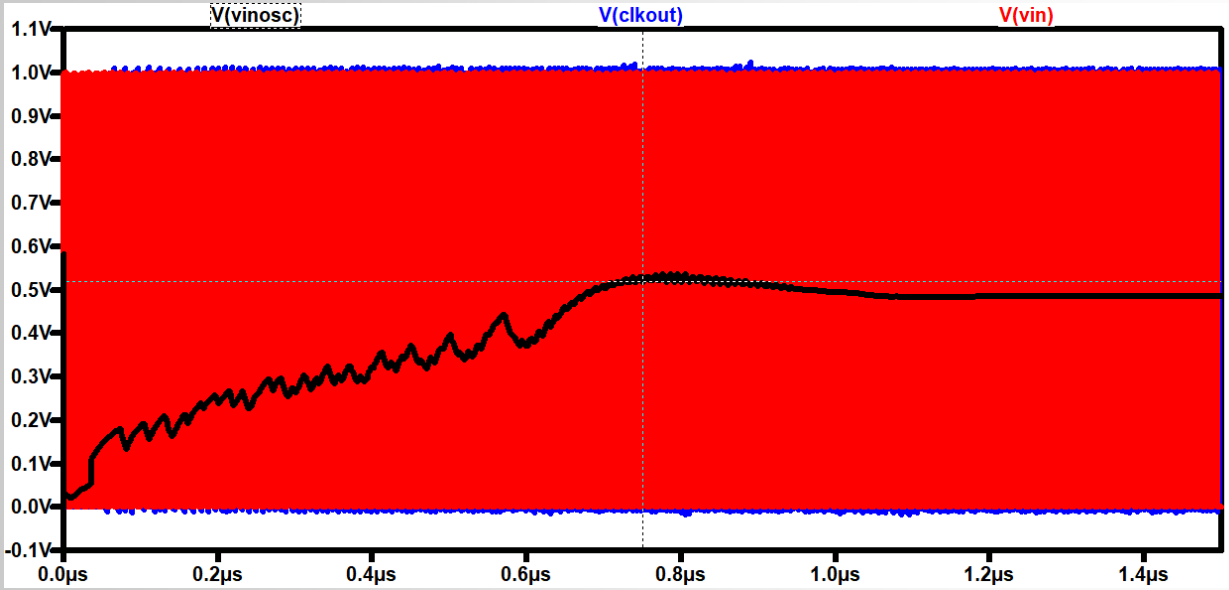
Notice: Due to the high VDD, the output did not lock for X8.

Conclusion: Under certain circumstances the BK1VCMA can operate properly with considerably high supply voltages.

Possible Solution: Create a higher voltage limiter so VinOSC never goes above 1V (similar to the lower voltage limiter).

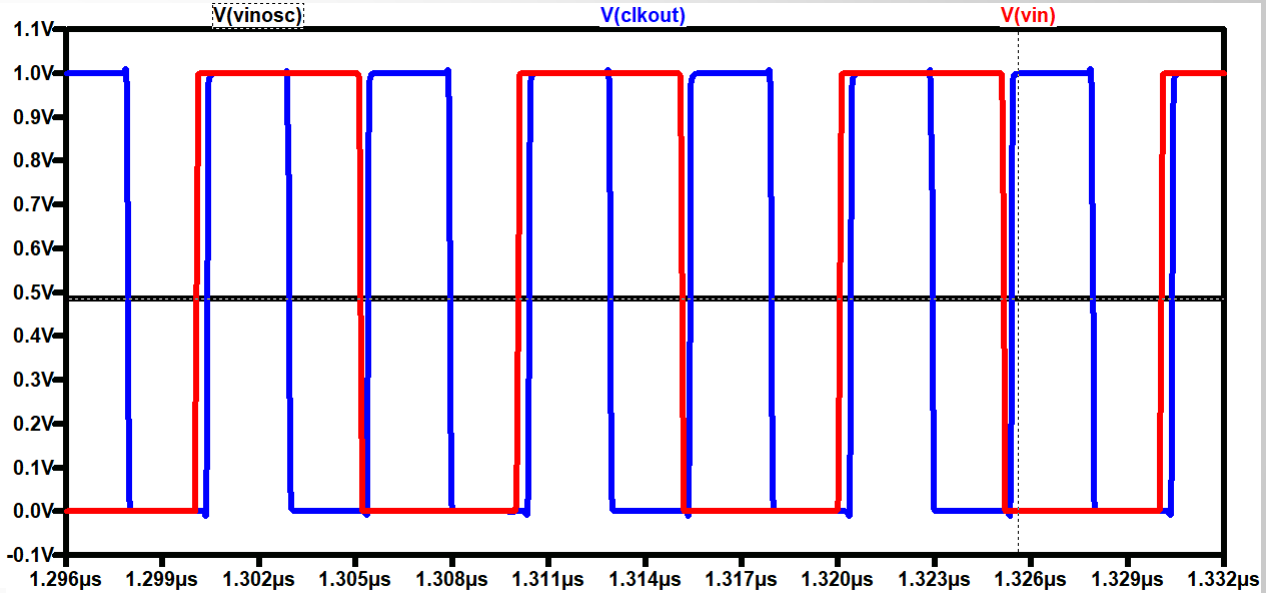
BK1VCMA SIMULATION: INPUT CLOCK TEST B

Input Frequency: 100MHz
VDD = 1V



Notice: The system locks after 1µs. The damping factor is satisfactory.

Multiplier: X2



Frequency: 200MHz

The multiplier of X2 is the only compatible multiplier for an input frequency of 100MHz.

CONCLUSION

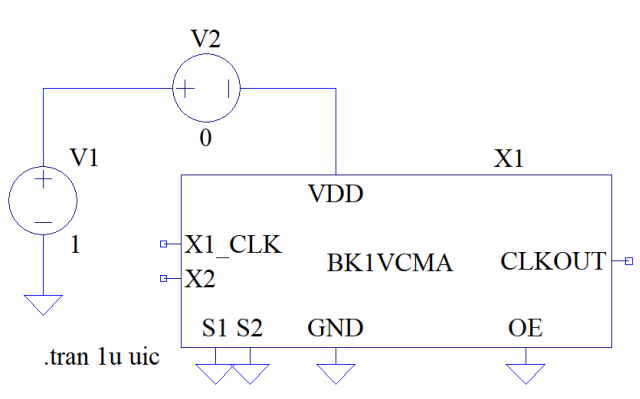
The BK1VCMA Variable DPLL Clock Multiplier design proved to be successful. All of the original goals were achieved:

- Accommodates a wide range of input frequencies
- Programmable multiplier
- Guarantees a 45%-55% output duty cycle
- Two possible input signal methods
  - Crystal Reference
  - Input Clock Frequency

FUTURE WORK

- Further improve crystal interface
- Add high voltage limiter for VinOSC
- Increase output frequency range
- Further linearize VCO response
- Remake clock multiplier in a process that can be laid out

Circuit used to measure average power draw under quiescent conditions.



SUMMARY OF RESULTS

Conservative Values

Multiplier	Input Frequency Range (MHz)
X2	10-100
X4	10-50
X6	10-33.33
X8	10-25

Metric	Value
Average Power Draw *(Quiescent Conditions)*	2.0311 mW
Output Frequency	~20-200 MHz

The supply voltage is able to vary. However, the best results occur at VDD = 1V.

REFERENCES

This presentation extensively references the fourth edition of Dr. R. Jacob Baker's CMOS: Circuit Design, Layout, and Simulation. Figures and equations are also from this book. View information about this book at:

- http://cmosedu.com/cmos1/book.htm

Other:

1. CMOS 4x Clock Multiplier by Bryan Kerstetter:
   - http://cmosedu.com/jbaker/courses/ee421L/f19/students/kerstett/project/project.htm
2. CMOS Ring Oscillator Using Stacking Techniques to Reduce Power Dissipation and Leakage Current by Vikas Sah:
   - https://www.slideshare.net/VikasSah3/vikas-77047966
3. Modelling Quartz Crystals by Pspice:
   - https://www.pspice.com/resources/application-notes/modelling-quartz-crystals
4. NB3N511 3.3V / 5.0V 4 MHz to 200 MHz PLL Clock Multiplier by ON Semiconductor Datasheet:
   - https://www.onsemi.com/pub/Collateral/NB3N511-D.PDF
5. Quartz Crystal Oscillator by Electronics Tutorials:
   - https://www.electronics-tutorials.ws/oscillator/crystal.html

QUESTIONS?