Design, Layout, and Simulation of a CMOS Boost Switching Power Supply

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***Abstract* – This document covers the design of a CMOS Boost Switching Power Supply (SPS). This boost SPS operates by taking in an input range of 3.75 to 4.75 V, and outputting a steady 5 V. The SPS will make use of an off-chip inductor, capacitor, and diode to supply this output voltage, and will be able to provide up to a 50 mA load.**

I. INTRODUCTION

A boost SPS operates by taking in a range of input voltages and outputting a steady voltage that is higher than its input at the cost of a lower output current compared to input current. These types of devices are typically highly efficient, and can be found in applications such as lighting systems and hybrid vehicles.

II. COMPONENTS

The main components of this design are a bandgap, comparator, ring oscillator, buffer, NMOS switch, voltage divider, as well as off-chip inductor, capacitor, and diode.

a. Bandgap

The bandgap is used to provide a constant voltage reference at varying temperatures and input voltages. In the case of this pre-designed bandgap, a voltage **reference of 1.25 V** is achieved. This voltage will be used as the reference for the comparator used later in this design, and is to be compared against the output of the design. Therefore, it is important to maintain a constant reference as it will be used to turn off the later explained switching frequency, which will help determine the final circuit's output voltage. The layout of the bandgap was prepared for this design, and is shown in Fig 1.

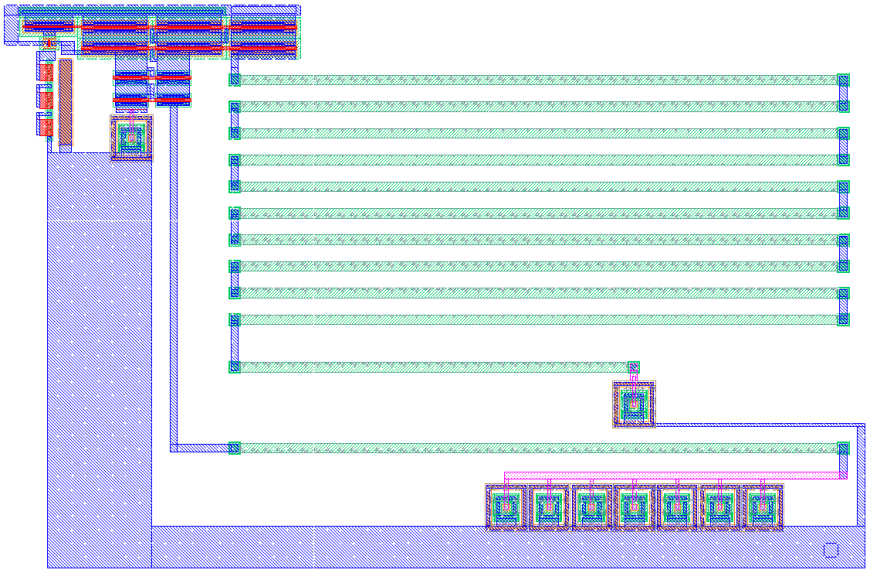

Fig 1. Bandgap Layout

The 1.25 V reference varies very little with different input voltages and extreme temperatures. Simulations of the bandgap show the output reference remains relatively constant so long as the voltage source is **above 3.7 V**. Furthermore, it is shown that current will steadily rise with an increasing voltage source. These results are shown in Fig 2.

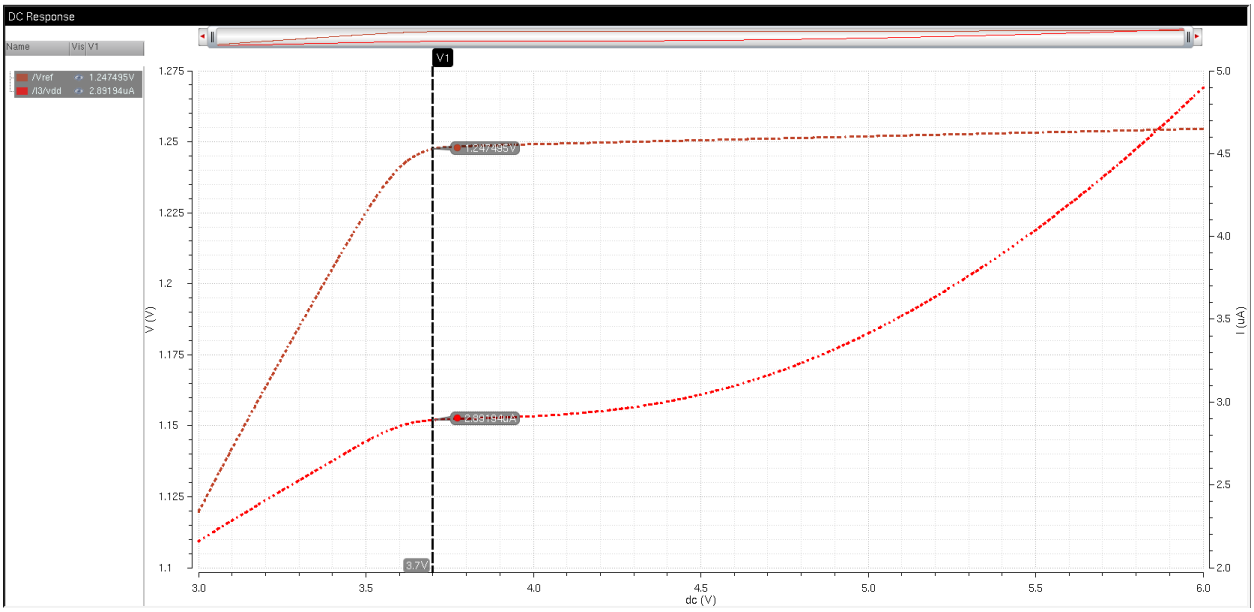

Fig 2. Bandgap with Increasing Source Voltage

Further simulations show little variations across large temperature differences, with the output ranging from **1.253 V at 0 °C and 1.245 at 100 °C**, showing an overall trend of voltage dropping off with temperature, to a small degree. These results are shown in Fig 3.

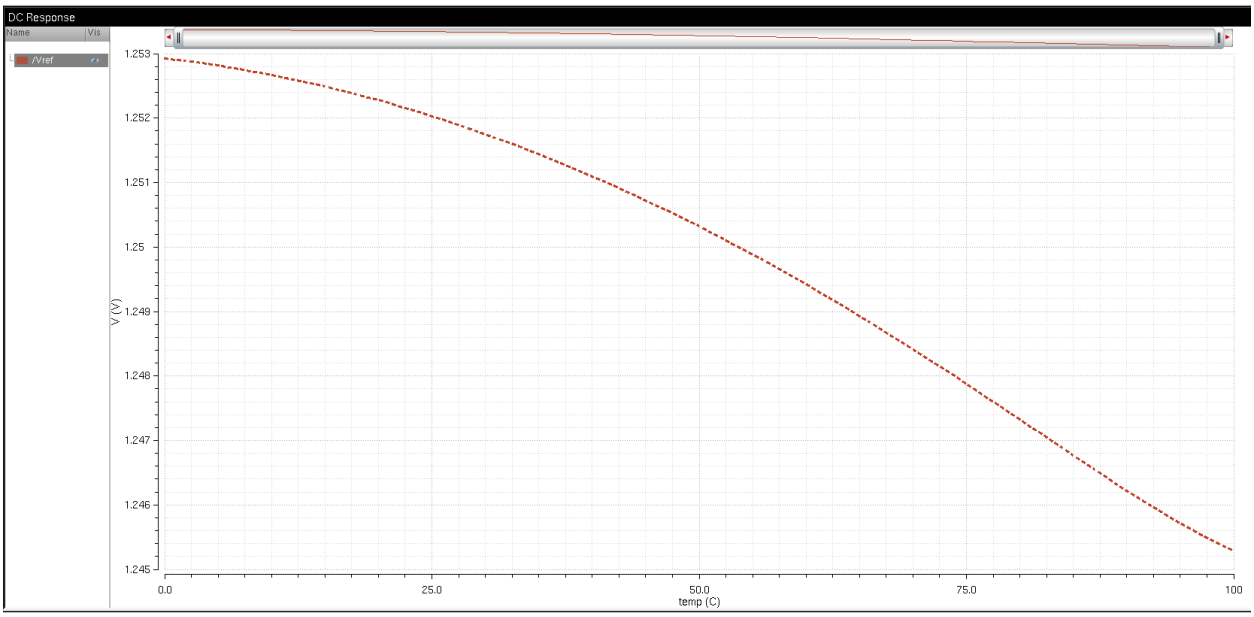

Fig 3. Bandgap with Increasing Temperature

b. Comparator

While under a load and not in operation, the output of the boost SPS will begin to drop below its nominal voltage, in this case, 5 V. However, the circuit cannot simply be set to always operate as, if the circuit is designed to output a voltage of exactly the nominal voltage, it will not be able to provide for any considerable load, and if designed for a higher voltage, it will simply overshoot the nominal voltage. Because this circuit operates in the second condition, that is, designed to output a voltage higher than the nominal voltage, an additional device must be used to sense the output of the final circuit, and control the operation of the device. The device is to be turned on when the output falls below 5 V, and the device is to be turned off when the output rises above 5 V. Accomplishing this, will be the job of the comparator.

The comparator operates through the use of three differential amplifiers (shown in Fig 4). Connected to the positive terminal is the voltage reference, supplied from the bandgap. Connected to the negative terminal is the final output divided by 4. The differential amplifiers magnify the difference between the reference voltage and output feedback. Each amplifier magnifies the output of the previous, thus providing a larger gain with each diff amp. This larger gain translates to a more sensitive circuit, which is needed to ensure delay is somewhat minimized between output falling below or above nominal voltage, and comparator toggling the circuit on or off, respectively.

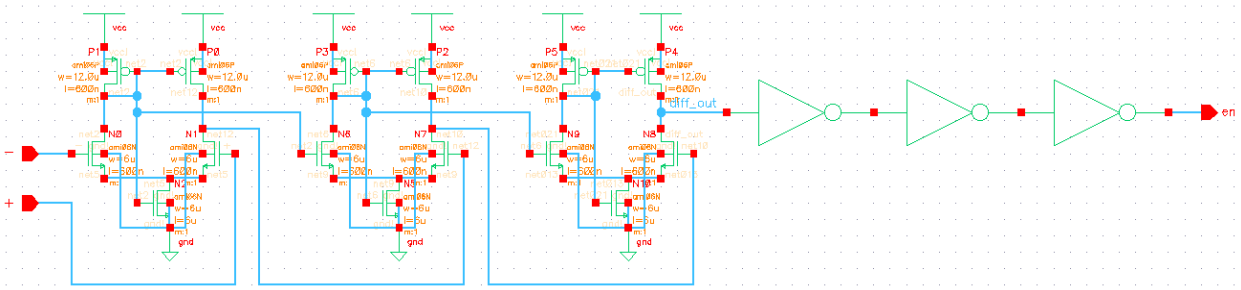

Fig 4. Comparator Composed of 3 Differential Amplifiers (left) and 3 Inverters (right)

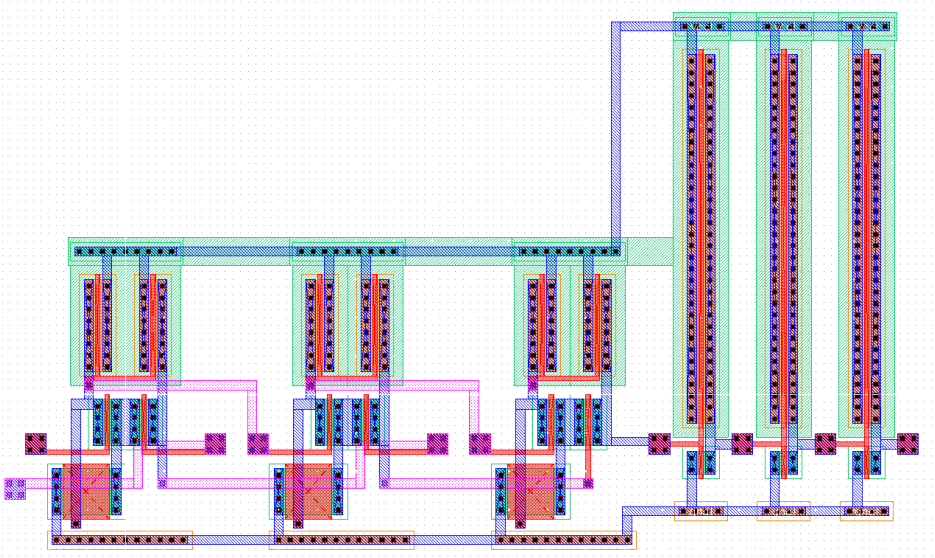

Fig 5. Layout of Comparator

Due to the in-series differential amplifiers, the output of this stage is a signal that **swings from 1.5 to 3.75 V** (see Fig 8). To ensure delay is controlled, and that enable is switching in the middle of this swing, a few buffers are first necessary with modified switching points. Because diff_out swings closer towards the voltage source, the buffers should be designed with a switching point that is close to the voltage source themselves. Going for a switching point of about 3.3 V should ensure that the enable signal is properly conditioned for output. The switching point of each inverter can be estimated with the following:

$$VSP = VDD * Rn/(Rn + Rp)$$

Solving for *VSP* equal to 3.3 V, and *VDD* equal to 3.75 V, the following relationship is found:

$$\frac{Rn}{Rn + Rp} = 0.8$$

An *Rn* and *Rp* of **4k Ohms and 500 Ohms** are selected, respectively. This indicates a PMOS with a width of 80 and an NMOS with width 5. The resulting inverter is shown in Fig 6.

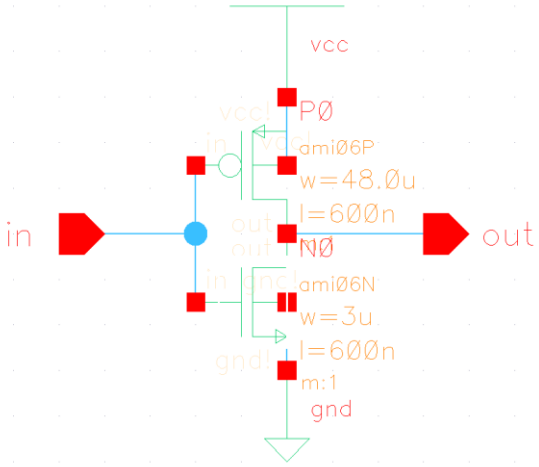

Fig 6. Inverter of Size 5/80

Of course the method used to estimate the switching point of the inverter is just that, an estimate. It is not ideal for finding an exact switching point, however, it does push the switching point of the voltage within an acceptable distance towards 3.75 V. Simulations shown in Fig 7 reveal a **switching point of 2.5 V**, putting the switching point almost exactly in the middle of the diff_out swing.

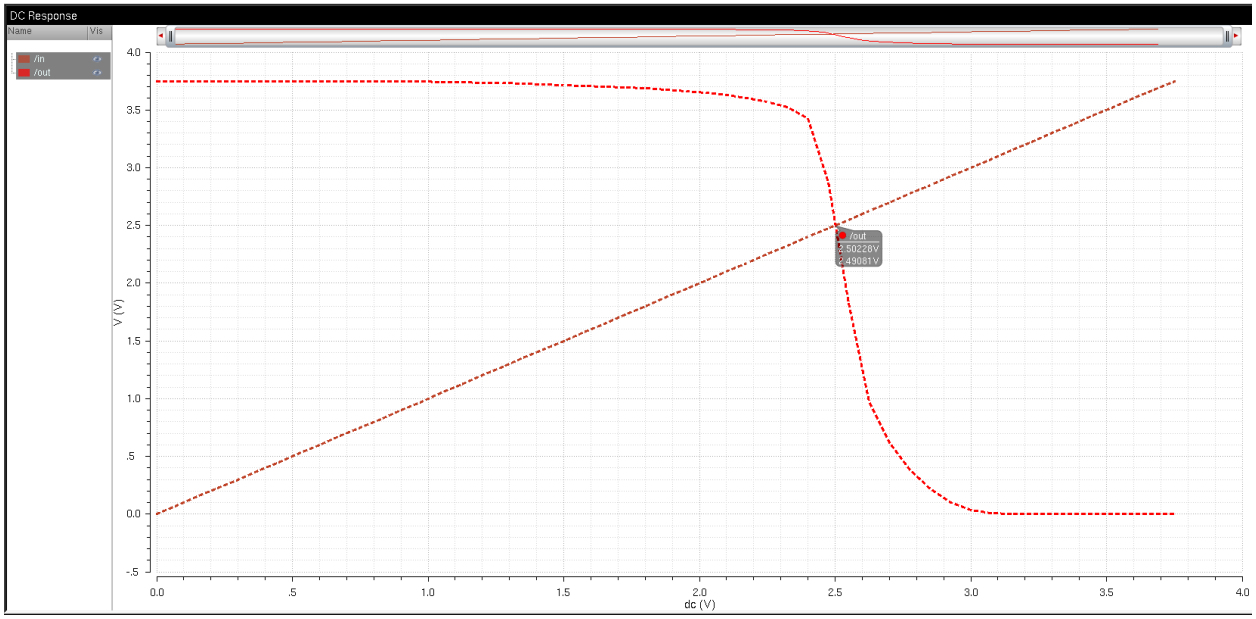

Fig 7. Inverter's Modified Switching Point

With the switching point established, a couple more inverters are added to square up the signal for final output. Because it is desirable for enable to be high when the feedback signal falls below the reference signal, an odd number of inverters are used to buffer the comparator's output.

A full simulation of the comparator is shown below (Fig 8). Enable is controlled by the feedback signal going below or above the reference voltage of 1.25 V, however, enable is **delayed by about 10 ns**. This is due to delay through the comparator as well as buffers, and will actually be useful for hysteresis purposes explained later.

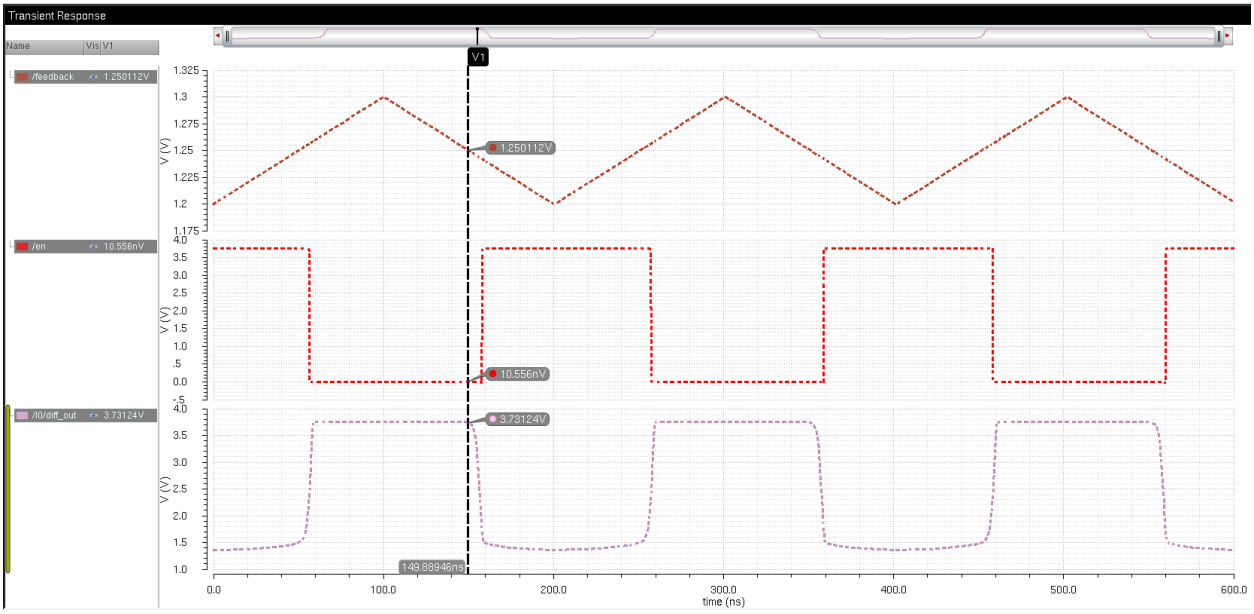

Fig 8. Simulation of Comparator

c. Ring Oscillator

The ring oscillator provides the clock which will generate a switching frequency. A boost SPS operates by continuously diverting built-up current in the off-chip inductor into a capacitor and this is accomplished by continuously switching one of the nodes of the inductor to ground. More on this process will be explained later, however, it is important to know that a clock signal will be necessary to generate this switching frequency. The schematic and layout for the clock are shown in Fig 9 and Fig 10, respectively.

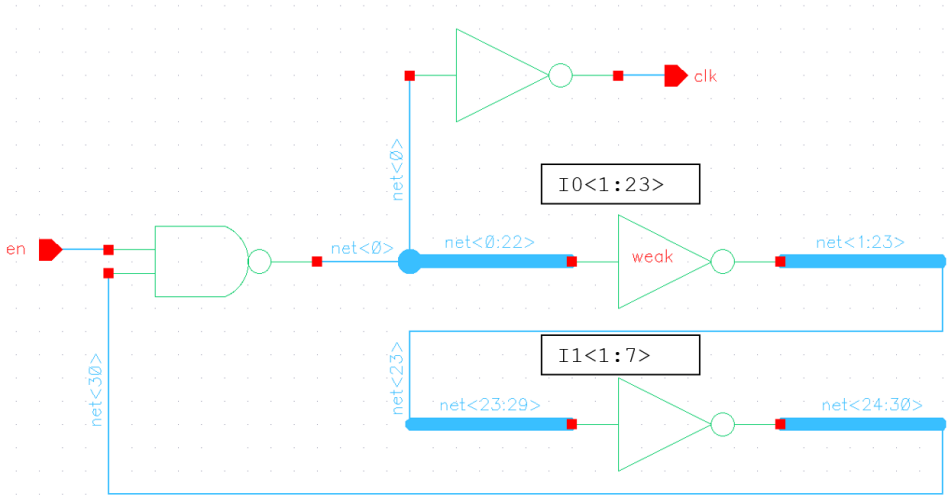

Fig 9. Ring Oscillator Schematic

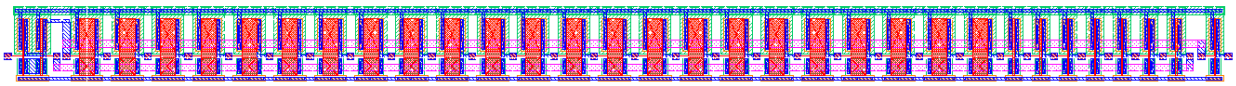

Fig 10. Ring Oscillator Layout

The clock is generated by a series of inverters to form a ring. An AND gate is used to enable the clock. Driven by the comparator, when the enable signal is high, the AND gate acts as an inverter for its second input, which is the feedback of the ring network. As there are an odd number of inverters, when a signal propagates through the network, upon reaching the beginning of the ring, it will arrive with opposite logic, and cause oscillation.

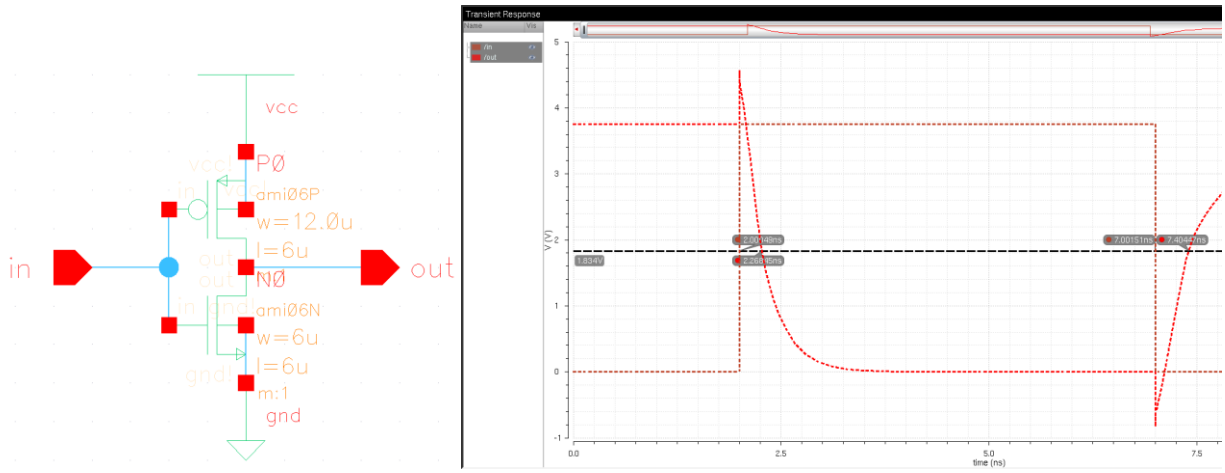

Fig 11. Weaker Inverter (Longer L) Used for Longer Delay (.266 ns)

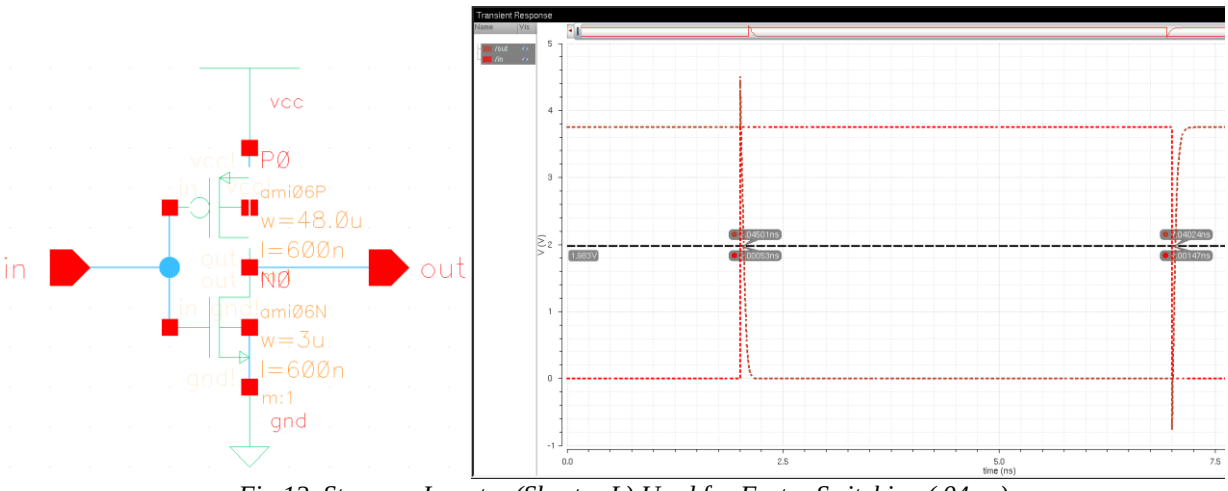

Fig 12. Stronger Inverter (Shorter L) Used for Faster Switching (.04 ns)

The frequency of the clock is determined by the number of inverters, as well as their individual delays. To limit the size of the layout, a combination of strong and weak inverters were used. The weak inverters (Fig 11) have a higher delay than the strong inverters (Fig 12), and thus by using less of them we can reach a more desirable clock frequency using a smaller layout. As a drawback to their favorable delay, however, they do not produce a quick enough change in output, thus losing out on the sharp edges expected of a clock signal. To correct this, output is taken after the series

of strong inverters, which square the wave and produces the desired output. As a final design choice, the output is tapped immediately after the AND gate, which minimizes the time that the clock output takes to turn on after the clock is enabled. Output must also be inverted here to ensure clock is grounded when enable is low. Simulation of the clock is shown in Fig 13.

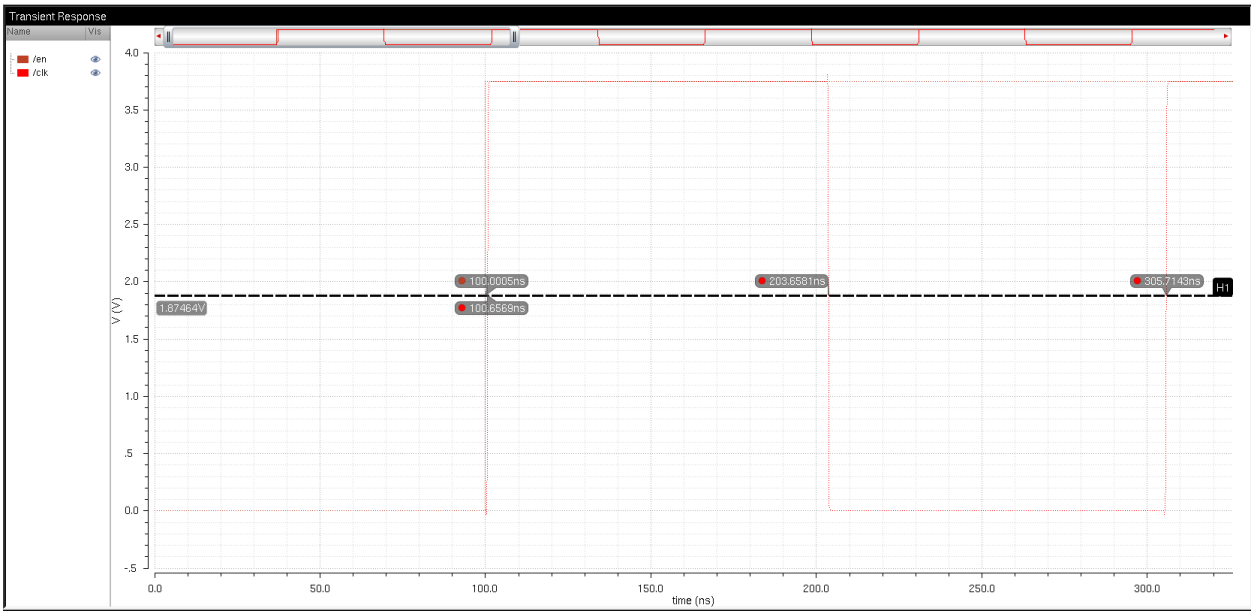

Fig 13. Simulation of Enabled Clock

The measured clock period is about 205 ns for a frequency of **4.8 MHz**. Additionally, the duty cycle, D, of the clock period, that is the time the signal is held high relative to the period, is approximately .5. Both of these values will be used in sizing later off-chip components, as well as determining the output voltage of the circuit. This output is calculated using the follow equation:

$$Vout = \frac{Vsource}{1 - D}$$

As our source voltage varies between 3.75 and 4.75 V, the output voltage can vary between 7.5 and 9.5 V (of course the circuit will turn off before either of these values are reached). Therefore, a duty cycle of .5 is more than enough to reach the desired nominal voltage of 5 V.

d. Buffer

The clock signal directly from the oscillator is a product of relatively small transistors, and is not strong enough to drive the large NMOS that'll be used later for switching. To drive the actual switch, the signal must first be strengthened though increasingly larger inverters. As seen in the schematic shown in Fig 14, the size of each inverter is twice that the size of the previous one, maintaining a ratio close to the ideal, *e*. The schematic of the buffer is shown below (Fig 14).

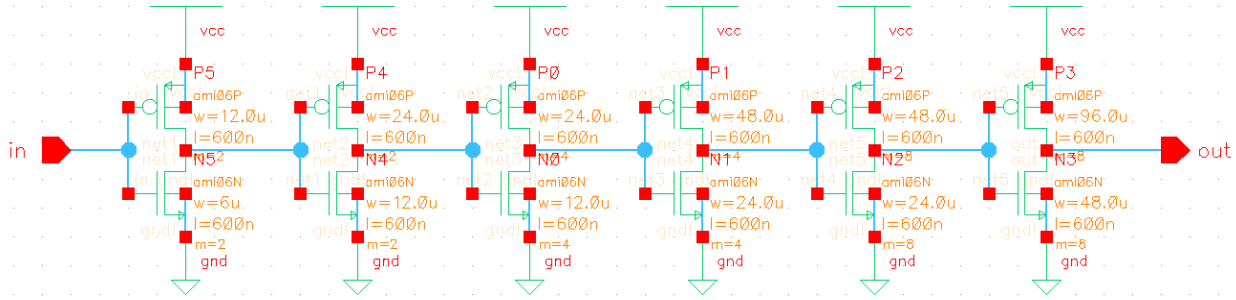

Fig 14. Buffer Schematic

To maintain the polarity of the signal through the buffer, an even number of inverters is required. Here 3 sets of inverters were chosen to smoothly transition from the original clock signal to the final output. Additionally, this is the minimum number of inverters maintaining that ideal ratio for reaching the size of the final switching NMOS.

To help minimize the layout from expanding too much in either the X or Y directions, the incrementing of each inverter was done by increasing physical width or increasing number of fingers (multiplier) in an alternating fashion. The resulting layout is shown in Fig 15.

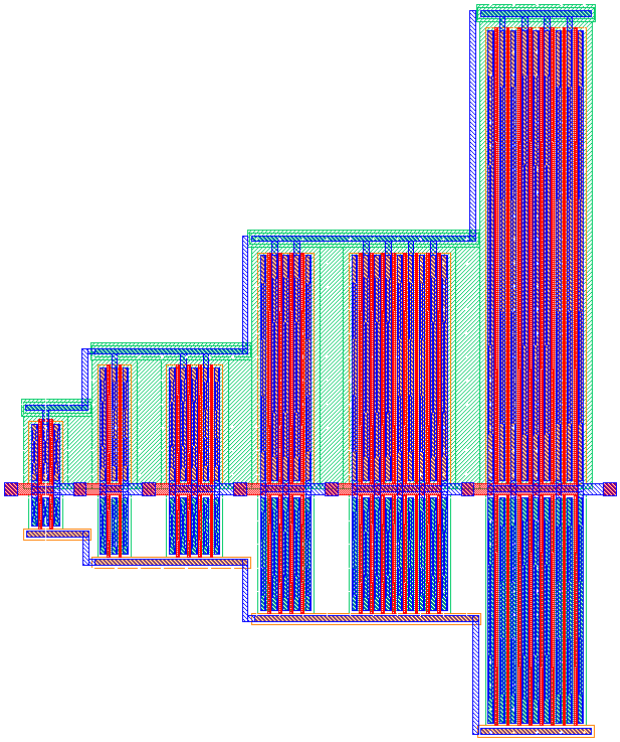

Fig 15. Buffer Layout

A quick simulation of the buffer (Fig 16) shows the output mirroring the input with minimal delay (less than 1 ns). While the signals look to be congruent, the output stage can now drive a much larger load due to its smaller switching resistance.

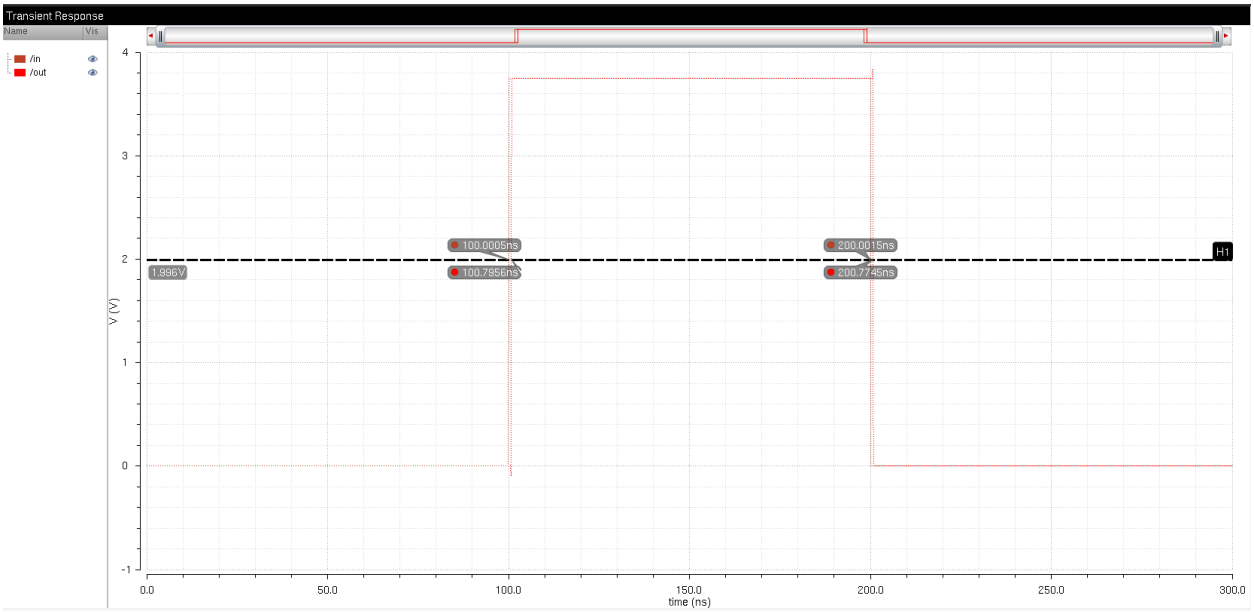

Fig 16. Buffer Delay (.795 ns)

e. NMOS Switch

The actual switching mechanism of the power supply is achieved by simply driving an NMOS on and off. Because of the current expected to be coming from the inductor, a relatively small *Rn* is required to ensure that the inductor is pulled fully to ground. For an average current of 100 mA from the inductor (see calculations under inductor section), and VSW being pulled to within half a volt from ground, it can be calculated that an *Rn* of **5 Ohms** is required. *Rn* can be calculated according to the following:

$$Rn = Rn'/Wn$$

Solving for *Wn*, the size of the final switching NMOS can be derived:

$$Wn = Rn'/Rn$$

$$Wn = 20\ kOhms/5\ Ohms$$

$$Wn = 4000$$

The actual NMOS used in the design has a ***Wn* set to 5120** (160 W * 32 Multiplier) and is shown below.

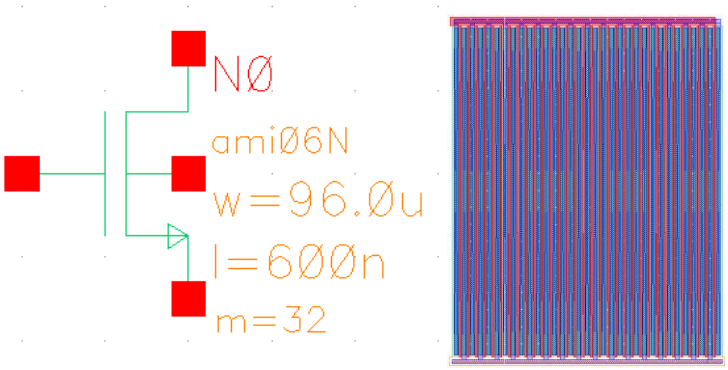

Fig 17. Switching NMOS (Wn = 5120)

f. Voltage Divider

The voltage divider takes the output voltage of the circuit and **divides it by 4**. Because the desired output of the circuit is 5 V, the output of the divider is nominally 1.25 V. This value is compared to the reference voltage from the bandgap and provides the second input to the comparator. When the output of the divider falls below 1.25 (i.e. final output voltage falls below 5), the comparator will enable the clock, thus boosting the output back towards 5 V. Once the output does reach 5 V, and the divider reaches 1.25 V, the comparator will disable the clock, and thus ceases to charge the output anymore past 5 V.

The resistors in the divider were sized according to specifications for feedback current. As feedback is **not to draw any more than 50 uA** from the output, a large enough total resistance is required to limit the current through the divider. Of course, just increasing the resistance without bound is not a suitable solution due partly because of layout constraints and because of the capacitive load seen at the input of the comparator. Too large of an RC constant, and the delay could cause issues with hysteresis, causing the output to swing too much below and above the target 5 V. A final design decision was made to use the same 34 kOhm resistors used in the bandgap to form a **102k/34k divider**. By using the same layout of resistor as in the bandgap and in each section of the divider, issues with temperature and approximate resistances can be mitigated, as the divider will be working purely on ratios of identical layouts.

A Note On Off-Chip Components

Up to this point of the report, everything detailed exists on chip, and very generally, the circuit on chip can only sense some feedback, and depending on that feedback, drive a connected node to ground at some frequency. This by itself is not enough to form the full boost SPS, but is necessary to operate the off-chip components which will generate the final output voltage. The full schematic, along with layout of the boost SPS, excluding off-chip components, is shown below (Fig 18 and Fig 19). The "BOOST" chip has two inputs/outputs, VSW and VFB, of course VCC and GND are also supplied. VSW is the chip's switching node while VFB is feedback from the chip output back to the internal comparator/resistor divider network.

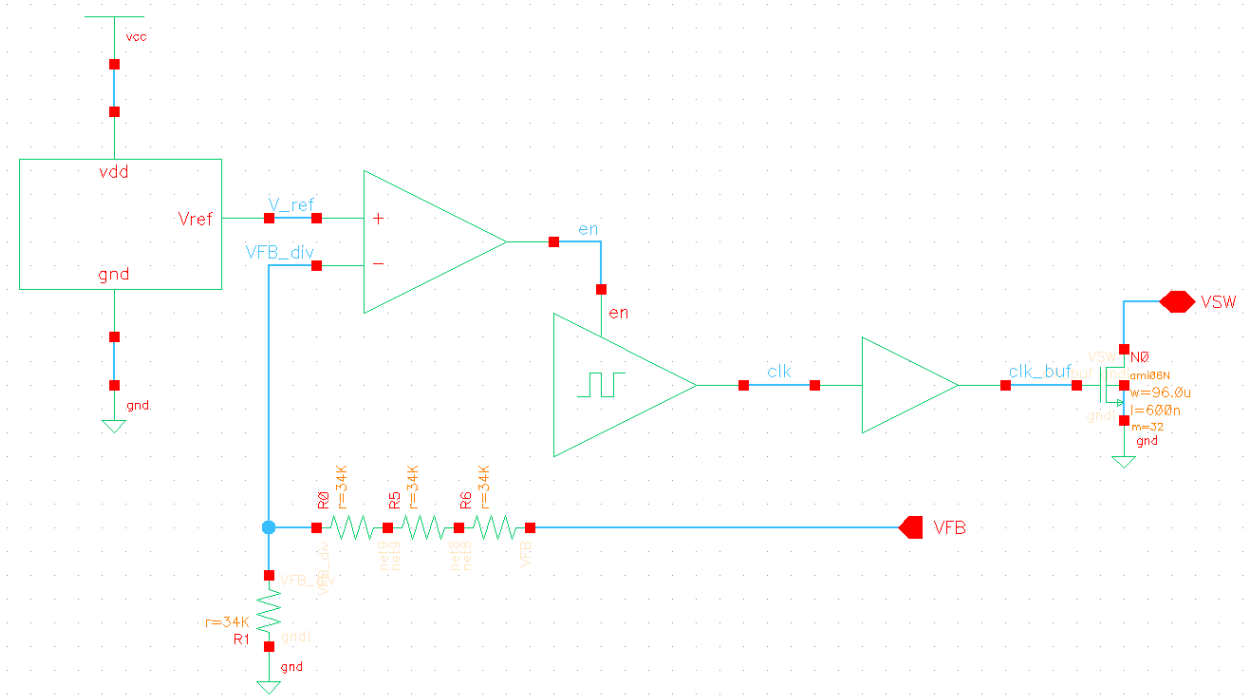

Fig 18. Full Chip Schematic

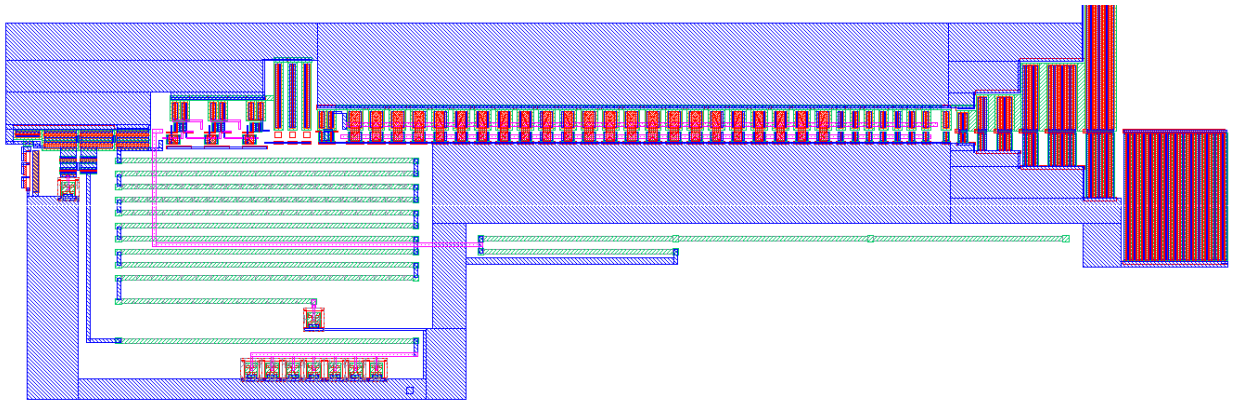

Fig 19. Full Chip Layout (Passes DRC and LVS)

g. Inductor

The inductor is connected to the voltage source and VSW. While operating, VSW is periodically grounded at the previously derived switching frequency of 4.8 MHz, and at a duty cycle of about 0.5. While grounded, the inductor begins conducting current, and once switched, that current is diverted through the diode, thus charging the output capacitor. This process is done whenever vout falls below 5 V as sensed by VFB. The average current through the inductor is calculated accordingly:

$$IL = \frac{IR}{1 - D}$$

$$IL = \frac{50\ mA}{1 - D}$$

$$IL = 100\ mA$$

Knowing the average current and selecting a maximum current change of about 5%, the sizing of the inductor can be calculated as follows:

$$L = Vout * \frac{D(1 - D)}{\Delta iL * f}$$

$$L = 5\ V * \frac{0.5(1 - 0.5)}{5\ mA * 4.8\ Mhz}$$

$$L = \ 52\ uH$$

h. Diode

The Schottky diode is used to limit current from vout to GND through VSW, as well as provide a low forward voltage bias. Additionally, it is important to choose a diode with relatively low capacitance, as a higher zero-bias depletion value requires more charge to fully discharge the diode. This charge is stolen from the capacitor every time VSW switches to ground, thus decreasing overall efficiency. The diode model used for all simulation has a **Cj0 value of 12 pF**.

i. Capacitor

The capacitor is what holds the voltage and supplies the current to the load. As current is drawn, the capacitor discharges, until the circuit turns on and the inductor begins periodically pouring current back into the capacitor to charge it back to nominal voltage. A minimum capacitance is calculated with the following:

$$Cmin = \frac{D}{R * f * (\frac{\Delta Vout}{Vout})}$$

$$Cmin = \frac{.5}{100\ Ohm * 4.8\ Mhz * (\frac{5mV}{5V})}$$

$$Cmin = 1.04\ uF$$

While this is the calculated minimum capacitance required for a less than 0.5% change in vout, this is not the value that was used for the circuit, as this capacitance proved to be too small with the hysteresis present in the rest of the circuit. Due to the small capacitance and delay present, vout was charged much too over and fell much too below 5 V. The capacitor was therefore swapped for one a factor of 10 times larger, **at 10.7 uF**. As to be shown, this resulted in a much more stable vout centered at 5 V.

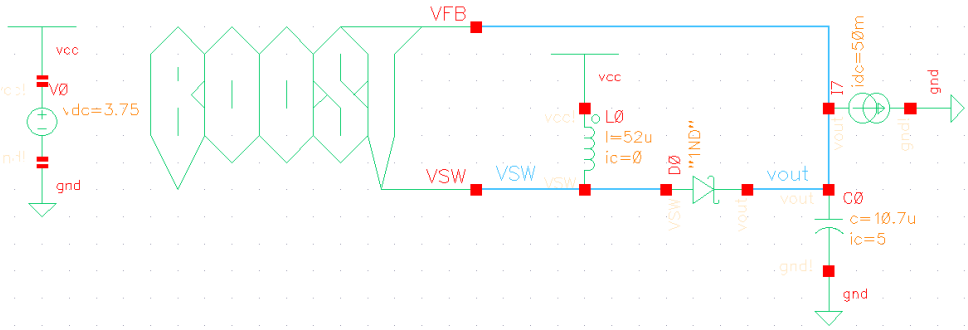

Fig 20. Full Schematic of Chip and Off-Chip Components

III. SIMULATIONS

The following simulation result shows an average output voltage of 5 V given a voltage source of 3.75 V, temperature of 25 °C, and load of 50 mA *(note: all simulation from here are considered to be under load of 50 mA unless otherwise stated)*.

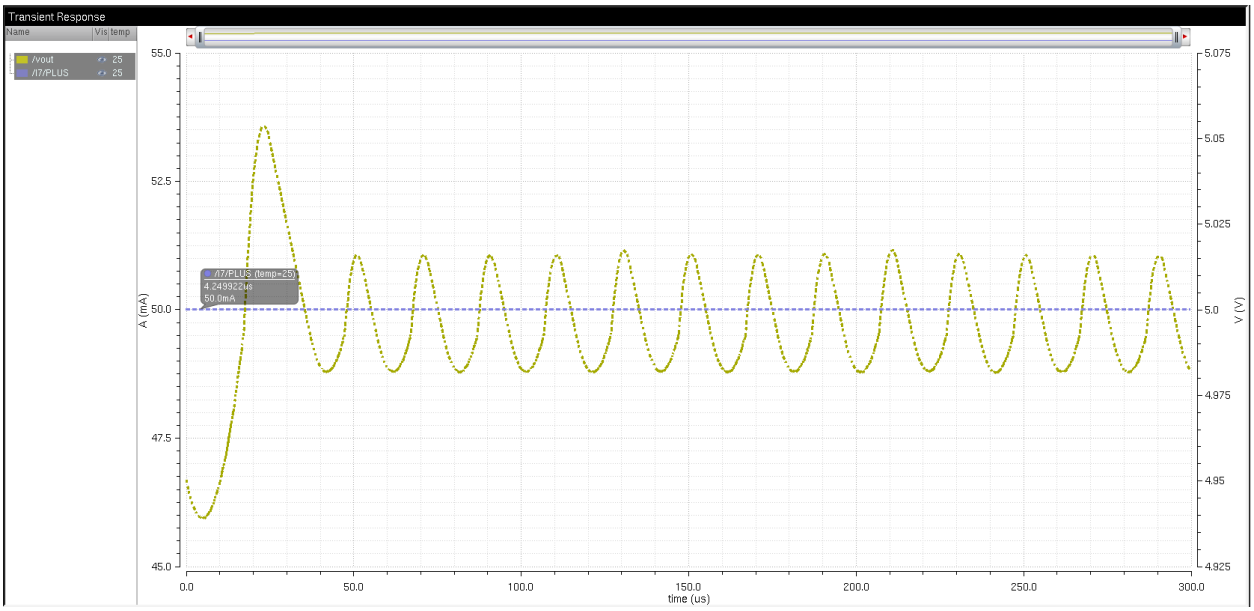

Fig 21. Basic Operation of Boost SPS (VCC = 3.75, T = 25 °C)

Looking closely at the output, it is observed that vout does not stay a steady 5 V and instead swings +/- 15 mV around the nominal voltage. This is due to the hysteresis caused by inherit delay in the circuit. When VFB senses vout dropping below, or rising above 5 V, there is an inherit delay though the comparator and buffers which takes time before the circuit can be turned on or off. During this time, the circuit continues to drain the output capacitor or charge the output capacitor past 5 V. This delay is actually somewhat beneficial, as it prevents the circuit from having to constantly turn on and off. Instead, the output is allowed to drift from 5 V in either direction somewhat, to limit the time the circuit is on and therefore operates more efficiently while providing the same average voltage over time.

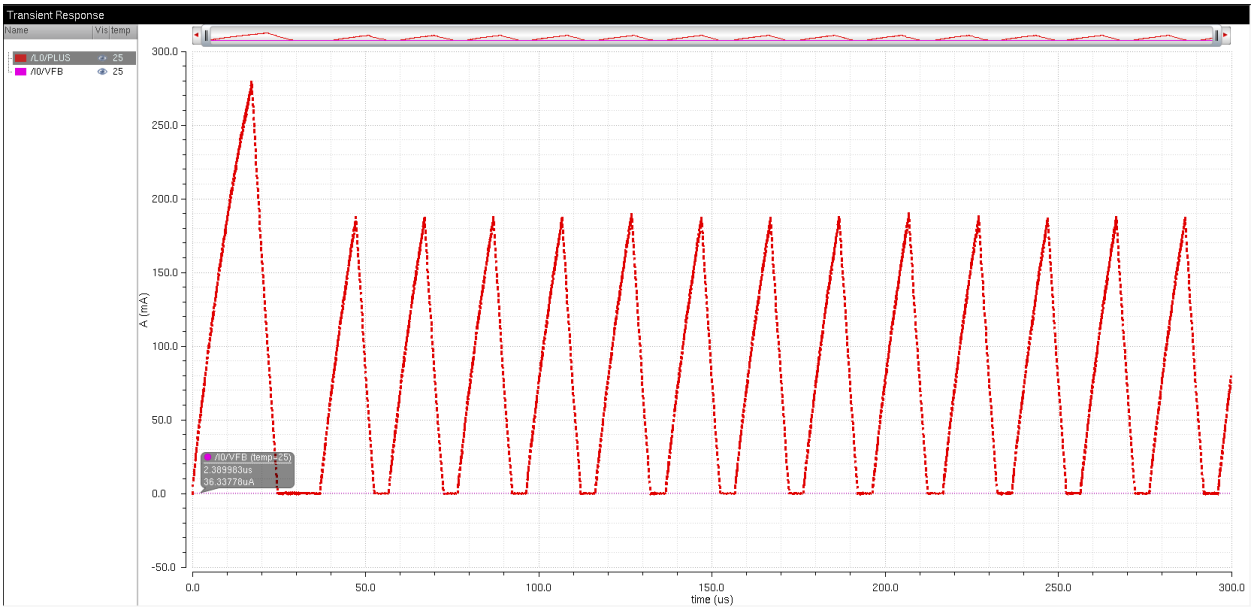

Fig 22. Feedback and Inductor Current (VCC = 3.75, T = 25 °C)

As mentioned previously, VFB is to draw no more current than 50 uA. The above simulation shows a current draw of just 36 uA. Additionally, the actual average current through the inductor is shown as well. Previously this value was calculated to be 100 mA, and simulations show an actual **80 mA on average** traveling through the inductor.

The following simulations show output of the circuit at varying input voltages and varying temperatures.

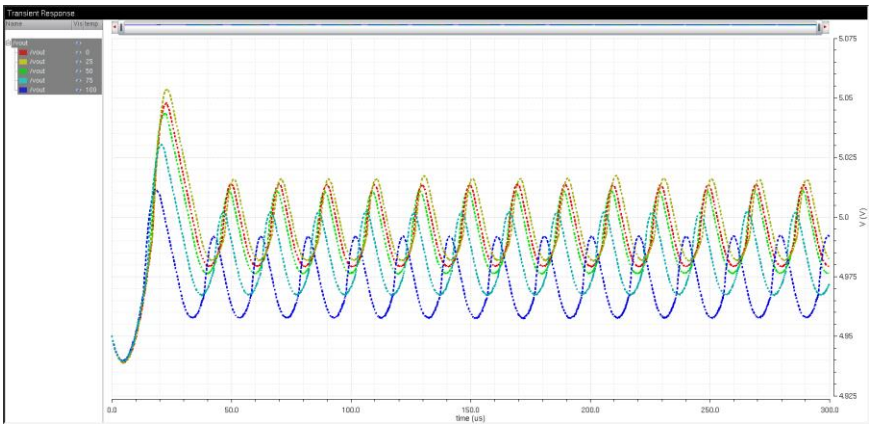

Fig 23. Basic Operation of Boost SPS (VCC = 3.75, T = 0-100 °C)

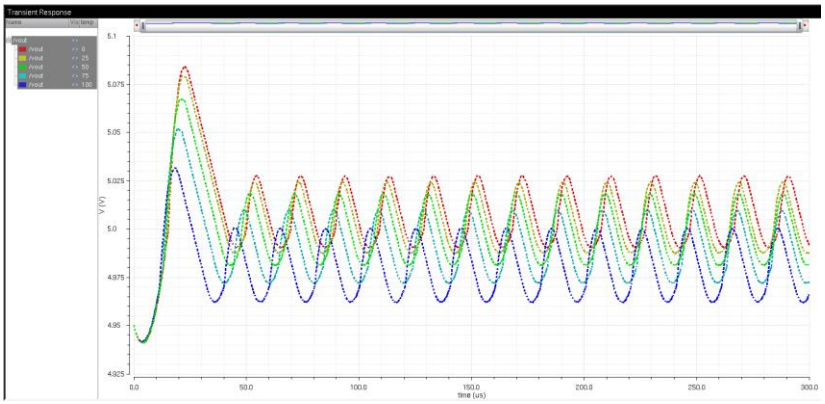

Fig 24. Basic Operation of Boost SPS (VCC = 4.00, T = 0-100 ℃)

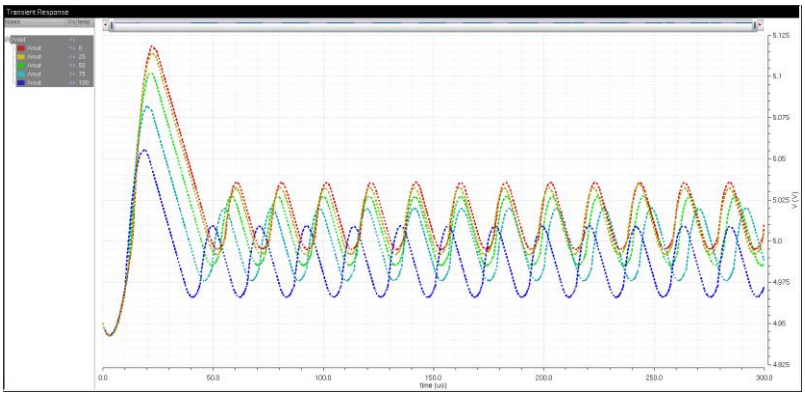

Fig 25. Basic Operation of Boost SPS (VCC = 4.25, T = 0-100 ℃)

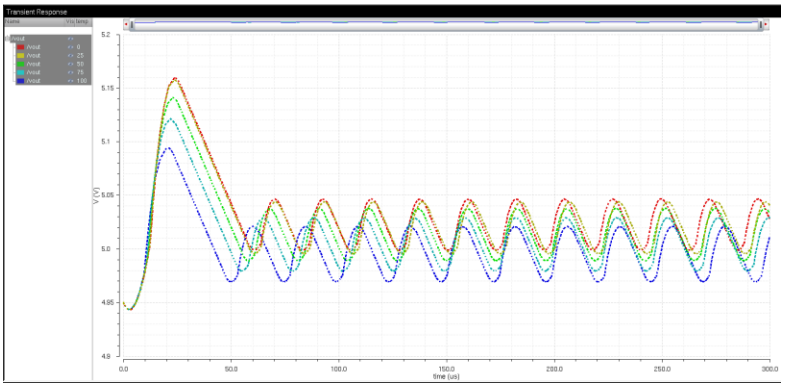

Fig 26. Basic Operation of Boost SPS (VCC = 4.50, T = 0-100 ℃)

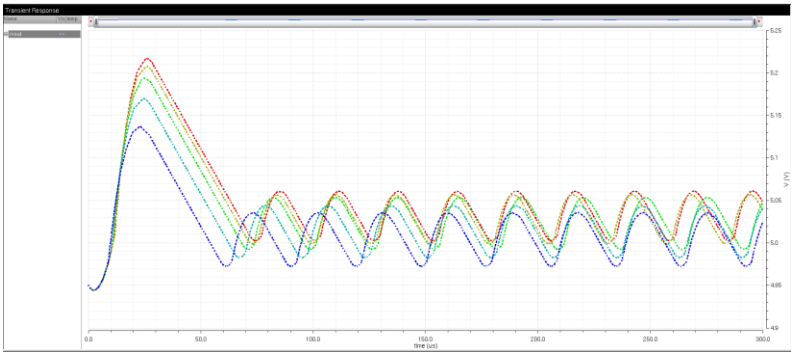

Fig 27. Basic Operation of Boost SPS (VCC = 4.75, T = 0-100 ℃)

Overall, simulations show the circuit to operate at the nominal voltage across both different input voltage and temperature ranges. The biggest difference seen across the simulations is a slight decrease in output voltage as temperature increases (about 30 mV difference between 0℃ and 100℃ at its peak).

IV. Results

The following graphs show the efficiency of the circuit across varying temperatures, source voltages, and well as loads.

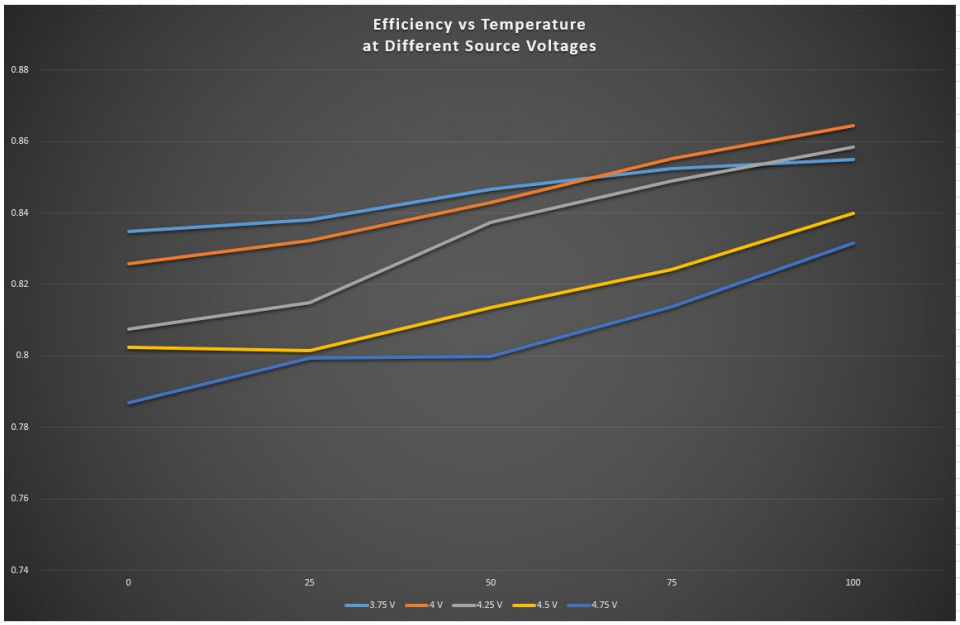

Fig 28. Efficiency vs Temperature at Varying Source Voltages, Load = 50 mA

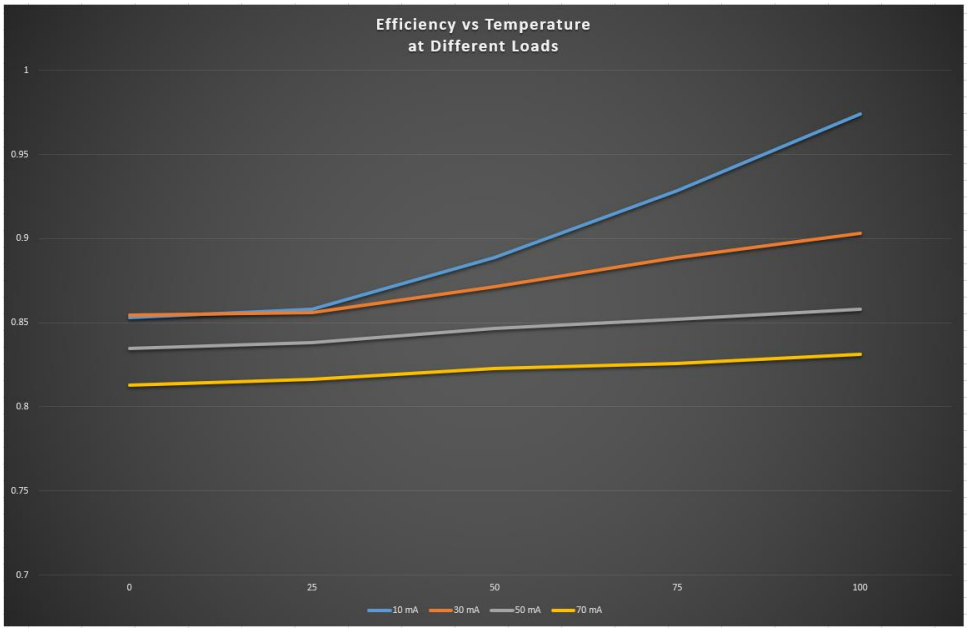

Fig 29. Efficiency vs Temperature at Varying Loads, Voltage Source = 3.25 V

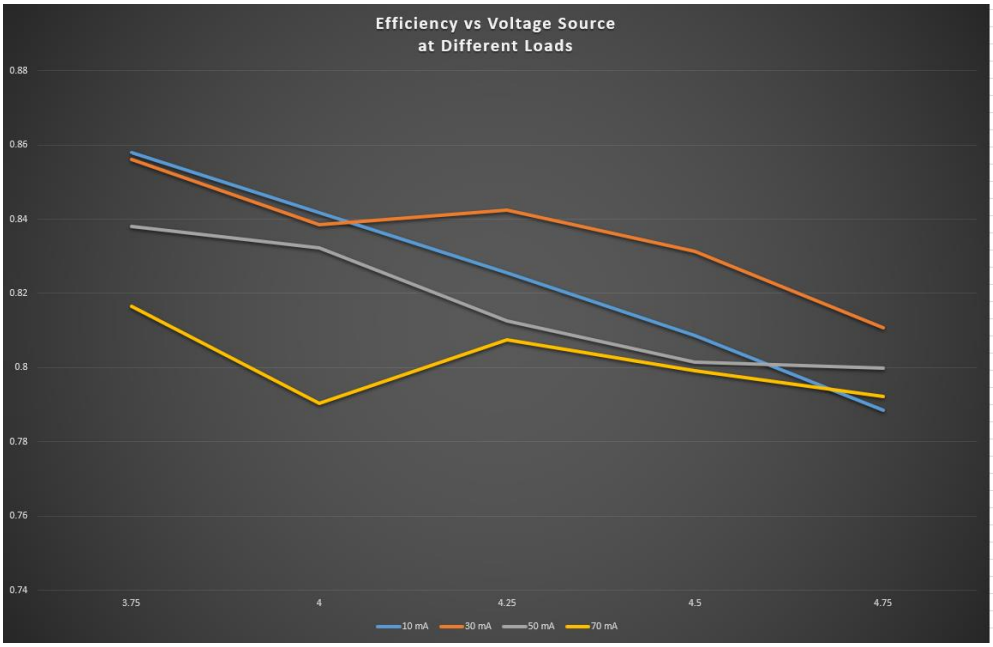

Fig 30. Efficiency vs Voltage Source at Varying Loads, Temperature = 25 ℃

Overall the efficiency across all parameters is relatively constant, within the 80% range. Expected losses of efficiency such as an increasing load are observed, however, the most noticeable trend here is the fact that efficiency almost always increases with temperature. Another interesting observation the fact that lower voltage sources seem to have higher efficiency. This is most evident in Fig 30, as at a voltage source of 4.75, efficiency begins to fall below even 80%.

V. LAYOUT OF PAD FRAME

Below is an example of how the chip would be padded out. At a size of approximately 940 um by 310 um, the layout has no problems fitting within the constraints of the pad frame.

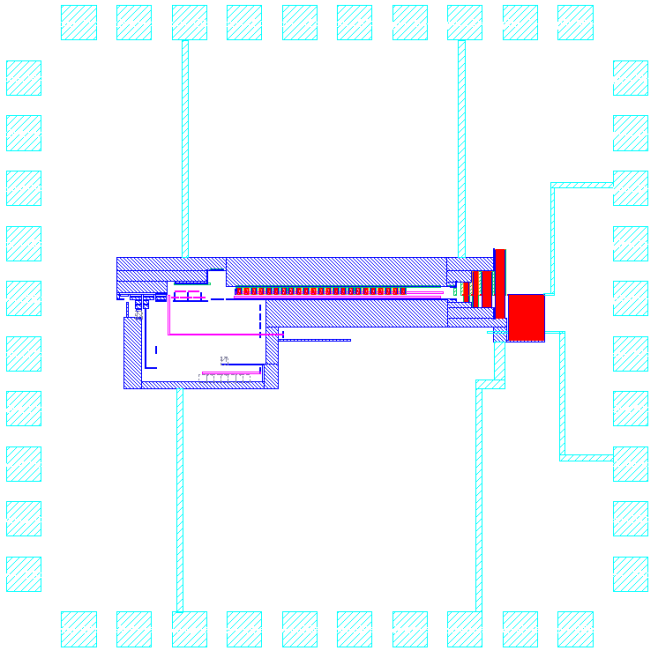

Fig 31. Layout Bonded to Pad Frame

The pinout of the chip is characterized by the following table:

Pin No.	Connection
3	VSW
8	VCC
13	VCC
28	GND
33	GND
38	VFB
Other	NC

Table 1. Pinout