Flyback Switching Power Supply (SPS) in the C5 process

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EE 421 – Integrated Circuit Design

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12/3/20

1. Introduction

The purpose of this report is to comment and document the design, layout, and simulation of a Flyback SPS in the C5 process. The Flyback SPS consists of an integrated chip, which was the main design of this project, and several off-chip components. These components include a transformer, power MOSFET, Zener diode, power supplies of 5 V and 170 V, 1 uF and 10 uF capacitors, and a resistive load on the output voltage of the Flyback (see Figure 1). A Flyback SPS is often used in consumer electronics such as laptop power supplies and /or electric shavers. The reason the Flyback is used in this devices is because of its ability to rectify an AC voltage to DC at a higher effective frequency by using the power MOSFET as a switch, which allows for the use smaller transformer, this is a must for ensuring a small power supply. The Flyback is meant to output a nominally value of 12.5 V at different load currents and it should be able to supply more than 2 A of current to a load as well.

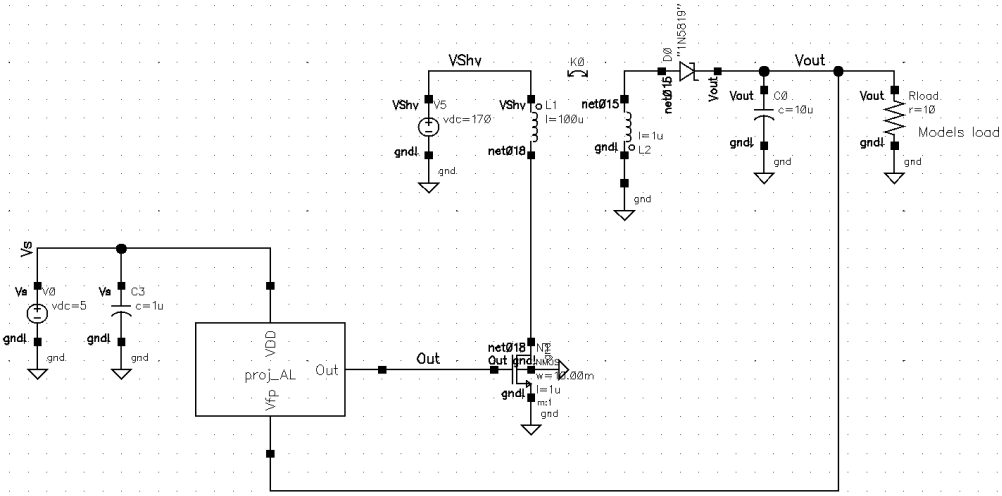

Figure 1 – Schematic of a Flyback SPS

2. Design of the Flyback SPS (Switching Power Supply)

The integrated chip for the Flyback implements feedback control for the system. The chip itself is comprised of a bandgap reference voltage, 1 pF capacitor, voltage comparator, enabled ring

oscillator, 1/10 voltage divider, and buffer (see Figure 2). The chip operates with the bandgap outputting a voltage reference of 1.25 V on the comparator. As the output of the Flyback feeds back into the chip where a 1/10 voltage divider lowers the voltage, so it is small enough to be compared with the voltage reference. The comparator will then start to turn on and off the enabled ring oscillator, which is designed to operate at 5 MHz, depending on the input voltage as it varies due to the constant charging and discharging of the off-chip 10 uF capacitor on the flyback. This allows the output to remain around the desired 12.5 V. Also, there is a large buffer after the ring oscillator, so that the output can drive the large power MOSFET which acts like a capacitor.

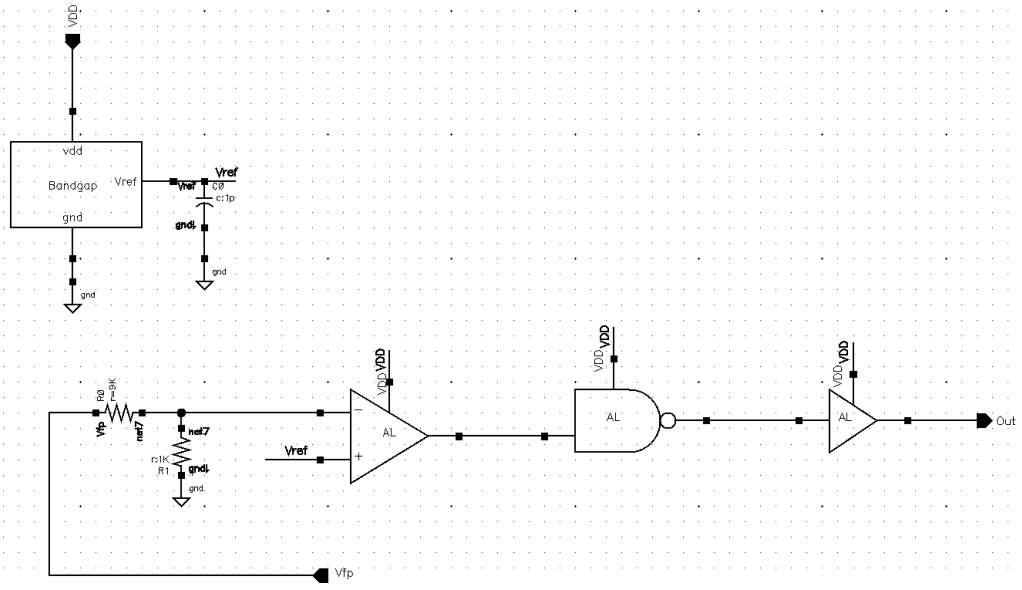

Figure 2 – Schematic of Flyback integrated chip

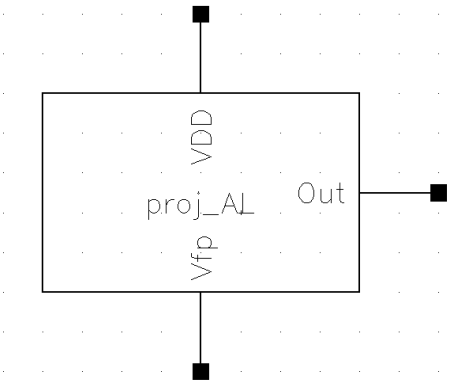

Figure 3 – Symbol for the integrated chip

2.1 Layout of the integrated Flyback chip

In Figure 4, the entire layout for the flyback chip can be seen and it includes the bandgap, 1 pF capacitor, 1/10 voltage divider, voltage comparator, enabled ring oscillator, and buffer. It can also be confirmed that this layout design passed DRC and matched with the schematic through LVS (see Figures 5 and 6).

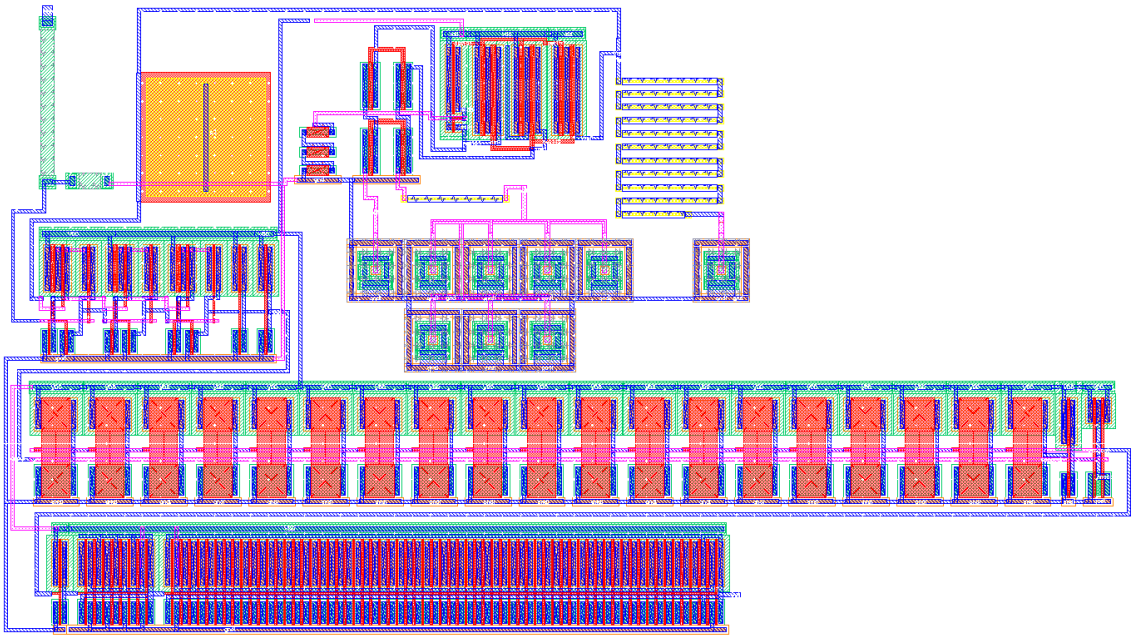

Figure 4 – Final Layout of Flyback chip

Figure 5 – LVS of layout design

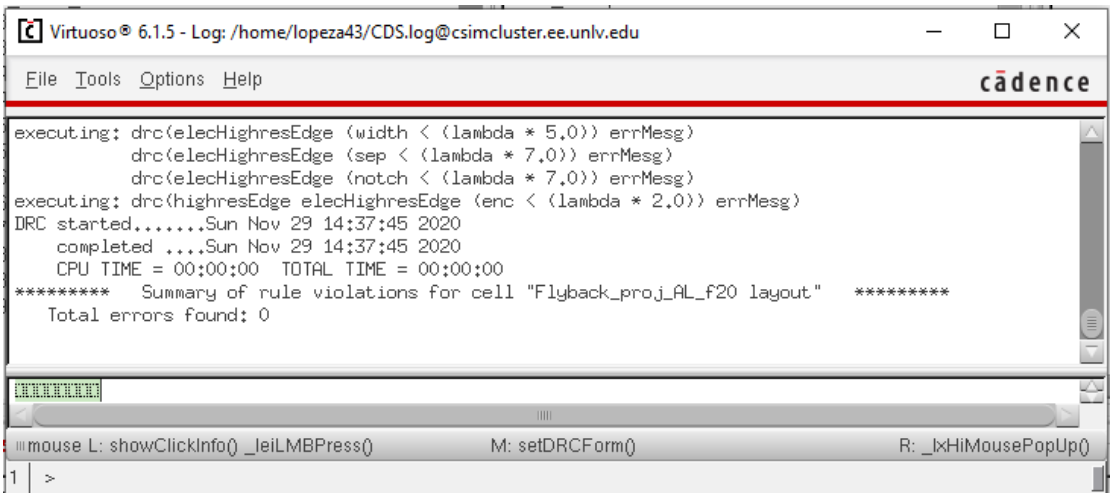

Figure 6 – DRC of layout design

2.2 Individual components of the chip

2.2.1 Bandgap voltage reference

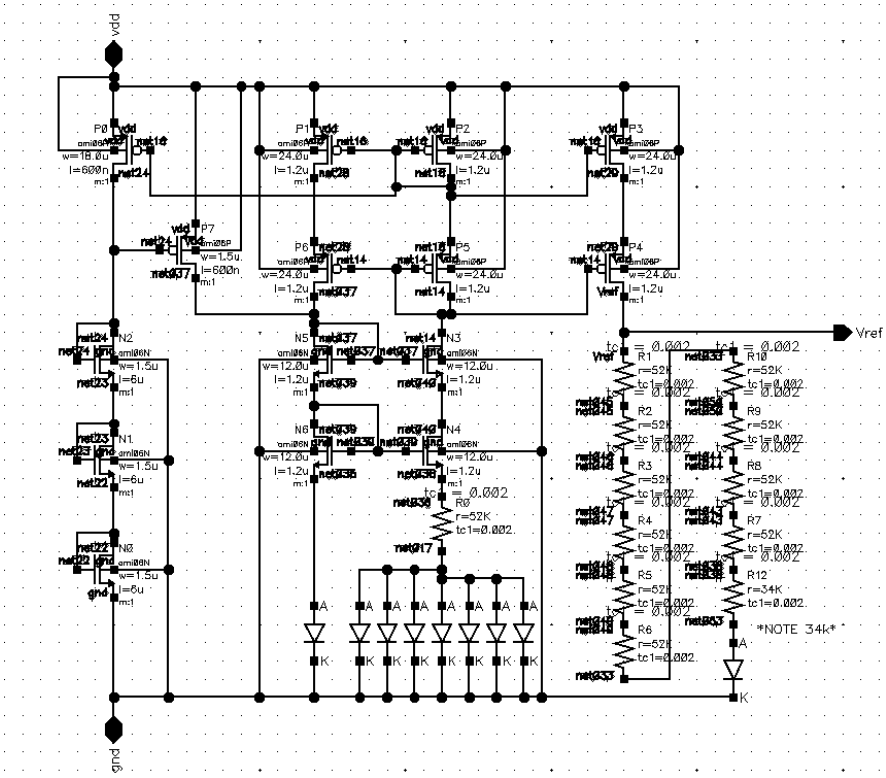

Figure 7 – Schematic of the bandgap

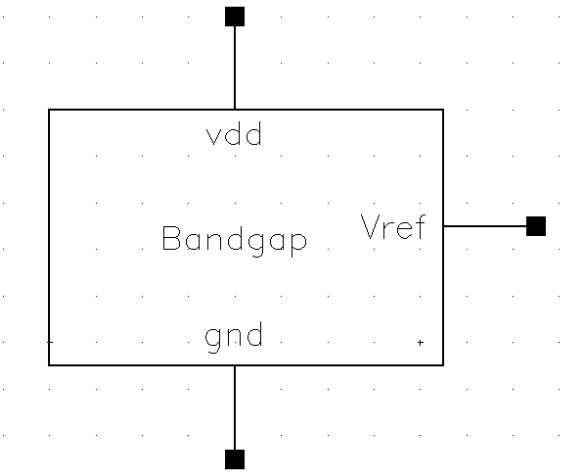

Figure 8 – Bandgap symbol

The bandgap was included in this design to output a voltage reference of 1.25 V independent of the power supply and temperature affecting the Flyback circuit and chip. This is important as the comparator needs a basis that does not change, so that the circuit can output the 12.5 V.

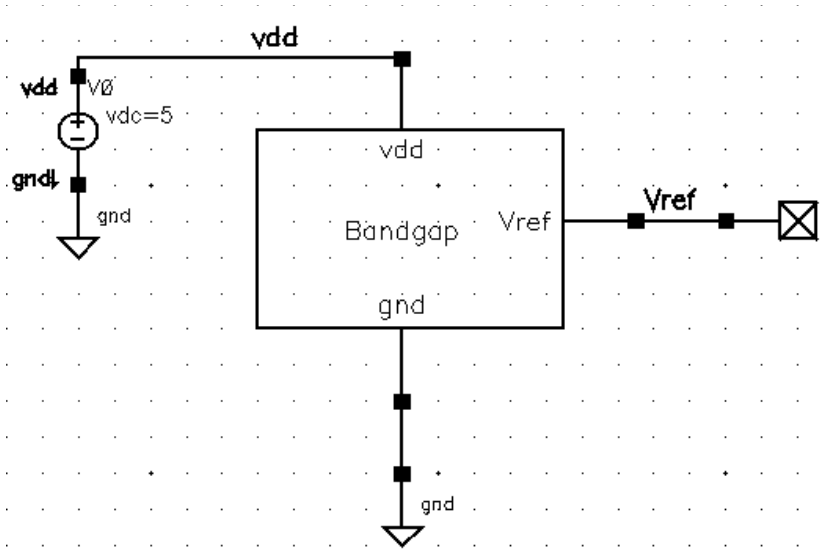

Figure 9 – Simulation circuit of the bandgap

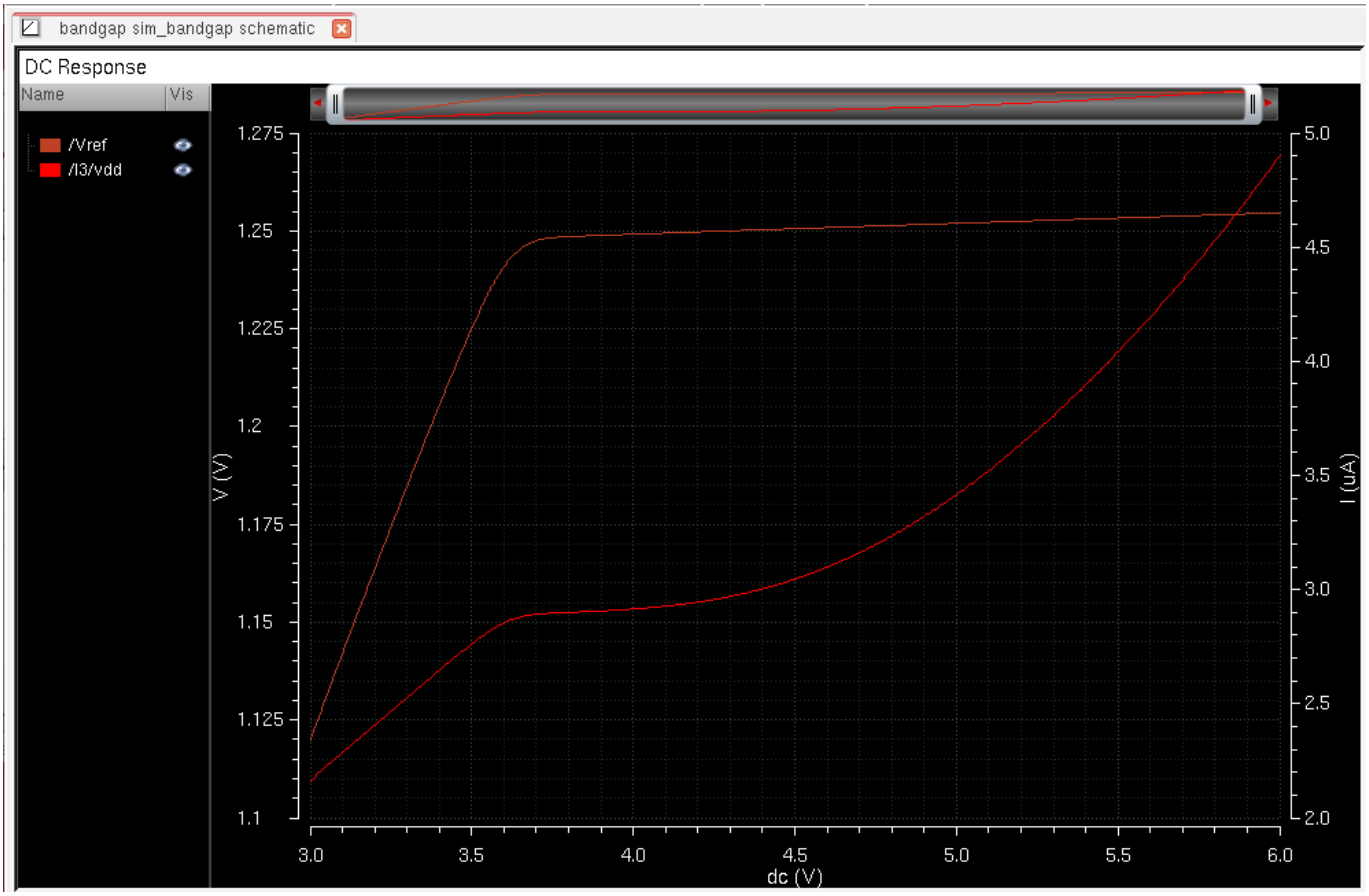

Figure 10 – DC sweep for VDD of bandgap

Looking at Figure 10, the bandgap starts to output 1.25 V when the power supply voltage reaches around 3.6 V and remains there as it increases. Being able to output the reference voltage at 3.6 V shows that the bandgap can operate independently of the power supply. The bandgap starts to draw more current as VDD increases from 2.2 uA to 4.9 uA, which is good as it shows the bandgap will not draw a large amount of current from the power supply.

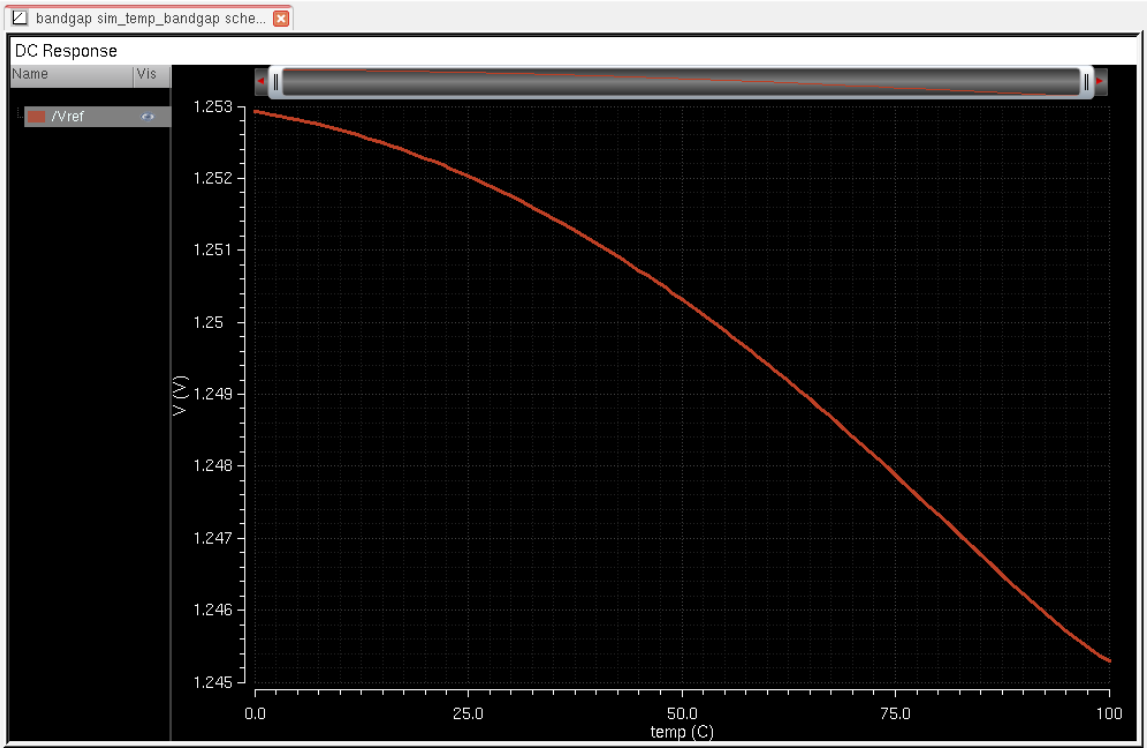

Figure 11 – Temperature simulation for bandgap

Looking at the output of the bandgap at 0 °C it is 1.253 V and drops down to around 1.245 V. After a change of 100 °C, it can be concluded that the bandgap voltage does not change drastically at a high temperature. Showing that the bandgap can provided a good voltage reference independent of temperature for the design.

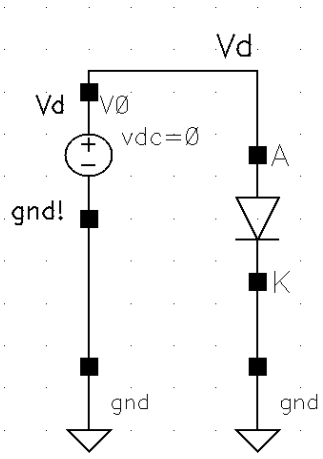

Figure 12 – Simulation circuit of parasitic diode

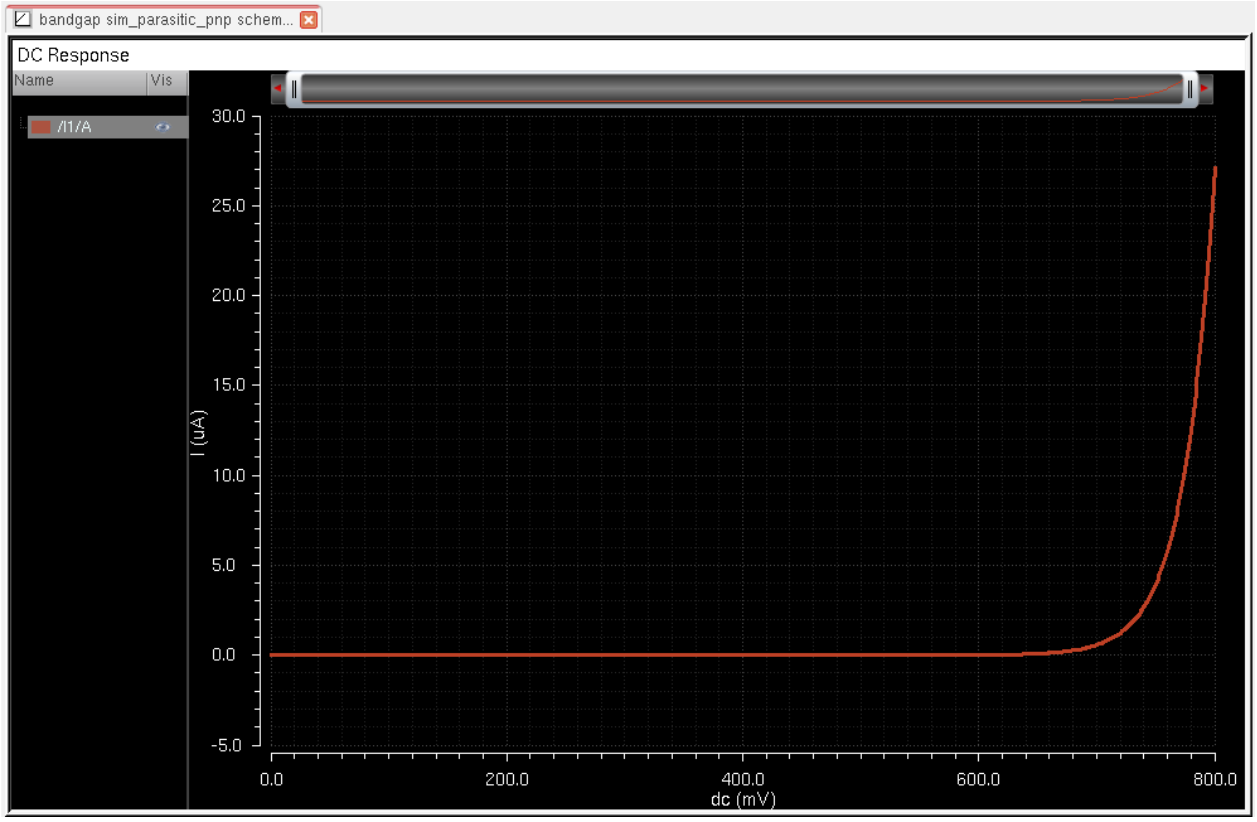

Figure 13 – DC sweep of parasitic diode

Inside the bandgap there are multiple parasitic diodes (see Figure 7). The simulation in Figure 12 shows that voltage threshold of the diode is 700 mV as the current increases once it passes.

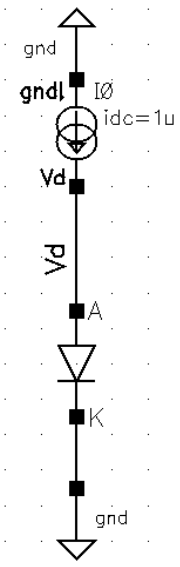

Figure 14 – Simulation circuit for temperature of diode

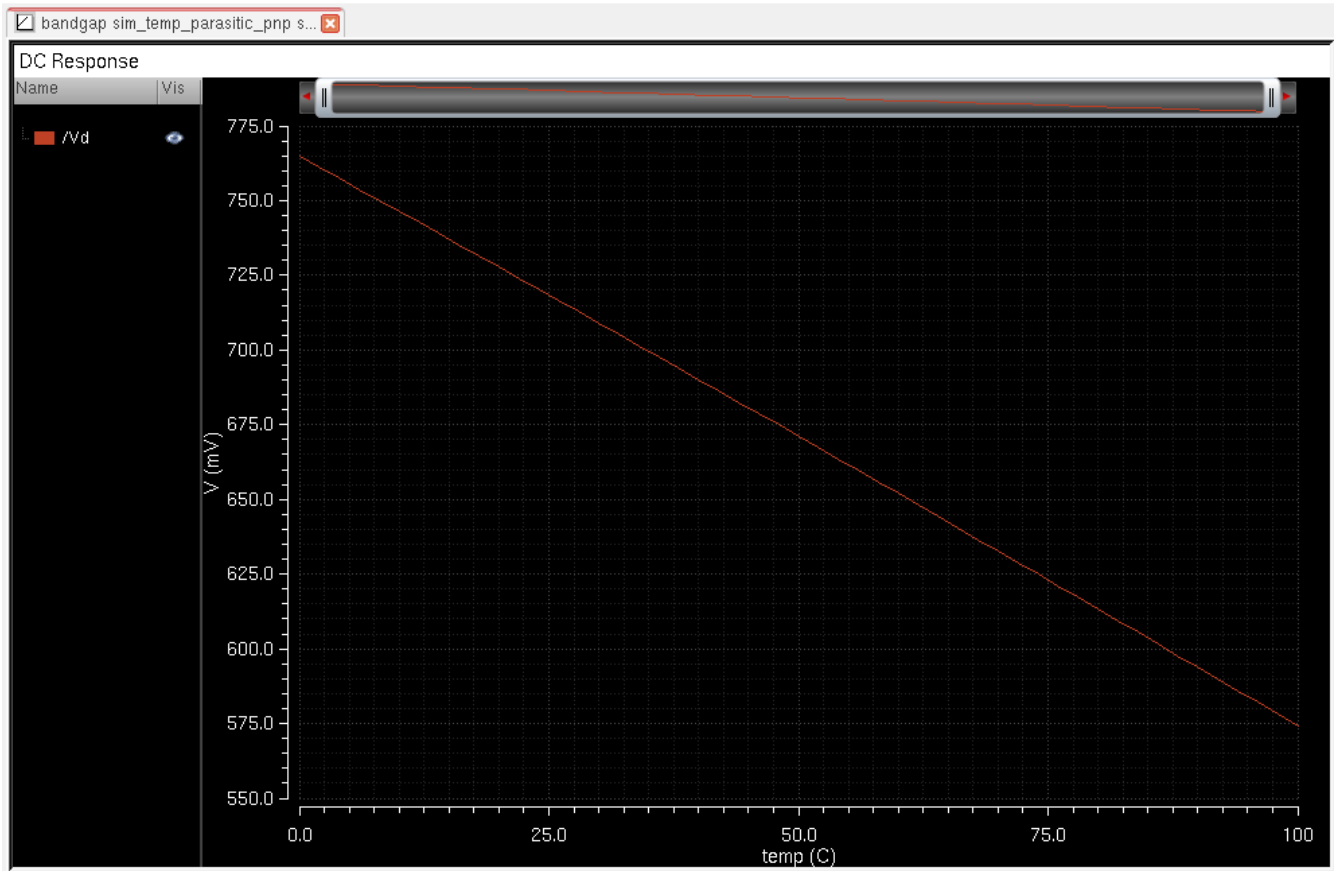

Figure 15 – Temperature simulation for diode

In Figure 15, testing the diode from a temperature range of 0 to 100 °C, it can be concluded that the diode performs worse at higher temperatures and better at higher temperatures as it goes from 765 mV to 575 mV. It can also be said that the temperatures for both the diode and bandgap are negatively linear.

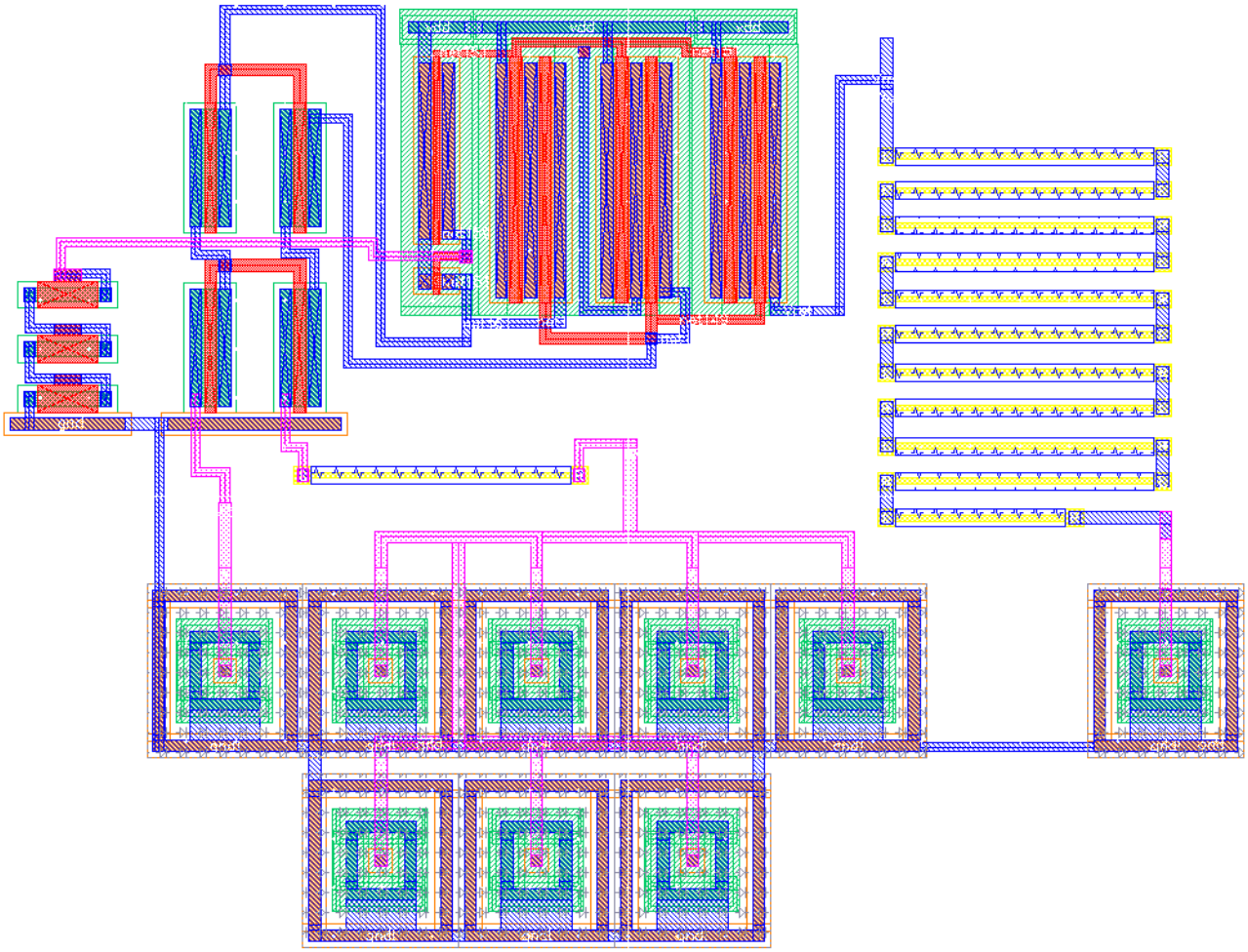

Figure 16 – Layout of bandgap

The bandgap section concludes with the layout of the schematic (see Figure 7) for it in Figure 16.

2.2.2 Inverter

For certain designs in the chip they require simple components that have been used in the EE 421 class before, so they have been pre-built and will be seen throughout this report. The first being a 12 um/6 um inverter (see Figure 17) used to either invert certain logic signals or square up the input or output of a signal.

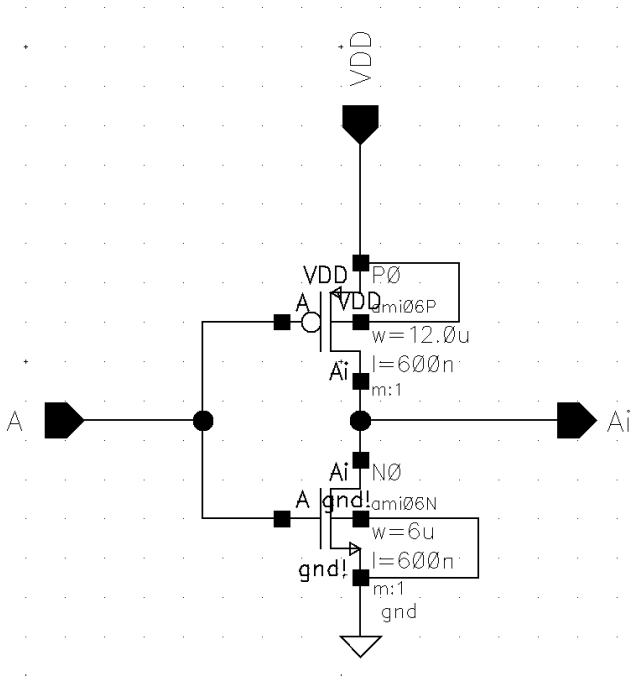

Figure 17 – Schematic for 12 um/6 um inverter

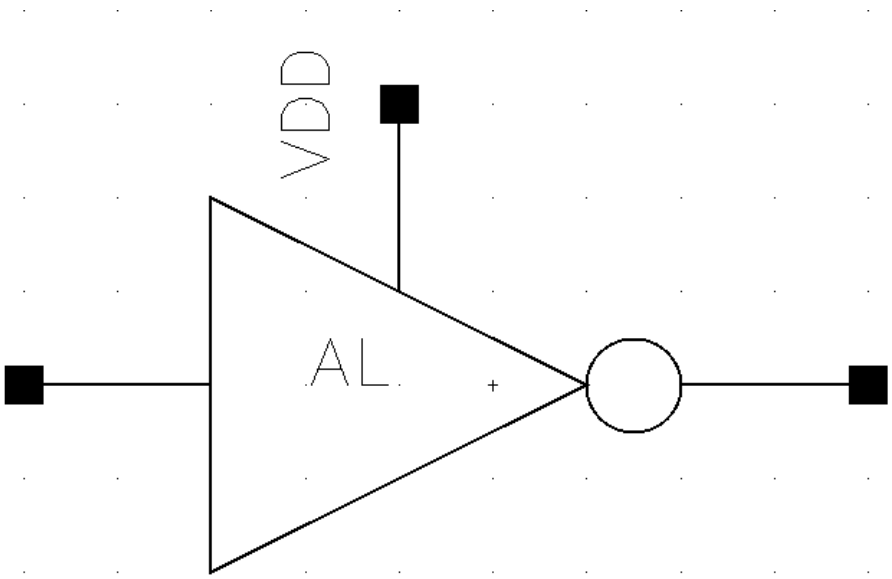

Figure 18 – Symbol for inverter

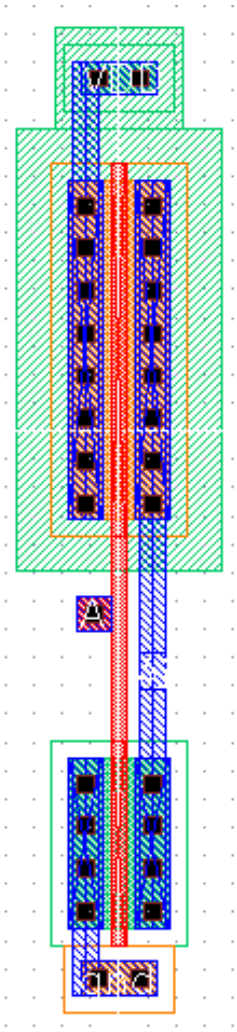

Figure 19 – Inverter layout

2.2.3 Slow Inverter

For the enabled ring oscillator, it needs to oscillate at a frequency of 5 MHz or have a period signal of 200 ns. To accomplish this, the ring oscillator needs to have an array of slow inverters to delay the signal enough that it reaches 5 MHz. Each slow inverter is 7.95 um in width and length for both the PMOS and NMOS to achieve this delay (see Figure 20).

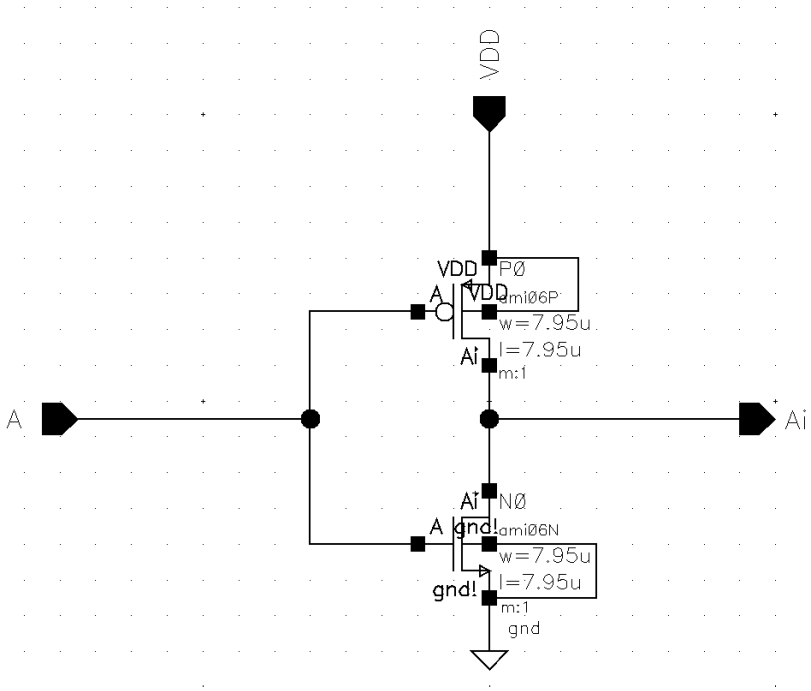

Figure 20 – Schematic of 7.95 um/7.95 um slow inverter

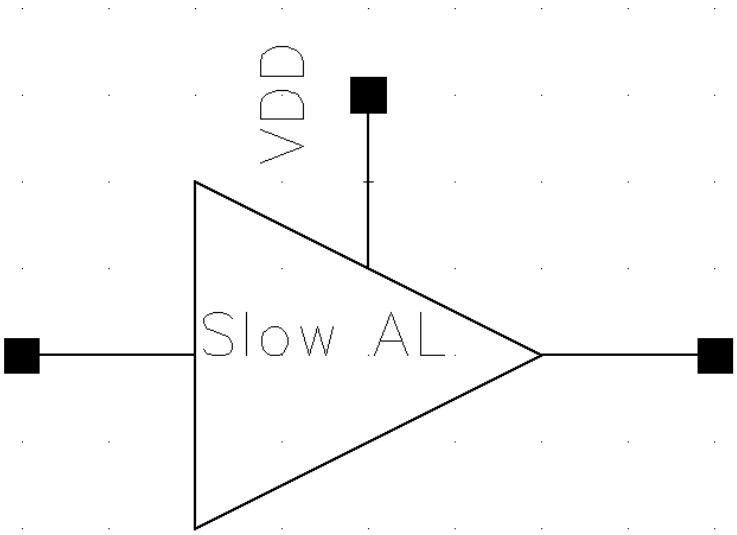

Figure 21 – Symbol for slow inverter

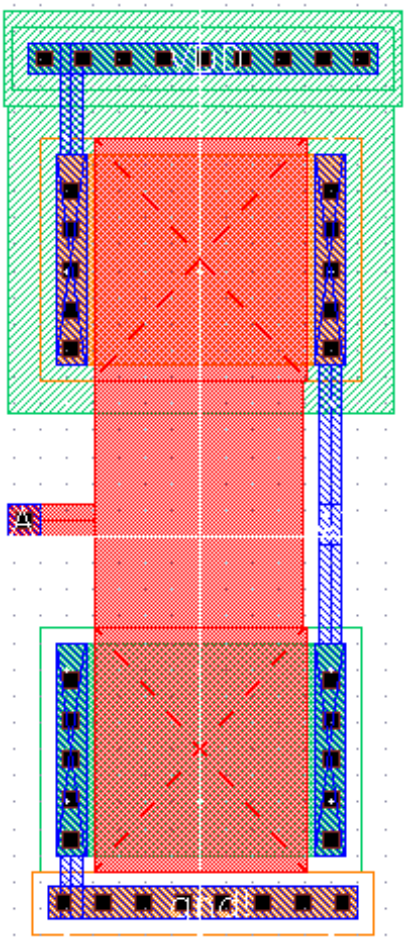

Figure 22 – Layout for slow inverter

2.2.3 NAND gate

The next component is a NAND gate, and it will be used in the enabled ring oscillator. The NAND gate's logic functions make it useful as an enable switch for the ring oscillator allowing the signal to be turned on and off quickly without much delay. Also sizing for both the PMOS and NMOS in the circuit is 6 um for the width and 600 nm for the length as to ensure proper switching times between the inputs and outputs of the gate (see Figure 23).

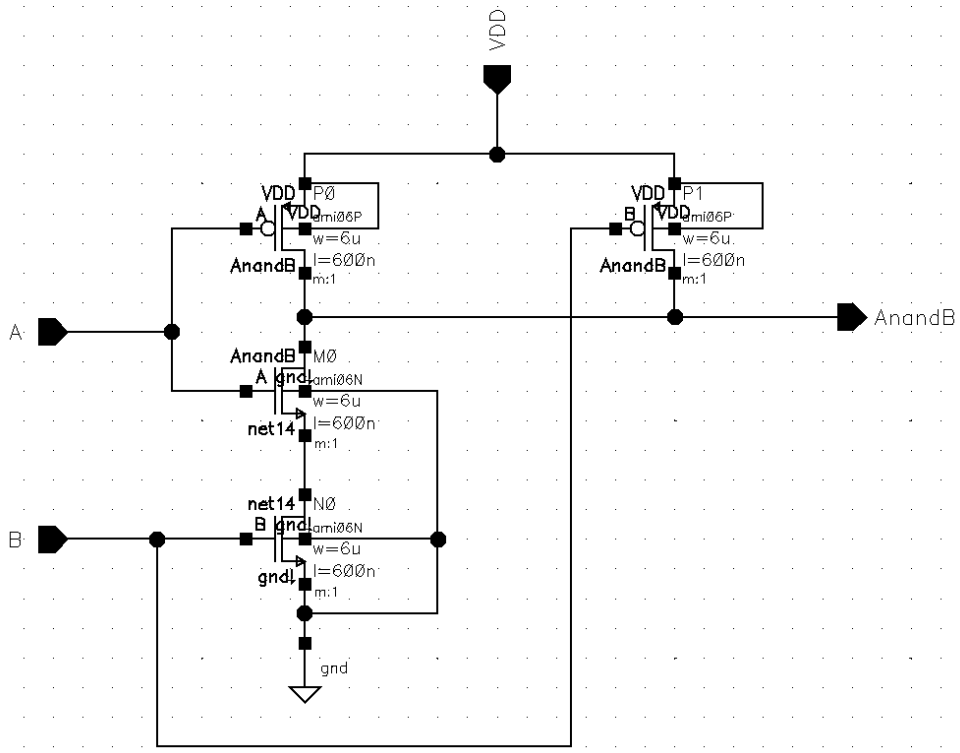

Figure 23 – Schematic for NAND gate

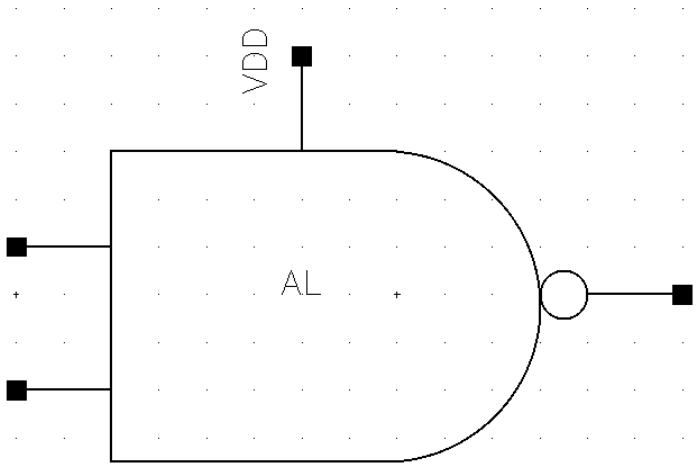

Figure 24 – Symbol for NAND gate

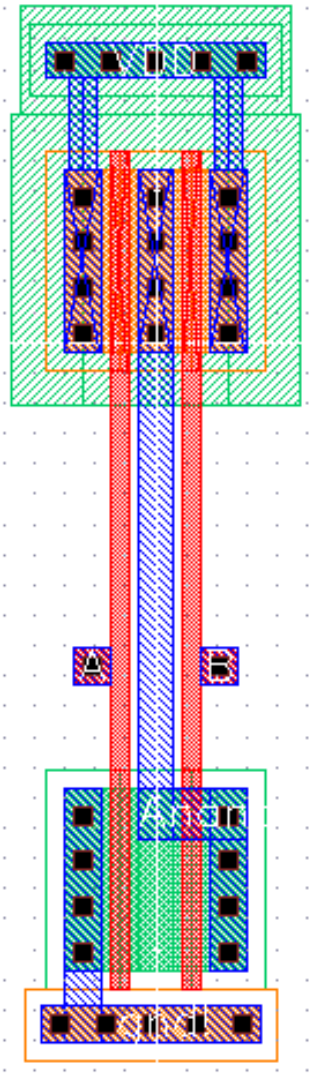

Figure 25 – Layout for NAND gate

2.2.4 1 pF capacitor

The design schematic requires a 1 pF capacitor (see Figure 26) on the output of the bandgap voltage reference to ensure that the 1.25 V is constant with no ripple or voltage swinging causing issue.

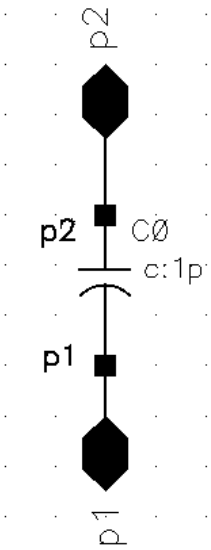

Figure 26 – Schematic for 1 pF capacitor

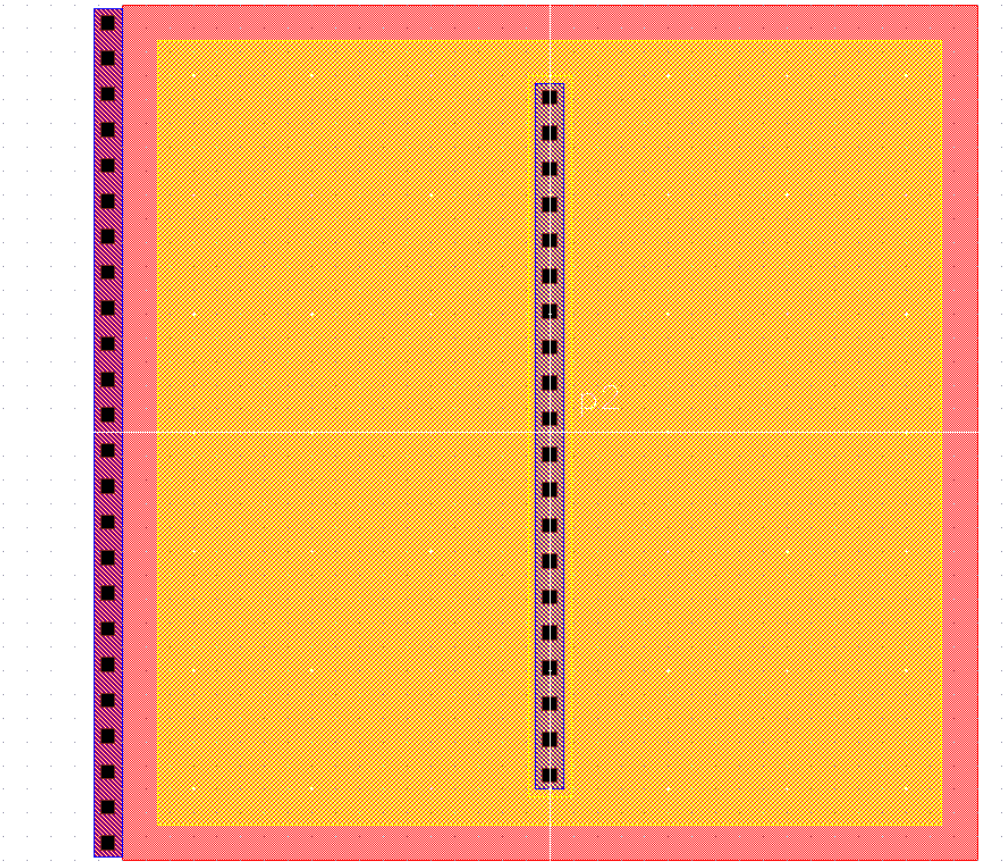

Figure 27 – Layout of 1 pF capacitor

2.2.5 1k and 9k resistor

For the comparator to work properly we need a 1/10 voltage divider on one of the inputs, so that the voltage is small enough to compare otherwise the comparator will never turn on. To make that voltage divider we use a 9k resistor in series with a 1k resistor (see Figure 28 and 30).

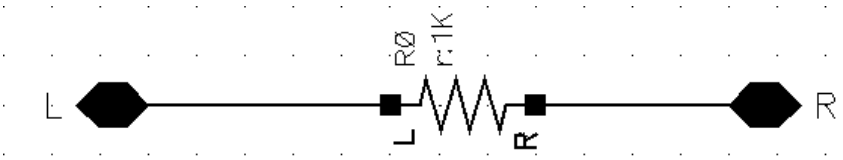

Figure 28 – Schematic for 1k resistor

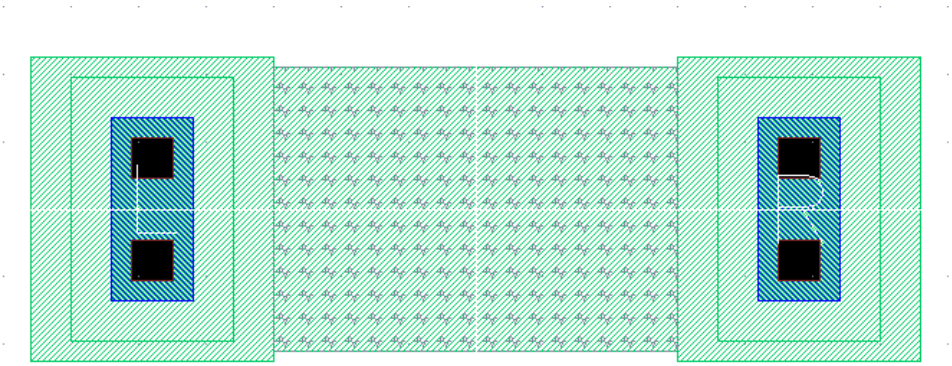

Figure 29 – Layout of 1k resistor

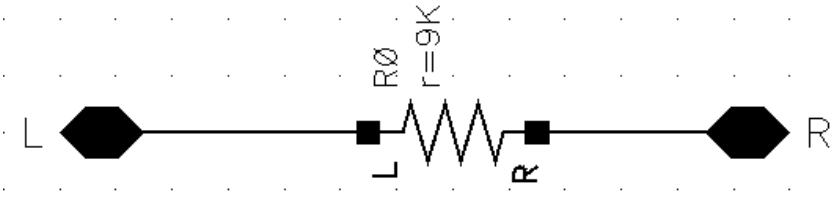

Figure 30 – Schematic for 9k resistor

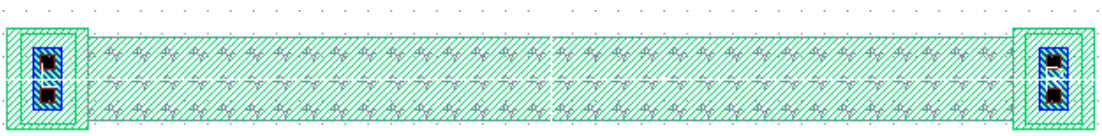

Figure 31 – Layout for 9k resistor

2.2.6 Buffer Design

An important design in this chip is the buffer for the output signal as the output is connected to the gate of a large power MOSFET (see Figure 32). The power MOSFET has a large input capacitance hence why we need to calculate both the input capacitance that needs to be driven and the number of stages our buffer needs.

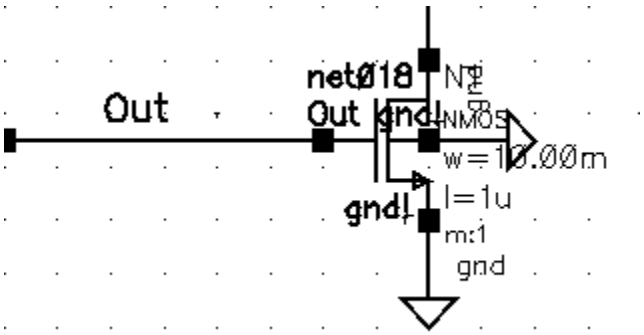

Figure 32 – 10 mm Power MOSFET

To determine the input capacitance of the MOSFET we take the width and length and multiple it the Cox of the MOSFET.

$$C_{load} = Cox \cdot W \cdot L$$

$$C_{load} = 3.453e^{-4}\ \frac{F}{um^2} \cdot 0.1 \cdot 1\ um = 3.453\ pF$$

Now that the capacitive load is known, it is now possible to calculate the number of stages that the inverter will use. Before starting however, take note the area factor, A, is going to be 8. The reason for this is because the ideal area factor 2.718 is too small of factor to make the buffer practical in a layout.

$$N \cdot \ln A = \ln \frac{C_{load}}{C_{in}}$$

$$C_{in} = \frac{3}{2} \cdot (Cox_n + Cox_p) = \frac{3}{2} \cdot (2.5\ \frac{fF}{um^2} \cdot 6\ um \cdot 0.6\ um + \ 2.5\ \frac{fF}{um^2} \cdot 12\ um \cdot 0.6\ um) = \ 40.5\ fF$$

$$N = \ \frac{1}{2} \cdot \ln \frac{3.453\ pF}{40.5\ fF} = \ 2.2$$

Couple of things to note before continuing. The natural log of 8 is around, hence why ½ is on the other side of the equation. Also, the C_{in} capacitance is calculated from the Cox' of both the PMOS and NMOS multiplied by their respective length and width. Looking at the hand

calculations we need about 2 stages for the buffer if we use an area factor of 8, but to maintain the inversion logic of our ring oscillator the buffer will use 3 stages in the schematic (see Figure 33). The buffer is comprised of 3 12 um/6um inverters with the last two inverters have a multicity of 8 and 64.

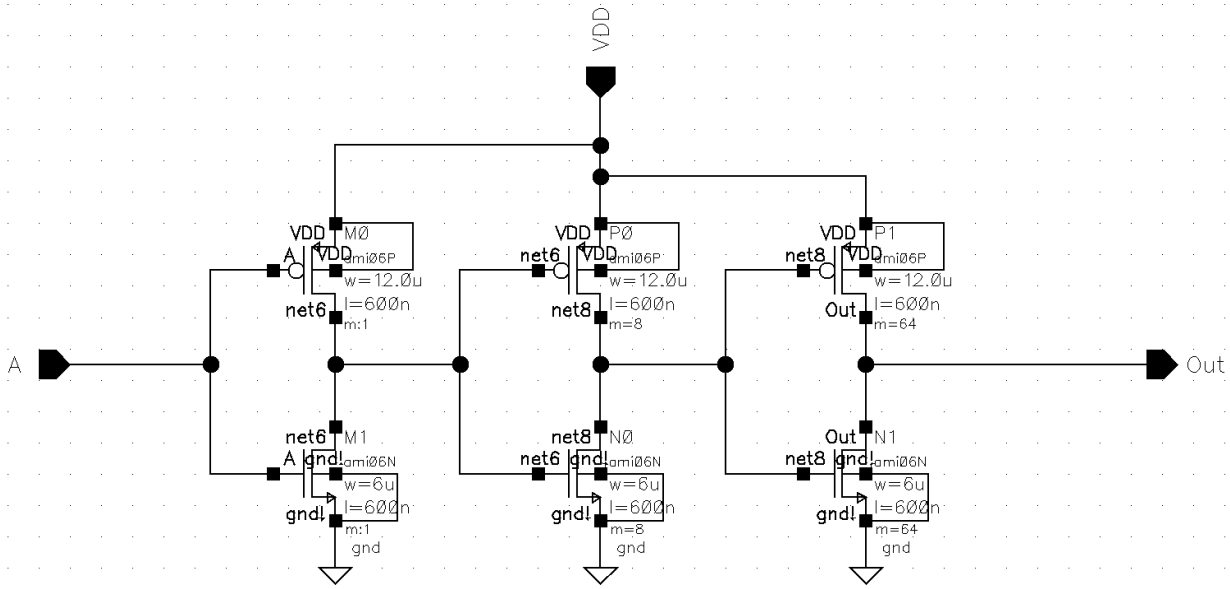

Figure 33 – Schematic for a 3-stage buffer

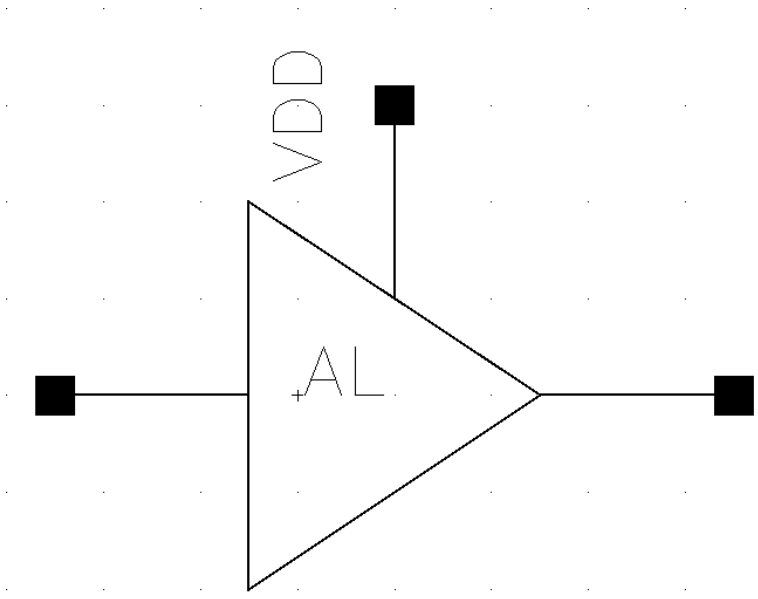

Figure 34 – Symbol for buffer

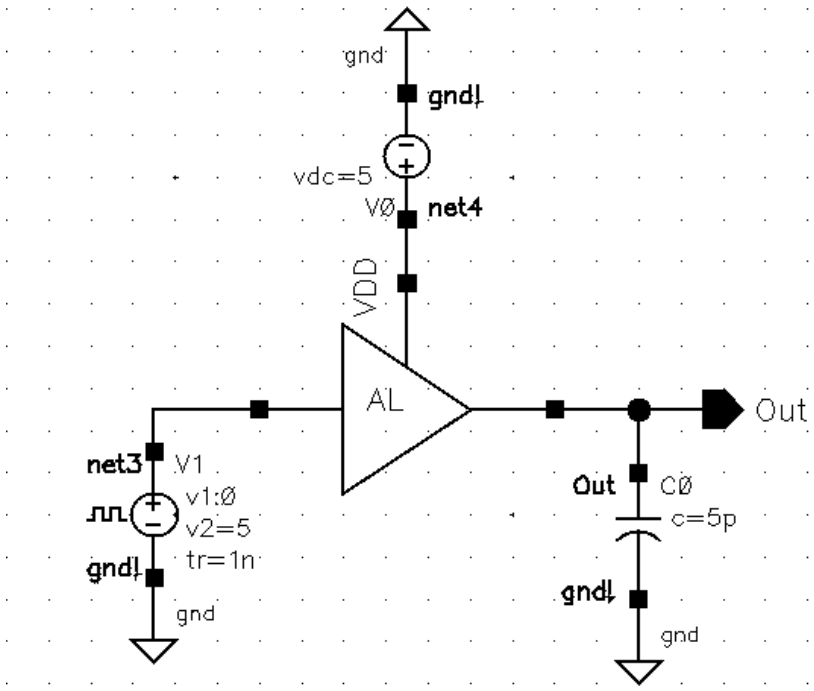

Figure 35 – Simulation circuit for buffer

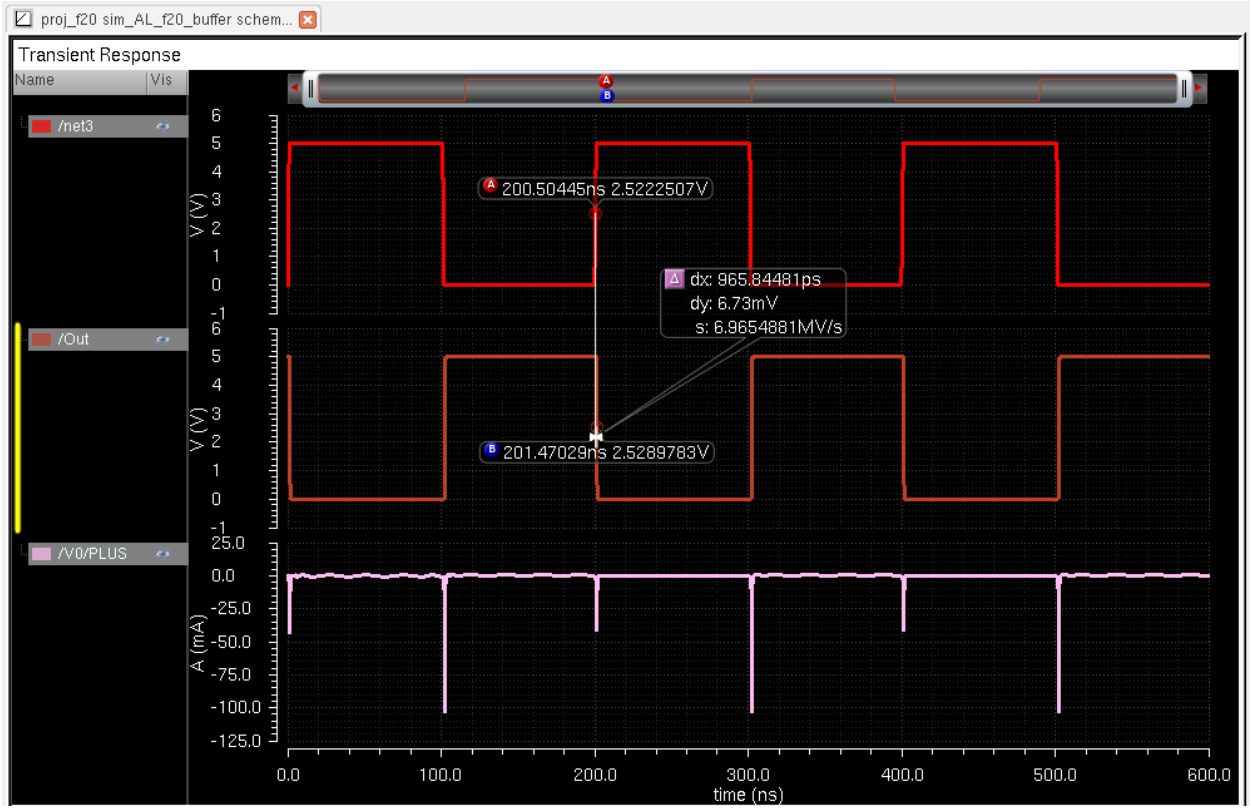

Figure 36 – Buffer simulation results

VDD: 5 V

Load capacitance: 5 pF

Temperature: 27 ˚C

Frequency and Period of input: 5 MHz, 200 ns

Component: Buffer

tpLH	tpHL	Average Power from VDD
966 ps	966 ps	1.643 mW

Table 1: Delay and average power of buffer

From the simulation results (see Figure 37 and table 1) the buffer is able to drive an input signal with a 5 pF load at a frequency of 5 MHz with a time delay for each edge of about 1 ns. Which accomplishes the goal of this design component to drive the signal with little delay.

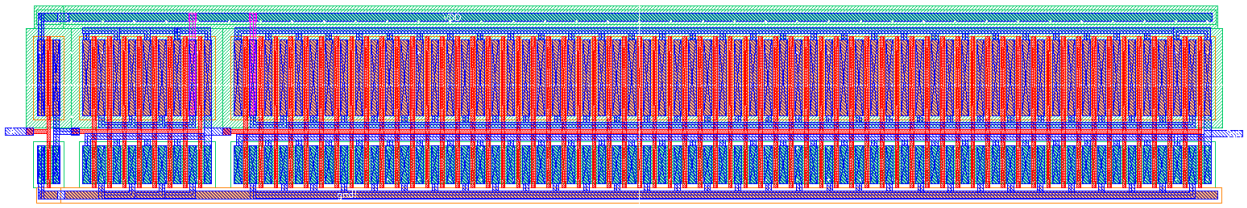

Figure 37 – Layout of buffer

2.2.7 Enabled ring oscillator

Another important part of this design chip is the enabled ring oscillator which gives a self-starting controlled frequency that can regulate the output voltage of the Flyback. For the Flyback to output 12.5 V, the ring oscillator needs to output a signal at a frequency of 5 MHz or with a period of 200 ns. Calculations will need to be done to find the number of inverters to output at this frequency. Also, recall from earlier that for the calculations the size of the inverter being used for the ring oscillator is 7.95 um in width and length. As these values to be large in order, to add a large amount of delay, for the signal to be at 5 MHz.

$$f_{osc} = \frac{1}{N \cdot (t_{PLH} + t_{PHL})}$$

$$t_{PLH} + t_{PHL} = 0.7 \cdot (R_n + R_P) \cdot C_{tot}$$

$$R_n = 20k \cdot \frac{7.95\ um}{7.95\ um} = 20k\ , R_p = 40k \cdot \frac{7.95\ um}{7.95\ um} = 40k$$

$$C_{tot} = \frac{5}{2} \cdot \left(2.5\frac{fF}{um^2} \cdot 7.95\ um \cdot 7.95\ um + 2.5\frac{fF}{um^2} \cdot 7.95\ um \cdot 7.95\ um\right) = 790\ fF$$

$$t_{PHL} + t_{PLH} = 0.7 \cdot 60k \cdot 790fF = 33\ ns$$

$$N = \frac{1}{5\ MHz \cdot 33\ ns} = 6.06$$

For the ring oscillator it was calculated that it would need 6 inverters to achieve the 5 MHz frequency. However, when using this number for the design, it would output a faster frequency in the simulations, so more inverters where added until the desired frequency was achieved where the design has 19 slow inverters (see Figure 38) instead of 6.

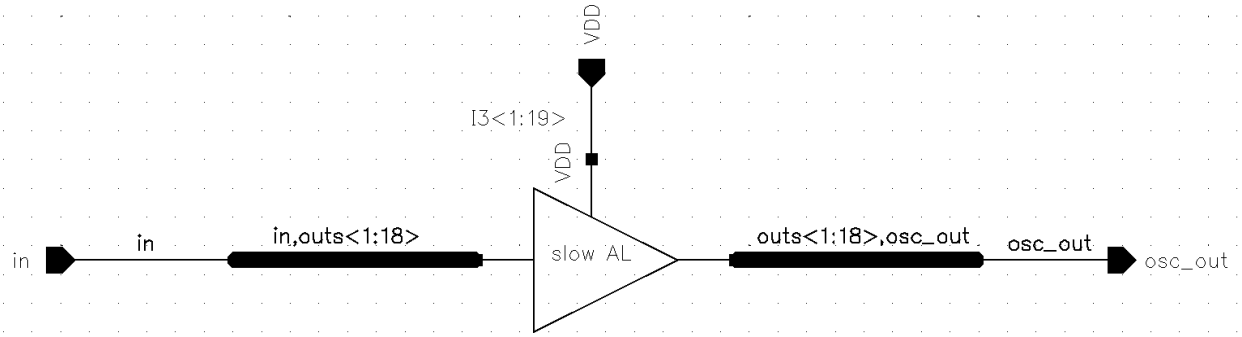

Figure 38 – Schematic for array of slow inverters

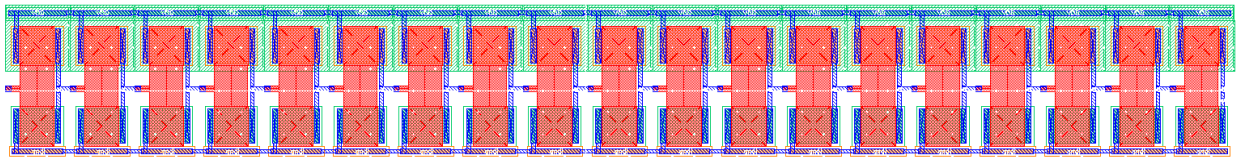

Figure 39 – Layout of slow inverters

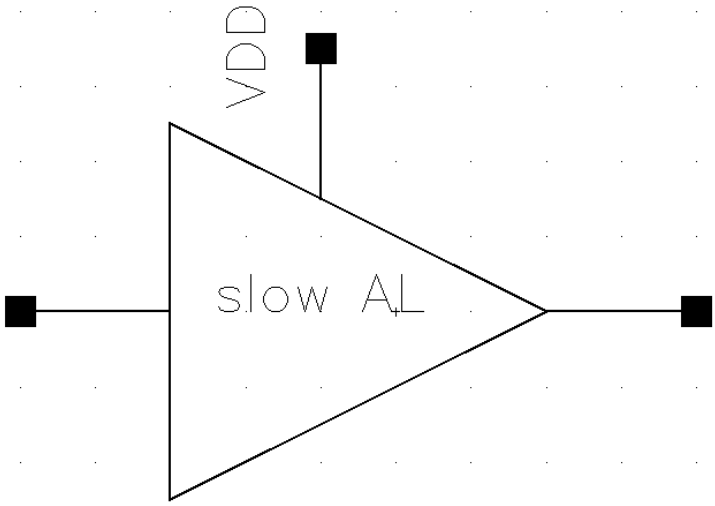

Figure 40 – Symbol for slow inverters

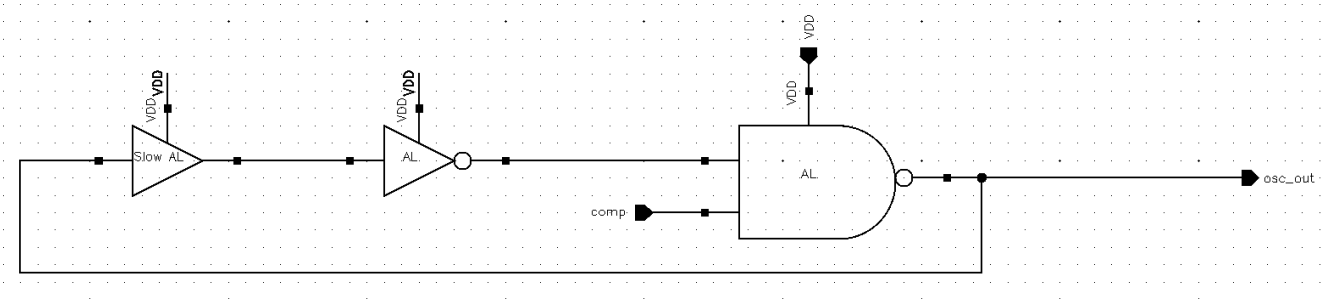

Figure 41 – Schematic for enabled ring oscillator

In Figure 41, the final schematic for the enabled ring oscillator can be seen. Where the array of long inverters first goes through a fast inverter to square up the signal and make the number of inverters in the circuit even, otherwise the design will not work with the NAND gate. Also, the NAND gate is present here to shut of the signal when the voltage of the Flyback is 12.5 V and it is in the front of the inverters to reduce the delay of the signal being turned off and the output feeds back into the inverters. It is important to note that for the simulation and proper operation of this ring oscillator that an initial condition of 0 is needed for the oscillator to start.

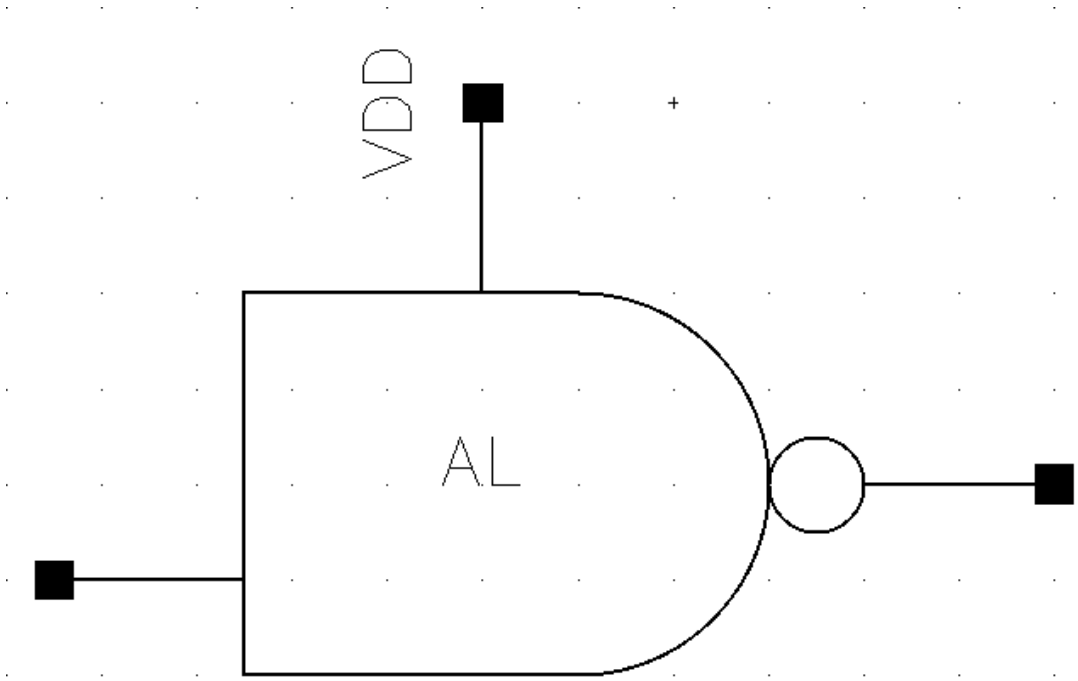

Figure 42 – Symbol for enabled ring oscillator

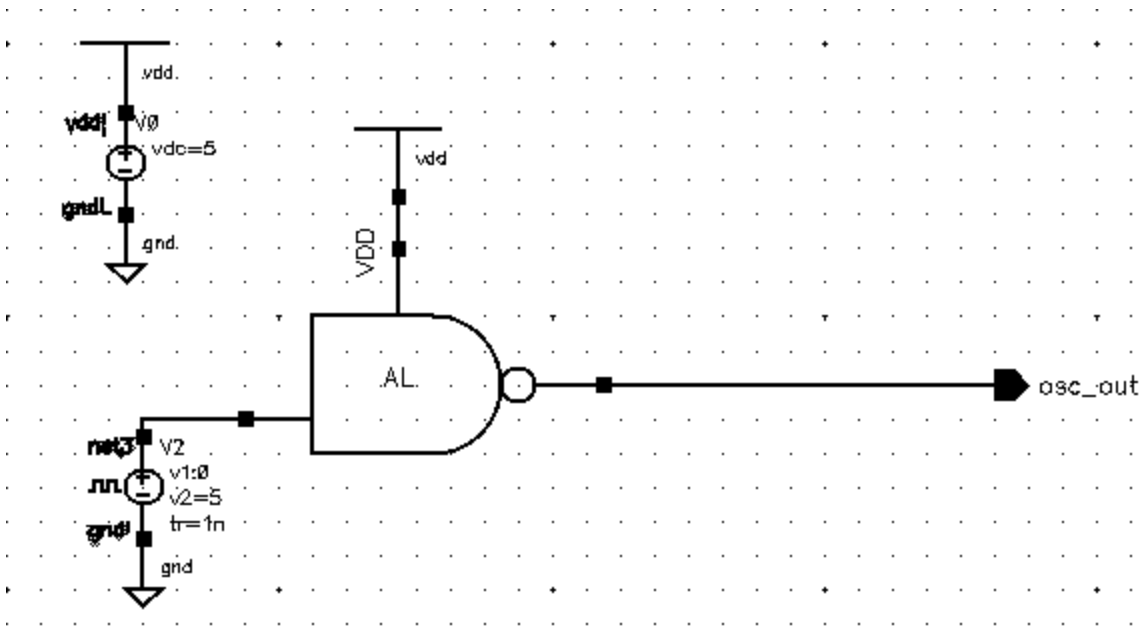

Figure 43 – Simulation circuit for ring oscillator

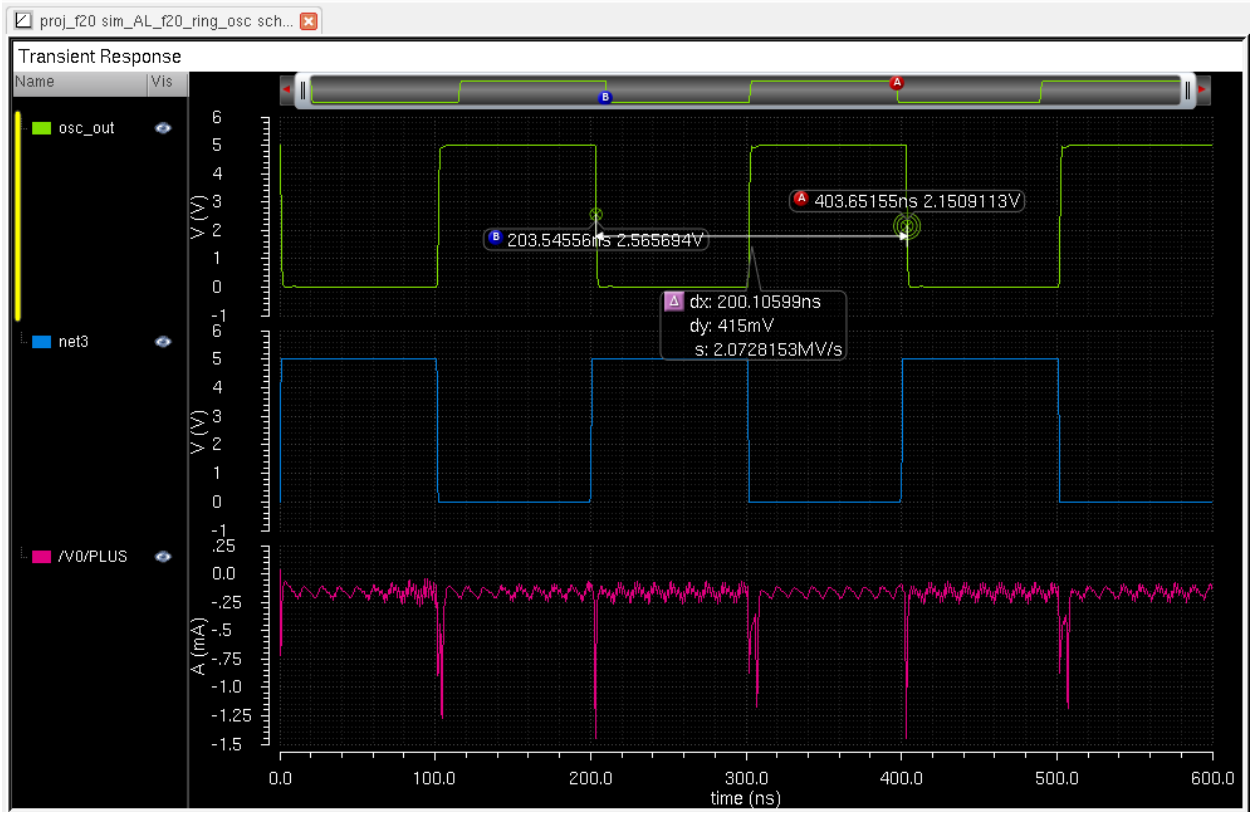

Figure 44 – Results for the ring oscillator

VDD: 5 V

Frequency and Period of input: 5 MHz, 200ns

Initial condition of output: 0

Temperature: 27 ˚C

Frequency and period of output	Average power from VDD	tpLH	tpHL
5 MHz, 200 ns	904.7 uW	686	3 ns

Table 2: Frequency, average power, and delay of ring oscillator

Looking at the simulation, the ring oscillator can output a signal at 5 MHz without drawing a lot of power and without too much delay on the edges.

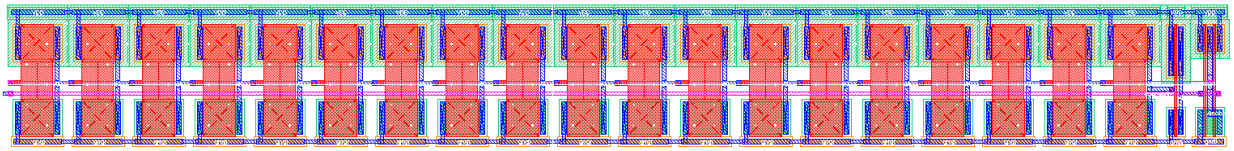

Figure 45 – Layout for enabled ring oscillator

2.2.8 Voltage comparator

The last important part of this design is the voltage comparator which turns on and off the output of the Flyback chip when the voltage is either higher or lower than the voltage reference on the input. For the Flyback to function properly, the comparator needs to be able to detect a small voltage difference between the voltage reference the feedback from the flyback, so it can output a “high” when the feedback volage is lower than the reference and a “low” when it is higher. The voltage difference needs to be 5 mV or lower so the output of the flyback can always stay around 12.5 volts, and to achieve this the gain of the comparator needs to be high. To attain a higher gain the there needs to be multiple differential amplifiers cascaded with each other or put them in series is another way to think of it. For this design 3 p-type diff-amps are cascaded with two inverters to square up the output (see Figure 47) and the p-type topology was chosen for the diff-amp as that topology does much better with lower input voltages. One last important thing to note is that there is a 1/10 voltage divider on the input of the comparator (see Figure 50), so it is important that the amount voltage difference that the comparator can detect is multiplied by a factor of 10 on the output of the Flyback, so in this case the 5 mV difference is actually 50 mV on the output of the Flyback. This is way it is important to have a small voltage difference as a higher has a larger affect on the output of the Flyback.

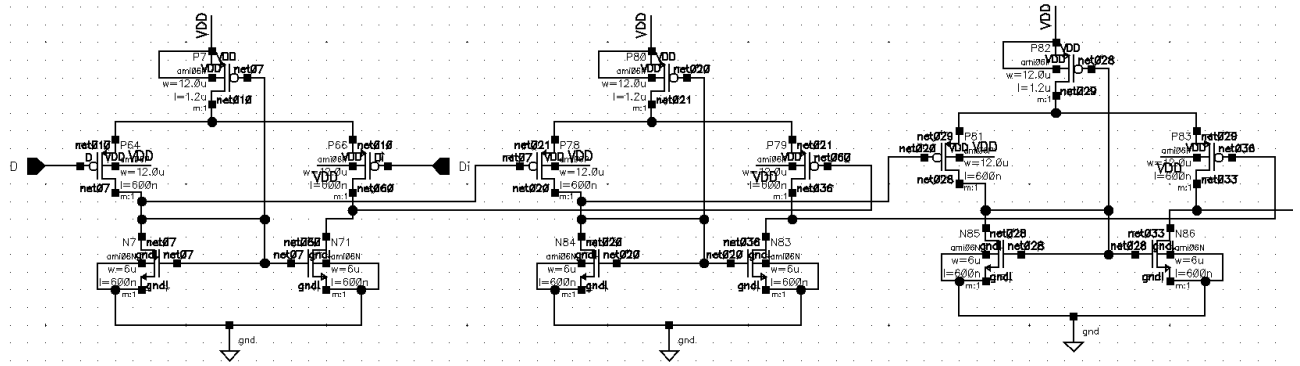

Figure 46 – Three p-type diff-amps cascaded with one another

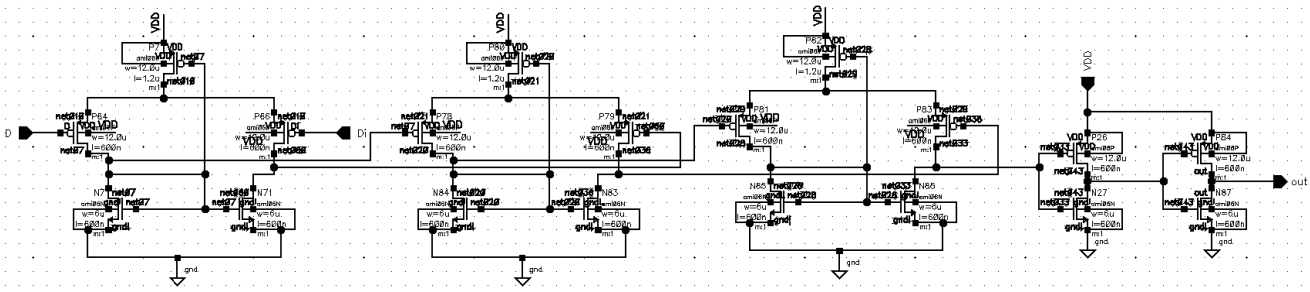

Figure 47 – Schematic of voltage comparator

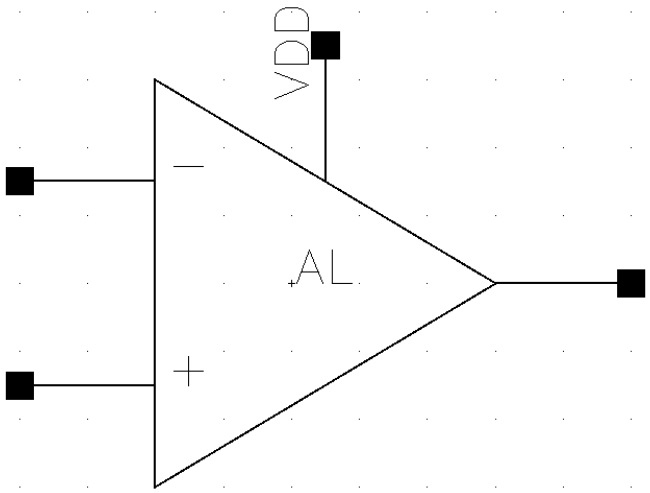

Figure 48 – Symbol for voltage comparator

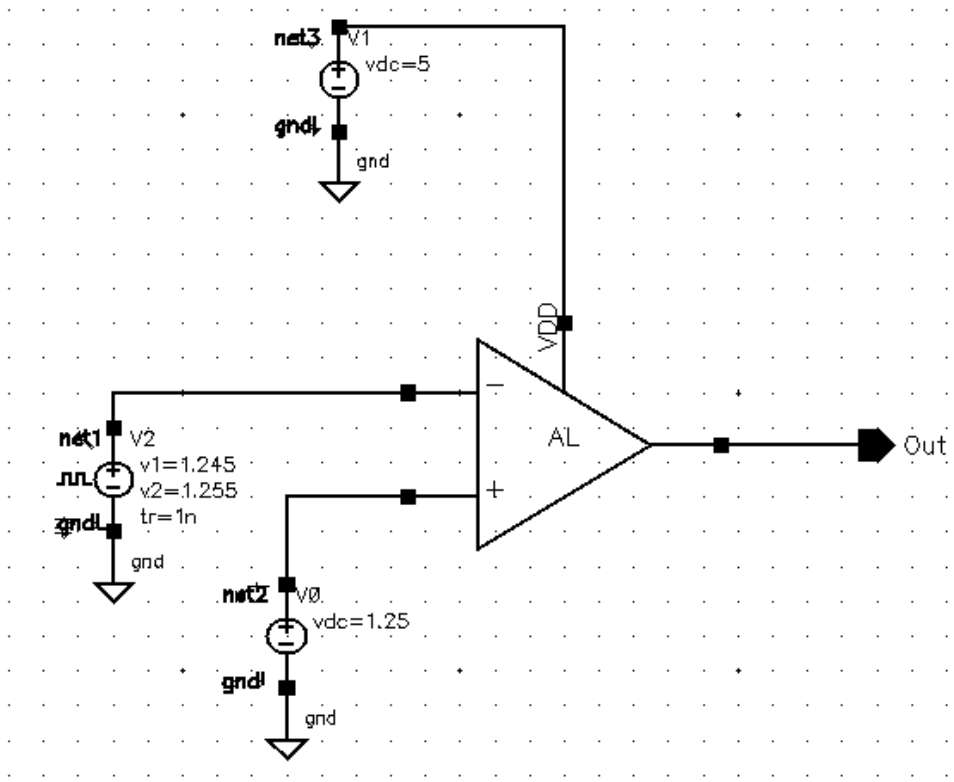

Figure 49 – Simulation circuit for comparator

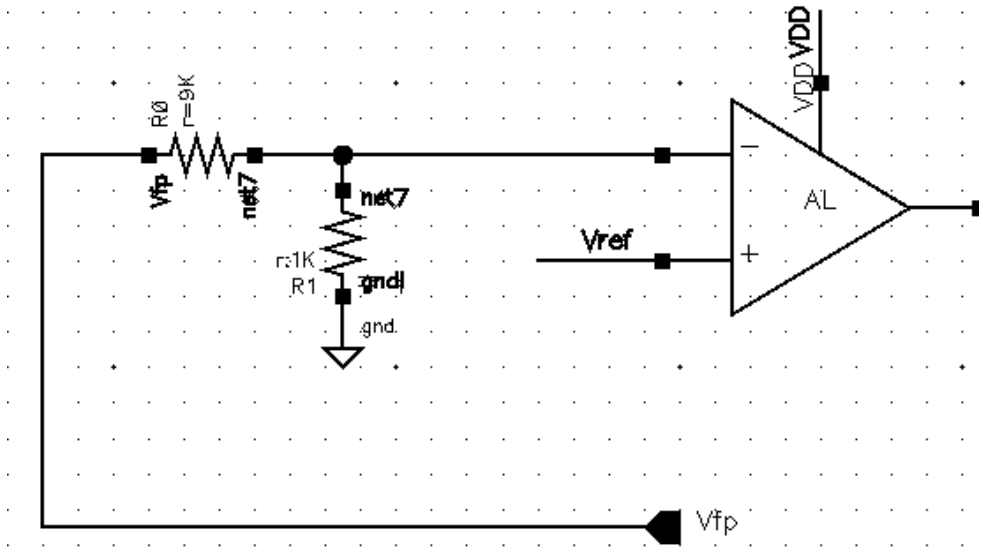

Figure 50 – Voltage divider on input of comparator

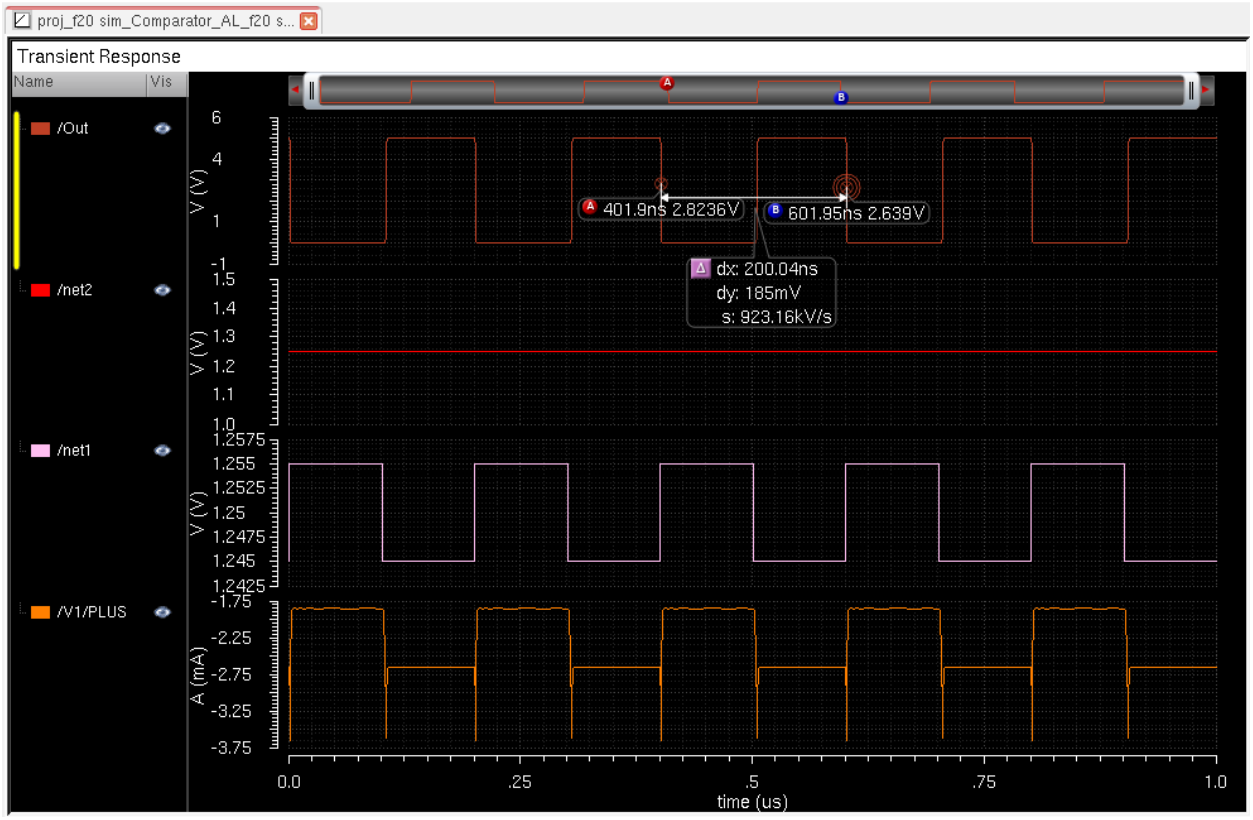

Figure 51 – Simulation results of comparator

VDD: 5 V

Frequency and period of input: 5 MHz, 200 ns

Voltage reference: 1.25 V

Voltage pulse: 1.245 V to 1.255

Hysteresis: 5 mV

Able to output full logic levels?	Average power from VDD	Frequency and period of output
Yes	11.28 mW	5 MHz, 200 ns

Table 3: Ability, average power, and frequency of comparator

The simulation and Table 3 show that the comparator can detect a small voltage difference of 5 mV by outputting a full logic level signal when the inputs change at 5 MHz. Note the average power from VDD is the highest from all the devices mentioned so far in this report, so the comparator is the major point of power consumption for the chip.

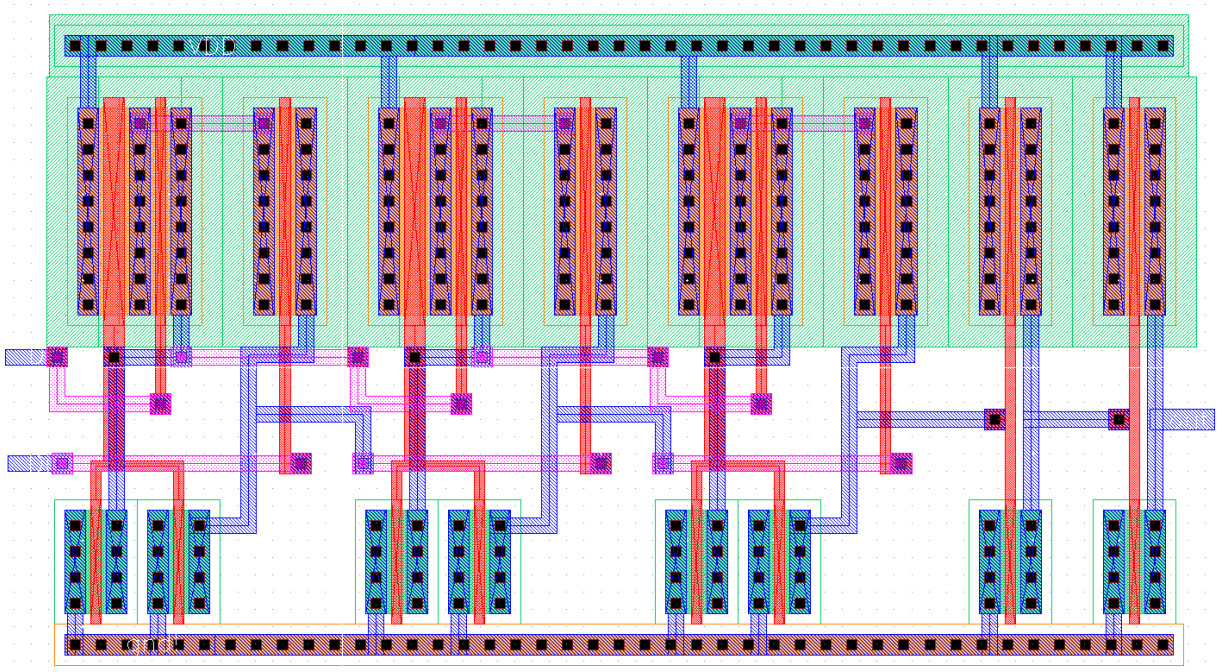

Figure 52 – Layout of voltage comparator

3. Simulation and Performance of Flyback chip at varying VDD, temperature, and load current

3.1 Performance at varying temperatures

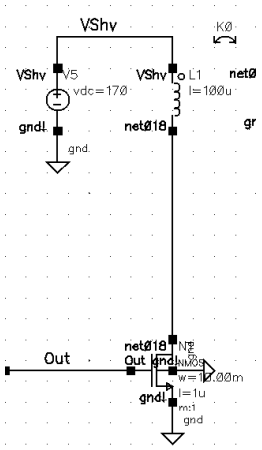

Figure 53 – Current of NMOS coming from 170 V supply

Load current: 1.25 A

Run time: 100 us

VDD: 5 V

Temperature (˚C)	Output voltage	Load current	Ripple voltage	Frequency and period of Out	Average Power from VDD	Average Power from 10m NMOS	Efficiency of circuit
0	12.54 V	1.254 A	~ 89 mV	5.61 MHz, 178 ns	18.72 mW	16.52 W	95.19 %
25	12.53 V	1.253 A	~ 90 mV	4.85 MHz, 206 ns	16.86 mW	16.54 W	94.92 %
50	12.5 V	1.251 A	~ 72 mV	4.20 MHz, 238 ns	15.18 mW	16.42 W	95.23 %
75	12.49 V	1.249 A	~ 69 mV	3.7 MHz, 270 ns	13.61 mW	16.22 W	96.18 %
100	12.46 V	1.246 A	~ 68 mV	3.4 MHz, 296 ns	12.52 mW	16.11 W	96.36 %

Table 4: Summary of chip performance at different temperatures

Some things to note before analyzing the results, the average power from the Flyback was calculated with taking the average current from the power MOSFET instead of the 170 V power supply, because the current from the power supply flows to the Drain of the MOSFET, hence why the calculations were done with that current instead of the power supply. Also, some of

the following calculations were made with the following equations seen below and for clarification V_{out} is the output voltage from table 4.

$$Average\ Power\ from\ VDD = AVG(I(VDD)) \cdot VDD$$

$$Average\ Power\ from\ 10\ m\ NMOS = I\big(AVG(D)\big) \cdot 170V$$

$$Efficiency = \frac{I_{load} \cdot V_{out}}{I(AVG(D)) \cdot 170V}$$

$$I_{load} = \frac{I_{load}}{R_{load}}$$

Looking at the simulations and table 4 it can be concluded that the Flyback can operate at higher temperatures with not much change. However, it should be noted that at 75 to 100 degrees Celsius. The voltage, load current, and frequency start to drop, so it can be inferred if the temperature continues to increase the performance will degrade as a result.

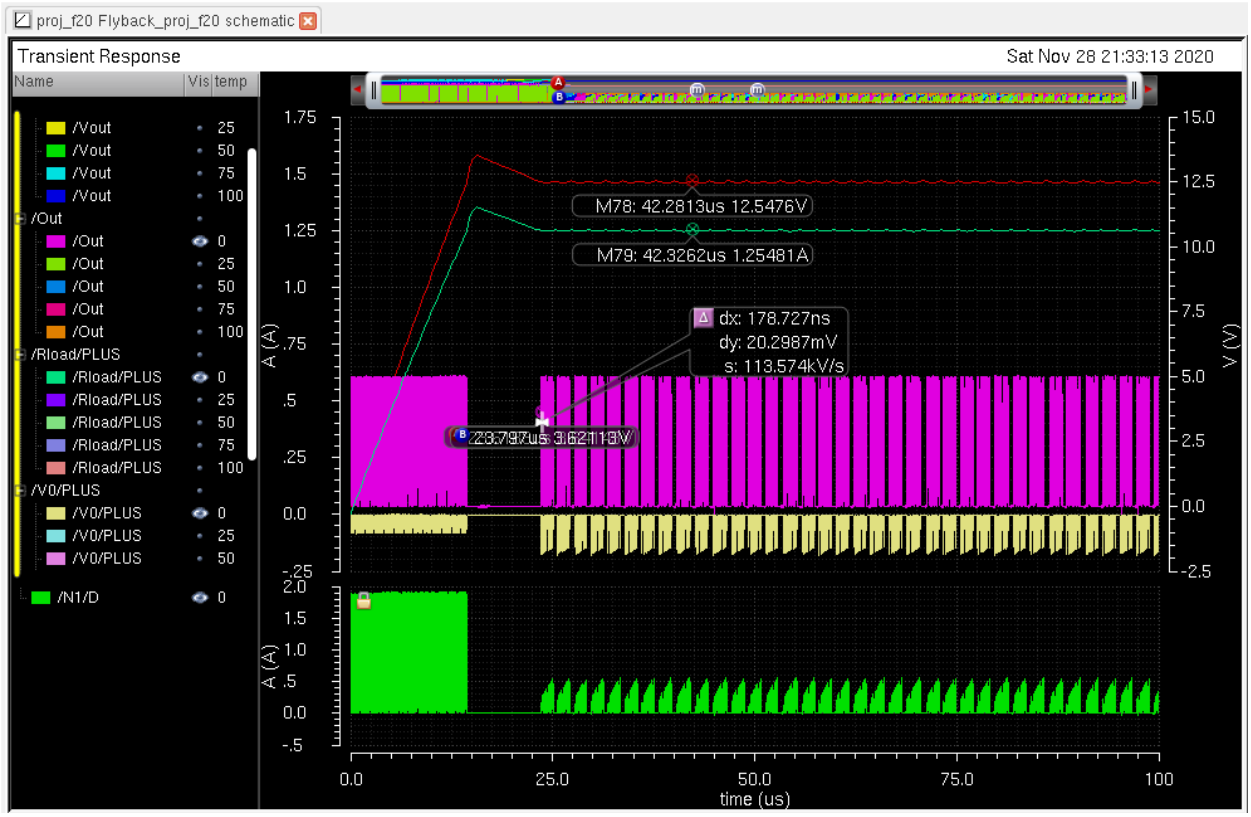

Figure 54 – Temperature at 0 °C

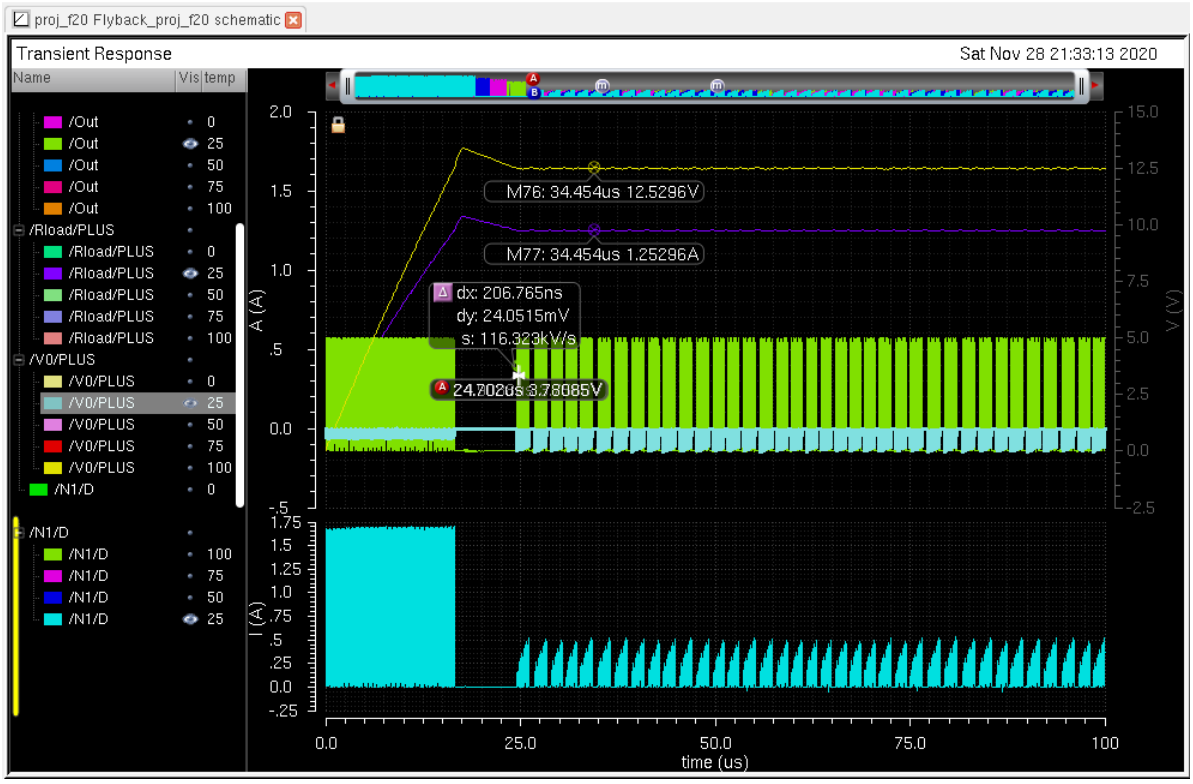

Figure 55 – Temperature at 25 °C

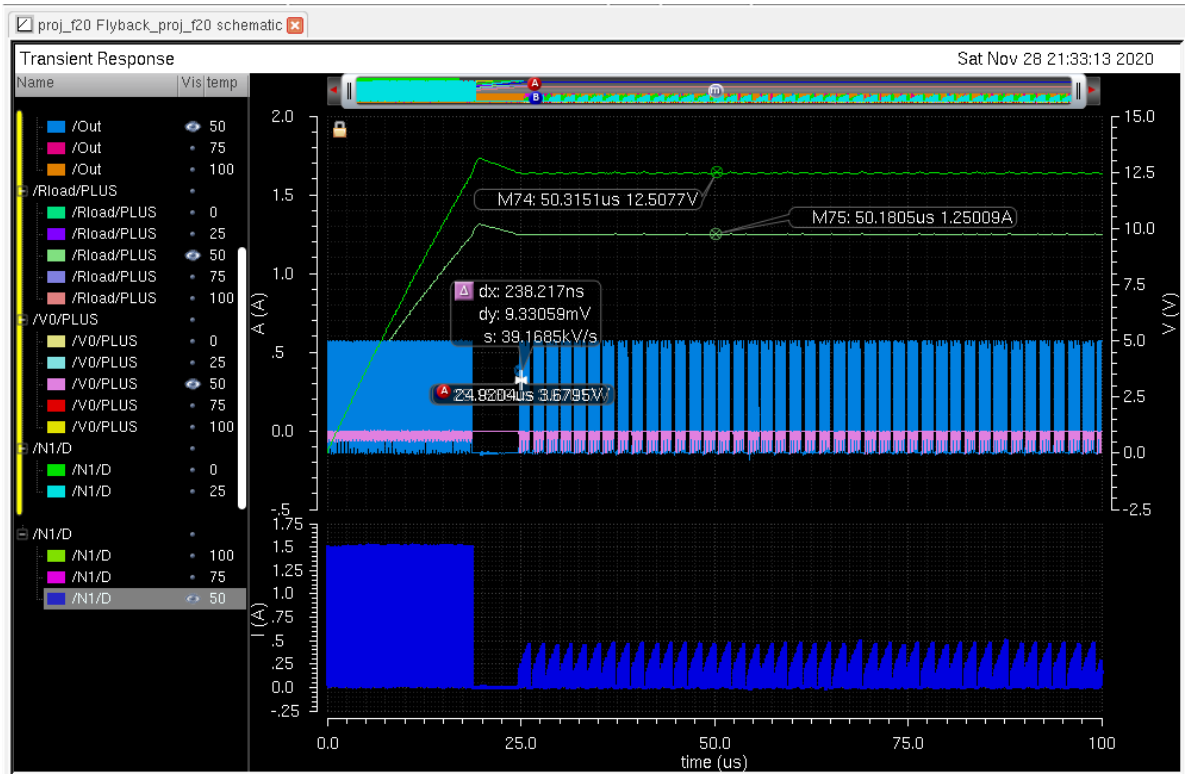

Figure 56 – Temperature at 50 °C

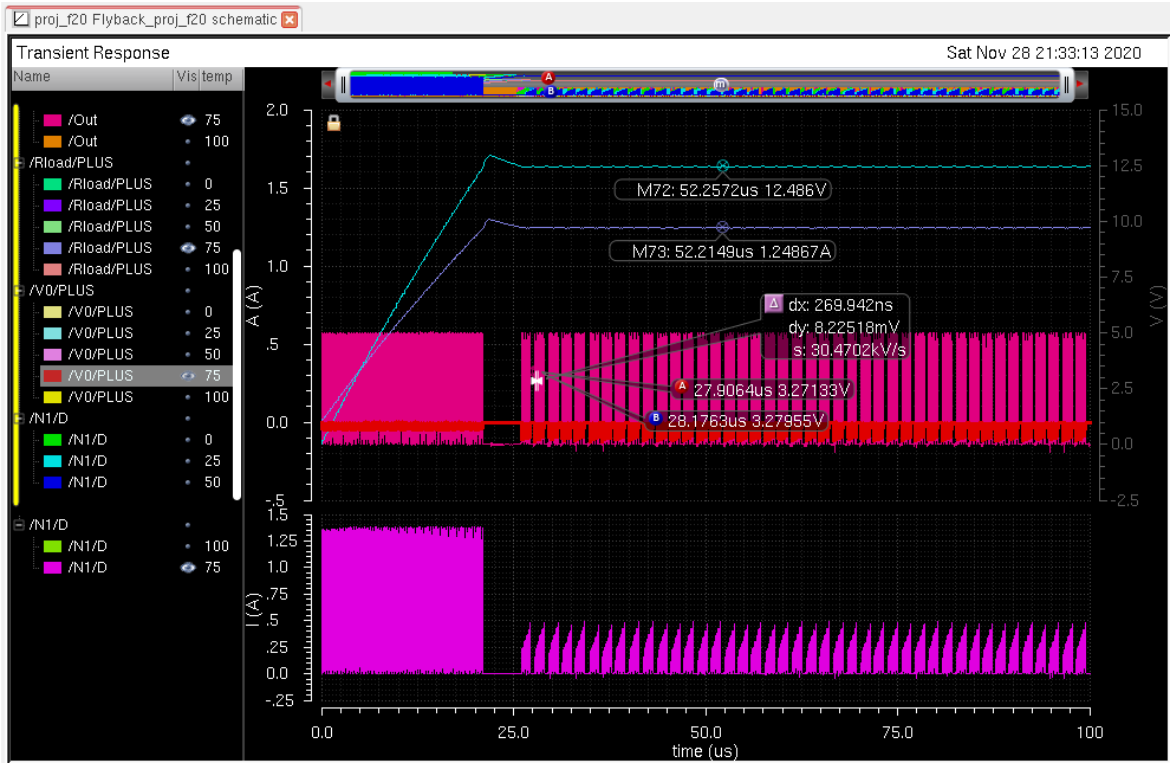

Figure 57 – Temperature at 75 °C

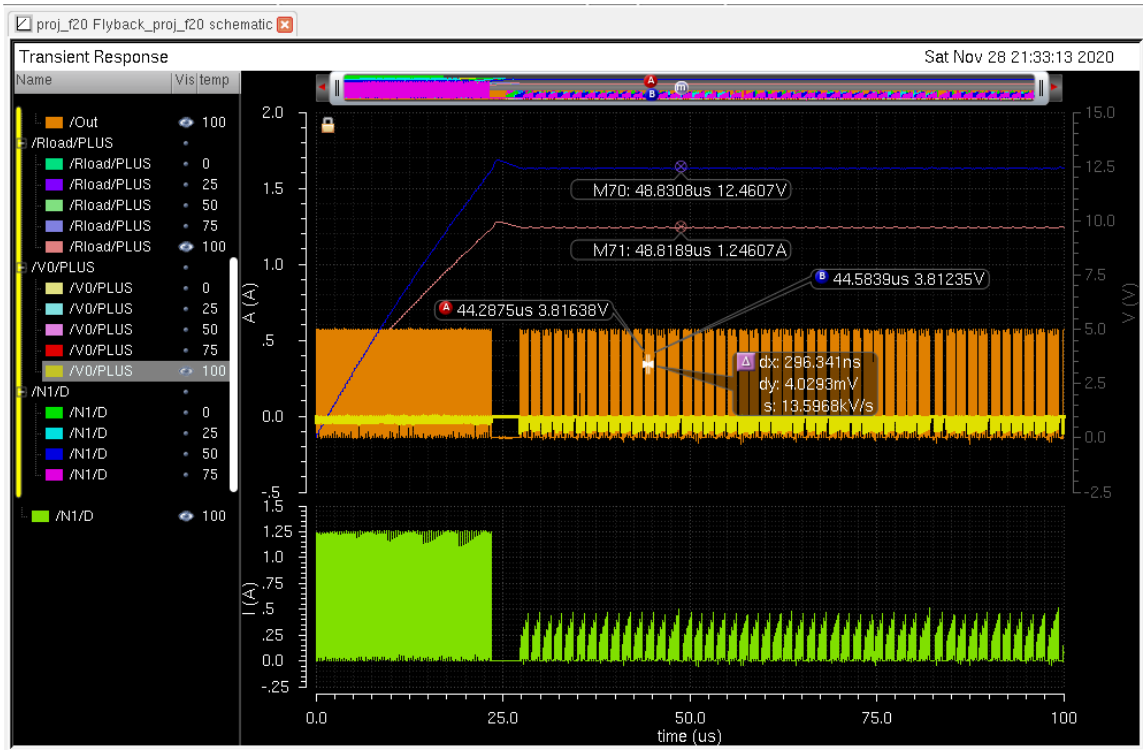

Figure 58 – Temperature at 100 °C

3.2 Performance of chip at varying load currents

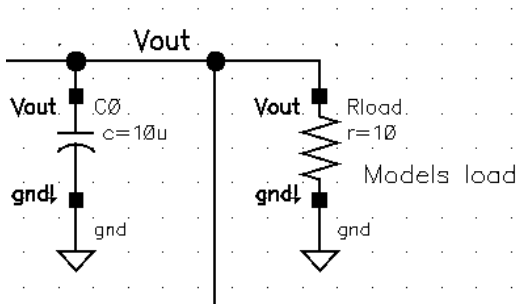

Figure 59 – Changing resistive load to change load current

Temperature: 27 ˚C

VDD: 5 V

Load Current	Output voltage	Ripple voltage	Frequency and period of Out	Average Power from VDD	Average power from 10m NMOS	Efficiency of circuit	Run time
0.0000125 uA (near 0)	12.51 V	~ 14.5 mV	8.6 kHz, 116000 ns	14.39 mW	17.37 mW	0.009 %	10 ms
10 mA	12.51 V	~ 14.2 mV	77.4 kHz, 12920 ns	14.58 mW	150.4 mW	83.18 %	1 ms
100 mA	12.50 V	~ 10.9 mV	749 kHz, 1335 ns	15.86 mW	1.311 W	95.35 %	500 us
200 mA	12.50 V	~ 10.8 mV	1.52 MHz, 656 ns	16.88 mW	2.636 W	94.84 %	500 us
250 mA	12.50 V	~ 11.5 mV	1.9 MHz, 519.9 ns	17.40 mW	3.239 W	96.48 %	100 us
1.25 A	12.53 V	~ 81 mV	4.78 MHz, 209 ns	16.61 mW	16.32 W	95.97 %	100 us
2 A	12.56 V	~ 216 mV	4.76 MHz, 209.8 ns	15.61 mW	26.67 W	94.19 %	100 us
2.5 A	12.64 V	~ 344 mV	4.76 MHz, 210 ns	15.23 mW	33.12 W	95.41 %	100 us
6.25 A	12.83 V	~ 1.58 V	4.76 MHz, 210 ns	14.49 mW	91.06 W	88.06 %	500 us
8 A	8.1 V	~ 84 mV	4.81 MHz, 208 ns	12.63 mW	141.2 W	45.89 %	500 us

Table 5: Performance of chip at varying load currents

Note in Figure 59, changing the load current means changing the value of the resistive load in the circuit where the load current is the output voltage divided by the resistive load. The Flyback for 0 to 2 A of load current can output the 12.5 V that is required of the circuit, and

maintaining a high efficiency as the load changes, expect for of course a load of near zero where there is no dissipation, hence an efficiency near zero. However, it seems that the circuit cannot output more than 8 A of current and if it does do this it comes at a cost of the voltage dropping significantly and dissipating a large amount of power which affects the efficiency greatly. At cases of 2.5 and 6.25 A of load the still performs decently albeit with an increase in the output voltage and increased ripple, but still at a high efficiency. Last thing to note at lower load current the frequency of the output starts to decrease as there is less change within the output voltage, hence the power MOSFET is being turned on and off for a greater amount of time. One more thing note the run time section as certain load currents look longer for the circuit to actually move past the initial charge phase of the power MOSFET, for example at a load of near zero load current it took a simulation time of 10 ms for the circuit to reach steady state. Also, notice that as the load current increases so does the ripple voltage and it decreases when lowered.

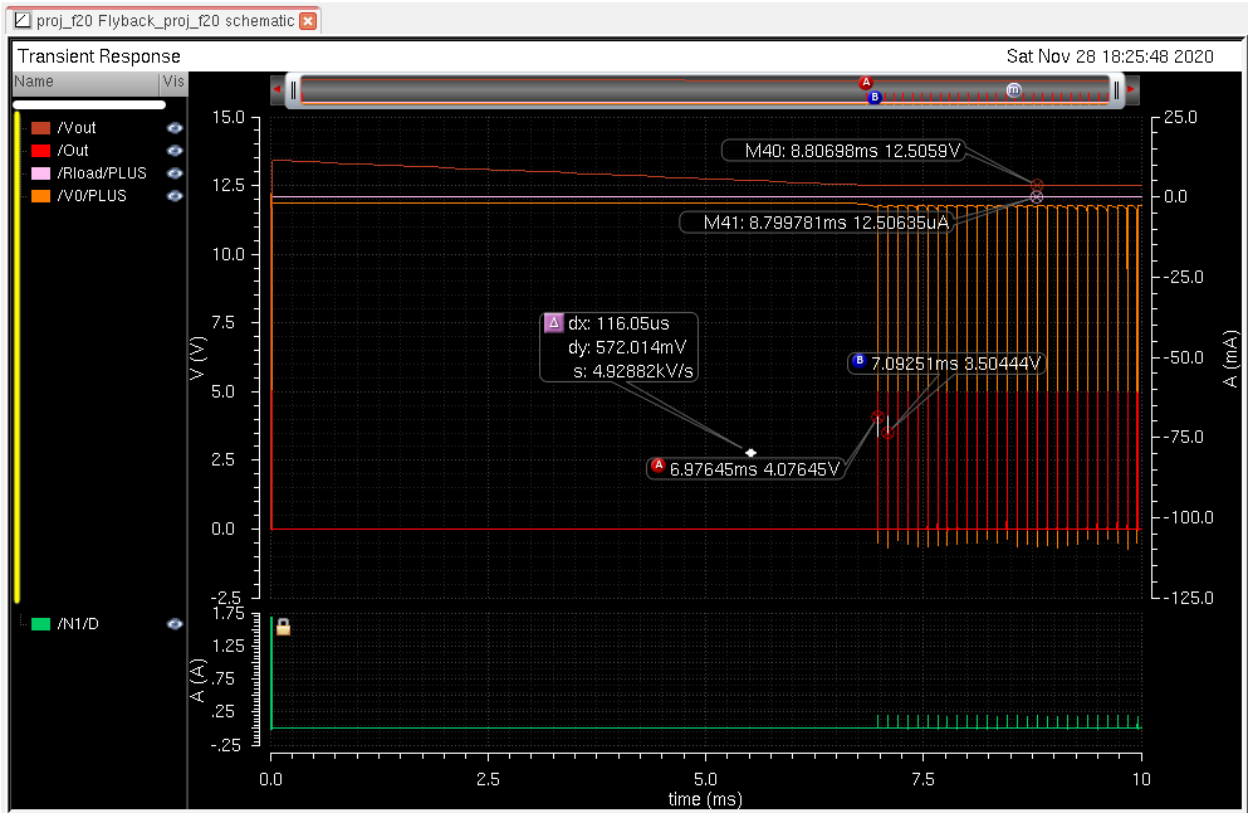

Figure 60 – Load current of 0.000125 uA

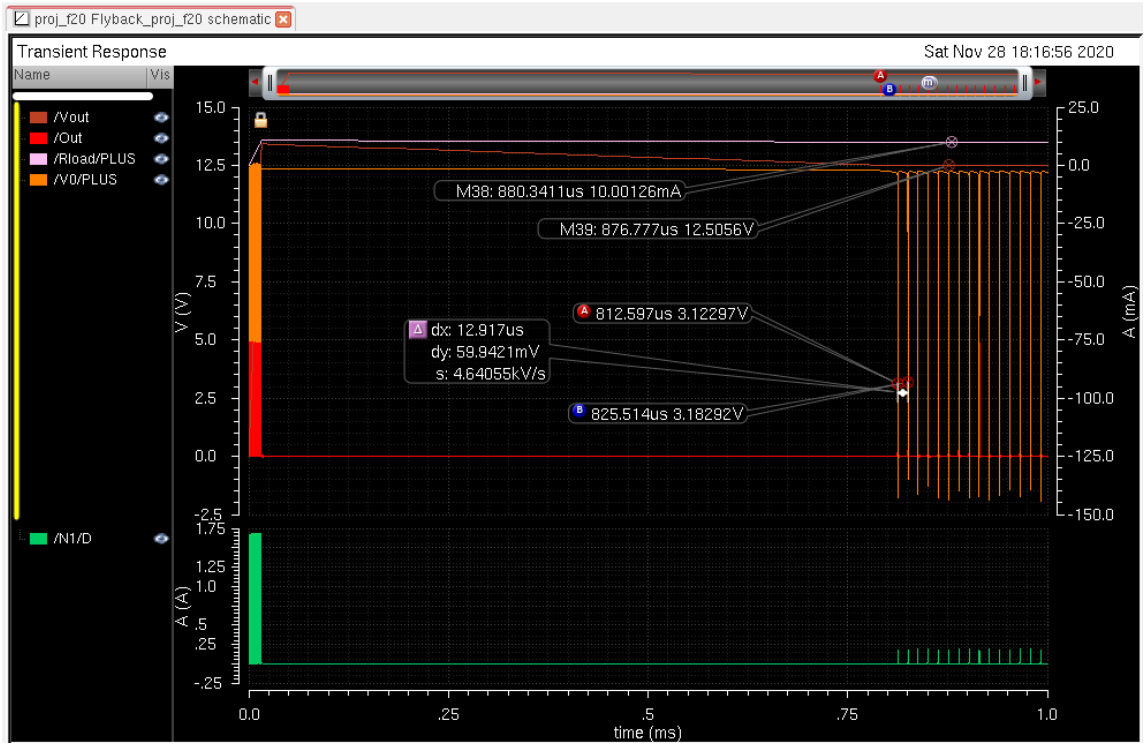

Figure 61 – Load current of 10 mA

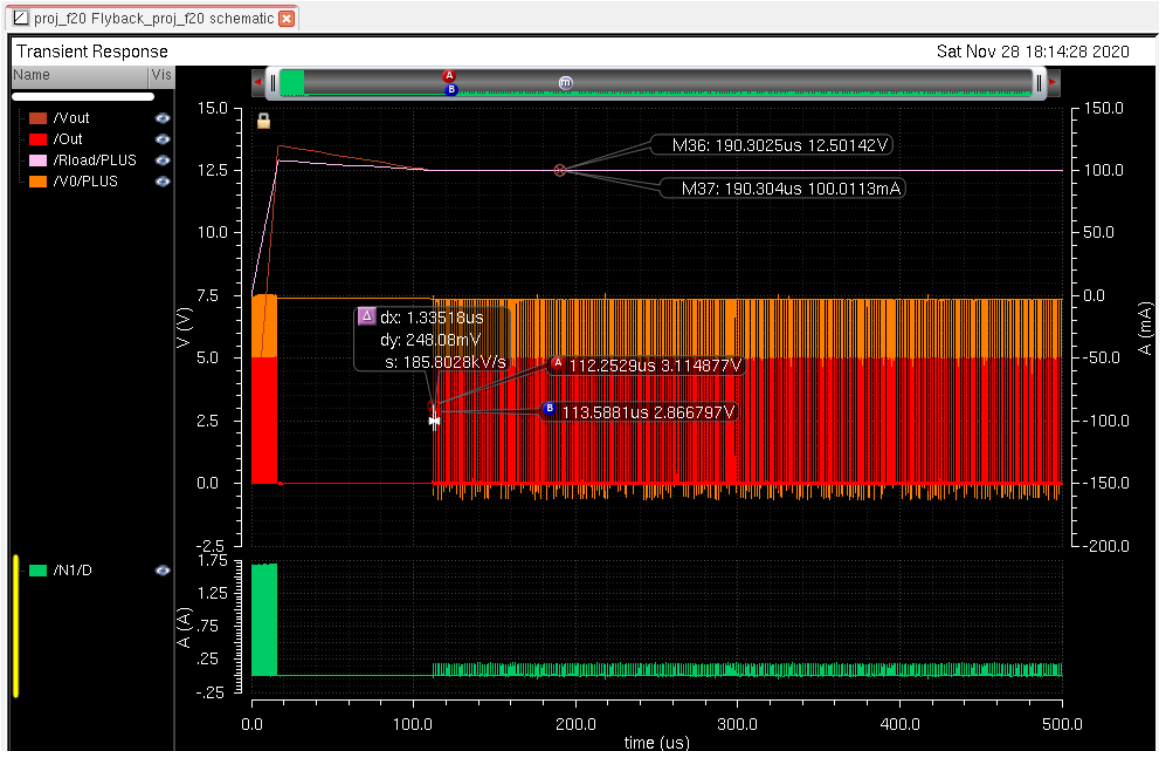

Figure 62 – Load current of 100 mA

Figure 63 – Load current of 200 mA

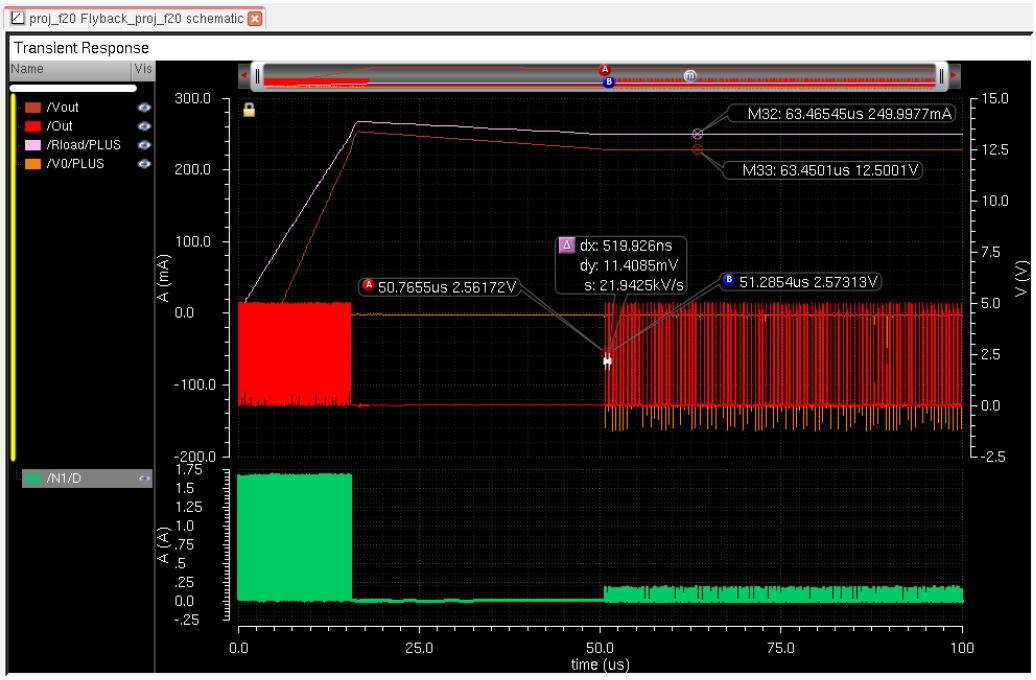

Figure 64 – Load current of 250 mA

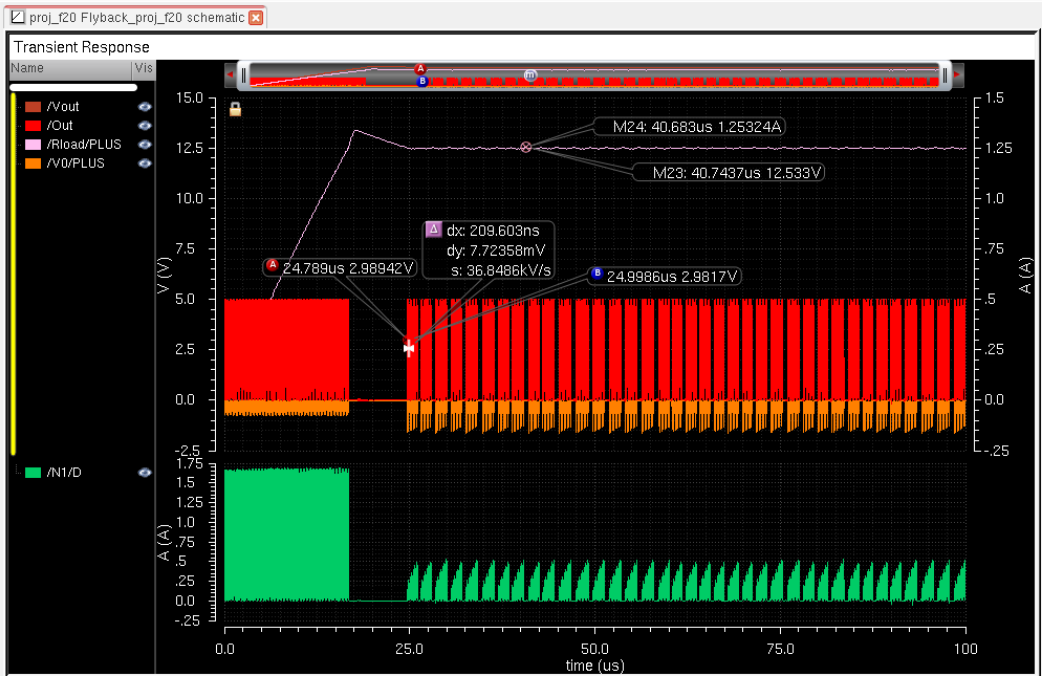

Figure 65 – Load current of 1.25 A

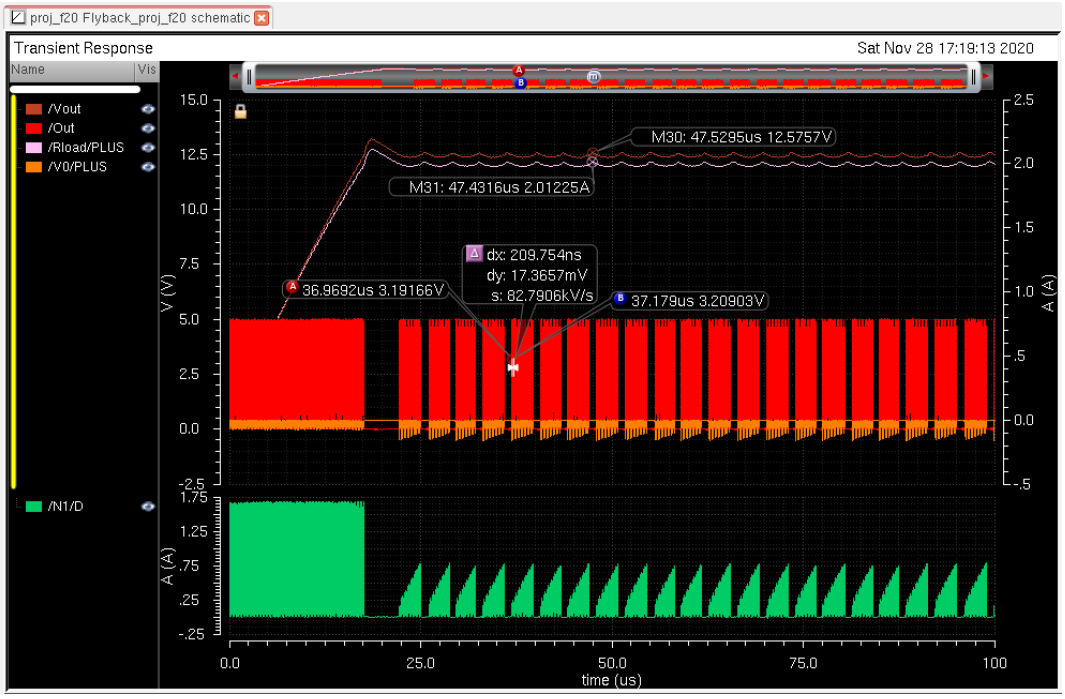

Figure 66 – Load current of 2 A

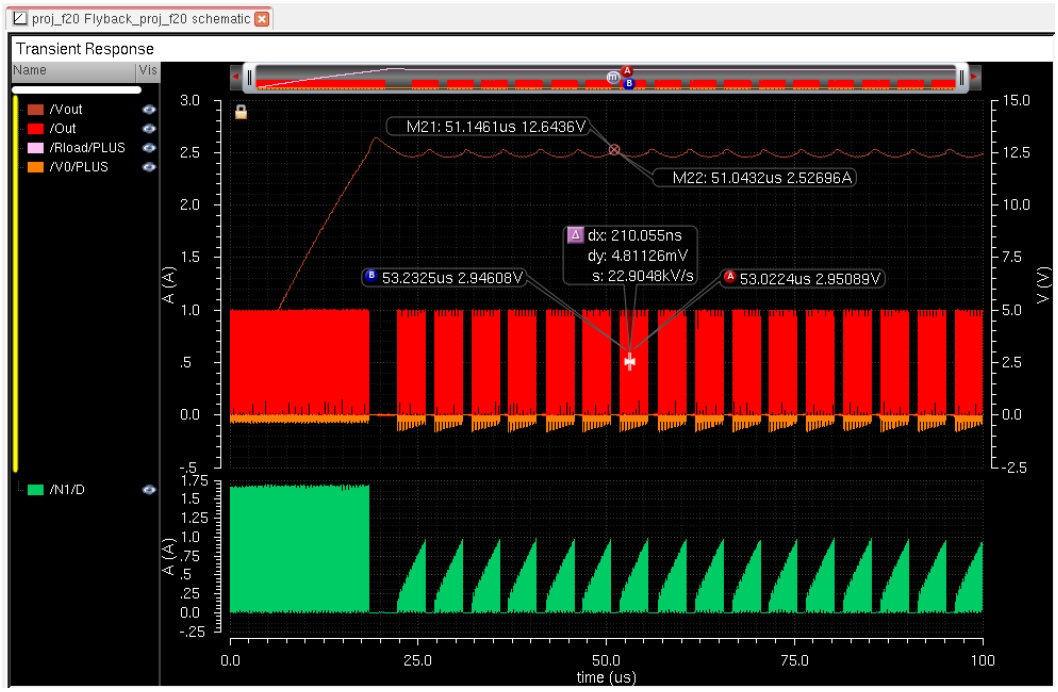

Figure 67 – Load current of 2.5 A

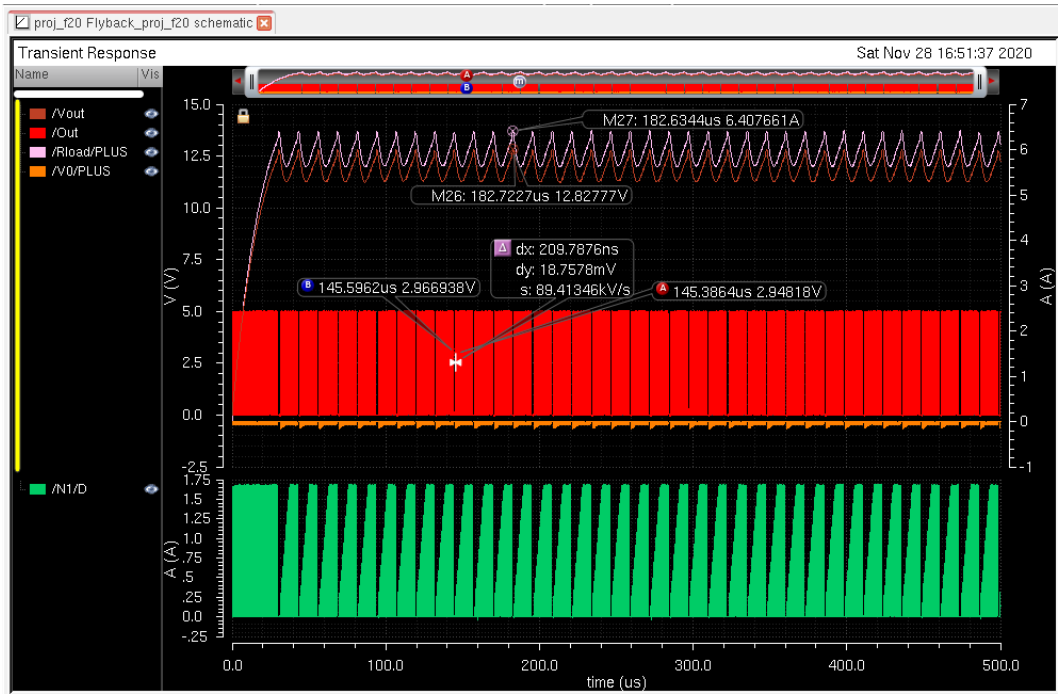

Figure 68 – Load current of 6.25 A

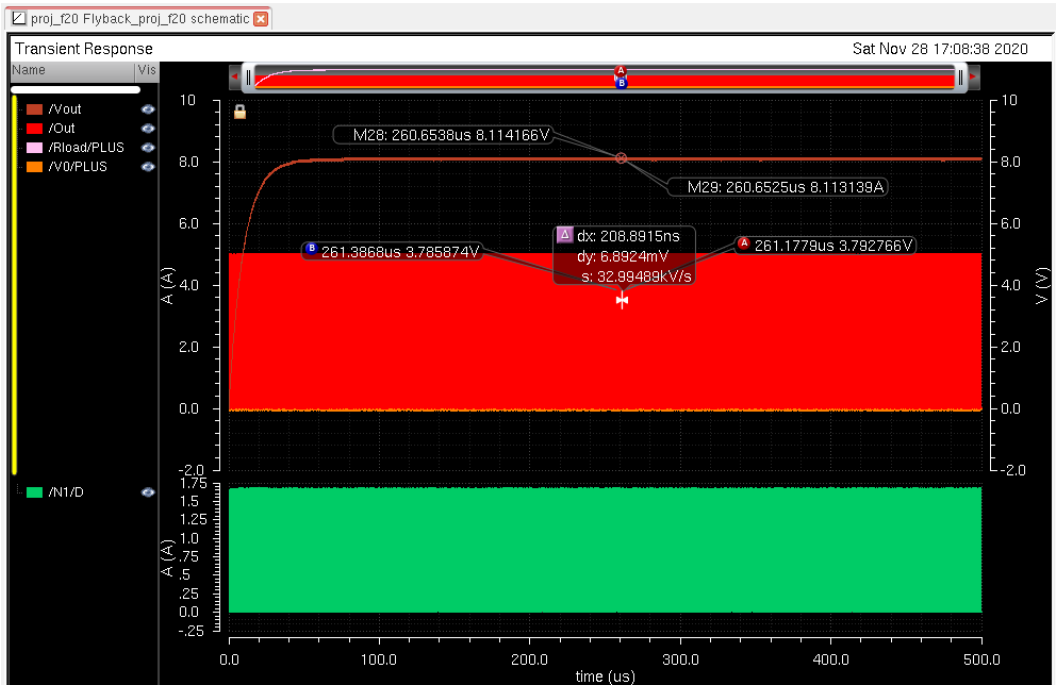

Figure 69 – Load current of 8 A

3.3 Performance of Flyback at varying VDD

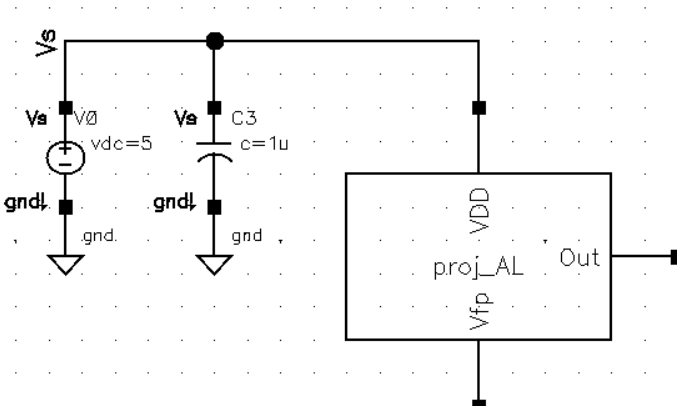

Figure 70 – Current taken from Vs supply

Load current: 1.25 A

Temperature: 27 ˚C

VDD	Output voltage	Load current	Ripple voltage	Frequency and period of Out	Average power from VDD supply	Average power from 10 m NMOS	Efficiency of circuit	Run time
3 V	11.21 V	1.121 A	~ 46 mV	2.54 MHz, 393 ns	1.66 mW	31.53 W	39.85 %	500 us
3.5 V	12.26 V	1.226 A	~ 61 mV	3.16 MHz, 316.8 ns	3.76 mW	28.06 W	53.56 %	100 us
3.75 V	12.50 V	1.25 A	~ 75 mV	3.45 MHz, 290 ns	5.30 mW	24.05 W	64.96 %	100 us
4 V	12.50 V	1.25 A	~ 64 mV	3.71 MHz, 269.9 ns	7.1 mW	18.58 W	84.09 %	100 us
4.25 V	12.51 V	1.251 A	~ 72 mV	4 MHz, 250 ns	9.26 mW	16.31 W	95.95 %	100 us
4.5 V	12.51 V	1.251 A	~ 61 mV	4.27 MHz, 234 ns	11.32 mW	16.39 W	95.49 %	100 us
4.75 V	12.52 V	1.251 A	~ 71 mV	4.54 MHz, 220 ns	13.88 mW	16.31 W	96.0 %	100 us
5 V	12.52 V	1.252 A	~ 81 mV	4.78 MHz, 209 ns	16.63 mW	16.33 W	95.98 %	100 us
5.25 V	12.53 V	1.253 A	~ 79 mV	5.01 MHz, 199 ns	19.93 mW	16.43 W	95.56 %	100 us
5.5 V	12.53 V	1.252 A	~ 78 mV	5.24 MHz, 191 ns	23.32 mW	16.24 W	96.59 %	100 us

Table 6: Performance of chip at varying VDD

Looking at the simulations and table 6 the Flyback can keep the voltage and load the current at their desired values until VDD is at 3.75 V. Which makes sense since the bandgap stop working when the VDD voltage is 3.6 V. However, looking at the performance for 3.75 V and 4 V the frequency and efficiency for the circuit drops significantly, so it would be best to rule out those as operating voltages. Seeing the performance for 4.25 V and 4.5 V the circuit seems to perform well, but yet looking at the frequency it drops, meaning the circuit has to use more power in order to keep the output voltage and load current the same, so again best to rule them out as operating voltages. Looking at the rest of the operating voltages it can be concluded that the Flyback works best under the operating voltages of 4.75 V to 5.5 V, as the efficiency is high, average power used is lower, frequency stays close enough to 5 MHz, and the output voltage and current remain constant. One last note, in Figure 70 for clarification the average current is taken from Vs power supply when calculating the average power from VDD.

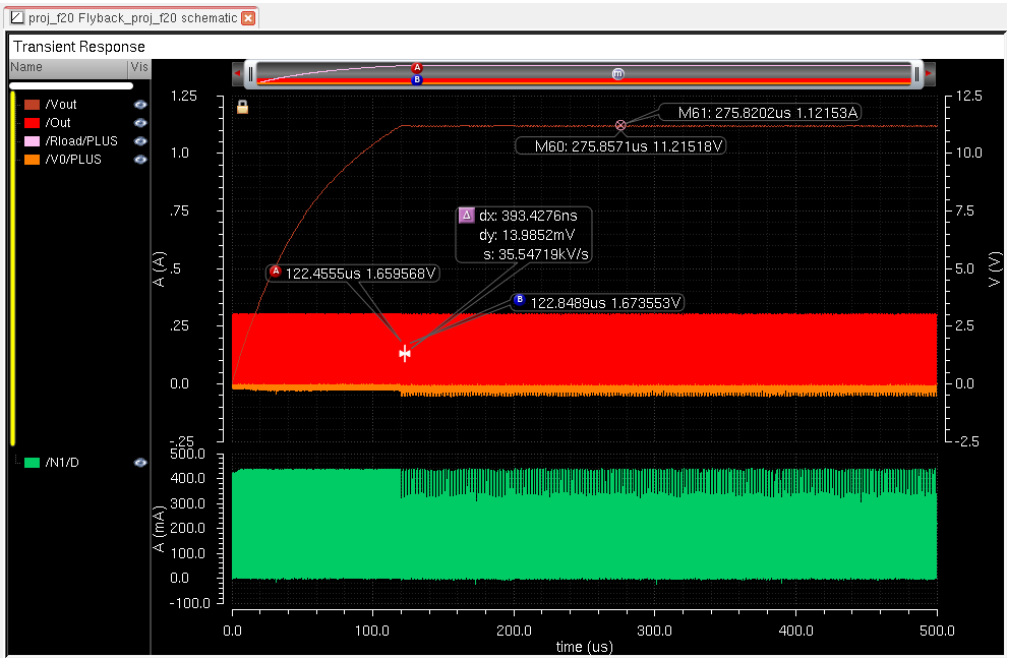

Figure 71 – VDD at 3 V

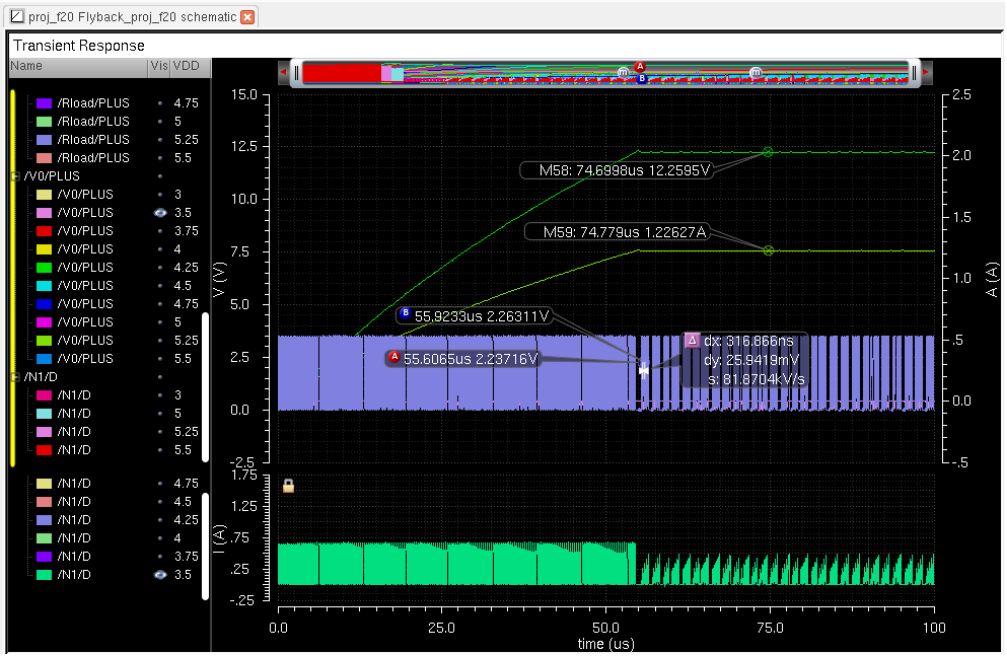

Figure 72 – VDD at 3.5 V

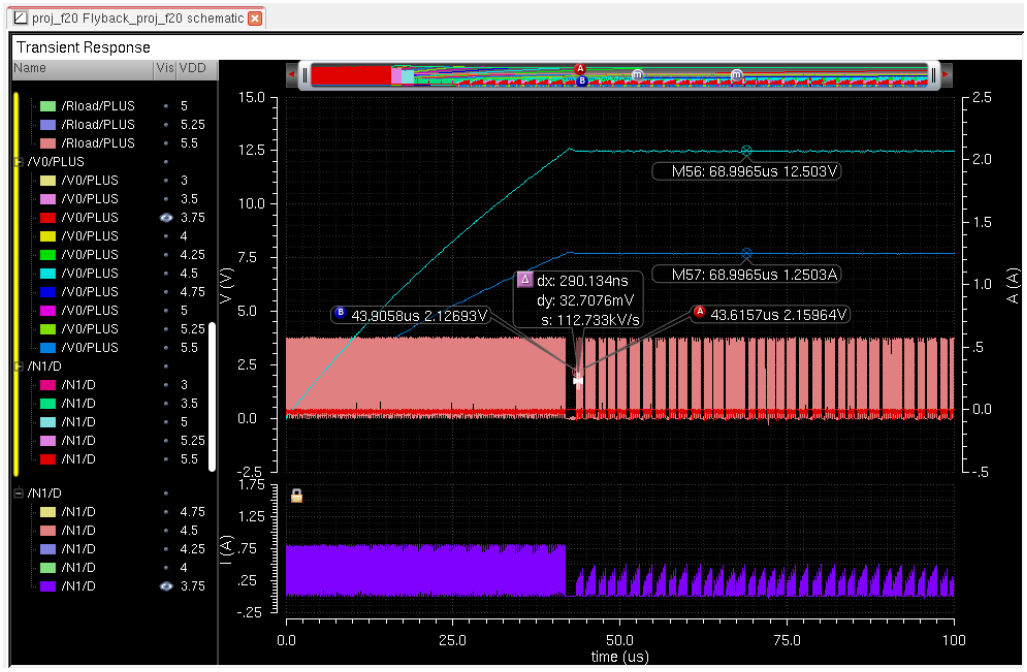

Figure 73 – VDD at 3.75 V

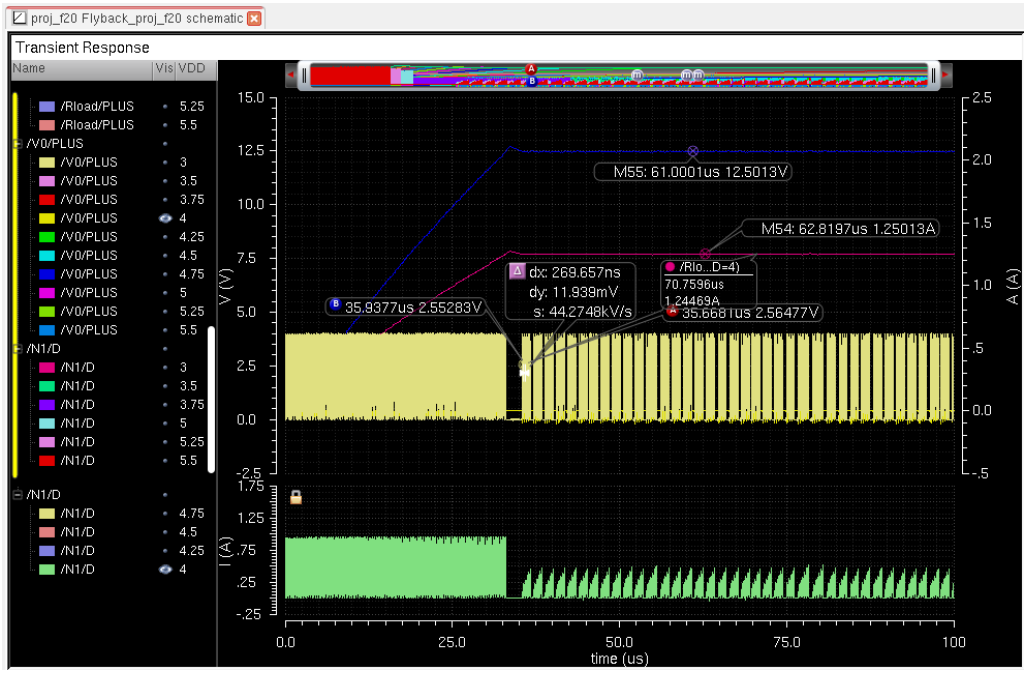

Figure 74 – VDD at 4 V

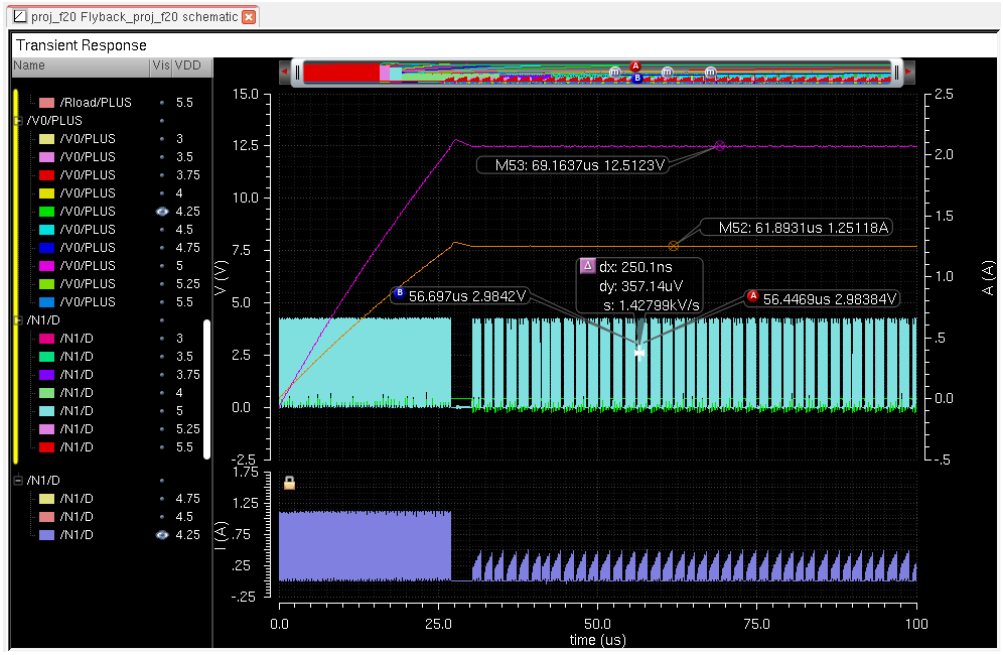

Figure 75 – VDD at 4.25 V

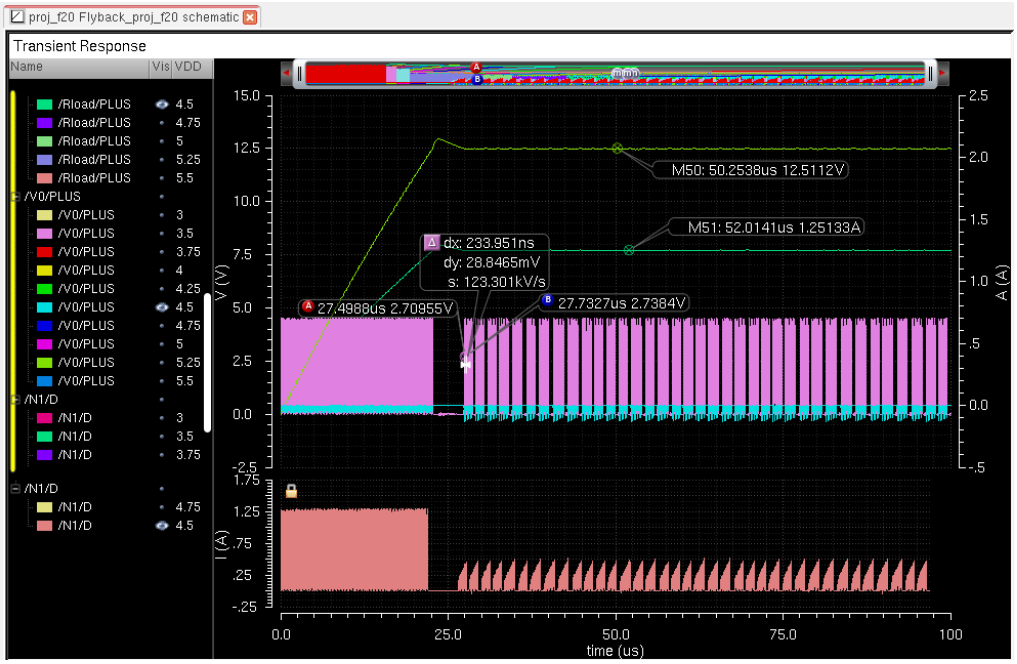

Figure 76 – VDD at 4.5 V

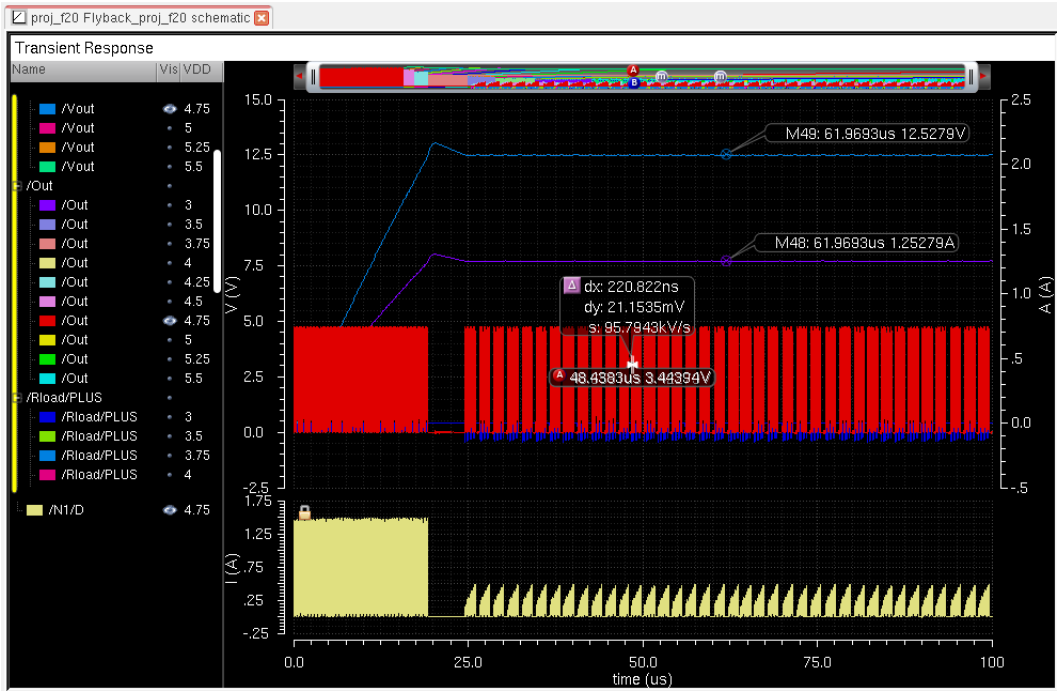

Figure 77 – VDD at 4.75 V

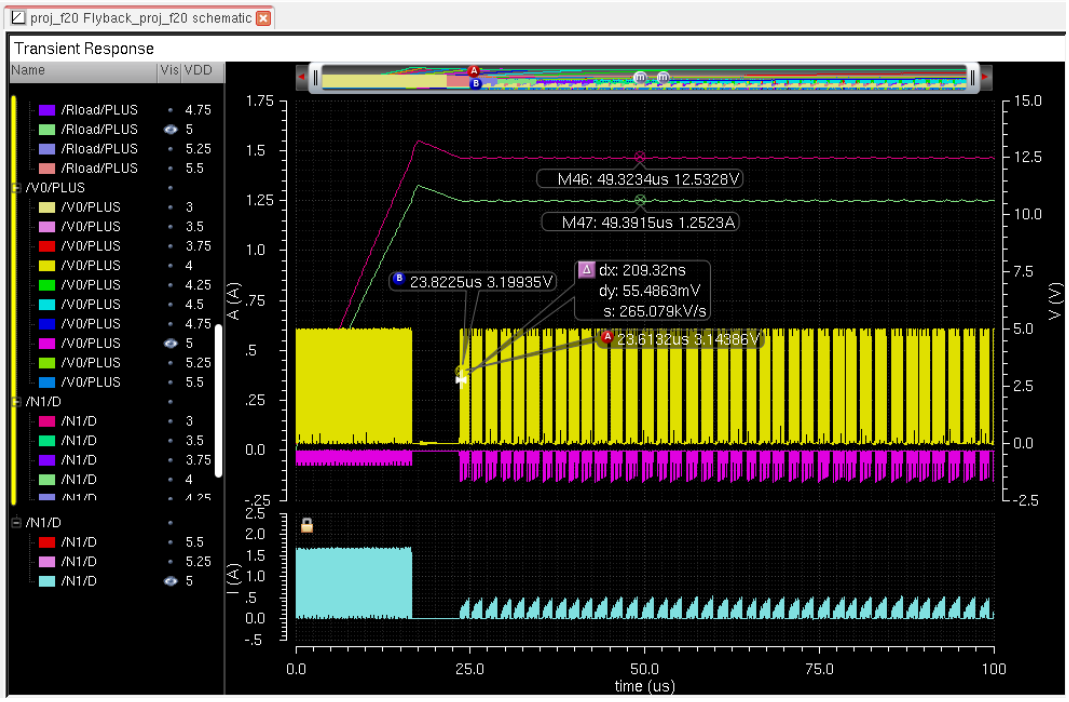

Figure 78 – VDD at 5V

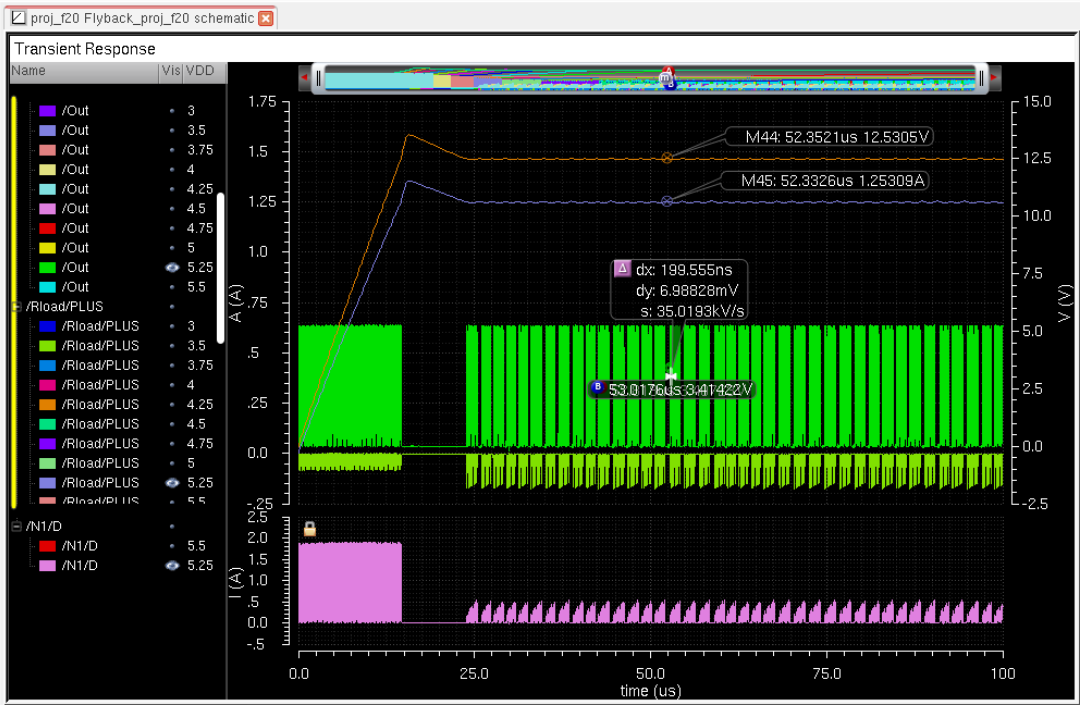

Figure 79 – VDD at 5.25 V

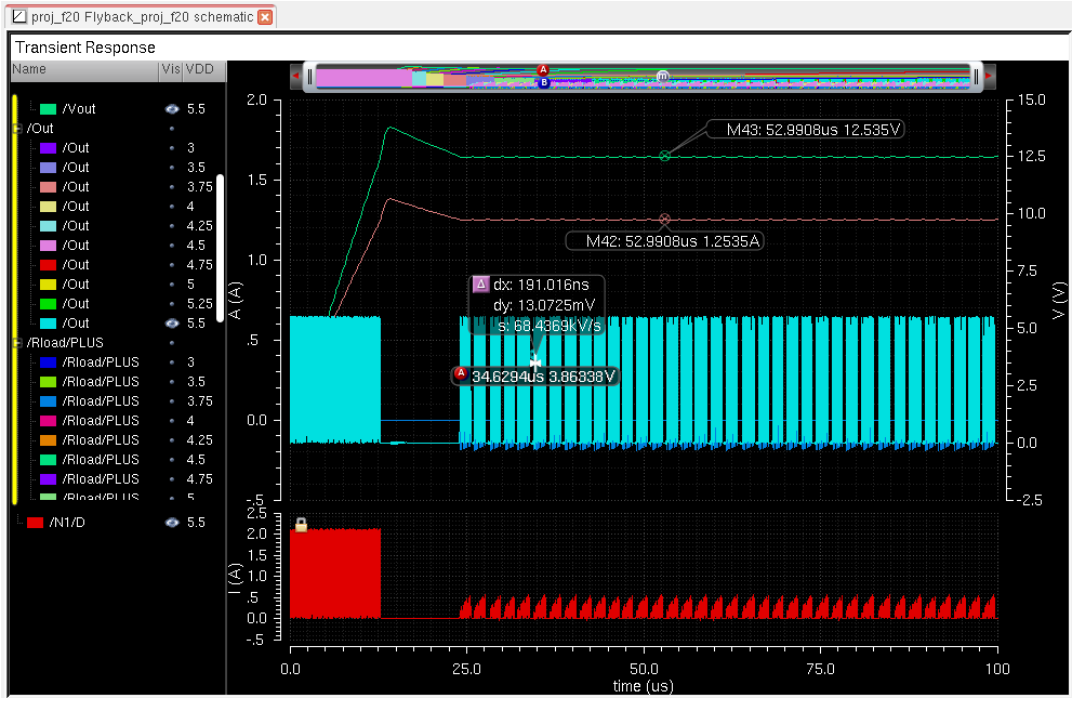

Figure 80 – VDD at 5.5 V

4. Layout and schematic of the Flyback design on a 40 pin frame chip

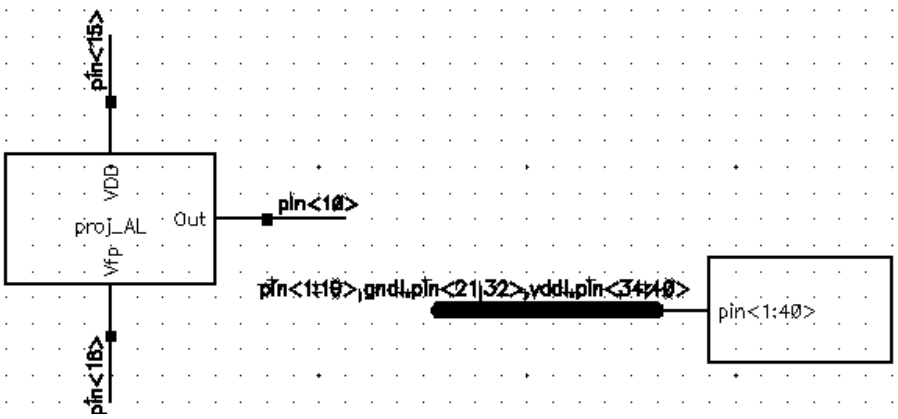

Figure 81 – Schematic for chip connections

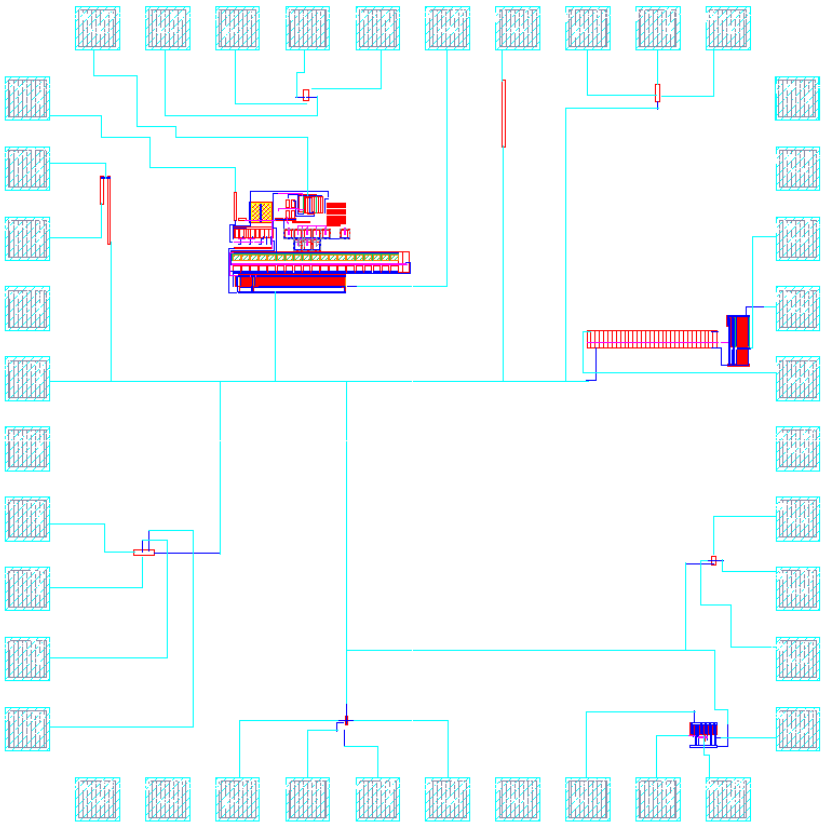

Figure 82 – Layout of chip

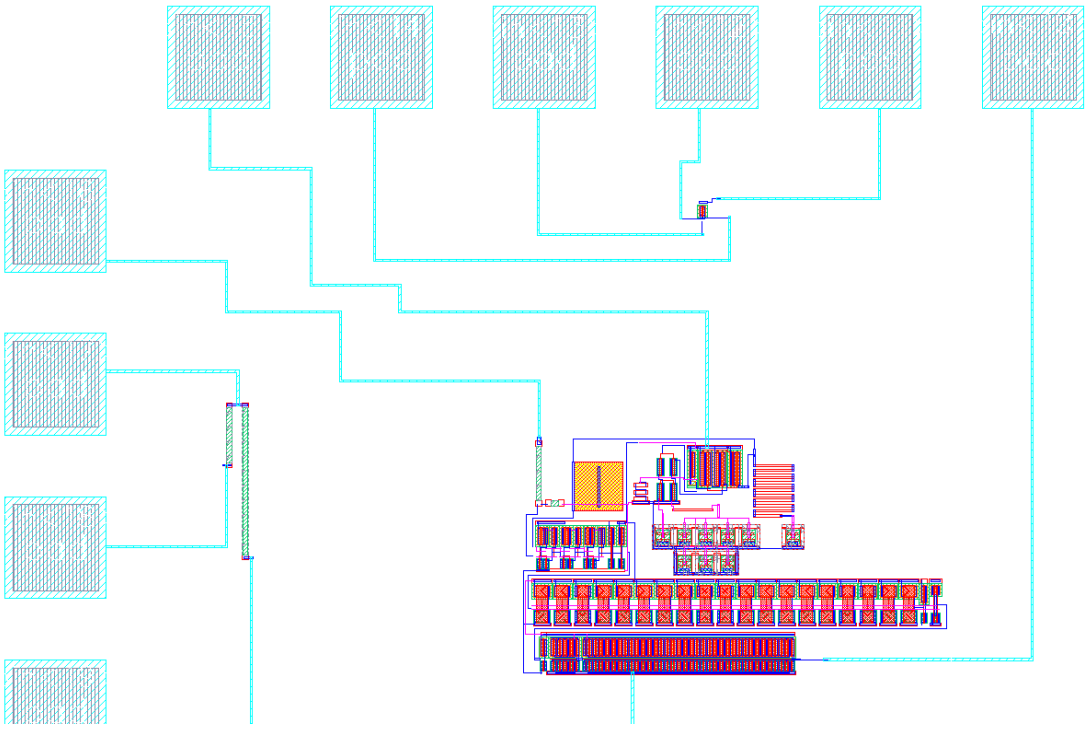

Figure 83 – Closer look at the connections for the chip

This section is to show a possible schematic and layout in putting the Flyback design in a chip, so that if the design were to be tested on a PCB it could be sent for fabrication and then testing. Where the design can be tested with pins 16, 15 and 10 connecting to Vfp, VDD, and Out respectively.

5. Conclusion and Future improvements

After analyzing the results from the various tests conducted on the Flyback design, it can be said that the circuit is able to meet its design requirements. Such as being to nominally output 12.5 V at various load currents, have a nice set of operating voltages to work at from 4.75 to 5.5 volts, and being able to perform decently at higher temperatures. It also accomplishes this with a high percentage of efficiency. However, there is still room for improvement for the design. One is the ripple voltage on the output voltage at higher load currents as looking at table 5 from earlier, the ripple voltage is usually high when the load current increases. This can be considered a flaw in the design as if there is too much voltage difference on the output, the Flyback will not be able to output a steady 12.5 V. There is two ways to address this issue one is to increase the gain of the comparator making it more sensitive to the voltage difference between the two signals. However, as noted from earlier the comparator already uses a lot of power in comparison to the other devices. It should be noted that taking this approach will use

more power. The other approach is to lessen the delay in the feedback path of the comparator. As there must be too much delay which does not allow the comparator to properly operate making the circuit work harder to keep, hence the greater ripple voltages. To lessen the delay, all time delays find in the circuit must be accounted and redesigned, for example reduce the sizing of the inverters in the ring oscillator or use a smaller stage buffer. There is one more way to reduce the ripple voltage, but it comes at making the cost of the circuit increase. There is a 10 uF capacitor on the output of the circuit which if increased to 100 uF reduces the ripple greatly, but this option is not viable as increasing the cost of the circuit even by a few cents is a lot in the semiconductor business. Lastly, power is another improvement especially for the comparator, a solution would be to use one comparator and change the sizing of the PMOS controlling the current to a smaller length and larger width, it should be noted however, that this still might not have enough gain and it might be necessary to use a different topology such as a n-type or rail type diff-amp. Overall the circuit worked well and the experience doing this project and report was great.