Application Report

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AN-1205 Electrical Performance of Packages

ABSTRACT

This note is a snapshot of electrical performance of National's IC packages. It is provided to help designers get an idea about electrical parasitics associated with the package, and help them compare the electrical performance of different packages. The electrical performance of a package is usually expressed in terms of resistance (R), inductance (L), and capacitance (C). Example R-L-C data is provided for National's package types.

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1 Introduction

This note is a snapshot of electrical performance of National's IC packages. It is provided to help designers get an idea about electrical parasitics associated with the package, and help them compare the electrical performance of different packages. The electrical performance of a package is usually expressed in terms of resistance (R), inductance (L), and capacitance (C). Example R-L-C data is provided for National's package types.

1.1 RESISTANCE

Resistance is the cause of IR drops in the package. DC resistance is the resistance of a conductor when the entire cross section of the conductor is carrying current. At higher frequencies, the current is concentrated along the surface of the conductor, due to skin effect. AC resistance increases with frequency, because as the frequency increases, skin depth decreases, and the available cross section for the current flow decreases. AC resistance varies linearly with length of the conductor, but not with respect to cross sectional area.

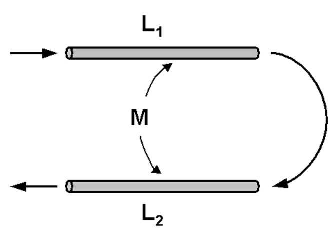
1.2 INDUCTANCE

Inductance (L) is defined as the relationship between the following for a closed current path:

- flux linkage (λ) and current flow (i): $\lambda = L \times i$ or
- time varying voltage (v) and current (i): $v = L \times di/dt$

On an IC package, signals propagate in and out through the signal leads and return through the power leads. The closed current path (or loop) is thus formed by signal leads together with power or ground leads. It is also possible to calculate inductance for an open circuit path, or a section of a closed loop (e.g., just a single lead). This is called **partial inductance**. Using this concept, the inductance contributions of different elements in the loop (and their interactions) can be separated into different inductance elements. This allows the designer to determine return paths and noise by simulation. It is possible to determine the total loop inductance of an IO signal (returning through the power lead) or a differential pair using partial self and mutual inductance. (See Figure 1).

DC and AC Inductance: DC Inductance is calculated assuming that the current flows through the entire cross section of the conductor. AC inductance is calculated assuming that the skin depth is small compared to the cross section of the conductor, and current flows only on the surface of the conductors. Both DC and AC Inductance can be provided for packages. To determine which inductance is appropriate for your application, please see the section "Frequency limitations of R-L-C parameters".



$$L_{LOOP} = L_1 + L_2 - 2M$$

Figure 1. Inductance of a Signal Loop

1.3 CAPACITANCE

Self capacitance is the capacitance of any element to "ground". In package electrical models, the plane on the PC board is assumed to be an ideal ground. Thus, self capacitance of any package element is the capacitance of that element to the board plane. Mutual capacitance is the capacitance between any two elements. For example, in a lumped model of ball grid array package, capacitance from a package trace to the package VSS plane is mutual capacitance.

1.4 FREQUENCY LIMITATIONS OF R-L-C PARAMETERS

As long as the conductor lengths are small compared to the maximum sinusoidal frequency of the signal, the lumped R-L-C approximation of the element is appropriate. For digital ICs, a lumped model is appropriate for a maximum lead length of 60 × t_r (t_r is rise time in nanoseconds and length is in millimeters). When using lumped elements, it is important to know which parameters (DC or AC) should be used. Table 1 gives this information.

Transmission line models or distributed models should be used for high frequencies. To determine if your product requires this analysis, contact your local National Semiconductor technical representative.

Table 1. Frequency limitations of RLC parameters

Parameter	Valid Frequency Range	
DC Resistance	Leadframe packages: DC to 500 kHz	Substrate packages: DC to 5 MHz
AC Resistance	Leadframe packages: 500 kHz to any freq.	Substrate packages: 5 MHz to any freq.
DC Inductance	Leadframe packages: DC to 10 MHz	Substrate packages: DC to 100 MHz
AC Inductance	Leadframe packages: 10 MHz to any frequency provided lumped model is adequate.	
	Substrate packages: 10 MHz to any frequency provided lumped model is adequate.	
Capacitance	From DC to any frequency, as long as dielectric loss can be neglected.	

2 Circuit Model of a Package Lead

National Semiconductor defines package models in terms of their T-equivalent circuits. Each lead has two terminals - a "source" and a "sink" - representing its two ends. In a T-equivalent circuit, the lead inductance and resistance are divided in two parts, and placed on either sides of the lead capacitance. Figure 2 shows a T-equivalent model of three leads. The leads are labeled "Lead 1", "Lead 2" and "Return". Signal current flows in or out of "Lead 1" and return current flows on the "Return" lead. Mutual inductance between signal and return lead significantly affects the performance of the signal loop. Therefore, mutual inductance of all leads to the ground lead must be included in detailed simulations. Similarly for calculating package cross-talk, mutual inductance between two signal leads should be taken into account. Package circuit models can be provided in SPICE format. For package SPICE models contact your local National Semiconductor technical representative.

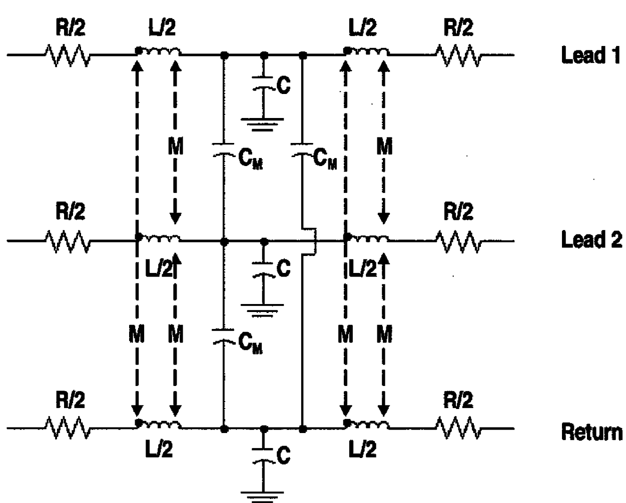


Figure 2. Equivalent of three package leads

3 Example R-L-C Values for Packages

This section provides RLC values for National's packages. The following is true for the data presented in this note:

1. Example R-L-C data is provided for typical leads only. For detailed analysis, accurate package models

should be obtained.

2. The PC board plane is assumed 20 mils (0.5 mm) below the seating plane of the package.
3. Wirebond parasitics are not included in this section; they are separately provided in Table 7.
4. Inductance given is partial AC inductance; it does not scale linearly with length.
5. Resistance provided is AC resistance calculated at 1GHz.
6. Mutual inductance to the immediate (M12) and the next-of-immediate (M13) leads is provided. It should be noted that in packages with no power planes, significant mutual coupling exists beyond these. For example for a PQFP, the coupling coefficient (k) between two leads that are separated by 10 leads can be as high as 0.3.

Table 2. Example RLC values for lead-frame based packages and micro SMD

Package	Body Size (mm)	Lead Count	R (ohm)		L (nH)		M (nH)				C (pF)		C_{M12} (pF)	
			Corner	Center	Corner	Center	Corner		Center		Corner	Center	Corner	Center
							M12	M13	M12	M13				
QFP	28 x 28	208	0.90	0.65	12.00	8.00	8.00	6.50	5.50	4.50	0.20	0.06	1.00	0.60
	20 x 14	128	1.2	0.8	4.50	2.40	2.80	2.20	1.40	1.10	0.10	0.05	0.45	0.20
	12 x 12	80	0.36	0.28	2.90	2.40	2.30	1.60	1.30	0.90	0.15	0.10	0.27	0.20
LLP	all sizes	all	0.001	0.001	0.008	0.008	0.001	0.001	0.001	0.001	0.03	0.03	0.03	0.03
Mini SOIC	5 x 3	8	0.015	0.015	0.45	0.45	0.15	0.08	0.15	0.08	0.05	0.05	0.04	0.04
SC-70	2 x 1.25	5	0.015	-	0.45	-	0.08	0.05	-	-	0.06	-	0.06	-
PLCC	11.43 x 11.43	28	0.05	0.04	4.4	3.2	2	1.5	1.5	1.1	0.35	0.25	0.6	0.45
SSOP	5.3 x 10.2	28	0.3	0.25	2.9	1.3	1.45	0.85	0.6	0.35	0.2	0.08	0.27	0.1
MDIP	19 x 6.35	14	0.15	0.05	7.0	3.0	2.5	1.8	1.0	0.7	0.65	0.25	1.1	0.4
Micro SMD (small bump) (1)	all sizes	all	0.003	-	0.011	-	0.002	-	-	-	0.012	-	0.005	-
Micro SMD (large bump) (1)	all sizes	all	0.002	-	0.013	-	0.002	-	-	-	0.016	-	0.012	-

(1) Micro SMD package does not have wirebonds.

3.1 LAMINATE BASED CSP (CHIP-SCALE PACKAGE)

There are two types of laminate based CSPs: single row and dual row. Because the lead-geometry of all single row CSPs is the same, the RLC parasitics are the same. However, for the dual row CSPs, there are three types of lead geometries (labeled as #1, #2 and #3 in Table 3), and the parasitics are different for different geometries. To determine which dual row design is being used for your product, please contact your local National Semiconductor technical representative. Figure 3 shows a picture of a typical single and dual row CSP. Table 3 gives typical RLC characteristics of CSPs. Mutual inductance terms in the columns in Table 3 are illustrated in Figure 3. M12 is the mutual inductance between two neighboring leads in the same (inner or outer) row. M_{RR} is the mutual inductance between the neighboring leads of different rows. For more details on the construction of CSP packages, browse to http://www.national.com/packaging.

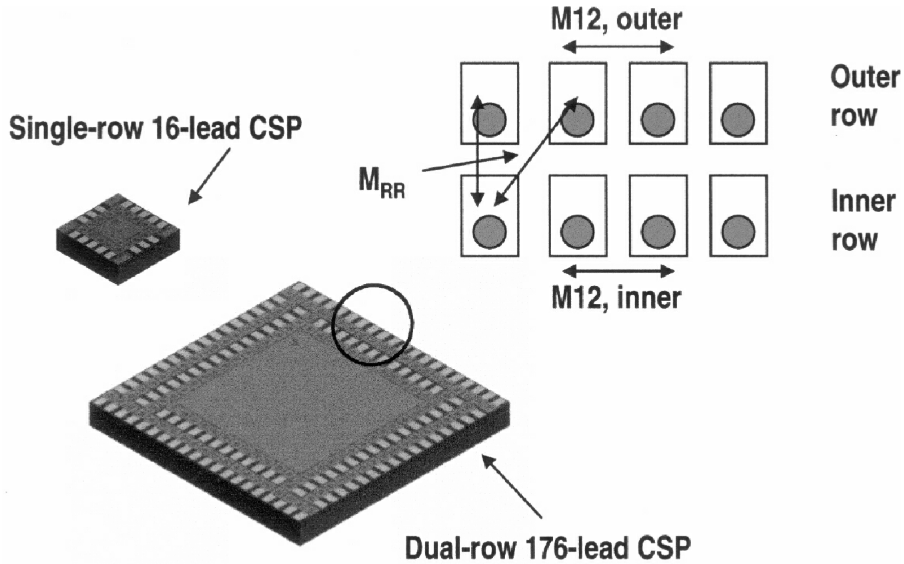


Figure 3. Laminate CSP packages (not to scale)

Table 3. Example RLC data for CSP packages

Package	Lead Count	R (ohm)		L (nH)		M (nH)			C (pF)		C_M (pF)
		Outer	Inner	Outer	Inner	M12 Outer	M12 Inner	MRR	Outer	Inner	
Dual row, #1	128 /176	0.03	0.03	0.40	0.40	0.10	0.10	0.08	0.08	0.08	0.07
Dual row/ inline bond pads #2	128 /176	0.04	0.03	0.60	0.40	0.09	0.06	0.06	0.10	0.08	0.07
Dual row/ inline bond pads #3	128 /176	0.03	0.08	0.40	1.00	0.06	0.27	0.12	0.08	0.10	0.07
Single row	all	0.03		0.40		0.10			0.08		0.07

3.2 BGA PACKAGES

A typical BGA (ball grid array) package is shown in Figure 4. Each side of the package has four rows of solder-balls. The traces going to the solder balls in the corners of the package are significantly longer, therefore the data is grouped by "corner" and "center" leads. In Table 4, "O" column gives data for the outermost row of solder-balls on the package (as illustrated in Figure 4); similarly, "I" column gives data for the innermost row of solder balls on the package. LBGAs and FBGAs (low-profile BGAs and fine-pitch BGAs, respectively) are often custom routed, and it is therefore difficult to provide generalized R-L-C data. Data for an LBGA and an FBGA is provided for reference.

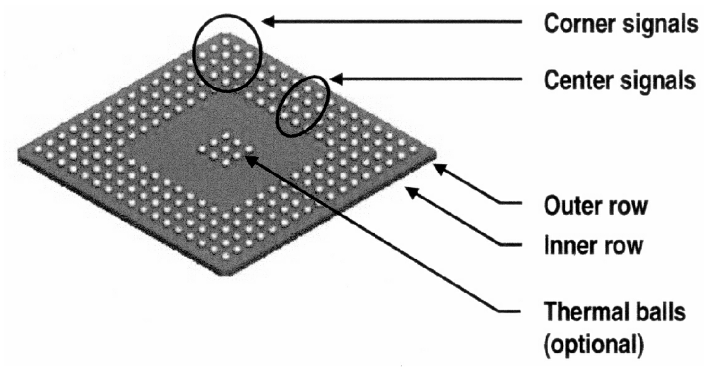


Figure 4. Ball Grid Array packages

Table 4. Example RLC Characteristics of BGAs (without planes)

Package	Body Size (mm)	R (ohm)				L (nH)				M (nH)				C (pF)				C_M (pF)			
		Corner		Center		Corner		Center		Corner		Center		Corner		Center		Corner		Center	
		O	I	O	I	O	I	O	I	O	I	O	I	O	I	O	I	O	I	O	I
PBGA-208	23 x 23	1.20	0.80	0.90	0.60	9.00	6.00	5.50	2.50	6.00	4.50	3.50	1.50	0.20	0.10	0.15	0.10	0.35	0.15	0.15	0.10
PBGA-388	35 x 35	1.80	1.20	1.35	1.00	14.00	10.00	8.00	4.50	9.00	6.50	5.00	3.00	0.30	0.15	0.25	0.18	0.50	0.25	0.25	0.15
LBGA-196	15 x 15	0.4		0.2	0.3	1.70		0.90	1.20	0.60		0.30	0.45	0.08		0.04	0.04	0.10		0.10	0.10
FBGA-81	9 x 9	0.025 - 0.075				0.4 - 1.5				0.03 - 0.1				0.04 - 0.06				0.03 - 0.075			

Modeling packages which have planes for power and ground is more complex. Signals propagate through the signal leads and return over the power and ground planes. The high-speed return signal tends to concentrate on the area of the plane closest to the propagating signal. This means that the current density on the plane is non-uniform, and non-constant with time. It is therefore not possible to give a ***single*** inductance number for a power or a ground plane in a package. However, inductance for the ***return path*** of a particular signal lead on a plane can be calculated. Table 5 and Table 6 give the example RLC values for EBGA packages. Plane inductance values in the L_{PLANE} column of Table 5 give inductance in the return path (VDDIO and/or VSSIO) of a typical signal that returns over the power plane. Similarly, the plane capacitance values pertain only to that section of the plane.

Table 5. AC Inductance - EBGA packages

Package	Lead Count	L		M		M (trace to planes)						L_{PLANE}
		Corner	Center	Corner	Center	Corner [(1)]			Center [(1)]			
						1	2	3	1	2	3	
EBGA	215	5.0 - 7.8	2.5 - 4.0	2.9 - 3.8	1.4 - 2.0	2.8 - 4.0	2.2 - 3.2	2.0 - 2.8	2.0 - 2.5	1.4 - 2.2	1.2 - 1.5	4.0
	368	7.5 - 10.5	6.5 - 8.0	2.5 - 4.0	2.5 - 3.5	3.1 - 4.0	2.5 - 3.0	2.5 - 2.8	1.8 - 3.0	1.5 - 2.0	1.1 - 1.5	4.0

(1) Mutual inductance to all the 3 planes is given, 1 is nearest to traces 3 is farthest.

Table 6. Resistance and Capacitance - EBGA packages

Package	Body Size (mm)	Lead Count	R		C	C_M	$C_{M\text{-}PLANE}$	C_{PLANE}	
			Corner	Center				Self (1)	Mutual (2)
EBGA	27 x 27	215	0.75 - 0.90	0.60 - 0.80	0.08 - 0.12	0.10 - 0.14	1.10 - 1.50	0.6 - 1.2	5.0 - 8.0
	40 x 40	368	1.00 - 1.30	0.7 - 1.0	0.30 - 0.50	0.10 - 0.20	1.20 - 1.80	1.5 - 2.0	14.51 - 50

(1) Self capacitance of the plane closest to the board ground plane. Self capacitance to planes other than this plane is zero.
(2) Mutual capacitance between adjacent planes. This capacitance, if between power planes, will provide help in decoupling.

4 Wirebonds

To obtain package parasitics with wirebonds, add the inductances and resistances for the appropriate wire lengths to the package parasitics provided in the previous sections. Following table gives wirebond inductance for different wire lengths. AC resistance of wirebonds (at 1GHz) is 0.1−Ω/mm (= 0.0025−Ω/mil). Capacitance of wirebonds is negligible, and is therefore omitted from this note. For CSPs and LLPs, use the L and M values in the "Wire Inductance" column of the table. It has been observed that there is a significant amount of coupling between wirebonds and leads/traces of a package (exceptions: CSPs and LLPs, due to their short trace/lead lengths). The column "Effective Inductance" in Table 7 gives L and M values corrected for this mutual coupling. Use the L and M values in this column for all packages other than CSPs and LLPs. Because of space limitations, mutual inductance is provided only for two neighboring wires. Significant mutual coupling exists beyond these, and it should be taken into account in detailed analysis.

Table 7. Wirebond inductance

Length		Wire Inductance (For CSPs and LLPs)			Effective Inductance (For all other packages)		
(mm)	(mils)	L (nH)	M12 (nH)	M13 (nH)	L (nH)	M12 (nH)	M13 (nH)
0.50	19.60	0.32	0.14	0.09	0.45	0.19	0.12
1.00	39.20	0.78	0.39	0.28	1.09	0.55	0.39
2.00	78.40	1.83	1.04	0.78	2.57	1.46	1.12
3.00	117.60	2.99	1.80	1.40	4.19	2.52	1.96
4.00	156.80	4.22	2.62	2.09	5.91	3.67	2.93
5.00	196.00	5.50	3.48	2.82	7.70	4.87	3.95

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