Wednesday, Thursday and Friday
February 10, 11 and 12, 1960

AIEE — U. of P. — IRE

1960—INTERNATIONAL SOLID-STATE CIRCUITS CONFERENCE

Advance Program

Irvine Auditorium and University Museum, University of Pennsylvania, and the Sheraton Hotel, Philadelphia, Pa.

REGISTRATION:

Sheraton Hotel—*Tuesday* —*February 9, 1960*—4:00 P.M.- 8:00 P.M.
Irvine Auditorium—*Wednesday*—*February 10, 1960*—8:00 A.M.- 4:00 P.M.
Irvine Auditorium—*Thursday* —*February 11, 1960*—8:00 A.M.- 4:00 P.M.
Irvine Auditorium—*Friday* —*February 12, 1960*—8:00 A.M.-12:00 Noon

The 1960—International Solid-State Circuits

MORNING SESSION

WEDNESDAY, FEBRUARY 10, 1960

AFTERNOON SESSION

SESSION I: Applications of Tunnel Diodes

Irvine Auditorium—9:00 A.M.-11:45 A.M.

Chairman: T. R. Finch, Bell Telephone Laboratories, Inc., Murray Hill, N. J.

1.1: Esaki Diodes: A Survey

G. C. Dacey, Bell Telephone Laboratories, Inc., Murray Hill, N. J.

The physical principles underlying Esaki-diode operation will be presented. Considerations leading to a simple shunt-equivalent circuit will be discussed, and general consequences for the use of Esaki diodes in both switching and transmission circuits will be drawn.

1.2: Tunnel Diodes and Their Use as Multi-Junction Circuit Elements

J. J. Tiemann, General Electric Research Laboratory, Schenectady, N. Y.

The factors influencing the electrical properties of tunnel diodes will be discussed, and experimental models exploiting these properties will be described. Emphasis will be given to an rf-communication system in which it was found possible to perform several different functions with one diode.

1.3: The Tunnel Diode as a Logic Element

M. H. Lewin, A. G. Samusenko and A. W. Lo, RCA, Princeton, N. J.

Three modes of operation using the tunnel diode as the only active switching element will be described. The dc-powered bistable mode with unconditional reset seems particularly attractive, and will be discussed extensively. Data on swtiching speed in the millimicrosecond range as a function of loading, overdrive, etc., will be included.

1.4: Circuit Principles for Application of Esaki Diodes at Microwave Frequencies

M. E. Hines, Bell Telephone Laboratories, Inc., Murray Hill, N. J.

The power capacity of single-spot and distributed Esaki-diode circuits is limited at high frequencies by the requirement of small diode-junction dimensions. This problem can be alleviated by using many diodes in parallel or extended narrow-strip diodes. Preliminary experimental results for several types of circuits will be given.

1.5: Tunnel-Diode Radio-Frequency Amplifier

E. Miller, H. B. Yin and J. Schultz, RCA, Princeton, N. J.

In most applications, in the past, conventional amplifiers have been superior to negative-resistance amplifiers. Tunnel-diode negative-resistance amplifiers are practical, and will be very useful in various receiver applications. This paper will discuss the advantages and disadvantages of tunnel-diode rf amplifiers.

1.6: Esaki Diode-Logic Circuits*

G. W. Neff, S. A. Butler and D. L. Critchlow, IBM, Yorktown, N. Y.

The Esaki diode is a potentially low-cost, high-speed, two-terminal device exhibiting a short-circuit stable negative resistance over a portion of its volt-ampere characteristic. This paper will describe digital computer circuits, such as shift registers, triggers and counters, which utilize the foregoing characteristics.

*For possible presentation in Session E7

LUNCH: 12:00 Noon to 1:15 P.M.—University Museum

Formal Opening of Conference: 1:45-2:45 P.M.—Irvine Auditorium

Introductory Comments—*Arthur P. Stern,* General Electric Electronics Laboratory, Chairman of Conference

Welcoming Remarks—*G. P. Harnwell,* President, University of Pennsylvania

Invited Addresses—

C. Guy Suits, Vice President and Director of Research, General Electric Company

The Impact of Solid-State Research on U. S. Industry and Technology

M. J. O. Strutt, Chairman, Electrical Engineering Department, Swiss Federal Institute of Technology

Solid-State Circuits Research in Europe

Dudley Buck Memorial Session

SESSION II: Thin Magnetic Films for Logic and Memory

Irvine Auditorium—2:45 P.M.-5:15 P.M.

Chairman, E. W. Fletcher, MIT, Cambridge, Mass.

2.1: Thin Magnetic Films: A Survey

A. V. Pohm, Iowa State College, Ames, Iowa

The ways in which the various modes can be employed for destructive and nondestructive memories will be discussed and their performance limitations considered. Existing film memory efforts will be partially surveyed, and the material and system problems examined. Possible future developments also will be discussed.

2.2: High-Speed Magnetic-Film Logic

W. E. Proebster, IBM Research Laboratory, Zurich, Switzerland

Thin films of Permalloy-type material exhibit bistability and millimicrosecond switching at low power level. The central problem in thin film logic is the control of the switching of one film by a second film. Methods of constructing a shift register and circuits performing logical functions will be described.

2.3: A Thin Magnetic-Film Shift Register

K. D. Broadbent and F. J. McClung, Jr., Hughes Research Laboratories, Los Angeles, Cal.

The dynamics and interactions of domains within continuous magnetic thin-film structures may lead to a variety of applications. Detailed will be the theory and operational characteristics of a shift register in which binary information is stored and translated in and along a continuous evaporated thin magnetic film.

2.4: An Evaporated-Film Cryotron Circuit

C. R. Smallman, M. L. Cohen, A. E. Slade and J. L. Miles, Arthur D. Little, Inc., Cambridge, Mass.

A pair of experimental cryotron circuits wherein each circuit is a ring oscillator consisting of 26 cryotrons, measuring 15 by 70 millimeters, will be described. Operation and construction of these circuits as two 13-stage oscillators, one 26-stage oscillator or one 13-stage (bit) shift register will be discussed.

6:00-7:30 P.M.: Open House Cocktail Party—Independence-Constitution Rooms—Sheraton Hotel

8:00 P.M.: *Informal Discussion Sessions—Sheraton Hotel*

E. 1: Tunnel Diode Characterization—Moderator, G. C. Dacey, Bell Telephone Laboratories, Inc., Murray Hill, N. J.

Panel Members:

D. E. Thomas, Bell Telephone Laboratories, Inc., Murray Hill, N. J.
J. J. Tiemann, General Electric Co., Schenectady, N. Y.
S. L. Miller, IBM, Poughkeepsie, N. Y.
H. Somers, RCA, Princeton, N. J.

E. 2: Thin Films for Memory—Moderator, A. V. Pohm, Iowa State College, Ames, Iowa

Panel Members:

J. I. Raffel, MIT, Lincoln Laboratories, Lexington, Mass.
S. M. Rubens, Remington Rand, St. Paul, Minn.
D. A. Meier, National Cash Register, Dayton, Ohio
R. A. Tracy, Burroughs Corp., Paoli, Pa.
D. H. Looney, Bell Telephone Laboratories, Inc., Murray Hill, N. J.
I. W. Wolf, General Electric Co., Syracuse, N. Y.

E. 3: Reliability Considerations—Moderator, W. D. Rowe, Westinghouse Electric Corp., Buffalo, N. Y.

Panel Members:

J. J. Scanlon, Bell Telephone Laboratories, Inc., Whippany, N. J.
G. T. Ross, RCA, Camden, N. J.
K. Davidson, Texas Instruments, Inc., Dallas, Tex.
C. J. Thorton, Lansdale Tube Co., Lansdale, Pa.
G. E. Cunnihan, Stromberg-Carlson, Rochester, N. Y.

E. 4: Noise Theory—Moderator, J. G. Linvill, Stanford University, Stanford, Cal.

Panel Members:

R. P. Rafuse*, MIT, Cambridge, Mass.
W. E. Dahlke, Telefunken, Ulm, Germany
R. B. Adler, MIT, Cambridge, Mass.
D. A. Linden, Stanford University, Stanford, Cal.
P. Penfield, Jr., MIT, Cambridge, Mass.
C. S. Kim, General Electric Co., Syracuse, N. Y.

E. 5: Energy Conversion—Moderator, S. J. Angello, Westinghouse Electric Corp., Pittsburgh, Pa.

Panel Members:

H. Reiner, Standard Elektrik, Stuttgart, Germany
S. R. Hoh, ITT Laboratories, Nutley, N. J.
P. S. Castro, Lockheed Aircraft Corp., Sunnyvale, Cal.
D. A. Paynter, General Electric Co., Syracuse, N. Y.
R. P. Putkovich, Westinghouse Electric Corp., Cheswick, Pa.

E. 6: Magnetic Logic—Moderator, D. C. Engelbart, Stanford Research Institute, Menlo Park, Cal.

Panel Members:

U. F. Gianola, Bell Telephone Laboratories, Inc., Murray Hill, N. J.
A. J. Meyerhoff, Burroughs Corp., Great Valley, Pa.
H. P. Wolff, IBM, Poughkeepsie, N. Y.
W. E. Proebster, IBM, Zurich, Switzerland
T. H. Bonn, Remington Rand Univac, Philadelphia, Pa.
D. Meier, National Cash Register, Hawthorne, Cal.
H. D. Crane, Stanford Research Institute, Menlo Park, Cal.

*Author of Parametric-Circuit Techniques Session Paper 8.6

SESSION III: Digital Logic

Irvine Auditorium—9:00 A.M.-12:00 Noon

Chairman, R. A. Henle, IBM, Poughkeepsie, N. Y.

3.1: Improvements in Current Switching
F. K. Buelow, IBM, Poughkeepsie, N. Y.
The use of stable, low-cost, high-speed diodes in current-switching circuits has reduced delay-per-logic connective to less than 5 mμsec; emitter followers were employed. The current-switching circuits offer level setting, wave reshaping, and optional signal inversion. Examples of system building blocks will be shown.

3.2: Tunnel-Diode Digital Circuitry
W. F. Chow, General Electric Electronics Laboratory, Syracuse, N. Y.
A tunnel-diode flip-flop stage which has advantages with respect to speed, ease of operation and component tolerances will be described. Combinations of these flip-flops in counter and shift-register configurations have been successfully operated. Several potential advantages over conventional transistor circuits will be indicated.

3.3: A Modulation-Demodulation Scheme for Ultrahigh-Speed Computing and Wideband Amplification
W. Eckhardt and F. Sterzer, RCA, Princeton, N. J.
When the variable-impedance element of a modulator of rf power is reactive, the modulating signal may be of smaller power than the rf (pump) signal which it controls. A single-stage amplifier with a 4-db power gain (between a 50-ohm generator and a 50-ohm load) and a rise time of approximately 0.5 nanosecond will be described.

*For possible presentation in Session E12

3.4: Adaptive Logic
R. J. Domenico and R. A. Henle, IBM, Poughkeepsie, N. Y.
This paper will describe a new approach to transistor logic design. Through the use of a photoconductor matrix with light patterns determining the interconnections, logical circuits can be rewired in milliseconds to achieve different system organization. This flexibility can be used to achieve the capability of self-repair.

3.5: Design of a Solid-State Neuron Circuit for Use in Self-Organizing Systems
C. L. Coates and E. A. Fisch, General Electric Electronics Laboratory, Syracuse, N. Y.
Practical neuron circuits which utilize semiconductor and magnetic techniques are being developed. All of the functions dealing with the memory are controlled by a transfluxor in each input channel. A continuous indication of its state, as well as a simple economical way of altering the gain of each channel, are thus provided.

3.6: Fast Logic Using Transistor Current-Routing Techniques*
D. B. Jarvis, L. P. Morgan and J. A. Weaver, Mullard Research Laboratories, Salsford, England
A current-routing system of circuit logic and its applications will be described. Using 100-Mc transistors, the following results have been achieved: A carry propagation time of 6 mμsec per stage; a shift rate in excess of 10 Mc in a shift register; and a delay time of 40 mμsec in a 5 to 32 decoder.

MORNING SESSION

SESSION IV: Applications of New Devices

University Museum—9:00 A.M.-12:00 Noon

Chairman: H. W. Katz, General Electric Electronics Laboratory, Syracuse, N. Y.

4.1: A Broad-Band, Fast-Acting, Ferrite Switch

D. E. Allen and N. G. Sakiotis, Motorola, Inc., Phoenix, Arizona

Techniques for the design of a Faraday-rotation switch using a ferrite-loaded, quadruply-ridged circular waveguide will be presented. A minimum isolation of 26 db in the OFF position and an insertion loss of approximately 1 db in the ON position over a 20% band has been obtained. The switching time is less than one microsecond.

4.2: A Solid-State Modulator for Millimeter Waves

E. T. Harkless and R. Vincent, Bell Telephone Laboratories, Inc., Murray Hill, N. J.

With suitable waveguide components, the rf impedance of gold-bonded, n-type germanium diodes can be varied to obtain nearly complete absorption or nearly complete reflection. Diode pairs, mounted in waveguide sections, have been combined with hybrid junctions to produce efficient, high-speed pulse modulators of millimeter waves.

4.3: Low-Noise Tunnel-Diode Down-Converter Having Conversion Gain

K. K. N. Chang, W. Y. Pan, H. B. Yin, G. H. Heilmeier, D. J. Carlson and H. J. Prager, RCA, Princeton, N. J.

Low-noise high-gain frequency down-conversion has not been possible with previous mixer devices or parametric devices. This paper will describe new tunnel-diode down-converters which have achieved both extremely high gains and very low noise.

4.4: Photorectifier Based on a Combination of a Photoconductor and an Electret

J. G. van Santen and G. Diemer, N. V. Philips Gloeilampenfabrieken, Eindhoven, The Netherlands

Layers consisting of photoconducting CdS powder bound by a suitable glass enamel can be formed after fusing to a stable photorectifier by means of a combination of heating and passage of dc. De- and reforming is possible. Characteristics and the mechanism involved will be discussed.

4.5: A New High-Speed Effect in Solid-State Diodes

A. F. Boff, R. Shen, Hewlett-Packard Co., Palo Alto, Cal., and J. L. Moll, Stanford University, Stanford, Cal.

The design of diodes to increase the rate of change of current in the recovery transient will be discussed. As applications, a variable-frequency 2-mμsec pulse generator and a harmonic generator with significantly higher output frequencies than can be obtained by previously-known methods will be considered.

LUNCH: 12:00 Noon to 1:15 P.M.—University Museum

SESSION V: Information Storage Techniques

Irvine Auditorium—1:30 P.M.-5:00 P.M.

Chairman: A. W. Lo, RCA, Princeton, N. J.

5.1: The Tunnel Diode as a Memory Element

J. C. Miller, K. Li and A. W. Lo, RCA, Princeton, N. J.

The tunnel diode has been found to be a promising new memory element because of its sharp well-defined threshold, double-valued volt-ampere characteristic, fast-switching speed and low dissipation. Relative merits and limitations of the tunnel diode compared with other memory elements will be discussed.

5.2: Sub-Microsecond Core Memories Using Multiple Coincidence

H. P. Schlaeppi and I. P. V. Carter, IBM, Zurich, Switzerland

Memories using toroidal ferrite cores with cycle times below 1 μsec will be described; multiple coincidence being used to increase the selection ratio. Switching problems which thereby arise can be solved by means of the two-core switch. Details of memory models with oscillograms for 3:1 and 7:1 selection ratios will be shown.

5.3: Fluxlok — A Non-Destructive High-Speed Memory Technique Using Standard Ferrite Cores

R. M. Tillman, Burroughs Corp., Paoli, Pa.

Rotation of magnetic moments in standard ferrite memory cores has been found to produce relatively large bipolar ONE's and ZERO's at clock rates beyond 10 Mc. Interrogation can be made with a single pulse of non-critical polarity, duration and amplitude. A 64-word/24-bit test memory operating at a 2-Mc clock rate will be described.

5.4: Low Coercive-Force Ferrite-Ring Cores for a Fast Non-Destructively Read Store

G. H. Perry and S. J. Widdows, Royal Radar Establishment, Great Malvern, England

Low coercive-force ferrite-ring cores used under partial switching conditions have properties very suitable for high-speed storage. Current requirements and heating in the core are low. Assuming a 4:1 read-to-write ratio and an address-selection time of 100 mμsec, it should be possible to perform 5 storage operations per μsec.

5.5: Memory for a 40-Megacycle Deltic Correlator

W. Peil and J. Hesler, General Electric Electronics Laboratory, Syracuse, N. Y.

This paper will describe the operation of a transistorized silica delay-line memory: Two standard methods for sending information through delay lines that have a bandpass characteristic are carrier modulation and impulse shocking. A third method which has the advantages of simplicity and bandwidth efficiency will be described.

5.6: Partial Switching, Non-Destructive Read-Out Storage Systems*

W. L. Shevel, Jr. and O. A. Gutwin, IBM, Poughkeepsie, N. Y.

This paper will describe an effort to combine three relatively new techniques to yield word-oriented storage systems characterized by high NDRO rates and short clear-write cycle times. Switching the ferrite elements in a rotational mode is desirable because of the lower switching coefficients characterizing this mode.

*For possible presentation in Session E8

AFTERNOON SESSIONS

SESSION VI: Linear Amplification and Generation

University Museum—1:30 P.M.-5:00 P.M.

Chairman: F. H. Blecher, Bell Telephone Laboratories, Inc., Murray Hill, N. J.

6.1: Circuit Applications of a Coaxially Encapsulated Microwave Transistor

V. R. Saari, C. A. Bittmann and R. E. Davis, Bell Telephone Laboratories, Inc., Murray Hill, N. J.

A diffused-base, alloyed-emitter, mesa germanium transistor with base thicknesses of ½ to ¼ micron has been developed. A power gainband product in excess of 5 kMc has been obtained. Biasing and feedback circuits which are compatible with a coaxial structure will be discussed for two-stage amplifiers.

6.2: Tunnel-Diode Amplifiers with Unlimited Gain-Bandwidth Products

E. W. Sard, Airborne Instruments Laboratory, Melville, N. Y.

With the use of the tunnel diode, an unlimited gain-bandwidth product is theoretically achievable in a single-stage amplifier employing realizable network elements. The performance of amplifiers using silicon tunnel diodes has agreed with theoretically predicted results.

6.3: Superconductive Devices and Electrical Measurements at Low Temperatures

I. M. Templeton, National Research Council, Ottawa, Canada

A new device capable of detecting small voltages (about 10^{-13} volt) will be introduced. It depends for its operation on a signal current in a superconducting solenoid winding disturbing the balance of a partially-superconducting bridge circuit. The unbalance is detected by fairly conventional means.

6.4: Solid-State Sampled-Data Bandpass Filters

L. E. Franks and F. J. Witt, Bell Telephone Laboratories, Inc., Murray Hill, N. J.

A new sampled-data filter principle has been used with high-speed switching transistors and diodes to realize a carrier-supply filter with frequency response flat to within ±0.1 db for 14 cps on either side of the 108-kc center frequency. The spurious products introduced by the switching process are at least 50 db down.

6.5: Analysis of Transistor Class-C Oscillators

J. A. Narud, Harvard University, Cambridge, Mass.

A general analytical investigation of Class-C oscillators will be presented and applied to a 1.5-Mc Class-C oscillator using a diffused-base transistor. The rise time and the width of the output pulses are 35 mμsec and 100 mμsec, respectively. The experimental results agree very well with the theory.

6:00-7:30 P.M.: Cocktail-Buffet Dinner—Pennsylvania Room and Grand Ballroom—Sheraton Hotel

THURSDAY, FEBRUARY 11, 1960 EVENING SESSIONS

FRIDAY, FEBRUARY 12, 1960 MORNING SESSION

AFTERNOON SESSION

8:00 P.M.: *Informal Discussion Sessions—Sheraton Hotel*

E. 7: Tunnel Diode Applications—Moderator, A. W. Lo, RCA, Princeton, N. J.

Panel Members:

G. W. Neff*, IBM, Ossining, N. Y.
M. E. Hines, Bell Telephone Laboratories, Inc., Murray Hill, N. J.
W. F. Chow, General Electric Co., Syracuse, N. Y.
K. K. N. Chang, RCA, Princeton, N. J.
E. W. Sard, Airborne Instruments Laboratory, Melville, N. Y.

E. 8: Storage Techniques—Moderator, J. A. Rajchman, RCA, Princeton, N. J.

Panel Members:

W. L. Shevel‡, IBM, Poughkeepsie, N. Y.
R. M. Tillman, Burroughs Corp., Great Valley, Pa.
W. Peil, General Electric Co., Syracuse, N. Y.
J. E. Mack, Bell Telephone Laboratories, Inc., Whippany, N. J.
G. H. Perry, Royal Radar Establishment, Great Malvern, England
H. P. Schlaeppi, IBM, Zurich, Switzerland
J. C. Miller, RCA, Princeton, N. J.

*Coauthor of Tunnel-Diode Session Paper 1.6
‡Coauthor of Storage-Technique Session Paper 5.6

E. 9: Microelectronics—Moderator, G. Sziklai, Westinghouse Electric Corp., Pittsburgh, Pa.

Panel Members:

I. N. Ross, Bell Telephone Laboratories, Inc., Murray Hill, N. J.
D. C. Engelbart, Stanford Research Institute, Menlo Park, Cal.
A. McWhorter, MIT, Cambridge, Mass.
I. A. Lesk, General Electric Co., Syracuse, N. Y.
P. B. Myers, Motorola, Phoenix, Arizona
W. Adcock, Texas Instruments, Inc., Dallas, Tex.
R. Norman, Fairchild Semiconductor Corp., Palo Alto, Cal.
H. W. Henkels, Westinghouse Electric Corp., Youngwood, Pa.

E. 10: Parametric Applications—Moderator, B. Salzberg, Airborne Instruments Laboratory, Melville, N. Y.

Panel Members:

A. Berk, Hughes Aircraft Co., Culver City, Cal.
K. E. Shreiner, IBM, Yorktown, N. Y.
Robert Adler, Zenith Radio Corp., Chicago, Ill.
R. S. Engelbrecht, Bell Telephone Laboratories, Inc., Whippany, N. J.
H. Hsu, General Electric Co., Syracuse, N. Y.
L. Nergaard, RCA, Princeton, N. J.

E. 11: High-Frequency Amplification and Generation—Moderator, J. B. Angell, Philco Corp., Philadelphia, Pa.

Panel Members:

C. H. Knowles, Motorola, Phoenix, Arizona
L. D. Wechsler, General Electric Co., Syracuse, N. Y.
R. L. Pritchard, Texas Instruments, Inc., Dallas, Tex.
V. H. Grinich, Fairchild Semiconductor Corp., Palo Alto, Cal.
J. M. Early, Bell Telephone Laboratories, Inc., Murray Hill, N. J.
F. H. Blecher, Bell Telephone Laboratories, Inc., Murray Hill, N. J.

E. 12: Semiconductor Logic—Moderator, W. B. Cagle, Bell Telephone Laboratories, Inc., Whippany, N. J.

Panel Members:

M. H. Lewin, RCA, Princeton, N. J.
R. F. Schauer, Iowa State College, Ames, Iowa
J. T. Lynch, Burroughs Corp., Paoli, Pa.
L. P. Morgan*, Mullard Research Laboratories, Salsford, England
E. G. Seymour, General Electric Co., Ithaca, N. Y.
F. K. Buelow, IBM, Poughkeepsie, N. Y.

*Coauthor of Digital Logic Session Paper 3.6

SESSION VII: Microelectronic Considerations

Irvine Auditorium—9:00 A.M.-12:00 Noon

Chairman: J. R. Nall, Fairchild Semiconductor Corp., Mountain View, Cal.

7.1: Microelectronics and the Art of Similitude
D. C. Engelbart, Stanford Research Institute, Menlo Park, Cal.

Extreme miniaturization of devices and circuits will take the researcher into realms of physical phenomena where his judgment and intuition may not serve him faithfully. This is due to the difference in relative scaling effects. How the art of scaled-model usage (similitude) may help will be discussed.

7.2: Speed, Power and Component Density in Multielement High-Speed Logic Systems
J. M. Early, Bell Telephone Laboratories, Inc., Murray Hill, N. J.

This paper will discuss the interrelationships between the factors upon which the maximum number of logic elements that can communicate with each other within a single cycle depends. Particular attention will be given to speed and system-volume considerations.

7.3: Concept of Molecular Engineering
H. W. Henkels, Westinghouse Electric Corp., Youngwood, Pa.

The concept of molecular engineering as applied to the development of functional electronic blocks to perform desired system functions will be reviewed. Advantages and disadvantages of this approach, as far as factors of reliability, weight, size and flexibility are concerned, will be discussed and examples will be given.

7.4: Solid-State Micrologic Elements
I. Haas, J. T. Last and R. H. Norman, Fairchild Semiconductor Corp., Palo Alto, Cal.

Basic micrologic elements which operate at 20 Mc per-logic function will be described. The feasibility of using the uncased elements for packaging the logic system of a typical real-time digital computer in a volume of the order of 1.5 cubic inches will be demonstrated.

7.5: Semiconductor Inductance Diode
J. Nishizawa and Y. Watanabe, Tohoku University, Sendai, Japan

The possibility of obtaining inductance using a semiconductor diode will be described. The inductance arises from the time delay of injected-carrier propagation through a highly resistive region. A value of 0.4 h at 3.5 kc has been obtained with a negative resistance in series.

LUNCH: 12:00 Noon to 1:15 P.M.—University Museum

SESSION VIII: Parametric Circuit Techniques

Irvine Auditorium—1:30 P.M.-4:30 P.M.

Chairman: H. Heffner, Stanford University, Stanford, Cal.

8.1: Microwave Properties of Semiconductors: A Survey
H. Kroemer, Varian Associates, Palo Alto, Cal.

An appraisal of microwave properties of semiconductors will be presented. The negative-mass effect, cyclotron resonance and the tunnel effect will be discussed.

8.2: Low-Frequency Reactance Amplifier
J. R. Biard, Texas Instruments, Inc., Dallas, Tex.

Stable voltage amplification of 30 db and noise figures of less than 1.0 db have been observed in a reactance amplifier for signal frequencies between 1 and 40 cps. The circuit configuration is a double-sideband up-converter or modulator, and employs a pump frequency of 150 kc.

8.3: A Passive Parametric Limiter
A. A. Wolf and J. E. Pippin, Sperry Microwave Electronics Co., Clearwater, Florida

This paper will discuss a passive parametric limiter in which limiting is achieved by converting signal-frequency power into oscillations at another frequency. Above five milliwatts, output power is constant within ± 1 db over an input power range greater than 20 db. Low-level insertion loss is less than 0.5 db.

8.4: Backward Traveling-Wave Parametric Amplifier
Hsiung Hsu, General Electric Electronics Laboratory, Syracuse, N. Y.

The backward traveling-wave parametric amplifier has a narrow bandwidth, but is tunable electronically over a wide frequency range. The amplifier may be used as an electronically-swept amplifier, similar to conventional backward wave tube amplifiers. The mechanism of this type of amplifier will be explained.

8.5: An Analysis of Sub-Harmonic Pumping of Parametric Amplifiers
K. E. Mortenson, General Electric Research Laboratory, Schenectady, N. Y.

The purpose of this analysis was to study in some detail the operation of a parametric amplifier pumped sub-harmonically as compared with being pumped directly.

8.6: Measurement of Absolute Noise Performance of Parametric Amplifiers*
R. P. Rafuse, MIT, Cambridge, Mass.

Any measurement procedure which seeks to determine the absolute noise performance of a negative-resistance amplifier must include the behavior of the amplifier in a cascade. This paper will propose and verify a method of optimizing the noise figure of a cascade of a negative-resistance amplifier and a noisy, unilateral second stage.

*For possible presentation in Session E4

1960—INTERNATIONAL SOLID-STATE CIRCUITS CONFERENCE

Scope of Conference

THE 1960-INTERNATIONAL SOLID-STATE CIRCUITS CONFERENCE will feature eight sessions at the University of Pennsylvania devoted to broad advances in the field of solid-state device applications and circuits. Forty-three papers covering new magnetic and semiconductor devices and circuits for digital storage and logic will be offered. Also presented will be a number of survey reports on tunnel diodes, thin magnetic films and microwave properties of semiconductors.

TWELVE INFORMAL SESSIONS, conducted by leaders in the solid-state field, will be held on Wednesday and Thursday evenings in the Sheraton Hotel to provide registrants an opportunity to discuss tunnel diodes and their applications, storage techniques, reliability, noise theory, logic circuits, microelectronics, parametric applications and energy conversion.

Conference Digest of Technical Papers

EVERY REGISTRANT will receive a 100-page letterpress conference-report book featuring digests of every paper, supplemented by over 300 illustrations. Post-conference copies of the report will be available at $5.00 each.

Location

THE CONFERENCE will be held on the campus of the University of Pennsylvania in the Irvine Auditorium and in the University Museum.

IRVINE AUDITORIUM is located at the northwest corner of 34th and Spruce Streets; the University Museum is just east of the southeast corner of 34th and Spruce Streets, Philadelphia, Pennsylvania. Central Philadelphia can be reached by bus route 42 and the 30th Street station of the Pennsylvania Railroad is less than a mile from the University Campus.

THE INFORMAL Wednesday-Thursday evening sessions will be held in the Sheraton Hotel, 1725 Pennsylvania Boulevard, in central Philadelphia.

Accommodations

THE SHERATON HOTEL, Conference headquarters, has reserved a block of rooms for Conference registrants. Offices of most major airlines are within one-half block of the hotel; several are in the lobby of the hotel. Railroads to all points are convenient to the hotel; ample indoor parking facilities are available via an underground concourse.

Luncheons . . . Cocktail-Buffet Dinner

LUNCHEONS on Wednesday, Thursday and Friday will be served to a limited number in the University Museum, University of Pennsylvania.

THE COCKTAIL PARTY-Buffet Dinner will be held on Thursday evening in the Pennsylvania Room and Grand Ballroom of the Sheraton Hotel.

AN OPEN-HOUSE COCKTAIL PARTY will be held on Wednesday evening in the Independence-Constitution Rooms.

Registration

REGISTRATION AND HOTEL reservation forms are enclosed with this Conference announcement. Additional forms may be obtained from John W. MacNeil, Remington Rand Univac, Box 5616, Philadelphia 29, Pa.

CONFERENCE FEES ARE:

	Advance—Before Feb. 3, 1960	At Conference or After—Feb. 3, 1960
Registration—		
Member AIEE or IRE:	$8.00	$12.00
Non-Member:	10.00	14.00
Wednesday Lunch:	2.75	3.50
Thursday Lunch:	2.75	3.50
Friday Lunch:	2.75	3.50
Cocktail Party:	2.50	3.50
Buffet Dinner:	6.50	7.50
Combination Cocktail Party and Buffet Dinner:	8.50	10.00

Full-time students will be registered free-of-charge for the technical sessions.

ALL TECHNICAL SESSIONS will start promptly at 9:00 A.M. on each day of the Conference. To avoid delays in registration and to assist the local arrangements committee, advance registration and meal purchases are strongly recommended.

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