1958 TRANSISTOR and SOLID-STATE CIRCUITS CONFERENCE

IRE—AIEE—U. of P.

Advance Program

Thursday and Friday—February 20 and 21, 1958

Irvine Auditorium and University Museum
University of Pennsylvania
and the Hotel Sheraton, Philadelphia, Pa.

REGISTRATION: Hotel Sheraton—*Wednesday, February 19, 1958*—6:00 P.M.-10:00 P.M.
Irvine Auditorium—*Thursday, February 20, 1958*—8:00 A.M.-9:30 A.M.
Irvine Auditorium—*Friday, February 21, 1958*—8:00 A.M.-9:00 A.M.

The 1958 Transistor and

Cosponsored by: IRE Professional Group on Circuit Theory .. AIEE Committee on Solid State Devices

THURSDAY, FEBRUARY 20, 1958

MORNING SESSIONS

SESSION I: Computer Circuits

Irvine Auditorium—9:30 A.M.-12:00 Noon

Chairman: T. R. Finch,
Bell Telephone Laboratories, Murray Hill, N. J.

1.1: Linear-Selection, Core-Memory Techniques Using Transistors
Robert E. McMahon, M.I.T. Lincoln Laboratory, Lexington, Mass.

Linear selection memory techniques using transistors are compared with coincident current techniques. It is shown that besides the natural advantages of linear selection, the memory has less transistors than the equivalent coincident current memory. The speed capability of linear selection is discussed and operational circuitry for a 2-microsecond access time memory is shown.

1.2: Transistor Resistor Logic Circuit Analysis
Q. W. Simkins, Bell Telephone Laboratories, Murray Hill, N. J.

The relationship of the transistor resistor logic building block operational characteristics, such as fan in, fan out and speed to the transistor properties, is discussed. It is shown that with a commercially available transistor a fan in and fan out of five can be achieved with a signal propagation speed of 0.5 microsecond per stage or less.

1.3: Ten Megapulse Transistorized Pulse Circuits for Computer Application
W. N. Carroll and R. A. Coopper, IBM Military Products Division, Kingston, N. Y.

Described are a group of ten-megapulse transistorized computer circuits which combine the simplicity of direct-coupled transistor logic and the speed of more complex circuitry. These transformer coupled circuits operate in a parallel organized pulse computer utilizing circuit techniques that minimize component count and the use of delay lines.

1.4: High-Speed, Graded-Base Transistor, Digital-Circuit Techniques
R. H. Baker, M.I.T. Lincoln Laboratory, Lexington, Mass.

High speed circuit configurations utilizing graded-base PNP and NPN transistors are discussed. Emphasis is placed upon reasons for the choice of the configurations. The circuit configurations are based on considerations from the areas of circuit techniques, components (transistor characteristics present and future), and system aspects (race problems, etc.). Although actual circuits are presented, the major purpose of the talk is to acquaint the audience with a new set of circuit configurations.

1.5: Higher-Speed Computer Circuits
A. K. Rapp and M. M. Fortini, Research Div., Philco Corp., Philadelphia, Pa.

Using a base-gating technique, a new high-speed flip-flop can provide scale-of-two counting at rates up to 50 megapulses per second using SB-100 surface-barrier transistors. To provide the high-speed, short-duration pulses necessary for driving fast counters, new methods of generating and shaping pulses, utilizing transmission lines, have been devised.

SESSION II: Tutorial Survey

University Museum—9:30 A.M.-12:00 Noon

Chairman: J. A. Rajchman,
Radio Corp. of America, Princeton, N. J.

2.1: Survey of Noise in Semiconductor Diodes and Triodes
W. H. Fonger, Radio Corp. of America, Princeton, N. J.

2.2: Review of Several Solid-State Devices and Their Applications
H. W. Katz, General Electric Co., Syracuse, N. Y.

LUNCH: 12:00 Noon to 1:30 P.M.—University Museum

Formal Opening of Conference: 1:45-2:45 P.M.—Irvine Auditorium
Introductory Comments—*J. H. Mulligan, Jr.*, Chairman of Conference
Welcoming Remarks—*G. P. Harnwell*, President, University of Pennsylvania
Invited Address—**Whither Transistor Electronics**—*William Shockley*, Nobel Laureate

AFTERNOON SESSIONS

SESSION III: Switching

Irvine Auditorium—2:45-5:15 P.M.

Chairman: Philip M. Thompson,
Defense Research Telecommunications Establishment, Ottawa, Canada

3.1: New Configurations in Non-Saturating Complementary Current Switching Circuits
Carl M. Campbell, Jr. Burroughs Corporation, Paoli, Pa.

Non-saturating complementary current switching circuits are presently of considerable interest to computer circuit designers because of their simplicity, reliability, and speed. An inhibit principle has been devised which retains these features while making possible new circuit configurations. For many circuits, these new configurations require fewer transistors than configurations possible from heretofore publicized techniques alone.

3.2: A Method of Designing Transistor Avalanche Circuits With Application to a Sensitive Transistor Oscilloscope
G. B. B. Chaplin, United Kingdom Atomic Energy Authority, Electronics Division, Harwell, England.

Many commercially available transistors exhibit the avalanche effect which enables them to produce pulses with rise times up to a factor of 100 times shorter than in conventional trigger circuits. Other advantages of the avalanche mode of operation are the simplicity of the circuits and the fact that the ensuing rate of rise of current is almost completely independent of the characteristics of the input trigger pulse.

3.3: The Use of a Junction Transistor as a Three-Terminal Temporary Memory for Digital Circuits
G. H. Perry and E. W. Shallow, Royal Radar Research Establishment, Great Malvern, England.

The phenomenon of carrier storage in junction transistors has generally been looked upon as one of their undesirable characteristics. It is the purpose of this paper to show that carrier storage can be controlled to provide a three-terminal temporary memory for digital computing circuits of a type not provided by any other single electronic component.

3.4: Transistor Bilateral Switches
W. M. Cook, RCA, Camden, N. J., and P. L. Bargellini, U. of Pa. Moore School of Electrical Engineering and RCA.

This paper discusses the basic transistor properties required for efficient bilateral switching. The transistor characteristics are related to the operation of typical bilateral switches. Such topics as signal feed-through in the off-switches, signal loading and attenuation in the on-switches, and obtaining bilateral action from non-ideal transistors are discussed.

3.5: A Two-Transistor Gate for Time-Division Switching
J. D. Johannesen and P. B. Myers, Bell Telephone Laboratories, Murray Hill, N. J.

A bilateral balanced solid state gate suitable for use in a pulse amplitude modulated time-division switching system is described. The gate, consisting of two junction transistors and a pulse transformer, is capable of handling the currents required to produce a low loss connection when operated for one or two microseconds every 125 microseconds. Device and circuit requirements are presented with performance data in an experimental system.

SESSION IV: New Techniques

University Museum—3:15-5:15 P.M.

Chairman: H. E. Tompkins,
U. of P., Moore School of Electrical Engineering

4.1: Low-Level, High-Speed Voltage Comparator
H. H. Douglass and J. W. Higginbotham, The Martin Company, Baltimore, Md.

The need for low-level high-speed accurate voltage comparators exists in applications such as missiles, automatic checkout equipment and analog computers. This paper discusses a technique for increasing the response speed and bandwidth of the comparator amplifier by use of an internally generated carrier frequency. Circuits using these principles have been tested from −55°C to +75°C with a change of ±1% in the error-switching point. Errors as low as 200 microamperes can be made to switch 10 amperes in 200 microseconds.

4.2: A High Speed Analogue Multiplier with a Linearity of Better than ±0.3%
R. J. Bibby and P. M. Thompson, Defense Research Telecommunications Establishment, Ottawa, Canada.

This paper describes the design and overall operation of a four-quadrant multiplier, which makes use of transistor and semiconductor diode properties and will handle inputs from dc to 10 kc. It is insensitive to changes in components and has a linearity better than ±0.3% from −50° to +70°C.

4.3: A Semiconductor Voltage Regulator for Rotating Generators
James L. Jensen, Minneapolis-Honeywell Regulator Co., Hopkins, Minn.

An analysis of a new circuit which performs the functions of voltage regulation, current limiting and reverse current cutoff of rotating generators with semiconductor control elements. The circuit uses no moving parts, vibrating contacts or carbon piles. Improved performance with high reliability and immunity to environmental effects are obtained.

4.4: A Transistorized Overload-Proof Electronic Regulator
Paul A. Dodge, General Electric Co., Syracuse, N. Y.

The optimum output characteristics of a regulated power supply have been determined, and a circuit has been invented to provide them. The regulator permits a supply having: Approximately zero output impedance, a maximum available load current, negligible current into a short circuit, and automatic electronic regression into (and recovery out of) overload.

6:00-7:30 P.M.: Cocktail-Buffet Dinner—Sheraton Hotel

8:00 P.M.: Informal Discussion Sessions—Sheraton Hotel
Power Control—Howard T. Mooers, Minneapolis-Honeywell Reg. Co.
Transistor Switching and Logic Circuits—R. H. Baker, Lincoln Lab., MIT
New and Future Solid-State Devices, Their Properties and Applications
R. B. Adler (MIT), J. B. Angell (Philco), J. M. Early (BTL), H. W. Katz (G.E.), R. L. Pritchard (Texas Inst.), W. M. Webster (RCA)
Reliability—W. D. Rowe, Westinghouse

Solid-State Circuits Conference

..IRE Philadelphia Section..AIEE Philadelphia Section and the University of Pennsylvania

FRIDAY, FEBRUARY 21, 1958

MORNING SESSIONS

SESSION V: Linear Application

Irvine Auditorium—9:00 A.M.-12:00 Noon

Chairman: John G. Linvill, Stanford University, Stanford, Calif.

5.1: Methods of Designing and Cascading Unneutralized Tuned-Transistor Amplifiers

Robert M. Frazier, Jr., Westinghouse Electric Corp., Baltimore, Md.

A proper choice of driving and terminating conductances combined with tuned circuits at the input and output terminals of an inherently unstable transistor can insure a desired stability and provide the maximum gain for that stability. This paper describes practical methods of designing and cascading tuned stages which have been stabilized by this method of mismatching.

5.2: Transistor 70-Mc IF Amplifier

V. R. Saari, Bell Telephone Laboratories, Murray Hill, N. J.

A 70-mc if amplifier using seven diffused-base germanium transistors is described. The insertion gain is 90 db, with bandwidth greater than 15 mc flat to within ±0.2 db. The +12 dbm output is stabilized against change in input level or temperature by 35 db of agc, and the noise figure is 5 db. A digital computer accurately predicted the circuit performance.

5.3: Optimum Noise Performance of Transistor Input Circuits

R. D. Middlebrook, E.E. Dept., California Institute of Technology, Pasadena, Calif.

Some results are presented for optimum noise performance of transistor input stages when fed from resistive or reactive sources. Expressions are developed for minimum noise figure and optimum source resistance in the presence of base bias resistors, emitter degeneration resistance, and various kinds of feedback. It is shown that for an inductive source, such as a magnetic tape head, there is a maximum signal-to-noise ratio obtainable with an optimum source inductance.

5.4: The Advantages of Tetrode Geometry for Power Transistors

Stability—The Control of Amplified Leakage Current

H. T. Mooers, Minneapolis-Honeywell Regulator Co.

Linearity—A Simple Direct Coupled High Quality Amplifier

J. T. Maupin, Minneapolis-Honeywell Regulator Co., Minneapolis, Minn.

The tetrode construction, when used in power transistors, provides a unit of exceptional stability and linearity, making possible direct coupled circuits with very low distortion. The stability factor may be made to approach unity without cumbersome interstage networks, and the linearity is achieved by tetrode biasing and balancing the signal between the two bases.

5.5: Dielectric Modulators Using the Space-Charge Capacitance of Junction Diodes

C. R. Hurtig, Research Laboratory of Electronics, M.I.T., Cambridge, Mass.

A low-level dc to ac modulator which uses the space-charge capacitance of silicon junction diodes is described. Theoretical values for the temperature coefficient of capacitance, conversion gain, and noise figure are derived. Experimental results for a bandwidth of 5000 cps yield a minimum detectable power of the order of thermal noise and an input impedance of 50 megohms at room temperature.

SESSION VI: Tutorial Survey

University Museum—9:00 A.M.-12:00 Noon

Chairman: J. J. Suran, General Electric Co., Syracuse, N. Y.

6:1: A Survey of Solid-State Logic Circuitry

E. Gary Clark, Burroughs Corp., Paoli, Pa.

6.2: Power Control With Semiconductors

Louis Bright, Westinghouse, Pittsburgh, Pa.

LUNCH: 12:00 Noon to 1:30 P.M.—University Museum

AFTERNOON SESSIONS

SESSION VII: New Devices

Irvine Auditorium—2:00-4:30 P.M.

Chairman: George Royer, IBM, Poughkeepsie, N. Y.

7.1: Operation of a Low-Temperature Memory Element

C. J. Kraus, IBM, Kingston, N. Y.

The cryogenic memory which has been developed by IBM's KMPD Development Laboratory can be readily adapted to two different modes of operation. The operation in one mode, the destructive readout mode, requires logic very similar to that of a core memory. The other mode of operation is known as non-destructive readout. Due to the uniqueness of this system, a detailed analysis of operation in this mode is included.

7.2: The Application of the Dynistor Diode to Off-On Controllers

P. F. Pittman, Westinghouse Electric Corp., Pittsburgh, Pa.

The Westinghouse dynistor diode is a new semiconductor device which exhibits a nondestructive voltage breakdown when biased in the reverse direction. The unique characteristics of this device make it suitable for use as a nonlinear power amplifier. Since the characteristics of the dynistor are so different from those of conventional semiconductor devices, completely new techniques must be developed to control the device.

7.3: Diode Amplifiers

H. W. Abbott and L. D. Wechsler, Electronics Laboratory, General Electric Co., Syracuse, N. Y.

Significant power gains have been achieved with junction diodes utilizing their reverse transient characteristics. Three basic diode amplifier configurations have been developed with operating characteristics similar to the common base, common emitter and common collector transistor stage. A linear analysis of these configurations is presented. Results are presented in a fashion which establishes the criteria responsible for circuit performance and permits intelligent selection of circuit parameters by design engineers.

7.4: Magnetoresistive Amplifiers and Second Harmonic Modulators

H. N. Putschi, Electronics Laboratory, General Electric Co., Syracuse, N. Y.

This paper gives an analysis of design criteria, achievable power gain and frequency range of magnetoresistive amplifiers and second harmonic modulators of a simple type. Experimental data are limited to proof of feasibility. These amplifiers can be designed to have a wide range of input impedances. Their output impedances are very low. With the structures described in this paper, amplifier operation is unilateral.

7.5: Photoelectric Circuit Applications

S. K. Ghandhi, Electronics Laboratory, General Electric Co., Syracuse, N. Y.

A study is made of the properties of electroluminescent cells and photoconductors, and of the applications of these elements to the design of computer circuits. This paper is confined to a study of circuits that are primarily electrical in nature; e.g., the inputs and outputs take the form of electrical signals and light is used as an intermediate actuating source.

1958 TRANSISTOR AND SOLID-STATE CIRCUITS CONFERENCE

Scope of Conference

THE 1958 TRANSISTOR and Solid-State Circuits Conference will feature sessions devoted to solid state circuits for computers, switching, and linear applications. Other sessions will be devoted to new techniques and new devices. There will also be two tutorial-survey sessions to provide those working in transistor and solid-state circuitry with an up-to-date report on the state of the art.

INFORMAL SESSIONS conducted by the nation's foremost specialists on Thursday evening will be held to provide all registrants an opportunity to discuss power control, switching and logic, future solid-state devices and applications, and reliability.

A BOOKLET, containing illustrations and substantial abstracts of the technical papers, will be furnished without charge to each registrant at the time of registration.

Location

THE CONFERENCE will be held on the campus of the University of Pennsylvania in the Irvine Auditorium and in the University Museum.

IRVINE AUDITORIUM is located at the northwest corner of 34th and Spruce Streets; the University Museum is just east of the southeast corner of 34th and Spruce Streets, Philadelphia, Pennsylvania. Central Philadelphia is easily reached by bus route 42, and the 30th Street station of the Pennyslvania Railroad is less than a mile from the University Campus.

THE INFORMAL Thursday evening sessions will be held in the Sheraton Hotel.

Registration

REGISTRATION AND HOTEL reservation forms are enclosed with this Conference announcement. Additional forms may be obtained from Joseph Veasey, Philco Corp., 4700 Wissahickon Avenue, Philadelphia 44, Pa.

Fees for the Conference are:

	Advance—Before Feb. 13, 1958	At Conference—or After—Feb. 13, 1958
Registration, Member AIEE, IRE:	$4.00	$5.00
Non-Member:	5.00	6.00
Thursday Lunch:	2.75	3.25
Friday Lunch:	2.75	3.25
Cocktail Party:	2.50	3.00
Buffet Dinner:	6.50	7.00
Combination Cocktail Party and Buffet Dinner:	8.50	9.50

Full-time students will be registered free of charge for the technical sessions.

All technical sessions will start promptly at 9:30 A.M. on February 20. To avoid delays in registration and to assist the local arrangements committee, advance registration and meal purchases are strongly recommended.

Accommodations

PHILADELPHIA'S NEW SHERATON Hotel at 1725 Pennsylvania Boulevard, chosen as Conference headquarters, has reserved a block of rooms for those attending the Conference. This luxurious new hotel is located in central Philadelphia with offices of most major airlines within one-half block (several in the hotel). Railroads to all points are convenient to the hotel, and ample indoor parking facilities are reached via underground concourse.

The Cocktail Party and Buffet Dinner will be held at the Sheraton on Thursday evening.

Luncheons on Thursday and Friday will be served to a limited number in the University Museum. Philadelphia offers many fine restaurants for those who do not wish to attend the luncheons or buffet dinner.

National Committee

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