1957 TRANSISTOR AND SOLID STATE CIRCUITS CONFERENCE

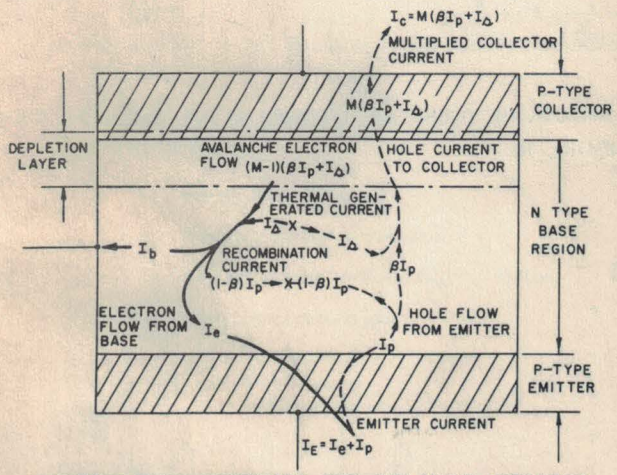
1.1 A DECADE RING COUNTER USING AVALANCHE-OPERATED JUNCTION TRANSISTORS

J. E. Lindsay – Radio Corp. of America, Camden

1. IMPROVED SWITCHING TIMES
2. CURRENT CONTROLLED N-TYPE NEGATIVE RESISTANCE CHARACTERISTICS SUITABLE FOR BISTABLE OPERATION
3. AVALANCHE-DERIVED PROPERTIES RELATIVELY INSENSITIVE TO TEMPERATURE CHANGE
4. IMPORTANT FEATURES CAN BE DESCRIBED ANALYTICALLY

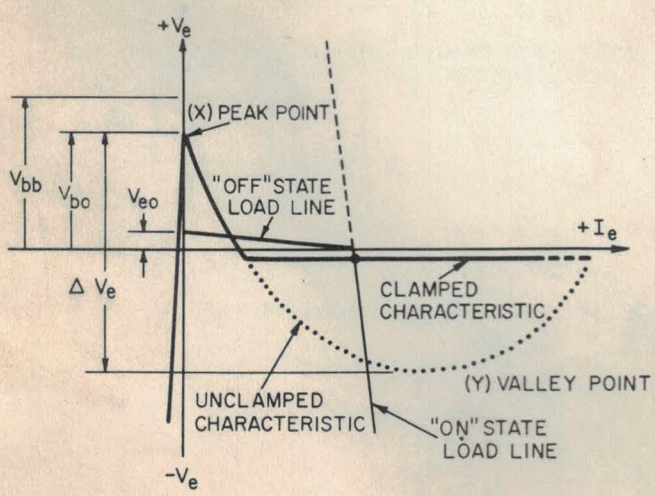
SUMMARY OF AVALANCHE CHARACTERISTICS

FIGURE 1



CURRENT FLOW SCHEMATIC FOR AVALANCHE OPERATION

FIGURE 3



EMITTER INPUT CHARACTERISTIC AND LOAD LINES FOR THE BISTABLE FLIP-FLOP

FIGURE 5

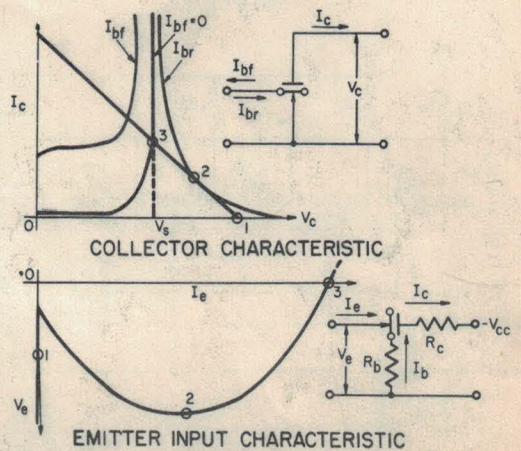
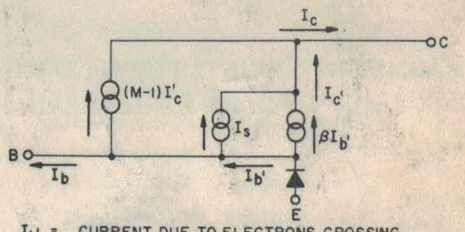


FIGURE 2



$I_{b'}$ = CURRENT DUE TO ELECTRONS CROSSING EMITTER JUNCTION

$\beta I_{b'}$ = HOLE CURRENT FROM EMITTER JUNCTION

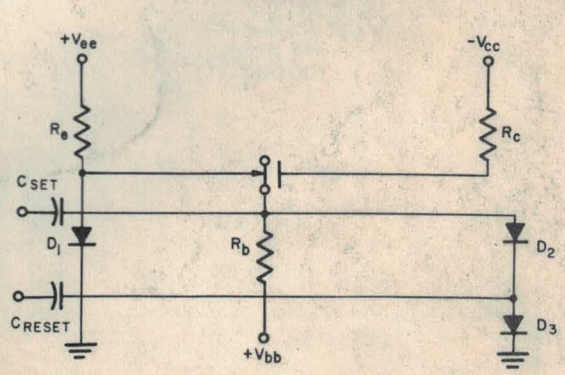
I_s = THERMAL CURRENT

$I_{c'}$ = HOLE CURRENT INTO COLLECTOR JUNCTION

$(M-1)\ I_{c'}$ = CURRENT FROM AVALANCHE MULTIPLICATION AT COLLECTOR JUNCTION

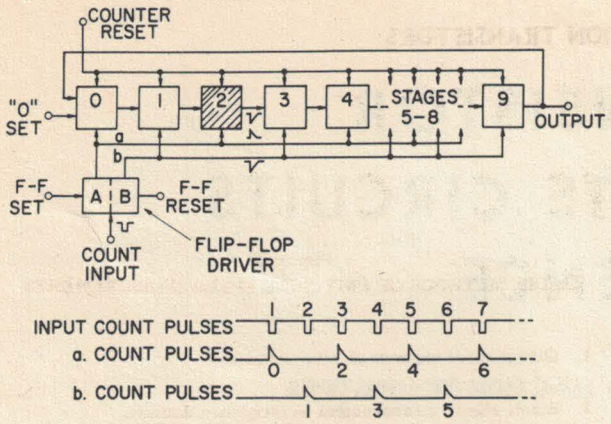
AN EQUIVALENT CIRCUIT FOR AVALANCHE OPERATION

FIGURE 4



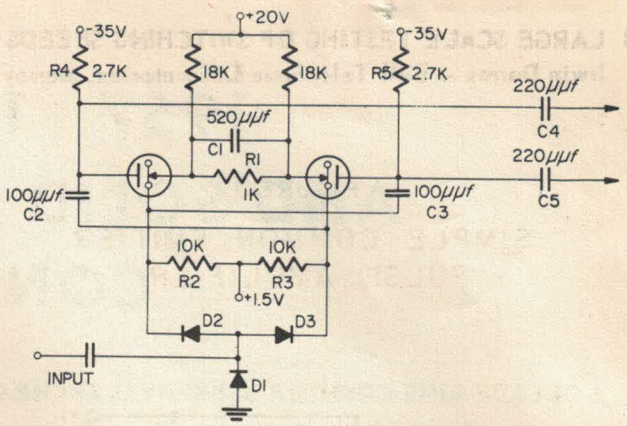
BISTABLE FLIP-FLOP

FIGURE 6



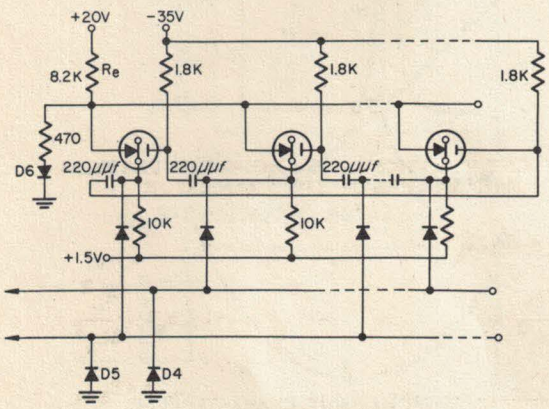
DUAL COUNT-TRANSFER COUNTER SYSTEM

FIGURE 7



DECADE COUNTER DRIVER

FIGURE 8



DECADE RING COUNTER

FIGURE 9

AVALANCHE BREAKDOWN

$$I_{co} = M I_s = \frac{1}{1-\left(\frac{V_c}{Vbd}\right)^n} I_s$$

AVALANCHE SUSTAIN VOLTAGE

$$V_s = \frac{Vbd}{(\beta+1)^{\frac{1}{n}}}$$

AVALANCHE CURRENT GAIN

$$\alpha' = \frac{\alpha}{1-\left(\frac{V_c}{Vbd}\right)^n} \qquad \beta' = \frac{\beta}{1-\left(\frac{V_c}{V_s}\right)^n}$$

FORMULAE FOR AVALANCHE OPERATION

FIGURE 10

COMMON EMITTER OUTPUT RESISTANCE

$$r'_d = \frac{\left(\frac{V_s}{V_c}\right)^n - 1}{n} \frac{V_c}{I_c} \approx \frac{1}{n} \frac{V_c}{I_c}$$

EMITTER INPUT CHARACTERISTIC

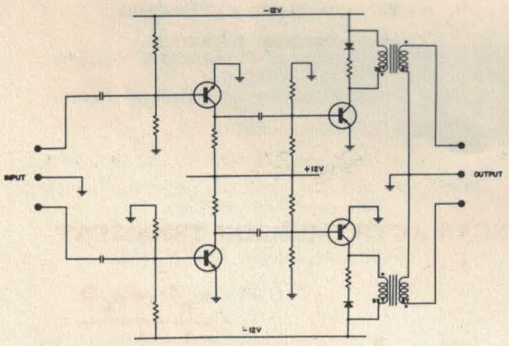
$$V_e = I_e \left[\frac{\left(\frac{V_s}{Vbd}\right)^n - \left(\frac{V_c}{Vbd}\right)^n}{1-\left(\frac{V_c}{Vbd}\right)^n} \right] R_b - I_{LO} R_b$$

FORMULAE FOR AVALANCHE OPERATION

FIGURE 11

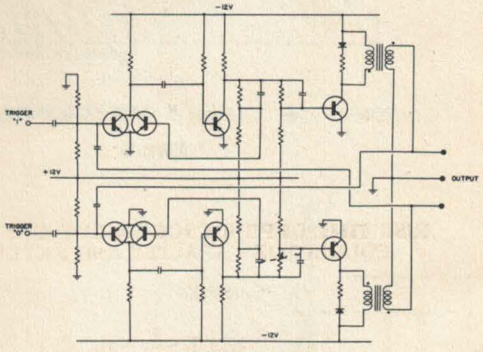
1.2 TRANSISTOR CIRCUITS FOR MAGNETIC DRUM RECORDING

G. R. Kuster – Ferranti Electric Limited, Toronto



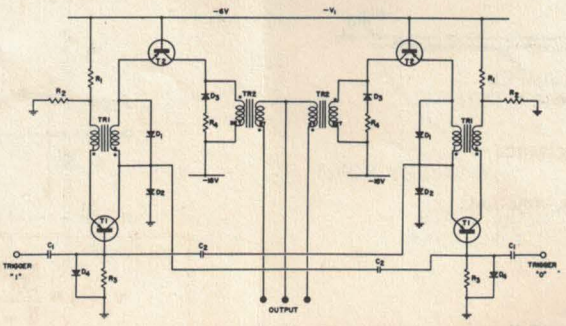
WRITE AMPLIFIER

FIGURE 1



POWER ONE-SHOT

FIGURE 2



BLOCKING OSCILLATOR

FIGURE 3

1.3 LARGE SCALE TESTING OF SWITCHING SPEEDS OF JUNCTION TRANSISTORS

Irwin Dorros – Bell Telephone Laboratories, Murray Hill

FIGURE I

SIMPLE COMMON EMITTER
PULSE AMPLIFIER

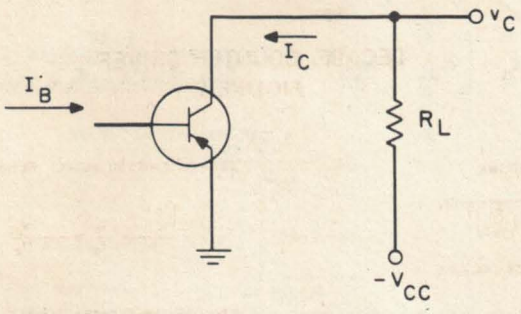


Figure 3
APPROXIMATION OF THE FREQUENCY DEPENDENCE OF ALPHA

$$\alpha(\omega) \approx \frac{\alpha_o e^{-j\omega\delta}}{1 + j\,\omega/\omega_n}$$

ω_n = cut-off radian frequency

α_o = d.c. short circuit current gain

δ = time delay factor such that $\delta\omega_n = .2$ radians

$\alpha(\omega)$ = short circuit current gain

Figure 2
THREE METHODS OF SWITCHING SPEED MEASUREMENTS

1. Direct measurement of rise time.
2. Small signal measurement in frequency domain.
3. Large signal slow speed measurement in the time domain.

Figure 4

PERTINENT RELATIONSHIPS AMONG THE PHYSICAL PARAMETERS OF THE TRANSISTOR

$$W_o \approx \left\{ d - f(\sqrt{v_c}) \right\}$$

$$\omega_n \approx \frac{2D_h}{W_o^2} \qquad (1 - \alpha_o) \approx \frac{W_o^2}{2L_b^2}$$

$$\alpha_o \approx \frac{1}{1 + \frac{W_o^2}{2L_b^2}} \qquad L_b = \sqrt{D_h \tau_h}$$

W_o = effective base width
d = actual base material width
v_c = collector junction voltage
D_h = diffusion constant in base region
L_b = diffusion length
τ_h = mean hole lifetime in the base
(pnp transistor assumed)

Figure 5

RISE TIME DEPENDENCE ON CUT-OFF FREQUENCY, COLLECTOR CAPACITY AND EXTERNAL LOAD

$$t_o = K\left(\frac{1}{\omega_n} + R_L C_c\right)$$

t_o = rise time

R_L = load resistance

C_c = collector capacitance

K = proportionality constant

Figure 6

LINEAR ACTIVE REGION TRANSIENT

$$v_c(t) = I_B R_L \frac{\alpha_o}{1 - \alpha_o}\left(1 - e^{-\frac{\omega_n(1 - \alpha_o)t}{1 + \delta\omega_n}}\right) - V_{cc}$$

$$\begin{cases} \omega_n(1 - \alpha_o) \approx 1/\tau_h \\ \omega_n\delta \approx .2 \\ \alpha_o \approx 1 \end{cases}$$

$$v_c(t) \approx \frac{I_B R_L}{1 - \alpha_o}\left(1 - e^{-t/1.2\tau_h}\right) - V_{cc}$$

FIGURE 7

SWITCHING TRANSIENT
CONSIDERING COLLECTOR VOLTAGE VARIATIONS

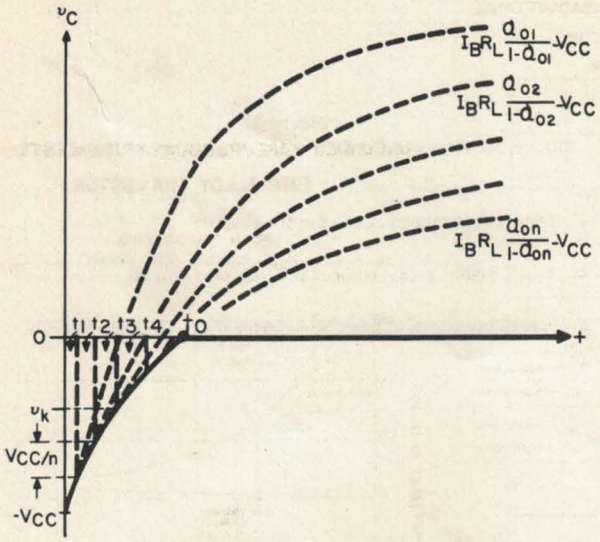
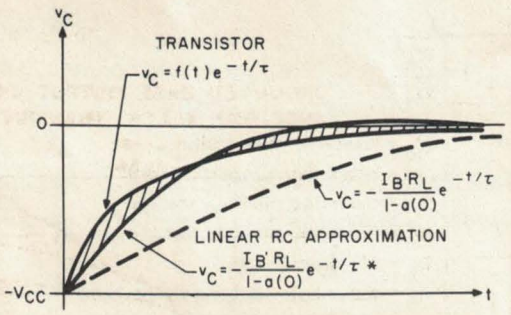


FIGURE 9

LINEAR RC APPROXIMATION TO TRANSISTOR TRANSIENT



SHADED AREA IS THE DIFFERENCE BETWEEN THE CURVES

$$\frac{-I_B' R_L}{1-\alpha_0(0)} e^{-t/\tau *} = -V_{CC} e^{-t/RC}$$

FIGURE 11
FULLY AUTOMATIC SYSTEM FOR MEASURING RISE TIME ON A SLOW SPEED BASIS

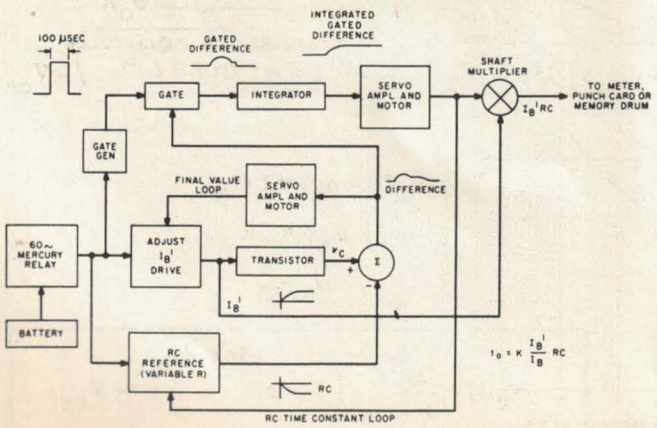


Figure 8

CALCULATION OF RISE TIME ON A SMALL SIGNAL BASIS

$$\frac{dv_{ck}}{dt} = \frac{I_B R_L \omega_{nk}}{1.2}$$

$$t_k = \frac{1.2 V_{cc}}{n I_B R_L \omega_{nk}}$$

$$t_o = \sum_{k=1}^{n} t_k$$

$$t_o = \left[W_{01}^2 + W_{02}^2 + \ldots + W_{on}^2 \right] \frac{1.2 V_{cc}}{2 D_h I_B R_L n}$$

$$t_o = \frac{1.2 V_{cc}}{I_B R_L \overline{\omega_n}}$$

Figure 10

CALCULATION OF RISE TIME ON THE LARGE SIGNAL BASIS

$$v_c(t) = f(t) e^{-t/\tau}$$

$$v_c(t) \approx \frac{-I_B' R_L}{1 - \alpha_0(0)} e^{-t/\tau *} = -V_{cc} e^{-t/RC}$$

$$\tau * = \frac{1}{K} \tau$$

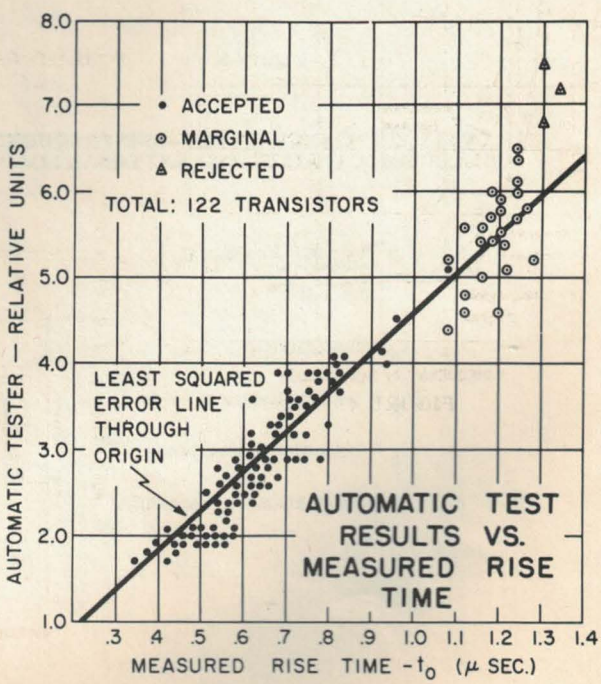
Equating coefficients and exponents:

$$\frac{I_B' R_L K}{[1 - \alpha_0(0)]\tau} = \frac{V_{cc}}{RC}$$

$$\overline{\omega_n} = \frac{1.2 V_{cc}}{RC I_B' R_L K'}$$

$$\boxed{t_o = K' RC \frac{I_B'}{I_B}}$$

FIGURE 12



1.4 EFFECTS OF LOW TEMPERATURES ON TRANSISTOR CHARACTERISTICS

A. B. Credle – IBM, Poughkeepsie

GROUNDED BASE OUTPUT ADMITTANCE
PNP ALLOY TRANSISTOR

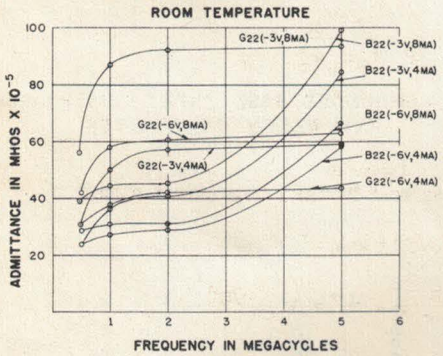


FIGURE 1

GROUNDED BASE REVERSE TRANSADMITTANCE
PNP ALLOY TRANSISTOR

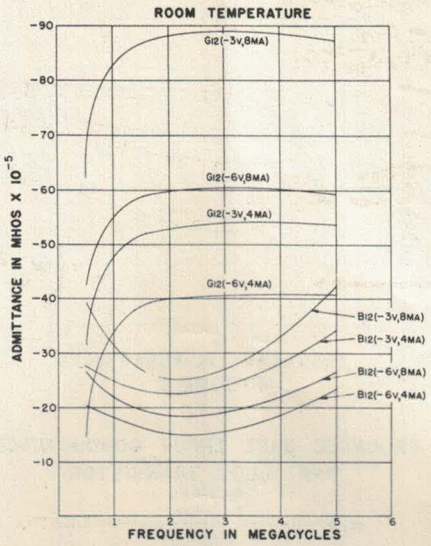


FIGURE 2

GROUNDED BASE FORWARD TRANSADMITTANCE
PNP ALLOY TRANSISTOR

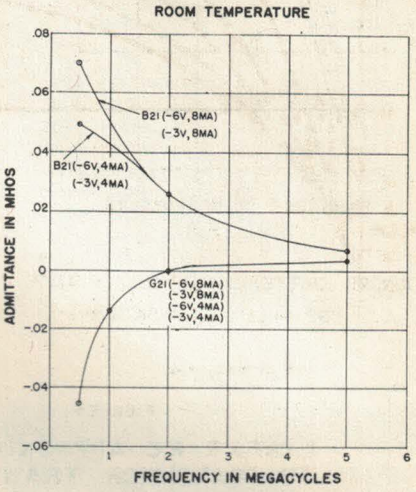


FIGURE 3

GROUNDED BASE PNP ALLOY TRANSISTOR
EQUIVALENT CIRCUITS

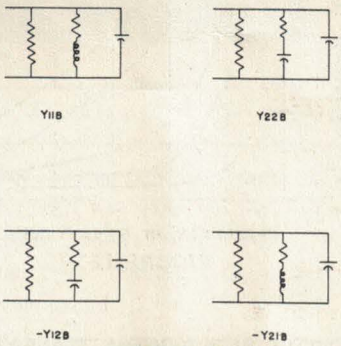


FIGURE 5

GROUNDED BASE INPUT ADMITTANCE
PNP ALLOY TRANSISTOR

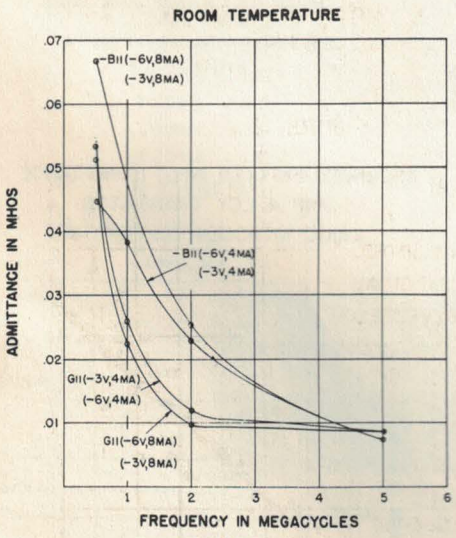


FIGURE 4

GROUNDED BASE OUTPUT SUSEPTANCE
PNP ALLOY TRANSISTOR
V_{CB} = -6
I_E = 4MA

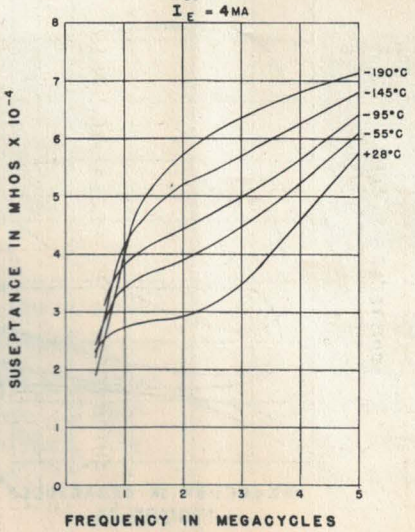


FIGURE 7

GROUNDED BASE OUTPUT CONDUCTANCE PNP ALLOY TRANSISTOR
V_{CB} = -6 V
I_E = 4 MA

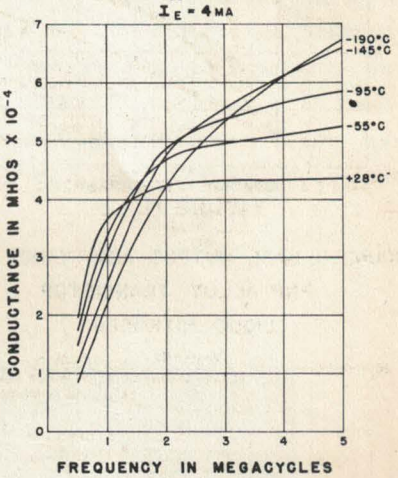


FIGURE 6

GROUNDED BASE REVERSE TRANS - CONDUCTANCE PNP ALLOY TRANSISTOR

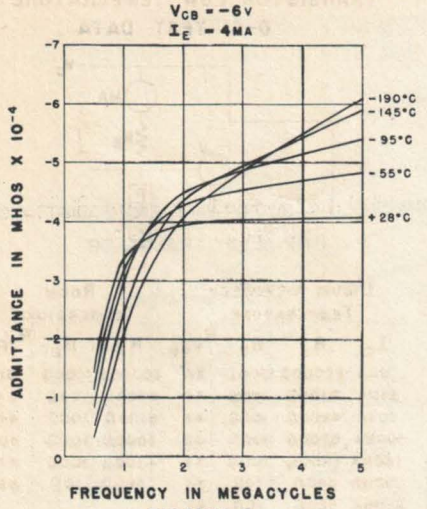


FIGURE 8

GROUNDED BASE REVERSE TRAN- SUSEPTANCE PNP ALLOY TRANSISTOR

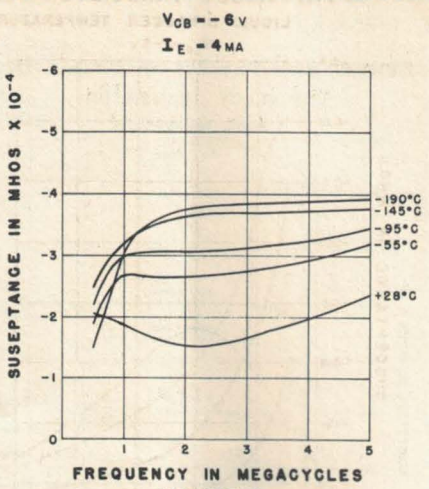


FIGURE 9

GROUNDED EMITTER INPUT CONDUCTANCE PNP ALLOY TRANSISTOR

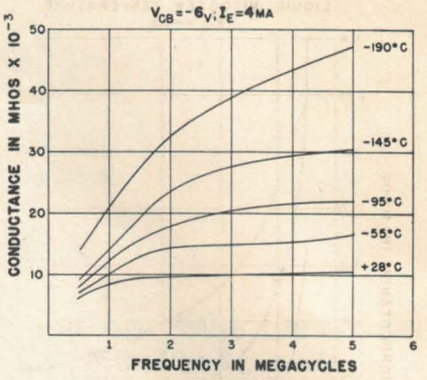


FIGURE 10

GROUNDED EMITTER INPUT SUSCEPTANCE PNP ALLOY TRANSISTOR

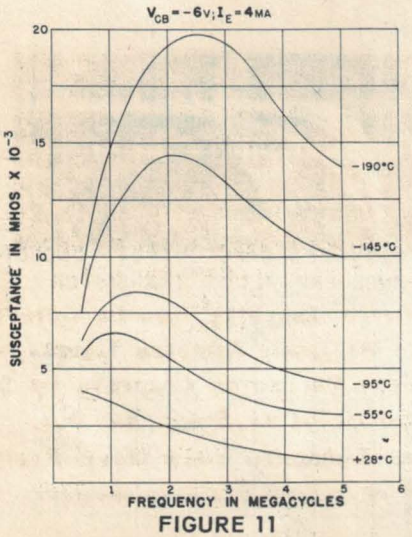


FIGURE 11

GROUNDED BASE INPUT CONDUCTANCE PNP ALLOY TRANSISTOR

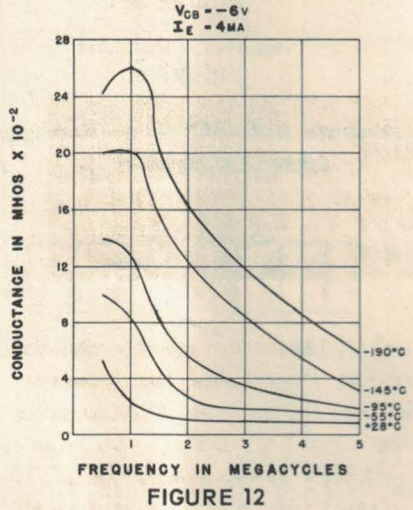


FIGURE 12

GROUNDED BASE INPUT SUSEPTANCE PNP ALLOY TRANSISTOR

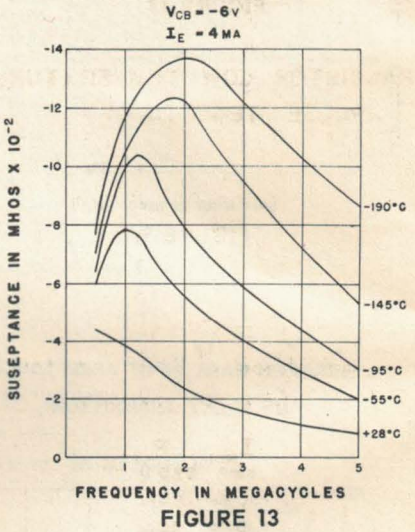


FIGURE 13

GROUNDED BASE OUTPUT ADMITTANCE PNP ALLOY TRANSISTOR LIQUID NITROGEN

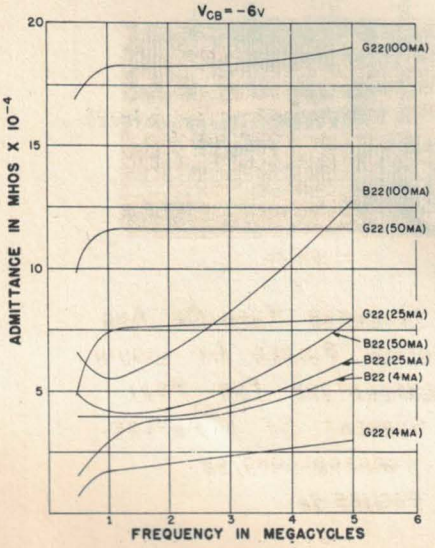


FIGURE 14

GROUNDED BASE REVERSE TRANSADMIT TANCE PNP ALLOY TRANSISTOR

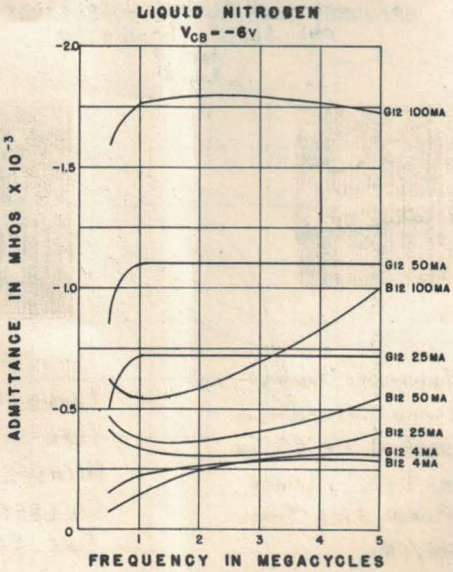


FIGURE 15

GROUNDED EMITTER INPUT ADMITTANCE PNP ALLOY TRANSISTOR LIQUID NITROGEN TEMPERATURE

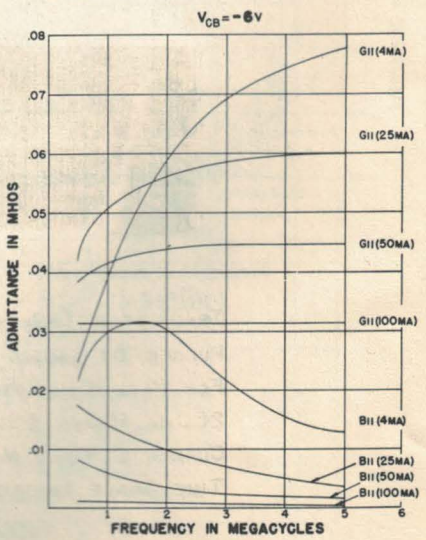


FIGURE 16

GROUNDED BASE INPUT CONDUCTANCE
PNP ALLOY TRANSISTOR
LIQUID NITROGEN TEMPERATURE
$V_{CB} = -6$ v

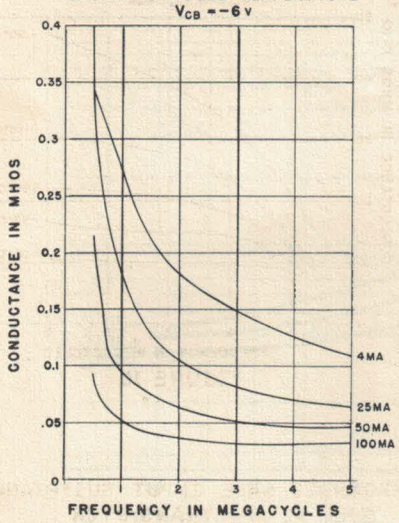


FIGURE 17

GROUNDED BASE INPUT SUSCEPTANCE
PNP ALLOY TRANSISTOR
LIQUID NITROGEN TEMPERATURE
$V_{CB} = -6$ v

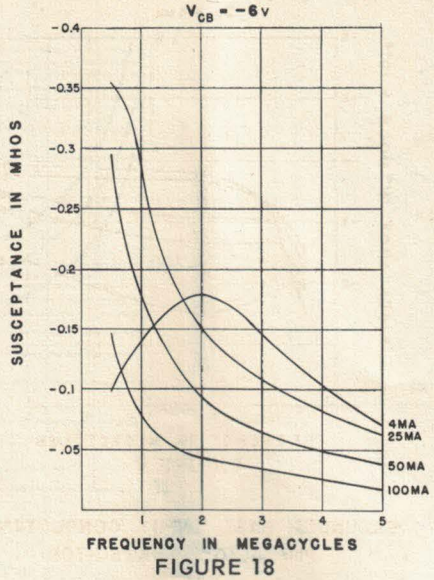
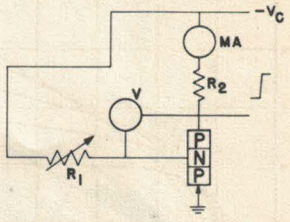


FIGURE 18

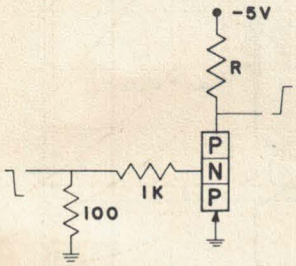
TRANSISTOR LOW TEMPERATURE
D-C TEST DATA



	Liquid Nitrogen Temperature			Room Temperature		
I_C	R_1	R_2	R_1/R_2	R_1	R_2	R_1/R_2
8MA	200000Ω	1000Ω	20	60000Ω	1000Ω	60
25MA	3300Ω	100Ω	33	6400Ω	100Ω	64
50MA	4200Ω	100Ω	42	6100Ω	100Ω	61
100MA	5200Ω	100Ω	52	5000Ω	100Ω	50
150MA	5400Ω	100Ω	54	4200Ω	100Ω	42
200MA	540Ω	10Ω	54	360Ω	10Ω	36
250MA	520Ω	10Ω	52			
500MA	300Ω	10Ω	30			
1000MA	200Ω	10Ω	20			

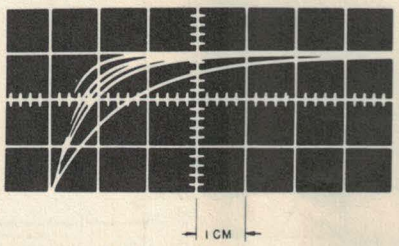
FIGURE 19

TRANSISTOR LOW TEMPERATURE
PULSE TEST DATA



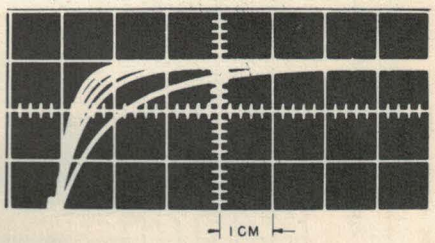
I_C	R
8MA	620Ω
50MA	100Ω
100MA	50Ω
250MA	20Ω
500MA	10Ω
1000MA	5Ω

FIGURE 20



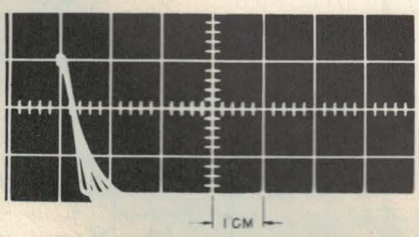
Transistor Inverter Turn-On Output Pulses For Peak Collector Current Of 8ma. And Transistor Temperatures Of -190°c., -145°c., -95°c., -45°c., And 28°c. Lower Temperatures Yield More Rapid Rise Time. Time Scale 2 microseconds/cm.

FIGURE 21



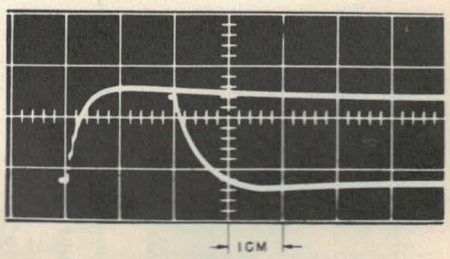
Transistor Inverter Turn-On Output Pulses At Liquid Nitrogen Temperature For Peak Collector Currents Of 500 ma., 250 ma., 100 ma., 50 ma., And 8 ma. Larger Currents Yield More Rapid Rise Time. Time Scale 1 microsecond/cm.

FIGURE 22



Transistor Inverter Turn-Off Output Pulses At Liquid Nitrogen Temperature For Peak Collector Currents Of 500ma., 250ma., 100ma., 50ma., And 8ma. Lower Currents Yield More Rapid Fall Time. Time Scale 1microsecond/cm.

FIGURE 23



Transistor Inverter Turn-On And Turn-Off Output Pulses At Liquid Nitrogen Temperature For Peak Collector Current Of 1 Ampere. Time Scale 1 microsecond/cm.

FIGURE 24

A.2 BIAS CONSIDERATIONS IN TRANSISTOR CIRCUIT DESIGN

Sorab K. Ghandhi – General Electric Company, Syracuse

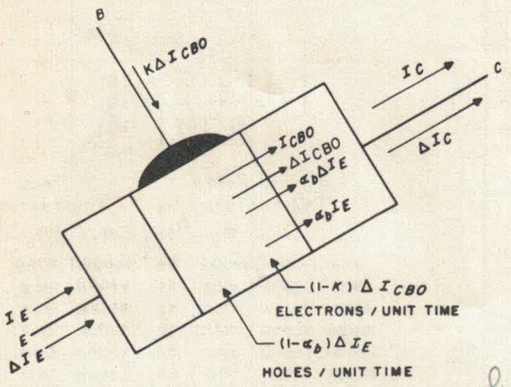


FIGURE 1

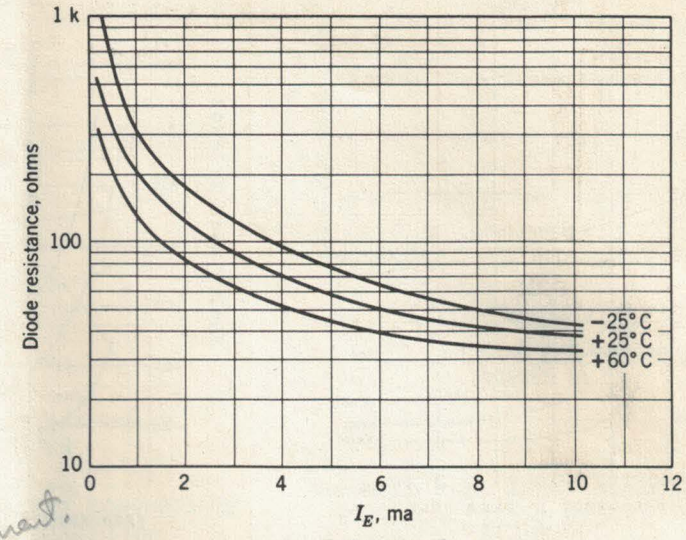


FIGURE 2

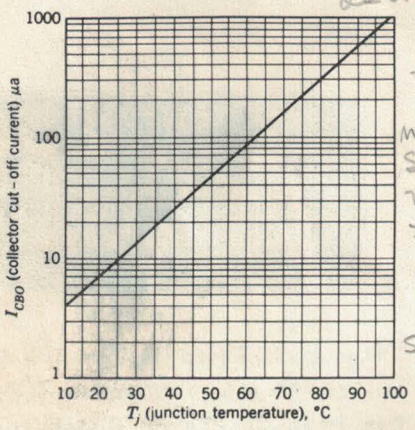


FIGURE 3

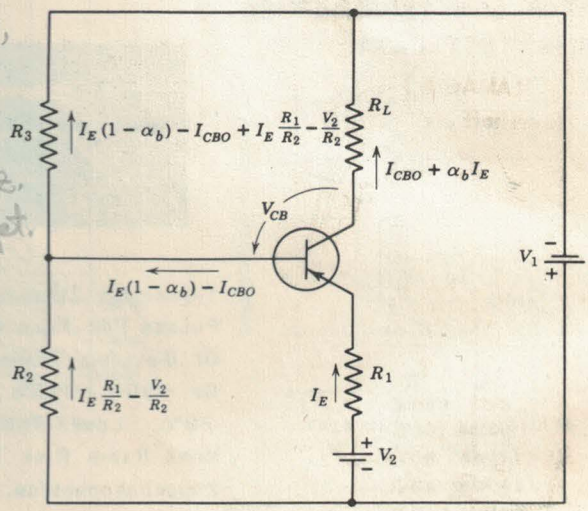
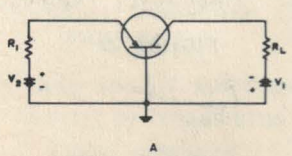
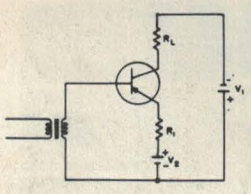


FIGURE 4





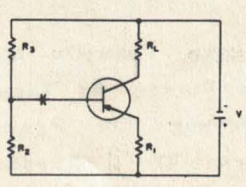


FIGURE 5

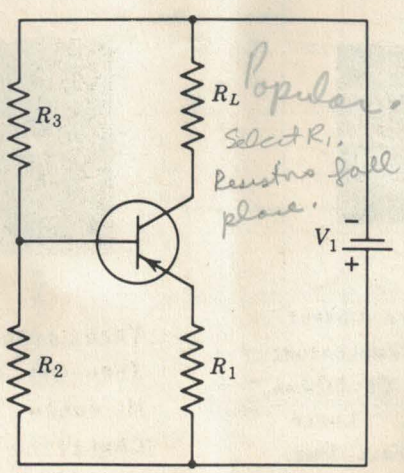


FIGURE 6

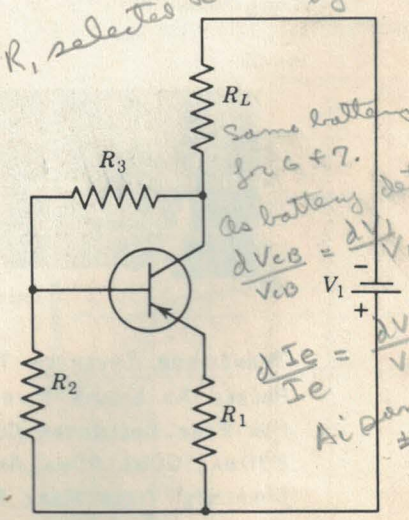


FIGURE 7

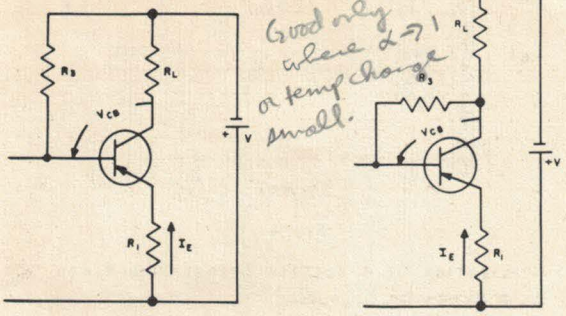


FIGURE 8

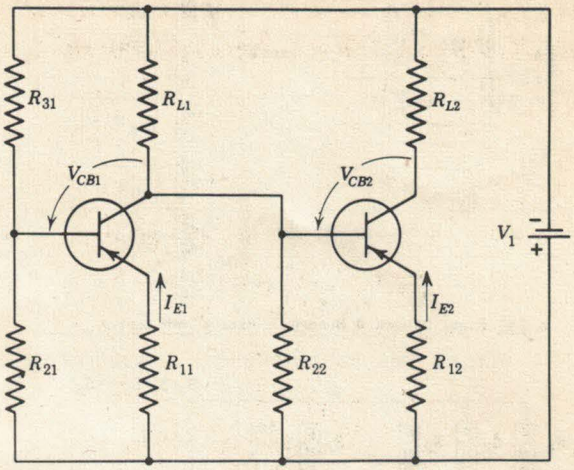


FIGURE 9

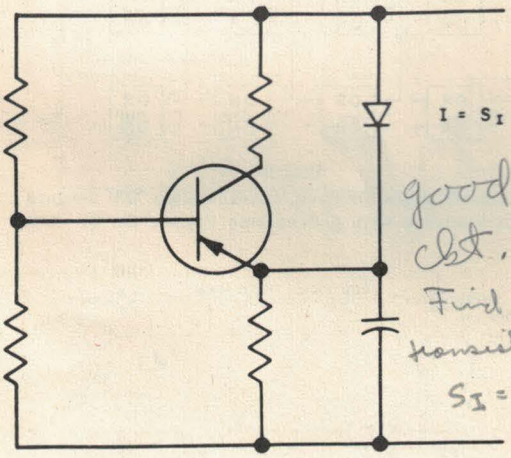


FIGURE 10

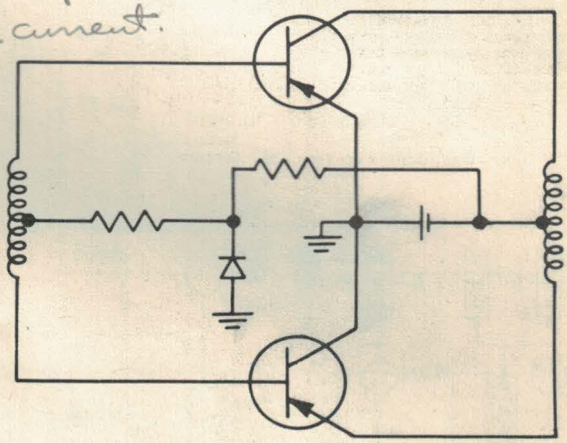
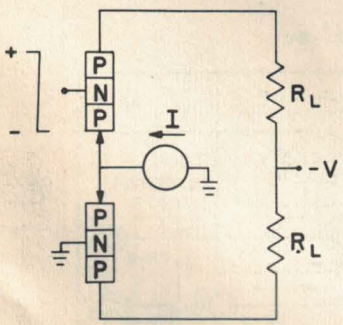


FIGURE 11

2.1 MILLIMICROSECOND TRANSISTOR CURRENT SWITCHING CIRCUITS

Hannon S. Yourke — IBM Research Center, Poughkeepsie



COLLECTOR CURRENT FOR ON TRANSISTOR = $\alpha I + I_{CO}$

COLLECTOR CURRENT FOR OFF TRANSISTOR = I_{CO}

FIG. 1

BASIC TRANSISTOR BLOCK

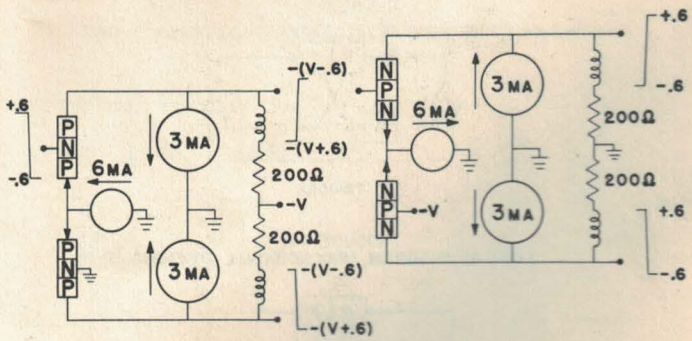


FIG. 2

NPN AND PNP BASIC TRANSISTOR BLOCKS WITH INPUT AND OUTPUT LEVELS SHOWN TO ILLUSTRATE COMPATIBILITY

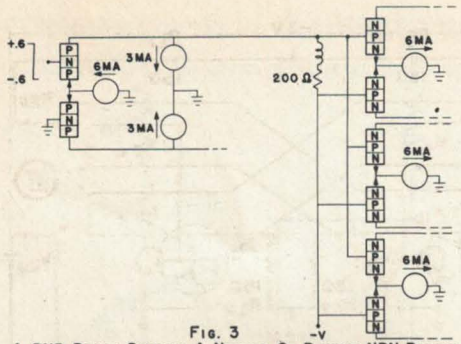


FIG. 3
A PNP BLOCK DRIVING A NUMBER OF REMOTE NPN BLOCKS.

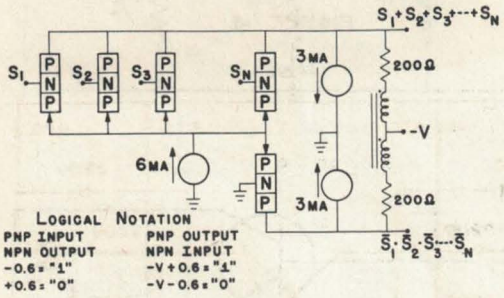


FIG. 5

"N"-WAY COMPLEMENTED "OR" CIRCUIT

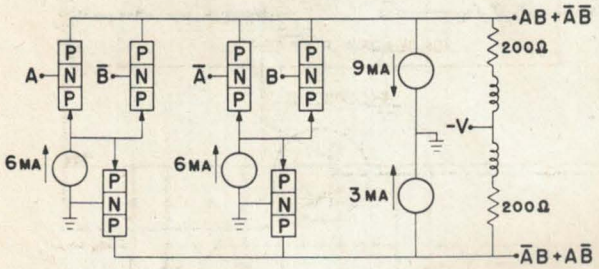


FIG. 11

SIX TRANSISTOR COMPLEMENTED EXCLUSIVE OR CIRCUIT

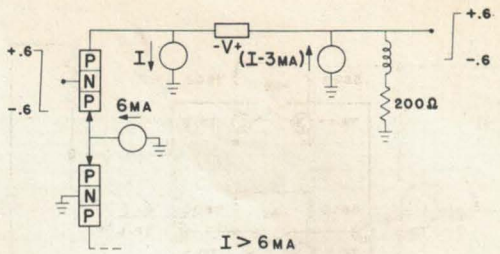


FIG. 4

APPLICATION OF A VOLTAGE TRANSLATING BLOCK AS A MEANS OF COUPLING.

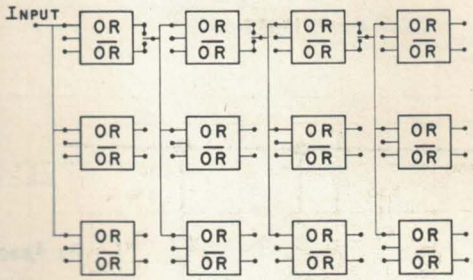


FIG. 9

BLOCK DIAGRAM OF FOUR COMPLEMENTED "OR" CIRCUITS IN SEQUENCE WITH A CASCADING FACTOR OF 3.

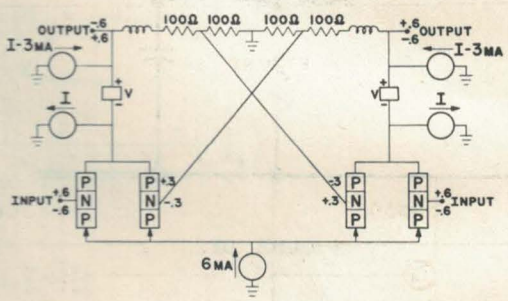


FIG. 12

ECCLES JORDAN TRIGGER WITH VOLTAGE TRANSLATE BLOCKS AND PULLOVER TRANSISTORS

2.2 DCTL COMPLEMENTING FLIP-FLOP CIRCUITS

E. Gary Clark – Burroughs Research Center, Paoli

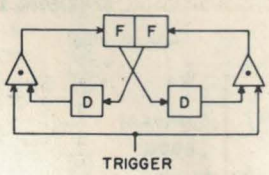


FIGURE 1-A
LOGICAL DIAGRAM, UNCONDITIONAL STEERING

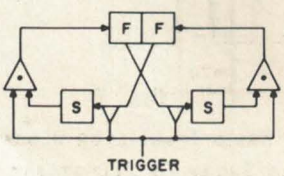


FIGURE 1-B
LOGICAL DIAGRAM, CONDITIONAL STEERING

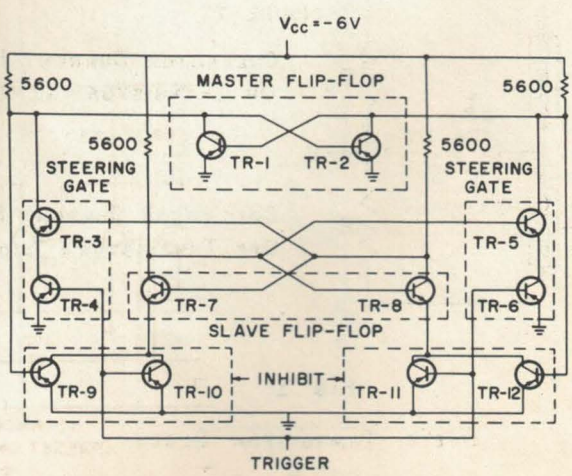


FIGURE 2

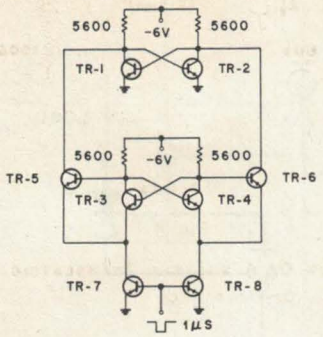


FIGURE 3

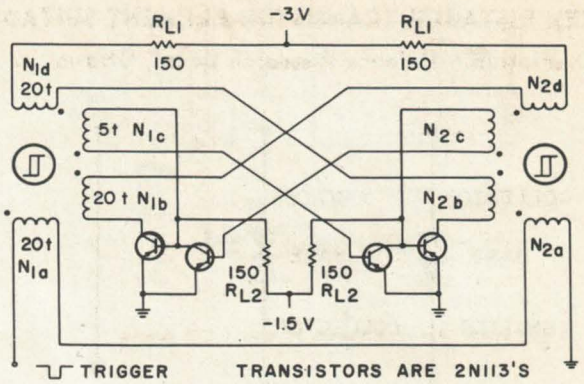


FIGURE 4

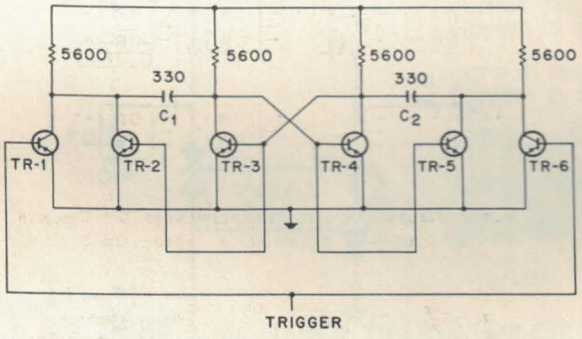


FIGURE 5

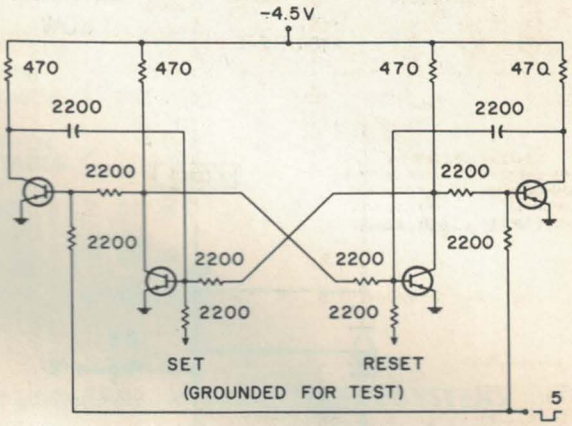
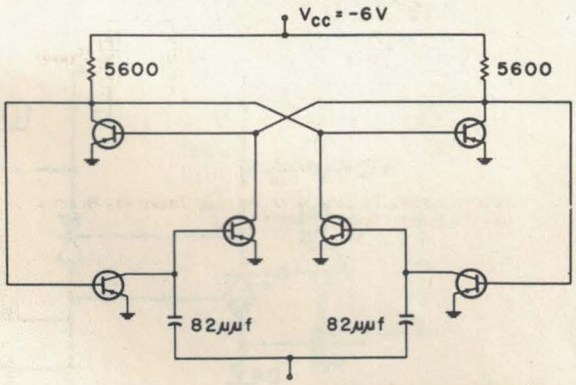


FIGURE 6



TRANSISTORS SB-100'S

FIGURE 7

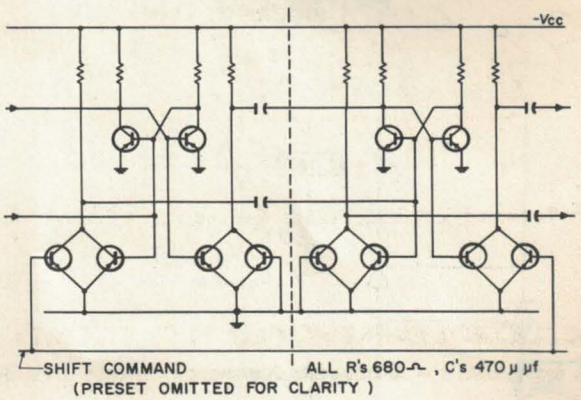


FIGURE 8

TWO STAGES, CONDITIONAL STEERING SHIFT REGISTER

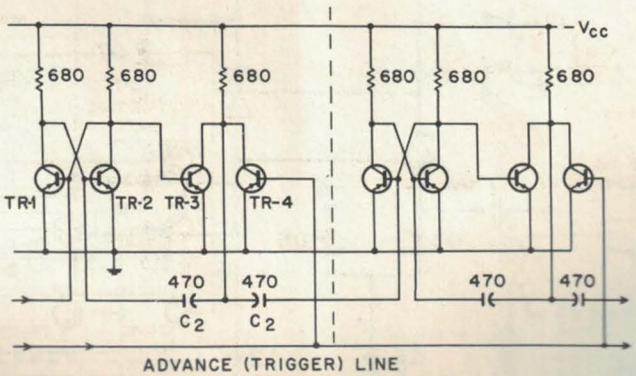


FIGURE 9

TWO STAGES, CONDITIONAL STEERING RING COUNTER

2.3 A NEW BISTABLE TRANSISTOR ELEMENT SUITABLE FOR DIGITAL COMPUTERS

C. D. Florida – Defence Research Board, Ottawa

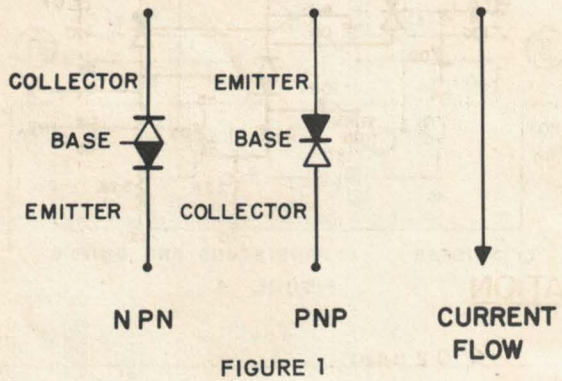


FIGURE 1

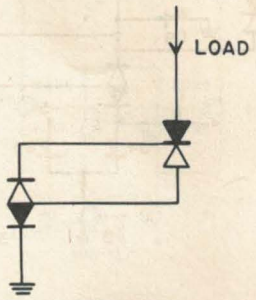


FIGURE 2

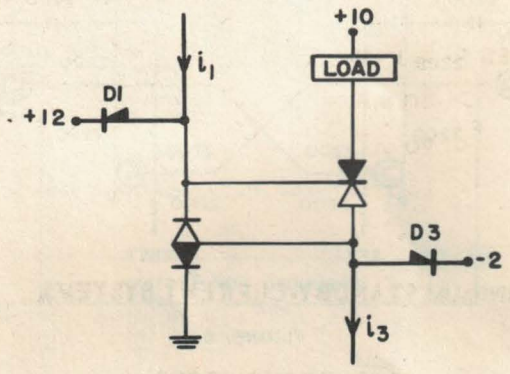


FIGURE 3

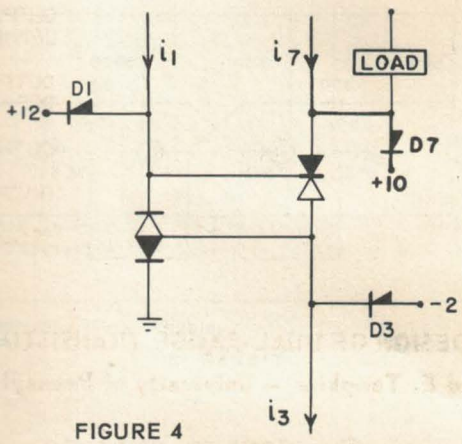


FIGURE 4

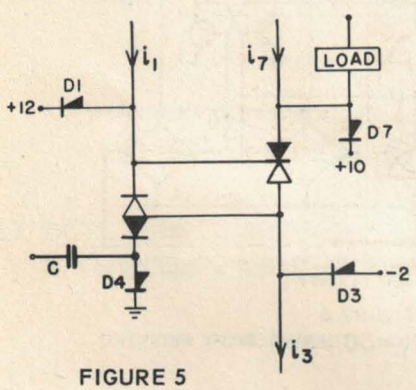


FIGURE 5

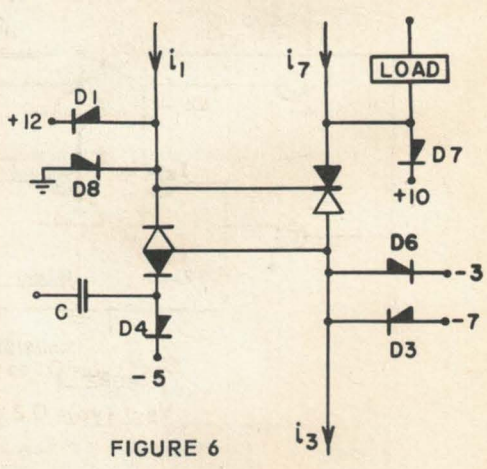
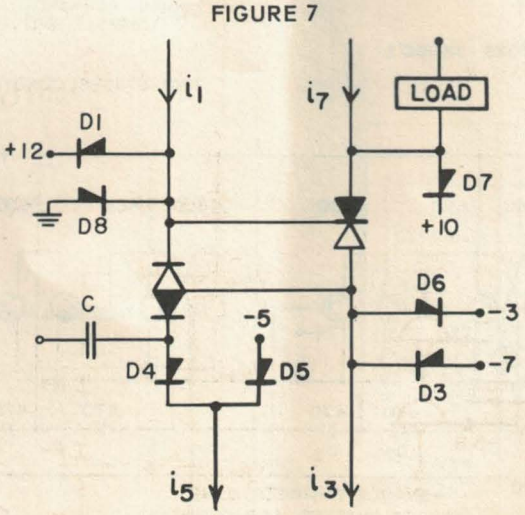
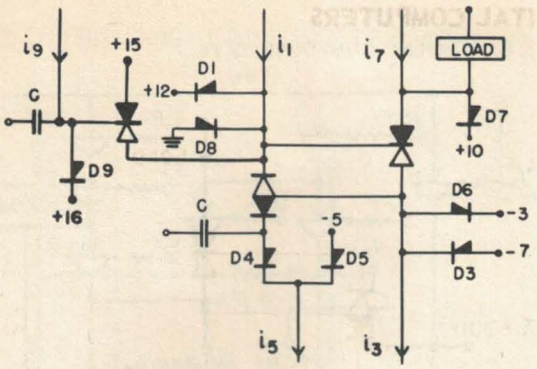
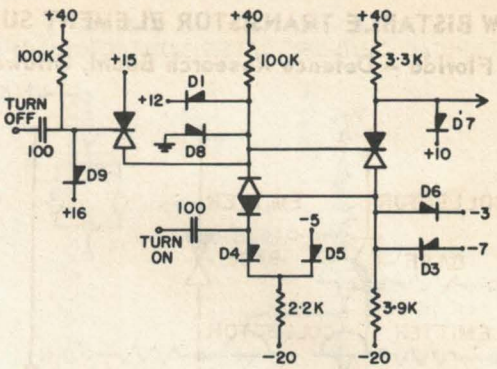


FIGURE 6

FIGURE 7







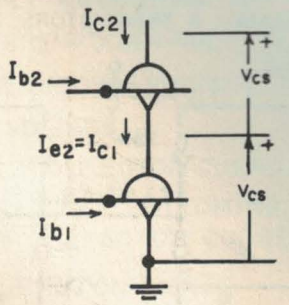
SPECIFICATION

SWITCHING TIME	< 0.2 μ sec.
OUTPUT FALL TIME WHEN DRIVING 5 SIMILAR STAGES	< 0.2 μ sec.
OUTPUT RISE TIME WHEN DRIVING 5 SIMILAR STAGES	< ½ μ sec.
OUTPUT LOAD CURRENT	> 30 mA
OUTPUT IMPEDANCE	< 20 Ω
RESOLVING TIME	< 1.5 μ sec.

2.6 THE DESIGN OF DUAL-RANGE TRANSISTOR CIRCUITS FOR MINIMUM STANDBY-CURRENT SYSTEMS

Howard E. Tompkins – University of Pennsylvania

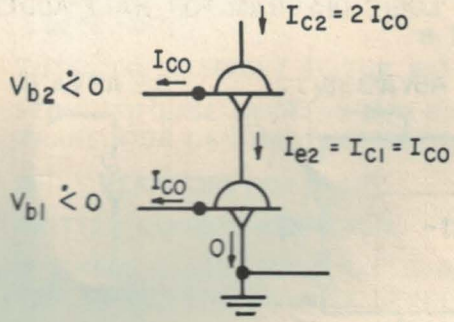
① "ON" TRANSISTORS (BOTTOMED)



V_{cs} (typ) = 0.1 to 0.15 V.

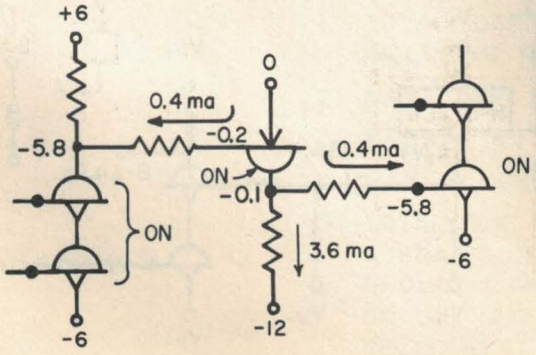
V_{BS} (typ) = 0.2 V.

② "OFF" TRANSISTORS

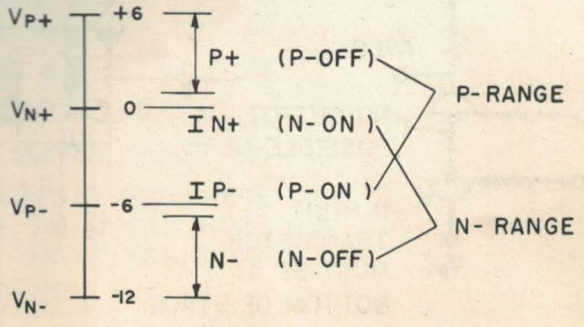


$I_{CO\,(typ)}$ = 50 μa

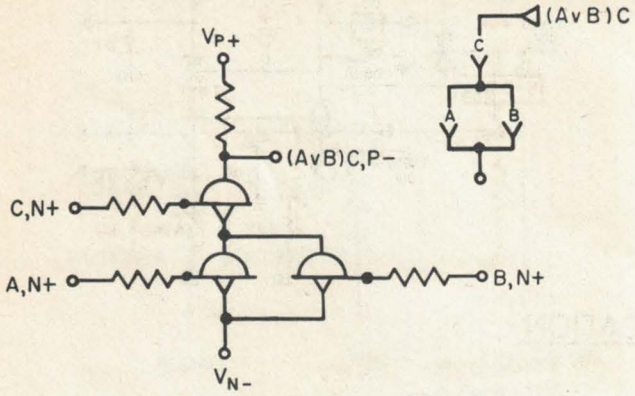
③ P AND N CASCADES



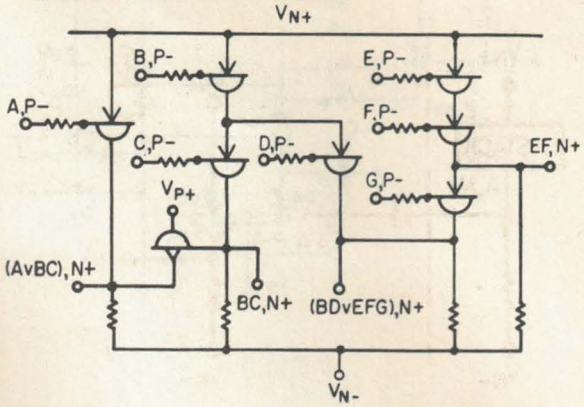
④ SUPPLY VOLTAGES AND SIGNAL RANGES



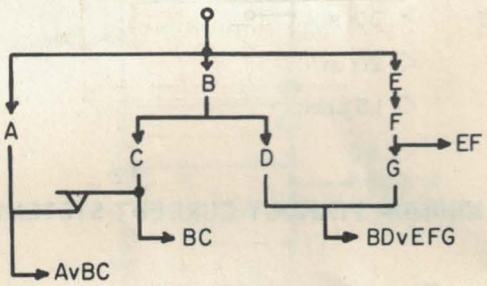
⑤ TYPICAL "AND-OR" GATES; CONTACT DIAGRAM



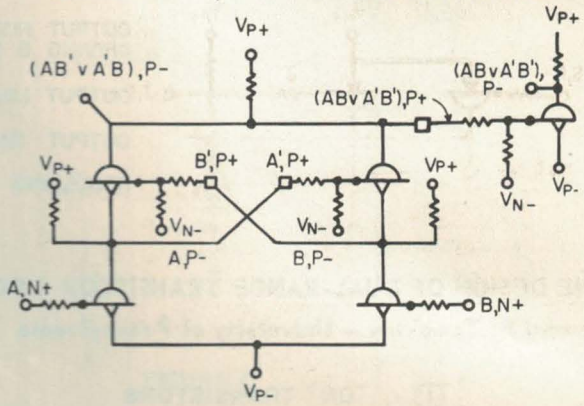
⑥ COMPLEX COMPOUND GATE



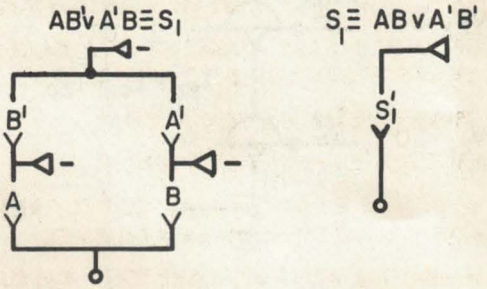
⑦ CONTACT LOGIC DIAGRAM FOR NETWORK OF SLIDE 6



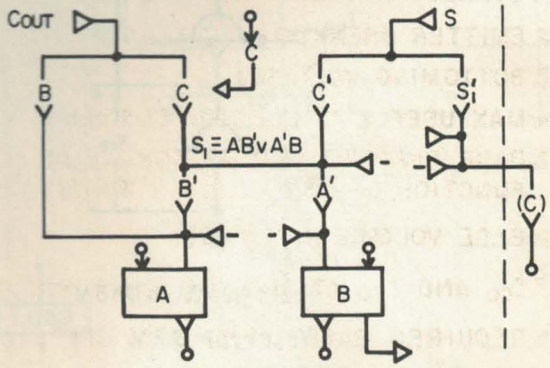
⑧ HALF-ADDER, SHOWING INHIBITION AND NEGATION



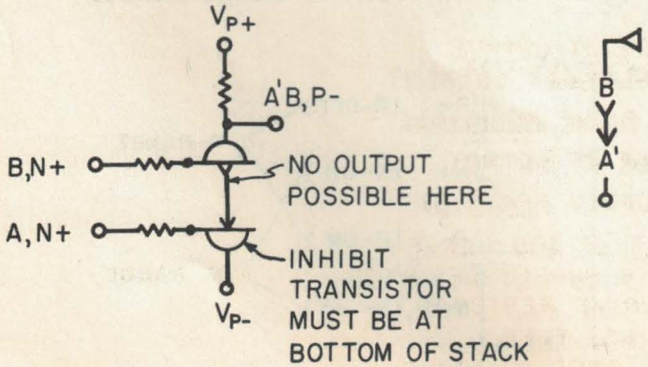
⑨ CONTACT LOGIC DIAGRAM FOR HALF-ADDER OF SLIDE 8



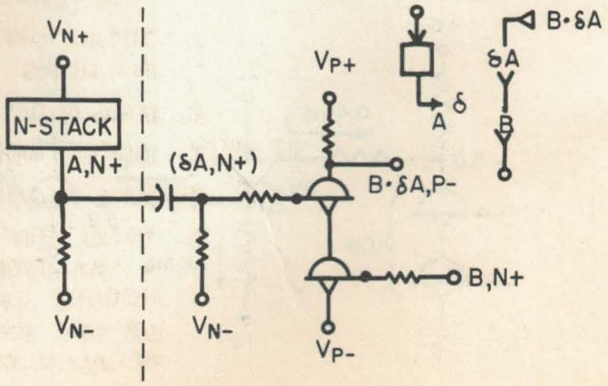
⑩ CONTACT DIAGRAM OF FULL ADDER WITH STORAGE, II TRANSISTORS PER STAGE



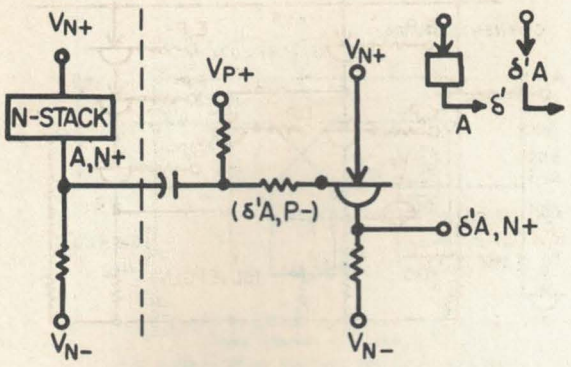
⑪ ALTERNATIVE INHIBIT CIRCUIT



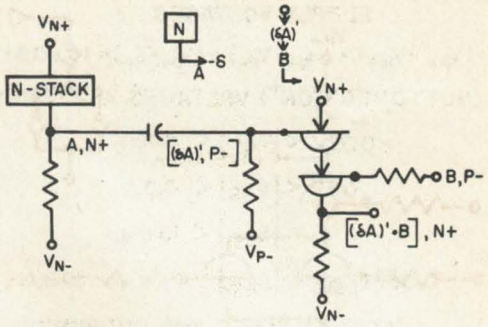
⑫ LEADING EDGE DIFFERENTIATION IN AN "AND" GATE



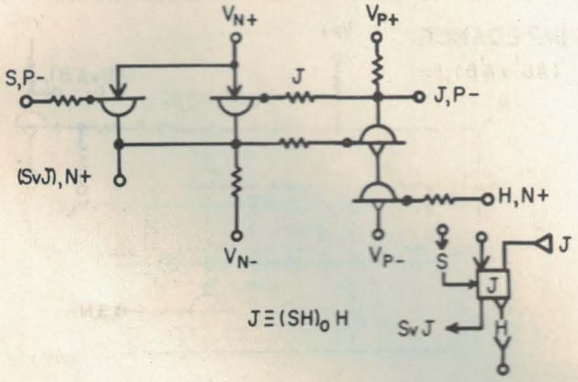
(13) TRAILING-EDGE DIFFERENTIATION



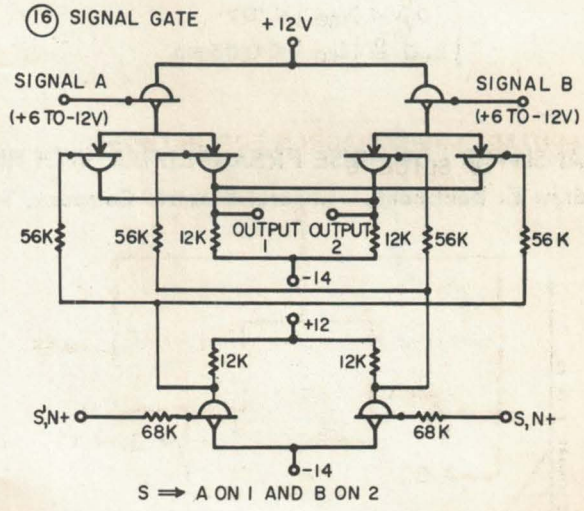
(14) LEADING-EDGE DIFFERENTIATION WITH NEGATION



(15) FLIP-FLOP WITH SET AND HOLD



(16) SIGNAL GATE



(17) FOR THE TRANSISTOR TYPES USED, NEED "WORST-CASE" KNOWLEDGE OF

1. COLLECTOR BREAKDOWN VOLTAGE
2. EMITTER BREAKDOWN VOLTAGE
3. BOTTOMING VOLTAGE
4. MAX. USEFUL COLLECTOR CURRENT
5. BASE CURRENT FOR BOTTOMING, AS FUNCTION OF COLLECTOR CURRENT
6. BASE VOLTAGE IN "ON" STATE
7. I_{CO} AND I_{BO} AT MAX. OP. TEMPERATURE
8. REQUIRED BASE VOLTAGE IN "OFF" STATE

(18) "ON" CALCULATION FOR A STACK; DETERMINE:

1. TOTAL "ON" CURRENT AT THE OUTPUT.
2. REQUIRED BASE CURRENT FOR EACH TRANSISTOR DRIVING THAT OUTPUT.
3. DRIVE RESISTORS FOR EACH.
4. EMITTER CURRENT FOR EACH.
5. IF SIMPLE STACK, TOTAL "ON" CURRENT FOR TRANSISTOR ON NEXT LEVEL.
6. IF PARTIAL OUTPUT, MAKE "OFF" CALCULATION, THEN RESUME "ON" CALCULATION, TO BOTTOM OF STACK.

(19) "OFF" CALCULATION FOR OUTPUT; DETERMINE:

1. TOTAL "OFF" CURRENT AT OUTPUT, INCLUDING INHIBIT BLEEDER CURRENT.
2. MAX. "OFF" DROP IN DRIVE RESISTORS.
3. WORST "OFF" VOLTAGE AT OUTPUT.
4. MAX. ALLOWABLE SUPPLY RESISTOR.
5. TOTAL "ON" CURRENT; IF TOO LARGE A FRACTION GOES TO SUPPLY RESISTOR, REDUCE LARGEST DRIVE RESISTOR, OR USE BASE LOADING, THEN RECALCULATE FROM STEP. 2, ABOVE.

(20) TYPICAL DESIGN ASSUMPTIONS (BOTH TYPES OF TRANSISTOR)

SUPPLY VOLTAGES

$(V_{P+} - V_{N+}) = (V_{N+} - V_{P-}) = (V_{P-} - V_{N-}) = (6 \pm 0.5)\,V$

BOTTOMED ("ON") VOLTAGES AND CURRENTS

$0.05\,V < |V_{CS}| < 0.15\,V$

$0.1\,V < |V_{BS}| < 0.3\,V$

$|I_{CS}| < 15\,ma.$

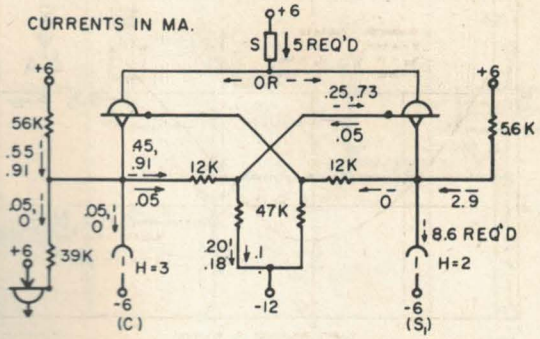
$0.05\,|I_{CS}| < |I_{BS}|$

"OFF" VOLTAGES AND CURRENTS

$0.1v < |V_{BO}| < 10V$

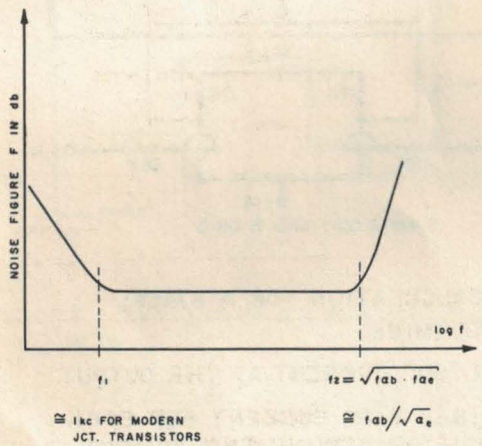
$|I_{BO}| \cong |I_{CO}| < 0.05\,ma.$

(21) CALCULATIONS ON THE ADDER CIRCUIT OF SLIDE 10



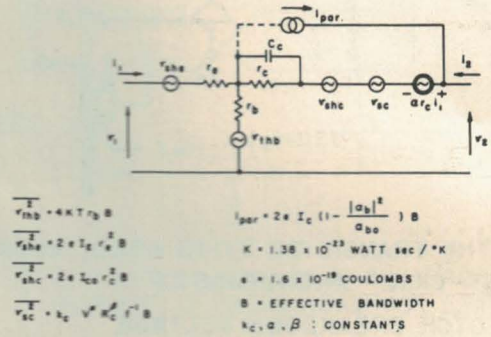
3.1 TRANSISTOR LOW NOISE PREAMPLIFIER WITH HIGH INPUT IMPEDANCE

Andrew E. Bachmann,– General Electric Company, Syracuse



TRANSISTOR NOISE VS. FREQUENCY

FIGURE 0



$\overline{i^2_{rthb}} = 4kT r_b B$

$\overline{i^2_{rshe}} = 2e I_E r_e^2 B$

$\overline{i^2_{rshc}} = 2e I_{CO} r_c^2 B$

$\overline{i^2_{sc}} = k_c\, V^{\alpha} K_c^{\beta} f^{-1} B$

$i_{par} = 2e\, I_c \left(1 - \frac{|a_b|^2}{a_{bo}}\right) B$

$K = 1.38 \times 10^{-23}$ WATT sec / °K

$e = 1.6 \times 10^{-19}$ COULOMBS

B = EFFECTIVE BANDWIDTH

k_c, α, β : CONSTANTS

EQUIVALENT TRANSISTOR CIRCUIT WITH NOISE

FIGURE 1

NOISE FIGURE : $F = \frac{(S/N)_i}{(S/N)_o} = \frac{N_o}{(S_o/S_i)\cdot N_i} = \frac{N_o}{G \cdot N_i}$

S_i = SIGNAL POWER AT THE INPUT AVAILABLE OUT OF THE SOURCE

N_i = NOISE POWER AT THE INPUT AVAILABLE OUT OF THE SOURCE

$N_i = kTB$

$k = 1.38 \times 10^{-23}$ WATT sec/°K

T = TEMPERATURE IN °K

$B = \frac{1}{A_o} \int_{-\infty}^{+\infty} A_f\, df$ = EFFECTIVE BANDWIDTH

S_o = AVAILABLE SIGNAL OUTPUT POWER

N_o = AVAILABLE TOTAL NOISE POWER OUT OF THE AMPLIFIER

$G = \frac{S_o}{S_i}$ = AVAILABLE POWER GAIN

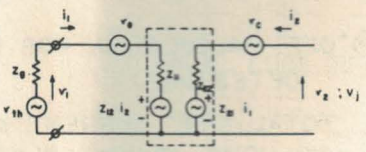
$N_o = F \cdot G \cdot kTB = G \cdot N_i + N_a$

N_a = AVAILABLE NOISE POWER DUE TO THE AMPLIFIER ALONE

FOR ADDITIONAL NOISE IN THE SOURCE : $N_{in} = n \cdot kTB$

$F_n = \frac{S_{in}/N_{in}}{S_{on}/N_{on}} = \frac{N_{on}}{G_n \cdot N_{in}} = 1 + \frac{F-1}{n}$

NOISE FIGURE



NOISY FOUR TERMINAL NETWORK

FIGURE 2

OPEN CIRCUIT OUTPUT VOLTAGES v_j :

$V_{th} = (4kTBR_g)^{\frac{1}{2}} Z_{21} / (Z_{11} + Z_g)$

$V_e = v_e\, Z_{21} / (Z_{11} + Z_g)$

$V_c = v_c$

MEAN SQUARE VALUE OF THE TOTAL OUTPUT VOLTAGE :

$\overline{v^2_{tot}} = V^*_{tot} \cdot V_{tot} = \overline{V^2_{th}} + \overline{V^2_e} + \overline{V^2_c} + 2r\left(\overline{V^2_e} \cdot \overline{V^2_c}\right)^{\frac{1}{2}}$

r = CORRELATION COEFFICIENT

NOISE FIGURE F :

$F = \frac{\overline{v^2_{tot}}}{\overline{V^2_{th}}} = 1 + \frac{\overline{V^2_e} + \overline{V^2_c} + 2r\sqrt{\overline{V^2_e} \cdot \overline{V^2_c}}}{\overline{V^2_{th}}}$

FOR LOW FREQUENCIES AND $r = 0$:

$F \cong 1 + \frac{1}{4kTBR_g}\left[\overline{V^2_e} + \overline{V^2_c}\left(\frac{R_{11} + R_g}{R_{21}}\right)^2\right]$

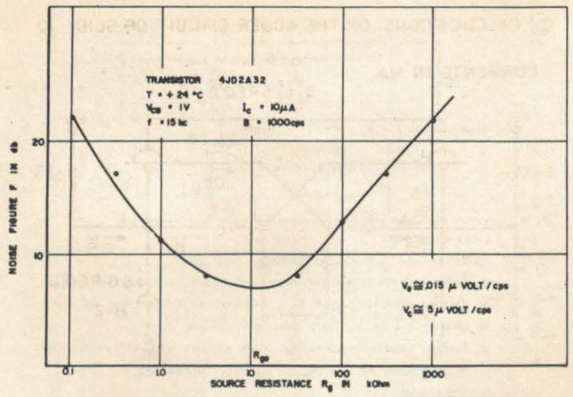
$= A + B/R_g + C\,R_g$

OPTIMAL SOURCE RESISTANCE :

$R_{go} = \left[R_{11}^2 + \left(\overline{V^2_e}/\overline{V^2_c}\right) R_{21}^2\right]^{\frac{1}{2}}$

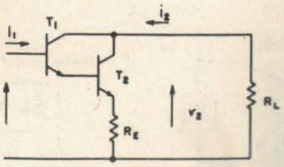
NOISE FIGURE OF GENERAL FOURTERMINAL NETWORK

FIGURE 3



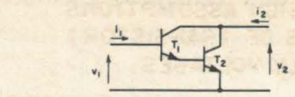
NOISE FIGURE VS. SOURCE RESISTANCE FOR COMMON BASE STAGE

FIGURE 4



DEGENERATIVE COMMON EMITTER DARLINGTON CONNECTION

FIGURE 6



$$h_{11_e} \cong h'_{11} + h''_{11}(1+h'_{21}) \qquad r_e \cong \frac{h''_{11}\, h''_{22}}{h''_{22} + h'_{22} h''_{21}}$$

$$h_{12_e} \cong h''_{11}\, h'_{22} \qquad r_b \cong h'_{11} + h''_{11}(1+h'_{21}) - r_e\,(1+h'_{21})\, h''_{21}$$

$$h_{21_e} \cong (1+h'_{21})(1+h''_{21}) \qquad r_c \cong \frac{(1+h'_{21})\, h''_{21}}{h''_{22} + h'_{22}\, h''_{21}}$$

$$h_{22_e} \cong h''_{22} + h'_{22}\, h''_{21} \qquad \alpha_e \cong (1+h'_{21})\, h''_{21}$$

h's : COMMON EMITTER VALUES

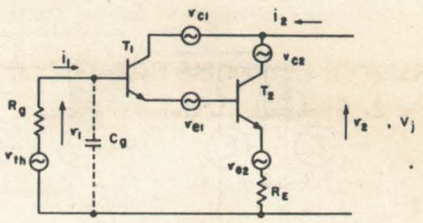
' FIRST TRANSISTOR T_1 ; " SECOND TRANSISTOR T_2

APPROXIMATIONS: $\Delta^{h'}$; $\Delta^{h''}$; h'_{12} ; h''_{12} ; $h''_{11}\, h'_{22} \ll 1$

$h''_{21} \gg 1$

DARLINGTON CONNECTION

FIGURE 5



DARLINGTON CONNECTION WITH NOISE

FIGURE 7

$$F = 1 + \frac{\overline{V_{e1}^2} + \overline{V_{e2}^2} + \overline{V_{c1}^2} + \overline{V_{c2}^2} + 2r\left(\sqrt{\overline{V_{c1}^2}\;\overline{V_{e1}^2}} + \sqrt{\overline{V_{c2}^2}\;\overline{V_{e2}^2}}\right)}{\overline{V_{th}^2}}$$

$$F = 1 + a + b + c + d + 2r\left(\sqrt{c \cdot a} + \sqrt{d \cdot b}\right)$$

$$a = \frac{\overline{V_{e1}^2}}{\overline{V_{th}^2}} \cong \frac{\overline{v_{e1}^2}}{4kTB}\left[\frac{(r_b + R_E)^2}{Rg^3} + \frac{2\,(r_b + R_E)}{Rg^2} + \frac{1}{Rg}\right]$$

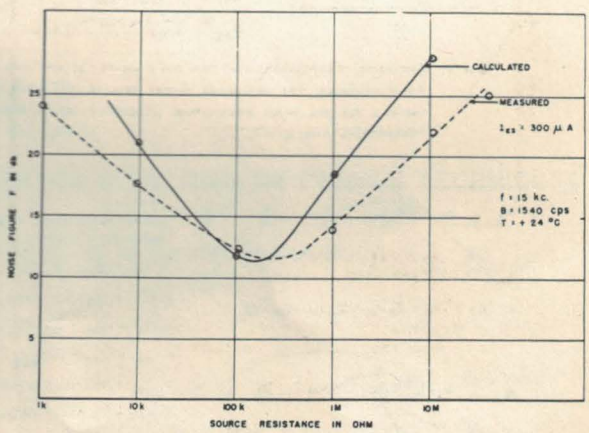
$$b = \frac{\overline{V_{e2}^2}}{\overline{V_{th}^2}} \cong \frac{\overline{v_{e2}^2}}{4kTB} \cdot \frac{1}{Rg}$$

$$c = \frac{\overline{V_{c1}^2}}{\overline{V_{th}^2}} \cong \frac{\overline{v_{c1}^2}}{4kTB}\,(2\pi fC_c)^2\left[\frac{(r_b + R_E)^2}{Rg} + 2\,(r_b + R_E) + Rg\right]$$

$$d = \frac{\overline{V_{c2}^2}}{\overline{V_{th}^2}} \cong 0$$

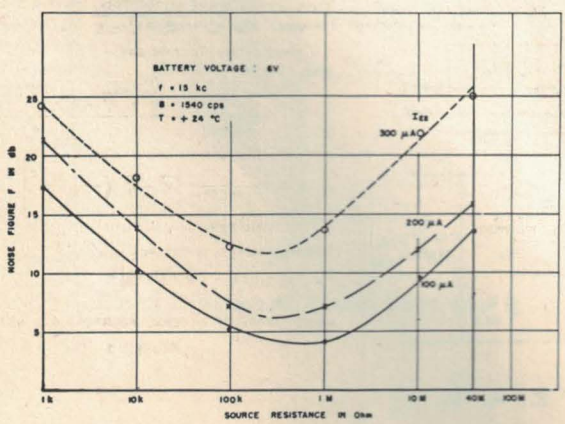
NOISE FIGURE OF THE DARLINGTON CONNECTION

FIGURE 8



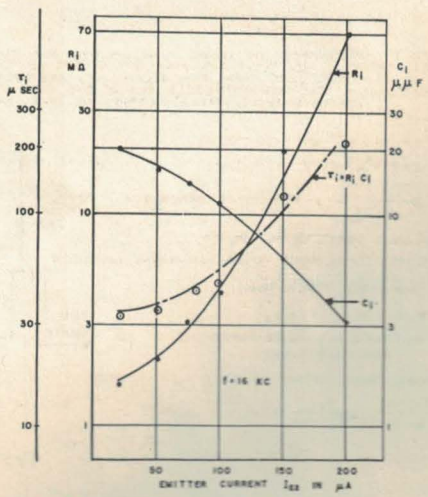
COMPARISON OF CALCULATED AND MEASURED NOISE FIGURE VS. SOURCE RESISTANCE

FIGURE 9



NOISE FIGURE VS. SOURCE RESISTANCE

FIGURE 10

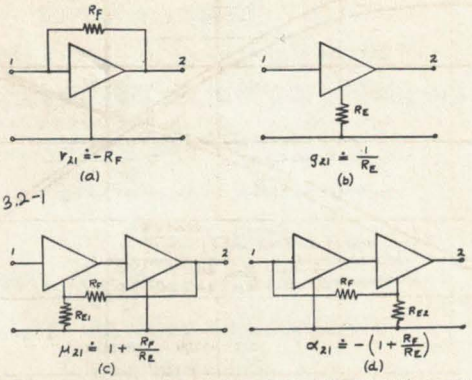


INPUT IMPEDANCE OF THE PREAMPLIFIER

FIGURE 11

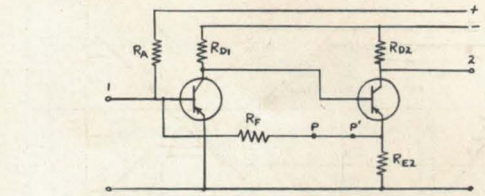
3.2 WIDE BAND FEEDBACK AMPLIFIERS

F. D. Waldhauer – Bell Telephone Laboratories, Murray Hill



3.2-1

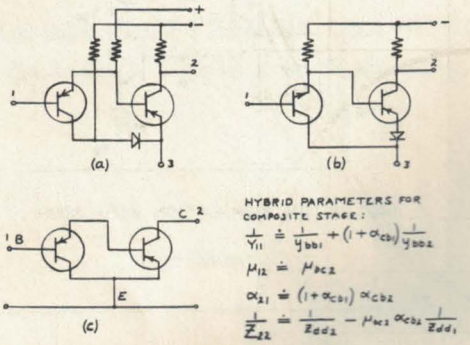
FIG. 1. FEEDBACK AMPLIFIER STRUCTURES FOR STABILIZING THE INDICATED TRANSFER FUNCTION. THE BLOCKS ALL REPRESENT PHASE REVERSING AMPLIFIERS OF HIGH GAIN.



DESIGN METHOD:

1. ESTABLISH OPERATING POINTS.
2. DETERMINE RELATION BETWEEN R_{E2} AND R_F FOR DESIRED α_{21}.
3. EXPRESS OPEN LOOP GAIN, $T_{p'p}$, IN TERMS OF EITHER R_{E2} OR R_F
4. CHOOSE R_{E2} OR R_F FOR MAXIMUM VALUE OF $T_{p'p}$.
5. CHECK RETURN DIFFERENCE FOR SECOND STAGE (APPROACHES A MAXIMUM OF $1+\alpha_{cb2}$ AS R_{E2} INCREASES).
6. MEASURE

FIG. 2. TWO-STAGE FEEDBACK AMPLIFIER SHOWING METHOD OF DESIGN WHEN HIGH-FREQUENCY STABILITY IS NOT OF PRIME CONCERN.



HYBRID PARAMETERS FOR COMPOSITE STAGE:

$$\frac{1}{Y_{11}} \doteq \frac{1}{y_{bb1}} + (1+\alpha_{cb})\frac{1}{y_{bb2}}$$

$$\mu_{12} \doteq \mu_{bc2}$$

$$\alpha_{21} \doteq (1+\alpha_{cb1})\alpha_{cb2}$$

$$\frac{1}{Z_{22}} \doteq \frac{1}{Z_{dd2}} - \mu_{e1}\alpha_{cb2}\frac{1}{Z_{dd1}}$$

FIG. 3. COMPOSITE TRANSISTORS: (a) TWO P-N-P UNITS, (b) NPN AND P-N-P COMBINED. THE AVALANCHE DIODES PROVIDE COLLECTOR VOLTAGE FOR THE INPUT TRANSISTOR. (c) CIRCUIT WHOSE HYBRID PARAMETERS ARE GIVEN.

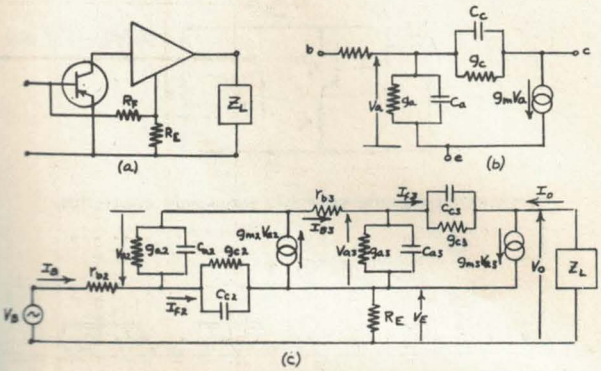
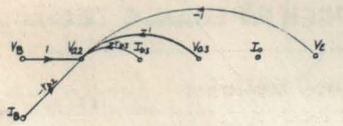
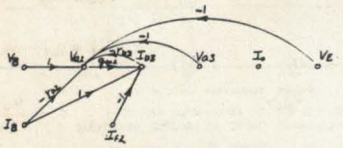


FIG 4. (a) BASIC AMPLIFIER STRUCTURE INCLUDING COMPOSITE STAGE. (b) TRANSISTOR EQUIVALENT CIRCUIT. (c) EQUIVALENT CIRCUIT OF COMPOSITE STAGE.



1. $V_{a2} = V_B - I_B r_{b2} - I_{b3} r_{b3} - V_{a3} - V_E$

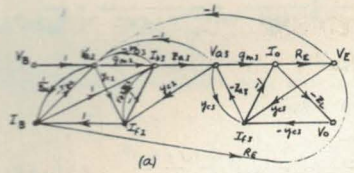


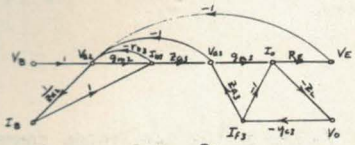
2. $I_{b3} = g_{m2}V_{a2} + I_B - I_{f2}$

ADDITIONAL EQUATIONS TO BE ADDED TO DIAGRAM:

3. $V_{a3} = (I_{b3} - I_{f3})Z_{a3}$
4. $I_o = g_{m3}V_{a3} - I_{f3}$
5. $V_E = (I_B + I_o)R_E$
6. $I_B = I_{f2} + V_{a2}\frac{1}{Z_{a2}}$
7. $I_{f2} = (V_{a2} + I_{b3}r_{b3} + V_{a3})y_{c2}$
8. $I_{f3} = (V_E + V_{a3} - V_o)y_{c3}$
9. $V_o = -I_o Z_L$

FIG 5. DEVELOPMENT OF SIGNAL FLOW DIAGRAM FOR COMPOSITE STAGE. (SEE MASON, PROC. IRE, SEPT 1953 AND MAY 1956; TRUXAL "CONTROL SYSTEM SYNTHESIS" McGRAW-HILL 1955, CHAP 2)

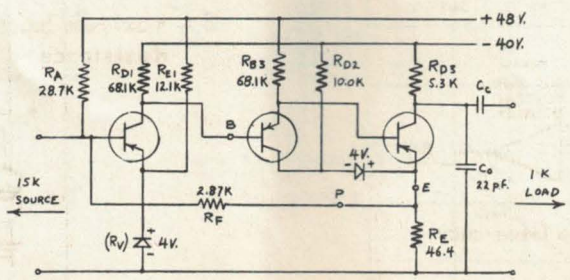




$$\mu_{EB} \doteq \frac{R_E}{R_E + \frac{r_{b2}+r_{c2}}{\alpha_{cb3}} + r_{e3} + Z_{L3}y_{c3}(r_{c3}+r_{b3}+r_{e3})} = \frac{A(s)}{B(s)}$$

$$Z_B \doteq \frac{(1+\alpha_{cb2})\alpha_{cb3}R_E}{1 - Z_L y_{c3}\alpha_{cb3}} = \frac{C(s)}{D(s)}$$

FIG 6 COMPLETE SIGNAL FLOW DIAGRAMS FOR COMPOSITE STAGE: IN (b), UNIMPORTANT BRANCHES ARE ELIMINATED.



$$T_{EP} = Y_{BP}\, Z_I\, \mu_{EB}\,, \text{ WHERE } \frac{1}{Z_I} = \frac{1}{Z_{01}} + \frac{1}{R_{D1}} + \frac{1}{Z_B}$$

FIG 7. AMPLIFIER INCORPORATING COMPOSITE STAGE

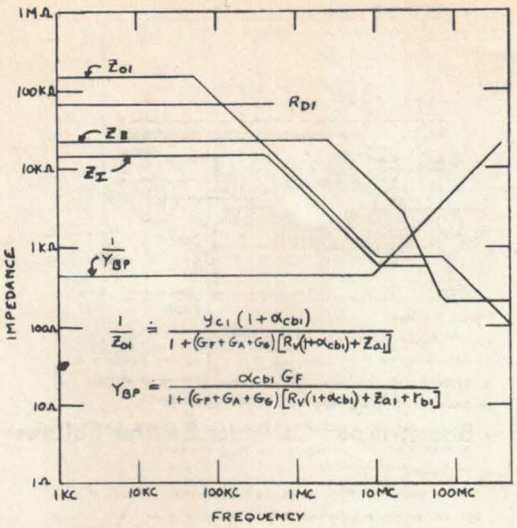


FIG. 8. GRAPHICAL METHOD OF DETERMINING RETURN RATIO

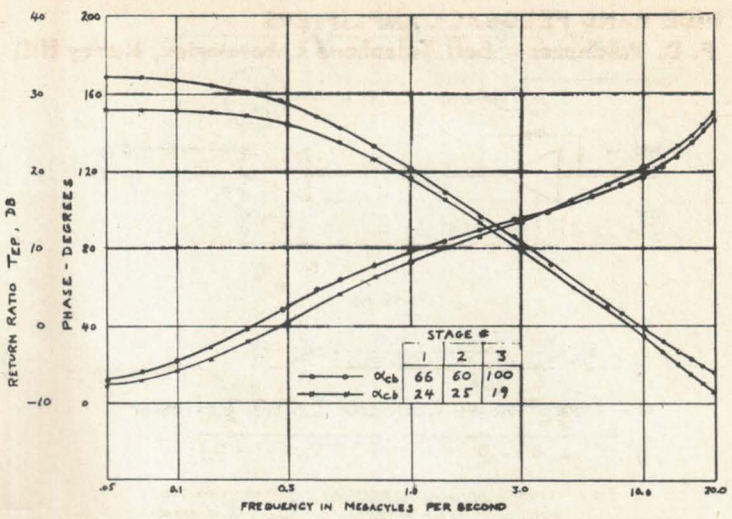


FIG 9. MEASURED OPEN LOOP RESPONSE OF AMPLIFIER OF FIG. 7 SHOWING EFFECT ON T_{EP} OF VARIATION IN α_{cb} OF TRANSISTORS.

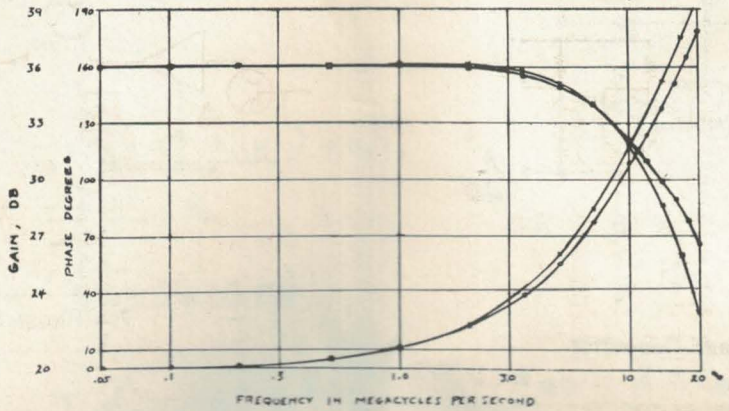
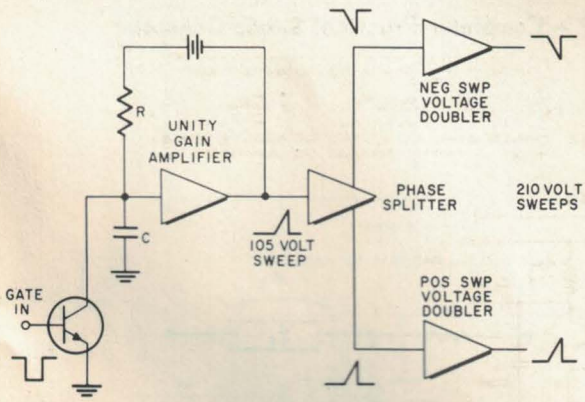


FIG 10. CLOSED LOOP GAIN AND PHASE CHARACTERISTIC

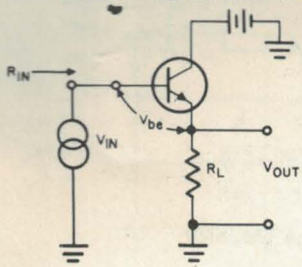
3.3 A TRANSISTORIZED HIGH VOLTAGE PUSH-PULL SWEEP GENERATOR USING HIGH IMPEDANCE TECHNIQUES

P. J. Anzalone – Radio Corp. of America, Camden



1 – Block Diagram of Sweep Generator

2 – Gain of an Emitter Follower



LET $g_m = \frac{i_e}{V_{be}}$

$V_{OUT} = i_e \times R_L$

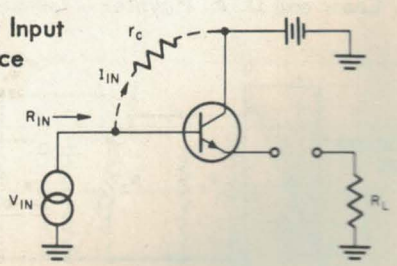
$V_{be} = V_{IN} - V_{OUT}$

$G = \frac{V_{OUT}}{V_{IN}}$

FOR R_L = 20K
AND g_m = 0.05 mhos
G = 0.999

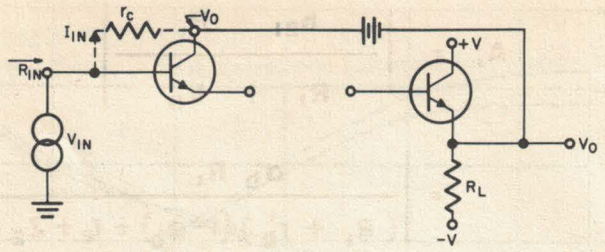
$G = \frac{1}{\frac{1}{g_m R_L}+1}$

3 – Maximum Input Resistance



$R_{IN} = \frac{V_{IN}}{I_{IN}} = \frac{V_{IN}}{V_{IN}/r_c} = r_c$

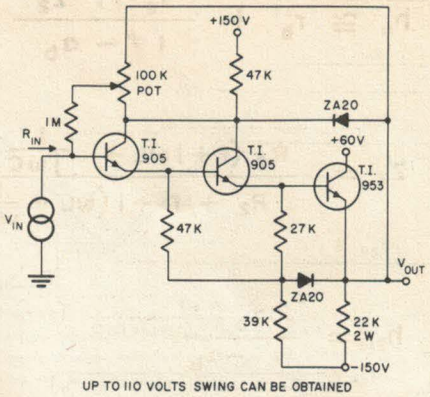
$R_{IN} = \frac{1}{\frac{1}{r_c} + \frac{1}{\beta R_L}}$ (PG. 109, "TRANSISTOR ELECTRONICS")



$$V_O = G\,V_{IN}$$

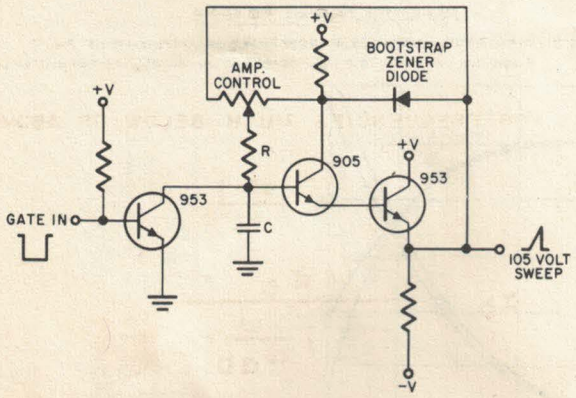
$$R_{IN} = \frac{V_{IN}}{I_{IN}} = \frac{V_{IN}}{\frac{V_{IN}-V_O}{r_c}} = \frac{V_{IN}\,r_c}{V_{IN}-G\,V_{IN}} = \frac{1}{1-G}\,r_c$$

4 – Bootstrapped Collector Emitter Follower

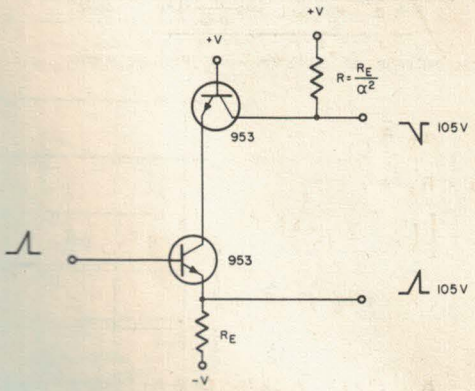


UP TO 110 VOLTS SWING CAN BE OBTAINED

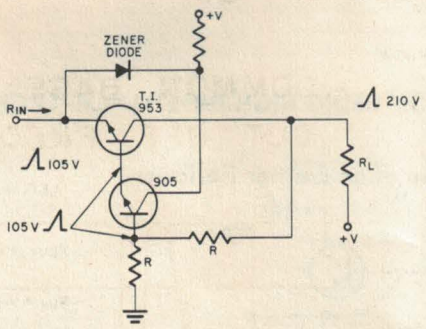
5 – Bootstrapped Collector Emitter Follower



6 – Bottstrap Sweep Generator



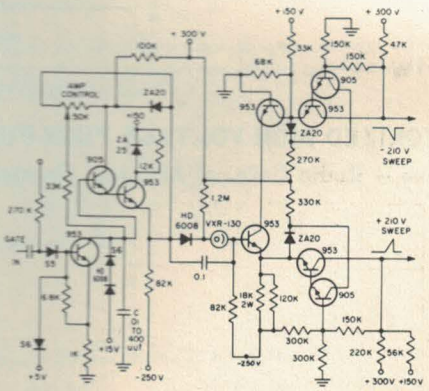
7 – Phase Splitter



$$I_{IN} = \frac{I_{OUT}}{\alpha} = \frac{V_{OUT}}{R_L\alpha} = \frac{2V_{IN}}{R_L\alpha}$$

$$R_{IN} = \frac{V_{IN}}{I_{IN}} = \frac{V_{IN}}{2V_{IN}}R_L\alpha = \frac{R_L\alpha}{2}$$

8 – Voltage Doubler



9 – Completer Practical Sweep Generator

3.4 SERIES TUNED METHODS IN TRANSISTOR RADIO CIRCUITRY

W. F. Chow and D. A. Paynter – General Electric Company, Syracuse

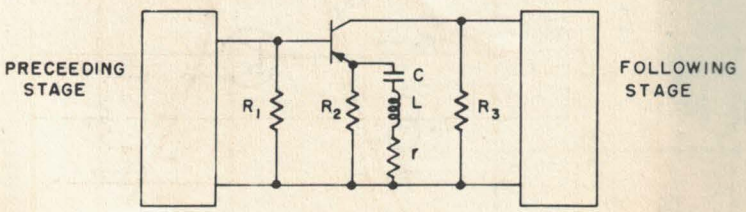


FIGURE 1

EMITTER DEGENERATIVE AMPLIFIER

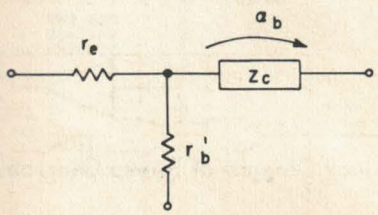


FIGURE 2

AN APPROXIMATE T EQUIVALENT CIRCUIT

$$h_{11} \cong r_b' + \frac{r_e + Z_2}{1 - \alpha_b}$$

$$Z_2 = \frac{R_2\left(r + j\omega L + \frac{1}{j\omega C}\right)}{R_2 + r + j\left(\omega L - \frac{1}{\omega C}\right)}$$

3 $$h_{21e} = \frac{\alpha_b}{1 - \alpha_b}$$

$$A_i = k\sqrt{\frac{a^2 + \left(\omega L - \frac{1}{\omega C}\right)^2}{b^2 + e^2\left(\omega L - \frac{1}{\omega C}\right)^2}}$$

$$k = \alpha_0 R_1$$

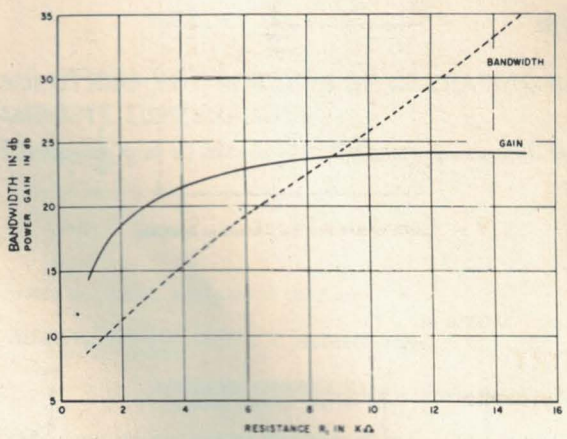
$$a = R_2 + r$$

$$b = \left[\left(R_1 + r_b'\right)\left(1 - \alpha_0\right) + r_e\right]\left(R_2 + r\right) + R_2 r$$

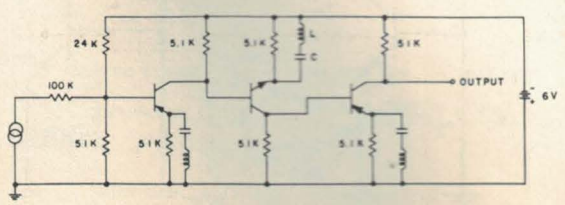
5 $$e = \left(R_1 + r_b'\right)\left(1 - \alpha_0\right) + r_e + R_2$$

THE ANGULAR BANDWIDTH

7 $$Bw \cong \omega_0^2\, C\sqrt{\frac{a^2 b^2}{a^2 e^2 - 2b^2}}$$



9 THE EFFECT OF R_1 ON GAIN AND BANDWIDTH



10 THREE STAGE DIRECT - COUPLED I F AMPLIFIER

$$A_i = \left|\frac{h_{21}\ R_1}{R_1 + h_{11}}\right|$$

$$= \left|\frac{\alpha_b R_1}{\left(R_1 + r_b'\right)\left(1 - \alpha_b\right) + r_e + Z_2}\right|$$

4 $$G = (A_i)^2$$

AT THE RESONANT FREQUENCY $\omega_0^2 LC = 1$

$$A_i \cong \frac{\alpha_b}{1 - \alpha_b}$$

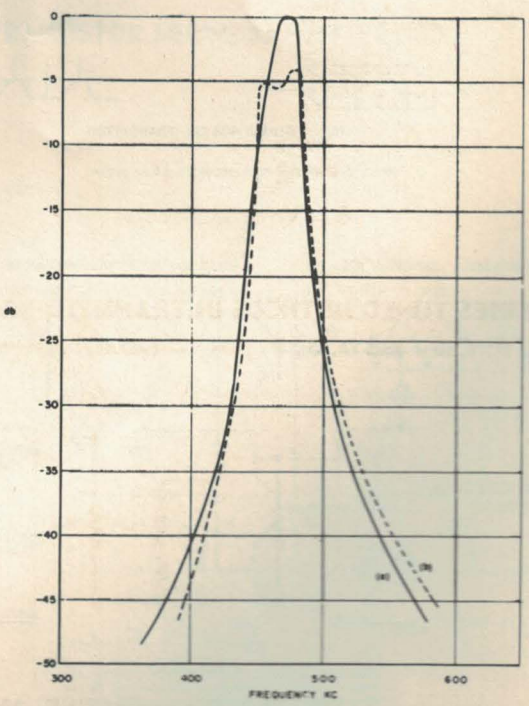
FOR FREQUENCIES MUCH BELOW OR ABOVE ω_0

6 $$A_i \cong \frac{\alpha R_1}{R_2}$$

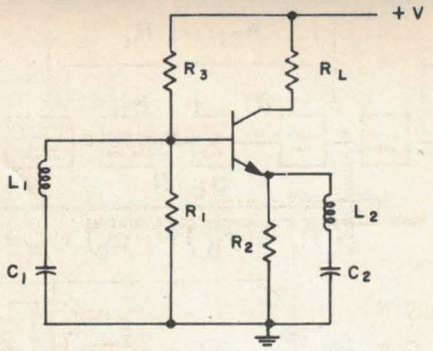
$$\alpha_b = \frac{\alpha_0}{1 + j\frac{\omega}{\omega_{\alpha b}}}$$

$$W_{\alpha b} = 2\pi f_{\alpha b}$$

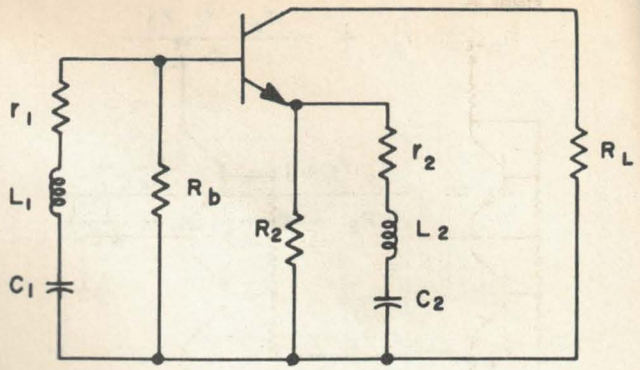
8 $f_{\alpha b}$ = COMMON BASE ALPHA CUT OFF FREQUENCY



11 THE BANDPASS CHARACTERISTIC OF A 3 STAGE DIRECT COUPLED AMPLIFIER



SERIES TUNED EMITTER - TUNED BASE OSCILLATOR
FIGURE 12



AC CIRCUIT OF THE OSCILLATOR
FIGURE 13

$$\frac{\omega_a}{\omega}\left(\frac{1}{\omega C_2}\right) \geq \left[r_1 + \omega_a L_2 + \left(r_b' + r_e + r_2\right)\left(1 + \frac{\omega}{\omega_a}\right)\right]$$

3.-1.,4

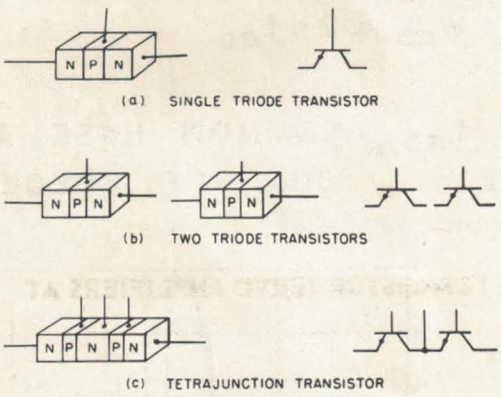
$$\omega = \frac{1}{\sqrt{\left(L_1 + L_2\right)\left(\frac{C_1 C_2}{C_1 + C_2}\right)}}$$

FIGURE 14

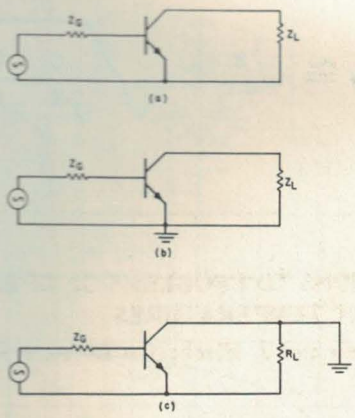
3.5 A NEW APPROACH TO TRANSISTOR RECEIVER DESIGN

A. Proudfit, K. M. St. John, C. R. Wilhelmsen, and R. J. Farber – Hazeltine Research Corp., Little Neck

FIGURE #1

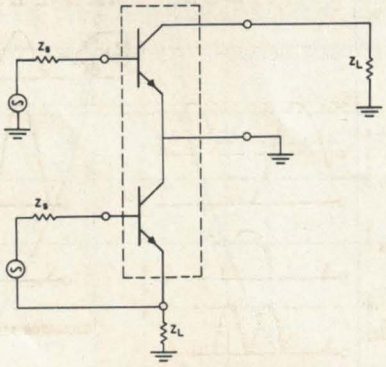


EVOLUTION OF THE TETRAJUNCTION TRANSISTOR



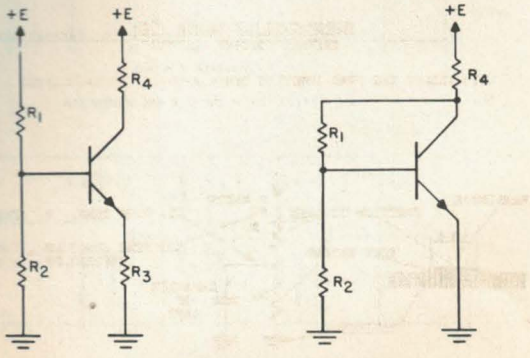
COMMON EMITTER OPERATION - FREEDOM OF GROUNDING

FIGURE #3



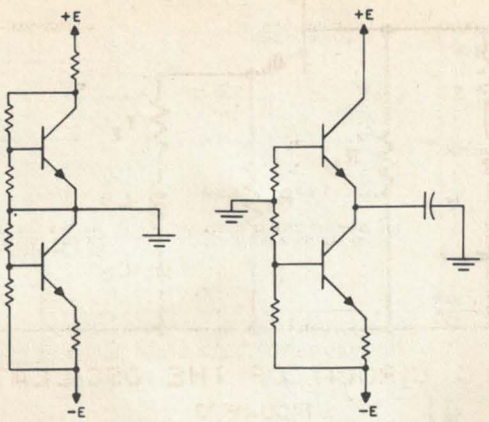
EQUIVALENT CIRCUIT SHOWING METHOD OF OBTAINING COMMON EMITTER OPERATION IN BOTH TRIODES OF THE TETRAJUNCTION TRANSISTOR

FIGURE #4



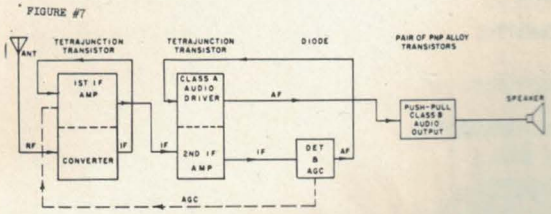
TYPICAL TRANSISTOR BIASING TECHNIQUES

FIGURE #5



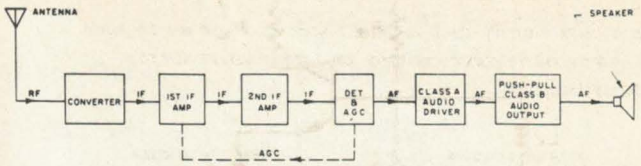
BIASING TECHNIQUES FOR TETRAJUNCTION TRANSISTORS

FIGURE #7



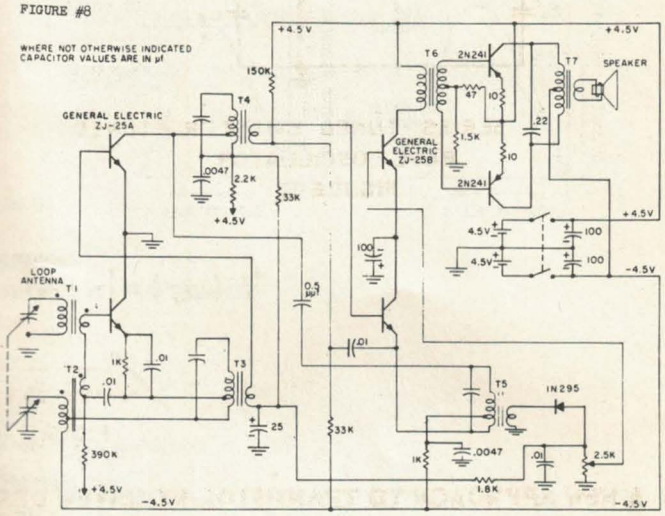
BLOCK DIAGRAM OF BROADCAST RECEIVER USING TETRAJUNCTION TRANSISTORS

FIGURE #6



BLOCK DIAGRAM OF TYPICAL TRANSISTOR RECEIVER

FIGURE #8



RECEIVER SCHEMATIC

TABLE I

For 50 mw Output		
Sensitivity - µv/m		350 - 500
	- db below 1 V/m	66 - 69
ENSI	- µv/m	15 - 20
	- db below 1 V/m	94 - 97
1.0 Mc 6 db Bandwidth - kc		6.0
AGC Figure of Merit - db		32
Total Battery Drain - ma		23

RECEIVER CHARACTERISTICS

4.1 SOME SOLUTIONS TO PROBLEMS OF OPERATING GERMANIUM TRANSISTOR SERVO AMPLIFIERS AT HIGH AMBIENT TEMPERATURES

P. M. Thompson and J. Mitchell – Defence Research Board, Ottawa

PLATE 1

THERE IS A THERMAL EQUIVALENT OF OHM'S LAW

$$\frac{\text{POTENTIAL DIFFERENCE (VOLTS)}}{\text{CURRENT (AMPERES)}} = \text{RESISTANCE (OHMS)}$$

$$\frac{\text{TEMPERATURE DIFFERENCE (°C)}}{\text{THERMAL CURRENT (WATTS)}} = \text{THERMAL RESISTANCE}$$

THIS ALLOWS THE PEAK JUNCTION TEMPERATURE TO BE CALCULATED.

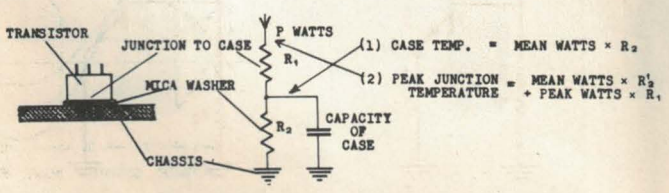
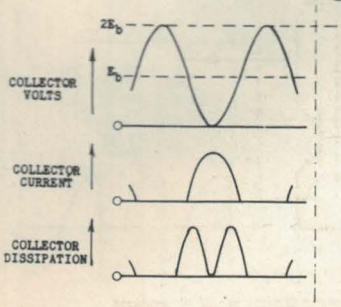
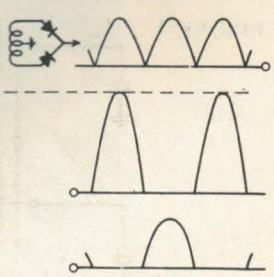


PLATE 2

AT MAXIMUM OUTPUT THE COLLECTOR WAVEFORMS OF A CLASS B AMPLIFIER ARE



BUT IF A RECTIFIED, UNSMOOTHED, A.C. SUPPLY IS USED



COLLECTOR DISSIPATION = 0.

PLATE 3

FOR A CLASS B OUTPUT STAGE TO DRIVE A STANDARD 3 WATT 400 C/S MOTOR WE COMPUTE THE FOLLOWING CURVES OF COLLECTOR POWER DISSIPATION AGAINST AMPLITUDE.

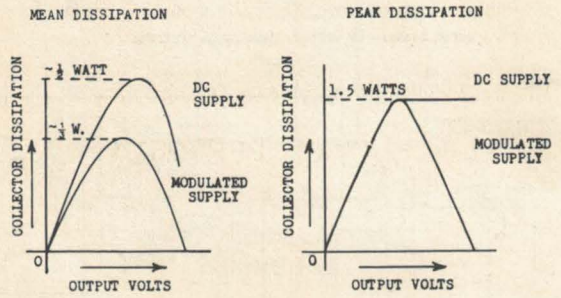


PLATE 4 CIRCUIT DEVELOPMENT

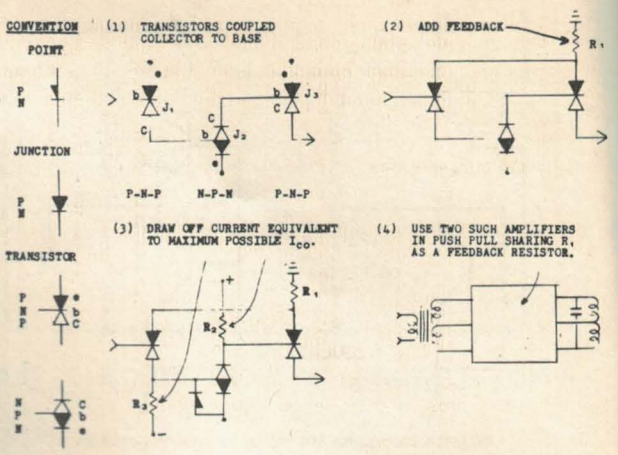
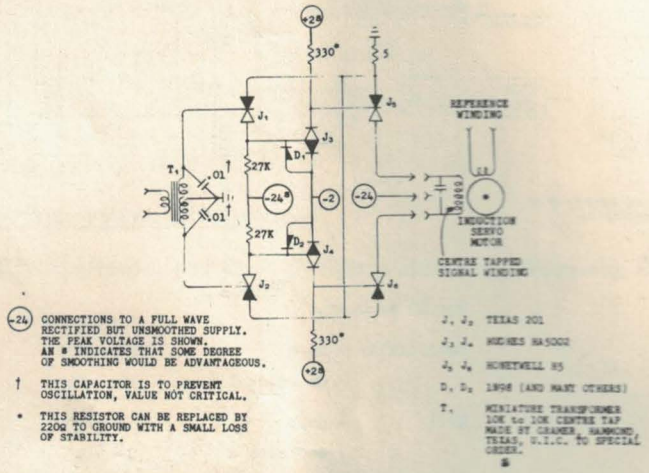


PLATE 5. COMPLETE SERVO AMPLIFIER CIRCUIT



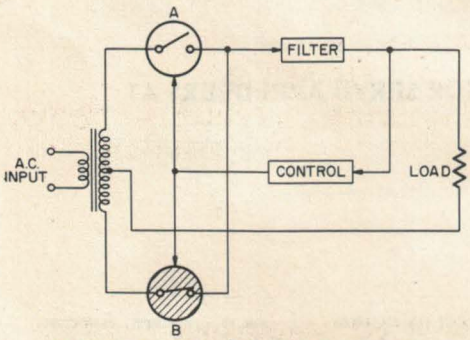
(-24) CONNECTIONS TO A FULL WAVE RECTIFIED BUT UNSMOOTHED SUPPLY. THE PEAK VOLTAGE IS SHOWN. AN * INDICATES THAT SOME DEGREE OF SMOOTHING WOULD BE ADVANTAGEOUS.

† THIS CAPACITOR IS TO PREVENT OSCILLATION, VALUE NOT CRITICAL.

* THIS RESISTOR CAN BE REPLACED BY 220Ω TO GROUND WITH A SMALL LOSS OF STABILITY.

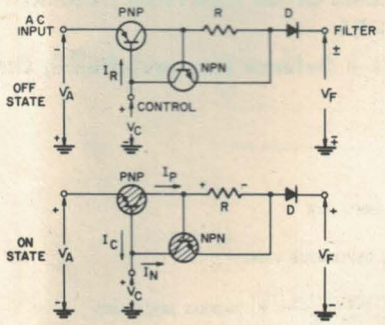
4.2 PHASE CONTROLLED TRANSISTOR POWER SUPPLY REGULATION

D. E. Deuitch and H. J. Paz – Radio Corp. of America, Camden



PHASE REGULATED POWER SUPPLY

FIGURE 1



TRANSISTOR SWITCH CIRCUIT

FIGURE 3

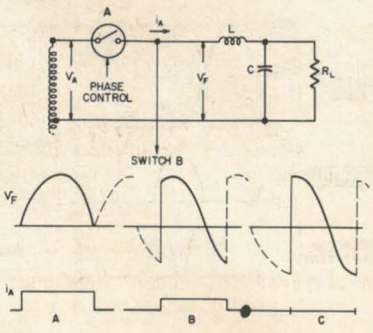
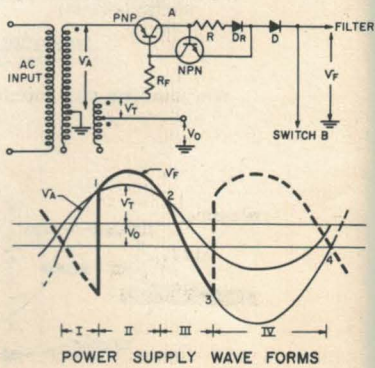
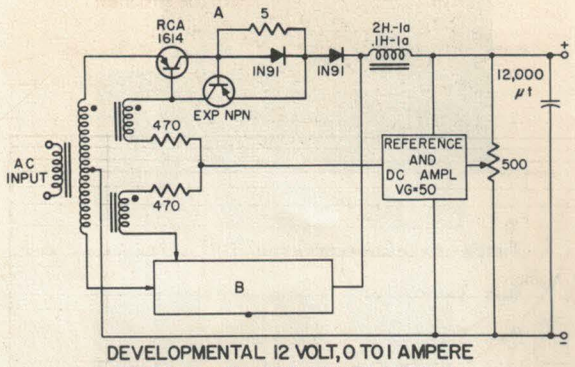


FIGURE 2 PHASE CONTROL ACTION



POWER SUPPLY WAVE FORMS

FIGURE 4



DEVELOPMENTAL 12 VOLT, 0 TO 1 AMPERE PHASE REGULATED POWER SUPPLY

FIGURE 5

REGULATION	4% 0 TO 1 AMP LOAD CURRENT 1% 85 TO 145 VOLTS INPUT VOLTAGE
PHASE CONTROL	5° TO 80°
RIPPLE VOLTAGE	16 MV 1 AMP LOAD
REGULATOR TRANSISTOR	250 MW AVG DISSIPATION
OVERALL EFFICIENCY	78° 1 AMP LOAD

POWER SUPPLY PERFORMANCE

FIGURE 6

ADVANTAGES

LOW REGULATION DISSIPATION
HIGH EFFICIENCY
GREATER POWER CAPACITY
IMPROVED HIGH TEMPERATURE PERFORMANCE

DISADVANTAGES

COMPLEXITY?
LARGE FILTER ELEMENTS
DIFFICULTY IN OBTAINING VERY HIGH REGULATION

FIGURE 8 SUMMARY

4.5 A NEW TRAMAG OSCILLATOR

A. J. Meyerhoff and R. M. Tillman – Burroughs Research Center, Paoli

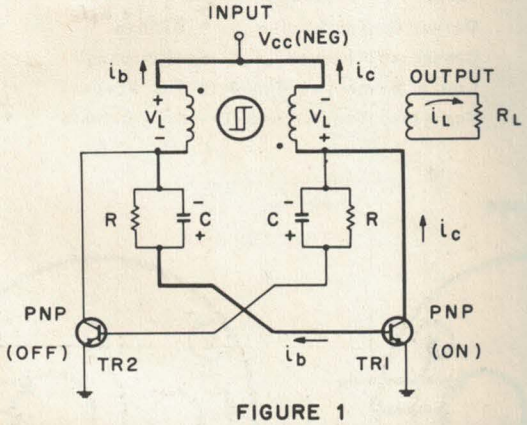
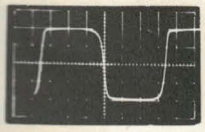


FIGURE 1
TWO-WINDING TRAMAG (TRANSISTOR-CORE) OSCILLATOR



VERT. SCALE: 1V/square

HORIZ. SCALE: 0.2 μs/square

FIGURE 2
TRAMAG OSCILLATOR OUTPUT – 700KC

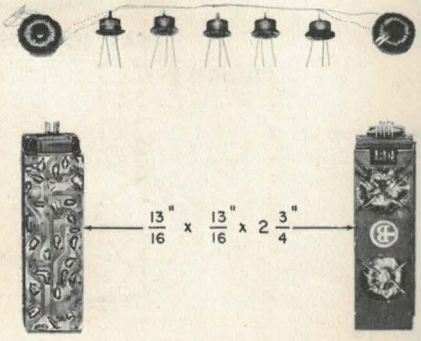


FIGURE 3
TRAMAG TELEMETERING SUB-CARRIER OSCILLATOR

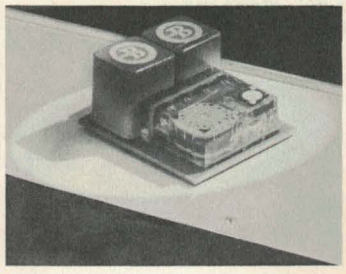


FIGURE 4
TRAMAG TELEMETERING SUB-CARRIER DISCRIMINATOR, 400 cps
SIZE -- 3-1/2" X 5" X 2"

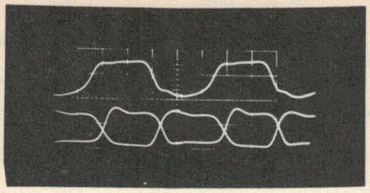


FIG. 6

THREE WAY COMPLEMENTED "OR" CIRCUIT
TWO INPUTS ARE LOGICAL ZEROS
THIRD INPUT IS THE TOP WAVEFORM
LOWER WAVEFORMS ARE OUTPUTS
HOR. 20 MμSEC/CM VERT. 1 VOLT/CM

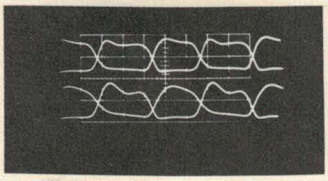


FIG. 8

OUTPUTS OF A TEN WAY COMPLEMENTED "OR" CIRCUIT (LOWER WAVEFORMS) COMPARED WITH THE OUTPUTS OF A THREE WAY COMPLIMENTED "OR" CIRCUIT (UPPER WAVEFORMS). WHEN DRIVEN BY THE SAME INPUT SIGNAL.
HOR. 20 MμSEC/CM VERT. 1 VOLT/CM

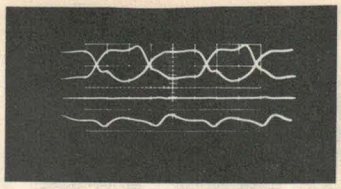


FIG. 7

THREE WAY COMPLEMENTED "OR" CIRCUIT
ONE INPUT IS A LOGICAL ZERO
TWO INPUTS ARE COMPLIMENTARY (TOP WAVEFORMS) "AND" OUTPUT (CENTER WAVEFORM) "OR" OUTPUT (LOWER WAVEFORM)
HOR. 20 MμSEC/CM VERT. 1 VOLT/CM

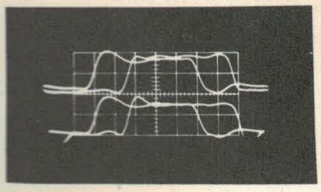


FIG. 10

INPUT AND OUTPUT WAVEFORMS OF FOUR SEQUENTIAL THREE WAY COMPLEMENTED "OR" CIRCUITS WITH A CASCADING FACTOR OF THREE. TOP WAVEFORMS ARE INPUT AND OUTPUT OF THE SYSTEM WITH BLOCKS CONNECTED THROUGH INVERTED OUTPUTS. LOWER WAVEFORMS ARE WITH THE BLOCKS CONNECTED THROUGH NON-INVERTED OUTPUTS.

5.1 TEMPERATURE COMPENSATION OF TRANSFLUXORS

H. W. Abbott and J. J. Suran – General Electric Company, Syracuse

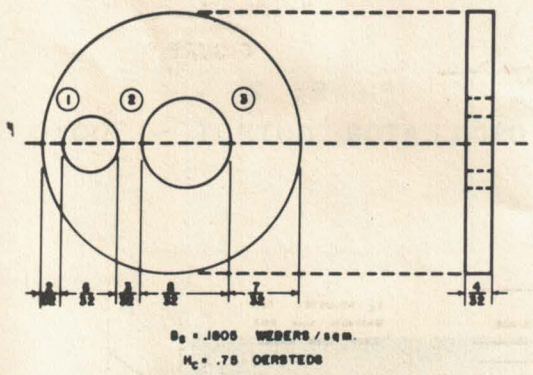


FIGURE 1

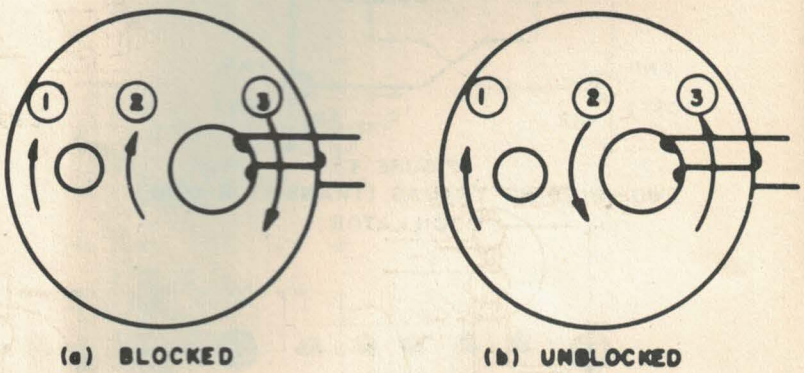


FIGURE 2

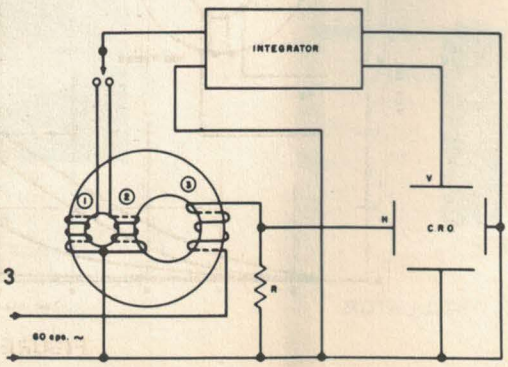


FIGURE 3

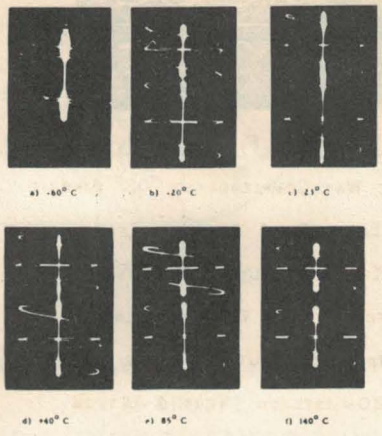


Figure 5 - ϕ - NI Characteristics. Top curve legs 3-1, Bottom curve legs 3-2.

FIGURE 4

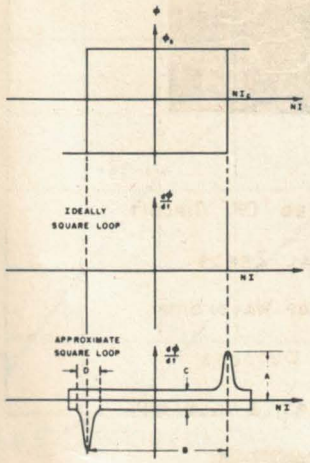


FIGURE 5

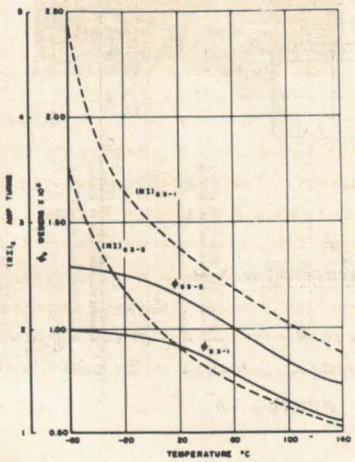


FIGURE 6

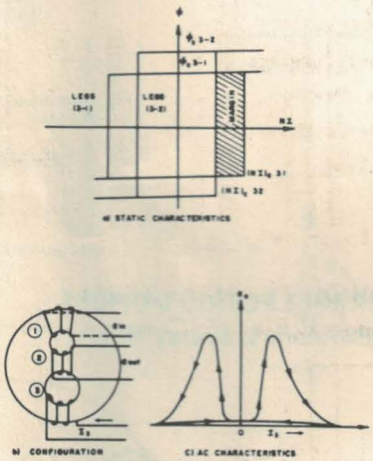


FIGURE 7

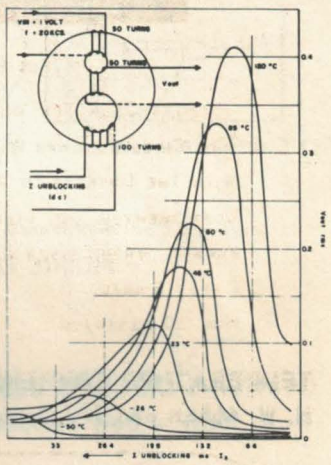


FIGURE 8

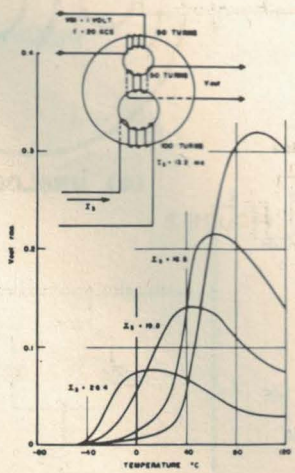


FIGURE 9

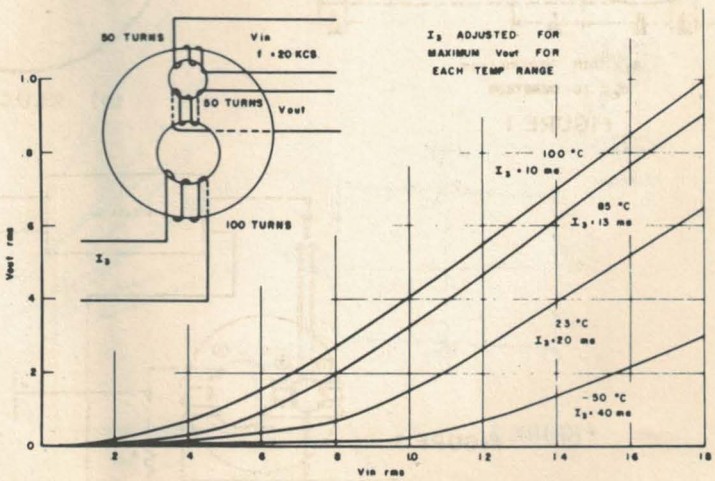


FIGURE 10

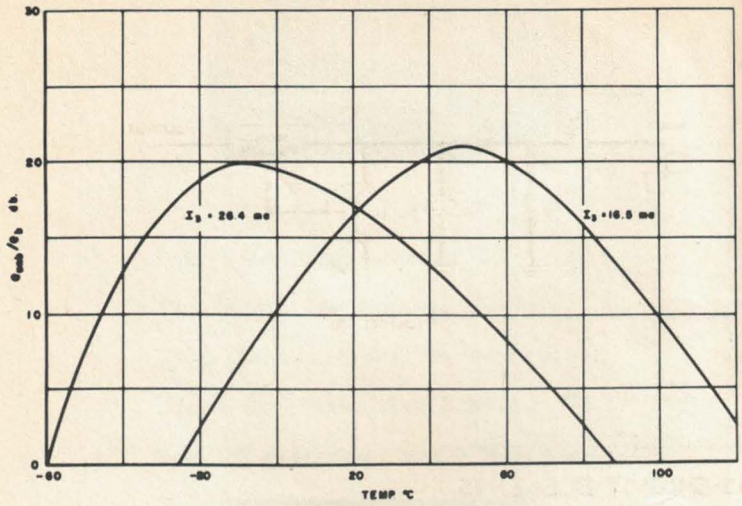
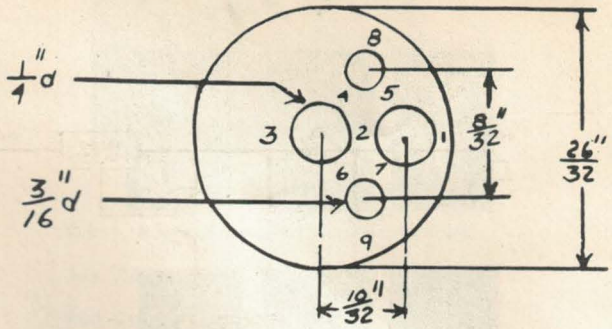
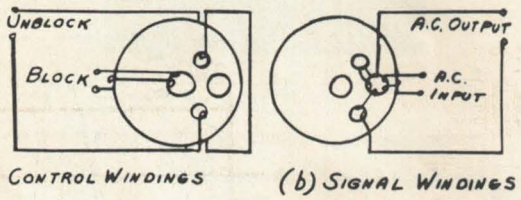


FIGURE 11



EXPERIMENTAL FOUR-HOLE TRANSFLUXOR

FIGURE 12



WINDING CONFIGURATIONS.

FIGURE 13

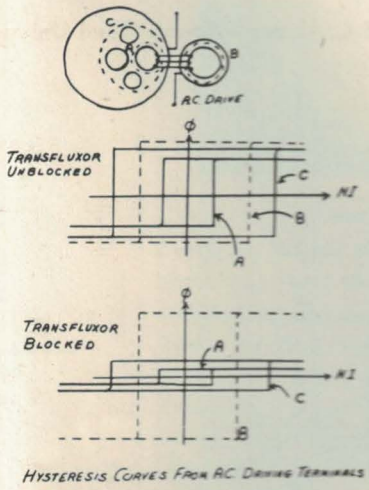


FIGURE 14

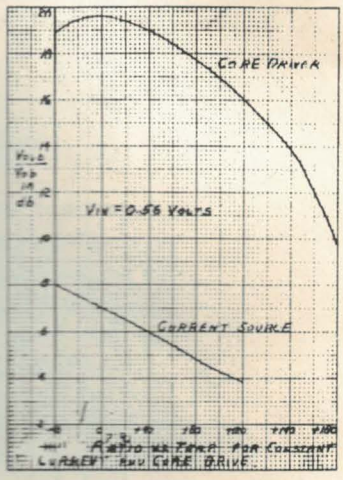


FIGURE 15

5.2 COUNTING CIRCUITS USING FERROELECTRIC DEVICES

R. M. Wolfe – Bell Telephone Laboratories, Murray Hill

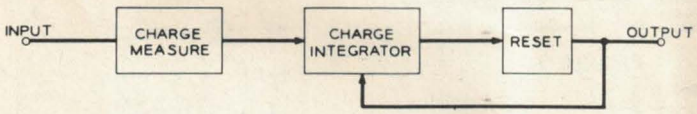


FIGURE 1

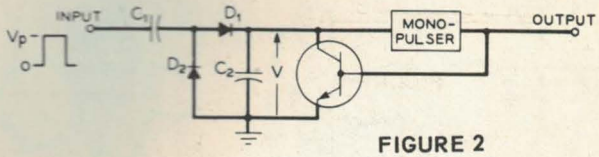


FIGURE 2

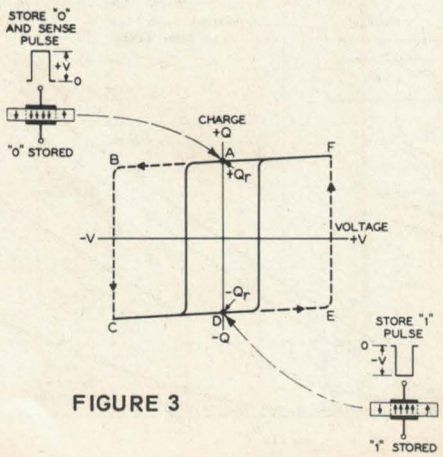


FIGURE 3

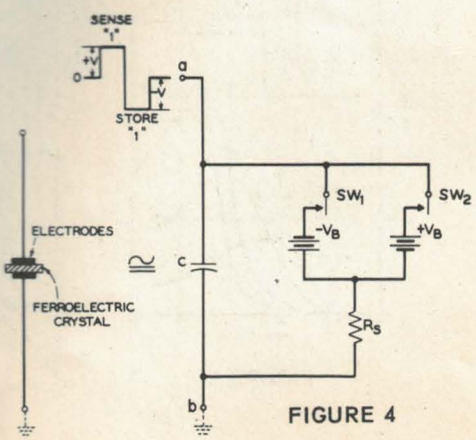


FIGURE 4

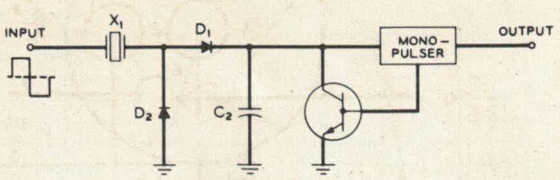


FIGURE 5

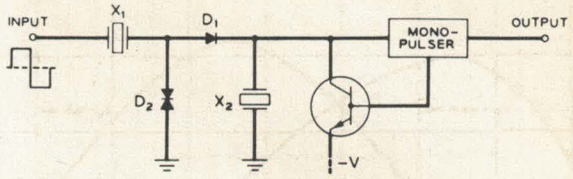


FIGURE 6

5.3 SWITCHING CHARACTERISTICS OF MAGNETIC CORES AS CIRCUIT ELEMENTS

R. D. Torrey, A. I. Krell, and C. Meyer -- Sperry Rand Univac, Philadelphia

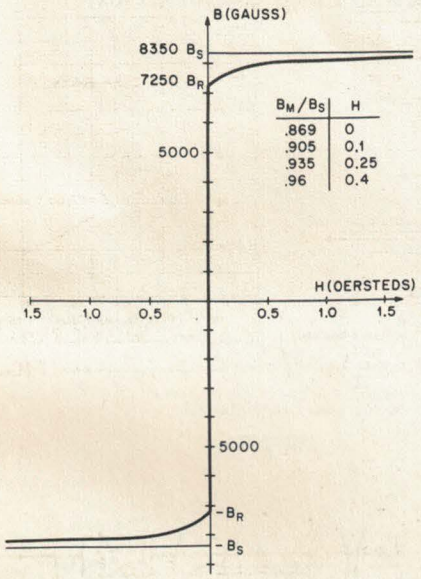
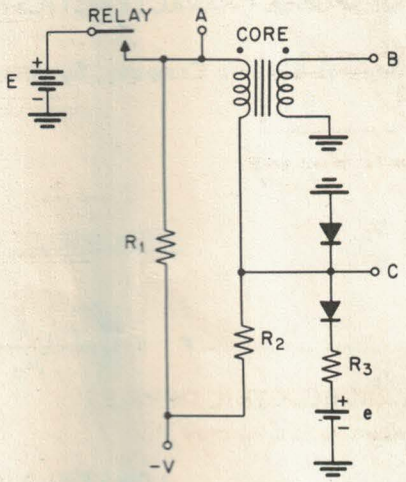


FIGURE 1



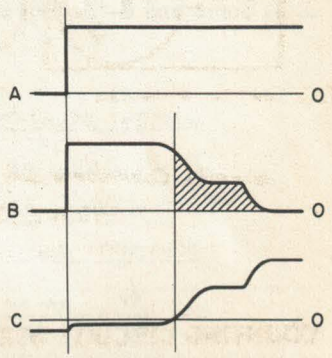


FIGURE 2

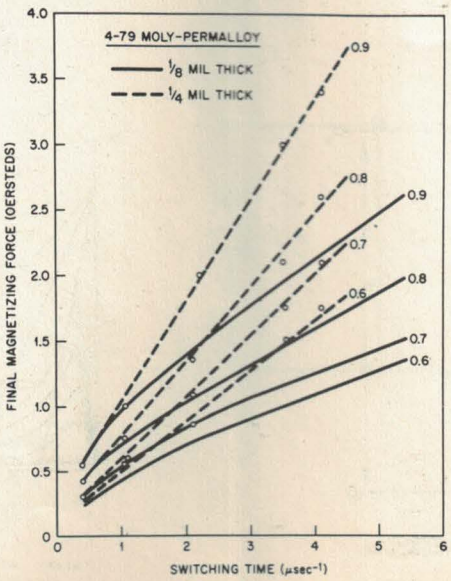


FIGURE 3

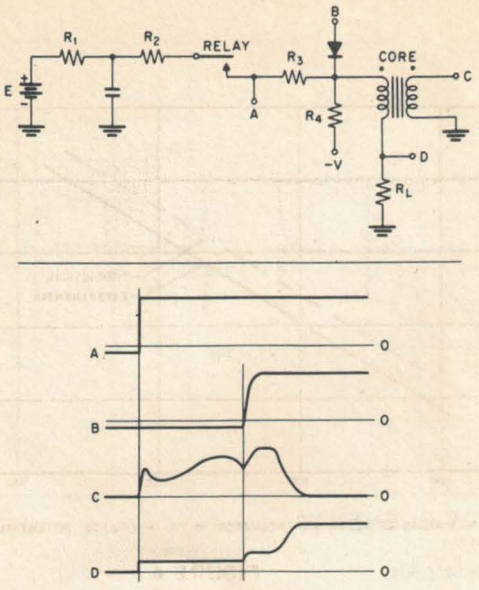


FIGURE 4

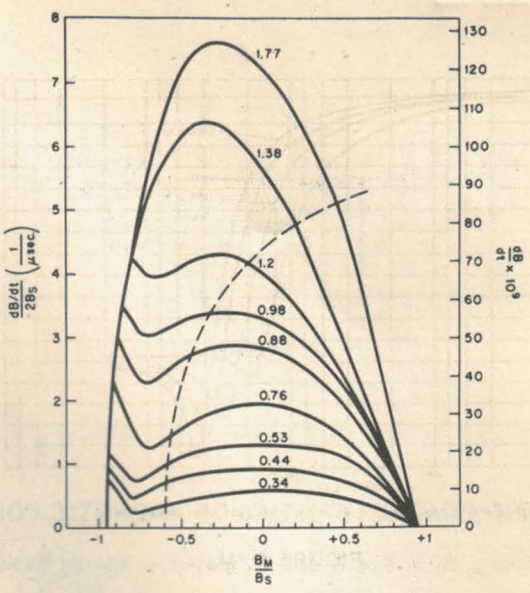


FIGURE 5

5.4 TRANSIENT AND FREQUENCY RESPONSE CHARACTERISTICS OF FIELD EFFECT UNIJUNCTION TRANSISTORS

J. J. Suran and B. K. Eriksen – General Electric Company, Syracuse

CURRENT EQUATIONS

$$J_p = Q\mu_p\, pE - Q D_p \nabla p$$

$$J_n = Q\mu_n\, nE + Q D_n \nabla n$$

CONTINUITY EQUATIONS

$$\frac{\partial p}{\partial t} = -\frac{(p-p_o)}{\tau_p} - \frac{1}{q}\nabla \cdot J_p$$

$$\frac{\partial n}{\partial t} = -\frac{(n-n_o)}{\tau_n} + \frac{1}{q}\nabla \cdot J_n$$

POISSON'S EQUATION

$$\nabla \cdot E = \frac{4\pi q}{\epsilon}\,(P - n + N_d - N_a)$$

SUPERPOSITION

$$J_T = J_p + J_n$$

FIGURE 1

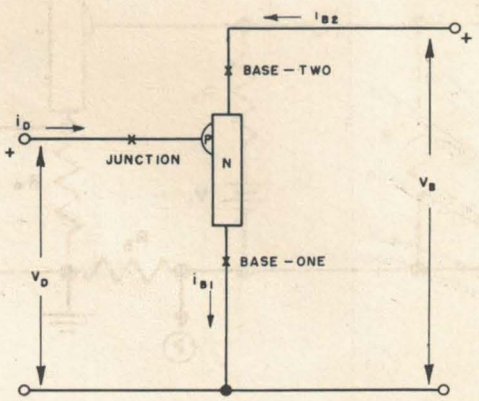
HIGH-FIELD CASE

$$\gamma = \left|\left(\frac{\mu_n + \mu_p}{\mu_p}\right)\left(\frac{\sin\frac{\omega t_t}{2}}{\frac{\omega t_t}{2}}\right)\right| \angle \frac{\omega t_t}{2}$$

LOW-FIELD CASE

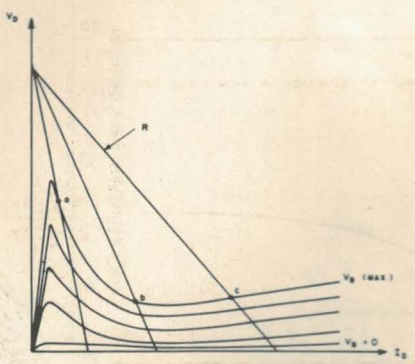
$$\gamma = \left|\left(\frac{\mu_n + \mu_p}{\mu_p}\right)\left(\frac{\tau_p}{t_t}\right)\left(\frac{1}{\sqrt{1+\omega^2\tau_p^2}}\right)\right| \angle \text{TAN}^{-1}\,\omega\,\tau_p$$

FIGURE 2



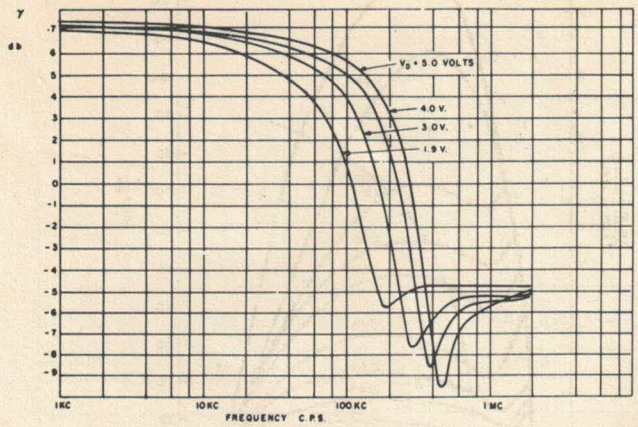
DOUBLE - BASE DIODE NOMENCLATURE

FIGURE 3



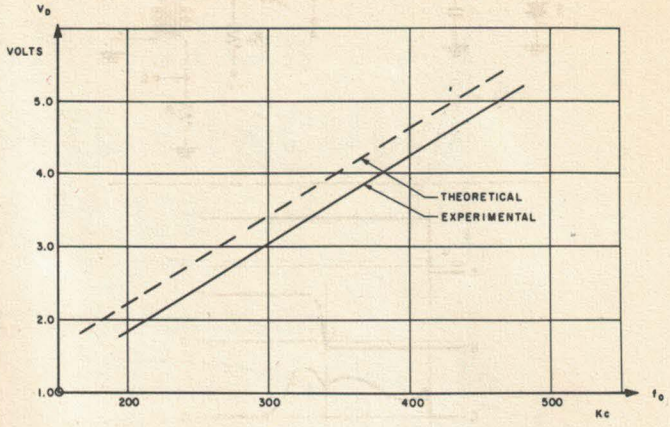
STATIC INPUT CHARACTERISTIC

FIGURE 4



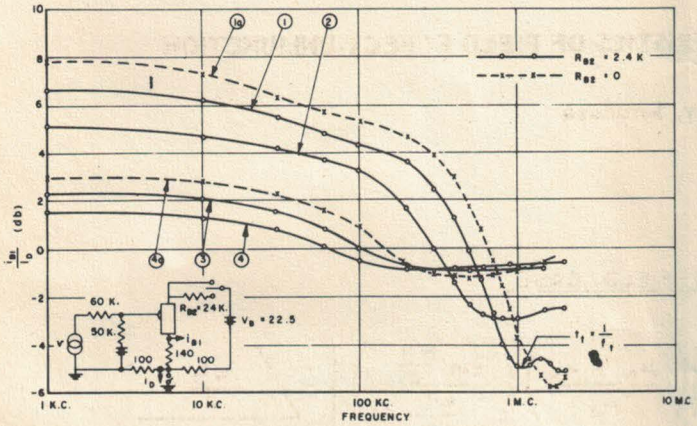
γ -CURVES FOR THE UNIJUNCTION TRANSISTOR (GERMANIUM)

FIGURE 5



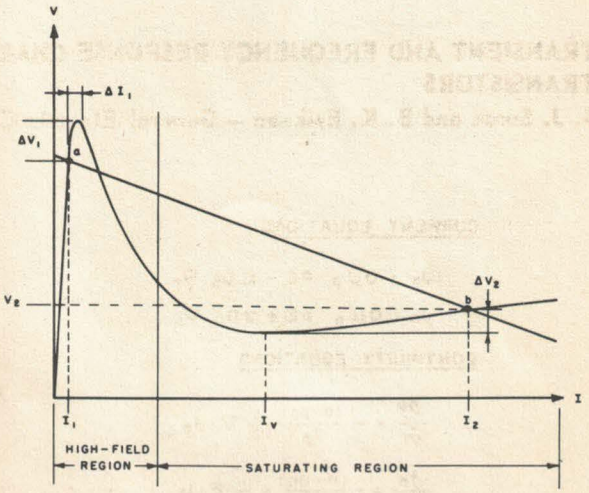
VARIATION OF RESONANT FREQUENCY WITH INTERBASE POTENTIAL

FIGURE 6



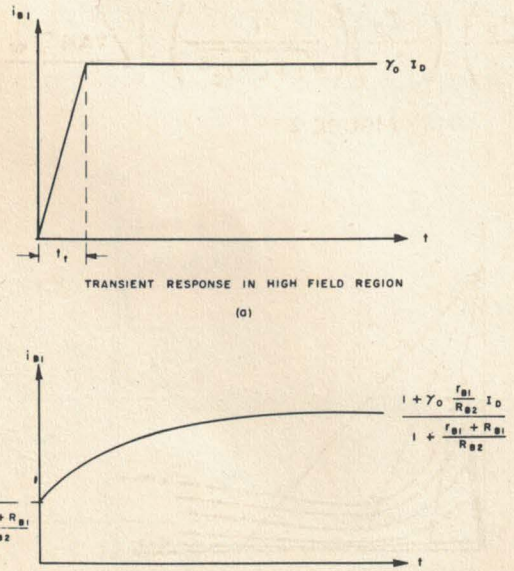
SMALL SIGNAL FREQUENCY RESPONSE
SILICON UNIJUNCTION TRANSISTOR

FIGURE 7



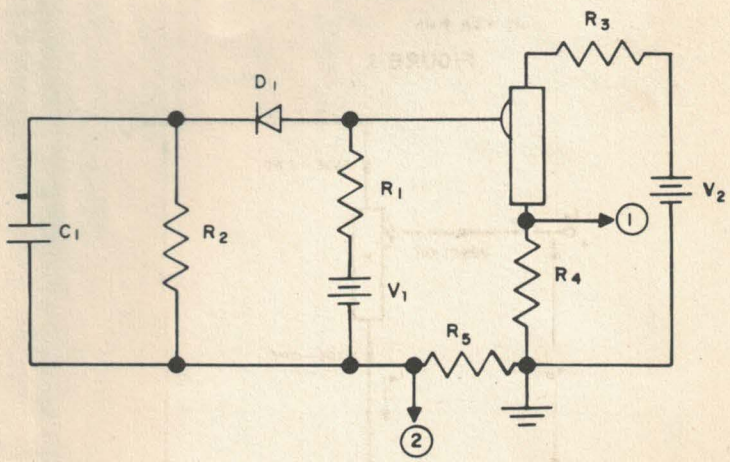
INPUT CHARACTERISTIC WITH BISTABLE LOAD LINE

FIGURE 8



SMALL SIGNAL TRANSIENT RESPONSES

FIGURE 9



MULTIVIBRATOR CIRCUIT

FIGURE 10

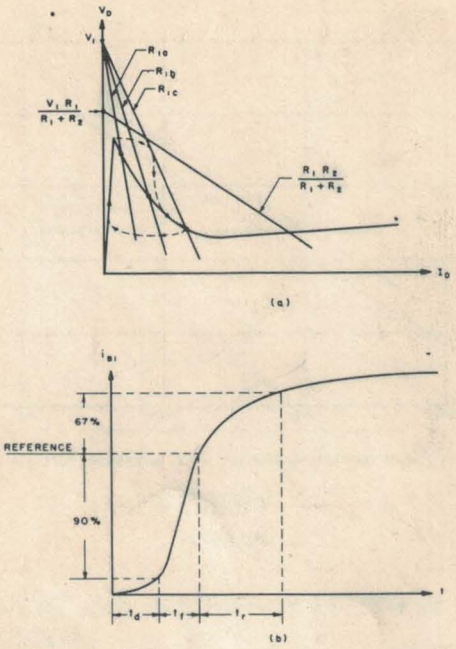
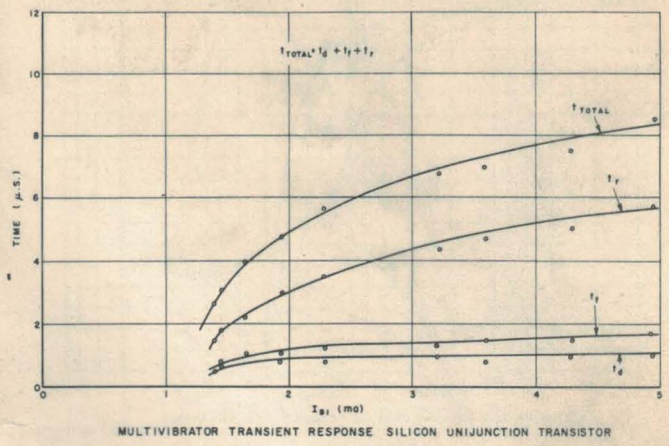


FIGURE 11



MULTIVIBRATOR TRANSIENT RESPONSE SILICON UNIJUNCTION TRANSISTOR

FIGURE 12

72" = 1"

720 min.

49 = 1"

25 = 5.6 = 1"

3

164

196 = 1"

3 1/2