1956 TRANSISTOR CIRCUITS CONFERENCE

Sponsored by

IRE-AIEE-U of P

THURSDAY-FRIDAY
16-17 FEBRUARY 1956

IRVINE AUDITORIUM
AND
UNIVERSITY MUSEUM

UNIVERSITY OF
PENNSYLVANIA

PHILADELPHIA

SCHEDULE

THURSDAY, FEBRUARY 16

8:00 A.M. — REGISTRATION OPENS
Irvine Auditorium

9:30 A.M. — 12:00 Noon — SESSION I
Irvine Auditorium

9:30 A.M.—12:00 Noon — SESSION A
University Museum

12:00 Noon — 2:00 P.M. — LUNCH
Houston Hall

2:00 P.M. — 2:30 P.M. — Irvine Auditorium
Formal Opening of Conference

2:30 P.M. — 5:30 P.M. — SESSION II
Irvine Auditorium

2:45 P.M. — 5:30 P.M. — SESSION B
University Museum

6:00 P.M. — COCKTAIL BUFFET
Penn Sherwood Hotel

7:00 P.M. — INFORMAL GROUP DISCUSSIONS
Penn Sherwood Hotel

FRIDAY, FEBRUARY 17

8:30 A.M. — REGISTRATION OPENS

9:00 A.M. — 12:00 Noon — SESSION III
Irvine Auditorium

12:00 Noon — 2:00 P.M. — LUNCH
Houston Hall

2:00 P.M. — 4:30 P.M. — SESSION IV
Irvine Auditorium

The 1956 Transistor Circuits Conference is sponsored jointly by the IRE Professional Group on Circuit Theory, The Committee on Transistor Circuits of AIEE, and the University of Pennsylvania. The Conference is patterned after the previous ones held at the same location for the past several years and will include information on both linear and nonlinear transistor circuit applications. Emphasis will be on material not previously available in the literature and the program is designed to be of greatest value to engineers who already possess some knowledge of transistor circuit behavior. However, there is one day of tutorial papers scheduled for the purpose of orienting those who are newer to this branch of science.

Publication of many of the papers in professional journals is planned in lieu of Conference Transactions.

SESSION 1

THURSDAY, 9:30 a.m.—12:00 Noon—Irvine Auditorium

SPECIAL CIRCUITS

Chairman: P. L. Bargellini, *University of Pa.*

1.1 Audio Automatic Volume Control Circuit

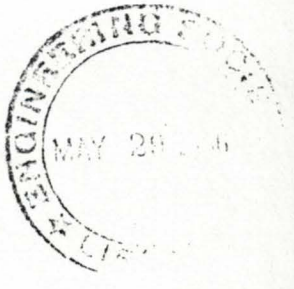
B. D. Griffith and J. Tom (U. S. Army)
Radio Corp. of America, Camden

Audio communication systems working through very high ambient noise levels require some kind of automatic volume control to maintain the signal above the noise and at the same time, protect the listeners' ears from painfully loud sounds. The problem is somewhat complicated by the fact that very little distortion can be tolerated.

The electron tube predecessor of this amplifier used a remote cut-off pentode for automatic gain control. No such principle is available in transistor circuits.

A large number of circuits were evaluated for automatic gain control characteristics. The most successful of these circuits was an absorption or shunting method in which the base-emitter resistance of a common base amplifier is the variable circuit element. A three-winding input transformer is connected between microphone and amplifier with the third winding being connected to the absorption circuit. A portion of the amplifier output signal is rectified, filtered and fed to the control transistor as its sole source of emitter current. This results in absorption of the microphone signal in proportion to amplifier output.

A 30 db increase in input signal can be reduced to less than 5 db increase in output with the total harmonic distortion being less than 5 percent.



(about 10:30 a.m., Thursday)

1.2 Linear Amplifier Employing Nonlinear Amplication

R. F. Grantges and J. Holzer

Signal Corps Engineering Laboratory, Fort Monmouth

A new type of linear amplifier is described which uses highly nonlinear active elements and yet achieves power amplification with essentially no nonlinear distortion. Linear amplification is accomplished by converting an input signal into a special type of pulse modulation in which only equally shaped pulses are employed. These pulses can be amplified by efficient pulse amplifiers of high nonlinearity and then reconverted to an amplified form of the original signal by means of linear passive networks.

A typical circuit using transistors as the nonlinear active devices will be presented. It will be shown that, so long as the input signal is within the amplitude and frequency limits imposed by the time constant of the input circuit and the pulse repetition frequency limit of the transistor, the amplifier will produce negligibly small distortion. The power efficiency of the amplifier and possible forms of output circuits will be discussed. Some promising applications will be mentioned.

(about 11:00 a.m., Thursday)

1.3 Voltage-Tuned Networks Using Junction Diodes

C. R. Hurtig, *Massachusetts Institute of Technology*

The use of conventional RC filters in transistor amplifiers often results in conflicting circuit requirements since conventional filters are designed for voltage source drive and open circuit load, whereas transistors readily supply a current source drive and short circuit load. By the use of Reciprocity and Thevenin's theorems, it can be shown that the open-circuit voltage transfer ratio of a conventional two-terminal pair network and the short-circuit current transfer ratio of the same network with its input and output terminals reversed are identical.

By use of forward biased junction diodes as the resistance elements of RC filters used in transistor feedback amplifiers, the magnitudes alone of the complex natural frequencies of the system may be made a linear function of a control voltage. Two specific examples are given: a phase shift oscillator, and a Twin-Tee amplifier. In each of these circuits the frequency of operation may be varied over at least a ten to one range by an external control voltage. The frequency, which is in the audio range, is, within a few percent, a linear function of the control signal. The dynamic range at the output is at least 40 db, and the harmonic distortion is less than 2%. In both circuits there are two basic limitations to the linearity of the frequency control. The upper limit is caused by a departure of the incremental resistance characteristic of the diode from a simple inverse dependence upon direct current bias, at high values of current. The lower limit is caused by the allowable distortion and/or the required signal-to-noise ratio.

(about 11:30 a.m., Thursday)

1.4 Multiterminal Semiconductors Operated as Two-Terminal Source-Free Switching Devices

Abraham Har'el, *University of Pennsylvania*

For various applications, particularly in a telephone switch ing matrix, it is important to have a semiconductor devic which can be operated as a two-terminal source-free switch ing and transmission device.

This has been accomplished with a single semiconducto device, combined with one ohmic resistor, the device bein either a point contact transistor, or a junction transistor, a modified junction doubled-base-diode.

The device should be able to exhibit a region of negativ AC resistance. The emphasis is on the use of the resisto to create the "blocking voltage" which prevents flow of cu rent until a desired voltage is reached.

END OF SESSION I

Lunch served in Houston Hall—12:00 Noon-2:00 p.m

SESSION A

THURSDAY, 9:30 a.m. — 12 Noon — University Museum

Tutorial Sessions

This series of four talks (two in Session A and two in Session B) is designed to cover the entire field of transistor circuit application. They are intended to benefit the engineer who has a general background in electronic circuits but who has little direct transistor experience. The lectures will explain the basic fundamentals and will include the latest concepts.

A.1 Analysis and Equivalent Circuits

R. B. Adler, *Massachusetts Institute of Technology*

(about 10:45 a.m., Thursday)

A.2 Switching Circuits

R. H. Baker, *Lincoln Laboratory, M.I.T.*

END OF SESSION A

Lunch served in Houston Hall—12:00 Noon-2:00 p.m.

SESSION II

2:30 p.m.—5:30 p.m.—Irvine Auditorium

SWITCHING CIRCUITS

Chairman: H. E. Tompkins, *Burroughs Corporation*

2.1 Direct-Coupled Transistor Logic Circuitry in Digital Computers

J. R. Harris, *Bell Telephone Laboratories, Murray Hill*

The TRADIC Computer Research Project is studying direct-coupled transistor logic (DCTL) circuitry for use in airborne computers. This circuitry, described by Philco in March, 1955, puts the burden of good performance on the transistor. Certain germanium alloy transistors are attractive because of high current-gain and low saturation resistance. Philco SB100 surface barrier units are attractive where more speed and less gain are needed. A new Texas Instruments grown silicon unit having low saturation voltage (LSV) offers high temperature operation plus greater signal voltage which gives greater freedom in logical design and minimizes crosstalk. Crosstalk studies indicate a possibility of false switching in a large system of germanium transistors. This problem, which is more severe with faster transistors, appears readily soluble in a system of a few thousand 10-megacycle germanium alloy units.

In order to write logical design rules and a transistor specification, a system has been viewed as an assemblage of current-supply resistors, all the same size, with bases and collectors attached to each resistor (node). When all transistors driving a node are nominally off, the object is that maximum leakage currents of the collectors, plus current that is adequate for the bases on that node under worst conditions, shall never exceed the supply current. When a transistor driving a node is nominally conducting, the object is that it shall handle the entire supply current, and do this at a collector voltage that is near enough ground that collector leakage in every transistor driven from the node is below a fixed maximum. These concepts (with specific allowance for crosstalk voltage, resistor tolerances, "regulation" of an individual current supply, unbalance of base currents and temperature) have led to transistor specifications and logical design rules in which simple restrictions on the number of bases and collectors on a node are sufficient to guarantee safe operation. The germanium transistor specification permits a maximum total of 7 bases and collectors on a node, fewer when a series circuit (2 level AND circuit) is driven.

A DCTL word generator using 119 Radio Receptor RR163 germanium alloy units operated without cut-and-try over a temperature range exceeding $-50°C$ to $+65°C$ at 400,000 parallel words per second. An 800-transistor system for exercising a magnetic core memory is being tested.

(about 3:05 p.m., Thursday)

2.2 Transistor Requirements for Direct-Coupled Transistor Logic Circuits

J. W. Easley,
Bell Telephone Laboratories, Murray Hill

The basic requirement for stability of a direct-coupled transistor logic (DCTL) circuit of the type described in the preceding paper is that a voltage margin, Δ, exist between the maximum V_{CE} of an "on" unit in the system environment and the minimum V_{BE} required for a transistor to be sufficiently "off." This margin has been expressed in the form $\Delta = \Delta(\alpha_N, \alpha_I, k, I_{co}) = \Delta_1(\alpha_N, \alpha_I, k) + \Delta_2(I_{co})$

where the parameter, k, is the ration of α at currents of the order of the collector leakage current in the "off" state to α at currents of the order of the collector current in the "on" state. Consequently the significant DCTL circuit variable, Δ, can be expressed in terms of transistor parameters which are related to the physical structure of the transistor through existing design theory. Similarly, any given transistor type can be evaluated for employment in DCTL systems on the basis of these more familiar and fundamental parameters.

In addition to the above factors, the connection of bases in parallel results in a dependence of stability on the magnitude of the ohmic base resistance in the saturation region, r_{bIII}, and on the variations of r_{bIII}, α_N, α_I and I_{co} among units connected in this manner. Circuit stability requirements have been expressed in terms of these parameters and their variations. This analysis permits a determination of the expected yield of transistors satisfactory to DCTL from a statistical description of any transistor population in terms of these parameters. A minimum value of r_{bIII}, which will provide stability without inclusion of external base resistance can be determined. Good correlation has been obtained between the results of the analysis and experimental observations.

(about 4:20 p.m., Thursday)

2.4 Circuit Properties of the Conjugate-Emitter (Hook-Collector) Transistor

J. J. Suran,
General Electric Company, Syracuse

The conjugate-emitter transistor is a three-junction, three-terminal semiconductor device which exhibits a negative-resistance characteristic. It is approximately equivalent to a directly-cascaded combination of an NPN and PNP transistor. By appropriate circuit variations, a negative resistance input characteristic may be obtained in any of the four quadrants of the $V_i - I_i$ plane. The conjugate-emitter transistor derives its negative-resistance characteristic from the fact that there is current amplification through the device and that the output current may be fed back through the common base lead to provide a regenerative potential in the input circuit.

The fact that conjugate-emitter transistors may be fabricated by wide-area junction techniques makes it possible to build these devices for high-power switching applications. Such circuits as sawtooth and square wave oscillators, regenerative pulse amplifiers and bistable flip-flops have been designed and operated with experimental devices to yield average power outputs in the order of 100 watts. Switching-on action at these power levels occurs in the order of one microsecond, but the time required to turn the device off is from ten to twenty times longer.

High-power conjugate-emitter transistors show considerable promise in such applications as video sweep circuits, computer read-out networks, pulse-code transmitters and motor-control circuits.

(about 4:55 p.m., Thursday)

2.5 High Speed Transistor Computer Circuits

S. Y. Wong and A. K. Rapp,
Philco Corporation, Philadelphia

Very fast switching circuits are made possible through the use of surface-barrier transistors (SBT's). Representative values of speed are given in the following table which lists the transition times of various flip-flops using typical commercially available SBT's. Transition time is defined as the time interval between the 10% point of the collector voltage of the gating transistor and the 90% point of the collector voltage of the off-going transistor in the flip-flop.

Flip-Flop Type	Transition Time in μsec.
Direct-Coupled	110
R-C-Coupled	90
Emitter-Follower-Coupled	36
Nonsaturating R-C-Coupled	33
Nonsaturating Emitter-Follower-Coupled	22

It should be emphasized that these speeds are merely representative ones and do not represent the ultimate obtainable with SBT's.

The use of emitter followers in carry propagation circuits can produce very fast parallel adders. Propagation speeds of the order of 10 millimicroseconds per stage are achievable.

The performance of these circuits suggests the physical realizability of a completely transistorized arithmetic and control unit for a computer capable of speeds that are at least as great as those available from computers using the fastest conventional vacuum tubes.

END OF SESSION II

6:00 p.m.—Cocktail-Buffet—Penn Sherwood Hotel
7:00 p.m.—Informal Group Discussions—
Penn Sherwood Hotel

SESSION B

THURSDAY, 2:45 p.m.-5:30 p.m.—University Museum

Tutorial Sessions

B.1 Low Frequency Circuits

F. D. Waldhauer,
Radio Corp. of America, Camden

(about 3:55 p.m., Thursday)

B.2 High Frequency Circuits

J. B. Angell,
Philco Corporation, Philadelphia

END OF SESSION B

6:00 p.m.—Cocktail-Buffet—Penn Sherwood Hotel
7:00 p.m.—Informal Group Discussions—
Penn Sherwood Hotel

SESSION III

FRIDAY, 9:00 a.m.-12 Noon—Irvine Auditorium

SMALL SIGNAL AMPLIFIERS

Chairman: R. H. Mattson,
Bell Telephone Laboratories, Murray Hill

3.1 Transistor D-C Amplifiers

J. W. Stanton,
G.E. Advanced Electronics Center at Cornell University

Transistorized d-c amplifiers offer several advantages over vacuum tube d-c amplifiers because of their small size, small power consumption and increased reliability. However, the inherent drift in the I_{co} of transistors and the extreme sensitivity of all of the transistor parameters to ambient temperature have discouraged and delayed the application of transistors to d-c amplifiers. This is generally true for all transistors, but particularly true for germanium transistors. This paper describes a unique circuit which makes the use of transistorized d-c amplifiers practical. This circuit may be used with germanium or silicon transistors.

The general problems that face the designer of transistorized d-c amplifiers are discussed. A specific d-c amplifier is described, and particular emphasis is placed on overcoming the difficulties associated with ambient temperature changes.

Results obtained on experimental models show that reliable transistorized d-c amplifiers may be built. Sensitivities in the microampere and millimicroampere range have been obtained even when the ambient temperature is varied over a wide range. Experimental circuits have been built with sensitivities of better than 0.01 microampere. The drift at room temperature is less than 0.05% full-scale per twenty-four hours. A linearity of better than 0.2% and an equivalent input drift current of less than 0.5 microampere over an ambient temperature range of 0 °C to 50 °C have been achieved. The frequency response is flat from zero to greater than 50 kc. Observations for relatively long periods of time have shown no noticeable transistor aging effects.

(about 9:40 a.m., Friday)

3.2 Transistor Amplifier Performance

J. F. Gibbons,
Stanford University

Fundamental restrictions on the gain, bandwidth, and sensitivity which can be achieved in multistage transistor amplifiers arise from the inherent internal feedback and frequency dependency of the device parameters. These gain and bandwidth limitations are discussed in terms of Linvill's power gain charts and the resistance integral theorem. A new set of charts are then devised which permit rapid evaluation of the effects of load impedance on input impedance at a given frequency. A sensitivity criterion is defined as the percentage change in input impedance for a given change in load impedance. This criterion allows one to plot areas on the charts from which the load impedances must be selected for the required sensitivity. For small sensitivity, a relation between sensitivity and power gain is derived which enables one to determine how much power gain must be lost for a given sensitivity. This information permits direct comparison of neutralized and unneutralized amplifiers.

The theory given above serves to specify operating impedances and insertion loss of the interstage and load networks at a set of discrete frequencies in the amplifier pass band. The design of these networks can again be cast in terms of the charts and power gain formulas.

(about 10:15 a.m., Friday)

3.3 Behavior of Noise Figure in Junction Transistors Over Their Useful Frequency Spectrum

E. G. Nielsen,
Bell Telephone Laboratories, Murray Hill

It is well known that the driving source resistance and DC emitter current are two major factors in determining the noise figure of junction transistors. Other factors are the base resistance, low frequency alpha (α_o), and alpha cut-off frequency ($f_{c\alpha}$). A method of calculating the noise figure in terms of these parameters, the frequency variation of the noise figure, and the conditions for minimizing the noise figure will be presented.

For the common base, common collector, and common emitter configurations the noise figure as a function of frequency is constant up to $f_{c\alpha}\sqrt{1-\alpha_o}\, f_{c\alpha}$. Above this frequency, it increases toward an asymptote of 6 db per octave. Calculations show that for minimum noise figure the base resistance and emitter current should be small, α_o should be close to one, $f_{c\alpha}$ should be large, and the driving source resistance has an optimum value.

Experimental verification of the results to frequencies beyond $f_{c\alpha}$ will be presented. The work is based on a simplified version of a transistor noise equivalent circuit developed by A. van der Ziel.*

*A. van der Ziel, "Theory of Shot Noise in Junction Diodes and Junction Transistors," *Proceedings of the I.R.E.*, November, 1955, v. 43, pp. 1639-1646.

(about 10:50 a.m., Friday)

3.4 A Carrier-Frequency Transistor Feedback Amplifier

D. A. DeGraaf and F. H. Blecher,
Bell Telephone Laboratories, Murray Hill

This paper describes techniques for designing transistor feedback amplifiers at carrier frequencies (above 5 kc). It is shown that the loop current transmission is a very useful measure of feedback for both theoretical and experimental considerations. Various methods of shaping the loop current transmission such as local feedback, interstage network, and overall β circuit shaping are discussed.

The design techniques are illustrated by a three-stage carrier frequency feedback amplifier which has 40 db of external voltage gain and 36 db of feedback over a frequency band extending from 5 kc to 500 kc. Over this band the external gain is maintained constant to within ± 0.2 db and the input and output impedances of the amplifier match a 600 ohm line within $\pm 3\%$. The loop current transmission is shaped in order to obtain a Bode type high frequency cutoff characteristic. The amplifier has a 30 degree phase margin and a 12 db gain margin. The low frequency end of the loop current transmission is cut off at a rate of 6 db per octave. Very close agreement is obtained between the theoretical design and experimental measurements.

(about 11:25 a.m., Friday)

3.5 The Design of Bridge-Derived Circuits for Precision Control of Transistorized Amplifiers

W. S. Chaskin, V. Babin and I. Gottlieb,
Lenkurt Electric Company, Inc., San Carlos

In the design of carrier telephone amplifiers and other precision amplifiers using transistors, the problem of maintaining constant input and output impedance is more severe than with vacuum tubes. This paper discusses application of negative feedback by bridge-derived methods which make possible amplifiers whose input and output impedances can be controlled within close limits for rather large variations in transistor parameters and ambient temperatures. Although the effect of simple feedback on the internal impedances of amplifiers is well known, the benefits to be gained by more complex networks have received very little publicity. In this discussion, it will be shown that combinations of shunt and series feedback can be arranged so that the advantages of bridge isolation can be obtained.

Equivalent and actual circuits will be analyzed mathematically, and certain design criteria derived; and it will be finally shown that, in addition to all the conventional benefits derived from negative feedback, very interesting and useful relationships between the input and output impedances of an amplifier may be established by the use of bridge-derived feedback methods.

END OF SESSION III

Lunch served in Houston Hall—12:00 Noon-2:00 p.m.

SESSION IV

FRIDAY, 2:00 p.m.-4:30 p.m.—Irvine Auditorium

POWER AMPLIFIERS AND POWER SUPPLIES

Chairman: G. H. Royer,
Westinghouse Electric Corp.

4.1 Temperature Effects in Circuits Using Junction Transistors

H. C. Lin and A. A. Barco
RCA Laboratories, Princeton

The effects of varying ambient temperature upon the performance of transistor circuits have been evident since the beginning of the transistor art. However, the nature of these effects, the causes of these effects, and the methods by which they may be minimized have not generally been appreciated by the circuit design engineer. This paper is concerned with these matters, principally as they relate to germanium alloy-junction transistors and the circuits in which they are used.

The behavior of the transistor with respect to temperature is most adversely affected by changes in the saturation current and the DC input conductance. The effects of variations in these parameters upon the transfer characteristics are shown experimentally and analytically.

When transistors are used in some of the more familiar and frequently employed circuits these two causes may affect performance by shifting the DC operating point, i.e., the bias. Such circuits are inherently sensitive to temperature and some may be severely affected by relatively small temperature changes.

For many circuit applications, from audio frequencies up through broadcast frequencies, satisfactory operation is obtained if the quiescent emitter current is held constant with changing temperature. Several means for achieving this condition, including circuits employing DC degeneration or feedback, are described. Such circuits are inherently stable with temperature and may be made to operate satisfactorily over a wide range of temperature.

Circuits such as those of detectors or class B amplifiers present special biasing problems which may be solved by means of techniques which use diodes, transistors, or thermistors to provide bias compensation.

When due circuit consideration is given to the effects both of saturation current changes and DC input conductance changes, germanium alloy-junction transistor circuits operate satisfactorily over a wide range of ambient temperature.

(about 2:30 p.m., Friday)

4.2 Design Considerations for Semiconductor Regulated Power Supplies

S. Sherr and P. Levy
General Precision Laboratory, Pleasantville

Circuit configurations have been developed for a number of all semiconductor regulated power supplies, both constant current and constant voltage, at low ripple factors. All of the circuits have been analyzed, assuming straight line transistor characteristics. The equation for these characteristics is $i_c = \frac{v_c}{r_c(1-\alpha)} + \beta i_b$

A convenient circuit is the shunt voltage regulator, requiring only one transistor and a reference diode as the semiconductor elements. The simplified regulation equations are

$$\frac{dE_o}{E_o} = \frac{1}{1+\beta\frac{E_r}{E_i}\frac{R_s}{R_b}}\frac{dE_i}{E_i} \qquad \frac{dE_o}{E_o} = \frac{1}{1+\frac{R_L}{R_s}+\beta\frac{R_L}{R_b}}\frac{dR_L}{R_L}$$

A second circuit provides voltage regulation using a NPN, PNP combination of two transistors, with one reference diode and no additional components. The simplified equations are

$$\frac{dE_o}{E_o} = \frac{1}{1+\beta_1\frac{E_r}{E_i}\frac{r_c(1-\alpha)}{r_b}}\frac{dE_i}{E_i} \qquad \frac{dE_o}{E_o} = \frac{1}{1+\beta_1\beta_2\frac{R_L}{R_b}}\frac{dR_L}{R_L}$$

These equations have been utilized to design circuits which have operated in good conformance with analysis.

Another circuit requires two transistors of only one type, either PNP or NPN and permits the use of presently available silicon transistors. These have been employed in a design which operated to 100° C. The simplified equations are

$$\frac{dE_o}{E_o} = \frac{1}{1+\beta_1\frac{E_r}{E_i}\frac{R_c}{R_b}}\frac{dE_i}{E_i} \qquad \frac{dE_o}{E_o} = \frac{1}{1+\beta_2\frac{R_L}{R_C}+\beta_1\beta_2\frac{R_L}{R_b}}\frac{dR_L}{R_L}$$

Variations of these basic circuits have been analyzed with some performance improvement indicated for certain configurations.

Heat sink design requires graphical information on dissipation and the equation $T_j = T_a + P \Sigma R_t$

A representative design has been made and tested for a six volt, two ampere supply.

The circuits described make it possible to design all semiconductor power supplies with efficiencies from 50% to 75%. Voltages from 6 to 150 and currents as high as two amperes are representative, though not necessarily the limits of operation. Certain low voltage high current supplies are now possible which could not have been conveniently achieved using vacuum tubes.

(about 3:00 p.m., Friday)

4.3 The Design of Transistor DC to DC Transformers for a High Degree of Reliability and Stability

U. M. Thompson,
Canadian Defence Research Establishment, Ottawa

Failures in transistor DC to DC converters have been more frequent than would be expected from transistor life.

This paper deals with the causes of failure, particularly the excessive dissipation of power in the collector during switching. The collector has a short thermal time constant, so that the instantaneous dissipation becomes important. This instantaneous dissipation depends upon several factors, particularly leakage inductances, and the type of rectifying and smoothing circuit.

It describes a method of designing these converters to be stable, and insensitive to variations in load and transistor parameters.

Finally, using a 10 watt converter as an example, it is shown how the desired characteristics, efficiency, small size, stability, and reliability can be traded with one another to achieve an acceptable design.

(about 3:30 p.m., Friday)

4.4 Single Power Transistor DC-DC Converter

D. A. Paynter,
General Electric Co., Syracuse

The usual transistor method for performing DC conversion at medium and high power levels utilizes two power transistors connected into a symmetrical push-pull square-wave oscillator circuit. An unsymmetrical version of the oscillator which uses only one power transistor and one low power core reset transistor is described in the paper.

Circuit configuration and operation is similar to that of the two power transistor converter. An unsymmetrical square wave of voltage is produced when the transistors alternately switch the converter supply voltage across the primary transformer windings. Transistor switching occurs each time the transformer core becomes saturated. The polarity of the windings and half-wave rectifier are arranged so that power is delivered to the load only during the time that the power transistor is conducting. The core reset transistor, which serves to reverse the magnetization of the transformer core after each operation of the power transistor, does not contribute power to the load and hence may be of the low power 150 mw variety in many applications.

The circuit is arranged so that the full capabilities of the power transistor (voltage rating and current handling ability) can be utilized without sacrificing the high efficiency of the symmetrical converter. Maximum power is obtained for a given supply voltage if the power transistor duty cycle is arranged for a maximum consistent with the transistor inverse voltage rating. A comparison of the power handling abilities of the single power transistor circuit with that of the two power transistor version indicates that the power capability of the former approaches that of the latter converter for the case when a low supply voltage is used along with a power transistor with a high inverse voltage rating.

An experimental converter which utilized a power transistor conduction ratio of 3 to 1 was capable of delivering about 20 watts at an efficiency of 75% and 10 watts at about 90% efficiency when powered from a 12 volt source.

(about 4:00 p.m., Friday)

4.5 Characteristics and Circuit Applications for a New Type Power Transistor

J. F. Marshall,
Minneapolis-Honeywell Regulator Company, Minneapolis

A power transistor whose current gain can be controlled over a wide range of currents, by means of associated circuitry, has been realized in the form of a tetrode power transistor. The shape of the current transfer characteristic of this transistor is adaptable to the most desirable form for several different modes of operation.

Circuit configurations for the power tetrode are discussed which provide the standard current gain characteristic of triode transistors in which the current gain becomes a maximum at relatively low currents and then falls progressively with increasing currents. This characteristic is desirable for class B null balance servo systems which want maximum gain near balance and lower gain at large error signals.

The current gain of this transistor can be controlled to provide an essentially linear current transfer characteristic out to collector currents of about 10 amperes. This mode of operation is important to those applications where good amplitude linearity is important, such as in audio and other distortion sensitive systems.

Other circuitry can be employed to depress the current gain to low values for relatively small currents while allowing the gain to rise to a peak value at some high collector current, say, 5 amperes, for example. This type of transfer characteristic is valuable in switching modes. In the "off" condition a transistor operated in the common emitter is less sensitive to variations in collector-to-base leakage because the current gain is low. Also, common emitter response times are considerably improved.

The tetrode power transistor promises to be a versatile component whose response can be tailored to a variety of requirements by means of external circuitry.

END OF SESSION IV

1956 TRANSISTOR CIRCUITS CONFERENCE
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Edmundo Gonzalez-Correa .. *Evans Signal Corps Laboratories*
Robert Henle ..... *IBM Corp.*
David D. Holmes ..... *RCA Laboratories*
Lionel E. Thibodeau ..... *Remington Rand Univac*
Howard E. Tompkins ..... *Burroughs Corp.*

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Wm. J. Popowsky, *Chairman*
Minneapolis-Honeywell Regulator Co.

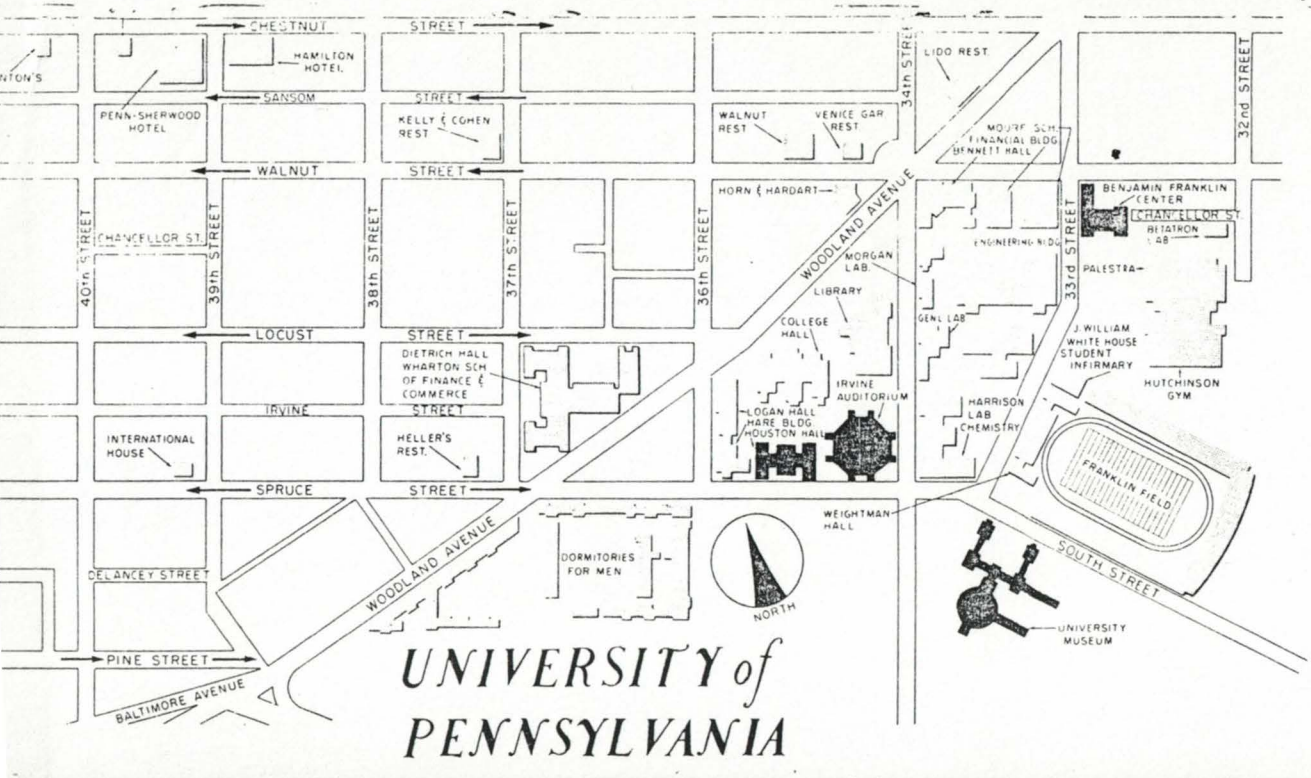
INFORMATION DESK

The attendant at the Information Desk, located in the main Lobby of Irvine Auditorium, will answer your questions regarding transportation, facilities, messages, Philadelphia restaurants, etc. A Convention map of the city is available to supplement the local area map on the back cover of this booklet.

INFORMAL GROUP DISCUSSIONS

A repeated feature from last year will be the informal group discussions to be held at the Penn Sherwood Hotel following the cocktail buffet on Thursday evening. Several discussion rooms have been reserved at the hotel.

Suggestions for discussion topics have been requested by the Chairman of the Program Committee, Harry J. Woll, who may be reached by way of the Information Desk during the first session.



UNIVERSITY of PENNSYLVANIA

(about 3:40 p.m., Thursday)

2.3 Junction Transistor Switching Circuits for High Speed Digital Computer Applications

G. J. Prom and R. L. Crosby
Sylvania Electric Products, Inc., Waltham

This paper describes junction transistor switching circuits capable of reliable operation at a rate of 1,000,000 pps. These circuits consist of a flip-flop, a gated pulse amplifier and diode gates which together provide the basic building blocks of the arithmetic section of a digital computer. The designs are based on transistor types, such as alloy junction and surface barrier transistors, which exhibit low and consistent values of extrinsic resistances. As a result, complete interchangeability is obtained from a simple circuit. Several suitable high frequency alloy junction transistor types, both NPN and PNP, are available commercially in large quantities at relatively low cost. A minimum alpha cutoff frequency, $f_{c\alpha}$, of 5 megacycles and a minimum alpha, α, of 0.95 are the most important transistor requirements. Special devices such as Zener diodes are not required.

Flip-flop rise and fall times of 0.3 microsecond and 0.2 microsecond, respectively, are obtained by the use of large drive currents, low values of collector load resistance, emitter followers to reduce loading effects, and by preventing transistor saturation. High speed diode gates and gated pulse amplifiers which are relatively insensitive to changes in gating levels are employed. Reliable operation over the temperature range of $-55°C$ to $+85°C$ is achieved by compensating for the decrease in β at low temperatures, and the increase of I_{co} at high temperatures. Test circuits have operated for over 1000 hours at $+85°C$ without failure.

A typical shift register constructed from the basic building blocks consists only of flip-flops and diode gates. Binary counters require the addition of a gated pulse amplifier for carry propagation. A multi-stage shift register with read-in and read-out gates and a multi-stage binary counter have been successfully operated at rates in excess of 1,000,000 pps. The combination of shift register and binary counters into typical accumulators is discussed with special reference to the solution of loading problems by proper impedance matching.