IRE — AIEE

Conference on

TRANSISTOR CIRCUITS

THURSDAY-FRIDAY
18-19 FEBRUARY 1954

MUSEUM OF THE UNIVERSITY OF PENNSYLVANIA

PHILADELPHIA

This Conference on Transistor Circuits is being sponsored by the IRE Professional Group on Circuit Theory, and the Science and Electronics Division of AIEE, with the objective of presenting a coherent set of papers, designed to interest the engineer already familiar with transistors, which describe in some detail the present state of the art of designing transistor circuits.

Detailed abstracts of each paper are presented on the following pages of this booklet. Many of the papers will be published in full in the journals of the sponsoring societies, or elsewhere. A multilithed list of bibliographical references has been prepared, and should have been enclosed with this booklet. If you did not receive one, inquire at the Information Desk.

The committee would welcome your comments about the program, arrangements, location, or any other aspect of the Conference. Please leave comments in written form at the Information Desk, or address them to any appropriate committee member. The committees for the Conference are listed at the end of this booklet.

FACILITIES

All sessions will be held in the Auditorium of the University of Pennsylvania Museum, 33rd, Spruce, and South Sts. Direct access to the Auditorium is via the driveway from 34th St., south of Spruce St. Alternatively, the main museum entrance, on South St. east of 33rd St., may be used. Parking space for a limited number of cars is available in the museum parking lot; the entrance is on the south side of South St., east of the Museum's main entrance.

The Rotunda of the Museum, two flights above the Auditorium, has been provided for our caterer to serve lunch. A very limited number of tickets will be available each day for those who have not ordered lunch in advance. They may be purchased at the Registration Desk. Those desiring to eat elsewhere will find several restaurants in the vicinity of 34th and Walnut Sts. (one block west and one block north of the Museum); some crowding may be expected, particularly after one o'clock, because of University lunch schedules.

The Brazilian Coffee Shop, one floor above the Auditorium lobby, is available for snacks throughout the day. The Museum itself is one of the finest in the world, and you are welcome to enjoy its extensive archeological and ethnological exhibits; descriptive literature is available at the desk just outside the Brazilian Coffee Shop.

A Cocktail-Buffet for Conference registrants will be held on Thursday at 6 p.m., at the Penn-Sherwood Hotel, 39th and Chestnut Sts. A limited number of tickets may still be available at conference-time; check at the Registration Desk.

TRANSPORTATION

Maps of the city are available at the Information Desk. Route 40 street cars provide direct transportation between the Museum and the Hotel Penn-Sherwood for those who do not care to walk seven blocks, and have not found a cab. From the Museum, board route 40 cars westbound on South or Spruce Sts., get off at 38th and Chestnut Sts., and walk one short block west. Returning, board route 40 cars southbound on 40th St. at Chestnut, one black west of the Hotel, and get off at the Museum, 33rd and Spruce Sts.

Routes 13 and 42, eastbound at 33rd and Spruce Sts., provide direct service to downtown Philadelphia via Chestnut St., and return to the same point via Walnut St. Running time is about fifteen or twenty minutes.

SCHEDULE

WEDNESDAY, FEBRUARY 17

7:00 p.m. - 11:00 p.m.—REGISTRATION
Penn-Sherwood Hotel

THURSDAY, FEBRUARY 18

8:00 a.m. - 5:30 p.m.—REGISTRATION
University of Pennsylvania Museum

10:00 a.m. - 12:30 p.m.—SESSION I
Auditorium of the University Museum

12:30 p.m. - 1:30 p.m.—LUNCH
Rotunda of the University Museum

2:30 p.m. - 5:00 p.m.—SESSION II
Auditorium of the University Museum

6:00 p.m. - 7:30 p.m.—COCKTAIL-BUFFET
Penn-Sherwood Hotel

FRIDAY, FEBRUARY 19

8:30 a.m. - 2:30 p.m.—REGISTRATION
University of Pennsylvania Museum

9:30 a.m. - 12:30 p.m.—SESSION III
Auditorium of the University Museum

12:30 p.m. - 1:30 p.m.—LUNCH
Rotunda of the University Museum

2:30 p.m. - 5:00 p.m.—SESSION IV
Auditorium of the University Museum

SESSION I

Thursday, 10 a.m. - 12:30 p.m.

Properties and Representation of Transistors

Chairman: H. L. Owens, *Evans Signal Laboratory, Belmar, N. J.*

Welcome, by Dr. G. P. Harnwell, President of the University of Pennsylvania, who will be introduced by Dr. I. Wolff, Director of Research, RCA Laboratories, and Chairman of the National Committee for this Conference.

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1. An Engineering View of Transistor Physics

J. M. Early, *Bell Telephone Laboratories, Murray Hill, N. J.*

The transmission circuit characteristics of junction transistor triodes depend on three electronic phenomena. These are: the diffusion of minority carriers through the base region, the depletion layer capacitances between the base and the other electrodes, and the ohmic base spreading resistance. The diffusion of minority carriers may be represented by admittances proportional to d-c currents. The diffusion transit time across the base region limits frequency response and appears either as the alpha cutoff frequency or as a time constant in the admittances. The collector capacitance shunts the output and by producing feedback from the collector electrode to the base region degrades high frequency response. The ohmic resistance between the base contact and the inter-electrode region acts as a feedback element or as a series loading element in reducing high frequency gain.

(about 10:45 a.m., Thursday)

2. A New Equivalent Circuit for Junction Transistors

J. Zawels, *RCA Victor Division, Camden, N. J.*

(Paper will be presented by H. Johnson)

A new equivalent circuit for a junction transistor is derived. It consists of two cascaded sections, one passive and one active. The passive section is mainly a transmission line which can be closely and simply approximated by lumped parameters. The active section is a frequency independent amplifier. A modification of the equivalent circuit especially suitable for common-emitter operation is shown. The common-emitter circuit uses the same elements as the common-base, with the addition of a current generator.

The basic equivalent circuit describes the diffusion equation and boundary condition as closely as they are formulated. The boundary conditions include the effect of base width modulation by the collector voltage.

Simple circuits explaining the h parameters are derived by inspection and experimental results are given.

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Thursday, 10 a.m. - 12:30 p.m.

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Simple circuits explaining the h parameters are derived by inspection and experimental results are given.

(about 11:15 a.m., Thursday)

3. Circuit Implications of Surface-Barrier Transistors

J. B. Angell, *Philco Corp., Philadelphia*

A description of the surface-barrier transistor, and the unique properties of its design which result in exceptionally good high-frequency performance, will open the discussion.

High-frequency equivalent circuits for representing the performance of these units over wide frequency ranges will be shown. These circuits are obtained by first isolating in the base lead the spreading resistance which exists in the bulk germanium between the active region and the tab. The active transistor is then represented by either the usual T-equivalent of three resistors, a frequency dependent current generator, and an output capacitance or a modified π-equivalent, also containing three resistors, a specially defined frequency-dependent current generator and an output capacitance. Comparisons of computed and measured gains will demonstrate that the π-equivalent gives a more accurate representation over a wide frequency range than does the T-equivalent, despite the fact both have the same number of independent parameters.

Data will be presented which show parameter values for surface-barrier transistors for both equivalent circuits. The tight control of tolerances on alpha cutoff frequency, base resistance, and collector capacitance will be illustrated together with a discussion of how this control of tolerances increases the interchangeability of the units in bandpass and video amplifiers.

The problem of measuring the high values of alpha cutoff frequency will be described, together with a description of a means for circumventing this problem

(about 11:45 a.m., Thursday)

4. The Variation of Junction Transistor Parameters with Operating Point and Temperature

J. S. Schaffner, *General Electric Co., Syracuse, N. Y.*

The change of the low frequency parameters of junction transistors with operating point and temperature is discussed in detail. Experimental results are presented together with the physical reasons for these changes. Specifically, the parameters discussed are the h-parameters of the grounded base stage (short circuit input resistance and current amplification, open circuit output resistance and voltage feedback ratio), the collector capacitance, I_{co} and the emitter base voltage. The results are given in the form of normalized curves.

END OF SESSION I

Lunch served in the Rotunda (upstairs) from 12:30 to 1:30

SESSION 2

Thursday, 2:30 p.m. - 5:00 p.m.

Junction Transistors in Linear Circuits

Chairman: J. G. Linvill, *Bell Telephone Laboratories, Murray Hill, N. J.*

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5. Transistor Circuits Utilizing Complementary Symmetry

G. C. Sziklai, *RCA Laboratories, Princeton, N. J.*

Circuits utilizing complementary symmetry are based on the two fundamental differences between pnp and npn junction or n and p type point contact transistors. First: with normal bias the current that flows in each electrode of one type unit is the negative of the corresponding electrode current of its complement. Second: the signal input that increases the conduction of one type unit, reduces the conduction of its complementary unit.

Circuits with complementary symmetry provide unique advantages for push-pull amplifiers, amplifier cascading, matrixing. Several of these type circuits will be described and analyzed.

(about 3 p.m., Thursday)

6. Compensation Techniques in Transistor Circuit Design

E. R. Kretzmer, *Bell Telephone Laboratories, Murray Hill, N. J.*

Transistors and other semiconductor devices have certain properties—notably temperature dependencies—which create circuit problems not encountered in vacuum tube circuits. Fortunately, in many semiconductor applications, there are techniques for minimizing these problems. In some cases, this may amount to using temperature-sensitive semiconductors as simple compensating elements. In other cases, certain properties of semiconductor junctions may be used to stabilize circuit operation, not only against temperature variations but other external influences as well. The basic principles involved are quite simple, but a high degree of stabilization sometimes requires a rather sophisticated combination of simple principles. The present paper discusses some of these principles and shows various circuits in which they have been successfully applied.

7. Neutralization of Transistor Bandpass Amplifiers

F. P. Keiper, Jr., *Philco Corp., Philadelphia*

This paper will discuss the utilization of surface-barrier and junction transistors in bandpass amplifier circuits.

The equivalent circuits useful in bandpass amplifier design will be presented and the difficulties encountered in the circuits will be demonstrated. These include input and output circuit tuning interaction, instability and oscillation.

A novel neutralizing circuit requiring but two additional components to form a bridge with r'_b and C_c as two arms to eliminate the aforementioned difficulties will be discussed and practical circuits presented. The previous equivalent circuit will be extended to include in one equivalent circuit the transistor and the neutralizing network and expressions will be derived for the terminal impedances and available gain of the neutralized transistor amplifier. These expressions will illustrate the relative importance of the various parameters of the transistor in this application.

8. Some Thoughts on Feedback in Transistor Circuits

S. J. Mason, *Research Laboratory of Electronics, M.I.T., Cambridge, Mass.*

A linear transistor model (or other linear two-terminal-pair device) is imbedded in a lossless passive network N and the properties of the complete system, as measured at two specified terminal pairs, are described by the open-circuit impedances Z_{11}, Z_{12}, Z_{21}, Z_{22}. The quantity

$$U = \frac{|Z_{21} - Z_{12}|^2}{4(R_{11}R_{22} - R_{12}R_{21})}$$

where R_{jk} is the real part of Z_{jk}, is defined as the unilateral gain of the transistor. Quantity U is independent of the choice of N and is (consequently) invariant under permutations of the three transistor terminals and also under replacement of the open-circuit impedances by short-circuit admittances. If U exceeds unity at a specified frequency, then N can always be chosen to make R_{11} and R_{22} positive and Z_{12} zero at that frequency. Quantity U is identifiable as the available power gain of the resulting unilateral structure.

An arbitrary coupling network may be decomposed into a portion which accomplishes unilateralization and a remaining complementary portion which provides feedback around the unilateralized structure. Such decomposition brings some of the methods of elementary feedback theory to bear upon nonunilateral circuit problems and offers a viewpoint from which signal flow and power flow can be simply related.

(about 4:20 p.m., Thursday)

9. On Certain Aspects of Noise in Transistor Circuits

P. L. Bargellini, *Moore School of Electrical Engineering, University of Pennsylvania, Philadelphia, and RCA Victor Division, Camden, N. J.*

After a review of the classical methods for the analysis of noise encountered in transistor circuits the noise reduction gained when using junction instead of point contact units is examined from a quantitative viewpoint based on preliminary experimental investigations.

The dependence of noise output and/or noise figure from various parameters or conditions such as d-c components of voltage and current in the input and output circuits, generator and load resistances, aging, humidity, etc., is presented. The role of statistical correlation between input and output noise generators is reviewed.

Further extensive measurements of noise in modern junction transistor amplifiers operating in the frequency range from 10^2 to 10^7 cps. have disclosed in the case of low noise units considerable departure from the "1/f" law generally accepted without too much questioning in the past.

"Flat" noise spectra of quiet transistors are presented and the lower limits of noise are indicated to reside in some form of equivalent shot and thermal noise effects.

An attempt to explain the eventual increase of noise figure at either end of the spectrum is presented in terms of the fluctuations of the hole current in the emitter-to-collector space and respectively the reduction of the gain at high frequencies.

Further advances in the understanding of the physical phenomena at the base of transistor noise will certainly result in a more uniform production of low noise units, but engineers should realize that presently available not critically selected junction transistors already offer definite advantages for certain low noise applications with respect to vacuum tubes because of the absence of spurious noise effects such as hum, microphonics, etc., and of the easier matching to low impedance sources.

END OF SESSION II

Cocktail-Buffet at the Penn-Sherwood Hotel, 6-7:30 p.m.

SESSION III

Friday, 9:30 a.m. - 12:30 p.m.

Junction Transistor Amplifiers

Chairman: T. R. Finch, *Bell Telephone Laboratories, Murray Hill, N. J.*

10. Transistor D-C Amplifiers

C. R. Hurtig, *Research Laboratory of Electronics, M.I.T., Cambridge, Mass.*

The use of direct-coupled transistor stages results in poor dynamic range due to the temperature sensitivity of the saturation current (I_{co}). Experimental results of the temperature dependence of the saturation current are given. Two methods of compensating the saturation currents by employing auxiliary transistors are given. Due to variation in transistor parameters, perfect compensation cannot be achieved over wide temperature ranges. The dynamic range obtainable with compensated stages depends upon the temperature range over which the amplifier is required to operate. A nomograph is presented that permits determination of the dynamic range for any temperature range if the drift signal at the input to the amplifier is known at room temperature.

To increase the dynamic range of transistor amplifiers, several different methods may be employed. A zero correcting device as described in a separate paper may be employed. Temperature control by means of miniature refrigerators may be used. Or a modulate-demodulate technique may be satisfactory

(about 10 a.m., Friday)

11. Summing and Integrating Amplifiers

F. H. Blecher, *Bell Telephone Laboratories, Murray Hill, N. J.*

One of the basic active circuits used in analogue systems and analogue-to-digital converters is a direct coupled amplifier. The amplifier is usually employed for summing a multiplicity of input voltages or as an integrator. This paper describes such an amplifier using NPN and PNP junction transistors.

The direct coupled amplifier is capable of summing input voltages to an accuracy of at least one part in 10,000. The maximum available output voltage, limited by transistor collector voltage restrictions, is ± 25 volts. The amplifier has 86 db of negative feedback at DC with a descending asymptote of approximately 6 db per octave. This results in an optimum transient performance which permits full accuracy to be attained in less than a millisecond. By the use of a DC-drift compensating circuit composed of a mechanical chopper and an auxiliary transistor AC amplifier, the accuracy of the direct coupled amplifier is maintained throughout the temperature range of 0 to 120 degrees Fahrenheit.

The paper places particular emphasis on the problem of stabilizing the negative feedback and providing satisfactory gain and phase margins against instability. The paper also considers the critical transistor parameters which limit the accuracy and rise time of the amplifier, and the improvements to be expected in the near future.

(about 10:30 a.m., Friday)

12. Transistor Power Amplifiers

R. F. Shea, *General Electric Company, Syracuse, N. Y.*

Graphical methods of analysis are presented for both Class A and Class B transistor power amplifiers. From this analysis the equations are derived for power output, load resistance, power gain, input resistance, efficiency and power dissipation. The analysis is made for all three configurations, grounded-base, grounded-emitter and grounded-collector

The effect of temperature is discussed and methods are described for the design of power amplifiers to operate over wide temperature ranges.

The effect of generator resistance on distortion is also described and means derived for determining the optimum value. In particular the problem of distortion inherent in Class B amplifiers is treated in considerable detail.

Complementary combinations are also described.

(about 11 a.m., Friday)

13. A Carrier Frequency Feedback Amplifier

R. E. Yaeger, *Bell Telephone Laboratories, Murray Hill, N. J.*

Application of feedback to multi-stage transistor amplifiers presents problems which, though not necessarily new, often may be disregarded in vacuum tube circuits. These problems include bilateral transmission with its interrelated input and output impedance effects in the transistor circuit. In addition, the frequency cutoff of alpha increases the difficulty in controlling mu-beta phase and gain in carrier amplifiers.

These problems are discussed in relation to the design of a two stage common-collector to common-emitter amplifier for the carrier frequency range of 8-100 kilocycles. A description of the circuit and performance is given. Input and output impedance are stabilized by bridge feedback of the hybrid coil type. With a net gain with feedback of 25 db, second and third harmonics are down more than 40 db and 60 db, respectively, for an output level of +6 dbm.

(about 11:30 a.m., Friday)

14. Junction Tetrode I.F. Amplifiers

L. G. Schimpf, *Bell Telephone Laboratories, Murray Hill, N. J.*

The use of junction tetrode transistors in I.F. amplifiers will be discussed. A brief review of some of the factors which limit the use of junction transistors at high frequencies will be given. One of these parameters which is quite important is the value of the base resistance. It will be demonstrated that the value of this resistance can be reduced from about 1000 ohms for a triode connected transistor, to about 50 ohms for the same transistor connected as a tetrode. This reduction in the value of base resistance, is sufficient to increase the frequency at which the gain is 3 db down in a resistance coupled amplifier by a factor of ten.

Several specific applications of junction tetrode transistors to band pass amplifiers will be given. The circuit and performance data of an amplifier with 22 db gain, flat to ±0.1 db from 0.4 to 11 mc will be shown. This amplifier uses a transistor with an alpha cutoff frequency of about 60 mc. An amplifier which passes about 200 kc at a center frequency of 10.7 mc will also be discussed. In this application a gain of about 20 db per stage can be obtained with transistors having an alpha cutoff frequency of about 40 mc. This amplifier uses the transistor in the common emitter connection with a collector voltage of about 5 volts.

The final example will show an amplifier centered at 70 mc with a 20 mc pass band. Using the common base connection, three stages result in a gain of 27 db, flat to within ±0.2 db over the 20 mc pass band. A number of units have been measured in this amplifier for both gain and noise figure. About two-thirds of them had a gain of 8 db or greater and a noise figure of 12 db or less. The frequency of alpha cutoff for these units varies from about 40 mc to 70 or 80 mc.

END OF SESSION III

Lunch served in the Rotunda (upstairs) from 12:30 to 1:30.

SESSION IV

Friday, 2:30 p.m. - 5 p.m.

Nonlinear Applications of Junction Transistors

Chairman: A. W. Lo, *RCA Laboratories, Princeton, N. J.*

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15. Large-Signal D-C Behavior of Junction Transistors

J. J. Ebers and J. L. Moll, *Bell Telephone Laboratories, Murray Hill, N. J.*

The d-c behavior of junction transistors when operated in large-signal applications, notable among which is switching, has been found to be expressible in analytic form, making possible quantitative design of large-signal circuits. Junction transistors, when operated as a switch, can perform many functions, some of which cannot be done by any other known electronic device. Junction transistors can be designed to have the characteristics required by specific switching applications. These factors, circuit designability, versatility, and device designability, make junction transistors particularly appealing for large-signal applications.

Even for the most generalized junction transistor in which practically no restrictions are placed upon the geometry, the d-c behavior in all regions of operation is given by the equations

$$I_E = a_{11} [\exp (q\varphi_E/kT) - 1] + a_{12} [\exp (q\varphi_C/kT - 1]$$

$$I_C = a_{21} [\exp (q\varphi_E/kT) - 1] + a_{22} [\exp (q\varphi_C/kT - 1],$$

where φ_E and φ_C are the junction potentials. Thus the transistor can be considered as a two-terminal-pair network and the behavior is specified by measurement of the a's. It has been shown that even for the most general cases $a_{12} = a_{21}$, which means that in the large-signal sense, junction transistors are bilateral. It can be shown that the a's are related to the two reverse saturation currents of the junctions and the two current gains or alphas (the normal alpha and the inverted alpha). Because of the bilateralism, only three of these quantities completely specify the a's.

The equations given above lead to equivalent circuits which are applicable in each region of operation. To take into account departures from the ideal transistor, additional circuit elements can be added to the equivalent circuit.

Measurements taken on transistors having various geometries show that the equations and equivalent circuits which have been formulated accurately describe the large signal behavior. Circuit examples have been worked out which demonstrate the utility of the theory.

(about 3 p.m., Friday)

16. Large-Signal Transient Behavior of Junction Transistors

J. L. Moll, *Bell Telephone Laboratories, Murray Hill, N. J.*

The large-signal transient behavior of junction transistors is presented in terms of equivalent circuits applicable to each region of operation. When the transistor operating point is in the active region, the equivalent circuit parameters change slowly with operating point. The part of the transient which corresponds to operation in the active region can therefore be analyzed by using the conventional equivalent circuit and standard methods of circuit analysis.

The transient behavior in the current saturation region can be described by adding several new circuit elements to the equivalent circuit. Particular attention is given to the transition between the active region and the current saturation region. A method is given for calculating the time when the transition occurs. Theoretical expressions are given for the times of transition into and out of the current saturation region for step function driving currents.

Equivalent circuit parameters of primary importance in determining the transition times are α_N, ω_N, α_I, and ω_I. The subscripts N refer to nomal active-region equivalent circuit parameters and the subscripts I refer to active-region equivalent circuit parameters with emitter and collector interchanged.

17. Junction Transistor Switching Characteristics

D. E. Deuitch, *RCA Victor Division, Camden, N. J.*

This paper includes four topics: (a) the switching properties and d-c characteristics of the junction transistor; (b) a general transient analysis of the junction transistor; (c) a qualitative description of the physical action involved in the storage phenomena; and (d) switching circuit applications.

(a) The cutoff and saturation impedance properties of the junction transistor are described, and the Zener voltage and α fall-off limitations are discussed briefly. Expressions for switching speed are presented. The problem of collector leakage current in grounded emitter operation is reviewed and two solutions to this problem are presented.

(b) The discussion of transient analysis is designed primarily to point out the principal factors limiting the transient response of the junction transistor in grounded base, grounded emitter and grounded collector operation.

A "T" equivalent circuit is introduced together with a brief description of parameters in this circuit. Expressions for the response of this circuit to an input step, together with calculated and measured response curves, are presented for the three aforementioned types of operation. Very close agreement between calculated and measured responses is shown.

Graphs of collector voltage rise time vs. collector load for an input step in grounded emitter and grounded base operation and emitter voltage rise time vs. base resistance in ground collector operation are shown, illustrating clearly the factors limiting circuit transient response.

(c) The storage phenomena in junction transistors is interpreted in terms of minority carrier charge density in the base region. Variation in storage with input current and saturation collector current are shown graphically, pointing out the salient properties and limitations of the storage conditions.

(d) Several types of switching circuits are presented. These include gating circuits for both grounded-base and grounded-emitter stages, a memory circuit and an integrator circuit (both utilizing the properties of the minority carrier charge storage), and two bistable circuits capable of operation at 400 Kc.

The important switching properties of the junction transistor are emphasized and special consideration is given to the problems brought about by storage and collector leakage current.

18. Junction Transistor Switching Circuits

J. T. Warnock, *Philco Corporation, Philadelphia, Pa.*

This paper discusses the design techniques which have been used successfully to provide junction transistor switching circuits of very high reliability.

These switching circuits will operate satisfactorily within the low and medium frequency range of from 0 to 150 kilocycles when alloy-junction transistors of the type currently available are used.

Since the flip-flop, or Eccles-Jordan circuit, is perhaps the most important of the common switching circuits, the greater portion of this paper is devoted to its design and operation. The other switching circuits which are discussed include pulse inverters, various types of multiple gates, and direct-coupled amplifiers.

The effect of saturation in switching circuits is very serious since it will cause considerable delay and therefore reduce the maximum switching rate attainable. A simple method of preventing saturation using a germanium diode is incorporated in each of the circuits presented. This system does not affect the circuit output voltage or the trigger sensitivity, but limits the base input current to a value slightly below the saturation point.

The circuits presented in this paper will operate with transistors having an alpha variation of from 0.93 to 1.00 and a collector cutoff current ranging from 0 to 100 microamperes. Reliable operation has been obtained at ambient temperatures as high as 65 degrees Centigrade.

Experimental work is in progress at the present time on the application of the surface barrier transistor to high frequency switching circuits. Although this work is far from complete, flip-flop circuits have been built with rise times of less than one-tenth of a microsecond. These results show that the surface barrier transistor may extend the maximum switching rate of transistor switching circuits to a value suitable for extensive use in computers and similar devices.

END OF SESSION IV

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