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Baker

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(54) **MEMORY WITH CORRELATED RESISTANCE**

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This patent is subject to a terminal disclaimer.

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Related U.S. Application Data

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G11C 16/04 (2006.01)

(52) **U.S. Cl.**
USPC **365/185.17**; 365/185.09; 365/185.29; 365/230.03

(58) **Field of Classification Search**
USPC 365/185.17, 185.09, 185.29, 230.03
See application file for complete search history.

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(57) **ABSTRACT**

Methods, systems, and devices include a system for sequentially writing to a data locations coupled to one another in series. The system includes a plurality of data locations and a controller. The controller is configured to sequentially write data values to the plurality of data locations, starting with the data location at an end of the series and then sequentially writing to each adjacent data location.

20 Claims, 16 Drawing Sheets
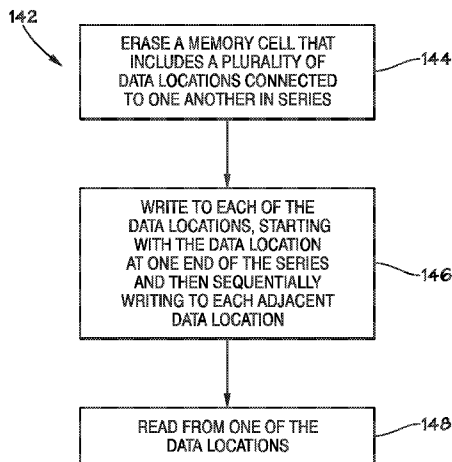
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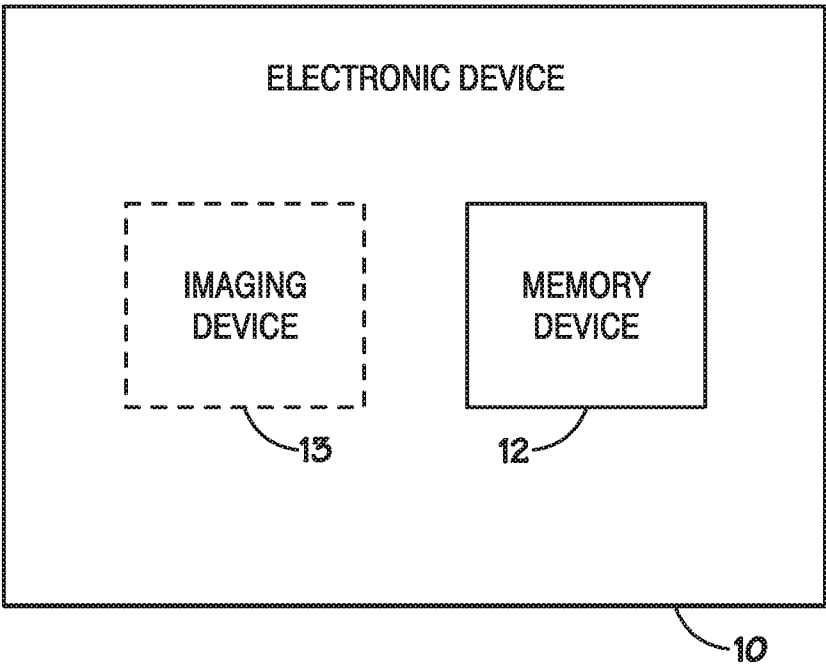
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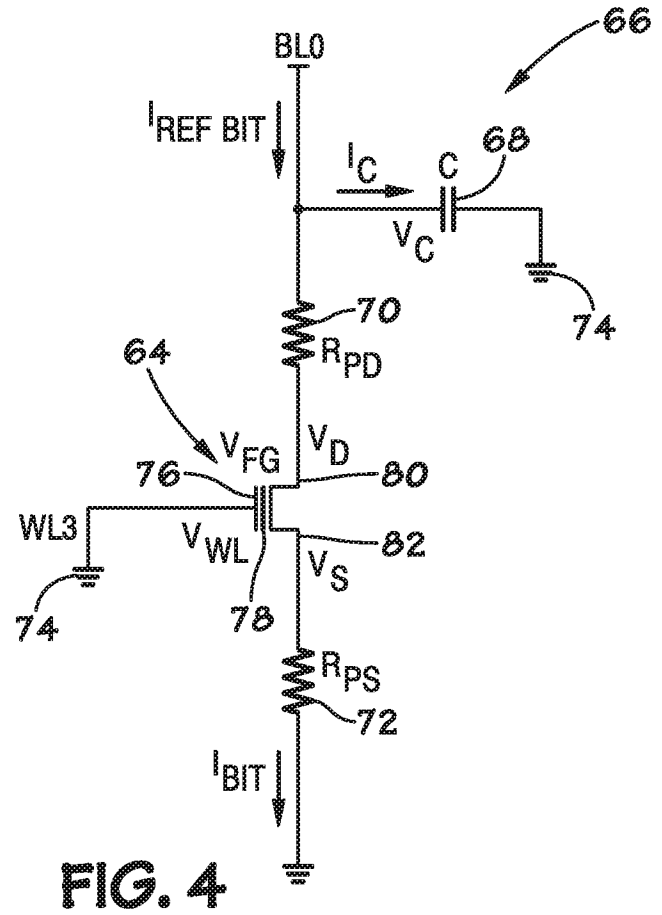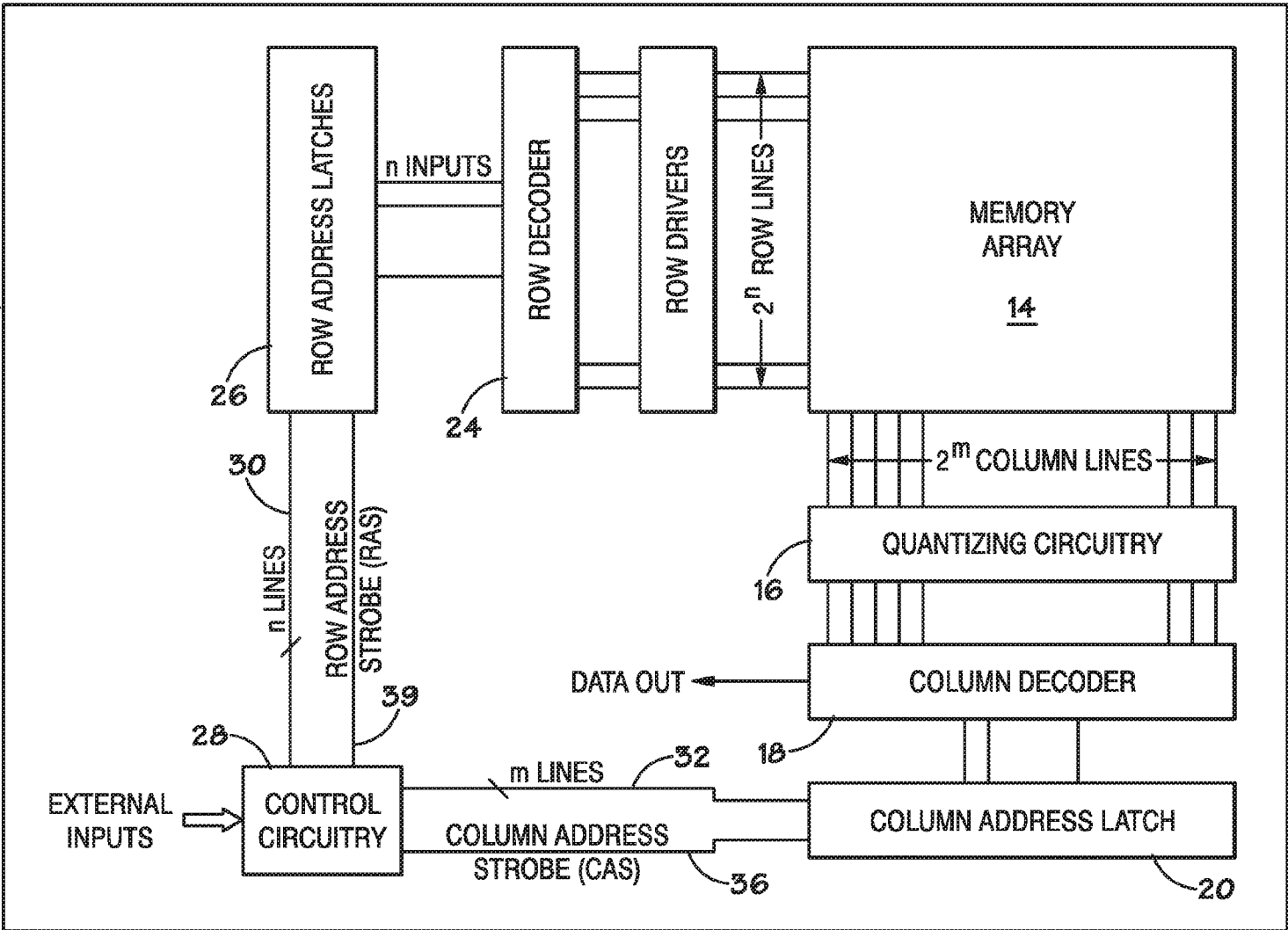ELECTRONIC DEVICE

IMAGING
DEVICE

MEMORY
DEVICE

13

12

10

FIG. 1

BL0

$I_{REF\ BIT}$

I_C C   68

V_C

66

74

70   R_{PD}

64

V_{FG} V_D

76   80

WL3 V_{WL} V_S 82

74   78

R_{PS}

72

I_{BIT}

FIG. 4

FIG. 2

FIG. 3

FIG. 5

BIT LINE CURRENT (I_{BIT})

$V_{FG} = 0x$
DATA = 000

$V_{FG} = -1x$
DATA = 001

$V_{FG} = -2x$
DATA = 010

$V_{FG} = -3x$
DATA = 011

$V_{FG} = -4x$
DATA = 100

$V_{FG} = -5x$
DATA = 101

$V_{FG} = -6x$
DATA = 110

$V_{FG} = -7x$
DATA = 111

WORD LINE VOLTAGE (V_{WL})
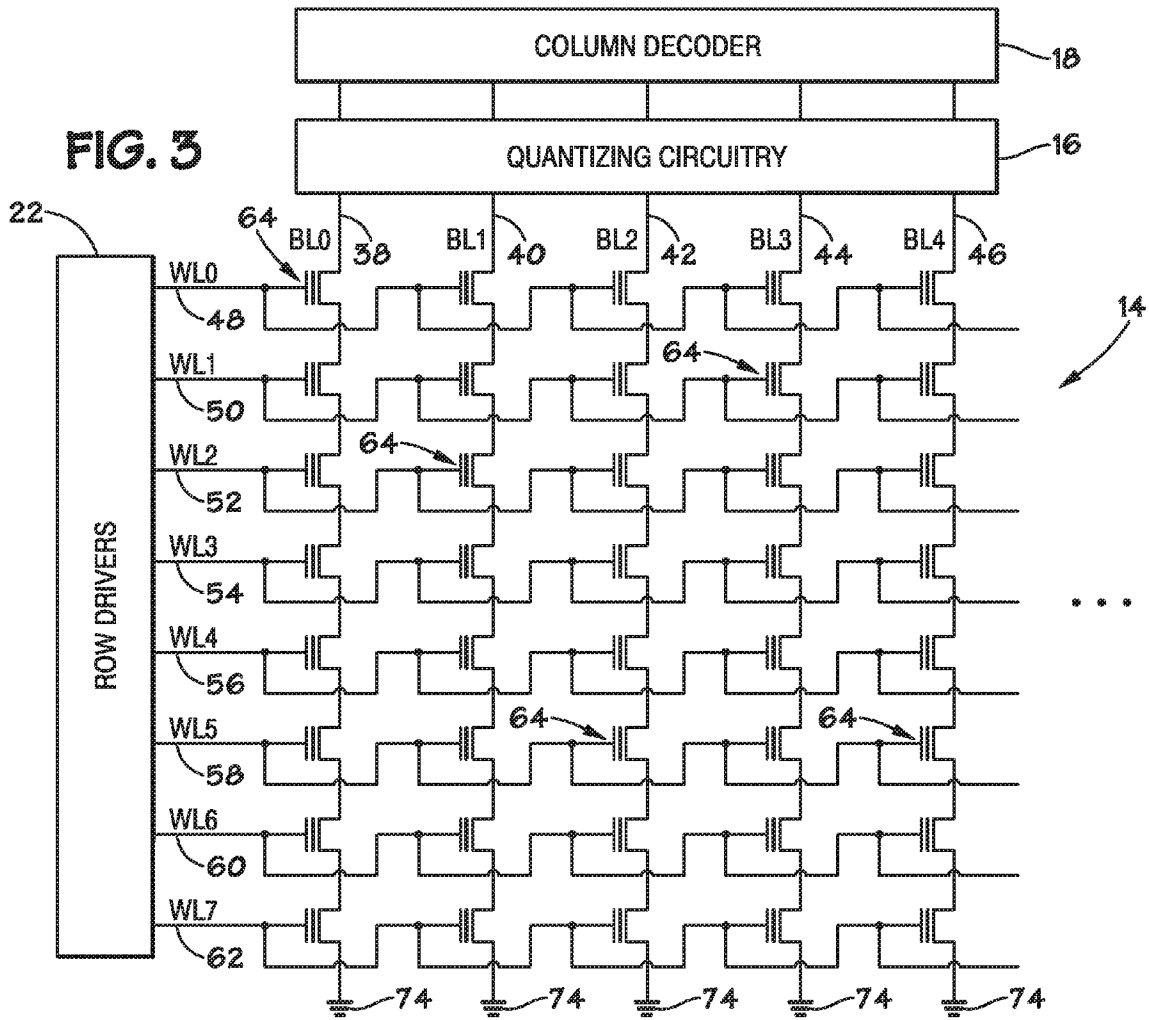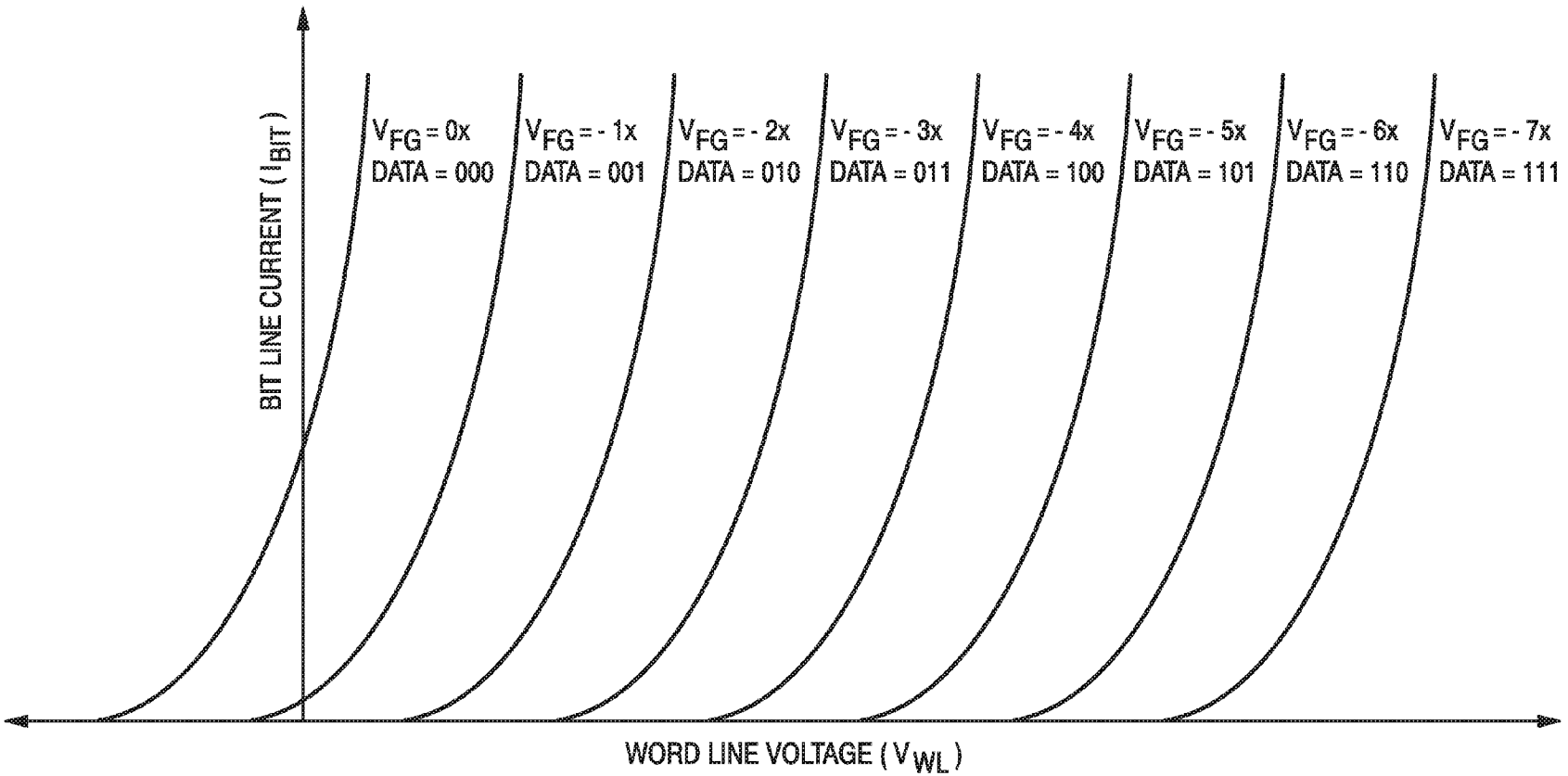
FIG. 6
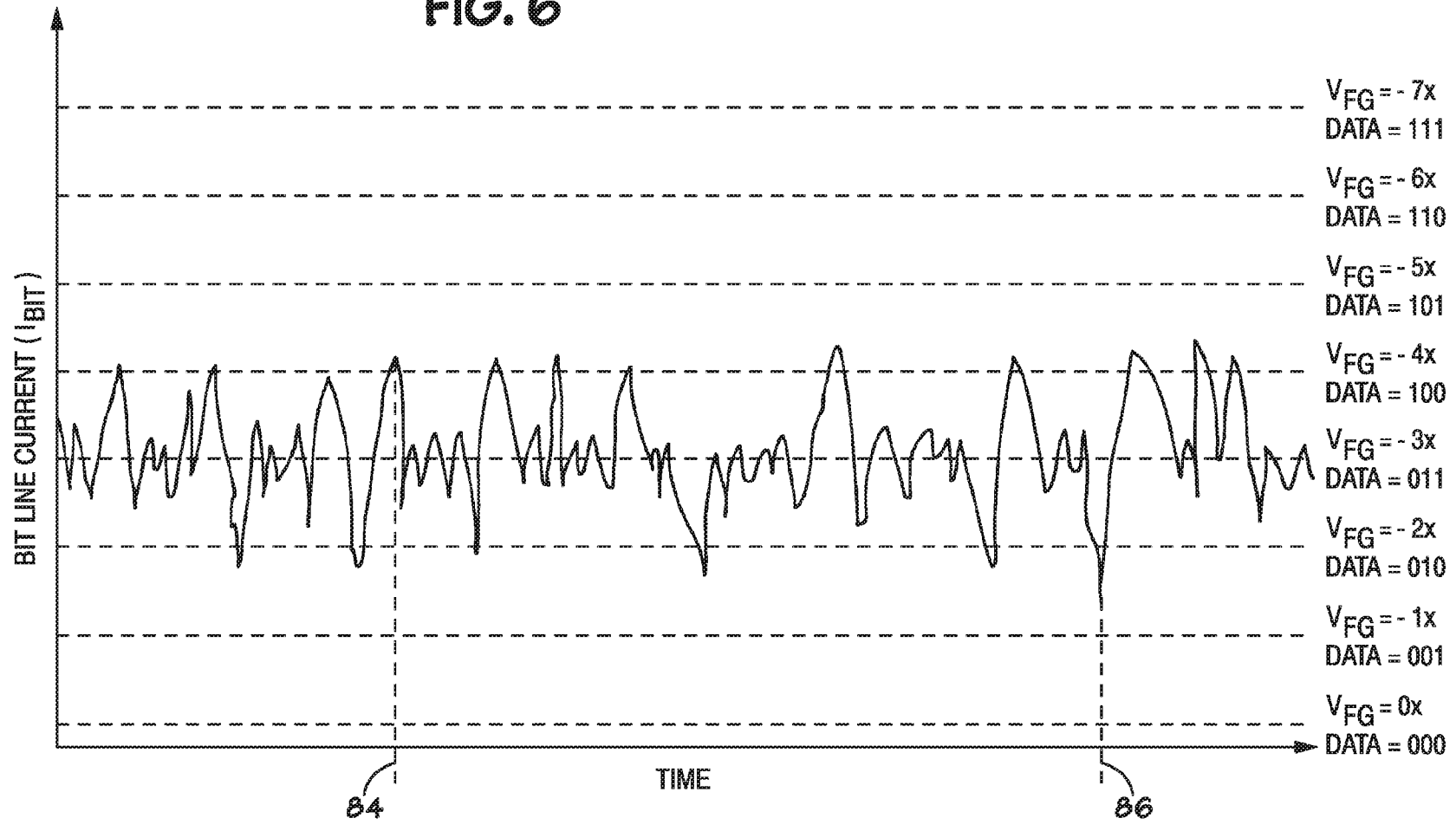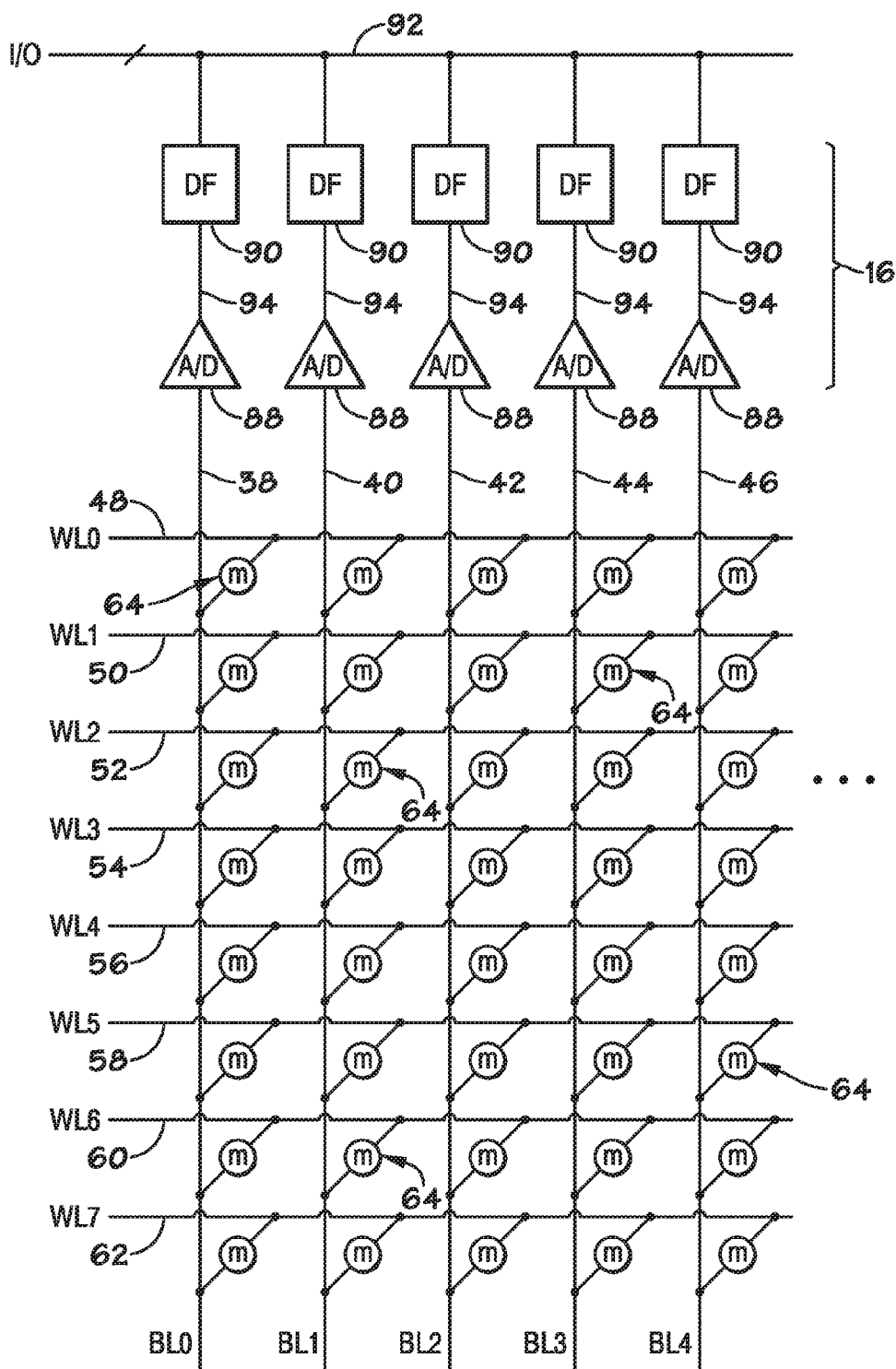
FIG. 7
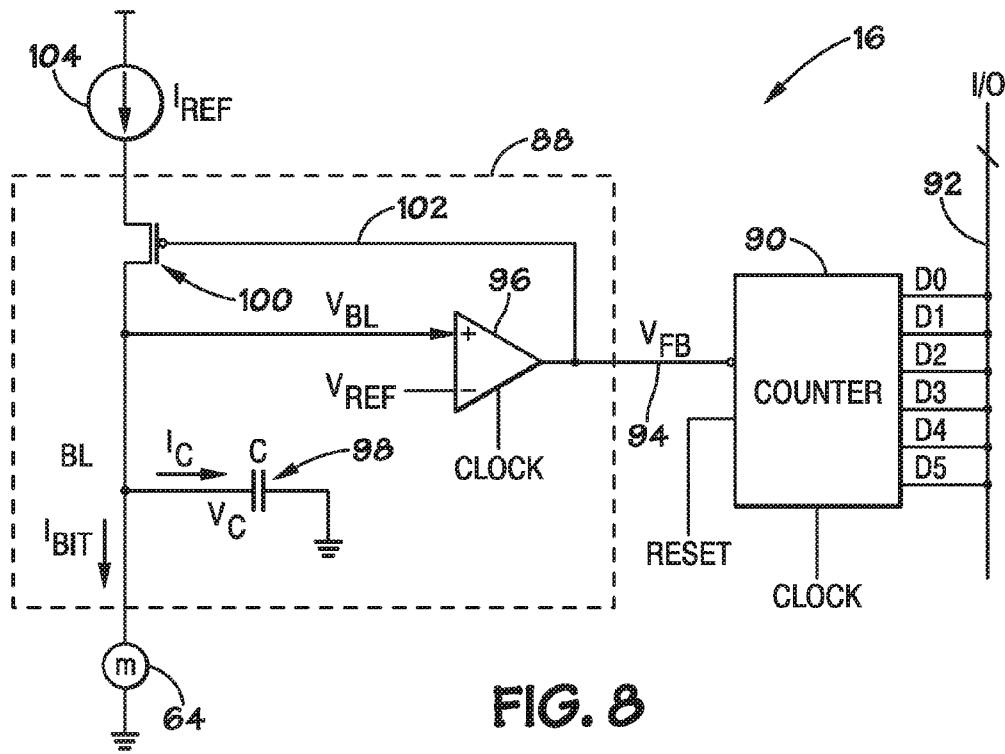
FIG. 8

FIG. 9

FIG. 10

FIG. 11

FIG. 12

FIG. 13

FIG. 14

FIG. 15

FIG. 16

FIG. 17

140

QUANTIZING_
CIRCUITRY

R_{D2}

BIT-LINE

R_{D1} R_D

R_{D0}

WL2 —   128

V_{GS}

R_{S5}

R_{S4}

R_{S3}

R_S

R_{S2}

I_{CDL}

R_{S1}

R_{S0}

142

ERASE A MEMORY CELL THAT
INCLUDES A PLURALITY OF
DATA LOCATIONS CONNECTED
TO ONE ANOTHER IN SERIES — 144

WRITE TO EACH OF THE
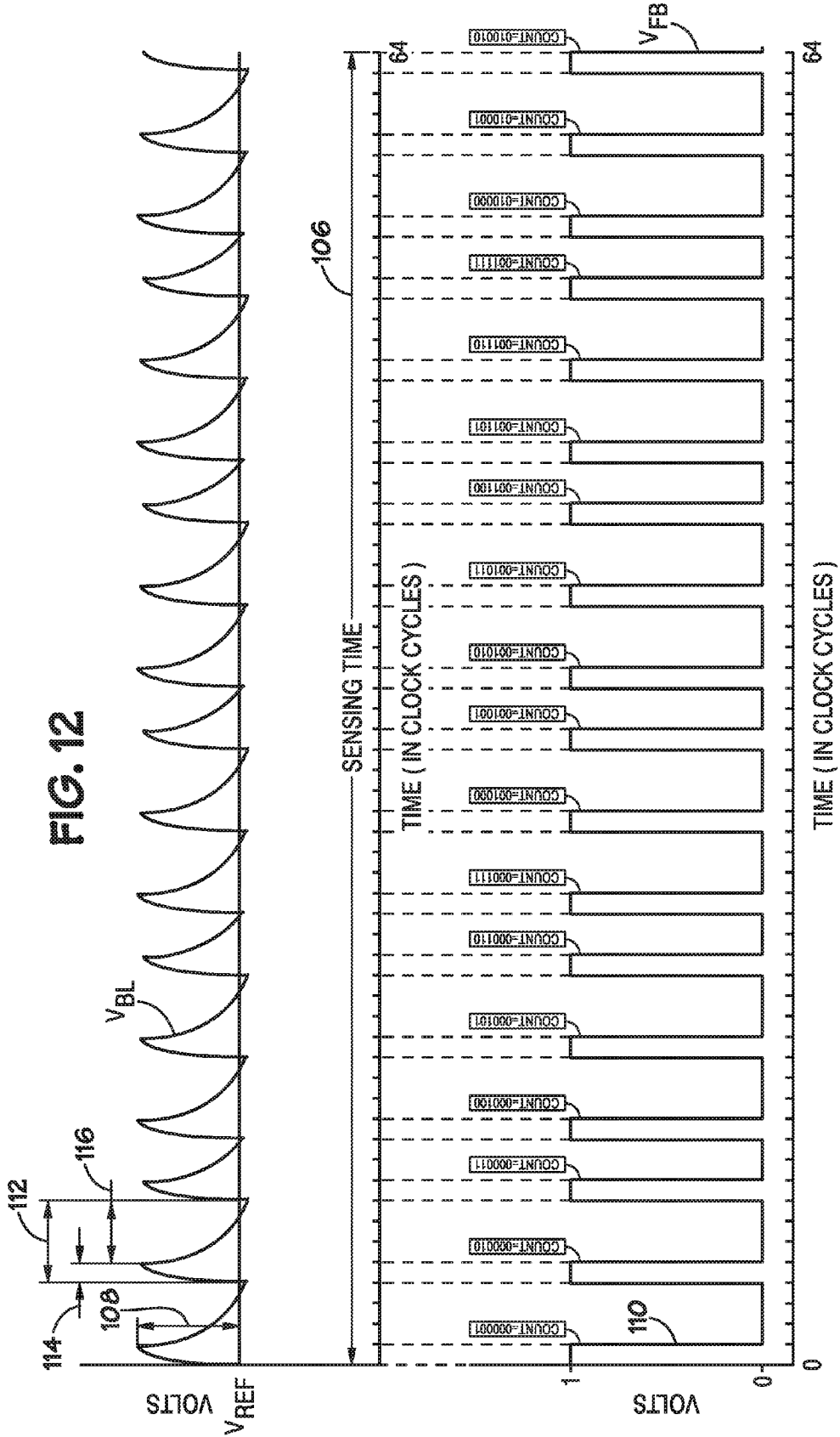DATA LOCATIONS, STARTING
WITH THE DATA LOCATION
AT ONE END OF THE SERIES
AND THEN SEQUENTIALLY
WRITING TO EACH ADJACENT
DATA LOCATION — 146

READ FROM ONE OF THE
DATA LOCATIONS — 148

FIG. 18

318

DISPLAY

310

312

320

RF SUBSYSTEM /
BASEBAND
PROCESSING

PROCESSOR

MEMORY
DEVICE

12

VOLATILE MEMORY
- DYNAMIC RAM
- STATIC RAM

326

COMMUNICATION
PORT

POWER

INPUT DEVICE
- KEYBOARD
- DIGITIZER

316

322

314

324

PERIPHERAL

FIG. 19

MEMORY WITH CORRELATED RESISTANCE

CROSS-REFERENCE TO RELATED APPLICATION

This application is a continuation of U.S. patent application Ser. No. 12/817,034, which was filed on Jun. 16, 2010 and issued as U.S. Pat. No. 8,289,772 on Oct. 16, 2012, which is a divisional of U.S. paten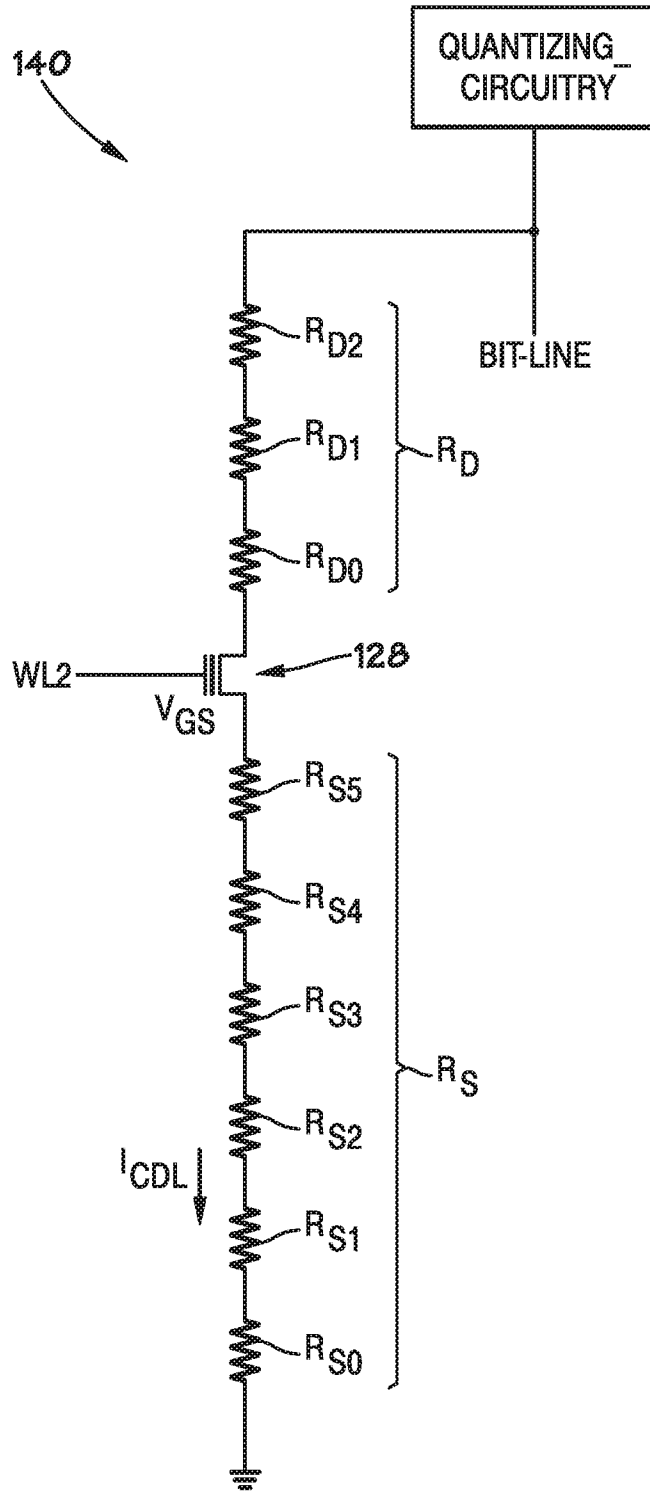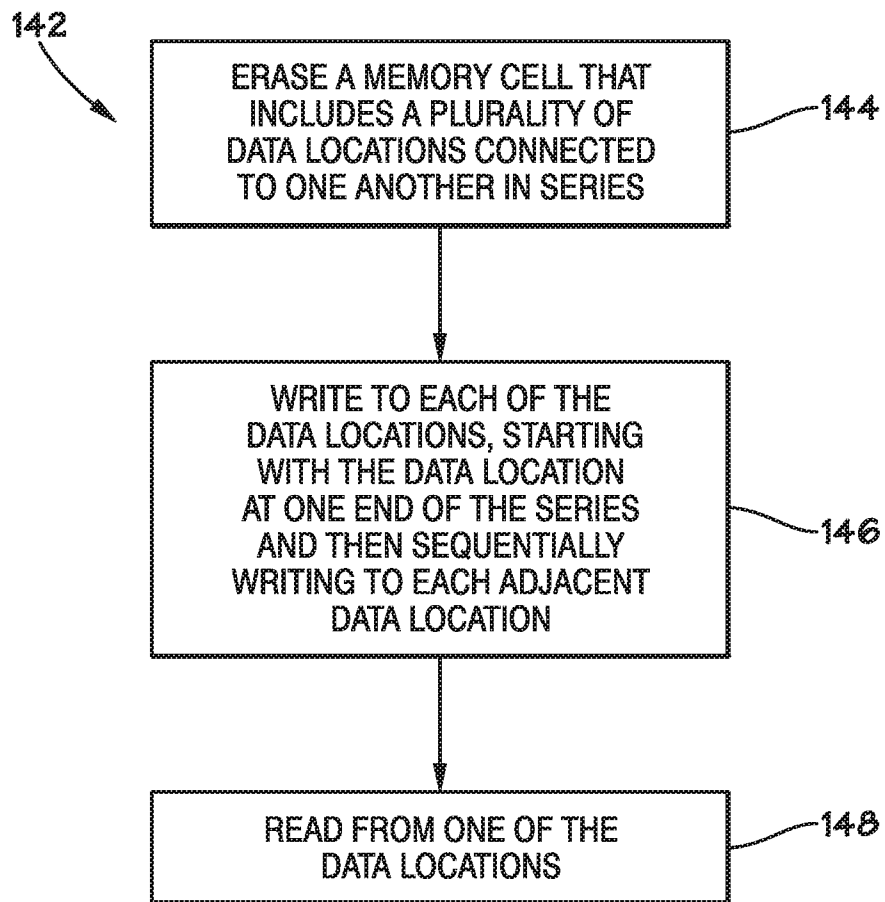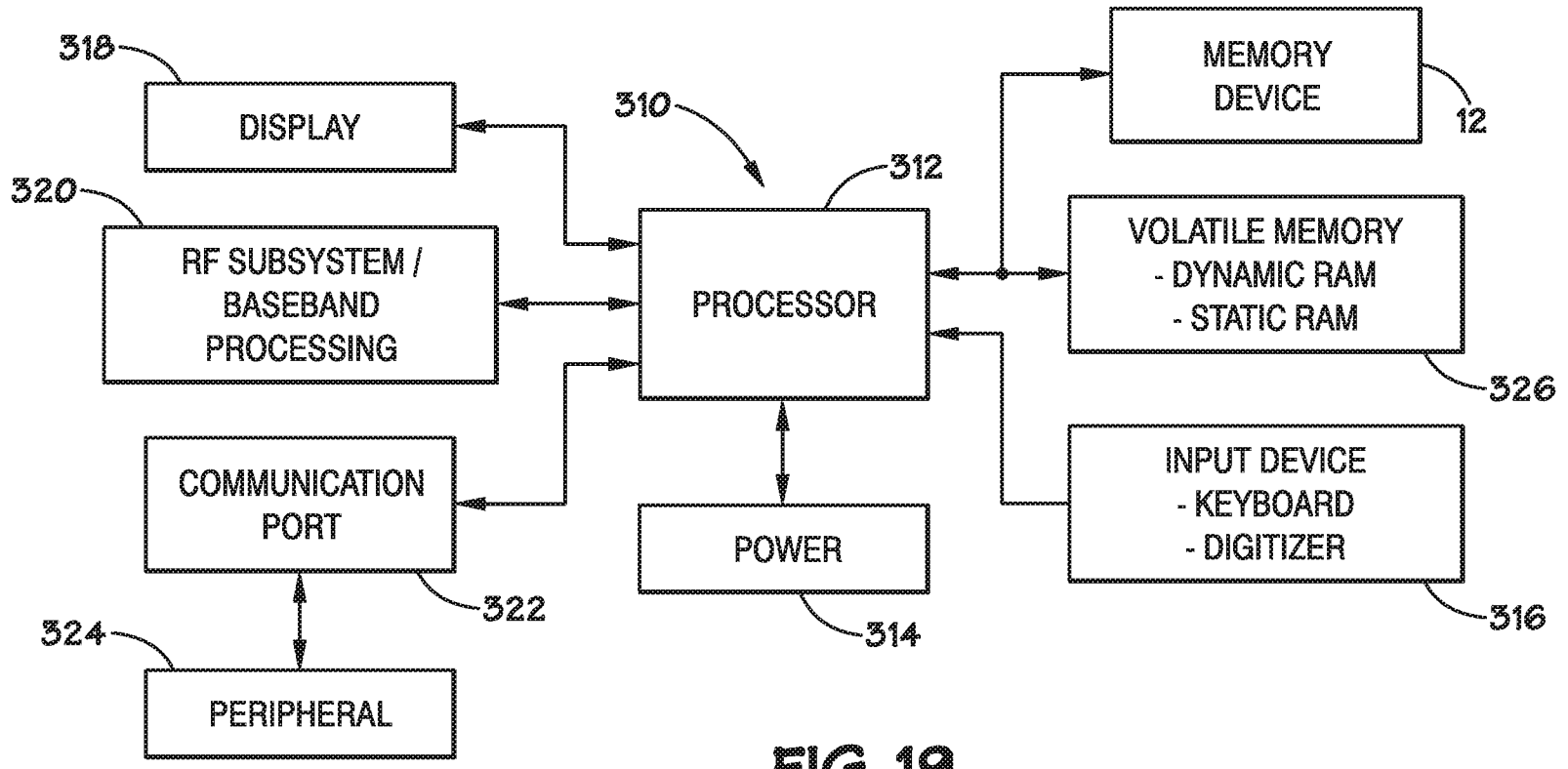t application Ser. No. 11/818,983, which was filed on Jun. 15, 2007, now U.S. Pat. No. 7,969,783, which issued on Jun. 28, 2011.

BACKGROUND

1. Field of Invention

Embodiments of the present invention relate generally to memory devices and, more specifically, in one embodiment, to memory devices with resistance that is correlated between read operations and write operations.

2. Description of Related Art

Generally, memory devices include an array of memory elements and associated sense amplifiers. The memory elements store data, and the sense amplifiers read the data from the memory elements. To read data, for example, a current is passed through the memory element, and the current or a resulting voltage is measured by the sense amplifier. Conventionally, the sense amplifier measures the current or voltage by comparing it to a reference current or voltage. Depending on whether the current or voltage is greater than the reference, the sense amplifier outputs a value of one or zero. That is, the sense amplifier quantizes (e.g., digitizes) the analog signal from the memory element into one of two logic states.

Many types of memory elements are capable of assuming more than just two states. For example, some memory elements are capable of multi-bit (e.g., more than two state) storage. For instance, rather than outputting either a high or low voltage, the memory element may output four or eight different voltage levels, each level corresponding to a different data value. However, conventional sense amplifiers often fail to distinguish accurately between the additional levels because the difference between the levels (e.g., a voltage difference) in a multi-bit memory element is often smaller than the difference between the levels in a single-bit (i.e., two state) memory element. Thus, conventional sense amplifiers often cannot read multi-bit memory elements. This problem may be increased as high performance multi-bit memory elements become increasingly dense, thereby reducing the size of the memory elements and the difference between the levels (e.g., voltage) to be sensed by the sense amplifiers.

A variety of factors may tend to prevent the sense amplifier from discerning small differences in the levels of a multi-bit memory element. For instance, noise in the power supply, ground, and reference voltage may cause an inaccurate reading of the memory element. The noise may have a variety of sources, such as temperature variations, parasitic signals, data dependent effects, and manufacturing process variations. This susceptibility to noise often leads a designer to reduce the number of readable states of the memory element, which tends to reduce memory density and increase the cost of memory.

Another source of noise is changing conditions in circuitry related to a memory element. For example, changing conditions in other memory elements that share a bit-line with the memory element may interfere with data storage. The data stored by these other memory elements may change between a write operation and a read operation, and the value of the

data stored by the other memory elements may affect the electrical properties of the circuit including the bit-line and the memory element at issue. For instance, in some devices, the total resistance of this circuit is related to the data that the other memory elements store. Consequently, in some devices, the memory element being read may appear to store a different value than was written because the data stored by other memory elements has changed.

BRIEF DESCRIPTION OF DRAWINGS

FIG. 1 illustrates an electronic device in accordance with an embodiment of the present invention;

FIG. 2 illustrates a memory device in accordance with an embodiment of the present invention;

FIG. 3 illustrates a memory array in accordance with an embodiment of the present invention;

FIG. 4 illustrates a memory element in accordance with an embodiment of the present invention;

FIG. 5 illustrates I-V traces of memory elements storing different values, in accordance with an embodiment of the present invention;

FIG. 6 illustrates noise in the bit-line current during a read operation;

FIG. 7 illustrates a quantizing circuit in accordance with an embodiment of the present invention;

FIG. 8 illustrates a delta-sigma sensing circuit in accordance with an embodiment of the present invention;

FIGS. 9 and 10 illustrate current flow during operation of the quantizing circuit of FIG. 8;

FIGS. 11-13 illustrate voltages in the quantizing circuit of FIG. 8 when sensing small, medium, and large currents, respectively;

FIG. 14 is a graph of bit-line current versus counter output for the quantizing circuit of FIG. 8;

FIG. 15 is a graph of count versus quantizing circuit output in accordance with an embodiment of the present invention;

FIG. 16 illustrates a memory cell in accordance with an embodiment of the present invention;

FIG. 17 illustrates a circuit that models the operation of the memory cell of FIG. 16 in accordance with an embodiment of the present invention;

FIG. 18 illustrates a process for correlating certain resistance values of the memory cell of FIG. 16 in accordance with an embodiment of the present invention; and

FIG. 19. illustrates an example of a system that includes the electronic device of FIG. 2.

DETAILED DESCRIPTION OF SPECIFIC EMBODIMENTS

Various embodiments of the present invention are described below. In an effort to provide a concise description of these embodiments, not all features of an actual implementation are described in the specification. It should be appreciated that in the development of any such actual implementation, as in any engineering or design project, numerous implementation-specific decisions must be made to achieve the developers' specific goals, such as compliance with system-related and business-related constraints, which may vary from one implementation to another. Moreover, it should be appreciated that such a development effort might be complex and time consuming but would nevertheless be a routine undertaking of design, fabrication, and manufacture for those of ordinary skill having the benefit of this disclosure.

Some of the subsequently described embodiments may address one or more of the problems with conventional sense

amplifiers discussed above. Some embodiments include a quantizing circuit configured to detect small differences in voltages and/or currents. As explained below, the quantizing circuit may sample the measured electrical parameter on multiple occasions and filter, e.g., average or sum, the samples to reduce the impact of noise. As a result, in some embodiments, the quantizing circuit may resolve small differences between voltage or current levels in multi-bit memory elements and/or light sensors, which may allow circuit designers to increase the number of bits stored per memory element and/or the sensitivity of an imaging device.

After describing examples of quantizing circuits, a process for correlating resistance is discussed. This process may be employed in combination with the quantizing circuits or it may be employed with other types of sensing circuits. As described below, the process for correlating resistance is believed to reduce noise from changing resistance in other memory elements, so the value written to a memory element can later be retrieved regardless of changes to surrounding memory elements. Prior to describing this process, systems that might benefit from its use are described.

FIG. 1 depicts an electronic device 10 that may be fabricated and configured in accordance with one or more of the present embodiments. The illustrated electronic device 10 includes a memory device 12 that, as explained further below, may include multi-bit memory elements and quantizing circuits. Alternatively, or additionally, the electronic device 10 may include an imaging device 13 having the quantizing circuits.

Myriad devices may embody one or more of the present techniques. For example, the electronic device 10 may be a storage device, a communications device, an entertainment device, an imaging system, or a computer system, such as a personal computer, a server, a mainframe, a tablet computer, a palm-top computer, or a laptop.

FIG. 2 depicts a block diagram of an embodiment of the memory device 12. The illustrated memory device 12 may include a memory array 14, a quantizing circuit 16, a column decoder 18, a column address latch 20, row drivers 22, a row decoder 24, row address latches 26, and control circuitry 28. As described below with reference to FIG. 3, the memory array 14 may include a matrix of memory elements arranged in rows and columns. As will be appreciated, the imaging device 13 (FIG. 1) may include similar features except that in the case of an imaging device 13, the array 14 might comprise an array of imaging elements, such as complementary-metal-oxide semiconductor (CMOS) imaging elements or charge coupled devices (CCDs).

When accessing the memory elements, the control circuitry may receive a command to read from or write to a target memory address. The control circuitry 28 (i.e., "controller") may then convert the target address into a row address and a column address. In the illustrated embodiment, the row address bus 30 transmits the row address to the row address latches 26, and a column address bus 32 transmits column address to the column address latches 20. After an appropriate settling time, a row address strobe (RAS) signal 34 (or other controlling clock signal) may be asserted by the control circuitry 28, and the row address latches 26 may latch the transmitted row address. Similarly, the control circuitry 28 may assert a column address strobe 36, and the column address latches 20 may latch the transmitted column address.

Once row and column addresses are latched, the row decoder 24 may determine which row of the memory array 14 corresponds to the latched row address, and the row drivers 22 may assert a signal on the selected row. Similarly, the column decoder 18 may determine which column of the memory

array 14 corresponds with the latched column address, and the quantizing circuit 16 may quantize (e.g., sense) a voltage or current on the selected column. Additional details of reading and writing are described below.

FIG. 3 illustrates an example of a memory array 14. The illustrated memory array 14 includes a plurality of bit-lines 38, 40, 42, 44, and 46 (also referred to as BL0-BL4) and a plurality of word-lines 48, 50, 52, 54, 56, 58, 60, and 62 (also referred to as WL0-WL7). These bit-lines and word-lines are examples of electrical conductors. The memory array 14 further includes a plurality of memory elements 64, each of which may be arranged to intersect one of the bit-lines and one of the word-lines. In other embodiments, imaging elements may be disposed at each of these intersections.

The memory elements and imaging elements may be referred to generally as data locations, i.e., devices or elements configured to convey data, either stored or generated by a sensor, when sensed by a sensing circuit, such as the quantizing circuits discussed below. The data locations may be formed on an integrated semiconductor device (e.g., a device formed on a single crystal of silicon) that also includes the other components of the memory device 12 (or imaging device 13).

In some embodiments, the illustrated memory elements 64 are flash memory devices. The operation of the flash memory elements is described further below with reference to the FIGS. 4 and 5. It should be noted that, in other embodiments, the memory elements 64 may include other types of volatile or nonvolatile memory. For example, the memory elements 64 may include a resistive memory, such as a phase change memory or magnetoresistive memory. In another example, the memory elements 64 may include a capacitor, such as a stacked or trench capacitor. Some types of memory elements 64 may include an access device, such as a transistor or a diode associated with each of the memory elements 64, or the memory elements 64 may not include an access device, for instance in a cross-point array.

FIG. 4 illustrates a circuit 66 that models the operation of an arbitrarily selected memory element 64, which is disposed at the intersection of WL3 and BL0. This circuit 66 includes a capacitor 68, a pre-drain resistor 70 (R_{PD}), a post-source resistor 72 (R_{PS}), and a ground 74. The resistors 70 and 72 model the other devices in series with the memory element 64 being sensed. The illustrated memory element 64 includes a gate 76, a floating gate 78, a drain 80, and a source 82. In the circuit 66, the drain 80 and source 82 are disposed in series between the pre-drain resistor 70 and the post-source resistor 72. The gate 76 is connected to WL3. The pre-drain resistor 70, the drain 80, the source 82, and the post-source resistor 72 are disposed in series on the bit-line BL0. The capacitor 68, which models the capacitance of the bit-line, has one plate connected to ground 74 and another plate connected to the bit-line BL0, in parallel with the memory elements 64.

Several of the components of the circuit 66 represent phenomenon affecting the memory elements 64 when it is sensed. The pre-drain resistor 70 generally represents the drain-to-bitline resistance of the memory elements 64 connected to the bit-line above (i.e., up current from) WL3 when these memory elements 64 are turned on, (e.g., during a read operation). Similarly, the post source resistor 72 generally corresponds to the source-to-ground resistance of the memory elements 64 connected to the bit-line below WL3 when the memory element 64 is sensed. The circuit 66 models electrical phenomena associated with reading the memory elements 64 at the intersection of WL3 and BL0.

The operation of the memory elements 64 will now be briefly described with reference to FIGS. 4 and 5. FIG. 5

illustrates one potential relationship between the bit-line current (I_{BIT}), the word-line voltage (V_{WL}), and the voltage of the floating gate 78 (V_{FG}). As illustrated by FIG. 5, V_{FG} affects the response of the memory element 64 to a given V_{WL}. Decreasing the voltage of the floating gate shifts the I-V curve of the memory elements 64 to the right. That is, the relationship between the bit-line current and a word-line voltage depends on the voltage of the floating gate 78. The memory elements 64 may store data by exploiting this effect.

To write data to the memory elements 64, a charge corresponding to the data may be stored on the floating gate 78. The charge of the floating gate 78 may be modified by applying voltages to the source 82, drain 80, and/or gate 76 such that the resulting electric fields produce phenomenon like Fowler-Northam tunneling and/or hot-electron injection near the floating gate 78. Initially, the memory elements 64 may be erased by applying a word-line voltage designed to drive electrons off of the floating gate 78. In some embodiments, an entire column or block of memory elements 64 may be erased generally simultaneously. Once the memory elements 64 are erased, the gate 76 voltage may be manipulated to drive a charge onto the floating gate 78 that is indicative of a data value. After the write operation ends, the stored charge may remain on the floating gate 78 (i.e., the memory elements 64 may store data in a nonvolatile fashion).

As illustrated by FIG. 5, the value stored by the memory element 64 may be read by applying a voltage, V_{WL}, to the gate 76 and quantizing (e.g., categorizing) a resulting bit-line current, I_{BIT}. Each of the I-V traces depicted by FIG. 5 correspond to a different charge stored on the floating gate, V_{FG}, which should not be confused with the voltage that is applied to the gate, V_{WL}. The difference in floating gate 70 voltage, V_{FG}, between each I-V trace is an arbitrarily selected scaling factor "x." The illustrated I-V traces correspond to eight-different data values stored by the memory element 64, with a V_{FG} of 0x representing a binary data value of 000, a V_{FG} of 1x representing a binary data value of 001, and so on through V_{FG} of 7x, which represents a binary data value of 111. Thus, by applying a voltage to the gate 76 and measuring the resulting bit-line current, the charge stored on the floating gate 78 may be sensed, and the stored data may be read.

The accuracy with which the bit-line current is quantized may affect the amount of data that a designer attempts to store in each memory element 64. For example, in a system with a low sensitivity, a single bit may be stored on each memory element 64. In such a system, a floating gate voltage V_{FG} of 0x may represent a binary value of 0, and a floating gate voltage V_{FG} of –7x may represent a binary value of one. Thus, the difference in floating gate voltages V_{FG} corresponding to different data values may be relatively large, and the resulting differences and bit-line currents for different data values may also be relatively large. As a result, even low-sensitivity sensing circuitry may quantize (e.g., discern) these large differences in bit-line current during a read operation. In contrast, high-sensitivity sensing circuitry may facilitate storing more data in each memory element 64. For instance, if the sensing circuitry can distinguish between the eight different I-V traces depicted by FIG. 5, then the memory elements 64 may store three bits. That is, each of the eight different charges stored on the floating gate 78 may represent a different three-bit value: 000, 001, 010, 011, 100, 101, 110, or 111. Thus, circuitry that precisely quantizes the bit-line current I_{BIT} may allow a designer to increase the amount of data stored in each memory element 64.

However, as mentioned above, a variety of effects may interfere with accurate measurement of the bit-line current. For instance, the position of the memory elements 64 along a

bit-line may affect R_{PD} and R_{PS}, which may affect the relationship between the word-line voltage V_{WL} and the bit-line current I_{BIT}. To illustrate these effects, FIG. 6 depicts noise on the bit-line while reading from the memory element 64. As illustrated, noise in the bit-line current I_{BIT} may cause the bit-line current I_{BIT} to fluctuate. Occasionally, the fluctuation may be large enough to cause the bit-line current I_{BIT} to reach a level that represents a different stored data value, which could cause the wrong value to be read from the memory elements 64. For instance, if the bit-line current is sensed at time 84, corresponding to an arbitrarily selected peak, a data value of 100 may be read rather than the correct data value of 011. Similarly, if the bit-line current is sensed at time 86, corresponding to an arbitrarily selected local minimum, a data value of 010 may be read rather than a data value of 011. Thus, noise on the bit-line may cause erroneous readings from memory elements 64.

FIG. 7 depicts a quantizing circuit 16 that may tend to reduce the likelihood of an erroneous reading. The illustrated quantizing circuit 16 includes an analog-to-digital converter 88 and a digital filter 90 connected to each of the bit-lines 38, 40, 42, 44, and 46, respectively. Each bit-line 38, 40, 42, 44, and 46 may connect to a different analog-to-digital converter 88 and digital filter 90. The digital filters 90, in turn, may connect to an input/output bus 92, which may connect to a column decoder 18, a column address latch 20, and/or control circuitry 28 (see FIG. 2).

In operation, the quantizing circuit 16 may quantize (e.g., digitize) analog signals from the memory elements 64 in a manner that is relatively robust to noise. As explained below, the quantizing circuit 16 may do this by converting the analog signals into a bit-stream and digitally filtering high-frequency components from the bit-stream.

The analog-to-digital converter 88 may be a one-bit, analog-to-digital converter or a multi-bit, analog-to-digital converter. In the present embodiment, an analog-to-digital converter 88 receives an analog signal from the memory element 64, e.g., a bit-line current I_{BIT} or a bit-line voltage V_{BL}, and outputs a bit-stream that represents the analog signal. The bit-stream may be a one-bit, serial signal with a time-averaged value that generally represents the time-averaged value of the analog signal from the memory element 64. That is, the bit-stream may fluctuate between values of zero and one, but its average value, over a sufficiently large period of time, may be proportional to the average value of the analog signal from the memory element 64. In certain embodiments, the bit-stream from the analog-to-digital converter 88 may be a pulse-density modulated (PDM) version of the analog signal. The analog-to-digital converter 88 may transmit the bit-stream to the digital filter 90 on a bit-stream signal path 94.

The digital filter 90 may digitally filter high-frequency noise from the bit-stream. To this end, the digital filter 90 may be a low-pass filter, such as a counter, configured to average (e.g., integrate and divide by the sensing time) the bit-stream over a sensing time, i.e., the time period over which the memory element 64 is read. (Alternatively, in some embodiments, the digital filter 90 is configured to integrate the bit-stream without dividing by the sensing time.) As a result, the digital filter 90 may output a value that is representative of both the average value of the bit-stream and the average value of the analog signal from the memory element 64. In some embodiments, the digital filter 90 is a counter, and the cut-off frequency of the digital filter 90 may be selected by adjusting the duration of the sensing time. In the present embodiment, increasing the sensing time will lower the cutoff frequency. That is, the frequency response of the digital filter 90 may be modified by adjusting the period of time over which the

bit-stream is integrated and/or averaged before outputting a final value. The frequency response of the digital filter **90** is described further below with reference to FIG. **15**. For multi-bit memory elements **64**, the output from the digital filter **90** may be a multi-bit binary signal, e.g., a digital word that is transmitted serially and/or in parallel.

Advantageously, in certain embodiments, the quantizing circuit **16** may facilitate the use of multi-bit memory elements **64**. As described above, in traditional designs, the number of discrete data values that a memory element **64** stores may be limited by sense amps that react to noise. In contrast, the quantizing circuit **16** may be less susceptible to noise, and, as a result, the memory elements **64** may be configured to store additional data. Without the high frequency noise, the intervals between signals representative of different data values may be made smaller, and the number of data values stored by a given memory element **64** may be increased. Thus, beneficially, the quantizing circuit **16** may read memory elements **64** that store several bits of data, e.g., 2, 3, 4, 5, 6, 7, 8, or more bits per memory element **64**.

Although the quantizing circuit **16** may sense the signal from the memory element **64** over a longer period of time than conventional designs, the overall speed of the memory device **12** may be improved. As compared to a conventional device, each read or write operation of the memory device **12** may transfer more bits of data into or out of the memory element **64**. As a result, while each read or write operation may take longer, more data may be read or written during the operation, thereby improving overall performance. Further, in some memory devices **12**, certain processes may be performed in parallel with a read or write operation, thereby further reducing the overall impact of the longer sensing time. For example, in some embodiments, the memory array **14** may be divided into banks that operate at least partially independently, so that, while data is being written or read from one bank, another bank can read or write data in parallel.

FIG. **8** illustrates details of one implementation of the quantizing circuit **16**. In this embodiment, the digital filter **90** is a counter, and the analog-to-digital converter **88** is a first-order delta-sigma modulator. The illustrated delta-sigma modulator **88** may include a latched comparator **96**, a capacitor **98**, and a switch **100**. In other embodiments, other types of digital filters and analog-to-digital converters may be employed, such as those described below in reference to FIGS. **17** and **18**.

As illustrated, an input of the counter **90** may connect to the bit-stream signal path **94**, which may connect to an output of the comparator **96**. The output of the comparator **96** may also connect to a gate of the switch **100** by a feedback signal path **102**. The output terminal (e.g., source or drain) of the switch **100** may connect in series to one of the bit-lines **38**, **40**, **42**, **44**, or **46**, and the input terminal of the switch **100** may connect to a reference current source **104** (I_{REF}). One plate of the capacitor **98** may connect to one of the bit-lines **38**, **40**, **42**, **44**, or **46**, and the other plate of the capacitor **98** may connect to ground.

The illustrated counter **90** counts the number of clock cycles that the bit-stream **94** is at a logic high value or logic low value during the sensing time. The counter may count up or count down, depending on the embodiment. In some embodiments, the counter **90** may do both, counting up one for each clock cycle that the bit-stream has a logic high value and down one for each clock cycle that the bit-stream has a logic low value. Output terminals (D0-D5) of the counter **90** may connect to the input/output bus **92** for transmitting the count. The counter **90** may be configured to be reset to zero or some other value when a reset signal is asserted. In some embodiments, the counter **90** may be a series connection of

D-flip flops, e.g., D-flip flops having SRAM or other memory for storing an initial value and/or values to be written to the memory element **64**.

In the illustrated embodiment, the clocked comparator **96** compares a reference voltage (V_{REF}) to the voltage of one of the bit-lines **38**, **40**, **42**, **44**, or **46** (V_{BL}), which may be generally equal to the voltage of one plate of the capacitor **98**. The comparator **96** may be clocked (e.g., falling and/or rising edge triggered), and the comparison may be performed at regular intervals based on the clock signal, e.g., once per clock cycle. Additionally, the comparator **96** may latch, i.e., continue to output, values (V_{FB}) between comparisons. Thus, when the clock signals the comparator **96** to perform a comparison, if V_{BL} is less than V_{REF}, then the comparator **96** may latch its output to a logic low value, as described below in reference to FIG. **9**. Conversely, if V_{BL} is greater than V_{REF}, then the comparator **96** may latch a logic high value on its output, as described below in reference to FIG. **10**. As a result, the illustrated comparator **96** outputs a bit-stream that indicates whether V_{BL} is larger than V_{REF}, where the indication is updated once per clock cycle.

Advantageously, in some embodiments, the quantizing circuit **16** may include a single comparator (e.g., not more than one) for each column of multi-level memory elements **64**. In contrast, conventional sense amplifiers often include multiple comparators to read from a multi-bit memory cell, thereby potentially increasing device complexity and cost.

The capacitor **98** may be formed by capacitive coupling of the bit-lines **38**, **40**, **42**, **44**, and **46**. In other designs, this type of capacitance is referred to as parasitic capacitance because it often hinders the operation of the device. However, in this embodiment, the capacitor **98** may be used to integrate differences between currents on the bit-lines **38**, **40**, **42**, **44**, or **46** and the reference current to form the bit-stream, as explained further below. In some embodiments, the capacitor **98** may be supplemented or replaced with an integrated capacitor that provides greater capacitance than the "parasitic" bit-line capacitance.

The illustrated switch **100** selectively transmits current I_{REF} from the reference current source **104**. In various embodiments, the switch **100** may be a PMOS transistor (as illustrated in FIGS. **8-10**) or an NMOS transistor (as illustrated in FIG. **17**) controlled by the V_{FB} signal on the feedback signal path **102**.

The operation of the quantizing circuit **16** will now be described with reference to FIGS. **9-12**. Specifically, FIGS. **9** and **10** depict current flows in the quantizing circuit **16** when the comparator **96** is latched low and high, respectively. FIG. **11** illustrates V_{BL}, the bit-stream output from the comparator **96**, and the corresponding increasing count of the counter **90** for a relatively small bit-line current. FIG. **12** depicts the same voltages when measuring a medium sized bit-line current, and FIG. **13** depicts these voltages when measuring a relatively large bit-line current.

To sense the current through the memory element **64**, the illustrated delta-sigma modulator **88** exploits transient effects to output a bit-stream representative of the bit-line current I_{BIT}. Specifically, the delta-sigma modulator **88** may repeatedly charge and discharge the capacitor **98** with a current divider that subtracts the bit-line current I_{BIT} from the reference current I_{REF}. Consequently, a large current through the memory element **64** may rapidly discharge the capacitor **98**, and a small current through the memory element **64** may slowly discharge the capacitor **98**.

To charge and discharge the capacitor **98**, the delta-sigma modulator **88** switches between two states: the state depicted by FIG. **9** (hereinafter "the charging state") and the state

depicted by FIG. **10** (hereinafter "the discharging state"). Each time the delta-sigma modulator **88** transitions between these states, the bit-stream changes from a logic high value to a logic low value or vice versa. The proportion of time that the delta-sigma modulator **88** is in the state illustrated by either FIG. **9** or FIG. **10** may be proportional to the size of the bit-line current I_{BIT} through the memory element **64**. The larger the bit-line current I_{BIT}, the more time that the delta-sigma modulator **88** is in the state illustrated by FIG. **9**, rather than the state illustrated by FIG. **10**, and the more time that the bit-stream has a logic low value.

Starting with the charging state (FIG. **9**), the capacitor **98** may initially accumulate a charge (e.g., become more charged). To this end, the output of the comparator **96** is latched to logic low, which, as mentioned above, may occur when V_{BL} is less than V_{REF}. The logic low may be conveyed to switch **100** by the feedback signal path **102**, and the switch **100** may close, thereby conducting the reference current I_{REF} through one of the bit-lines **38**, **40**, **42**, **44**, or **46**, as indicated by the larger arrows in FIG. **9**. A portion of the electrons flowing through the reference current source **104** may be accumulated by the capacitor **98**, as indicated by the smaller-horizontal arrows, and the remainder may be conducted through the memory element **64**, i.e., the bit-line current I_{BIT}, as indicated by the smaller vertical arrows. Thus, the capacitor **98** may accumulate a charge, and V_{BL} may increase.

The comparator **96** and the reference current source **104** may cooperate to charge the capacitor **98** for a discrete number of clock cycles. That is, when the delta-sigma modulator **88** transitions to the charging state, the delta-sigma modulator **88** may remain in this state for an integer number of clock cycles. In the illustrated embodiment, the comparator **96**, the output of which is latched, changes state no more than once per clock cycle, so the switch **100**, which is controlled by the output of the comparator **96**, V_{FB}, conducts current for a discrete number of clock cycles. As a result, the reference current source **104** conducts current I_{REF} through the bit-line and into the capacitor **98** for an integer number of clock cycles.

After each clock cycle of charging the capacitor **98**, the delta-sigma modulator **88** may transition from the charging state to the discharging state, which is illustrated by FIG. **10**, depending on the relative values of V_{BL} and V_{REF}. Once per clock cycle (or at some other appropriate interval, such as twice per clock cycle), the comparator **96** may compare the voltage of the capacitor V_{BL} to the reference voltage V_{REF}. If the capacitor **98** has been charged to the point that V_{BL} is greater than V_{REF}, then the output of the comparator **96** may transition to logic high, as illustrated in FIG. **10**. The logic high signal may be conveyed to the switch **100** by the feedback signal path **102**, thereby opening the switch **100**. As a result, the reference current source **104** may cease conducting current through the memory element **64** and into the capacitor **98**, and the capacitor **98** may begin to discharge through the memory element **64**.

In the present embodiment, the delta-sigma modulator **88** discharges the capacitor **98** for a discrete number of clock intervals. After each clock cycle of discharging the capacitor **98**, the delta-sigma modulator **88** compares V_{BL} to V_{REF}. If V_{BL} is still greater than V_{REF}, then the comparator **96** may continue to output a logic high signal, i.e., V_{FB}=1, and the switch **100** remains open. On the other hand, if enough current has flowed out of the capacitor **98** that V_{BL} is less than V_{REF}, then the comparator **96** may output a logic low signal, i.e., V_{FB}=0, and the switch **100** may close, thereby transitioning the delta-sigma modulator **88** back to the charging state and initiating a new cycle.

The counter **90** may count the number of clock cycles that the delta-sigma modulator **88** is in either the charging state or the discharging state by monitoring the bit-stream signal path **94**. The bit-stream signal path **94** may transition back and forth between logic high and logic low with the output of the comparator **96**, V_{FB}, and the counter **90** may increment and/or decrement a count once per clock cycle (or other appropriate interval) based on whether the bit-stream is logic high or logic low. After the sensing time has passed, the counter **90** may output a signal indicative of the count on output terminals **D0**-**D5**. As explained below, the count may correspond, e.g., proportionally, to the bit-line current, I_{BIT}.

FIGS. **11**-**13** illustrate voltages V_{FB} and V_{BL} in the quantizing circuit **16** when reading data from a memory element **64**. Specifically, FIG. **11** illustrates a low-current case, in which the value stored by the memory element **64** is represented by a relatively low bit-line current. Similarly, FIG. **12** illustrates a medium-current case, and FIG. **13** illustrates a high-current case. In each of these figures, the ordinate of the lower trace represents the voltage of the bit-stream signal path **94**, V_{FB}, and the ordinate of the upper trace illustrates the bit-line voltage, V_{BL}. The abscissa in each of the traces represents time, with the lower trace synchronized with the upper trace, and the duration of the time axes is one sensing time **106**.

As illustrated by FIG. **11**, the counter **90** is initially preset to zero (or some other appropriate value) by applying a reset signal. In some embodiments, the delta-sigma modulator **88** may undergo a number of start-up cycles to reach steady-state operation before initiating the sensing time and resetting the counter **90**. At the beginning of the illustrated read operation, the delta-sigma modulator **88** is in the charging state, which charges the capacitor **98** and increases V_{BL}, as indicated by dimension arrow **108**. At the beginning of the next clock cycle, the comparator **96** compares the bit-line voltage to the reference voltage and determines that the bit-line voltage is greater than the reference voltage. As a result, the bit-stream signal path **94** (V_{FB}) transitions to a logic high voltage, and the delta-sigma modulator **88** transitions to the discharging state. Additionally, the counter **90** increments the count by one to account for one clock cycle of the bit-stream signal **94** holding a logic low value. Next, the charge stored on the capacitor **98** drains out through the memory element **64**, and the bit-line voltage drops until the comparator **96** determines that V_{BL} is less than V_{REF}, at which point the cycle repeats. The cycle has a period **112**, which may be divided into a charging portion **114** and a discharging portion **116**. Once during each cycle in the sensing time **106**, the count stored in the counter **90** may increase by one. At the end of the sensing time **106**, the counter **90** may output the total count.

A comparison of FIG. **11** to FIGS. **12** and **13** illustrates why the count correlates with the bit-line current. In FIG. **13**, the high-current case, the stored charge drains from the capacitor **98** quickly, relative to the other cases, because the bit-line current I_{BIT} is large and, as a result, the delta-sigma modulator **88** spends more time in the charging state than the discharging state. As a result, the bit-stream has a logic low value for a large portion of the sensing time **106**, thereby increasing the count.

The capacitance of the capacitor **98** may be selected with both the clock frequency and the range of expected bit-line currents in mind. For example, the capacitor **98** may be large enough that the capacitor **98** does not fully discharge (e.g., saturate) when the bit-line current I_{BIT} is either at its lowest expected value or at its highest expected value. That is, in some embodiments, the capacitor **98** generally remains in a transient state while reading the memory element **64**. Simi-

larly, the frequency at which the comparator **96** is clocked may affect the design of the capacitor **98**. A relatively high frequency clock signal may leave the capacitor **98** with relatively little time to discharge or saturate between clock cycles, thereby leading a designer to choose a smaller capacitor **98**.

Similarly, the size of the reference current may be selected with the range of expected bit-line currents in mind. Specifically, in certain embodiments, the reference current is less than the largest expected bit-line current I_{BIT}, so that, in the case of maximum bit-line current I_{BIT}, the capacitor **98** can draw charge from the reference current while the rest of the reference current flows through the memory element **64**.

FIG. **14** illustrates the relationship between the bit-line current I_{BIT} and the count for the presently discussed embodiment. As illustrated by FIG. **14**, the count corresponds with (e.g., is generally proportional to) the bit-line current I_{BIT}. This relationship is described by the following equation (Equation 1), in which N_{ST} represents the number of clock cycles during the sensing time:

$$I_{BIT}/I_{REF}=\text{Count}/N_{ST}$$

Thus, in the illustrated embodiment, the count corresponds with (e.g., is indicative of) the bit-line current I_{BIT}, which corresponds with the value stored by the memory element **64**.

Advantageously, the quantizing circuit **16** may quantize (e.g., categorize) the bit-line current I_{BIT} as falling into one of a large number of categories, each of which is represented by an increment of the count. In doing so, in some embodiments, the quantizing circuit **16** may resolve small differences in the bit-line current I_{BIT}. The resolution of the quantizing circuit **16** may be characterized by the following equation (Equation 2), in which I_{MR} represents the smallest resolvable difference in bit-line current I_{BIT}, i.e., the resolution of the quantizing circuit **16**:

$$I_{MR}=I_{REF}/N_{ST}$$

Thus, the resolution of the quantizing circuit **16** may be increased by increasing the sensing time or the clock frequency or by decreasing I_{REF}, which may limit the maximum cell current since I_{MR} is less than I_{REF}.

The resolution of the quantizing circuit **16** may facilitate storing multiple bits in the memory element **64** or sensing multiple levels of light intensity in an image sensor element. For example, if the quantizing circuit **16** is configured to quantize (e.g., categorize) the bit-line current I_{BIT} into one of four different levels, then the memory element **64** may store two-bits of data or, if the quantizing circuit **16** is configured to categorize the bit-line current I_{BIT} into one of eight different current levels, then the memory element **64** may store three-bits of data. For the present embodiment, the number of bits stored by the memory element **64** may be characterized by the following equation (Equation 3), in which N_B represents the number of bits stored by a memory element **64** and I_{RANGE} represents the range of programmable bit-line currents through the memory element **64**:

$$N_B=\log(I_{RANGE}/I_{MR})/\log 2$$

In short, in the present embodiment, greater resolution translates into higher density data storage for a given memory element **64**.

FIG. **15** is a graph that illustrates one way in which the counter **90** may be configured to further reduce the effects of noise. In FIG. **15**, the abscissa represents the count, and the ordinate represents the output of the quantizing circuit **16**. In the present embodiment, the three-least-significant digits of the count are disregarded as potentially corrupted by noise. That is, D**0**-D**2** (FIG. **8**) either do not connect to the input/ output bus **92** or are not interpreted as conveying data that is stored by the memory element **64**. As a result, a range of counter values may represent a single data value stored by the memory element **64**. For example, in the present embodiment, count values ranging from 00 1000 to 00 1111 are construed as representing a data value of 001. Representing data in this manner may further reduce the effects of noise because, even if noise affects the count, in many embodiments, it would have to affect the count in a consistent manner over a substantial portion of the sensing time to affect the more significant digits of the count. That is, disregarding less significant digits may lower the cutoff frequency of the counter **90**. In other embodiments, fewer, more, or no digits may be truncated from the count as potentially representing noise.

Truncating less significant digits may introduce a rounding error, or a downward bias, in the output. This effect may be mitigated by presetting (e.g., driving latches to a particular state in advance of counting or storing a value in memory) the counter **90** in a manner that accounts for this bias. The counter **90** may be preset either before reading from the memory element **64** or before writing to the memory element **64**. In some embodiments, the preset value may be one-half of the size of the range of counter values that represent a single output value. In other words, if m digits are truncated from the output, then the counter **90** may be preset to one-half of 2^m before reading from a memory element **64** or before writing to the memory element **64**. In some embodiments, the memory in the counter **90** may store this preset value.

In addition to truncating less significant bits, other techniques may improve the accuracy of the memory device **12**. For example, a process that, in certain embodiments, tends to compensate for changing conditions in the memory device **12** is described below. This process is described by first explaining the changing conditions that may impede the operation of the memory device **12** and then explaining how certain embodiments may mitigate this phenomenon. To explain this embodiment, FIG. **16** illustrates a single flash memory cell **118**, and FIG. **17** illustrates a circuit that models the operation of the flash memory cell **118**. As described below in reference to these figures, data may be written to the flash memory cell **118** in a sequence, e.g., top-to-bottom or bottom-to-top, and this sequence may affect the fidelity of the flash memory cell **118**. After describing this effect, embodiments wherein the effect may be advantageously reduced or eliminated by a process illustrated by FIG. **18** are described with further reference to FIG. **16**.

FIG. **16** illustrates the flash memory cell **118**, which along with an array of similar flash memory cells, may be included in the memory array **14** (FIG. **3**). The illustrated flash memory cell **118** includes two-select transistors **120** and **122** and eight floating gate transistors **124**, **126**, **128**, **130**, **132**, **134**, **136**, and **138**. Other embodiments may include more or fewer floating gate transistors.

These transistors **124-138** may be connected to each other in series, with the source of one transistor connected to the drain of the adjacent transistor. In the schematic view of FIG. **16**, the source of each of the transistors **124-138** is on the bottom, and the drain of each of the transistors **124-138** is on the top. As used herein, the terms "bottom" and "top" do not refer to any particular spatial orientation. Rather, that the term "bottom" refers to the terminal of each of these transistors **124-138** that is closer to ground **74**, and the term "top" refers to the terminal of each of these transistors **124-138** that is closer to the quantizing circuitry **16**.

In operation, the data read from the transistors **124-138** may be affected by the sequence with which data is written to

the transistors **124-138**. Depending on the sequence, the fidelity of each of the transistors **124-138** may be affected by the data stored in the other transistors **124-138**. To illustrate this effect, FIG. **17** depicts a circuit **140** that models the operation of the memory cell **118** when accessing the transistor **128**, which is arbitrarily selected for purposes of explanation. When writing to, or reading from, a given transistor, in the present embodiment, the control gates of the other transistors are energized, so that the other transistors conduct and the transistor being accessed can set the current. Although the other control gates are energized, these other transistors may still have a source-to-drain resistance, which the circuit **140** models with resistors R_{D0-2} and R_{S0-5}. The total series resistance of the transistors above the accessed transistor **128** is referred to as R_D, and the total series resistance of the transistors below the accessed transistor **128** is referred to as R_S. Thus, the transistor **128** may be modeled as having the resistor R_D coupled to its drain and the resistor R_S coupled to its source.

The magnitude of R_S and R_D may depend, in part, on the data stored by the other transistors **124-138**. For example, if a non-accessed transistor stores a large charge on its floating gate, corresponding to a large, stored data value, then it may have a high source-to-drain resistance, because the charge on the floating gate may counteract the charge on the control gate. As a result, although the control gate of the non-accessed transistor is energized, the non-accessed transistor may still partially resist the flow of current between its source and drain. Further, the size of this effect may depend on the data value stored on the non-accessed transistor. For instance, if the source-side transistors **130-138** all store relatively large data values, then R_S may be relatively large. In other designs, this effect may be reversed, but the data dependent variation remains. Thus, the values of R_S and R_D may vary, depending on the data stored by the memory cell **118**.

Data dependent changes in R_S are particularly significant because variations in R_S directly modulate the gate-source voltage of the memory cell **128**. To store data, each transistor **124-138** stores a charge on its floating gate. In the present embodiment, the charge on the floating gate is manipulated by controlling the voltage between the control gate and the source (V_{GS}) of each of the transistors **124-138**. The value of V_{GS} depends on the current through the transistor **128** (I_{CELL}) and R_S. Specifically, V_{GS} is related to the product of these two values. Thus, because the effective V_{GS} is a function of the amount of charge on the floating gate, and because V_{GS} is affected by R_S, variations in R_S can affect the value stored by the transistor **128**.

By a similar mechanism, variations in R_S can affect the value or read from the transistor **128**. As described above with reference to FIG. **4**, data may be read from the transistor **128** by changing V_{GS} and measuring a resulting change in the current I_{CELL}. In the present embodiment, the value of the stored data is indicated by the effect of the floating gate voltage V_{FG} on the resulting current I_{CELL}. However, variations in V_{GS} may have a similar effect, and as described above, changes in R_S may cause V_{GS} to change. Thus, changes in R_S may interfere with reading from the transistor **128**, because changes in R_S may produce an effect on I_{CELL} that is similar to a change in V_{FG}, which stores data. That is, the value read from the transistor **128** may be affected by R_S, which is determined, in part, by the values of the data stored in the source-side flash memory devices. As a result, in some embodiments, if the values stored by the source-side transistors change between reading and writing, the value read from the transistor **128** may not correlate with the value written to the transistor **128**.

This effect may be mitigated by a process **142** illustrated by FIG. **18**. As described below, the process **142** may write to, and read from, the memory cell **118** in a sequence configured to match R_S when reading to R_S when writing. That is, the process **142**, in certain embodiments, may correlate source-side resistance when reading and writing, thus reducing the effects of the variation in the bottom transistors in the memory cell.

The process **142** begins with erasing a memory cell, as illustrated by block **144**. The memory cell, in this embodiment, includes a plurality of data locations (e.g., floating gate transistors or other memory elements) that are connected to one another in the series. In some embodiments, the entire memory cell may be erased generally simultaneously. For example, certain types of flash memory devices may be erased in this manner. In such devices, erasing may include energizing the control gate to a voltage sufficient to drive a charge on to, or off of, the floating gate. Different embodiments may include different numbers of data locations, e.g., some embodiments may include 4, 8, 16, 32, or more data locations in the memory cell.

As indicated in block **144**, the data locations may be connected to one another in series. An example of such a series is illustrated by FIG. **16**, which as described above, depicts a memory cell **118** with a plurality of flash memory transistors **124-138** connected source-to-drain in series. The series of FIG. **16** also has ends, i.e., the transistors **124** and **138**. In the illustrated embodiment, all of the floating gate transistors **124-138** are oriented in the same direction with respect to the series, i.e., each of the non-end transistors **125-137** has a source connected to the drain of an adjacent transistor. The distal terminal of the end transistors **124** and **138** may connect to either a source or a drain of the select transistors **120** and **122**, respectively, depending on the orientation of the select transistors **120** and **122**. This arrangement of transistors **124-138** is referred to as a source-to-drain series, and in this series, the transistors extending from the source of a given transistor are referred to as source-side transistors. In other embodiments, a plurality of phase change memory elements or other resistive memory elements may be connected in series.

Next in the process **142**, values are written to each of the data locations, starting with the data location at one end of the series, and then sequentially writing to each adjacent data location, as illustrated by block **146**. As previously described, writing may include driving a charge onto, or off of, a floating gate or manipulating the phase of a phase change memory element, depending on the type of data location. In this embodiment of the process **142**, the data locations are written to sequentially, so applying this embodiment of the process **142** to the memory cell **118** illustrated by FIG. **16**, a value is first written to the transistor **138** and then transistors **136, 134, 132**, and so on, in sequence, until transistor **124**. Thus, before writing to each of the transistors **124-138**, each source-side transistor is written to first.

Fixing the value of the source-side transistors before writing is believed to improve the fidelity of the memory cell **118**. As explained above, the data stored by the source-side transistors determines R_S, and R_S affects V_{GS}, which is modulated to store a charge that is representative of data. Writing from the bottom of the series of devices up establishes a value of R_S that does not change between reading and writing. That is, in this embodiment, the data that determines R_S is the same when reading from a transistor and when writing to a transistor. As a result, the reading-R_S is correlated to the writing-R_S, and a source of noise is mitigated.

The act illustrated by block **146** begins with writing to an data location at one end of the series. Different ends may be

selected, depending on the embodiment. That is, in certain embodiments, the end of the series with which this step starts may be either a transistor with its source on the distal end of the series (e.g., transistor **138** in FIG. **16**) or a transistor with its drain on the distal end of the series (e.g., transistor **124** and FIG. **16**).

Values may be written to each data location through an iterative feedback process. In an example of such a process, a value is first written to the data location and, then, read back from the data location. The value read back is compared to a desired value to determine whether the data location stores the correct value. If it does not, a property of the data location, e.g., a charge on a floating gate, may be adjusted by another increment. In other words, the step **146** may include incrementally adjusting a property of the data location until that property correlates with the value to be written. For instance, the charge on the floating gate may be incrementally increased until the charge indicates the value to be written. In another example, the crystallinity of a phase change memory element may be incrementally adjusted until the resistance of the phase change memory element correlates with the value to be written. In these examples, writing includes repeatedly adjusting and reading from an data location until that data location indicates the proper value.

Next, a value is read from one of the data locations, as illustrated by block **148**. Reading may include sensing the current I_{CELL}, also referred to in some embodiments as I_{BIT}, with the previously described delta-sigma modulators. Reading may include reading from each of the data locations or an arbitrarily selected one of the data locations. Advantageously, because the data locations were written to from the bottom up, the value of R_S, when reading, is generally equal to the value of R_S when writing. Correlating source-side resistance R_S is believed to reduce noise that could otherwise mask the value of the data being read. As a result, the data location may be sensed more accurately.

FIG. **19** depicts an exemplary processor-based system **310** that includes the memory device **12**. Alternatively or additionally, the system **310** may include the imaging device **13**. The system **310** may be any of a variety of types such as a computer, pager, cellular phone, personal organizer, control circuit, etc. In a typical processor-based system, one or more processors **312**, such as a microprocessor, control the processing of system functions and requests in the system **310**. The processor **312** and other subcomponents of the system **310** may include quantizing circuits, such as those discussed above.

The system **310** typically includes a power supply **314**. For instance, if the system **310** is a portable system, the power supply **314** may advantageously include a fuel cell, permanent batteries, replaceable batteries, and/or rechargeable batteries. The power supply **314** may also include an AC adapter, so the system **310** may be plugged into a wall outlet, for instance. The power supply **314** may also include a DC adapter such that the system **310** may be plugged into a vehicle cigarette lighter, for instance.

Various other devices may be coupled to the processor **312** depending on the functions that the system **310** performs. For instance, a user interface **316** may be coupled to the processor **312**. The user interface **316** may include buttons, switches, a keyboard, a light pen, a mouse, a digitizer and stylus, and/or a voice recognition system, for instance. A display **318** may also be coupled to the processor **312**. The display **318** may include an LCD, an SED display, a CRT display, a DLP display, a plasma display, an OLED display, LEDs, and/or an audio display, for example. Furthermore, an RF sub-system/baseband processor **320** may also be coupled to the processor

312. The RF sub-system/baseband processor **320** may include an antenna that is coupled to an RF receiver and to an RF transmitter (not shown). One or more communication ports **322** may also be coupled to the processor **312**. The communication port **322** may be adapted to be coupled to one or more peripheral devices **324** such as a modem, a printer, a computer, or to a network, such as a local area network, remote area network, intranet, or the Internet, for instance.

The processor **312** generally controls the system **310** by implementing software programs stored in the memory. The memory is operably coupled to the processor **312** to store and facilitate execution of various programs. For instance, the processor **312** may be coupled to the volatile memory **326** which may include Dynamic Random Access Memory (DRAM) and/or Static Random Access Memory (SRAM). The volatile memory **326** is typically large so that it can store dynamically loaded applications and data. As described further below, the volatile memory **326** may be configured in accordance with embodiments of the present invention.

The processor **312** may also be coupled to the memory device **12**. The memory device **12** may include a read-only memory (ROM), such as an EPROM, and/or flash memory to be used in conjunction with the volatile memory **326**. The size of the ROM is typically selected to be just large enough to store any necessary operating system, application programs, and fixed data. Additionally, the non-volatile memory **328** may include a high capacity memory such as a tape or disk drive memory.

The memory device **10** and volatile memory **326** may store various types of software, such as an operating system or office productivity suite including a word processing application, a spreadsheet application, an email application, and/or a database application. This software may be stored on a variety of types of tangible machine readable mediums.

While the invention may be susceptible to various modifications and alternative forms, specific embodiments have been shown by way of example in the drawings and have been described in detail herein. However, it should be understood that the invention is not intended to be limited to the particular forms disclosed. Rather, the invention is to cover all modifications, equivalents, and alternatives falling within the spirit and scope of the invention as defined by the following appended claims.

What is claimed is:

1. A method, comprising:
   writing to each of a plurality of floating gate transistors one at a time, in sequence, starting with a first floating gate transistor at an end of the series and finishing with a second floating gate transistor at the other end of the series, wherein writing comprises incrementally adjusting a charge on each of the floating gate transistors and sensing whether the charge corresponds to a desired value.

2. The method of claim **1**, comprising erasing the plurality of floating gate transistors generally simultaneously.

3. The method of claim **1**, comprising reading from one of the plurality of floating gate transistors, wherein reading is performed before any of the floating gate transistors is written to again.

4. The method of claim **1**, comprising reading from one of the plurality of floating gate transistors with a delta-sigma modulator.

5. The method of claim **4**, wherein reading comprises transmitting a bit-stream from the delta-sigma modulator to a counter.

6. The method of claim **4**, wherein reading comprises truncating a least significant bit from an output of the counter.

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7. A method, comprising:
writing a plurality of data values to a plurality of data locations one at a time, in sequence, wherein the writing comprises:
adjusting a parameter of one of the data locations by an increment;
reading the value stored by the one of the data locations;
determining whether the value stored corresponds to a value to be written; and
if the value stored does not correspond to the value to be written, adjusting the parameter by another increment.

8. The method of claim 7, wherein adjusting the parameter comprises changing a charge on the one of the data locations.

9. The method of claim 7, wherein adjusting the parameter comprises adjusting the crystallinity of the one of the data locations.

10. The method of claim 7, wherein writing the plurality of data values to the plurality of data locations one at a time, in sequence, comprises starting with a data location at an end of the series and sequentially writing to each adjacent data location.

11. The method of claim 10, wherein starting with the data location at an end of the series comprises starting with a data location with its source on a distal end of the series.

12. The method of claim 10, wherein starting with the data location at an end of the series comprises starting with a data location with its drain on a distal end of the series.

13. The method of claim 7, wherein writing the plurality of data values to the plurality of data locations comprises writing the plurality of data values to a plurality of floating gate transistors.

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14. The method of claim 7, wherein writing the plurality of data values to the plurality of data locations comprises writing the plurality of data values to a plurality of phase change memory elements.

15. A method, comprising:
writing to each of a plurality of data locations starting with a data location at an end of the plurality of data locations and then sequentially writing to each adjacent data location; and
reading from one of the data locations by sensing a current through the data location with a delta-sigma modulator.

16. The method of claim 15, wherein writing comprises writing to every data location transistor in the plurality of data locations based on a number of data locations between a given data location and a data location at the end of the plurality of data locations.

17. The method of claim 15, wherein writing comprises:
adjusting a parameter of one of the data locations by an increment;
reading the value stored by the one of the data locations;
determining whether the value stored corresponds to a value to be written; and
if the value stored does not correspond to the value to be written, adjusting the parameter by another increment.

18. The method of claim 17, wherein reading comprises sensing a current through the one of the data locations with the delta-sigma modulator.

19. The method of claim 15, comprising erasing the plurality of data locations generally simultaneously.

20. The method of claim 15, comprising transmitting data read from the one of the data locations to a processor of a computer system.

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