Disclosed are methods, systems and devices, such as a device including a data location, a quantizing circuit coupled to the data location, and a test module coupled to the quantizing circuit. In one or more embodiments, the test module can include a linear-feedback shift register.

27 Claims, 16 Drawing Sheets
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FIG. 5

<table>
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<th>DATA</th>
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<tr>
<td>0.0</td>
<td>000</td>
</tr>
<tr>
<td>-1.0</td>
<td>010</td>
</tr>
<tr>
<td>-2.0</td>
<td>010</td>
</tr>
<tr>
<td>-3.0</td>
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</tr>
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<td>-4.0</td>
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<td>-5.0</td>
<td>101</td>
</tr>
<tr>
<td>-6.0</td>
<td>110</td>
</tr>
<tr>
<td>-7.0</td>
<td>111</td>
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BIT LINE CURRENT (I.BL) vs. WORD LINE VOLTAGE (V.WL)
FIG. 7
FIG. 10

VREF

VREF

100

VBL

C

96

98

92

D0 D1 D2 D3 D4 D5

CLOCK

RESET

I/0

90

VFB = 1

16

VBL < VREF

10.4

lREF

102

94

US 7,818,638 B2
FIG. 14

![Graph showing relationship between COUNT and BIT LINE CURRENT (I_BIT)]

FIG. 15

![Graph showing relationship between OUTPUT and COUNT]
FIG. 16

BIST COLUMN DECODER MODULE

MEMORY

DF

A/D

WL0

WL1

WL2

WL3

WL4

WL5

WL6

WL7

BL0

BL1

BL2

BL3

BL4
OUTPUT TEST DATA

WRITE THE TEST DATA TO A DATA LOCATION

READ THE TEST DATA FROM THE DATA LOCATION

DETERMINE WHETHER THE TEST DATA WRITTEN TO THE DATA LOCATION CORRESPONDS TO THE DATA READ FROM THE DATA LOCATION

FIG. 19
1. Field of Invention

Embodiments of the present invention relate generally to electronic devices and, more specifically, in certain embodiments, to memory with built-in self-test.

2. Description of Related Art

Generally, memory devices include an array of memory elements and associated sense amplifiers. The memory elements store data, and the sense amplifiers read the data from the memory elements. To read data, for example, a current is passed through the memory element, and the current or a resulting voltage is measured by the sense amplifier. Conventionally, the sense amplifier measures the current or voltage by comparing it to a reference current or voltage. Depending on whether the current or voltage is greater than the reference, the sense amplifier outputs a value of one or zero. That is, the sense amplifier quantizes (e.g., digitizes) the analog signal from the memory element into one of two logic states.

Many types of memory elements are capable of assuming more than just two states. For example, some memory elements are capable of multi-bit (e.g., more than two state) storage. For instance, rather than outputting either a high or low voltage, the memory element may output four or eight different voltage levels, each level corresponding to a different data value. However, conventional sense amplifiers often fail to distinguish accurately between the additional levels because the difference between the levels (e.g., a voltage difference) in a multi-bit memory element is often smaller than the difference between the levels in a single-bit (i.e., two state) memory element. Thus, conventional sense amplifiers often cannot read multi-bit memory elements. This problem may be increased as high performance multi-bit memory elements become increasingly dense, thereby reducing the size of the memory elements and the difference between the levels (e.g., voltage) to be sensed by the sense amplifiers.

A variety of factors may tend to prevent the sense amplifier from discerning small differences in the levels of a multi-bit memory element. For instance, noise in the power supply, ground, and reference voltage may cause an inaccurate reading of the memory element. The noise may have a variety of sources, such as temperature variations, parasitic signals, data dependent effects, and manufacturing process variations. This susceptibility to noise often leads a designer to reduce the number of readable states of the memory element, which tends to reduce memory density and increase the cost of memory.

In addtion to problems with discerning differences in the levels of multi-bit memory elements, these memory elements are often difficult to test. The additional bits stored by a multi-bit memory element may cause the multi-bit memory element to take more time to test than some single-bit memory elements. This extra test time may delay the manufacture or use of multi-bit memory elements and add to their cost.

BRIEF DESCRIPTION OF DRAWINGS

FIG. 1 illustrates an electronic device in accordance with an embodiment of the invention;

FIG. 2 illustrates a memory device in accordance with an embodiment of the invention;

FIG. 3 illustrates a memory array in accordance with an embodiment of the invention;

FIG. 4 illustrates a memory element in accordance with an embodiment of the invention;

FIG. 5 illustrates I-V traces of memory elements storing different values, in accordance with an embodiment of the invention;

FIG. 6 illustrates noise in the bit-line current during a read operation;

FIG. 7 illustrates a quantizing circuit in accordance with an embodiment of the invention;

FIG. 8 illustrates a delta-sigma sensing circuit in accordance with an embodiment of the invention;

FIGS. 9 and 10 illustrate current flow during operation of the quantizing circuit of FIG. 8;

FIGS. 11-13 illustrate voltages in the quantizing circuit of FIG. 8 when sensing small, medium, and large currents, respectively;

FIG. 14 is a graph of bit-line current versus counter output for the quantizing circuit of FIG. 8;

FIG. 15 is a graph of counter versus quantizing circuit output in accordance with an embodiment of the invention;

FIG. 16 illustrates a memory device with a built-in, self-test module in accordance with an embodiment of the invention;

FIG. 17 illustrates details of the built-in, self-test module in the memory device of FIG. 16;

FIG. 18 illustrates a linear-feedback shift register in the built-in, self-test module of FIG. 17;

FIG. 19 illustrates an example of a self-test process, which may be executed by the memory device of FIG. 16; and

FIG. 20 illustrates an example of a system including the memory devices of FIGS. 2 and 16.

DETAILED DESCRIPTION OF SPECIFIC EMBODIMENTS

Various embodiments of the present invention are described below. In an effort to provide a concise description of these embodiments, not all features of an actual implementation are described in the specification. It should be appreciated that in the development of any such actual implementation, as in any engineering or design project, numerous implementation-specific decisions must be made to achieve the developers’ specific goals, such as compliance with system-related and business-related constraints, which may vary from one implementation to another. Moreover, it should be appreciated that such a development effort might be complex and time consuming but would nevertheless be a routine undertaking of design, fabrication, and manufacture for those of ordinary skill having the benefit of this disclosure.

Some of the subsequently described embodiments may address one or more of the problems with conventional sense amplifiers discussed above. Some embodiments include a quantizing circuit configured to detect small differences in voltages and/or currents. As explained below, the quantizing circuit may sample the measured electrical parameter on multiple occasions and filter, e.g., average or sum, the samples to reduce the impact of noise. As a result, in some embodiments, the quantizing circuit may resolve small differences between voltage or current levels in multi-bit memory elements and/or light sensors, which may allow circuit designers to increase the number of bits stored per memory element and/or the sensitivity of an imaging device.

Certain embodiments described below may include a built-in, self-test module that may mitigate certain problems with testing memory devices, including single-bit and multi-bit
memory address. The control circuitry 28 may then convert the target address into a row address and a column address. In other embodiments, the illustrated memory elements 64 may include an imaging device 13 having the quantizing circuits discussed below. The data locations may be formed on an integrated semiconductor device (e.g., a device formed on a single crystal of silicon) that also includes the other components of the memory device 12 (or imaging device 13).

In some embodiments, the illustrated memory elements 64 are flash memory devices. The operation of the flash memory elements is described further below with reference to FIGS. 4 and 5. It should be noted that, in other embodiments, the memory elements 64 may include other types of volatile or nonvolatile memory. For example, the memory elements 64 may include a resistive memory, such as a phase change memory or magnetoresistive memory. In another example, the memory elements 64 may include a capacitor, such as a stacked or trench capacitor. Some types of memory elements 64 may include an access device, such as a transistor or a diode associated with each of the memory elements 64, or the memory elements 64 may not include an access device, for instance in a cross-point array.

FIG. 2 depicts a block diagram of an embodiment of the memory device 12. The illustrated memory device 12 may include a memory array 14, a quantizing circuit 16, a column decoder 18, a column address latch 20, row drivers 22, a row decoder 24, row address latches 26, and control circuitry 28. As described below with reference to FIG. 3, the memory array 14 may include a matrix of memory elements arranged in rows and columns. As will be appreciated, the imaging device 13 (FIG. 1) may include similar features except that in the case of an imaging device 13, the array 14 might comprise an array of imaging elements, such as complementary-metall-oxide semiconductor (CMOS) imaging elements or charge coupled devices (CCDs).

When accessing the memory elements, the control circuitry may receive a command to read from or write to a target memory address. The control circuitry 28 may then convert the target address into a row address and a column address. In the illustrated embodiment, the row address bus 30 transmits the row address to the row address latches 26, and a column address bus 32 transmits column address to the column address latches 20. After an appropriate settling time, a row address strobe (RAS) signal 34 (or other controlling clock signal) may be asserted by the control circuitry 28, and the row address latches 26 may latch the transmitted row address. Similarly, the control circuitry 28 may assert a column address strobe 36, and the column address latches 20 may latch the transmitted column address.

FIG. 4 illustrates a circuit 66 that models the operation of an arbitrarily selected memory element 64, which is disposed at the intersection of WL3 and BL0. This circuit 66 includes a capacitor 68, a pre-drain resistor 70 (RFD), a post-source resistor 72 (RPS), and a ground 74. The resistors 70 and 72 are connected to the bit-line BLO, in parallel with the memory elements 64. Several of the components of the circuit 66 represent phenomenon affecting the memory elements 64 when it is sensed. The pre-drain resistor 70 generally represents the drain-to-bitline resistance of the memory elements 64 connected to the bit-line above (i.e., up current from) WL3 when these memory elements 64 are turned on, (e.g., during a read operation). Similarly, the post source resistor 72 generally corresponds to the source-to-ground resistance of the memory elements 64 connected to the bit-line below WL3 when the memory element 64 is sensed. The circuit 66 models electrical phenomena associated with reading the memory elements 64 at the intersection of WL3 and BL0.

The operation of the memory elements 64 will now be briefly described with reference to FIGS. 4 and 5. FIG. 5 illustrates one potential relationship between the bit-line current (IBL), the word-line voltage (VWL), and the voltage of the floating gate 78 (VFG). As illustrated by FIG. 5, VFG affects the response of the memory element 64 to a given VBL. Decreasing the voltage of the floating gate shifts the I-V curve of the memory elements 64 to the right. That is, the relationship between the bit-line current and a word-line voltage depends on the voltage of the floating gate 78. The memory elements 64 may store data by exploiting this effect.

To write data to the memory elements 64, a charge corresponding to the data may be stored on the floating gate 78. The charge of the floating gate 78 may be modified by applying voltages to the source 82, drain 80, and/or gate 76 such that the resulting electric fields produce phenomenon like Fowler-Nordheim tunneling and/or hot-electron injection near the floating gate 78. Initially, the memory elements 64 may be erased by applying a word-line voltage designed to drive
Electrons off of the floating gate \( G \). In some embodiments, an entire column or block of memory elements \( M \) may be erased generally simultaneously. Once the memory elements \( M \) are erased, the gate \( G \) voltage may be manipulated to drive a charge onto the floating gate \( G \) that is indicative of a data value. After the write operation ends, the stored charge may remain on the floating gate \( G \) (i.e., the memory elements \( M \) may store data in a nonvolatile fashion).

As illustrated by FIG. 5, the value stored by the memory element \( M \) may be read by applying a voltage, \( V_{AG} \), to the gate \( G \) and quantizing (e.g., categorizing) a resulting bit-line current, \( I_{B} \). Each of the I-V traces depicted by FIG. 5 correspond to a different charge stored on the floating gate, \( V_{FG} \), which should not be confused with the voltage that is applied to the gate, \( V_{G} \). The difference in floating gate \( G \) voltage, \( V_{FG} \), between each I-V trace is an arbitrarily selected scaling factor \( x \). The illustrated I-V traces correspond to eight-different data values stored by the memory element \( M \), with a \( V_{FG} \) of 0x representing a binary data value of 000, a \( V_{FG} \) of 1x representing a binary data value of 001, and so on through \( V_{FG} \) of 7x, which represents a binary data value of 111. Thus, by applying a voltage to the gate \( G \) and measuring the resulting bit-line current, the charge stored on the floating gate \( G \) may be sensed, and the stored data may be read.

The accuracy with which the bit-line current is quantized may affect the amount of data that a designer attempts to store in each memory element \( M \). For example, in a system with a low sensitivity, a single bit may be stored on each memory element \( M \). In such a system, a floating gate voltage \( V_{FG} \) of 0x may represent a binary value of 0, and a floating gate voltage \( V_{FG} \) of \(-7x\) may represent a binary value of 1. Thus, the difference in floating gate voltages \( V_{FG} \) corresponding to different data values may be relatively large, and the resulting differences and bit-line currents for different data values may also be relatively large. As a result, even low-sensitivity sensing circuitry may quantize (e.g., discern) these large differences in bit-line current during a read operation. In contrast, high-sensitivity sensing circuitry may facilitate storing more data in each memory element \( M \). For instance, if the sensing circuitry can distinguish between the eight different I-V traces depicted by FIG. 5, then the memory elements \( M \) may store three bits. That is, each of the eight different charges stored on the floating gate \( G \) may represent a different three-bit value: 000, 001, 010, 011, 100, 101, 110, or 111. Thus, the circuitry that precisely quantizes the bit-line current \( I_{B} \) may allow a designer to increase the amount of data stored in each memory element \( M \).

However, as mentioned above, a variety of effects may interfere with accurate measurement of the bit-line current. For instance, the position of the memory elements \( M \) along a bit-line may affect \( R_{PD} \) and \( R_{PG} \), which may affect the relationship between the word-line voltage \( V_{WP} \) and the bit-line current \( I_{B} \). To illustrate these effects, FIG. 6 depicts noise on the bit-line while reading from the memory element \( M \). As illustrated, noise in the bit-line current \( I_{B} \) may cause the bit-line current \( I_{B} \) to fluctuate. Occasionally, the fluctuation may be large enough to cause the bit-line current \( I_{B} \) to reach a level that represents a different stored data value, which could cause the wrong value to be read from the memory elements \( M \). For instance, if the bit-line current is sensed at time \( t \), corresponding to an arbitrarily selected peak, a data value of 100 may be read rather than the correct data value of 011. Similarly, if the bit-line current is sensed at time \( t \), corresponding to an arbitrarily selected local minimum, a data value of 001 may be read rather than a data value of 111. Thus, noise on the bit-line may cause erroneous readings from memory elements \( M \).

FIG. 7 depicts a quantizing circuit \( Q \) that may tend to reduce the likelihood of an erroneous reading. The illustrated quantizing circuit \( Q \) includes an analog-to-digital converter \( A/D \) and a digital filter \( D \) connected to each of the bit-lines \( B \) and \( D \), respectively. Each bit-line \( B \), \( D \), \( E \), and \( F \) may connect to a different analog-to-digital converter \( A/D \) and digital filter \( D \). The digital filters \( D \), in turn, may connect to an input/output bus \( I/O \), which may connect to a column decoder \( CD \), a column address latch \( CAL \), and/or control circuitry \( CC \) (see FIG. 2).

In operation, the quantizing circuit \( Q \) may quantize (e.g., digitize) analog signals from the memory elements \( M \) in a manner that is relatively robust to noise. As explained below, the quantizing circuit \( Q \) may do this by converting the analog signals into a bit-stream and digitally filtering high-frequency components from the bit-stream.

The analog-to-digital converter \( A/D \) may be a one-bit, analog-to-digital converter or a multi-bit, analog-to-digital converter. In the present embodiment, an analog-to-digital converter \( A/D \) receives an analog signal from the memory element \( M \). Thus, a bit-line current \( I_{B} \) or a bit-line voltage \( V_{B} \) and outputs a bit-stream that represents the analog signal. The bit-stream may be a one-bit, serial signal with a time-averaged value that generally represents the time-averaged value of the analog signal from the memory element \( M \). That is, the bit-stream may fluctuate between values of zero and one, but its average value, over a sufficiently large period of time, may be proportional to the average value of the analog signal from the memory element \( M \). In certain embodiments, the bit-stream from the analog-to-digital converter \( A/D \) may be a pulse-density modulated (PDM) version of the analog signal. The analog-to-digital converter \( A/D \) may transmit the bit-stream to the digital filter \( D \) on a bit-stream signal path \( SB \).

The digital filter \( D \) may digitally filter high-frequency noise from the bit-stream. To this end, the digital filter \( D \) may be a low-pass filter, such as a counter, configured to average (e.g., integrate and divide by the sensing time) the bit-stream over a sensing time, i.e., the time period over which the memory element \( M \) is read. (Alternatively, in some embodiments, the digital filter \( D \) is configured to integrate the bit-stream without dividing by the sensing time.) As a result, the digital filter \( D \) may output a value that is representative of both the average value of the bit-stream and the average value of the analog signal from the memory element \( M \). In some embodiments, the digital filter \( D \) is a counter, and the cut-off frequency of the digital filter \( D \) may be selected by adjusting the duration of the sensing time. In the present embodiment, increasing the sensing time will lower the cut-off frequency. That is, the frequency response of the digital filter \( D \) may be modified by adjusting the period of time over which the bit-stream is integrated and/or averaged before outputting a final value. The frequency response of the digital filter \( D \) is described further below with reference to FIG. 15. For multi-bit memory elements \( M \), the output from the digital filter \( D \) may be a multi-bit binary signal, e.g., a digital word that is transmitted serially and/or in parallel.

Advantageously, in certain embodiments, the quantizing circuit \( Q \) may facilitate the use of multi-bit memory elements \( M \). As described above, in traditional designs, the number of discrete data values that a memory element \( M \) stores may be limited by sense amps that react to noise. In contrast, the quantizing circuit \( Q \) may be less susceptible to noise, and, as a result, the memory elements \( M \) may be configured to store additional data. Without the high frequency noise, the intervals between signals representative of different data values may be made smaller, and the number of data values stored by a given memory element \( M \) may be increased. Thus, benefi-
cially, the quantizing circuit 16 may read memory elements 64 that store several bits of data, e.g., 2, 3, 4, 5, 6, 7, 8, or more bits per memory element 64.

Although the quantizing circuit 16 may sense the signal from the memory element 64 over a longer period of time than conventional designs, the overall speed of the memory device 12 may be improved. As compared to a conventional device, each read or write operation of the memory device 12 may transfer more bits of data into or out of the memory element 64. As a result, while each read or write operation may take longer, more data may be read or written during the operation, thereby improving overall performance. Further, in some memory devices 12, certain processes may be performed in parallel with a read or write operation, thereby further reducing the overall impact of the longer sensing time. For example, in some embodiments, the memory array 14 may be divided into banks that operate at least partially independently, so that, while data is being written or read from one bank, another bank can read or write data in parallel.

FIG. 8 illustrates details of one implementation of the quantizing circuit 16. In this embodiment, the digital filter 90 is a counter, and the analog-to-digital converter 88 is a first-order delta-sigma modulator. The illustrated delta-sigma modulator 88 may include a latched comparator 96, a capacitor 98, and a switch 100. In other embodiments, other types of digital filters and analog-to-digital converters may be employed, such as those described below in reference to FIG. 16.

As illustrated, an input of the counter 90 may connect to the bit-stream signal path 94, which may connect to an output of the comparator 96. The output of the comparator 96 may also connect to a gate of the switch 100 by a feedback signal path 102. The output terminal (e.g., source or drain) of the switch 100 may connect in series to one of the bit-lines 38, 40, 42, 44, or 46, and the input terminal of the switch 100 may connect to a reference current source 104. One plate of the capacitor 98 may connect to one of the bit-lines 38, 40, 42, 44, or 46, and the other plate of the capacitor 98 may connect to ground.

The illustrated counter 90 counts the number of clock cycles that the bit-stream 94 is at a logic high value or logic low value during the sensing time. The counter may count up or count down, depending on the embodiment. In some embodiments, the counter 90 may do both, counting up one for each clock cycle that the bit-stream has a logic high value and down one for each clock cycle that the bit-stream has a logic low value. Output terminals (DO-DS) of the counter 90 may connect to the input/output bus 92 for transmitting the count. The counter 90 may be configured to be reset to zero or some other value when a reset signal is asserted. In some embodiments, the counter 90 may be a series connection of D-flip-flops, e.g., D-flip-flops having SRAM or other memory for storing an initial value and/or values to be written to the memory element 64.

In the illustrated embodiment, the clocked comparator 96 compares a reference voltage (V_{REF}) to the voltage of one of the bit-lines 38, 40, 42, 44, or 46 (V_{BL}), which may be generally equal to the voltage of one plate of the capacitor 98. The comparator 96 may be clocked (e.g., falling and/or rising edge triggered), and the comparison may be performed at regular intervals based on the clock signal, e.g., once per clock cycle. Additionally, the comparator 96 may latch, i.e., continue to output values (V_{FB}) between comparisons. Thus, when the clock signals the comparator 96 to perform a comparison, if V_{BL} is less than V_{REF}, then the comparator 96 may latch its output to a logic low value, as described below in reference to FIG. 9. Conversely, if V_{BL} is greater than V_{REF}, then the comparator 96 may latch a logic high value on its output, as described below in reference to FIG. 10. As a result, the illustrated comparator 96 outputs a bit-stream that indicates whether V_{BL} is larger than V_{REF}, where the indication is updated once per clock cycle.

Advantageously, in some embodiments, the quantizing circuit 16 may include a single comparator (e.g., not more than one) for each column of multi-level memory elements 64. In contrast, conventional sense amplifiers often include multiple comparators to read from a multi-bit memory cell, thereby potentially increasing device complexity and cost.

The capacitor 98 may be formed by capacitive coupling of the bit-lines 38, 40, 42, 44, and 46. In other designs, this type of capacitance is referred to as parasitic capacitance because it often hinders the operation of the device. However, in this embodiment, the capacitor 98 may be used to integrate differences between currents on the bit-lines 38, 40, 42, 44, or 46 and the reference current to form the bit-stream, as explained further below. In some embodiments, the capacitor 98 may be supplemented or replaced with an integrated capacitor that provides greater capacitance than the “parasitic” bit-line capacitance.

The illustrated switch 100 selectively transmits current I_{REF} from the reference current source 104. In various embodiments, the switch 100 may be a PMOS transistor (as illustrated in FIGS. 8-10) or an NMOS transistor controlled by the V_{FB} signal on the feedback signal path 102.

The operation of the quantizing circuit 16 will now be described with reference to FIGS. 9-12. Specifically, FIGS. 9 and 10 depict current flows in the quantizing circuit 16 when the comparator 96 is latched low and high, respectively. FIG. 11 illustrates V_{BL}, the bit-stream output from the comparator 96, and the corresponding increasing count 110 of the counter 90 for a relatively small bit-line current. FIG. 12 depicts the same voltages when measuring a medium sized bit-line current, and FIG. 13 depicts these voltages when measuring a relatively large bit-line current.

To sense the current through the memory element 64, the illustrated delta-sigma modulator 88 exploits transient effects output a bit-stream representative of the bit-line current I_{BL}. Specifically, the delta-sigma modulator 88 may repeatedly charge and discharge the capacitor 98 with a current divider that subtracts the bit-line current I_{BL} from the reference current I_{REF}. Consequently, a large current through the memory element 64 may rapidly discharge the capacitor 98, and a small current through the memory element 64 may slowly discharge the capacitor 98.

To charge and discharge the capacitor 98, the delta-sigma modulator 88 switches between two states: the state depicted by FIG. 9 (hereinafter “the charging state”) and the state depicted by FIG. 10 (hereinafter “the discharging state”). Each time the delta-sigma modulator 88 transitions between these states, the bit-stream changes from a logic high value to a logic low value or vice versa. The proportion of time that the delta-sigma modulator 88 is in the state illustrated by either FIG. 9 or FIG. 10 may be proportional to the size of the bit-line current I_{BL} through the memory element 64. The larger the bit-line current I_{BL}, the more time that the delta-sigma modulator 88 is in the state illustrated by FIG. 9, rather than the state illustrated by FIG. 10, and the more time that the bit-stream has a logic low value.

Starting with the charging state (FIG. 9), the capacitor 98 may initially accumulate a charge (e.g., become more charged). To this end, the output of the comparator 96 is latched to logic low, which, as mentioned above, may occur when V_{BL} is less than V_{REF}. The logic low may be conveyed to switch 100 by the feedback signal path 102, and the switch 100 may close, thereby conducting the reference current I_{REF}.
through one of the bit-lines 38, 40, 42, 44, or 46, as indicated by
the larger arrows in FIG. 9. A portion of the electrons
flowing through the reference current source 104 may be
accumulated by the capacitor 98, as indicated by the smaller
horizontal arrows, and the remainder may be conducted
through the memory element 64, i.e., the bit-line current $I_{BL}$, as
indicated by the smaller vertical arrows. Thus, the capaci-
tor 98 may accumulate a charge, and $V_{BL}$ may increase.

The comparator 96 and the reference current source 104
may cooperate to charge the capacitor 98 for a discrete num-
ber of clock cycles. That is, when the delta-sigma modulator
88 transitions to the charging state, the delta-sigma modulator
88 may remain in this state for an integer number of clock
cycles. In the illustrated embodiment, the comparator 96, the
output of which is latched, changes state no more than once
per clock cycle, so the switch 100, which is controlled by the
output of the comparator 96, $V_{FB}$, conducts current for a
discrete number of clock cycles. As a result, the reference
current source 104 conducts current $I_{REF}$ through the bit-line
and into the capacitor 98 for an integer number of clock
cycles.

After each clock cycle of charging the capacitor 98, the
delta-sigma modulator 88 may transition from the charging
state to the discharging state, which is illustrated by FIG. 10,
depending on the relative values of $V_{BL}$ and $V_{REF}$. Once per
clock cycle (or at some other appropriate interval, such as
twice per clock cycle), the comparator 96 may compare the
voltage of the capacitor $V_{BL}$ to the reference voltage $V_{REF}$. If
the capacitor 98 has been charged to the point that $V_{BL}$ is
greater than $V_{REF}$, then the output of the comparator 96 may
transition to logic high, as illustrated in FIG. 10. The logic
high signal may be conveyed to the switch 100 by the feed-
back signal path 102, thereby opening the switch 100. As
a result, the reference current source 104 may cease conducting
current through the memory element 64 and into the capacitor
98, and the capacitor 98 may begin to discharge through the
memory element 64.

In the present embodiment, the delta-sigma modulator 88
discharges the capacitor 98 for a discrete number of clock
intervals. After each clock cycle of discharging the capacitor
98, the delta-sigma modulator 88 compares $V_{BL}$ to $V_{REF}$. If
$V_{BL}$ is still greater than $V_{REF}$, then the comparator 96 may
continue to output a logic high signal, i.e., $V_{FB}$ = 1, and the
switch 100 remains open. On the other hand, if enough cur-
rent has flowed out of the capacitor 98 that $V_{BL}$ is less than
$V_{REF}$, then the comparator 96 may output a logic low signal,
i.e., $V_{FB}$ = 0, and the switch 100 may close, thereby transition-
ing the delta-sigma modulator 88 back to the charging state
and initiating a new cycle.

The counter 90 may count the number of clock cycles that
the delta-sigma modulator 88 is in either the charging state or
the discharging state by monitoring the bit-stream signal path
94. The bit-stream signal path 94 may transition back and
forth between logic high and logic low with the output of the
comparator 96, $V_{FB}$, and the counter 90 may increment and/or
decrement a count once per clock cycle (or other appropriate
interval) based on whether the bit-stream is logic high or logic
low. After the sensing time has passed, the counter 90 may
output a signal indicative of the count on output terminals
D0-D5. As explained below, the count may correspond, e.g.,
proportionally, to the bit-line current, $I_{BIU}$. FIGS. 11-13 illustrate voltages $V_{FB}$ and $V_{BL}$ in the quant-
izing circuit 16 when reading data from a memory element
64. Specifically, FIG. 11 illustrates a low-current case, in
which the voltage stored by the memory element 64 is repre-
sented by a relatively low bit-line current. Similarly, FIG. 12
illustrates a medium-current case, and FIG. 13 illustrates a
high-current case. In each of these figures, the ordinate of the
lower trace represents the voltage of the bit-stream signal path
94, $V_{FB}$, and the ordinate of the upper trace illustrates the
bit-line voltage, $V_{BL}$. The abscissa in each of the traces rep-
resents time, with the lower trace synchronized with the upper
trace, and the duration of the time axes is one sensing time
106.

As illustrated by FIG. 11, the counter 90 is initially preset
to zero (or some other appropriate value) by applying a reset
signal. In some embodiments, the delta-sigma modulator 88
may undergo a number of start-up cycles to reach steady-state
operation before initiating the sensing time and resetting the
counter 90. At the beginning of the illustrated read operation,
the delta-sigma modulator 88 is in the charging state, which
charges the capacitor 98 and increases $V_{BL}$, as indicated by
dimension arrow 108. At the beginning of the next clock
cycle, the comparator 96 compares the bit-line voltage to the
reference voltage and determines that the bit-line voltage is
greater than the reference voltage. As a result, the bit-stream
signal path 94 ($V_{FB}$) transitions to a logic high voltage, and
the delta-sigma modulator 88 transitions to the discharging
state. Additionally, the counter 90 increments the count 110
every cycle. In one embodiment, the counter 90 increments the
count 110 by one to account for one clock cycle of the bit-stream
signal 94 holding a logical low value. Next, the charge stored on
the capacitor 98 drains out through the memory element 64, and
the bit-line voltage drops until the comparator 96 determines
that $V_{BL}$ is less than $V_{REF}$, at which point the cycle repeats.

The cycle has a period 112, which may be divided into a
charging portion 114 and a discharging portion 116. Once
during each cycle in the sensing time 106, the count 110
stored in the counter 90 may increase by one. At the end of the
sensing time 106, the counter 90 may output the total count.

A comparison of FIG. 11 to FIGS. 12 and 13 illustrates why
the count 110 correlates with the bit-line current. In FIG. 13,
the high-current case, the stored charge drains from the
capacitor 98 quickly, relative to the other cases, because the
bit-line current $I_{BIT}$ is large and, as a result, the delta-sigma
modulator 88 spends more time in the charging state than the
discharging state. As a result, the bit-stream has a logical low
value for a large portion of the sensing time 106, thereby
increasing the count 110.

The capacitance of the capacitor 98 may be selected with
both the clock frequency and the range of expected bit-line
currents in mind. For example, the capacitor 98 may be large
enough that the capacitor 98 does not fully discharge (e.g.,
saturate) when the bit-line current $I_{BIT}$ is either at its lowest
expected value or at its highest expected value. That is, in
some embodiments, the capacitor 98 generally remains in a
transient state while reading the memory element 64. Simi-
larly, the frequency at which the comparator 96 is clocked
can affect the design of the capacitor 98. A relatively high
frequency clock signal may leave the capacitor 98 with rela-
tively little time to discharge or saturate between clock cycles,
thereby leading a designer to choose a smaller capacitor 98.

Similarly, the size of the reference current may be selected
with the range of expected bit-line currents in mind. Specifi-
cally, in certain embodiments, the reference current is less
than the largest expected bit-line current $I_{BIT}$, so that, in the
case of maximum bit-line current $I_{BIT}$, the capacitor 98 can
draw charge from the reference current while the rest of the
reference current flows through the memory element 64.

FIG. 14 illustrates the relationship between the bit-line
current $I_{BIT}$ and the count for the presently discussed embodi-
ment. As illustrated by FIG. 14, the count corresponds to (e.g.,
proportionally) the bit-line current $I_{BIT}$. This

This
relationship is described by the following equation (Equation 1), in which $N_{ST}$ represents the number of clock cycles during the sensing time:

\[ I_{REF} = \frac{\text{Count}}{N_{ST}} \]

Thus, in the illustrated embodiment, the count corresponds to (e.g., is indicative of) the bit-line current $I_{BIT}$, which corresponds to the value stored by the memory element $64$.

Advantageously, the quantizing circuit $16$ may quantize (e.g., categorize) the bit-line current $I_{BIT}$ as falling into one of a large number of categories, each of which is represented by an increment of the count. In doing so, in some embodiments, the quantizing circuit $16$ may resolve small differences in the bit-line current $I_{BIT}$. The resolution of the quantizing circuit $16$ may be characterized by the following equation (Equation 2), in which $I_{REF}$ represents the smallest resolvable difference in bit-line current $I_{BIT}$, i.e., the resolution of the quantizing circuit $16$:

\[ I_{REF} = \frac{I_{BIT}}{N_{RANGE}} \]

Thus, the resolution of the quantizing circuit $16$ may be increased by increasing the sensing time or the clock frequency or by decreasing $I_{REF}$, which may limit the maximum cell current since $I_{SP}$ is less than $I_{REF}$.

The resolution of the quantizing circuit $16$ may facilitate storing multiple bits in the memory element $64$ or sensing multiple levels of light intensity in an image sensor element. For example, if the quantizing circuit $16$ is configured to quantize (e.g., categorize) the bit-line current $I_{BIT}$ into one of four different levels, then the memory element $64$ may store two-bits of data. If the quantizing circuit $16$ is configured to categorize the bit-line current $I_{BIT}$ into one of eight different current levels, then the memory element $64$ may store three-bits of data. For the present embodiment, the number of bits stored by the memory element $64$ may be characterized by the following equation (Equation 3), in which $N_R$ represents the number of bits stored by a memory element $64$ and $I_{RANGE}$ represents the range of programmable bit-line currents through the memory element $64$:

\[ N_R = \log(I_{RANGE}/I_{REF})/\log 2 \]

In short, in the present embodiment, greater resolution translates into higher density data storage for a given memory element $64$.

FIG. 15 is a graph that illustrates one way in which the counter $90$ may be configured to further reduce the effects of noise. In FIG. 15, the abscissa represents the count, and the ordinate represents the output of the quantizing circuit $16$. In the present embodiment, the three least-significant digits of the count are disregarded as potentially corrupted by noise. That is, D0-D2 (FIG. 8) either do not connect to the input/output bus $92$ or are not interpreted as conveying data that is stored by the memory element $64$. As a result, a range of counter values may represent a single data value stored by the memory element $64$. For example, in the present embodiment, count values ranging from $00\ 0000$ to $00\ 1111$ are construed as representing a data value of $001$. Representing data in this manner may further reduce the effects of noise because, even if noise affects the count, in many embodiments, it would have to affect the count in a consistent manner over a substantial portion of the sensing time to affect the more significant digits of the count. That is, disregarding less significant digits may lower the cutoff frequency of the counter $90$. In other embodiments, fewer, more, or no digits may be truncated from the count as potentially representing noise.
provide the test data to some other intermediate component. The test data may be written to the data location, and after the test data is written, the stored data, which may or may not correspond to the test data depending on whether the data location is functioning properly, may be read from the data location. The read data may then be transmitted to the built-in self-test module, which receives the read data and determines whether it corresponds to the test data that was written to the data locations. If the test data and read data do not correspond, the built-in self-test module may identify the data location from which the data was read as failing the test.

In the event that a data location fails the test, the built-in self-test module may take a variety of actions, depending on the embodiment. For example, the built-in, self-test module may store the address of the failing data location in a look-up table on the memory device or off the memory device. In some embodiments, the memory device may be configured to not write data to addresses in such a look-up table. In another example, the built-in, self-test module may store the test data in a look-up table. In some embodiments, the built-in, self-test module may be configured to transmit statistics about failing data locations, such as a total number of failing data locations, addresses of failing data locations, or addresses of failing data locations, to a network, a memory controller, a quality control database, or external test equipment. In some embodiments, the built-in self-test module may be configured to respond to a failed test by blowing a fuse that disables the failing data location, e.g., by blowing a fuse connected to a wordline or a bit line or signaling that such a fuse should be blown. The built-in self-test module may also be configured to render redundant data locations accessible, e.g., by blowing a fuse or signaling that such a fuse should be blown by other equipment.

FIG. 17 illustrates details of the built-in, self-test module. In this embodiment, the built-in self-test module includes a controller coupled to the one or more lines and a linear-feedback shift register (LFSR) which is described in further detail below with reference to FIG. 18. The illustrated linear-feedback shift register includes a test data output and a reset signal input. As described further below, the linear-feedback shift register may be configured to generate pseudo-random test data, e.g., a sequence or collection of data that approximates properties of random numbers but is substantially or completely determined by a relatively small set of initial values as compared to the sequence or collection of data. In some embodiments, the initial values may determine a value in a sequence of test data, and the test data may include substantially all possible patterns of n bits, excluding the all zero pattern. The linear-feedback shift register may be configured to provide this test data to the controller via the test data output, and the controller may be configured to either provide the test data to a data location or compare this test data with data read from a data location, depending on the portion of a test being executed, as described further below with reference to FIG. 19.

FIG. 18 illustrates an embodiment of the linear-feedback shift register in greater detail. The linear-feedback shift register may include flip-flops and an XOR gate. The flip-flops may be connected to a clock signal and a reset signal. The XOR gate may be connected to the D input of the flip-flops, and the Q outputs of the flip-flops may be connected to the Q outputs of the adjacent flip-flops. The inputs of the XOR gate may be connected to both the Q outputs of the flip-flops and the Q outputs of the flip-flops, and the output of the XOR gate may be connected to the Q inputs of the flip-flops.
to this, in some embodiments, if a current state of the linear-feedback shift register 126 is known, a subsequent state of the linear-feedback shift register 126 can be calculated. It follows then that, when the illustrated linear-feedback shift register 126 is reset, it may subsequently provide substantially the same sequence of pseudo-random test data. As described below, the deterministic behavior of the linear-feedback shift register 126 can be used to identify data locations 64 that fail to store data, e.g., data locations in which the data read from the data location does not correspond to the data written to the data location.

FIG. 19 illustrates an example of a test process 144, which may be executed by certain embodiments of the built-in, self-test module 120 (FIG. 16). The illustrated process 144 begins with providing test data, as illustrated by block 146. Providing test data may include generating test data with, for example, a linear-feedback shift register 126 (FIG. 16), or it may include receiving test data from some other device, such as automated test equipment, or reading test data from internal or external memory. The test data may be digital, e.g., binary, and it may include a sequence of the same value repeated or a sequence of values that vary, e.g., in a linear, cyclical, exponential, polynomial, random, or pseudo-random fashion. In some embodiments, the test data may include a sequence of values that vary in a deterministic fashion such that the test data can be re-generated with a set of initial values.

After providing the test data, the test data may be written to a data location, as illustrated by block 148 (FIG. 19). Writing the test data to a data location may include incrementally adjusting a parameter of the data location and reading the data location until the parameter of the data location corresponds to the test data. Depending on the type of data location, different parameters may be adjusted, such as a change on a floating gate, a magnetic state, or a degree of crystallinity of a phase-change memory element. After the parameter of the data location is adjusted by an increment, the quantizing circuit 16 may read the data location and determine whether the read data corresponds to the test data. To this end, in some embodiments, the test data may be stored temporarily in memory 91 (FIG. 16), such as SRAM, in the quantizing circuit 16, and the quantizing circuit 16 may read the data location 64. If the test data does not correspond to the data read from the data location 64, the parameter of the data location 64 may be adjusted by another increment, and the quantizing circuit 16 may read the data location again after the parameter is adjusted. The cycle of adjusting and reading may be repeated until the data read from the data location 64 corresponds to the test data in memory 91. If, after a number of cycles, the data read from the data location 64 does not correspond to the test data in memory 91, the data location 64 may be designated as failing to receive data.

In certain embodiments, a plurality of data locations may be written to before proceeding to the next step. For example, a data word may be written generally simultaneously to a plurality of data locations connected to a word line or a bit line. In some embodiments, an entire row, column, block, or memory device may be written to before proceeding.

After writing the test data, the data location may be stressed. Stressing the data location might include measuring the likelihood of a data location failing under a worst-case scenario, such as high temperatures, large mechanical stresses, or combinations thereof. The data location may be left to store the test data for a period of time, and during this period, the data location may be exposed to elevated temperatures, e.g., more than 100 degrees above room temperature, mechanical stresses, electromagnetic radiation, or other forms of energy, such as cosmic rays. Or, in some embodiments, the data location may not be stressed during testing.

Next in the process 144, the test data may be read from the data location 64, as illustrated by block 150 (FIG. 19). Reading the test data may include reading the test data with a quantizing circuit, such as the quantizing circuits 16 illustrated by FIG. 8 or 16. In some embodiments, reading may include truncating a portion of a count produced by a counter 90 coupled to a delta sigma modulator 88, as illustrated by FIG. 15. The test data may be provided to the built-in, self-test module 120.

Next, in the present embodiment, it is determined whether the test data written to the data location corresponds to the data read from the data location, as illustrated by block 152. This step may be executed, for example, by the controller 124 in the built-in, self-test module 120 (FIG. 17) or external automated test equipment. To determine whether the data corresponds, the controller 124 may provide a signal that directs some other component, such as the linear-feedback shift register 126, to generate the test data again. Generating the test data again may include resetting the linear-feedback shift register 126 by providing a reset signal 130. The controller 124 may receive pseudo-random test data from the linear-feedback shift register 126, which corresponds to the pseudo-random test data that was previously written, and compare this pseudo-random test data to the data that was read from the data location. If the test data is deterministic, the linear-feedback shift register 126 may provide generally the same sequence of test data as was initially written to the data location. The controller 124 may compare the re-generated test data to the read data and determine whether they correspond, e.g., whether they are the same or whether a certain number of more-significant digits are the same.

In some embodiments, parameters of the memory device 118 may be adjusted in response to the determination in the step illustrated by block 152. For example, data locations 64 may be disabled by, for example, blowing a fuse, or redundant data locations 64 may be enabled, for example by blowing and fuse connected to redundant data locations. In some embodiments, the result of the determination in block 152 may be used to categorize the memory device 118 into one of a variety of categories, such as a failing device; a lower performance device; a higher performance device; a device having certain voltage, power, or speed characteristics; or a device capable of storing some amount of data.

The test process 144 may be repeated after varying certain conditions in the memory device 118. For instance, the size of the increment by which a data location's parameter is adjusted may be decreased or increased between instances of performing the test process 144. In some embodiments, a reference voltage of a delta-sigma modulator may be increased or decreased between instances of performing the test process 144, or a number of bits truncated by a counter may be increased or decreased, or a duration of a sensing time may be increased or decreased. Certain embodiments may attempt to recover failing data locations by increasing the number of bits truncated, increasing the sensing time, or decreasing the increment by which a data location's parameter is adjusted.

In some embodiments, an error-detection module or an error-correction module may be connected to the built-in, self-test module 120 and the data location 64. Such embodiments may encode the test data, and other data, with redundant data that is indicative of the data being written and examine read data for internal consistency between the redundant data and the data that was written. Examples of encoding include a Hamming code or a parity bit.
FIG. 20 depicts an example of a processor-based system 310 that includes the memory device 12 (FIG. 2) or the memory device 118 (FIG. 16). Alternatively or additionally, the system 310 may include the imaging device 13. The system 310 may be any of a variety of types such as a computer, pager, cellular phone, personal organizer, control circuit, etc. In a typical processor-based system, one or more processors 312, such as a microprocessor, control the processing of system functions and requests in the system 310. The processor 312 and other subcomponents of the system 310 may include quantizing circuits, such as those discussed above.

The system 310 typically includes a power supply 314. For instance, if the system 310 is a portable system, the power supply 314 may advantageously include a fuel cell, permanent batteries, replaceable batteries, and/or rechargeable batteries. The power supply 314 may also include an AC adapter, so the system 310 may be plugged into a wall outlet, for instance. The power supply 314 may also include a DC adapter such that the system 310 may be plugged into a vehicle cigarette lighter, for instance.

Various other devices may be connected to the processor 312 depending on the functions that the system 310 performs. For instance, a user interface 316 may be connected to the processor 312. The user interface 316 may include buttons, switches, a keyboard, a light pen, a mouse, a digitizer and stylus, and/or a voice recognition system, for instance. A display 318 may also be connected to the processor 312. The display 318 may include an LCD, an LCD display, a CRT display, a DLP display, a plasma display, an OLED display, LEDs, and/or an audio display, for example. Furthermore, an RF sub-system/baseband processor 320 may also be connected to the processor 312. The RF sub-system/baseband processor 320 may include an antenna that is connected to an RF receiver and to an RF transmitter (not shown). One or more communication ports 322 may also be connected to the processor 312. The communication port 322 may be adapted to be connected to one or more peripheral devices 324 such as a modem, a printer, a computer, or to a network, such as a local area network, remote area network, intranet, or the Internet, for instance.

The processor 312 generally controls the system 310 by implementing software programs stored in the memory. The memory is operably connected to the processor 312 to store and facilitate execution of various programs. For instance, the processor 312 may be connected to the volatile memory 326 which may include Dynamic Random Access Memory (DRAM) and/or Static Random Access Memory (SRAM). The volatile memory 326 is typically large so that it can store dynamically loaded applications and data. As described further below, the volatile memory 326 may be configured in accordance with embodiments of the present invention.

The processor 312 may also be connected to the memory device 12. The memory device 12 may include a read-only memory (ROM), such as an EPROM, and/or flash memory to be used in conjunction with the volatile memory 326. The size of the ROM is typically selected to be just large enough to store any necessary operating system, application programs, and fixed data.

The memory device 10 and volatile memory 326 may store various types of software, such as an operating system or office productivity suite including a word processing application, a spreadsheet application, an email application, and/or a database application. These programs may be stored on a variety of tangible machine readable mediums.

While the invention may be susceptible to various modifications and alternative forms, specific embodiments have been shown by way of example in the drawings and have been described in detail herein. However, it should be understood that the invention is not intended to be limited to the particular forms disclosed. Rather, the invention is to cover all modifications, equivalents, and alternatives falling within the spirit and scope of the invention as defined by the following appended claims.

What is claimed is:

1. A device, comprising:
   a data location;
   a quantizing circuit coupled to the data location; and
   a test module coupled to the quantizing circuit, wherein the test module comprises a built-in, self-test module comprising:
   a controller; and
   a linear-feedback shift register, wherein the linear-feedback shift register generates test data to test the data location;
   wherein the quantizing circuit comprises:
   a digital filter;
   an analog-to-digital converter;
   a switch coupled to the data location; and
   a feedback signal path coupled to the output of the analog-to-digital converter and to the switch.

2. The device of claim 1, wherein the data location comprises a floating gate transistor or a phase-change memory element.

3. The device of claim 1, wherein the digital filter comprises a counter.

4. The device of claim 1, wherein the analog-to-digital converter comprises a delta-sigma modulator.

5. The device of claim 1, wherein the linear-feedback shift register comprises:
   a plurality of flip-flops coupled to one another; and
   an XOR gate having an output coupled to an input of a flip-flop of the plurality of flip-flops.

6. The device of claim 5, wherein the XOR gate comprises two inputs that are each coupled to outputs of another two flip-flops of the plurality of flip-flops.

7. A system, comprising:
   a memory device comprising:
   a plurality of data locations;
   a delta-sigma modulator coupled to the plurality of data locations;
   a switch coupled to the plurality of data locations;
   a feedback signal path coupled to the output of the delta-sigma modulator and to the switch;
   a counter coupled to the delta-sigma modulator; and
   a built-in, self-test module coupled to the plurality of data locations, wherein the built-in, self-test module comprises a linear-feedback shift register configured to generate test data to test the plurality of data locations.

8. The system of claim 7, wherein the plurality of data locations each comprise flash memory, phase-change memory, or magneto-resistive memory.

9. The system of claim 7, wherein the delta-sigma modulator comprises a comparator with an input coupled to the plurality of data locations and an output coupled to the counter.

10. The system of claim 7, wherein the counter comprises memory.

11. The system of claim 7, wherein the linear-feedback shift register comprises three or more DQ flip-flops coupled to one another in series.

12. The system of claim 7, wherein the built-in, self-test module comprises a controller configured to provide test data to the plurality of data locations, receive data read from the
plurality of data locations, and compare the test data to the data read from the plurality of data locations.

13. The system of claim 12, wherein the controller is configured to designate a data location from among the plurality of data locations as failing to store data during a test.

14. A method, comprising:
   generating test data via a linear-feedback shift register,
   writing the test data to a data location;
   reading the test data from the data location with a quantizing circuit comprising a digital filter and an analog-to-digital converter wherein reading comprises truncating a count; and
   determining whether the test data written to the data location corresponds to the test data.

15. The method of claim 14, wherein generating the test data comprises generating pseudo-random test data.

16. The method of claim 14, wherein generating the test data comprises resetting a linear-feedback shift register and providing data from the linear-feedback shift register.

17. The method of claim 14, wherein generating the test data comprises providing the test data from a built-in, self-test module.

18. The method of claim 14, wherein writing the test data comprises:
   storing the test data in memory;
   adjusting a parameter of a data location by an increment;
   comparing data read from the data location to the test data; and
   if the data read from the data location does not correspond to the test data, then adjusting the parameter by another increment.

19. The method of claim 14, wherein reading the test data comprises sensing a charge on a floating gate or sensing a resistance of a resistive memory element.

20. The method of claim 14, wherein determining comprises determining whether the test data is the same as the data read from the data location.

21. The method of claim 14, further comprising generating the test data before writing the test data to the data location and generating the test data a second time after writing the test data to the data location.

22. The method of claim 14, further comprising resetting a linear-feedback shift register.

23. The method of claim 14, comprising adjusting one or more of a reference voltage, a number of bits truncated, and a sensing time duration, or a combination thereof in response to determining whether the test data written to the data location corresponds to the test data.

24. The method of claim 14, comprising stressing the data location.

25. A device, comprising:
   a test circuit, wherein the test circuit comprises a linear-feedback shift register configured to generate test data to test the plurality of data locations;
   a memory element coupled to the test circuit; and
   a quantizing circuit coupled to the memory element, wherein the quantizing circuit comprises:
   a digital filter;
   an analog-to-digital converter;
   a switch coupled to the memory element; and
   a feedback signal path coupled to the output of the analog-to-digital converter and to the switch.

26. The device of claim 25, wherein the test circuit is disposed on a common silicon substrate with the memory element and the quantizing circuit.

27. The device of claim 25, wherein the test circuit is configured to deterministically generate data.

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