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Baker

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(54) INTEGRATORS FOR DELTA-SIGMA MODULATORS

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(51) **Int. Cl.**
H03M 3/00 (2006.01)

(52) **U.S. Cl.** **341/143**; 341/155

(58) **Field of Classification Search** 341/130–155
See application file for complete search history.

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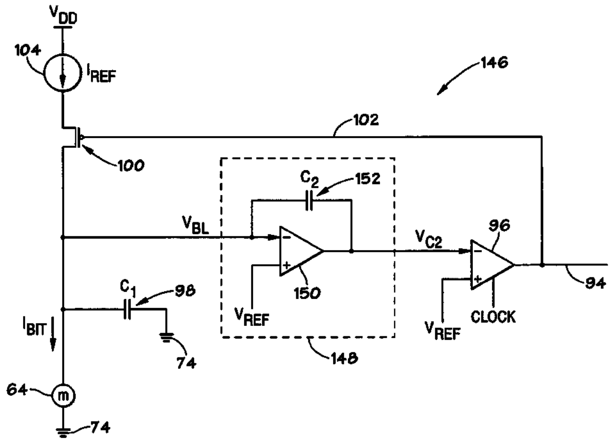
(57) **ABSTRACT**

Methods, systems and devices are disclosed. Among the disclosed devices is an electronic device that, in certain embodiments, includes a plurality of memory elements or imaging elements connected to a bit-line and a delta-sigma modulator connected to the bit-line. The delta-sigma modulator may include an integrator having a differential amplifier.

22 Claims, 15 Drawing Sheets



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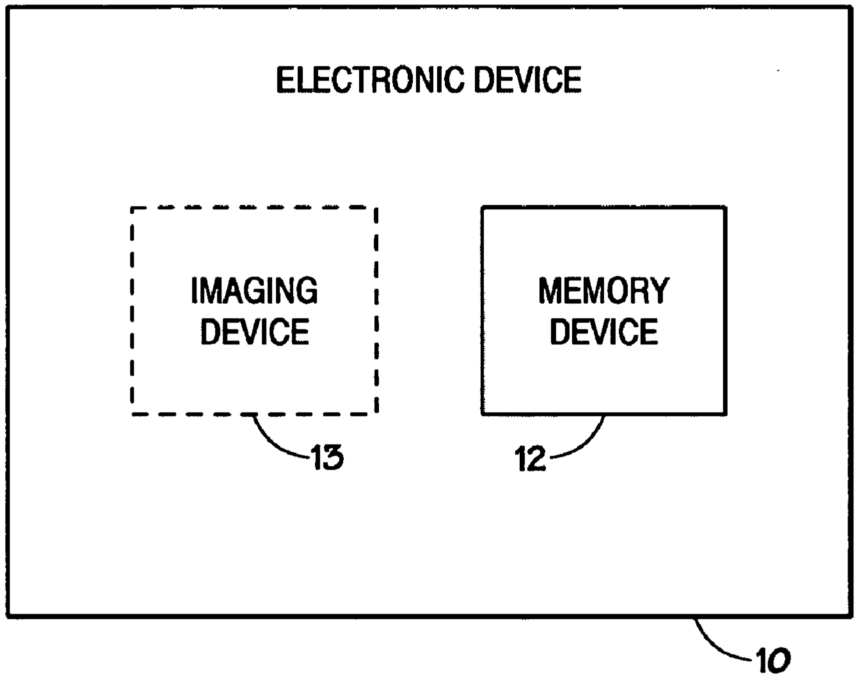

ELECTRONIC DEVICE
IMAGING DEVICE
MEMORY DEVICE
13
12
10

FIG. 1

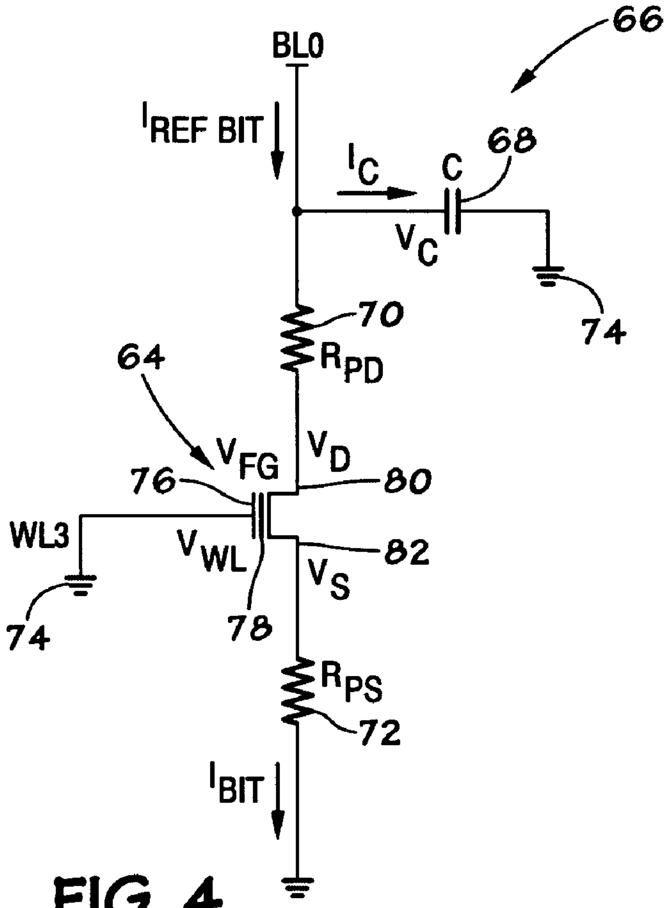

66
BL0
$I_{REF\ BIT}$
I_C
C
68
V_C
74
70
R_{PD}
64
V_{FG}
V_D
76
80
WL3
V_{WL}
82
V_S
74
78
R_{PS}
72
I_{BIT}

FIG. 4

FIG. 2

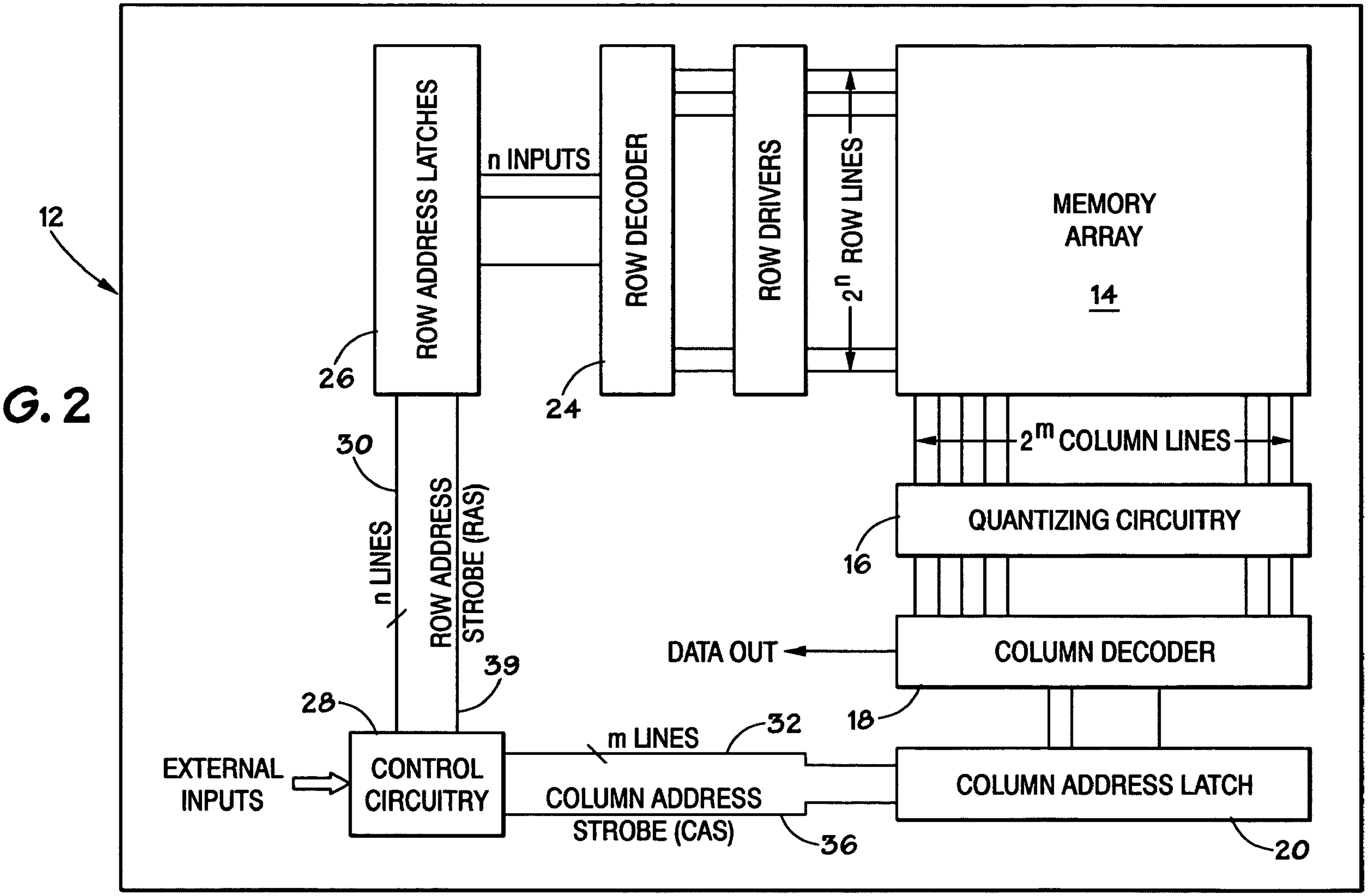

12
ROW ADDRESS LATCHES
26
n INPUTS
ROW DECODER
24
ROW DRIVERS
2^n ROW LINES
MEMORY ARRAY
14
30
n LINES
ROW ADDRESS STROBE (RAS)
39
2^m COLUMN LINES
QUANTIZING CIRCUITRY
16
DATA OUT
COLUMN DECODER
18
28
EXTERNAL INPUTS
CONTROL CIRCUITRY
m LINES
32
COLUMN ADDRESS STROBE (CAS)
36
COLUMN ADDRESS LATCH
20

FIG. 3

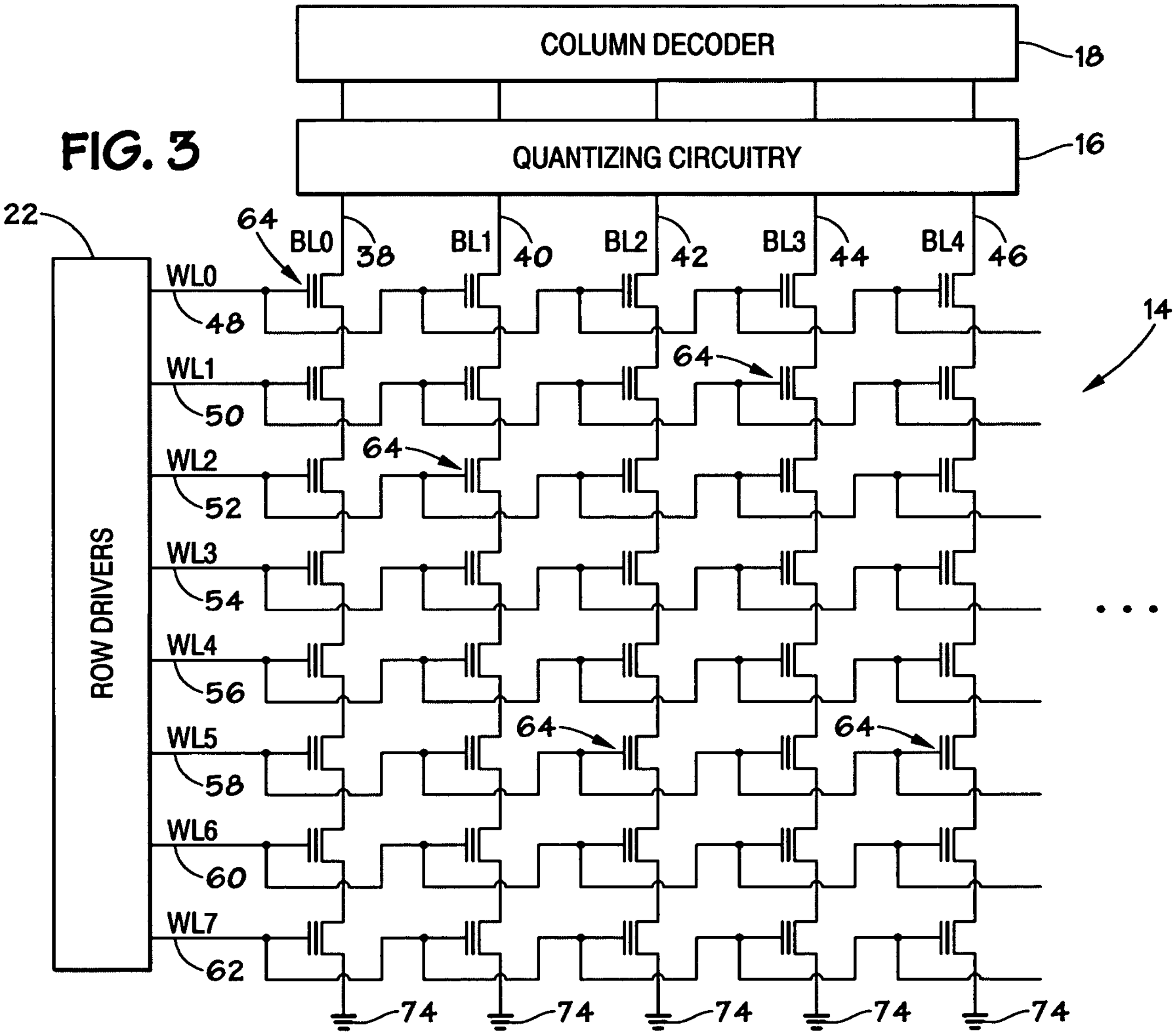

COLUMN DECODER
18
QUANTIZING CIRCUITRY
16
22
ROW DRIVERS
64
BL0
38
BL1
40
BL2
42
BL3
44
BL4
46
14
WL0
48
WL1
50
WL2
52
WL3
54
WL4
56
WL5
58
WL6
60
WL7
62
64
64
64
64
74
74
74
74
74

FIG. 5

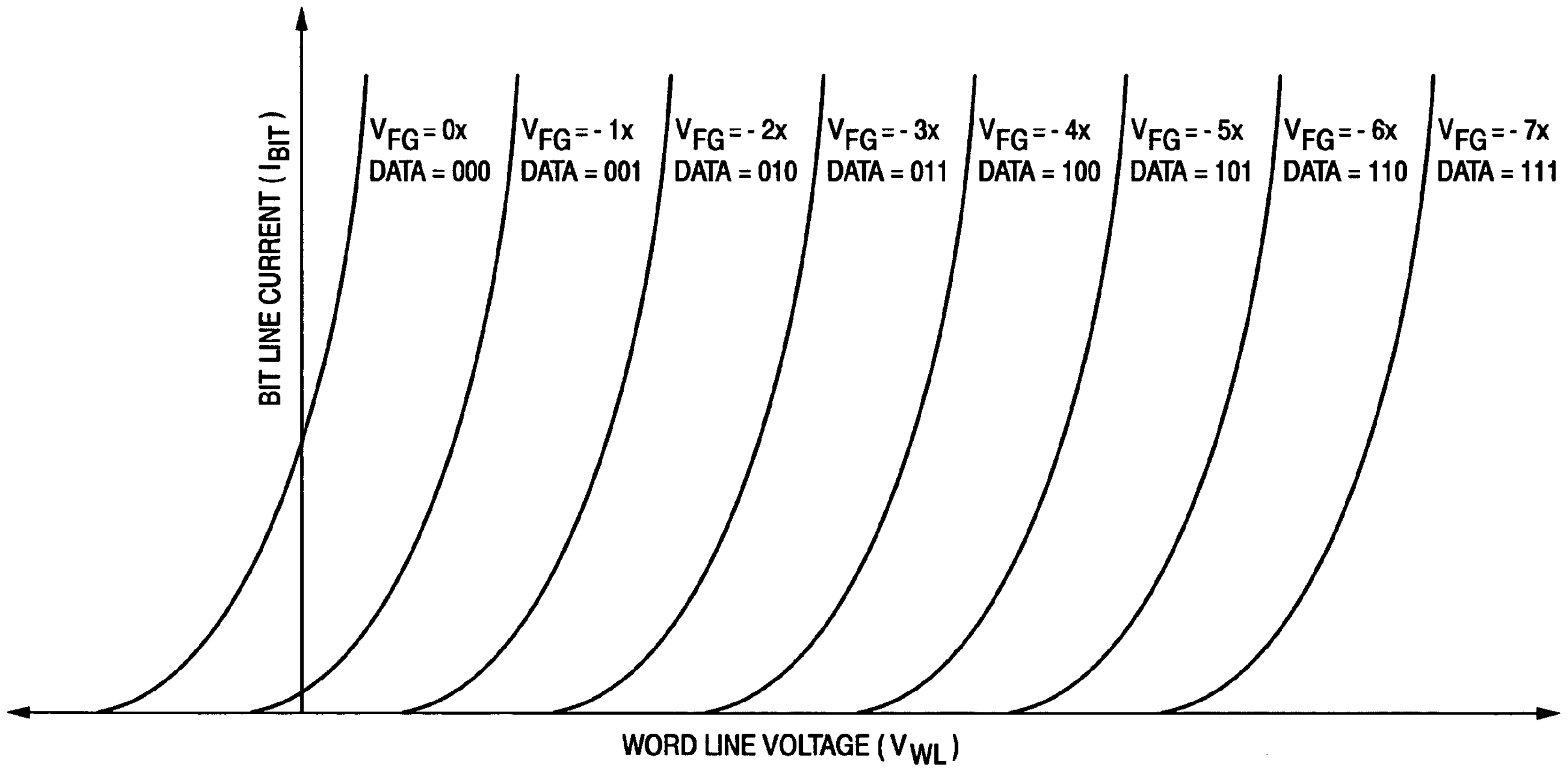
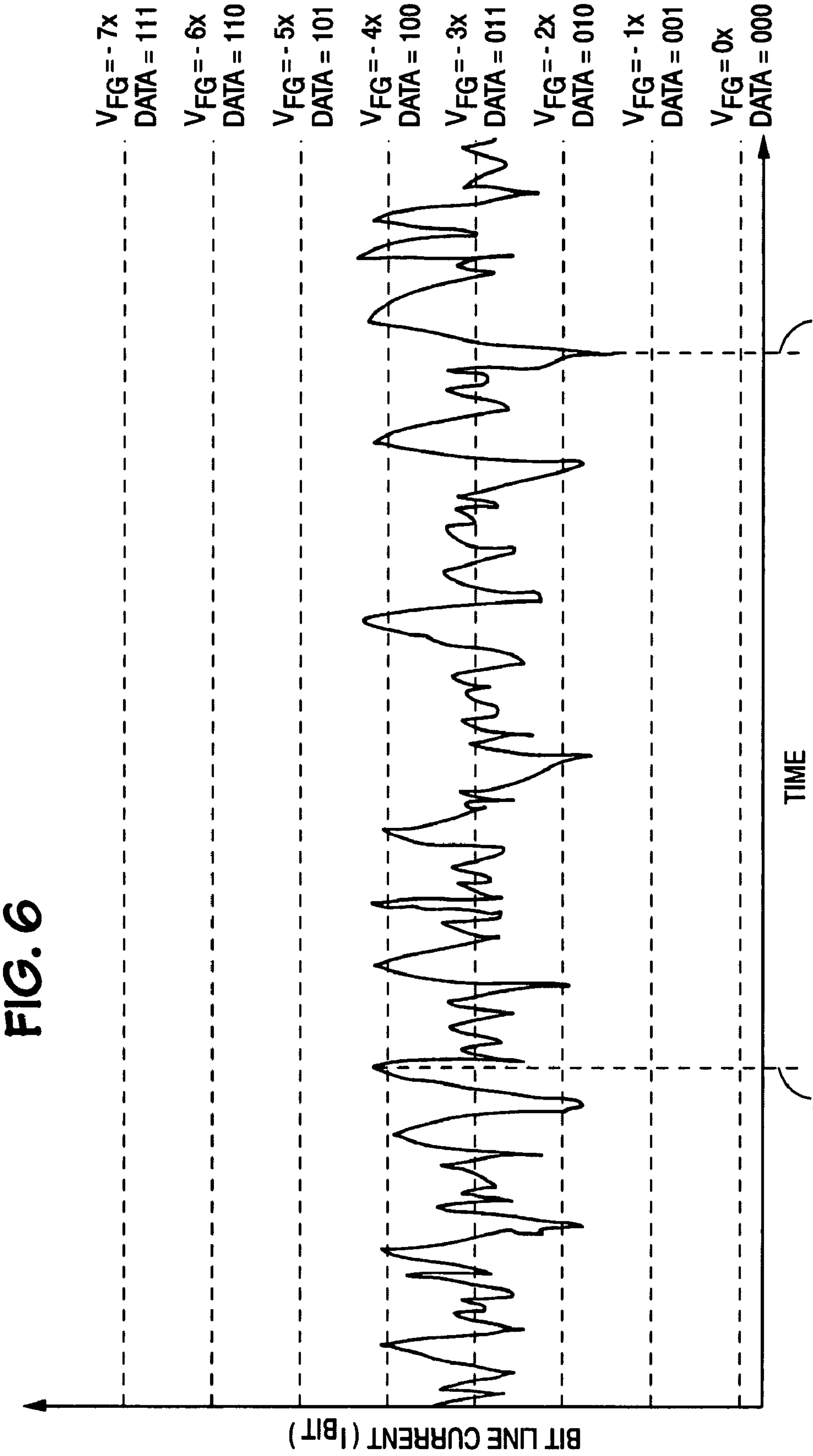

BIT LINE CURRENT (I_{BIT})
V_{FG} = 0x
DATA = 000
V_{FG} = - 1x
DATA = 001
V_{FG} = - 2x
DATA = 010
V_{FG} = - 3x
DATA = 011
V_{FG} = - 4x
DATA = 100
V_{FG} = - 5x
DATA = 101
V_{FG} = - 6x
DATA = 110
V_{FG} = - 7x
DATA = 111
WORD LINE VOLTAGE (V_{WL})

FIG. 6


V_{FG} = - 7x
DATA = 111
V_{FG} = - 6x
DATA = 110
V_{FG} = - 5x
DATA = 101
V_{FG} = - 4x
DATA = 100
V_{FG} = - 3x
DATA = 011
V_{FG} = - 2x
DATA = 010
V_{FG} = - 1x
DATA = 001
V_{FG} = 0x
DATA = 000
86
84
TIME
BIT LINE CURRENT (I_{BIT})

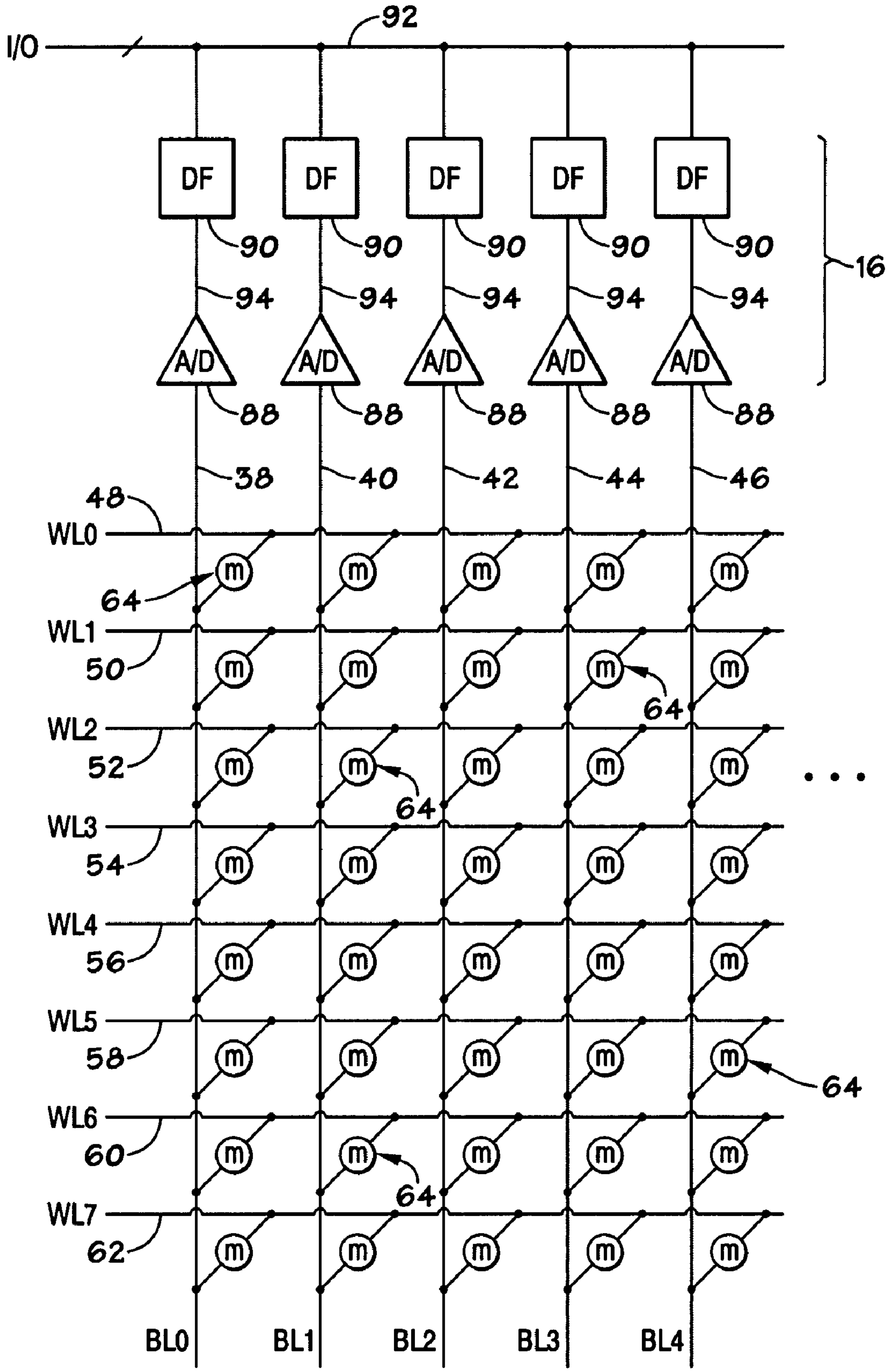

I/O
92
DF
DF
DF
DF
DF
90
90
90
90
90
16
94
94
94
94
94
A/D
A/D
A/D
A/D
A/D
88
88
88
88
88
38
40
42
44
46
48
WL0
64
WL1
50
64
WL2
52
64
WL3
54
WL4
56
WL5
58
64
WL6
60
64
WL7
62
m
. . .
BL0
BL1
BL2
BL3
BL4

FIG. 7

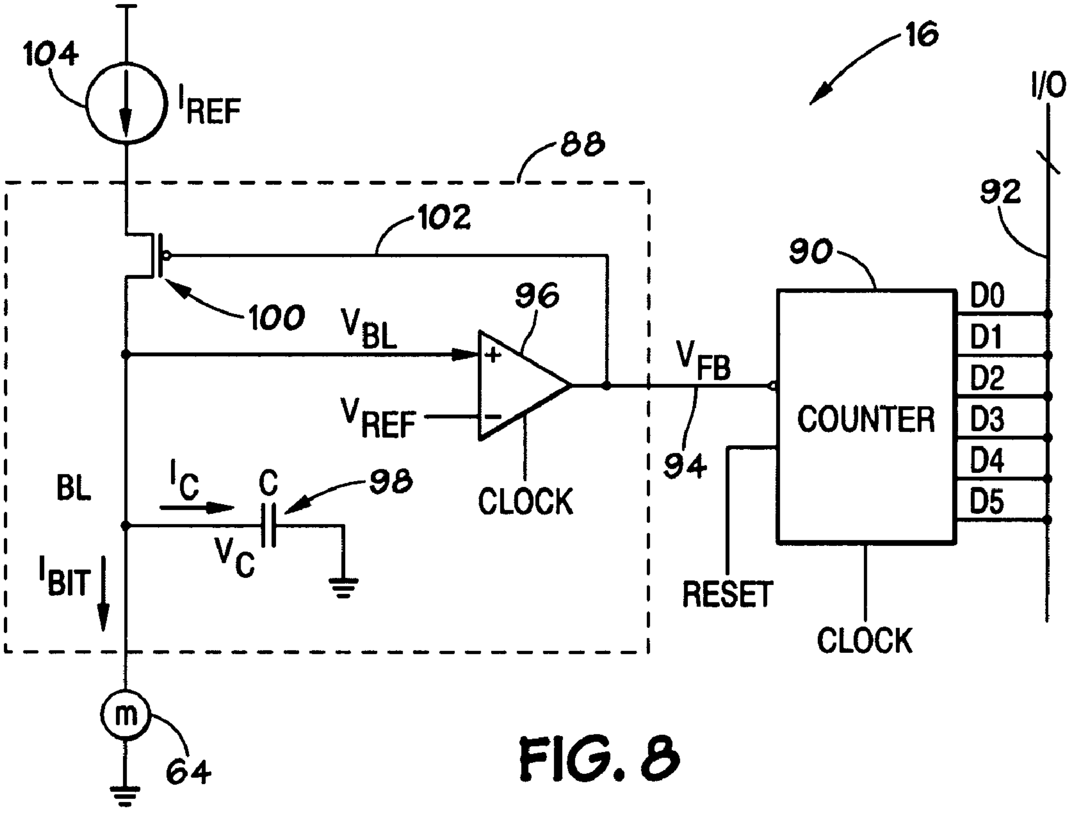

104
I_{REF}
16
I/O
88
102
92
90
100
96
V_{BL}
V_{FB}
V_{REF}
COUNTER
D0
D1
D2
D3
D4
D5
94
BL
I_C
C
98
CLOCK
V_C
I_{BIT}
RESET
CLOCK
m
64

FIG. 8

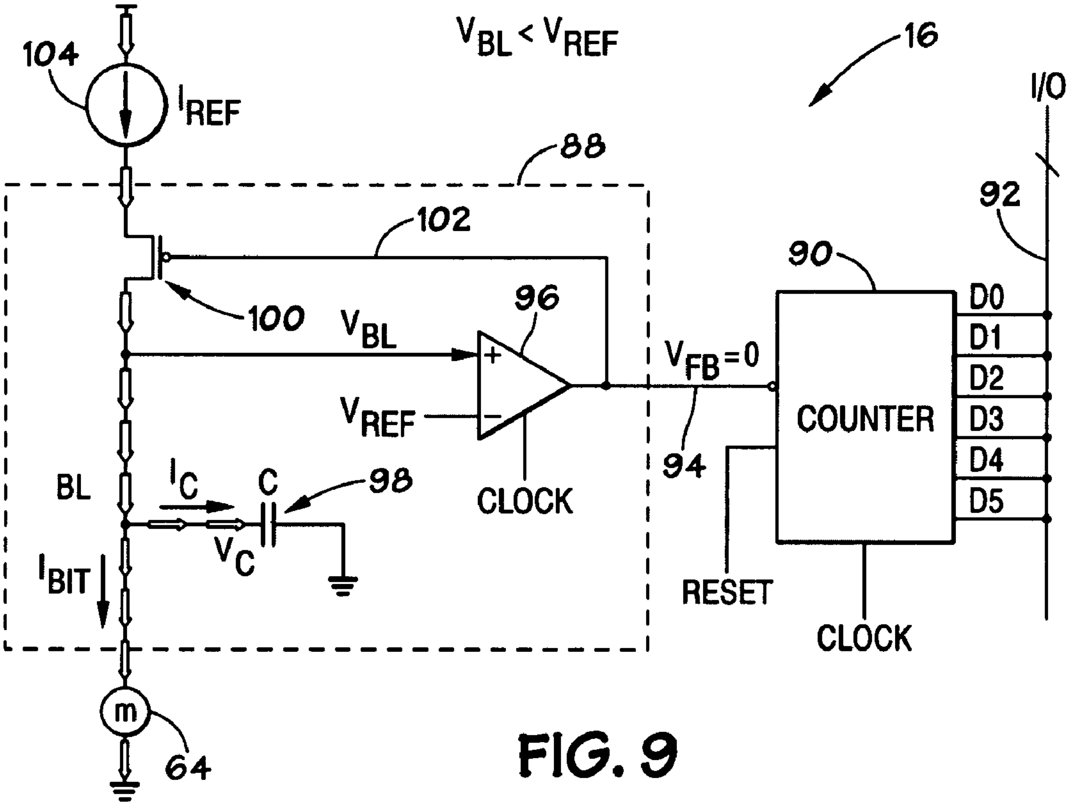

$V_{BL} < V_{REF}$
104
I_{REF}
16
I/O
88
102
92
90
100
96
V_{BL}
$V_{FB}=0$
V_{REF}
COUNTER
D0
D1
D2
D3
D4
D5
94
BL
I_C
C
98
CLOCK
V_C
I_{BIT}
RESET
CLOCK
m
64

FIG. 9

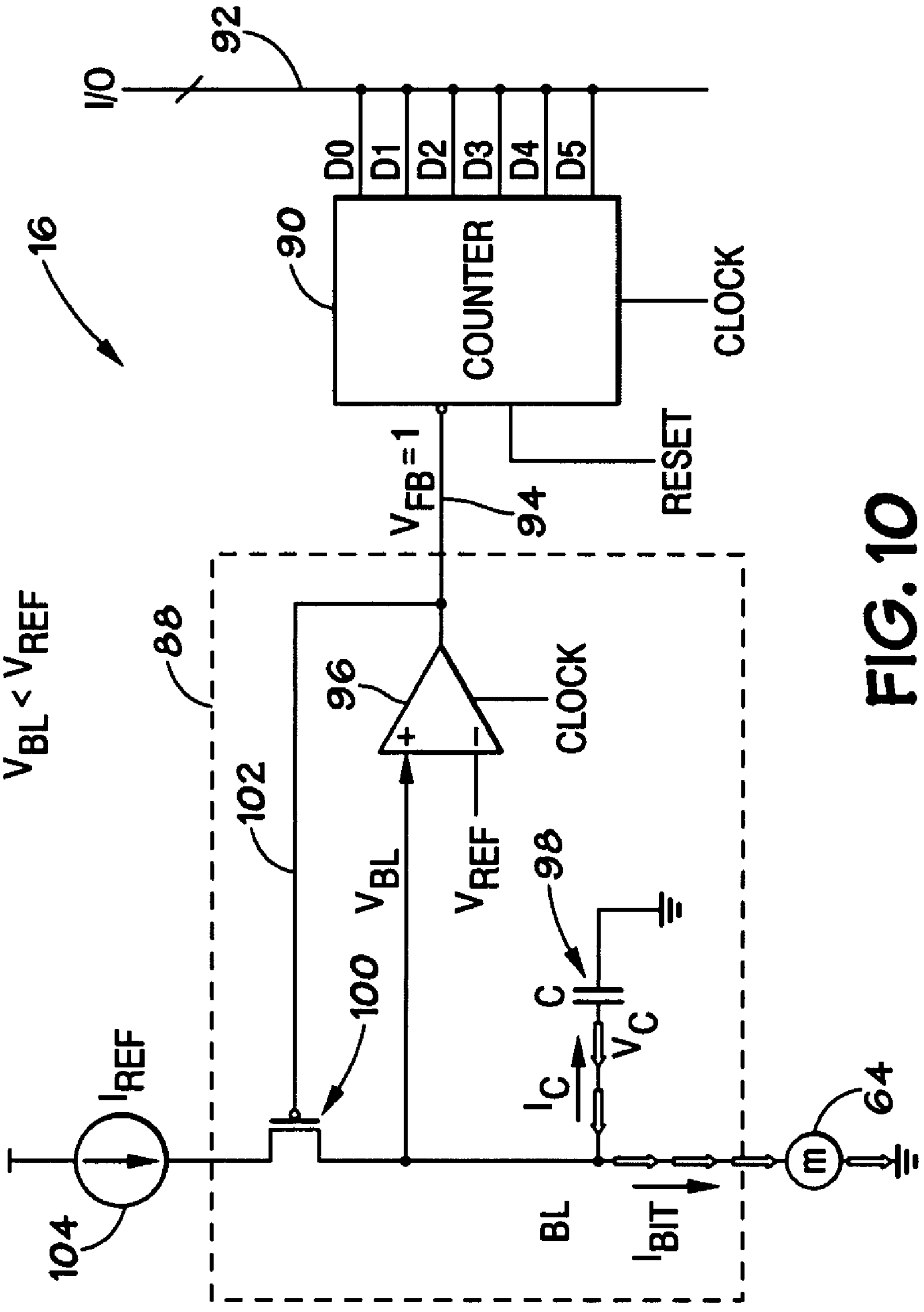

16
I/O
92
D0
D1
D2
D3
D4
D5
90
COUNTER
CLOCK
RESET
$V_{FB}=1$
94
$V_{BL} < V_{REF}$
88
96
+
-
CLOCK
102
V_{BL}
V_{REF}
98
100
C
V_C
I_C
I_{REF}
104
BL
I_{BIT}
m
64

FIG. 10

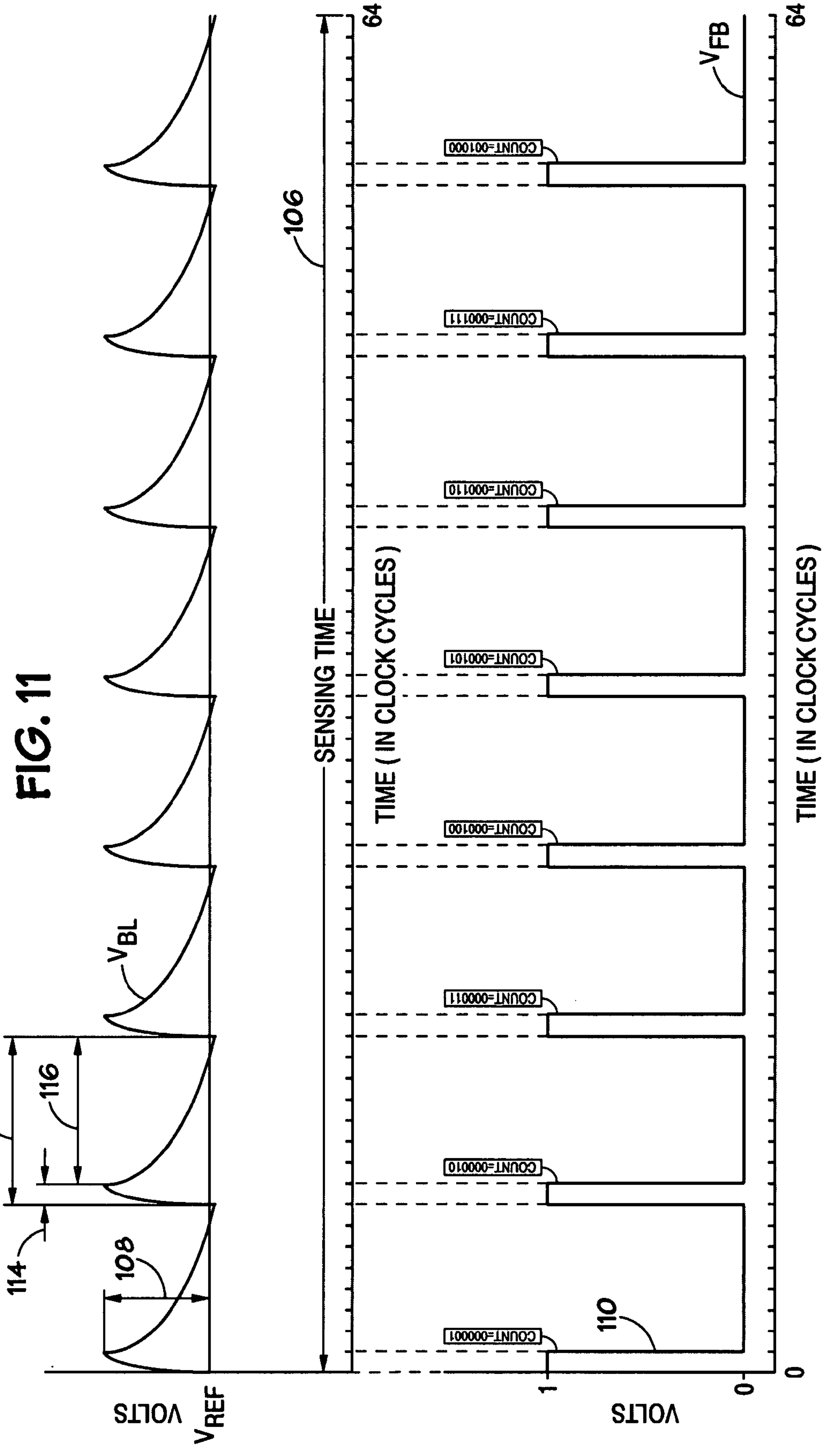


FIG. 11

VOLTS
V_{REF}
V_{BL}
108
114
112
116
SENSING TIME
106
TIME (IN CLOCK CYCLES)
0
64
VOLTS
1
0
110
V_{FB}
COUNT=000001
COUNT=000010
COUNT=000011
COUNT=000100
COUNT=000101
COUNT=000110
COUNT=000111
COUNT=001000
TIME (IN CLOCK CYCLES)
0
64

FIG. 12

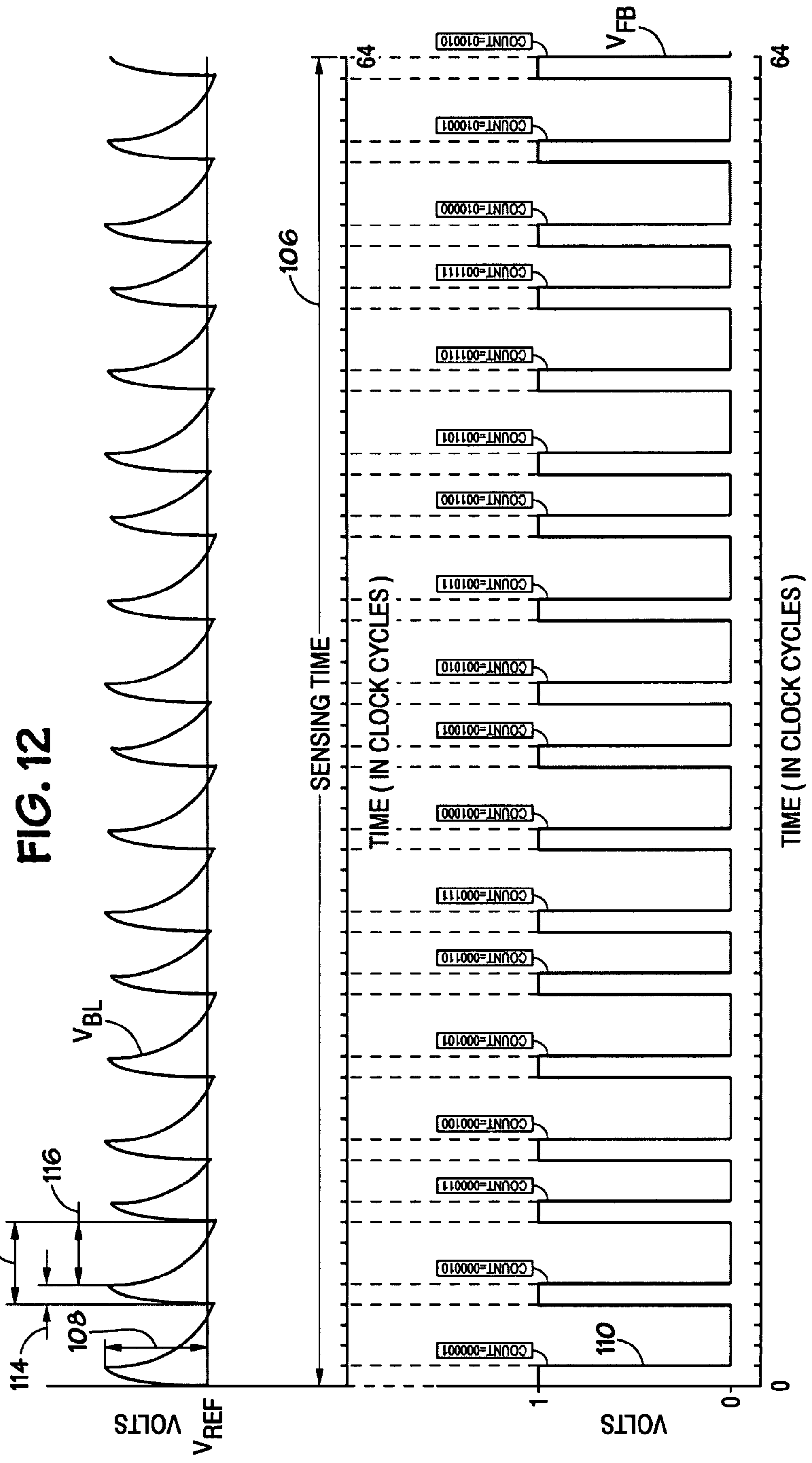

VOLTS
V_{REF}
114
108
112
116
V_{BL}
SENSING TIME
106
TIME (IN CLOCK CYCLES)
0
64
1
0
VOLTS
110
V_{FB}
COUNT=000001
COUNT=000010
COUNT=000011
COUNT=000100
COUNT=000101
COUNT=000110
COUNT=000111
COUNT=001000
COUNT=001001
COUNT=001010
COUNT=001011
COUNT=001100
COUNT=001101
COUNT=001110
COUNT=001111
COUNT=010000
COUNT=010001
COUNT=010010
TIME (IN CLOCK CYCLES)
0
64

FIG. 13

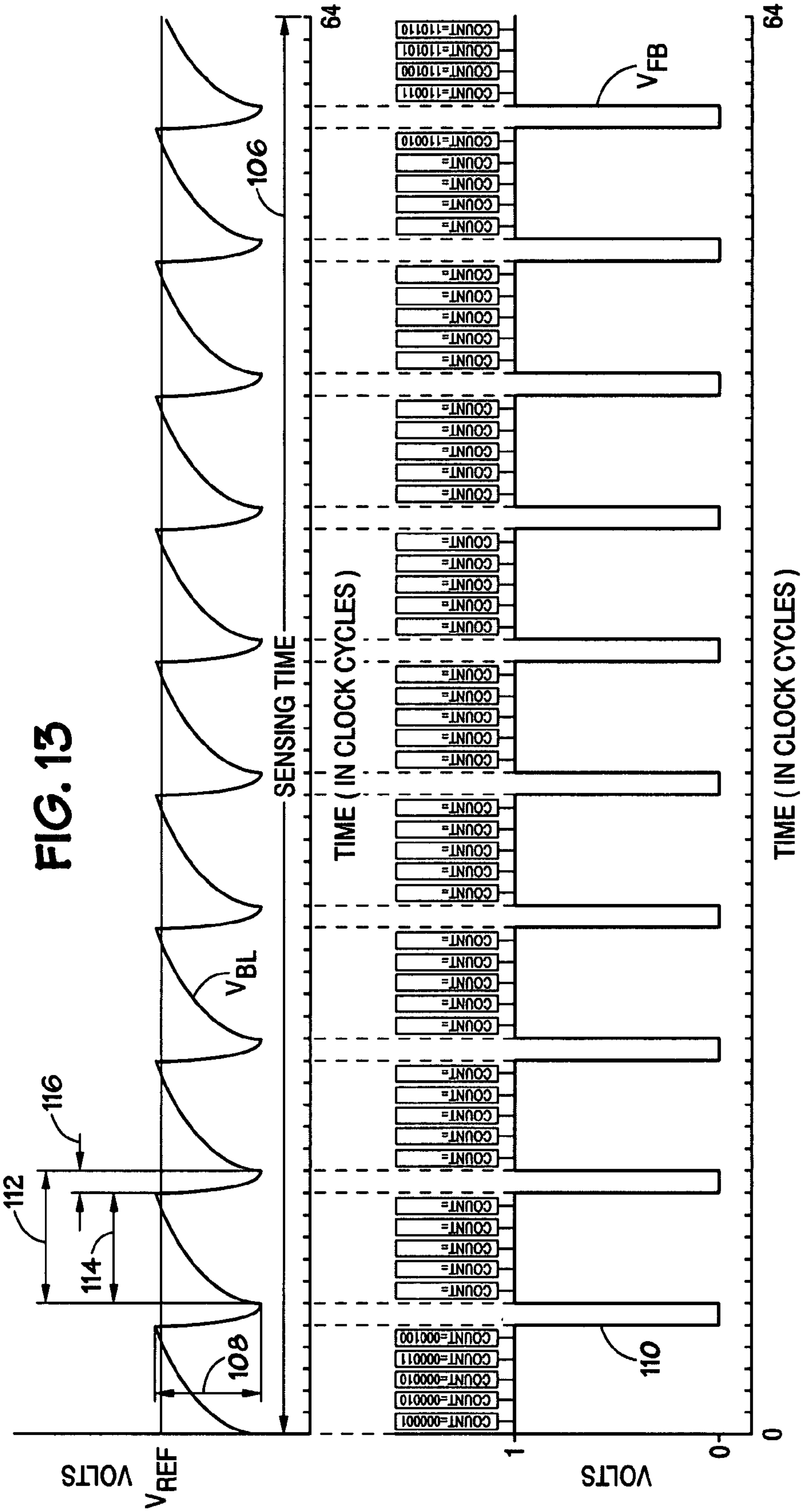

VOLTS
V_{REF}
108
112
114
116
V_{BL}
106
SENSING TIME
TIME (IN CLOCK CYCLES)
0
64
VOLTS
1
0
COUNT=000001
COUNT=000010
COUNT=000010
COUNT=000011
COUNT=000100
COUNT=
COUNT=110010
COUNT=110011
COUNT=110100
COUNT=110101
COUNT=110110
110
V_{FB}
TIME (IN CLOCK CYCLES)
0
64

FIG. 14

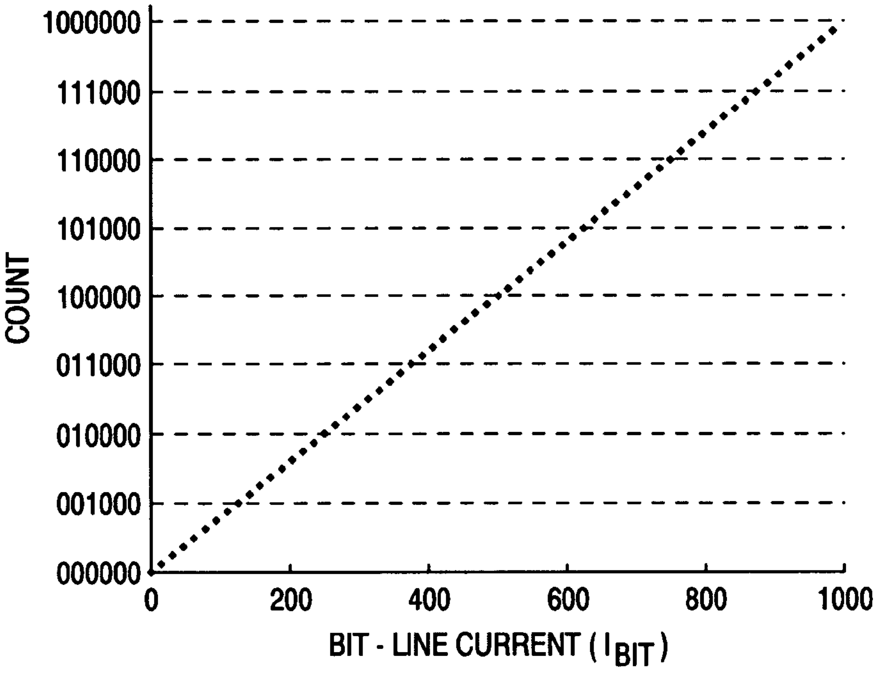
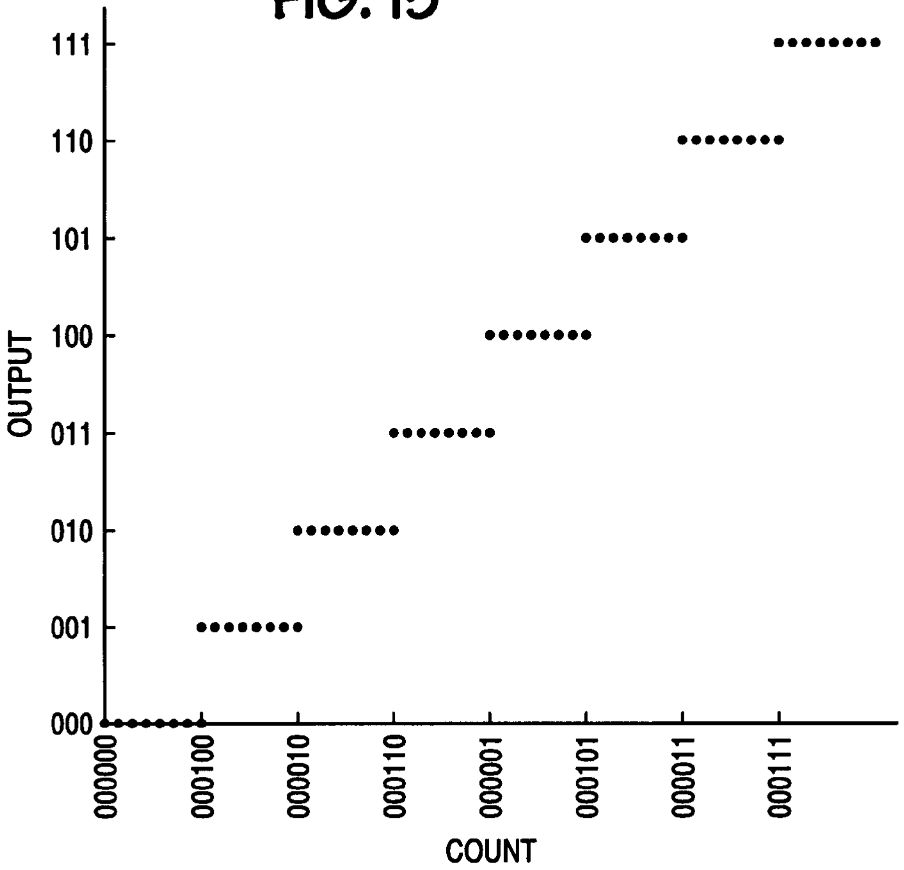

1000000
111000
110000
101000
100000
011000
010000
001000
000000
COUNT
0
200
400
600
800
1000
BIT - LINE CURRENT (I_{BIT})

FIG. 15


111
110
101
100
011
010
001
000
OUTPUT
000000
000100
000010
000110
000001
000101
000011
000111
COUNT

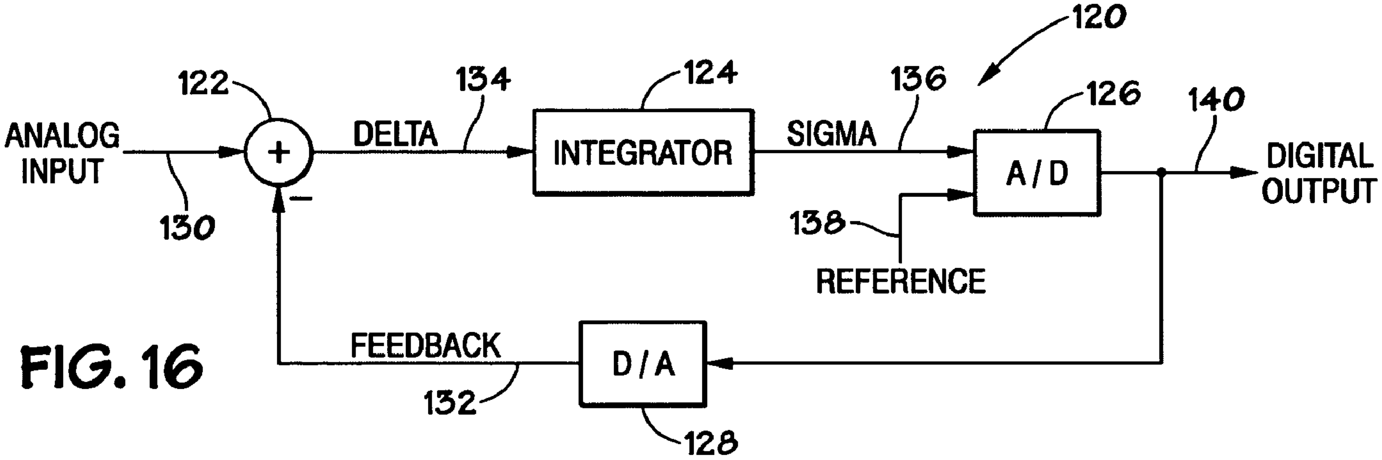

120
122
134
124
136
126
140
ANALOG INPUT
DELTA
INTEGRATOR
SIGMA
A / D
DIGITAL OUTPUT
+
−
130
138
REFERENCE
FEEDBACK
D / A
132
128

FIG. 16

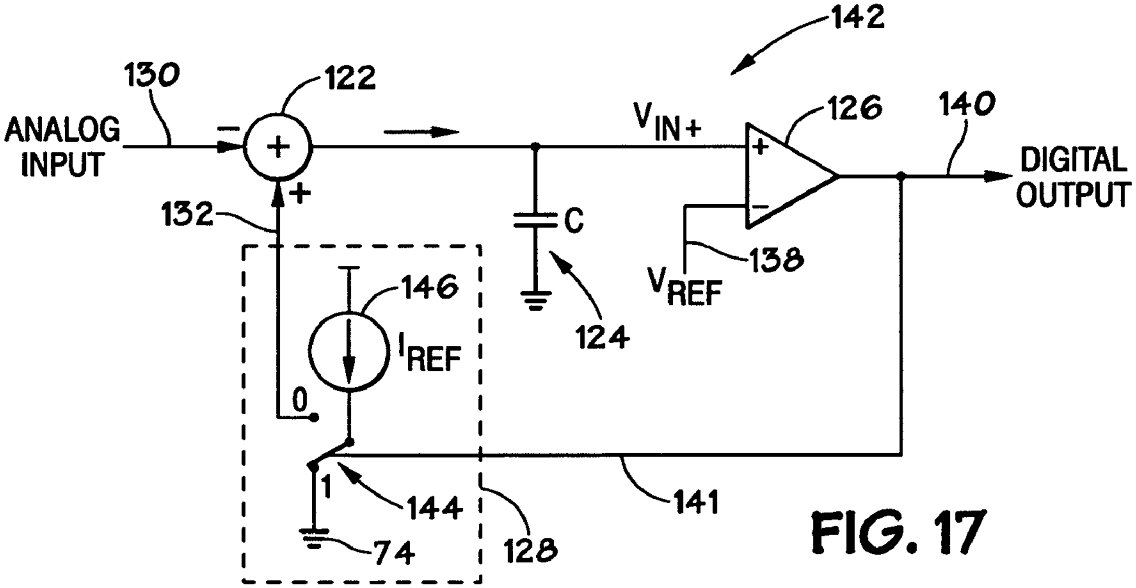

142
130
122
126
140
ANALOG INPUT
−
+
V_{IN+}
+
−
DIGITAL OUTPUT
132
C
138
V_{REF}
146
I_{REF}
124
0
1
144
141
74
128

FIG. 17

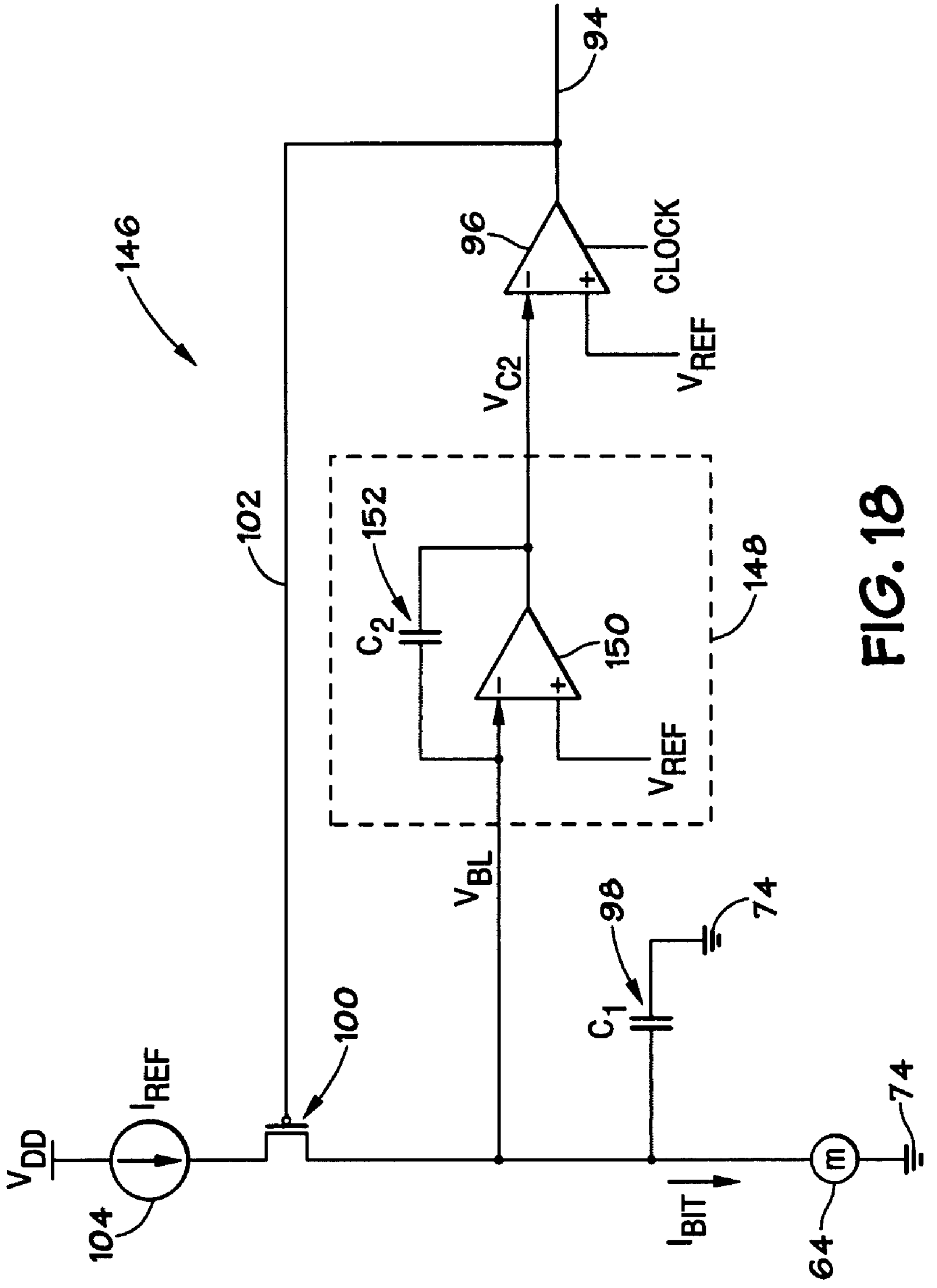

146
94
96
CLOCK
V_{REF}
V_{C2}
102
152
C_2
150
148
V_{REF}
V_{BL}
98
74
C_1
100
I_{REF}
V_{DD}
104
I_{BIT}
m
64
74

FIG. 18

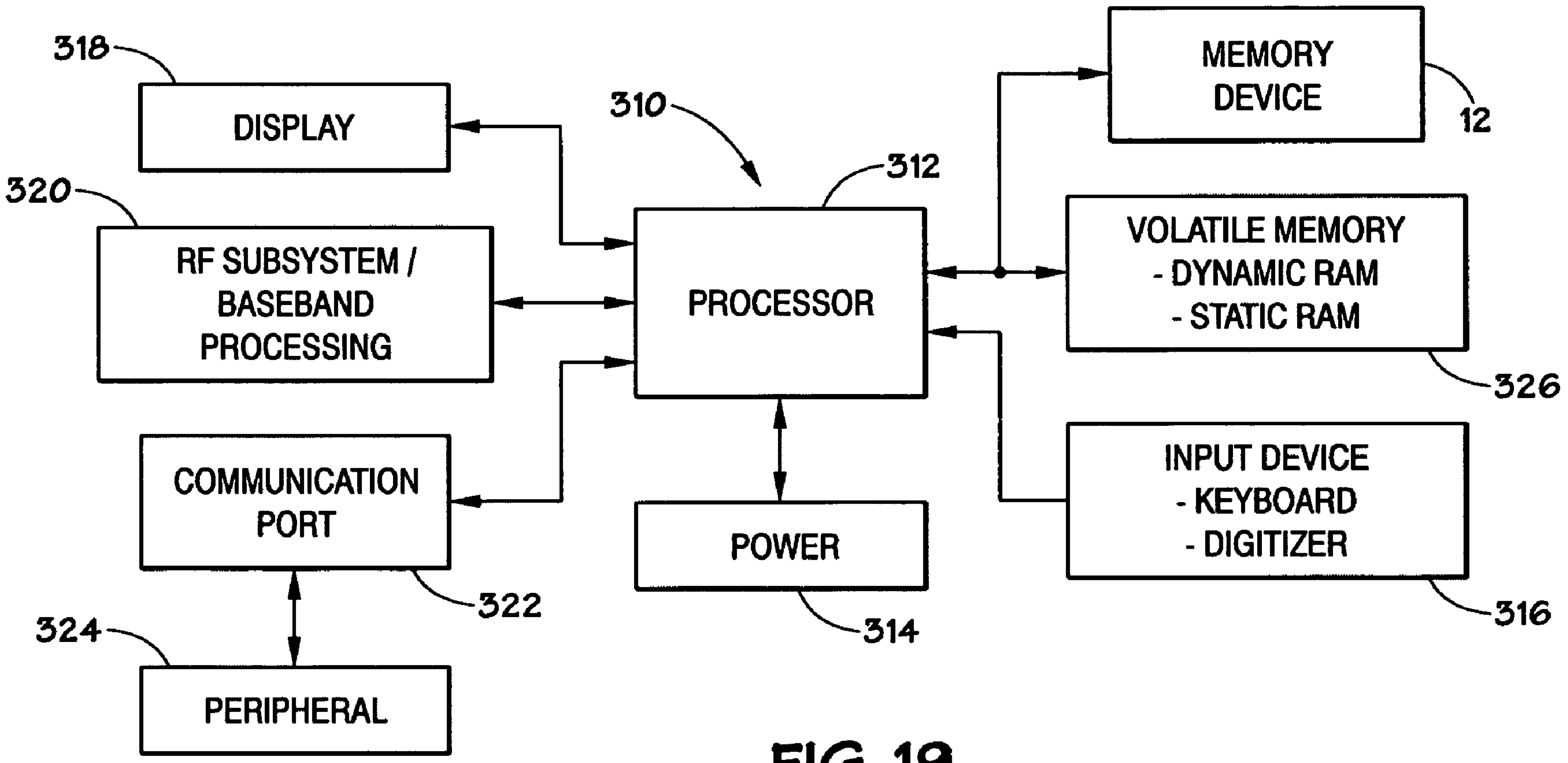

318
DISPLAY
310
312
PROCESSOR
MEMORY DEVICE
12
320
RF SUBSYSTEM / BASEBAND PROCESSING
VOLATILE MEMORY
- DYNAMIC RAM
- STATIC RAM
326
COMMUNICATION PORT
322
POWER
314
INPUT DEVICE
- KEYBOARD
- DIGITIZER
316
324
PERIPHERAL

FIG. 19

INTEGRATORS FOR DELTA-SIGMA MODULATORS

BACKGROUND

1. Field of Invention

Embodiments of the present invention relate generally to electronic devices and, more specifically, in one embodiment, to integrators for delta-sigma modulators in electronic devices.

2. Description of Related Art

Generally, memory devices include an array of memory elements and associated sense amplifiers. The memory elements store data, and the sense amplifiers read the data from the memory elements. To read data, for example, a current is passed through the memory element, and the current or a resulting voltage is measured by the sense amplifier. Conventionally, the sense amplifier measures the current or voltage by comparing it to a reference current or voltage. Depending on whether the current or voltage is greater than the reference, the sense amplifier outputs a value of one or zero. That is, the sense amplifier quantizes the analog signal from the memory element into one of two logic states.

Many types of memory elements are capable of assuming more than just two states. For example, some memory elements are capable of muti-bit (e.g., more than two state) storage. For instance, rather than outputting either a high or low voltage, the memory element may output four or eight different voltage levels, each level corresponding to a different data value. However, conventional sense amplifiers often fail to distinguish accurately between the additional levels because the difference between the levels (e.g., a voltage difference) in a multi-bit memory element is often smaller than the difference between the levels in a single-bit (i.e., two state) memory element. Thus, conventional sense amplifiers often cannot read multi-bit memory elements. This problem may be increased as high performance multi-bit memory elements become increasingly dense, thereby reducing the size of the memory elements and the difference between the levels (e.g., voltage) to be sensed by the sense amplifiers.

A variety of factors may tend to prevent the sense amplifier from discerning small differences in the levels of a multi-bit memory element. For instance, noise in the power supply, ground, and reference voltage may cause an inaccurate reading of the memory element. The noise may have a variety of sources, such as temperature variations, parasitic signals, data dependent effects, and manufacturing process variations. This susceptibility to noise often leads a designer to reduce the number of readable states of the memory element, which tends to reduce memory density and increase the cost of memory.

Conventional sense amplifiers present similar problems in imaging devices. In these devices, an array of light sensors output a current or voltage in response to light impinging upon the sensor. The magnitude of the current or voltage typically depends upon the intensity of the light. Thus, the capacity of the sense amplifier to accurately convert the current or voltage into a digital signal may determine, in part, the fidelity of the captured image. Consequently, noise affecting the sense amplifier may diminish the performance of imaging devices.

BRIEF DESCRIPTION OF DRAWINGS

FIG. **1** illustrates an electronic device in accordance with an embodiment of the present invention;

FIG. **2** illustrates a memory device in accordance with an embodiment of the present invention;

FIG. **3** illustrates a memory array in accordance with an embodiment of the present invention;

FIG. **4** illustrates a memory element in accordance with an embodiment of the present invention;

FIG. **5** illustrates I-V traces of memory elements storing different values, in accordance with an embodiment of the present invention;

FIG. **6** illustrates noise in the bit-line current during a read operation;

FIG. **7** illustrates a quantizing circuit in accordance with an embodiment of the present invention;

FIG. **8** illustrates a delta-sigma sensing circuit in accordance with an embodiment of the present invention;

FIGS. **9** and **10** illustrate current flow during operation of the quantizing circuit of FIG. **8**;

FIGS. **11**-**13** illustrate voltages in the quantizing circuit of FIG. **8** when sensing small, medium, and large currents, respectively;

FIG. **14** is a graph of bit-line current versus counter output for the quantizing circuit of FIG. **8**;

FIG. **15** is a graph of count versus quantizing circuit output in accordance with an embodiment of the present invention;

FIG. **16** is a block diagram of a delta-sigma modulator in accordance with an embodiment of the present invention;

FIG. **17** is a block diagram of a one-bit delta-sigma modulator in accordance with an embodiment of the present invention;

FIG. **18** illustrates an integrator in accordance with an embodiment of the present invention; and

FIG. **19** illustrates an example of a system including the memory device of FIG. **2**.

DETAILED DESCRIPTION OF SPECIFIC EMBODIMENTS

Various embodiments of the present invention are described below. In an effort to provide a concise description of these embodiments, not all features of an actual implementation are described in the specification. It should be appreciated that in the development of any such actual implementation, as in any engineering or design project, numerous implementation-specific decisions must be made to achieve the developers' specific goals, such as compliance with system-related and business-related constraints, which may vary from one implementation to another. Moreover, it should be appreciated that such a development effort might be complex and time consuming but would nevertheless be a routine undertaking of design, fabrication, and manufacture for those of ordinary skill having the benefit of this disclosure.

Some of the subsequently described embodiments may address one or more of the problems with conventional sense amplifiers discussed above. Some embodiments include a quantizing circuit configured to detect small differences in voltages and/or currents. As explained below, the quantizing circuit may sample the measured electrical parameter on multiple occasions and filter, e.g., average or sum, the samples to reduce the impact of noise. As a result, in some embodiments, the quantizing circuit may resolve small differences between voltage or current levels in multi-bit memory elements and/or light sensors, which may allow circuit designers to increase the number of bits stored per memory element and/or the sensitivity of an imaging device.

FIG. **1** depicts an electronic device **10** that may be fabricated and configured in accordance with one or more of the present embodiments. The illustrated electronic device **10** includes a memory device **12** that, as explained further below, may include multi-bit memory elements and quantizing circuits. Alternatively, or additionally, the electronic device **10** may include an imaging device **13** having the quantizing circuits.

Myriad devices may embody one or more of the present techniques. For example, the electronic device **10** may be a storage device, a communications device, an entertainment device, an imaging system, or a computer system, such as a personal computer, a server, a mainframe, a tablet computer, a palm-top computer, or a laptop.

FIG. **2** depicts a block diagram of an embodiment of the memory device **12**. The illustrated memory device **12** may include a memory array **14**, a quantizing circuit **16**, a column decoder **18**, a column address latch **20**, row drivers **22**, a row decoder **24**, row address latches **26**, and control circuitry **28**. As described below with reference to FIG. **3**, the memory array **14** may include a matrix of memory elements arranged in rows and columns. As will be appreciated, the imaging device **13** (FIG. **1**) may include similar features except that in the case of an imaging device **13**, the array **14** might comprise an array of imaging elements, such as complementary-metal-oxide semiconductor (CMOS) imaging elements or charge coupled devices (CCDs).

When accessing the memory elements, the control circuitry may receive a command to read from or write to a target memory address. The control circuitry **28** may then convert the target address into a row address and a column address. In the illustrated embodiment, the row address bus **30** transmits the row address to the row address latches **26**, and a column address bus **32** transmits column address to the column address latches **20**. After an appropriate settling time, a row address strobe (RAS) signal **34** (or other controlling clock signal) may be asserted by the control circuitry **28**, and the row address latches **26** may latch the transmitted row address. Similarly, the control circuitry **28** may assert a column address strobe **36**, and the column address latches **20** may latch the transmitted column address.

Once row and column addresses are latched, the row decoder **24** may determine which row of the memory array **14** corresponds to the latched row address, and the row drivers **22** may assert a signal on the selected row. Similarly, the column decoder **18** may determine which column of the memory array **14** corresponds with the latched column address, and the quantizing circuit **16** may quantize (e.g., sense) a voltage or current on the selected column. Additional details of reading and writing are described below.

FIG. **3** illustrates an example of a memory array **14**. The illustrated memory array **14** includes a plurality of bit-lines **38**, **40**, **42**, **44**, and **46** (also referred to as BL**0**-BL**4**) and a plurality of word-lines **48**, **50**, **52**, **54**, **56**, **58**, **60**, and **62** (also referred to as WL**0**-WL**7**). These bit-lines and word-lines are examples of electrical conductors. The memory array **14** further includes a plurality of memory elements **64**, each of which may be arranged to intersect one of the bit-lines and one of the word-lines. In other embodiments, imaging elements may be disposed at each of these intersections.

The memory elements and imaging elements may be referred to generally as data locations, i.e., devices or elements configured to convey data, either stored or generated by a sensor, when sensed by a sensing circuit, such as the quantizing circuits discussed below. The data locations may be formed on an integrated semiconductor device (e.g., a device formed on a single crystal of silicon) that also includes the other components of the memory device **12** (or imaging device **13**).

In some embodiments, the illustrated memory elements **64** are flash memory devices. The operation of the flash memory elements is described further below with reference to the FIGS. **4** and **5**. It should be noted that, in other embodiments, the memory elements **64** may include other types of volatile or nonvolatile memory. For example, the memory elements **64** may include a resistive memory, such as a phase change memory or magnetoresistive memory. In another example, the memory elements **64** may include a capacitor, such as a stacked or trench capacitor. Some types of memory elements **64** may include an access device, such as a transistor or a diode associated with each of the memory elements **64**, or the memory elements **64** may not include an access device, for instance in a cross-point array.

FIG. **4** illustrates a circuit **66** that models the operation of an arbitrarily selected memory element **64**, which is disposed at the intersection of WL**3** and BL**0**. This circuit **66** includes a capacitor **68**, a pre-drain resistor **70** (R_{PD}), a post-source resistor **72** (R_{PS}), and a ground **74**. The resistors **70** and **72** model the other devices in series with the memory element **64** being sensed. The illustrated memory element **64** includes a gate **76**, a floating gate **78**, a drain **80**, and a source **82**. In the circuit **66**, the drain **80** and source **82** are disposed in series between the pre-drain resistor **70** and the post-source resistor **72**. The gate **76** is connected to WL**3**. The pre-drain resistor **70**, the drain **80**, the source **82**, and the post-source resistor **72** are disposed in series on the bit-line BL**0**. The capacitor **68**, which models the capacitance of the bit-line, has one plate connected to ground **74** and another plate connected to the bit-line BL**0**, in parallel with the memory elements **64**.

Several of the components of the circuit **66** represent phenomenon affecting the memory elements **64** when it is sensed. The pre-drain resistor **70** generally represents the drain-to-bitline resistance of the memory elements **64** connected to the bit-line above (i.e., up current from) WL**3** when these memory elements **64** are turned on, (e.g., during a read operation). Similarly, the post source resistor **72** generally corresponds to the source-to-ground resistance of the memory elements **64** connected to the bit-line below WL**3** when the memory element **64** is sensed. The circuit **66** models electrical phenomena associated with reading the memory elements **64** at the intersection of WL**3** and BL**0**.

The operation of the memory elements **64** will now be briefly described with reference to FIGS. **4** and **5**. FIG. **5** illustrates one potential relationship between the bit-line current (I_{BIT}), the word-line voltage (V_{WL}), and the voltage of the floating gate **78** (V_{FG}). As illustrated by FIG. **5**, V_{FG} affects the response of the memory element **64** to a given V_{WL}. Decreasing the voltage of the floating gate shifts the I-V curve of the memory elements **64** to the right. That is, the relationship between the bit-line current and a word-line voltage depends on the voltage of the floating gate **78**. The memory elements **64** may store data by exploiting this effect.

To write data to the memory elements **64**, a charge corresponding to the data may be stored on the floating gate **78**. The charge of the floating gate **78** may be modified by applying voltages to the source **82**, drain **80**, and/or gate **76** such that the resulting electric fields produce phenomenon like Fowler-Northam tunneling and/or hot-electron injection near the floating gate **78**. Initially, the memory elements **64** may be erased by applying a word-line voltage designed to drive electrons off of the floating gate **78**. In some embodiments, an entire column or block of memory elements **64** may be erased generally simultaneously. Once the memory elements **64** are erased, the gate **76** voltage may be manipulated to drive a charge onto the floating gate **78** that is indicative of a data value. After the write operation ends, the stored charge may remain on the floating gate **78** (i.e., the memory elements **64** may store data in a nonvolatile fashion).

As illustrated by FIG. **5**, the value stored by the memory element **64** may be read by applying a voltage, V_{WL}, to the gate **76** and quantizing (e.g., categorizing) a resulting bit-line current, I_{BIT}. Each of the I-V traces depicted by FIG. **5** correspond to a different charge stored on the floating gate, V_{FG}, which should not be confused with the voltage that is applied to the gate, V_{WL}. The difference in floating gate **70** voltage, V_{FG}, between each I-V trace is an arbitrarily selected scaling factor "x." The illustrated I-V traces correspond to eight-different data values stored by the memory element **64**, with a V_{FG} of 0x representing a binary data value of 000, a V_{FG} of 1x representing a binary data value of 001, and so on through V_{FG} of 7x, which represents a binary data value of 111. Thus, by applying a voltage to the gate **76** and measuring the resulting bit-line current, the charge stored on the floating gate **78** may be sensed, and the stored data may be read.

The accuracy with which the bit-line current is quantized may affect the amount of data that a designer attempts to store in each memory element **64**. For example, in a system with a low sensitivity, a single bit may be stored on each memory element **64**. In such a system, a floating gate voltage V_{FG} of 0x may represent a binary value of 0, and a floating gate voltage V_{FG} of −7x may represent a binary value of one. Thus, the difference in floating gate voltages V_{FG} corresponding to different data values may be relatively large, and the resulting differences and bit-line currents for different data values may also be relatively large. As a result, even low-sensitivity sensing circuitry may quantize (e.g., discern) these large differences in bit-line current during a read operation. In contrast, high-sensitivity sensing circuitry may facilitate storing more data in each memory element **64**. For instance, if the sensing circuitry can distinguish between the eight different I-V traces depicted by FIG. **5**, then the memory elements **64** may store three bits. That is, each of the eight different charges stored on the floating gate **78** may represent a different three-bit value: 000, 001, 010, 011, 100, 101, 110, or 111. Thus, circuitry that precisely quantizes the bit-line current I_{BIT} may allow a designer to increase the amount of data stored in each memory element **64**.

However, as mentioned above, a variety of effects may interfere with accurate measurement of the bit-line current. For instance, the position of the memory elements **64** along a bit-line may affect R_{PD} and R_{PS}, which may affect the relationship between the word-line voltage V_{WL} and the bit-line current I_{BIT}. To illustrate these effects, FIG. **6** depicts noise on the bit-line while reading from the memory element **64**. As illustrated, noise in the bit-line current I_{BIT} may cause the bit-line current I_{BIT} to fluctuate. Occasionally, the fluctuation may be large enough to cause the bit-line current I_{BIT} to reach a level that represents a different stored data value, which could cause the wrong value to be read from the memory elements **64**. For instance, if the bit-line current is sensed at time **84**, corresponding to an arbitrarily selected peak, a data value of 100 may be read rather than the correct data value of 011. Similarly, if the bit-line current is sensed at time **86**, corresponding to an arbitrarily selected local minimum, a data value of 010 may be read rather than a data value of 011. Thus, noise on the bit-line may cause erroneous readings from memory elements **64**.

FIG. **7** depicts a quantizing circuit **16** that may tend to reduce the likelihood of an erroneous reading. The illustrated quantizing circuit **16** includes an analog-to-digital converter **88** and a digital filter **90** connected to each of the bit-lines **38**, **40**, **42**, **44**, and **46**, respectively. Each bit-line **38**, **40**, **42**, **44**, and **46** may connect to a different analog-to-digital converter **88** and digital filter **90**. The digital filters **90**, in turn, may connect to an input/output bus **92**, which may connect to a column decoder **18**, a column address latch **20**, and/or control circuitry **28** (see FIG. **2**).

In operation, the quantizing circuit **16** may quantize (e.g., digitize) analog signals from the memory elements **64** in a manner that is relatively robust to noise. As explained below, the quantizing circuit **16** may do this by converting the analog signals into a bit-stream and digitally filtering high-frequency components from the bit-stream.

The analog-to-digital converter **88** may be a one-bit, analog-to-digital converter or a multi-bit, analog-to-digital converter. In the present embodiment, an analog-to-digital converter **88** receives an analog signal from the memory element **64**, e.g., a bit-line current I_{BIT} or a bit-line voltage V_{BL}, and outputs a bit-stream that represents the analog signal. The bit-stream may be a one-bit, serial signal with a time-averaged value that generally represents the time-averaged value of the analog signal from the memory element **64**. That is, the bit-stream may fluctuate between values of zero and one, but its average value, over a sufficiently large period of time, may be proportional to the average value of the analog signal from the memory element **64**. In certain embodiments, the bit-stream from the analog-to-digital converter **88** may be a pulse-density modulated (PDM) version of the analog signal. The analog-to-digital converter **88** may transmit the bit-stream to the digital filter **90** on a bit-stream signal path **94**.

The digital filter **90** may digitally filter high-frequency noise from the bit-stream. To this end, the digital filter **90** may be a low-pass filter, such as a counter, configured to average (e.g., integrate and divide by the sensing time) the bit-stream over a sensing time, i.e., the time period over which the memory element **64** is read. (Alternatively, in some embodiments, the digital filter **90** is configured to integrate the bit-stream without dividing by the sensing time.) As a result, the digital filter **90** may output a value that is representative of both the average value of the bit-stream and the average value of the analog signal from the memory element **64**. In some embodiments, the digital filter **90** is a counter, and the cut-off frequency of the digital filter **90** may be selected by adjusting the duration of the sensing time. In the present embodiment, increasing the sensing time will lower the cutoff frequency. That is, the frequency response of the digital filter **90** may be modified by adjusting the period of time over which the bit-stream is integrated and/or averaged before outputting a final value. The frequency response of the digital filter **90** is described further below with reference to FIG. **15**. For multi-bit memory elements **64**, the output from the digital filter **90** may be a multi-bit binary signal, e.g., a digital word that is transmitted serially and/or in parallel.

Advantageously, in certain embodiments, the quantizing circuit **16** may facilitate the use of multi-bit memory elements **64**. As described above, in traditional designs, the number of discrete data values that a memory element **64** stores may be limited by sense amps that react to noise. In contrast, the quantizing circuit **16** may be less susceptible to noise, and, as a result, the memory elements **64** may be configured to store additional data. Without the high frequency noise, the intervals between signals representative of different data values may be made smaller, and the number of data values stored by a given memory element **64** may be increased. Thus, beneficially, the quantizing circuit **16** may read memory elements **64** that store several bits of data, e.g., 2, 3, 4, 5, 6, 7, 8, or more bits per memory element **64**.

Although the quantizing circuit **16** may sense the signal from the memory element **64** over a longer period of time than conventional designs, the overall speed of the memory device

12 may be improved. As compared to a conventional device, each read or write operation of the memory device **12** may transfer more bits of data into or out of the memory element **64**. As a result, while each read or write operation may take longer, more data may be read or written during the operation, thereby improving overall performance. Further, in some memory devices **12**, certain processes may be performed in parallel with a read or write operation, thereby further reducing the overall impact of the longer sensing time. For example, in some embodiments, the memory array **14** may be divided into banks that operate at least partially independently, so that, while data is being written or read from one bank, another bank can read or write data in parallel.

FIG. **8** illustrates details of one implementation of the quantizing circuit **16**. In this embodiment, the digital filter **90** is a counter, and the analog-to-digital converter **88** is a first-order delta-sigma modulator. The illustrated delta-sigma modulator **88** may include a latched comparator **96**, a capacitor **98**, and a switch **100**. In other embodiments, other types of digital filters and analog-to-digital converters may be employed, such as those described below in reference to FIGS. **17** and **18**.

As illustrated, an input of the counter **90** may connect to the bit-stream signal path **94**, which may connect to an output of the comparator **96**. The output of the comparator **96** may also connect to a gate of the switch **100** by a feedback signal path **102**. The output terminal (e.g., source or drain) of the switch **100** may connect in series to one of the bit-lines **38**, **40**, **42**, **44**, or **46**, and the input terminal of the switch **100** may connect to a reference current source **104** (I_{REF}). One plate of the capacitor **98** may connect to one of the bit-lines **38**, **40**, **42**, **44**, or **46**, and the other plate of the capacitor **98** may connect to ground.

The illustrated counter **90** counts the number of clock cycles that the bit-stream **94** is at a logic high value or logic low value during the sensing time. The counter may count up or count down, depending on the embodiment. In some embodiments, the counter **90** may do both, counting up one for each clock cycle that the bit-stream has a logic high value and down one for each clock cycle that the bit-stream has a logic low value. Output terminals (D**0**-D**5**) of the counter **90** may connect to the input/output bus **92** for transmitting the count. The counter **90** may be configured to be reset to zero or some other value when a reset signal is asserted. In some embodiments, the counter **90** may be a series connection of D-flip flops, e.g., D-flip flops having SRAM or other memory for storing an initial value and/or values to be written to the memory element **64**.

In the illustrated embodiment, the clocked comparator **96** compares a reference voltage (V_{REF}) to the voltage of one of the bit-lines **38**, **40**, **42**, **44**, or **46** (V_{BL}), which may be generally equal to the voltage of one plate of the capacitor **98**. The comparator **96** may be clocked (e.g., falling and/or rising edge triggered), and the comparison may be performed at regular intervals based on the clock signal, e.g., once per clock cycle. Additionally, the comparator **96** may latch, i.e., continue to output, values (V_{FB}) between comparisons. Thus, when the clock signals the comparator **96** to perform a comparison, if V_{BL} is less than V_{REF}, then the comparator **96** may latch its output to a logic low value, as described below in reference to FIG. **9**. Conversely, if V_{BL} is greater than V_{REF}, then the comparator **96** may latch a logic high value on its output, as described below in reference to FIG. **10**. As a result, the illustrated comparator **96** outputs a bit-stream that indicates whether V_{BL} is larger than V_{REF}, where the indication is updated once per clock cycle.

Advantageously, in some embodiments, the quantizing circuit **16** may include a single comparator (e.g., not more than one) for each column of multi-level memory elements **64**. In contrast, conventional sense amplifiers often include multiple comparators to read from a multi-bit memory cell, thereby potentially increasing device complexity and cost.

The capacitor **98** may be formed by capacitive coupling of the bit-lines **38**, **40**, **42**, **44**, and **46**. In other designs, this type of capacitance is referred to as parasitic capacitance because it often hinders the operation of the device. However, in this embodiment, the capacitor **98** may be used to integrate differences between currents on the bit-lines **38**, **40**, **42**, **44**, or **46** and the reference current to form the bit-stream, as explained further below. In some embodiments, the capacitor **98** may be supplemented or replaced with an integrated capacitor that provides greater capacitance than the “parasitic” bit-line capacitance.

The illustrated switch **100** selectively transmits current I_{REF} from the reference current source **104**. In various embodiments, the switch **100** may be a PMOS transistor (as illustrated in FIGS. **8-10**) or an NMOS transistor (as illustrated in FIG. **17**) controlled by the V_{FB} signal on the feedback signal path **102**.

The operation of the quantizing circuit **16** will now be described with reference to FIGS. **9-12**. Specifically, FIGS. **9** and **10** depict current flows in the quantizing circuit **16** when the comparator **96** is latched low and high, respectively. FIG. **11** illustrates V_{BL}, the bit-stream output from the comparator **96**, and the corresponding increasing count of the counter **90** for a relatively small bit-line current. FIG. **12** depicts the same voltages when measuring a medium sized bit-line current, and FIG. **13** depicts these voltages when measuring a relatively large bit-line current.

To sense the current through the memory element **64**, the illustrated delta-sigma modulator **88** exploits transient effects to output a bit-stream representative of the bit-line current I_{BIT}. Specifically, the delta-sigma modulator **88** may repeatedly charge and discharge the capacitor **98** with a current divider that subtracts the bit-line current I_{BIT} from the reference current I_{REF}. Consequently, a large current through the memory element **64** may rapidly discharge the capacitor **98**, and a small current through the memory element **64** may slowly discharge the capacitor **98**.

To charge and discharge the capacitor **98**, the delta-sigma modulator **88** switches between two states: the state depicted by FIG. **9** (hereinafter “the charging state”) and the state depicted by FIG. **10** (hereinafter “the discharging state”). Each time the delta-sigma modulator **88** transitions between these states, the bit-stream changes from a logic high value to a logic low value or vice versa. The proportion of time that the delta-sigma modulator **88** is in the state illustrated by either FIGS. **9** or FIG. **10** may be proportional to the size of the bit-line current I_{BIT} through the memory element **64**. The larger the bit-line current I_{BIT}, the more time that the delta-sigma modulator **88** is in the state illustrated by FIG. **9**, rather than the state illustrated by FIG. **10**, and the more time that the bit-stream has a logic low value.

Starting with the charging state (FIG. **9**), the capacitor **98** may initially accumulate a charge (e.g., become more charged). To this end, the output of the comparator **96** is latched to logic low, which, as mentioned above, may occur when V_{BL} is less than V_{REF}. The logic low may be conveyed to switch **100** by the feedback signal path **102**, and the switch **100** may close, thereby conducting the reference current I_{REF} through one of the bit-lines **38**, **40**, **42**, **44**, or **46**, as indicated by the larger arrows in FIG. **9**. A portion of the electrons flowing through the reference current source **104** may be accumulated by the capacitor **98**, as indicated by the smaller-horizontal arrows, and the remainder may be conducted through the memory element **64**, i.e., the bit-line current I_{BIT}, as indicated by the smaller vertical arrows. Thus, the capacitor **98** may accumulate a charge, and V_{BL} may increase.

The comparator **96** and the reference current source **104** may cooperate to charge the capacitor **98** for a discrete number of clock cycles. That is, when the delta-sigma modulator **88** transitions to the charging state, the delta-sigma modulator **88** may remain in this state for an integer number of clock cycles. In the illustrated embodiment, the comparator **96**, the output of which is latched, changes state no more than once per clock cycle, so the switch **100**, which is controlled by the output of the comparator **96**, V_{FB}, conducts current for a discrete number of clock cycles. As a result, the reference current source **104** conducts current I_{REF} through the bit-line and into the capacitor **98** for an integer number of clock cycles.

After each clock cycle of charging the capacitor **98**, the delta-sigma modulator **88** may transition from the charging state to the discharging state, which is illustrated by FIG. **10**, depending on the relative values of V_{BL} and V_{REF}. Once per clock cycle (or at some other appropriate interval, such as twice per clock cycle), the comparator **96** may compare the voltage of the capacitor V_{BL} to the reference voltage V_{REF}. If the capacitor **98** has been charged to the point that V_{BL} is greater than V_{REF}, then the output of the comparator **96** may transition to logic high, as illustrated in FIG. **10**. The logic high signal may be conveyed to the switch **100** by the feedback signal path **102**, thereby opening the switch **100**. As a result, the reference current source **104** may cease conducting current through the memory element **64** and into the capacitor **98**, and the capacitor **98** may begin to discharge through the memory element **64**.

In the present embodiment, the delta-sigma modulator **88** discharges the capacitor **98** for a discrete number of clock intervals. After each clock cycle of discharging the capacitor **98**, the delta-sigma modulator **88** compares V_{BL} to V_{REF}. If V_{BL} is still greater than V_{REF}, then the comparator **96** may continue to output a logic high signal, i.e., $V_{FB}=1$, and the switch **100** remains open. On the other hand, if enough current has flowed out of the capacitor **98** that V_{BL} is less than V_{REF}, then the comparator **96** may output a logic low signal, i.e., $V_{FB}=0$, and the switch **100** may close, thereby transitioning the delta-sigma modulator **88** back to the charging state and initiating a new cycle.

The counter **90** may count the number of clock cycles that the delta-sigma modulator **88** is in either the charging state or the discharging state by monitoring the bit-stream signal path **94**. The bit-stream signal path **94** may transition back and forth between logic high and logic low with the output of the comparator **96**, V_{FB}, and the counter **90** may increment and/or decrement a count once per clock cycle (or other appropriate interval) based on whether the bit-stream is logic high or logic low. After the sensing time has passed, the counter **90** may output a signal indicative of the count on output terminals **D0**-**D5**. As explained below, the count may correspond, e.g., proportionally, to the bit-line current, I_{BIT}.

FIGS. **11**-**13** illustrate voltages V_{FB} and V_{BL} in the quantizing circuit **16** when reading data from a memory element **64**. Specifically, FIG. **11** illustrates a low-current case, in which the value stored by the memory element **64** is represented by a relatively low bit-line current. Similarly, FIG. **12** illustrates a medium-current case, and FIG. **13** illustrates a high-current case. In each of these figures, the ordinate of the lower trace represents the voltage of the bit-stream signal path **94**, V_{FB}, and the ordinate of the upper trace illustrates the bit-line voltage, V_{BL}. The abscissa in each of the traces represents time, with the lower trace synchronized with the upper trace, and the duration of the time axes is one sensing time **106**.

As illustrated by FIG. **11**, the counter **90** is initially preset to zero (or some other appropriate value) by applying a reset signal. In some embodiments, the delta-sigma modulator **88** may undergo a number of start-up cycles to reach steady-state operation before initiating the sensing time and resetting the counter **90**. At the beginning of the illustrated read operation, the delta-sigma modulator **88** is in the charging state, which charges the capacitor **98** and increases V_{BL}, as indicated by dimension arrow **108**. At the beginning of the next clock cycle, the comparator **96** compares the bit-line voltage to the reference voltage and determines that the bit-line voltage is greater than the reference voltage. As a result, the bit-stream signal path **94** (V_{FB}) transitions to a logic high voltage, and the delta-sigma modulator **88** transitions to the discharging state. Additionally, the counter **90** increments the count by one to account for one clock cycle of the bit-stream signal **94** holding a logic low value. Next, the charge stored on the capacitor **98** drains out through the memory element **64**, and the bit-line voltage drops until the comparator **96** determines that V_{BL} is less than V_{REF}, at which point the cycle repeats. The cycle has a period **112**, which may be divided into a charging portion **114** and a discharging portion **116**. Once during each cycle in the sensing time **106**, the count stored in the counter **90** may increase by one. At the end of the sensing time **106**, the counter **90** may output the total count.

A comparison of FIG. **11** to FIGS. **12** and **13** illustrates why the count correlates with the bit-line current. In FIG. **13**, the high-current case, the stored charge drains from the capacitor **98** quickly, relative to the other cases, because the bit-line current I_{BIT} is large and, as a result, the delta-sigma modulator **88** spends more time in the charging state than the discharging state. As a result, the bit-stream has a logic low value for a large portion of the sensing time **106**, thereby increasing the count.

The capacitance of the capacitor **98** may be selected with both the clock frequency and the range of expected bit-line currents in mind. For example, the capacitor **98** may be large enough that the capacitor **98** does not fully discharge (e.g., saturate) when the bit-line current I_{BIT} is either at its lowest expected value or at its highest expected value. That is, in some embodiments, the capacitor **98** generally remains in a transient state while reading the memory element **64**. Similarly, the frequency at which the comparator **96** is clocked may affect the design of the capacitor **98**. A relatively high frequency clock signal may leave the capacitor **98** with relatively little time to discharge or saturate between clock cycles, thereby leading a designer to choose a smaller capacitor **98**.

Similarly, the size of the reference current may be selected with the range of expected bit-line currents in mind. Specifically, in certain embodiments, the reference current is less than the largest expected bit-line current I_{BIT}, so that, in the case of maximum bit-line current I_{BIT}, the capacitor **98** can draw charge from the reference current while the rest of the reference current flows through the memory element **64**.

FIG. **14** illustrates the relationship between the bit-line current I_{BIT} and the count for the presently discussed embodiment. As illustrated by FIG. **14**, the count corresponds with (e.g., is generally proportional to) the bit-line current I_{BIT}. This relationship is described by the following equation (Equation 1), in which N_{ST} represents the number of clock cycles during the sensing time:

$$I_{BIT}/I_{REF}=Count/N_{ST}$$

Thus, in the illustrated embodiment, the count corresponds with (e.g., is indicative of) the bit-line current I_{BIT}, which corresponds with the value stored by the memory element **64**.

Advantageously, the quantizing circuit **16** may quantize (e.g., categorize) the bit-line current I_{BIT} as falling into one of a large number of categories, each of which is represented by an increment of the count. In doing so, in some embodiments, the quantizing circuit **16** may resolve small differences in the bit-line current I_{BIT}. The resolution of the quantizing circuit **16** may be characterized by the following equation (Equation 2), in which I_{MR} represents the smallest resolvable difference in bit-line current I_{BIT}, i.e., the resolution of the quantizing circuit **16**:

$$I_{MR}=I_{REF}/N_{ST}$$

Thus, the resolution of the quantizing circuit **16** may be increased by increasing the sensing time or the clock frequency or by decreasing I_{REF}, which may limit the maximum cell current since I_{MR} is less than I_{REF}.

The resolution of the quantizing circuit **16** may facilitate storing multiple bits in the memory element **64** or sensing multiple levels of light intensity in an image sensor element. For example, if the quantizing circuit **16** is configured to quantize (e.g., categorize) the bit-line current I_{BIT} into one of four different levels, then the memory element **64** may store two-bits of data or, if the quantizing circuit **16** is configured to categorize the bit-line current I_{BIT} into one of eight different current levels, then the memory element **64** may store three-bits of data. For the present embodiment, the number of bits stored by the memory element **64** may be characterized by the following equation (Equation 3), in which N_B represents the number of bits stored by a memory element **64** and I_{RANGE} represents the range of programmable bit-line currents through the memory element **64**:

$$N_B=\log(I_{RANGE}/I_{MR})/\log 2$$

In short, in the present embodiment, greater resolution translates into higher density data storage for a given memory element **64**.

FIG. **15** is a graph that illustrates one way in which the counter **90** may be configured to further reduce the effects of noise. In FIG. **15**, the abscissa represents the count, and the ordinate represents the output of the quantizing circuit **16**. In the present embodiment, the three-least-significant digits of the count are disregarded as potentially corrupted by noise. That is, D**0**-D**2** (FIG. **8**) either do not connect to the input/output bus **92** or are not interpreted as conveying data that is stored by the memory element **64**. As a result, a range of counter values may represent a single data value stored by the memory element **64**. For example, in the present embodiment, count values ranging from 00 1000 to 00 1111 are construed as representing a data value of 001. Representing data in this manner may further reduce the effects of noise because, even if noise affects the count, in many embodiments, it would have to affect the count in a consistent manner over a substantial portion of the sensing time to affect the more significant digits of the count. That is, disregarding less significant digits may lower the cutoff frequency of the counter **90**. In other embodiments, fewer, more, or no digits may be truncated from the count as potentially representing noise.

Truncating less significant digits may introduce a rounding error, or a downward bias, in the output. This effect may be mitigated by presetting (e.g., driving latches to a particular state in advance of counting or storing a value in memory) the counter **90** in a manner that accounts for this bias. The counter **90** may be preset either before reading from the memory element **64** or before writing to the memory element **64**. In some embodiments, the preset value may be one-half of the size of the range of counter values that represent a single output value. In other words, if m digits are truncated from the output, then the counter **90** may be preset to one-half of 2^m before reading from a memory element **64** or before writing to the memory element **64**. In some embodiments, the memory in the counter **90** may store this preset value.

Delta-sigma modulators may be embodied by a variety of circuit topologies, including the one illustrated by FIG. **8**. Many of these topologies are depicted more generically by FIG. **16**, which is a block diagram of an example of a first-order delta-sigma modulator **120**. The illustrated delta-sigma modulator **120** includes an adder **122**, an integrator **124**, an analog-to-digital converter **126**, and a digital-to-analog converter **128**. The illustrated adder **122** receives an analog input signal **130** and a feedback signal **132** from the digital-to-analog converter **128**. The illustrated adder **122** outputs a delta signal **134** to an input of the integrator **124**, which outputs a sigma signal **136** to an input of the analog-to-digital converter **126**. The analog-to-digital converter **126** also receives a reference signal **138**. The analog-to-digital converter **126** outputs a digital output signal **140**, which is received by an input to the digital-to-analog converter **128**.

Less generically but still depicting a variety of topologies, FIG. **17** is a block diagram of an example of a one-bit delta-sigma modulator **142**, which may embody the delta-sigma modulator **120** illustrated by FIG. **16**, and which may be embodied by the delta-sigma modulator **88** illustrated by FIG. **8**. In this example, the integrator **124** is a capacitor and the analog-to-digital converter **126** is a comparator. The reference signal **138** is a voltage V_{REF}, and the digital-to-analog converter **128** includes a switch **144** and a reference current source **146**.

In operation, the illustrated delta-sigma modulators **120** and **142** sense the analog input signal **130** by integrating a difference between the analog input signal **130** and the feedback signal **132** and exercising feedback control over this integrated difference. The smaller the difference, the stronger or the more frequent the feedback signal **132**. For instance, in the embodiment of FIG. **8**, the difference between the bit-line current I_{BIT} and the reference current I_{REF} is integrated by the voltage of the capacitor **98**, and the comparator **96** controls this voltage by outputting feedback **102**, which is converted to an analog feedback signal by the current switch **100** and reference current source **104**. In certain embodiments, if the difference between the analog feedback signal **132** (FIGS. **16** and **17**) and the analog input signal **130** is accurately measured and integrated, the proportion of time that the feedback signal **132** is applied (and the proportion of time that the digital output **140** is logic high or low) is indicative of the analog input signal **130**. Thus, consistently integrating this difference may improve the correlation between the digital output **140** and the analog input **130**, thereby potentially improving the accuracy of the quantizing circuit **16**.

Several phenomena may prevent the delta-sigma modulators **120** and **142** from accurately integrating the difference between the analog input signal **130** and the analog feedback signal **132**. For example, if the adder **122** overloads the digital-to-analog converter **128**, the analog feedback signal **132** may not accurately reflect the digital output **140**, and the difference being integrated may be inaccurate. In another example, the sigma signal **136** output from the integrator **124** may saturate the integrator **124** (i.e., the sigma signal **136** may reach a maximum or minimum of the integrator **124**). For instance, in the delta-sigma modulator **88** of FIG. **8**, the bit-line voltage V_{BL} may drop to ground, thereby preventing the capacitor **98** from integrating the difference between the bit-line current I_{BIT} and the reference current I_{REF} by storing a charge. Similarly, the voltage of the bit-line V_{BL} may rise to the voltage source of the reference current source **104** (e.g., V_{DD}), and the reference current I_{REF} may stop flowing, thereby preventing the capacitor **98** from integrating a difference between the reference current I_{REF} and the bit-line current I_{BIT}. In some embodiments, the correspondence between the digital output **140** and the analog input **130** may be weakened when the integrator **124** (FIGS. **16** and **17**) is not integrating, and the accuracy of the quantizing circuit **16** may be compromised.

FIG. **18** illustrates an example of a delta-sigma modulator **146** with an integrator **148** that may have a wider range than other designs. The illustrated integrator **148** includes a differential amplifier **150** and a capacitor **152**. The non-inverting input of the differential amplifier **150** is connected to the reference voltage V_{REF}, and the inverting input is connected to the bit-line voltage V_{BL}. The output of the differential amplifier **150** is connected to an input of the comparator **96**. The plates of the capacitor **152** are each connected to either the bit-line or the output of the differential amplifier **150**.

In operation, the integrator **148** may integrate the difference between the bit-line voltage V_{BL} and the reference voltage V_{REF}, while holding the bit-line voltage V_{BL} generally constant. In the present embodiment, if the bit-line voltage V_{BL} rises above the reference voltage V_{REF}, the output of the differential amplifier V_{C2} falls negative at a generally linear rate, thereby both charging the capacitor **152** and counteracting the change in the bit-line voltage V_{BL} via the capacitor **152**. On the other hand, if the bit-line voltage V_{BL} drops below the reference voltage V_{REF}, the output of the differential amplifier V_{C2} rises at a generally linear rate, thereby both discharging the capacitor **152** and counteracting the change in the bit-line voltage V_{BL}. Thus, in the present embodiment, the voltage of the output of the differential amplifier V_{C2} represents the integral of the difference between the bit-line voltage V_{BL} and the reference voltage V_{REF} over time. The operation of the integrator **148** may be characterized by the following equation (Equation 5), in which t represents time, C_2 represents the capacitance of the capacitor **152**, and $V_{C2\,(t=0)}$ represents the voltage of the output of the differential amplifier V_{C2} at time zero:

$$V_{C2} = \int_o^t \frac{(V_{BL} + V_{Ref})}{C_2} + V_{C2(t=0)}$$

The comparator **96** may control the output of the differential amplifier V_{C2} relative to the reference voltage V_{REF} by attempting to keep $V_{C2}>V_{REF}$ or by attempting to keep $V_{C2}<V_{REF}$. In the illustrated embodiment, when V_{C2} drops below the reference voltage V_{REF}, the output of the comparator **96** transitions to a logic low value, and the current switch **100** turns on, thereby conducting the reference current I_{REF} through the bit-line. The reference current I_{REF} may cause the bit-line voltage V_{BL} increase, which the differential amplifier **150** may counteract by increasing its output V_{C2} and charging the capacitor **152**. As a result, V_{C2} increases. On the other hand, when the comparator **96** detects that V_{C2} is greater than the reference voltage V_{REF}, its output may transition to logic high, thereby stopping the flow of the reference current I_{REF} and causing the bit-line voltage V_{BL} to decrease, which the differential amplifier **150** counteracts by lowering its output voltage V_{C2} and discharging the capacitor **152**. Thus, V_{C2}

decreases until it drops below V_{REF} and the cycle repeats. As a result, in the present embodiment, the integrator **148** integrates the difference between the bit-line voltage V_{BL} and the reference voltage V_{REF}, and the comparator **96** outputs a bit-stream **94** (or the digital output **140** of FIGS. **16** and **17**) that is a pulse-density modulated representation of the bit-line current I_{BIT}.

Advantageously, the present embodiment may decouple the bit-line voltage V_{BL} from the measurement of the bit-line current I_{BIT}. As a result, in some embodiments, the design of the delta-sigma modulator **146** may not be constrained by the capacitance of the capacitor **98**, which may be a parasitic capacitance subject to the physical dimensions of the bit-line. The range of the integrator **148** may be selected with the range of potential bit-line currents I_{BIT} in mind, and the risk of the integrator **148** saturating may be reduced, which may tend to improve the reliability and accuracy of the delta-sigma modulator **146**.

In some embodiments, the capacitor **152** may be connected to a reset transistor, with one terminal of the reset transistor connected to one plate of the capacitor **152** and the other terminal of the reset transistor connected to the other plate of the capacitor **152**. The gate of the reset transistor may be controlled by a reset signal. In this embodiment, the capacitor **152** may be discharged, for example between reading from memory elements **64**, by asserting the reset signal. Advantageously, resetting the capacitor **152** may initialize the delta-sigma modulator **146** to a known state, so that the delta-sigma modulator **146** reaches steady-state operation within a predictable period of time.

FIG. **19** depicts an example of a processor-based system **310** that includes the memory device **12** (FIG. **2**). Alternatively or additionally, the system **310** may include the imaging device **13**. The system **310** may be any of a variety of types such as a computer, pager, cellular phone, personal organizer, control circuit, etc. In a typical processor-based system, one or more processors **312**, such as a microprocessor, control the processing of system functions and requests in the system **310**. The processor **312** and other subcomponents of the system **310** may include quantizing circuits, such as those discussed above.

The system **310** typically includes a power supply **314**. For instance, if the system **310** is a portable system, the power supply **314** may advantageously include a fuel cell, permanent batteries, replaceable batteries, and/or rechargeable batteries. The power supply **314** may also include an AC adapter, so the system **310** may be plugged into a wall outlet, for instance. The power supply **314** may also include a DC adapter such that the system **310** may be plugged into a vehicle cigarette lighter, for instance.

Various other devices may be connected to the processor **312** depending on the functions that the system **310** performs. For instance, a user interface **316** may be connected to the processor **312**. The user interface **316** may include buttons, switches, a keyboard, a light pen, a mouse, a digitizer and stylus, and/or a voice recognition system, for instance. A display **318** may also be connected to the processor **312**. The display **318** may include an LCD, an SED display, a CRT display, a DLP display, a plasma display, an OLED display, LEDs, and/or an audio display, for example. Furthermore, an RF sub-system/baseband processor **320** may also be connected to the processor **312**. The RF sub-system/baseband processor **320** may include an antenna that is connected to an RF receiver and to an RF transmitter (not shown). One or more communication ports **322** may also be connected to the processor **312**. The communication port **322** may be adapted to be connected to one or more peripheral devices **324** such as a modem, a printer, a computer, or to a network, such as a local area network, remote area network, intranet, or the Internet, for instance.

The processor **312** generally controls the system **310** by implementing software programs stored in the memory. The memory is operably connected to the processor **312** to store and facilitate execution of various programs. For instance, the processor **312** may be connected to the volatile memory **326** which may include Dynamic Random Access Memory (DRAM) and/or Static Random Access Memory (SRAM). The volatile memory **326** is typically large so that it can store dynamically loaded applications and data. As described further below, the volatile memory **326** may be configured in accordance with embodiments of the present invention.

The processor **312** may also be connected to the memory device **12**. The memory device **12** may include a read-only memory (ROM), such as an EPROM, and/or flash memory to be used in conjunction with the volatile memory **326**. The size of the ROM is typically selected to be just large enough to store any necessary operating system, application programs, and fixed data. Additionally, the non-volatile memory **328** may include a high capacity memory such as a tape or disk drive memory.

The memory device **10** and volatile memory **326** may store various types of software, such as an operating system or office productivity suite including a word processing application, a spreadsheet application, an email application, and/or a database application. These programs may be stored on a variety of tangible machine readable mediums.

While the invention may be susceptible to various modifications and alternative forms, specific embodiments have been shown by way of example in the drawings and have been described in detail herein. However, it should be understood that the invention is not intended to be limited to the particular forms disclosed. Rather, the invention is to cover all modifications, equivalents, and alternatives falling within the spirit and scope of the invention as defined by the following appended claims.

What is claimed is:

1. An electronic device, comprising:

a plurality of data locations, wherein the plurality of data locations each comprise a floating gate transistor, a phase change memory element, or a light sensor; and

a delta-sigma modulator connected to the data locations, wherein the delta-sigma modulator comprises an integrator having a differential amplifier.

2. The electronic device of claim **1**, wherein the delta-sigma modulator comprises a comparator with an input connected to an output of the differential amplifier.

3. The electronic device of claim **1**, wherein an output of the delta-sigma modulator is connected to a counter.

4. The electronic device of claim **1**, wherein an input of the differential amplifier is connected to the plurality of data locations.

5. The electronic device of claim **4**, wherein the input of the differential amplifier is also connected to a plate of a capacitor.

6. The electronic device of claim **5**, wherein another plate of the capacitor is connected to the output of the differential amplifier.

7. The electronic device of claim **6**, wherein another input of the differential amplifier is connected to a reference voltage, and wherein the reference voltage is also connected to an input of a comparator.

8. The electronic device of claim **7**, wherein the comparator has another input connected to the output of the differential amplifier.

9. The electronic device of claim **8**, wherein an output of the comparator is connected to a counter.

10. An electronic device, comprising:

a plurality of data locations; and

a delta-sigma modulator connected to the data locations, wherein the delta-sigma modulator comprises an integrator having a differential amplifier, wherein an input of the differential amplifier is connected to the plurality of data locations.

11. The electronic device of claim **10**, wherein the input of the differential amplifier is also connected to a plate of a capacitor.

12. The electronic device of claim **11**, wherein another plate of the capacitor is connected to the output of the differential amplifier.

13. The electronic device of claim **12**, wherein another input of the differential amplifier is connected to a reference voltage, and wherein the reference voltage is also connected to an input of a comparator.

14. The electronic device of claim **13**, wherein the comparator has another input connected to the output of the differential amplifier.

15. The electronic device of claim **14**, wherein an output of the comparator is connected to a counter.

16. An electronic device, comprising:

a plurality of data locations; and

a delta-sigma modulator connected to the data locations, wherein the delta-sigma modulator comprises an integrator having a differential amplifier, wherein the delta-sigma modulator comprises a comparator with an input connected to an output of the differential amplifier.

17. The device of claim **16**, wherein the plurality of data locations comprise flash memory, phase change memory, magnetoresistive memory, or photo-diodes.

18. The electronic device of claim **16**, wherein an output of the delta-sigma modulator is connected to a counter.

19. The electronic device of claim **16**, wherein an input of the differential amplifier is connected to the plurality of data locations.

20. The electronic device of claim **19**, wherein the input of the differential amplifier is also connected to a plate of a capacitor.

21. The electronic device of claim **20**, wherein another plate of the capacitor is connected to the output of the differential amplifier.

22. The electronic device of claim **21**, wherein another input of the differential amplifier is connected to a reference voltage, and wherein the reference voltage is also connected to an input of a comparator.

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